(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 193 325 A1

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
19.07.2017 Bulletin 2017/29

(51) Int Cl.:
G09G 3/36 *(2006.01)* ***G11C 19/00*** *(2006.01)*

(21) Application number: **16207554.3**

(22) Date of filing: **30.12.2016**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
MA MD

(30) Priority: **30.12.2015 KR 20150190179**

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(54) **LIQUID CRYSTAL DISPLAY DEVICE**

(57) A liquid crystal display device includes a display panel including a display area (AA) and a non-display area (NAA). In the display area, m/2 (m is a positive even number) data lines (DL1 - DL5) of a first direction and 2n (n is an integer more than 5) gate lines (GL2 - GL7) of a second direction cross each other to thereby define m × n pixels (150). Two gate lines are disposed between two adjacent pixel rows, and two pixel columns are disposed between two adjacent two data lines. Furthermore 2n gate driver in panel (GIP) circuits are located in the display area, each including signal lines (QL) and transistors (T1-T5), wherein the signal lines and the transistors are separately disposed between the two pixel columns.

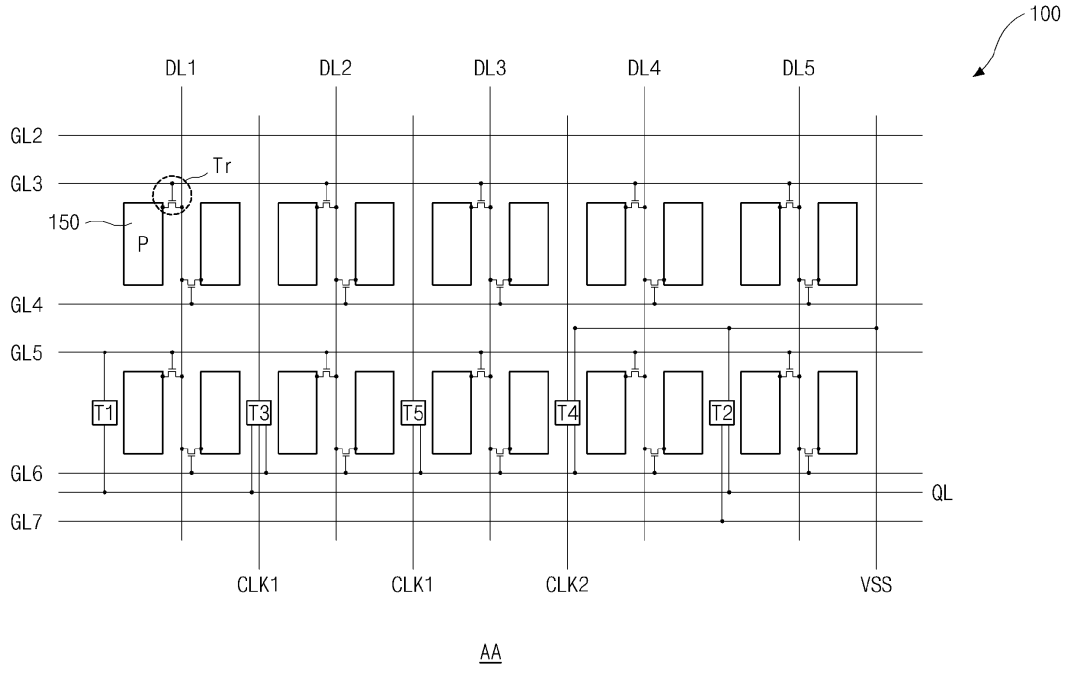

FIG. 5

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Description

BACKGROUND

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to a liquid crystal display device, and more particularly, to a liquid crystal display having a narrow bezel.

DISCUSSION OF THE RELATED ART

[0002] A liquid crystal display (LCD) device includes a display panel, a data driving unit for providing data signals to data lines of the display panel, a gate driving unit for providing gate signals to gate lines of the display panel, and a timing controller for controlling the data driving unit and the gate driving unit.

[0003] In the LCD device, the gate driving unit and the data driving unit are generally manufactured in an integrated circuit form and attached to the display panel in a TCP (tape carrier package) or COF (chip on film) type.

[0004] Therefore, the number of components increases, and manufacturing processes and costs also rise due to an increase in the number of components. This causes a problem in decreasing a weight and size of the LCD device. To solve the problem, a GIP (gate in panel) type LCD device, in which the gate driving unit is formed in the display panel, has been suggested.

[0005] FIG. 1 is a plan view of a display panel of a GIP type LCD device according to a related art.

[0006] In FIG. 1, a display panel 10 of a GIP type LCD device according to the related art includes a display area AA and non-display areas NAA. The non-display areas NAA are disposed at outer sides of the display area AA, for example, at left and right sides of the display area AA, respectively.

[0007] Here, pixels P defined by gate lines GL and data lines DL crossing each other are disposed in the display area AA of the display panel 10, and GIP circuits each including signal lines (not shown) and transistors (not shown) are disposed in respective non-display areas NAA.

[0008] Meantime, recently, in the LCD device, it is required to narrow a bezel, which is defined as a width of the non-display area NAA, with pursuing a light weight and thin thickness for a slim design of a final product such as monitors or TVs.

[0009] However, as stated above, in the GIP type LCD device according to the related art, since the GIP circuits GIP, each of which includes the signal lines (not shown) and the transistors (not shown), are formed in the non-display areas NAA at left and right sides of the display area AA, there is a limitation on achieving a narrow bezel.

SUMMARY

[0010] Accordingly, the present disclosure is directed to an LCD device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0011] An object of the present disclosure is to provide an LCD device that has a narrow bezel by disposing signal lines and transistors of a GIP circuit.

[0012] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings. The objects are solved by the features of the independent claim.

[0013] According to one aspect, there is provided a liquid crystal display device including a display panel including a display area and a non-display area, wherein in the display area, m/2 (m is a positive even number) data lines of a first direction and 2n (n is an integer more than 5) gate lines of a second direction cross each other to thereby define m $\times$ n pixels; and 2n GIP circuits in the display area and each including signal lines and transistors, wherein two gate lines are disposed between adjacent two pixel rows, and two pixel columns are disposed between adjacent two data lines, and wherein the signal lines and the transistors are separately disposed between the two pixel columns. Preferably, odd GIP circuits of the GIP circuits output odd gate lines of the gate lines, and even GIP circuits of the GIP circuits output even gate lines of the gate lines. Preferably, the signal lines include at least one of first and second clock signal lines, a start signal line, a reset signal line and a low level voltage line. Preferably, the signal lines are disposed on a same layer as the data lines. Preferably, the GIP circuit further includes first and second node lines. The first and second node lines may be disposed between adjacent two pixel rows. Preferably, the first and second node lines are spaced apart from the gate lines. Preferably, the first and second node lines are disposed on a same layer as the gate lines. Preferably, the first and second node lines overlap the gate lines. Preferably, the first and second node lines are disposed on a different layer from the gate lines. Preferably, the transistors include at least one of: a first transistor connected to the start signal line and the first node line; a second transistor connected to the first node line and the low level voltage line; a third transistor connected to the first clock signal line and the first node line; a fourth transistor connected to the second clock signal line, the low level voltage line and the third transistor; and a fifth transistor connected to the first clock signal line and the third transistor. Preferably, the liquid crystal display device further comprises a data driving unit in the non-display area and outputting data signals to the data lines.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to pro-

vide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a plan view of a display panel of a GIP type LCD device according to a related art;

FIG. 2 is a plan view of a display panel of a GIP type LCD device according to an embodiment of the present disclosure;

FIG. 3 is a schematic view of illustrating a plurality of GIP circuits according to the embodiment of the present disclosure;

FIG. 4 is a view of schematically illustrating the first GIP circuit according to the embodiment of the present disclosure; and

FIG. 5 is a view of a display panel including GIP circuits in a display area according to the embodiment of the present disclosure.

DETAILED DESCRIPTION

[0016] Reference will now be made in detail to the embodiment of the disclosure, an example of which is illustrated in the accompanying drawings.

[0017] FIG. 2 is a plan view of a display panel of a GIP type LCD device according to an embodiment of the present disclosure.

[0018] In FIG. 2, the display panel 100 of a GIP type LCD device according to the embodiment of the present disclosure includes a display area AA and non-display areas (not shown) at outer sides of the display area AA.

[0019] More specifically, a plurality of pixels (not shown), which are defined by a plurality of gate lines GL1 to GL6 and a plurality of data lines (not shown) crossing each other, are disposed in the display area AA of the display panel 100.

[0020] Particularly, a plurality of GIP circuits GIP1 to GIP6, each of which includes a plurality of signal lines (not shown) and a plurality of transistors (not shown), are disposed in the display area AA of the display panel 100.

[0021] In the embodiment of the present disclosure, a narrow bezel can be achieved by disposing the GIP circuits GIP1 to GIP6 in the display area AA while the GIP circuits are disposed in the non-display areas NAA of FIG. 1 at the left and right sides of the display area AA of FIG. 1 in the LCD device according to the related art. This will be described in more detail later.

[0022] Meanwhile, although more gate lines and GIP circuits may be disposed in the display area AA of the display panel 100, for convenience of explanation, six gate lines GL1 to GL6 and six GIP circuits GIP1 to GIP6 are shown in the figure.

[0023] At this time, odd GIP circuits GIP1, GIP3 and GIP5 of the GIP circuits GIP1 to GIP6 output gate signals to odd gate lines GL1, GL3 and GL5 of the gate lines GL1 to GL6, respectively, and even GIP circuits GIP2, GIP4 and GIP6 of the GIP circuits GIP1 to GIP6 output gate signals to even gate lines GL2, GL4 and GL6 of the gate lines GL1 to GL6, respectively.

[0024] In the meantime, although not shown in the figure, a data driving unit (not shown) may be further disposed in the non-display area (not shown) at an upper or lower side of the display area AA.

[0025] At this time, the data driving unit (not shown) outputs data signals to the data lines (not shown) in the display area AA.

[0026] FIG. 3 is a schematic view of illustrating a plurality of GIP circuits according to the embodiment of the present disclosure.

[0027] In FIG. 3, the GIP circuits GIP1, ..., GIP(i-1), GIP(i), GIP(i+1), ..., and GIP(j) respectively output gate signals Vout1, ..., Vout(i-1), Vout(i), Vout(i+1), ..., and Vout(j), each of which has one high level during a frame, wherein i is an integer larger than 2, and j is an integer larger than 4.

[0028] At this time, first GIP circuit to (j)th GIP circuit GIP1 to GIP(j) each receive at least one of a plurality of clock signals CLK1 and CLK2 and sequentially output the gate signals Vout1, ..., Vout(i-1), Vout(i), Vout(i+1), ..., and Vout(j) having the high level to the gate lines GL1, ..., GL(i-1), GL(i), GL(i+1), ..., and GL(j), respectively, wherein i is an integer larger than 2, and j is an integer larger than 4.

[0029] In addition, each of the plurality of clock signals CLK1 and CLK2 partially overlaps the next clock signal, and the plurality of clock signals CLK1 and CLK2 are sequentially and repeatedly applied to the GIP circuits GIP1, ..., GIP(i-1), GIP(i), GIP(i+1), ..., and GIP(j). For example, each of the plurality of clock signals CLK1 and CLK2 may overlap 2/3 of a high level section of the next clock signal. Here, although two clock signals CLK1 and CLK2 are used, the number of clock signals CLK1 and CLK2 are not limited to this.

[0030] The gate signals Vout1, ..., Vout(i-1), Vout(i), Vout(i+1), ..., and Vout(j), which are respectively outputted from the GIP circuits GIP1, ..., GIP(i-1), GIP(i), GIP(i+1), ..., and GIP(j), are sequentially provided to the gate lines GL1, ..., GL(i-1), GL(i), GL(i+1), ..., and GL(j) of a display panel (not shown) displaying images.

[0031] More specifically, the first GIP circuit GIP1 outputs the first gate signal Vout1 having the high level to the first gate line GL1, ..., the (i-1)th GIP circuit GIP(i-1) outputs the (i-1)th gate signal Vout(i-1) having the high level to the (i-1)th gate line GL(i-1), the (i)th GIP circuit GIP(i) outputs the (i)th gate signal Vout(i) having the high level to the (i)th gate line GL(i), the (i+1)th GIP circuit GIP(i+1) outputs the (i+1)th gate signal Vout(i+1) having the high level to the (i+1)th gate line GL(i+1), ..., and the (j)th GIP circuit GIP(j) outputs the (j)th gate signal Vout(j)

having the high level to the (j)th gate line GL(j).

[0032] First, since there is no previous GIP circuit before the first GIP circuit GIP1, the first GIP circuit GIP1 cannot receive a gate signal of the previous GIP circuit as a starting signal to start. Thus, the first GIP circuit GIP1 receives a start signal Vst and starts.

[0033] Accordingly, the start signal Vst is applied to the first GIP circuit GIP1, the first GIP circuit GIP1 outputs the first gate signal Vout1 of the high level using the first clock signal CLK1, ..., the (i-1)th gate signal Vout(i-1) of the high level outputted from the (i-1)th GIP circuit GIP(i-1) is provided to the (i)th GIP circuit GIP(i) to thereby start the (i)th GIP circuit GIP(i), and the (i)th GIP circuit GIP(i) outputs the (i)th gate signal Vout(i) of the high level using the second clock signal CLK2 (in the figure, although the second clock signal CLK2 is used, the first clock signal CLK1 or another clock signal may be used).

[0034] Next, the (i)th gate signal Vout(i) of the high level outputted from the (i)th GIP circuit GIP(i) is provided to the (i+1)th GIP circuit GIP(i+1) to thereby start the (i+1)th GIP circuit GIP(i+1), and the (i+1)th GIP circuit GIP(i+1) outputs the (i+1)th gate signal Vout(i+1) of the high level using the first clock signal CLK1 (in the figure, although the first clock signal CLK1 is used, the first clock signal CLK1 or another clock signal may be used), ..., the (j)th GIP circuit GIP(j) outputs the (j)th gate signal Vout(j) of the high level using the second clock signal CLK2 (in the figure, although the second clock signal CLK2 is used, the first clock signal CLK1 or another clock signal may be used).

[0035] When the (j)th gate signal Vout(j) is outputted from the (j)th GIP circuit GIP(j) where one frame ends, the (j)th GIP circuit GIP(j) receives a reset signal Rst and is initialized such that the first gate signal Vout1 is outputted from the first GIP circuit GIP1 where the next frame starts.

[0036] FIG. 4 is a view of schematically illustrating the first GIP circuit according to the embodiment of the present disclosure.

[0037] In FIG. 4, the first GIP circuit GIP1 includes a control unit 110 controlling a first node Q and an output unit 120 outputting the first gate signal Vout1 corresponding to the first clock signal CLK1 depending on a voltage state at the first node Q.

[0038] Here, the control unit 110 controls the voltage state of the first node Q such that the first gate signal Vout1 corresponding to the first clock signal CLK1 is outputted from the output unit 120.

[0039] To do this, the control unit 110 includes a first transistor T1 connected between a start signal (Vst) input terminal and the first node Q and a second transistor T2 connected between the first node Q, a second gate signal Vg2 input terminal and a low level voltage VSS input terminal.

[0040] Here, drain and gate of the first transistor T1 are connected to each other, and the first transistor T1 functions as a diode. That is, a voltage at the drain of the first transistor T1 is inputted to source, and on the contrary to this, a voltage at the source is not inputted to the drain.

[0041] Therefore, the first transistor T1 applies the start signal Vst to the first node Q, and at the same time, the first transistor T1 prevents a voltage charged at the first node Q from being discharged to the outside through the first transistor T1.

[0042] In addition, the second transistor T2 initializes the first node Q. At this time, the second transistor T2 turns on by the second gate signal Vg2 and charges the first node Q with the low level voltage VSS.

[0043] According to this, the first node Q can be charged by the start signal Vst of a high level at the next frame.

[0044] The output unit 120 outputs a high level of the first gate signal Vout1 or a low level of the first gate signal Vout1 depending on the voltage state of the first node Q.

[0045] To do this, the output unit 120 includes a third transistor T3 connected between a first clock signal CLK1 input terminal, the first node Q and a first gate signal Vout1 output terminal, a fourth transistor T4 connected between a second clock signal CLK2 input terminal, the low level voltage VSS input terminal and source of the third transistor T3, a fifth transistor T5 connected between drain of the third transistor T3 and the first gate signal Vout1 output terminal, and a capacitor C connected between the first node Q and the source of the third transistor T3.

[0046] At this time, the third transistor T3 turns on by a voltage of a high level charged at the first node Q and outputs the first gate signal Vout1 corresponding to a high level of the first clock signal CLK1.

[0047] Additionally, the first gate signal Vout1 is inputted to the second GIP circuit (not shown) as a starting signal. Then, the second GIP circuit outputs the second gate signal Vg2.

[0048] Moreover, the second gate signal Vg2 is inputted to the second gate signal Vg2 input terminal, and the second transistor T2 turns on by the second gate signal Vg2, whereby the first node Q is charged by the low level voltage VSS.

[0049] Furthermore, source and gate of the fifth transistor T5 are connected to each other, and the fifth transistor T5 functions as a diode. At this time, the fifth transistor T5 turns on if the high level of the first clock signal is applied to the gate of the fifth transistor T5, and the fifth transistor T5 turns off if the low level voltage VSS is applied to the gate of the fifth transistor T5.

[0050] In addition, the capacitor C is charged by a voltage level of the start signal Vst when the start signal Vst of the high level is inputted to the gate of the first transistor T1 and the first transistor T1 turns on.

[0051] Then, when the capacitor C is charged with a voltage more than a threshold voltage between the gate and source of the third transistor T3 and the first clock signal CLK1 is high, bootstrapping occurs. A voltage larger than the high level of the start signal Vst is charged at the first node Q, and the voltage of the first node Q is

definitely high. Thus, the third transistor T3 turns on.

[0052] Moreover, the fourth transistor T4 turns on by the second clock signal CLK2 and outputs the low level voltage VSS to the first gate signal Vout1 output terminal.

[0053] At this time, the low level voltage VSS is charged at the first node Q by the second transistor T2, which turns on by the second gate signal Vg2, the third transistor T3 turns off, and initialization is accomplished.

[0054] These processes are repeatedly performed at each frame.

[0055] FIG. 5 is a view of a display panel including GIP circuits in a display area according to the embodiment of the present disclosure.

[0056] In the display area AA of the display panel 100, m/2 (m is a positive even number) data lines extending in a first direction and 2n (n is an integer more than 5) gate lines extending in a second direction cross each other to thereby define m × n pixels, and 2n GIP circuits are disposed. However, for convenience of explanation, second to seventh gate lines GL2 to GL7, first to fifth data lines DL1 to DL5 and one GIP circuit are shown in the figure. At this time, the GIP circuit corresponds to the sixth GIP circuit GIP6 of FIG. 2 wherein i is 6.

[0057] In FIG. 5, two pixel columns are disposed between adjacent two of the first to fifth data lines DL1 to DL5, and two of the second to seventh gate lines GL2 to GL7 are disposed between adjacent two pixel rows.

[0058] In addition, each pixel includes a pixel electrode P and a thin film transistor Tr. A data signal from one of the first to fifth data lines DL1 to DL5 is provided to two pixel columns, which are adjacent to each other with the one of the first to fifth data lines DL1 to DL5 therebetween.

[0059] At this time, there is no data line between the two pixel columns, which are adjacent to each other with the one of the first to fifth data lines DL1 to DL5 therebetween, and the next two pixel columns.

[0060] Here, signal lines CLK, CLK2, VSS, Vst of FIG. 3 and Rst of FIG. 3 and transistors T1 to T5, which are included in the GIP circuit, are separately disposed between the two pixel columns and the next two pixel columns where there is no data line.

[0061] Namely, the LCD device according to the present invention utilizes an area where the data lines DL1 to DL5 are not disposed in the display area AA. Accordingly, since it is not necessary to arrange an additional area for the signal lines CLK1, CLK2, VSS, Vst and Rst of FIG.3 and the transistors T1 to T5 in the display area AA, an aperture ratio can be prevented from being lowered.

[0062] At this time, the signal lines CLK1, CLK2, VSS, Vst and Rst of FIG.3 include first and second clock signal lines CLK1 and CLK2, a start signal line Vst of FIG. 3, a reset signal line Rst of FIG.3, and a low level voltage line VSS.

[0063] In addition, the GIP circuit further includes a first node line QL and a second node line (not shown). Each of the first node line QL and the second node line may be disposed between adjacent two pixel rows.

[0064] Meanwhile, the signal lines CLK1, CLK2, VSS, Vst and Rst of FIG.3 extend in the first direction, and may be formed of a same material on a same layer as the data lines DL1 to DL5.

[0065] Moreover, the first node line QL and the second node line extend in the second direction. If the first node line QL and the second node line are spaced apart from the gate lines GL2 to GL7, the first node line QL and the second node line may be formed of the same material on the same layer as the gate lines GL2 to GL7. Alternatively, if the first node line QL and the second node line overlap the gate lines GL2 to GL7, the first node line QL and the second node line may be formed of a different material on a different layer from the gate lines GL2 to GL7.

[0066] Furthermore, the transistors T1 to T5 include first to fifth transistors T1 to T5.

[0067] More specifically, gate and drain electrodes of the first transistor T1 are connected to the fifth gate line GL5, and a source electrode of the first transistor T1 is connected to the first node line QL.

[0068] At this time, the first transistor T1 receives a gate signal supplied from the fifth gate line GL5 as a starting signal and inputs it to the first node line QL.

[0069] In the meantime, since there is no previous GIP circuit before the first GIP circuit GIP1 of FIG. 3, the first transistor T1 of the first GIP circuit GIP1 of FIG. 3 cannot receive a gate signal outputted from the previous GIP circuit as a starting signal to start. Thus, the gate electrode of the first transistor T1 of the first GIP circuit GIP1 of FIG. 3 is connected to the start signal line Vst of FIG. 3 and receives a start signal supplied from the start signal line Vst of FIG. 3 to start.

[0070] In addition, the gate and drain electrodes of the first transistor T1 are connected to each other, and the first transistor T1 functions as a diode. A voltage charged at the first node line QL is prevented from being discharged to the outside through the first transistor T 1.

[0071] Moreover, a drain electrode of the second transistor T2 is connected to the first node line QL, a source electrode of the second transistor T2 is connected to the low level voltage line VSS, and a gate electrode of the second transistor T2 is connected to the seventh gate line GL7.

[0072] At this time, the second transistor T2 turns on by a gate signal supplied from the seventh gate line GL7 and inputs a low level voltage supplied from the low level voltage line VSS to the first node line QL.

[0073] Like this, a next frame is prepared by charging the first node line QL with the low level voltage.

[0074] Additionally, a source electrode of the third transistor T3 is connected to the sixth gate line GL6, a drain electrode of the third transistor T3 is connected to the first clock signal line CLK1, and a gate electrode of the third transistor T3 is connected to the first node line QL.

[0075] At this time, the third transistor T3 turns on by a high level voltage charged at the first node line QL and outputs a gate signal corresponding to the clock signal

supplied from the first clock signal line CLK1 to the sixth gate line GL6.

[0076] In the meantime, as stated above, if the low level voltage is charged at the first node line QL by the second transistor T2 turning on, the third transistor T3 turns on, and the initialization is accomplished.

[0077] In addition, a gate electrode of the fourth transistor T4 is connected to the second clock signal line CLK2, a source electrode of the forth transistor T4 is connected to the low level voltage line VSS, and a drain electrode of the fourth transistor T4 is connected to the sixth gate line GL6 and the source electrode of the third transistor T3.

[0078] At this time, the fourth transistor T4 turns on by a clock signal supplied from the second clock signal line CLK2 and outputs the low level voltage supplied from the low level voltage line VSS to the sixth gate line GL6.

[0079] Moreover, a drain electrode of the fifth transistor T5 is connected to the first clock signal line CLK1, and a gate electrode and a source electrode of the fifth transistor T5 are connected to the sixth gate line GL6 and the drain electrode of the third transistor T3.

[0080] At this time, the fifth transistor T5 turns on a clock signal supplied from the first clock signal line CLK1 and outputs a gate signal corresponding to the clock signal to the sixth gate line GL6, and the fifth transistor T5 turn off by the low level voltage supplied from the low level voltage line VSS and outputs the low level voltage to the sixth gate line GL6.

[0081] Meanwhile, the gate and source electrodes of the fifth transistor T5 are connected to each other and the fifth transistor T5 functions as a diode.

[0082] In the above processes, although it is explained to output a gate signal from a sixth GIP circuit GIP6 of FIG. 3 disposed in the display area AA to the sixth gate line GL6, other GIP circuits may output gate signals to respective gate lines according to the same processes as the above processes.

[0083] Hereinafter, arrangement structures and connection relations of the first to fifth transistors T1 to T5, the signal lines CLK1, CLK2 and VSS connected to the first to fifth transistors T1 to T5, and the first node line QL will be explained with reference to FIG. 5.

[0084] First, since the sixth GIP circuit GIP6 of FIG. 3 outputs the gate signal to the sixth gate line GL6, the first to fifth transistors T1 to T5 of the sixth GIP circuit GIP6 of FIG. 3 are disposed between the fifth gate line GL5 and the sixth gate line GL6.

[0085] At this time, the first transistor T1 is disposed at a left side of the first pixel column connected to the first data line DL1, the second transistor T2 is disposed between two pixels P, which are located between the fourth and fifth data lines DL4 and DL5, the third transistor T3 is disposed between the two pixels P, which are located between the first and second data lines DL1 and DL2, the fourth transistor T4 is disposed between the two pixels P, which are located between the third and fourth data lines DL3 and DL4, and the fifth transistor T5 is disposed between the two pixels P, which are located between the second and third data lines DL2 and DL3.

[0086] In addition, the first clock signal line CLK1 is disposed between the two pixel columns, which are located between the first and second data lines DL1 and DL2, and also disposed between the two pixel columns, which are located between the second and third data lines DL2 and DL3.

[0087] At this time, the first clock signal line CLK1 are connected to the third and fifth transistors T3 and T5.

[0088] Moreover, the second clock signal line CLK2 is disposed between the two pixel columns, which are located between the third and fourth data lines DL3 and DL4, and is connected to the fourth transistor T4.

[0089] Furthermore, the low level voltage line VSS is disposed at a right side of the pixel column, which is located at a right side of the fifth data line DL5.

[0090] At this time, the low level voltage line VSS extends parallel to the fourth and fifth gate lines GL4 and GL5 between the fourth and fifth gate lines GL4 and GL5 and is connected to the second and fourth transistors T2 and T4.

[0091] Additionally, the first node line QL is disposed parallel to the sixth and seventh gate lines GL6 and GL7 between the sixth and seventh gate lines GL6 and GL7 and is connected to the first, second and third transistors T1, T2 and T3.

[0092] In the above embodiment, two clock signals are used. However, the number of the clock signals is not limited to this and is changeable.

[0093] Meanwhile, the gate line from which the first transistor T1 receives the starting signal and the gate line from which the second transistor T2 receives the gate signal to turn on may be changed.

[0094] For example, when eight clock signals are used, the first transistor T1 may receive the starting signal from the (i-4)th gate line, and the second transistor T2 may receive the gate signal of the (i+4)th gate line to turn on. That is, since i is 6, the gate electrode of the first transistor T1 may be connected to the second gate line, and the gate electrode of the second transistor T2 may be connected to the tenth gate line.

[0095] At this time, the gate electrode of the first transistor T1 of each of the first to fourth GIP circuits may be connected to the start signal line Vst of FIG. 3, and the gate electrode of the second transistor T2 of each of the (j-3)th to (j)th GIP circuits may be connected to the reset signal line Rst of FIG. 3.

[0096] Like this, the narrow bezel can be achieved by disposing the signal lines CLK1, CLK2, VSS, Vst of FIG. 3 and Rst of FIG. 3 and the transistors T1 to T5 of the GIP circuits, which were disposed at the non-display areas NAA of FIG. 1 at the left and right sides of the display area AA of FIG. 1, in the display area AA.

[0097] In addition, since the signal lines CLK1, CLK2, VSS, Vst of FIG. 3 and Rst of FIG. 3 and the transistors T1 to T5 of the GIP circuits are formed together when the data lines DL1 to DL5, the gate lines GL2 and GL7,

and the thin film transistors Tr of the pixels P are formed, the manufacturing processes are simplified, and the manufacturing costs are decreased.

[0098] It will be apparent to those skilled in the art that various modifications and variations can be made in a display device of the present disclosure without departing from the scope of the invention. Thus, it is intended that the present disclosure covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

1. A liquid crystal display device comprising:

a display panel including a display area with m × n pixels and a non-display area,
m/2 data lines arranged in the display area in a first direction, with m being a positive even number,
2n gate lines arranged in the display area in a second direction, with n being an integer more than 5, wherein the gate lines and the data lines cross each other for defining the m × n pixels arranged in m pixel columns and n pixel rows; and
2n GIP circuits arranged in the display area, the GIP circuit including transistors,

wherein two gate lines are disposed between adjacent two pixel rows, and two pixel columns are disposed between adjacent two data lines, and
wherein the transistors are arranged between pixel columns disposed between adjacent two data lines.

2. The liquid crystal display device of claim 1, wherein output of odd GIP circuits of the 2n GIP circuits is provided to odd gate lines of the 2n gate lines, and output of even GIP circuits of the 2n GIP circuits is provided to even gate lines of the 2n gate lines.

3. The liquid crystal display device of claim 1 or 2, further including signal lines for providing signals to the GIP circuits, the signal lines being arranged between pixel columns disposed between adjacent two data lines.

4. The liquid crystal display device of claim 3, wherein the signal lines are disposed on a same layer as the data lines and/or are made of a same material as the data lines.

5. The liquid crystal display device according to any one of the preceding claims 3 or 4, wherein the signal lines extend in the first direction.

6. The liquid crystal display device according to any one of the preceding claims, wherein the GIP circuit further includes at least one of a first and second node lines disposed between adjacent two pixel rows.

7. The liquid crystal display device of claim 6, wherein at least one of the first and second node lines is spaced apart from the gate lines and/or is disposed on a same layer as the gate lines and/or is made of a same material as the gate lines.

8. The liquid crystal display device of claim 6, wherein at least one of the first and second node lines is arranged overlapping one of the gate lines and is disposed on a different layer from the gate lines.

9. The liquid crystal display device according to any one of the preceding claims 6 to 8, wherein the first and/or second node lines extend in the second direction.

10. The liquid crystal display device according to any one of the preceding claims 3 to 9, wherein the signal lines include first and second clock signal lines, a start signal line, a reset signal line and a low level voltage line.

11. The liquid crystal display device of claim 10, wherein a first GIP circuit configured to output a gate signal to a first gate line includes:

a first transistor connected to the start signal line and the first node line;
a second transistor connected to the first node line and the low level voltage line;
a third transistor connected to the first clock signal line and the first node line;
a fourth transistor connected to the second clock signal line, the low level voltage line and the third transistor; and
a fifth transistor connected to the first clock signal line and the third transistor.

12. The liquid crystal display device of claim 10 or 11, wherein an ith GIP circuit configured to output a gate signal to an ith gate line, with i being an integer larger than 2, includes:

a first transistor connected to a (i-1)th gate line and the first node line;
a second transistor connected to the first node line and the low level voltage line;
a third transistor connected to the first clock signal line and the first node line;
a fourth transistor connected to the second clock signal line, the low level voltage line and the third transistor; and
a fifth transistor connected to the first clock sig-

nal line and the third transistor.

13. The liquid crystal display device according to any one of the preceding claims, wherein each transistor of one GIP circuit is arranged between two pixel columns that are disposed between adjacent two data lines and/or wherein the transistors of one GIP circuit are arranged in the second direction along one of the gate lines.

14. The liquid crystal display device according to any one of the preceding claims, further comprising a data driving unit in the non-display area and configured to output data signals to the data lines.

15. The liquid crystal display device according to any one of the preceding claims, wherein two pixels of one pixel row are connected to a same data line arranged therebetween and/or wherein pixels of one pixel row are alternately connected to an odd and an even gate line.

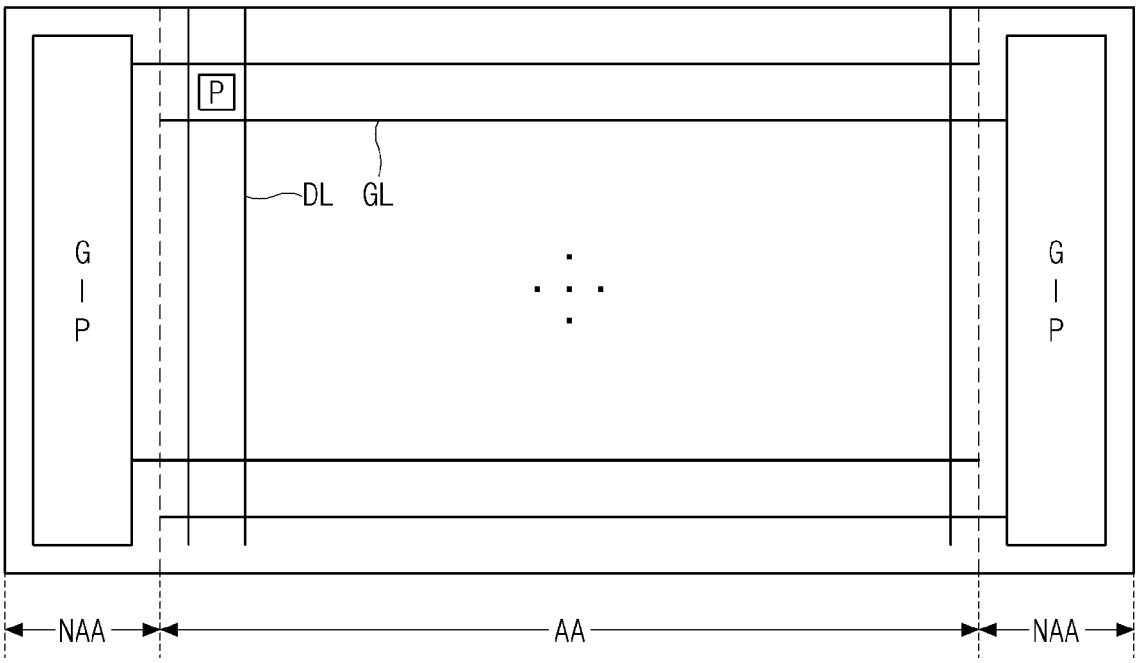
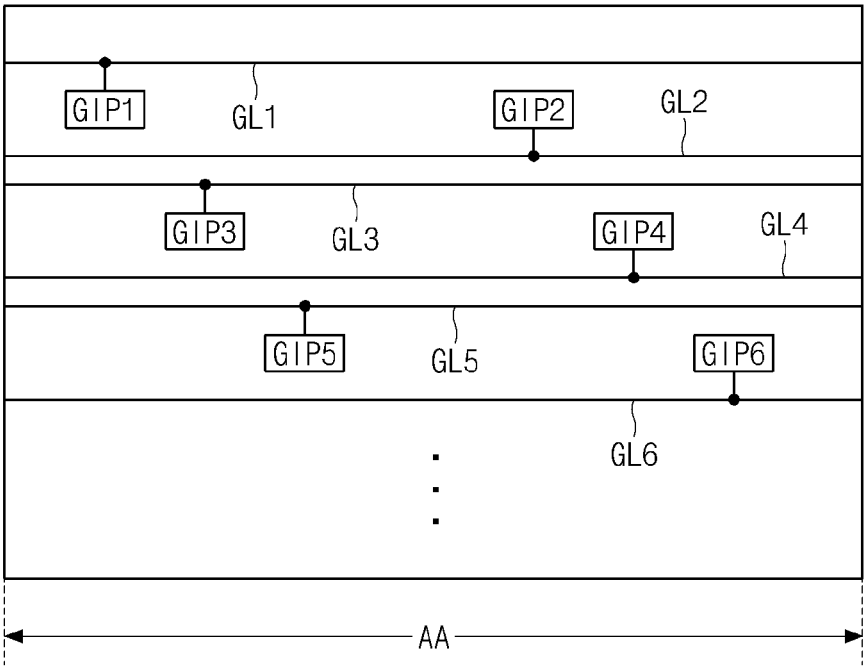


FIG. 1



100

FIG. 2

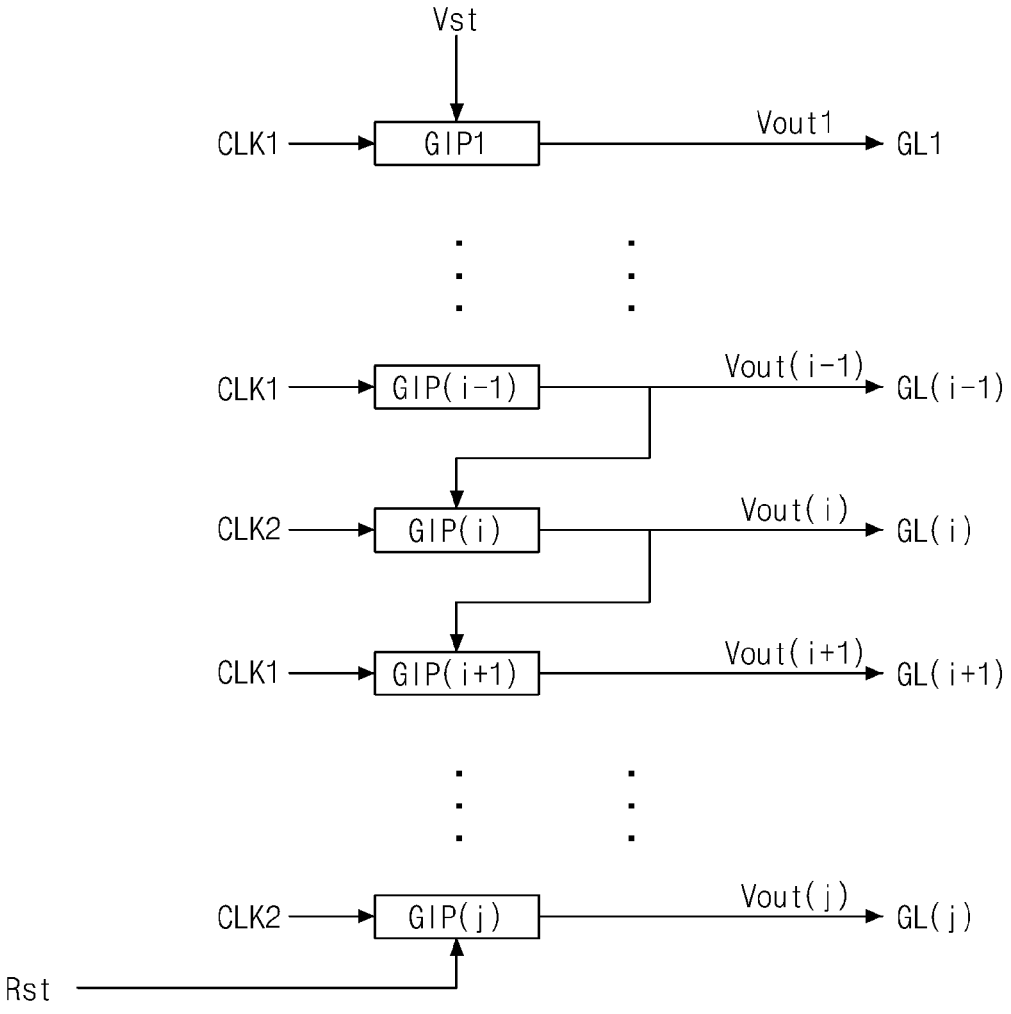

Vst
CLK1
GIP1
Vout1
GL1
CLK1
GIP(i-1)
Vout(i-1)
GL(i-1)
CLK2
GIP(i)
Vout(i)
GL(i)
CLK1
GIP(i+1)
Vout(i+1)
GL(i+1)
CLK2
GIP(j)
Vout(j)
GL(j)
Rst

FIG. 3

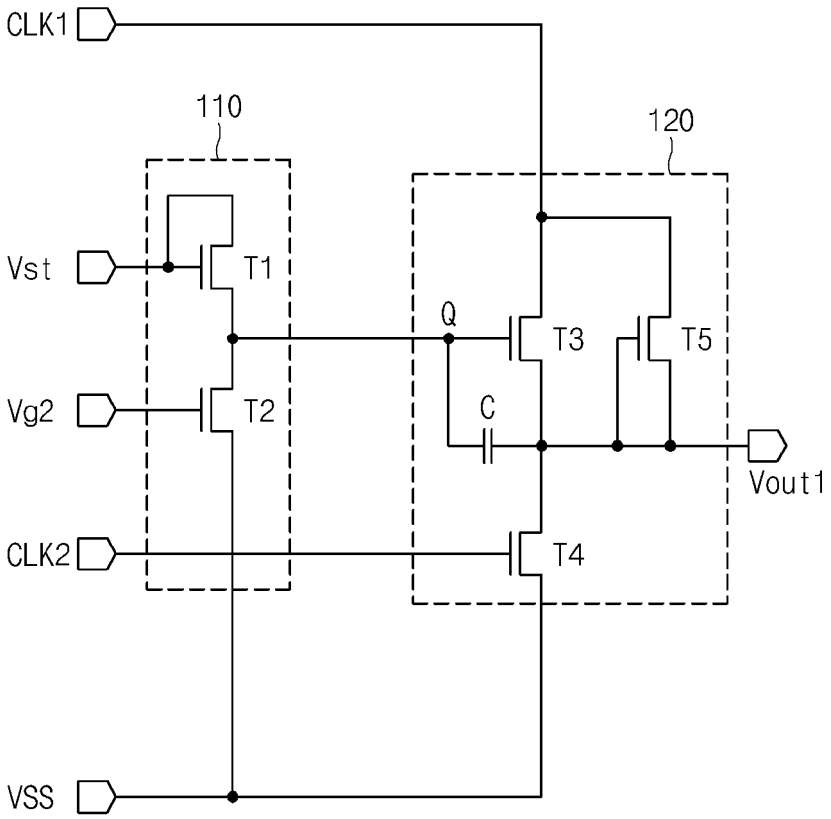


FIG. 4

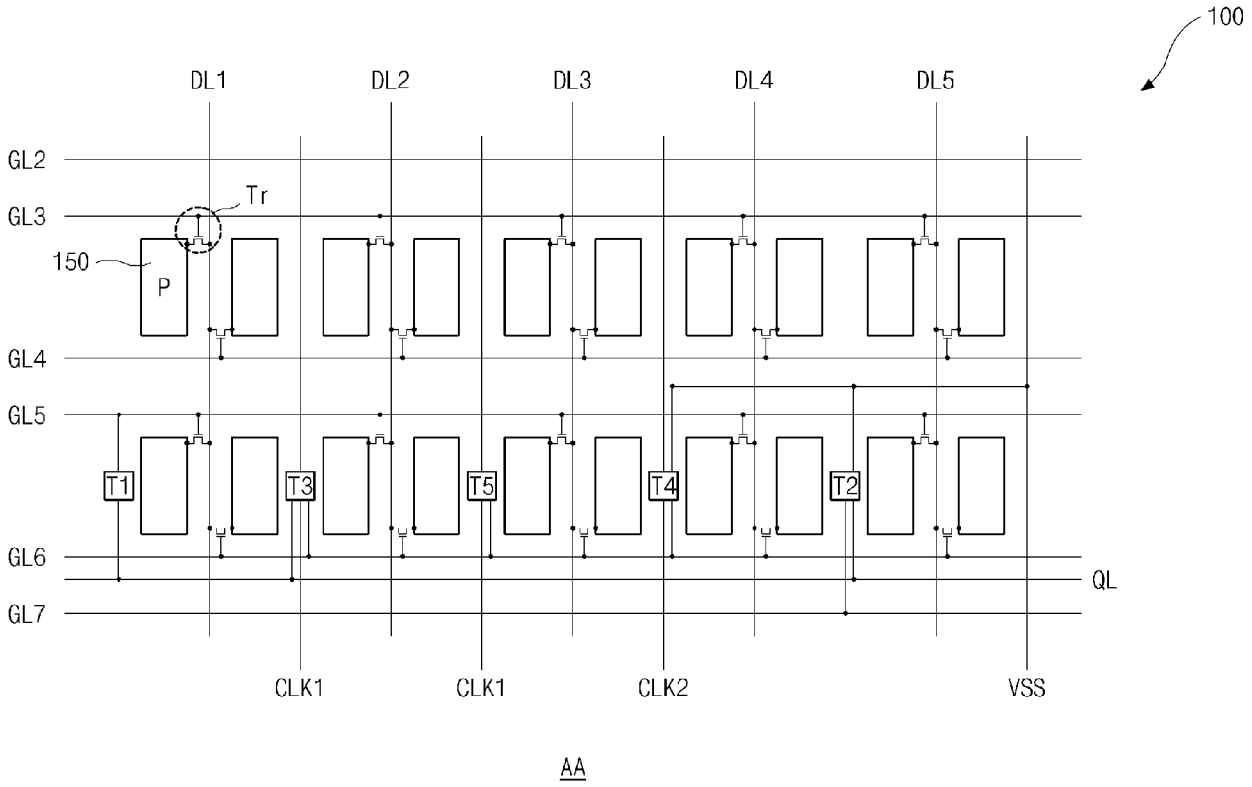

100
DL1
DL2
DL3
DL4
DL5
GL2
GL3
Tr
150
P
GL4
GL5
T1
T3
T5
T4
T2
GL6
QL
GL7
CLK1
CLK1
CLK2
VSS
AA

FIG. 5

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EUROPEAN SEARCH REPORT

Application Number
EP 16 20 7554

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2014/043306 A1 (MIN WOONG KI [KR] ET AL) 13 February 2014 (2014-02-13) * paragraphs [0016], [0030] - [0036], [0044], [0076], [0079]; figures 2-4,9 * -----	1-15	INV. G09G3/36 G11C19/00
Y	CN 104 849 928 A (SHANGHAI AVIC OPTOELECTRONICS; TIANMA MICRO ELECTRONICS CO) 19 August 2015 (2015-08-19) * abstract * -& US 2016/307937 A1 (JIN HUIJUN [CN]) 20 October 2016 (2016-10-20) * paragraphs [0002] - [0006], [0047] - [0049]; figure 5 * -----	1-15	
Y	EP 1 492 078 A2 (SAMSUNG ELECTRONICS CO LTD [KR]) 29 December 2004 (2004-12-29) * paragraphs [0016], [0042] - [0044]; figure 6 * -----	1-15	
			TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	18 May 2017	Demin, Stefan

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18-05-2017

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014043306 A1	13-02-2014	CN 103578443 A	12-02-2014
		US 2014043306 A1	13-02-2014
CN 104849928 A	19-08-2015	CN 104849928 A	19-08-2015
		US 2016307937 A1	20-10-2016
US 2016307937 A1	20-10-2016	CN 104849928 A	19-08-2015
		US 2016307937 A1	20-10-2016
EP 1492078 A2	29-12-2004	CN 1573459 A	02-02-2005
		EP 1492078 A2	29-12-2004
		JP 2005018066 A	20-01-2005
		KR 20050000105 A	03-01-2005
		TW I277938 B	01-04-2007
		US 2004257322 A1	23-12-2004
		US 2008204390 A1	28-08-2008
		US 2013215097 A1	22-08-2013

EPO FORM P0459

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