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(54) **RESISTIVE INTERPOLATION MESH CIRCUIT FOR TIME-TO-DIGITAL CONVERTERS**

(57) Resistive interpolation mesh circuits (RIMCs) for time-to-digital converter (TDCs) are disclosed. ROs are arranged and coupled in a two-dimensional parallel configuration, each RO comprising an uneven number of DEs. The RIMCs may be used in high resolution TDCs

with a broad range of applications from Positron Emission Tomography (PET) to lifetime, coincidence, synchronous data transfer, distance measurement, 3D imaging systems requiring high resolution timing.

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Description

[0001] The present disclosure relates to time-to-digital converters (TDCs) and more specifically to resistive interpolation circuits and to their applications in TDCs.

BACKGROUND

[0002] In electronic instrumentation and signal processing, a TDC (also known as Time Counter (TC)) is a device for recognizing events and providing a digital representation of the time they occurred. For example, a TDC might output the arrival time of incoming pulses. Other applications might measure the time interval between two events rather than some notion of an absolute time.

[0003] TDCs are used in many different applications, for example in lifetime measurements of physical, chemical or biological processes, measurements of velocity in almost any field or in any kind of coincidence experiments, pulse based systems using lasers, and others such as Ultra-Wide-Band (UWB) transceivers.

[0004] In electronics, TDCs (or time digitizers) are devices commonly used to measure the time when an event occurred, or the time interval between two events covering them into digital (binary) outputs. Interpolation is an effective mean to improve the resolution of a TDC. Applications requiring a high resolution TDC include lifetime measurements of processes like atomic or nuclear decays, time resolved fluorescence or, in general, any fast (sub-nanosecond (sub-ns)) physical, chemical or biological process. Any application based on interval or coincidence measurements of fast occurring events ranging from astrophysics to nuclear physics as well as many others in between will benefit from any improvement of the timing resolution.

[0005] High resolution TDCs may be used in node synchronization in packet-based networks requiring sub-ns accuracy. This type of networks are used in geographically distributed synchronous data transfer systems such as High Energy Physics (HEP) experiments, for example in the Large Hadron Collider (LHC) machine, or in the Cherenkov Telescope Array (CTA) and in the Cubic Kilometer Neutrino Telescope (KM3NeT). In the White Rabbit (WR) protocol for data transfer and sub-ns synchronization, each link delay is measured precisely so that the transmitter and receiver nodes can adjust their relative time offset corresponding to the link distance and delay introduced by transmission/reception circuitry. To measure these delays an accurate timestamping system is required. Thus, the higher the accuracy of the timestamp measurement, the better synchronization can be achieved.

[0006] Another application field is 3D imaging technologies using distance measurement, such as LIDAR, RADAR or SONAR. In these technologies, distance is measured by emitting a signal (laser pulses, radio waves or acoustic waves) towards a target and then computing the round trip time using the reflected signal.

[0007] Of particular interest, for its impact on the health system is the case of Positron Emission Tomography (PET), a nuclear medicine imaging technique that allows in-vivo 3D visualization of functional processes inside the body. A PET system is based in the simultaneous detection of pairs of gamma rays following the annihilation of positrons emitted by certain radionuclide tracers, which are introduced into the body on a biologically active molecule. The emitted positrons slow down as they cross the surrounding tissues until they find an electron (almost at rest), annihilates and yields two simultaneous gamma rays (with an identical energy of 511 keV), traveling almost back-to-back in the same direction. The PET scanner (or readout) shall detect both photons in coincidence and identify them as a single (correlated) pair.

[0008] The interest of a high resolution TDC in detection systems in which the interesting events are selected based on the coincidence among a number of detector elements comes from the fact that the number of random coincidences is directly proportional to the width of the coincidence window to the power of the number of elements. This has direct implications on: (1) the quality of the image on PET systems in which signal events are selected based on the simultaneous detection of two gamma rays; (2) the amount of collected data in any non-accelerator based Particle Physics experiments in which the event selection system is typically based on the coincidence among a number of detector elements; or (3) the amount of random noise on sky observation experiments (using e.g. a CTA) due to the coincidences with random signals from night photons hitting the telescopes.

[0009] In many cases, an exact timing determination will typically allow a correspondingly exact position determination. For example, at the speed of light, 100 picoseconds correspond to 30 mm. This type of precision allows reducing a Line of Interest (LoI) in PET coincidence (the line connecting the two detected photons typically 400 to 1200 mm away), to a Segment of Interest (SoI) of few mm within the corresponding LoI. Thus a PET system with improved time resolution will not only have reduced number of random coincidences, but at the same time the noise in the resulting image will be further reduced. As a consequence, to achieve the same quality of image the dose to the patient or the scanning time (or both) can be reduced, thus saving in cost and reducing patient risk.

[0010] The resolution of a TDC, and therefore its accuracy, is limited by the frequency of the reference clock. If time is measured by whole counts, then the resolution is given by the clock period. For example, a 10 MHz clock implies a resolution of 100 ns. To get resolutions finer than the clock period time interpolation circuits are used. These circuits measure the fraction of a clock period. The interpolation circuits often require a significant amount of time to perform

their function. Consequently, such a TDC requires a quiet interval between consecutive measurements (dead time).

[0011] Delay line based TDCs are a class of TDC in which an input clock is delayed by M Delay Elements (DE), obtaining a bus of M+1 clocks. The minimum time difference between these clocks, i.e. TDC resolution, is constrained by the minimum end-to-end delay of DEs for a given technology.

[0012] The resolution of a TDC is typically expressed in terms of the time equivalence of the Least Significant Bit (LSB). To improve timing resolution of the LSB, digital interpolation has been proposed by Perktold et al. (L. Perktold and J. Christiansen, "A multichannel time-to-digital converter ASIC with better than 3 ps RMS time resolution", 2014, JINST 9 C01060). In Fig. 1 a detailed view of the fine-time interpolator structure proposed by Perktold et al. is shown. This technique consists in placing N resistors between two consecutive DE nodes, and thus obtaining N-1 intermediate sub-delay nodes. Thus, the minimum clock delay is scaled down by a factor N.

[0013] However, the implementation described in Perktold et al. might vary substantially according to the target resolution, since each resistor requires manual tuning to achieve uniform TDC bin sizes. This affects the design time and limits the reusability of blocks for different implementations. Furthermore, it requires more than one resistor and one buffer per stage which affects area resources and power consumption.

[0014] It would be desirable to provide a resistive interpolation circuit that at least partially resolves the aforementioned problems.

SUMMARY

[0015] A new resistive interpolation mesh circuit (RIMC) for high resolution TDCs is proposed using a single DE (based on an inverter, such as a current starved inverter, and a resistor) which is replicated in two dimensions and thus obtaining a mesh of sub-delay nodes. Top and bottom nodes are coupled to make the circuit oscillate. An odd (uneven) number of rows are used to achieve oscillation.

[0016] In a first aspect, a RIMC for a TDC is provided. The RIMC comprises two or more Ring Oscillators (RO) arranged in a two-dimensional parallel configuration, all ROs having identical components. Each RO comprises an uneven number of three or more DEs, each DE comprising an inverter having an input and an output, and a resistor coupled at one end to the input of the inverter. The inverters of the DEs of each RO are connected in series and the output of the last inverter in the series connection is coupled to the input of the first inverter in the series. Between two consecutive ROs in parallel configuration the input of the inverter of the DE of the following RO is coupled to the other end of the resistor of the DE of the same rank of the preceding RO, respectively, to generate a mesh circuit.

[0017] Each DE of the mesh circuit may provide an output of the RIMC at the other end of the resistor.

[0018] The proposed interpolation mesh circuit requires only a single type of device (the DE having an inverter and a resistor) to build a clock matrix, thus providing a simplified and scalable design. The resulting clock matrix may be perceived as a series of rows and columns of the DE. Furthermore, each node of the mesh circuit has identical capacitive loading, which means that no local tuning is required. Further to that, different TDC performances and power consumptions may be achieved by modifying the number of rows and columns of the clock matrix. The DE of the proposed mesh circuit, having one adjustable buffer (with three transistors for each inverter) and one resistor per clock phase allows for low power consumption. Power consumption basically depends on three factors: the drive strength of inverters, the number of sub-delay stages and the parasitic capacity of the clock stages. While an increase in drive strength increases the ring frequency, and thus decreases end-to-end delay between rows, an increase in the number of columns increases dynamic range at row level (which in turn means an improvement in resolution). Both factors contribute to an increase in TDC resolution at the expense of power consumption.

[0019] All the inverters have the same performance characteristics within predefined variation ranges. The inverters may comprise PMOS or NMOS transistors. The transistor width may be selected based on desired oscillation frequency and power consumption of the mesh circuit, and consequently of the TDC.

[0020] The inverters may be current starved inverters. A current starved inverter comprises a logic inverter where an additional NMOS transistor is placed in series between the original NMOS transistor of a bare inverter and ground. In this way, the current flow -and thus delay- of this inverter is controlled by modifying the V_{GS} voltage (voltage between gate and source) of the additional NMOS transistor, which is therefore called V_{CTL} (control voltage).

[0021] The use of this V_{CTL} enables the capability of adjusting the mean RIMC performance to a nominal value despite the presence of process, voltage or temperature variations.

[0022] Furthermore, all the resistors have the same performance characteristics within predefined variation ranges. The value of the resistors may be selected to determine sub-delay resolution of the TDC.

[0023] The number of ROs, i.e. mesh columns, may be selected based on a desired resolution of the TDC. The RIMC may comprise any number of ROs. For a more efficient codification of the measurements, the RIMC may comprise 2^k ROs, k being a natural number.

[0024] In some examples, the RIMC may further comprise at least four ROs. The first and the last ROs of the parallel configuration may then be dummy ROs, to thus avoid bin nonuniformities. The generated clocks in the first and the last

columns may not be used for the timing conversion since the node capacitances will be slightly different from the ones in the middle of the mesh.

[0025] In a second aspect, a TDC is provided. The TDC comprises a RIMC according to any of the examples disclosed herein. TDCs according to this aspect may be high resolution TDCs with low power consumption. Power consumption of the RIMC is lower than that of the digital interpolation TDC proposed by Perktold et al. for the same TDC resolution and manufacturing technology because there is no need for the n (32 in Perktold et al.) number of elements of the 1st stage of the DLL (Delay Locked Loop) employed in Perktold et al. as this functionality is provided by the same RIMC that, as mentioned, oscillates having an uneven number of elements. Thus any apparatus or application where high resolution TDCs are employed (e.g. PETs, CTAs, UWB etc.) may benefit from TDCs according to this aspect.

[0026] In some examples, the TDC may further comprise a front-end readout circuit and a back-end readout circuit. The front-end readout circuit may comprise a time capture register matrix, having one time capture register for each stage of the RIMC, each register being latched by the rising edge of the timing signal to be digitized. Each data input terminal of the time capture register is connected to one of the outputs of the DEs belonging to the same rank of the RIMC. Furthermore, the front-end circuit may comprise a XOR circuit to convert the unary data input into a binary encoded sequence. The XOR circuit may comprise one XOR element for each pair of inverters of the same stage of consecutive ROs. A first input of each XOR element may be coupled to the input of the first inverter of the pair and a second input may be coupled to the input of the second inverter of the pair. Finally, XOR outputs (as many as matrix columns) may be encoded into binary.

[0027] The back-end readout circuit may aggregate the data from each stage (row) of the mesh circuit and determine the RO (column of the mesh circuit or the number of LSBs) where the transition occurred.

[0028] In a third aspect, a 3D imaging system is provided. The 3D imaging system may comprise a PET, a LIDAR, a SONAR or a RADAR system. The 3D imaging system may comprise a TDC according to examples disclosed herein.

[0029] In yet a fourth aspect, a geographically distributed synchronous data transfer system is provided. This system may comprise a TDC according to examples disclosed herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] Non-limiting examples of the present disclosure will be described in the following, with reference to the appended drawings, in which:

Fig. 1 is a detailed view of the fine-time interpolator structure proposed by Perktold et al.

Fig. 2a schematically represents a DE according to an example and Fig. 2b a RIMC using such DE.

Fig. 3 schematically represents a RIMC according to another example.

Fig. 4 is a resistive interpolation mesh chronogram and data acquisition example

Fig. 5 schematically represents a TDC according to an example.

Fig. 6 schematically represents a readout circuit for a TDC according to an example.

Fig. 7 schematically represents a PET according to an example.

DETAILED DESCRIPTION OF EXAMPLES

[0031] Fig. 2a schematically represents a DE according to an example and Fig. 2b a RIMC using such DEs. RIMC 200 comprises two ROs 210 and 220. Each RO comprises three DEs. Each DE comprises an inverter and a resistor. RO 210 comprises DEs 211, 213 and 215. DE 211 comprises inverter 212 and resistor 232 coupled at one end to the input of inverter 212. Accordingly, DEs 213 and 215 comprise inverters 214, 216 and resistors 234, 236, respectively. Inverters 212, 214, 216 are connected in series. The output of the last inverter (216) in the series is coupled to the input of the first inverter (212) in the series. Accordingly, RO 220 comprises DEs 221, 223 and 225. DE 221 comprises inverter 222 and resistor 242. Accordingly, DEs 223 and 225 comprise inverters 224, 226 and resistors 244, 246, respectively. Again, inverters 222, 224, 226 are connected in series and the output of the last inverter (226) in the series is coupled to the input of the first inverter (222) in the series. The other end of resistor 232 is coupled at the input of inverter 222. Accordingly, the other end of resistor 234 is coupled at the input of inverter 224, and the other end of resistor 236 is coupled at the input of inverter 226. The nodes of the mesh correspond to outputs of the interpolator. Assuming that the ROs are arranged in columns of the interpolator mesh, each row covers a different timing slot and within each slot sub-

delays determine timing resolution. As the mesh circuit comprises an odd (uneven) number of rows and the output of the last inverters is coupled to the input of the first inverters, the circuit will oscillate. The sub-delays are determined by the timing differences between the two nodes of the resistances.

[0032] Fig. 3 schematically represents a RIMC according to another example. In the example of Fig. 3, the mesh circuit has seven rows (ROW0-ROW6) where in each row there is an arbitrary number of DEs (18 in this example, R0<0> to R0<15> plus 2 dummies DIN0 and DOUT0). Another way of looking at it is that there are 18 ROs in a parallel configuration, each with seven DEs coupled between them at the inputs of the corresponding inverters of consecutive ROs as well as at the inputs of the inverters of the last RO. The minimum delay (sub-delay) in the circuit is determined by the timing difference between resistor terminals, while inverter delay may determine delay between rows. Again, as there is an odd (uneven) number of rows and the output of the bottom inverters is coupled to the input of the top inverters, the circuit will oscillate.

[0033] Fig. 4 is a resistive interpolation mesh chronogram and data acquisition example. The example chronogram corresponds to the circuit shown in Fig. 3. Each row covers a different timing slot and within this slot sub-delays determine timing resolution. A small overlap exists between slots to accommodate process and mismatch variations. In a first example situation, a first event (TIME_A) generates a timing pulse that raises an edge matching with one of the rising edges in ROW4, more concisely the number 8. In a second example, a second event (TIME_B) generates another timing pulse that rises an edge matching with rising edges in ROW2 (number 15) and ROW3 (number 2).

[0034] Fig. 5 is a TDC according to an example. TDC 500 comprises PLL 505. PLL 505 comprises a RIMC 510, substantially similar to the one described with reference to Fig. 3, and a voltage controller 515. Voltage controller 515 comprises a Phase/Frequency Detector (PFD) 516, a clock divider 517 and a Charge Pump (CP) 518. The PFD compares the reference clock frequency with the output (clk800) of the RIMC clock divided by M which is the multiplicative factor of the PLL. In the example of Fig. 5, the RIMC output clock frequency is 800 MHz and M equals 4 (four). Therefore the output of the clock divider 517 (clk200) has a frequency of 200 MHz. The CP 518 adjusts the control voltage.

[0035] The RIMC 510 not only provides all the clock phases, but it is also in charge of implementing the voltage control oscillator (VCO) function in the PLL. This is possible because the RIMC 510 is composed of a number of ROs arranged in parallel, as explained with reference to Fig. 2 and 3. The VCO functionality is achieved through the voltage control of the inverters. Furthermore, the RIMC 510 provides timing pulses that latch the logic level of clocks by means of Time Capture Registers (TCR) of a front-end readout circuit 520. These TCRs may also be organized in rows and columns and are explained in detail with reference to Fig. 6. TDC 500 further comprises a back-end readout circuit 530 that receives fine data from the front end readout 520 and registers the events. The back-end readout 530 is also coupled to coarse counter 535. The coarse counter 535 is incremented every time there is a rising edge in the 800 MHz clock. It is used to increase the dynamic range of the TDC. For example, for a 10 bit coarse counter, there is an overflow of the counter every 1024 clock cycles, which happens every 1280 ns. When this happens the overflow signal (COARSE_OVF) is generated in such a way that an external system (e.g. an Field Programmable Gate Array (FPGA)) is able to increment indefinitely the dynamic range through the counting of the overflows that the coarse counter generates. The back-end readout 530 may be coupled to serializer 550 which may convert the events to a series of bits and send them to an external system that may read the data. One skilled in the art may appreciate that the TDC may further comprise further input/output/interface elements, such as receptors/drivers Low-Voltage Differential Signaling (LVDS) 507, 555, an Serial Peripheral Interface (SPI) slave 540, etc.

[0036] Fig. 6 schematically depicts a front-end readout for the RIMC of Fig. 3. The front-end readout of Fig. 3 comprises TCRs and XOR elements. The front-end readout design proposed for this example is as follows: the timing signal of the RIMC is used to latch the 16 clock phases that may be found in each row using one D-type flip flop 605 per row. Then, the same timing pulse may be used to generate a secondary delayed pulse that will store data while data is being converted using a D-type flip flop with Reset 610. This delayed version of the timing pulse may introduce some busy logic mechanism to ensure that no timing violations occur during data conversion. Therefore, T_i<15:0> data will be stable during readout procedure.

[0037] An XOR operation with 2 inputs between consecutive columns may be performed using XOR gates 615 to determine the location where transition either from 0 to 1 or from 1 to 0 occurs. When timing signal is in phase with one (or two) clock transitions, the XOR operation between the captured data of the adjacent columns will differ. If this happens, the column number where transition occurs is encoded. A row flag rises thus indicating that an event occurred. Finally, the row and column number will be encoded into TDC counts of the back-end readout circuit 530. The following table is an example of the four possible states that the time capture row may take:

Event	Type	T _i <15:0>	XOR _i <14:0>	COL _i	HIT<i>	CLK_PHASE<i>
No	-	0000000000000000	0000000000000000	0	0	!mod(i,2)
No	-	1111111111111111	0000000000000000	0	0	mod(i,2)

(continued)

Event	Type	$T_i<15:0>$	$XOR_i<14:0>$	COL_i	HIT<i>	$CLK_PHASE<i>$
Yes	0 to 1	0000011111111111	0000100000000000	5	1	$!mod(i,2)$
Yes	1 to 0	1111111111000000	0000000001000000	10	1	$mod(i,2)$

[0038] The first column of the table indicates if an event has occurred or not. The second column indicates the type of event which, in case an event has occurred may be either a logical transition from a logical 0 to a logical 1 or from a logical 1 to a logical 0. If no event has occurred then the bit sequence of $T_i<15:0>$ shall remain the same and unchanged. If an event occurs then this will be reflected within $T_i<15:0>$ where a bit change will appear. This may be confirmed by the $XOR_i<14:0>$ bit sequence that will indicate the position where the change occurred. This is also reflected in the next column of the table, COL_i , where the number of the column, i.e. the number of the DE in a row, has provided the corresponding signal. The column where the transition occurs may be binary encoded in 4 bits using binary encoder 620 in Fig. 6. An additional flag, HIT<i>, may be generated to alert the back-end readout circuit that one transition occurred at this row. Finally, a signal $CLK_PHASE<i>$ may be generated by XOR gates 625 to disambiguate between rising and falling transitions that may occur in the row. Rising transitions may produce $CLK_PHASE<i>$ equal to 1 for those even rows, and vice versa for those uneven rows, as indicated by the modulo functions $mod(i, 2)$ and $!mod(i, 2)$, which is the logic negation of $mod(i, 2)$, in the last column.

[0039] The back-end readout may compute the data offset determined by the clock phase and the row number value where the first event was produced. Then, the column number value may be computed by averaging column transitions using arithmetic expansion techniques. If only one transition is detected, the column value may be obtained by multiplying the column number of the transition by 2. Otherwise, the column value may be obtained by summing both column numbers and adding an extra offset equivalent to the number of matrix columns. The number of bits of the fine interpolation output value may be: 1 for the clock phase, M for the number of rows, N for the number of columns and 1 for the arithmetic expansion of the average calculation.

[0040] Additionally, the back-end readout block may generate a BUSY signal to prevent the Front-End block from overwriting an event while the event is being processed.

[0041] Fig. 7 is a Time-of-Flight (ToF) PET according to an example. ToF PET 700 comprises a TDC 710. TDC 710 comprises RIMC 720. The ToF PET system 700 may comprise a plurality of gamma detectors 705 that may receive the results of positron annihilation. A ToF PET module 710 of the ToF PET 700 may then receive an electric pulse signal from detector 705. PET module 710 may comprise a ToF PET front-end 715, a TDC 720 and a data acquisition module (DAQ) 725. The TDC 720 may be substantially similar to the TDC 500 described with reference to Fig. 5. The ToF PET front-end 710 may receive the analog pulse signal and measure its energy which is proportional to the time integral over the pulse. This measurement may be directed to the DAQ 725. The ToF PET front-end 710 may also generate a digital pulse every time an electric pulse arrives. The TDC may then identify at which instance (based on the TDC resolution) the signal was produced. The DAQ 725 may reconstruct the event with the energy and timing information and transfer the data to an external system that may receive all information from all PET modules and may then determine coincidences and calculate Lol or Sol if the pulses are simultaneous, or identify and discard undesired or erroneous measurements and noise. It is noted that the resolution of the TDC, and therefore the timing precision, may define both the precision in the measurement of the position where positron annihilation is produced, as well as the amount of noise in the reconstructed image by going from a Lol to Sol. In PET scanning, a higher precision may reduce the time a patient is exposed, as less data is required to achieve the same image quality.

[0042] Although only a number of examples have been disclosed herein, other alternatives, modifications, uses and/or equivalents thereof are possible. Furthermore, all possible combinations of the described examples are also covered. Thus, the scope of the present disclosure should not be limited by particular examples, but should be determined only by a fair reading of the claims that follow. If reference signs related to drawings are placed in parentheses in a claim, they are solely for attempting to increase the intelligibility of the claim, and shall not be construed as limiting the scope of the claim.

Claims

1. A resistive interpolation mesh circuit (RIMC) for a time-to-digital converter (TDC) comprising:

two or more ring oscillators (ROs) arranged in a two-dimensional parallel configuration, all ROs having identical components,

each RO comprising an uneven number of three or more delay elements (DEs), each DE comprising an inverter having an input and an output, and a resistor coupled at one end to the input of the inverter, wherein the inverters of the DEs of each RO are connected in series and the output of the last inverter in the series connection is coupled to the input of the first inverter in the series connection;

wherein, between two consecutive ROs, one preceding and the other following in the parallel configuration, the input of the inverter of the DE of the following RO is coupled to the other end of the resistor of the DE of the same rank of the preceding RO, respectively, to generate a mesh circuit.

2. The RIMC according to claim 1, wherein each DE of the mesh circuit provides an output of the RIMC at the other end of the resistor.

3. The RIMC according to any of claims 1 to 2, wherein the inverters are current starved inverters.

4. The RIMC according to claim 3, wherein the inverters comprise PMOS and NMOS transistors, whereby the transistor width is selected based on desired oscillation frequency and power consumption of the TDC.

5. The RIMC according to any of claims 1 to 4, wherein all the resistors have the same performance characteristics within predefined variation ranges.

6. The RIMC according to claim 5, wherein the value of the resistors is selected to determine sub-delay resolution of the TDC.

7. The RIMC according to any of claims 1 to 6, wherein the number of ROs is selected based on a desired resolution of the TDC.

8. The RIMC according to claim 7, comprising 2^k ROs.

9. The RIMC according to any of claims 1 to 8, wherein the RIMC comprises at least four ROs and wherein the first and the last ROs of the parallel configuration are dummy ROs.

10. A TDC comprising a RIMC according to any of claims 1 to 9.

11. The TDC according to claim 10, further comprising:

a front-end readout circuit, and
a back-end readout circuit, coupled to the output of the front-end circuit.

12. The TDC according to claim 11, wherein the front-end readout circuit comprises:

a Time Capture Register (TCR) matrix, having one TCR for each stage of the RIMC, each TCR having as many inputs as the inverters belonging to the same rank of the RIMC, and
an XOR circuit, comprising one XOR element for each pair of inverters of the same stage of consecutive ROs, wherein a first input of each XOR element is coupled to the input of the first inverter of the pair and a second input is coupled to the input of the second inverter of the pair.

13. The TDC according to claim 11 or 12, wherein the back-end readout circuit is configured to aggregate the data from each stage of the mesh circuit and determine the RO where the transition occurred.

14. A 3D imaging system comprising a TDC according to any of claims 10 to 13.

15. A geographically distributed synchronous data transfer system comprising a TDC according to any of claims 10 to 13.

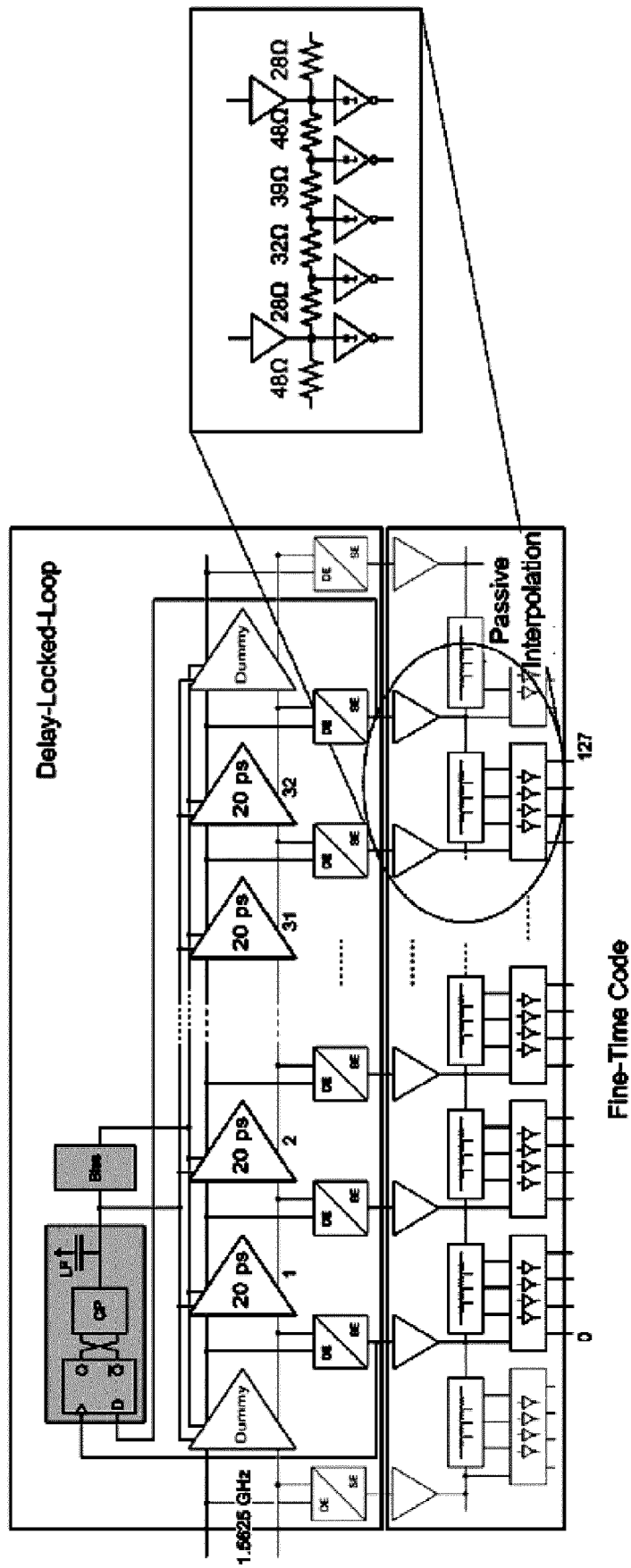
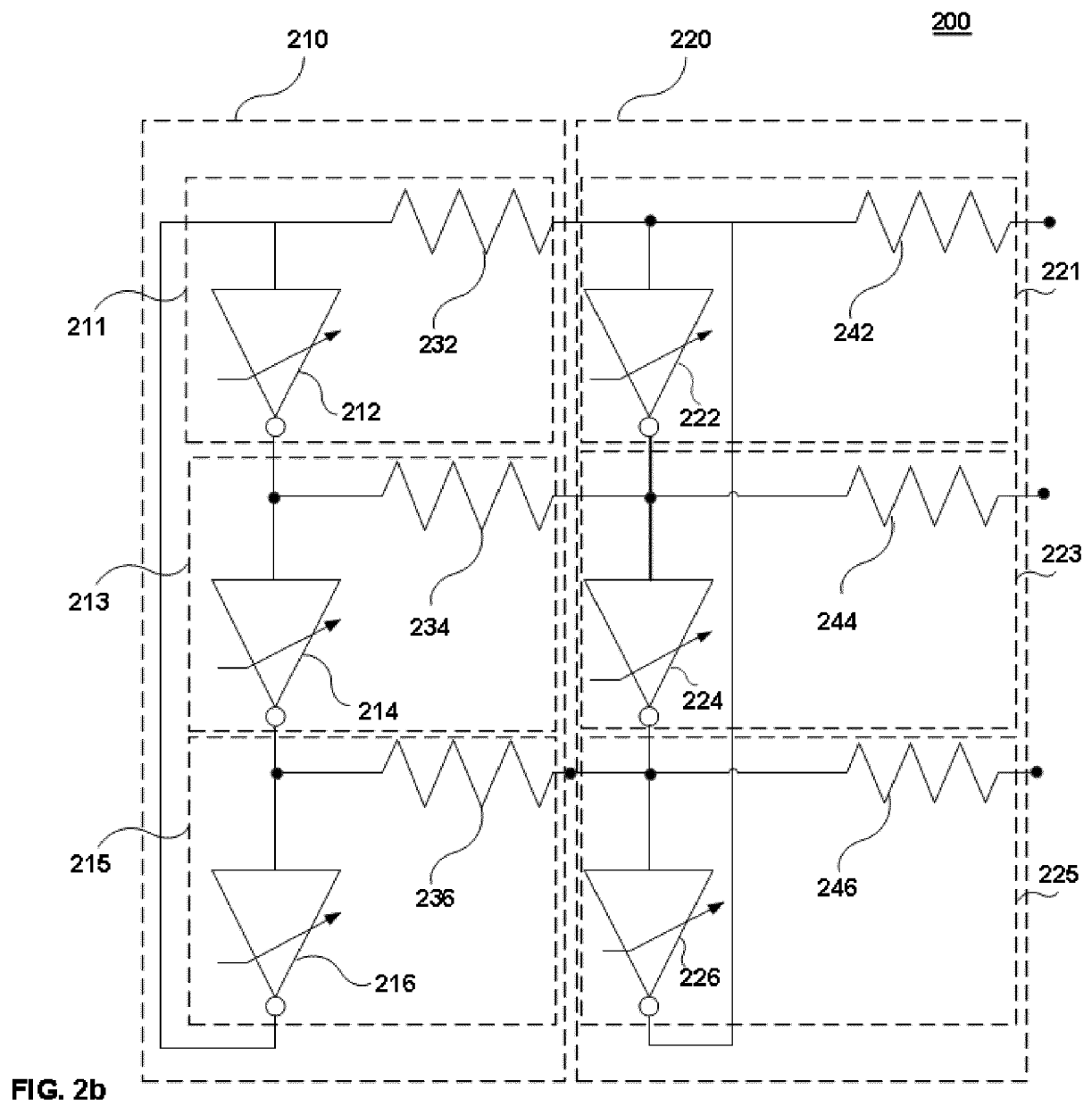
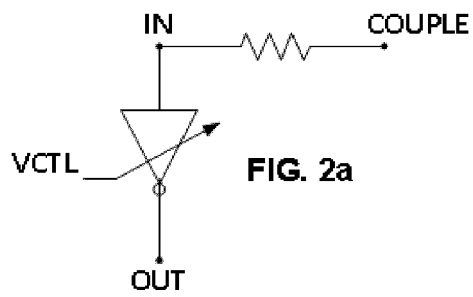


FIG. 1
(Prior Art)



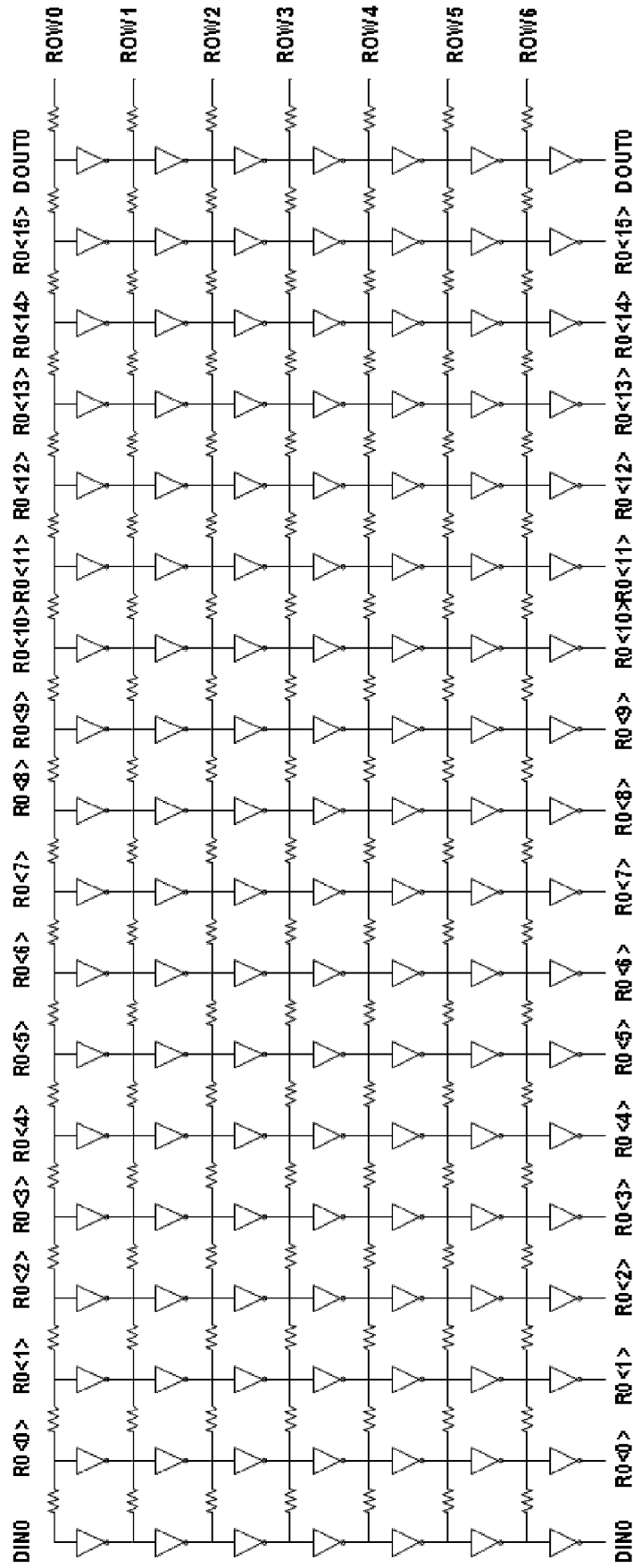
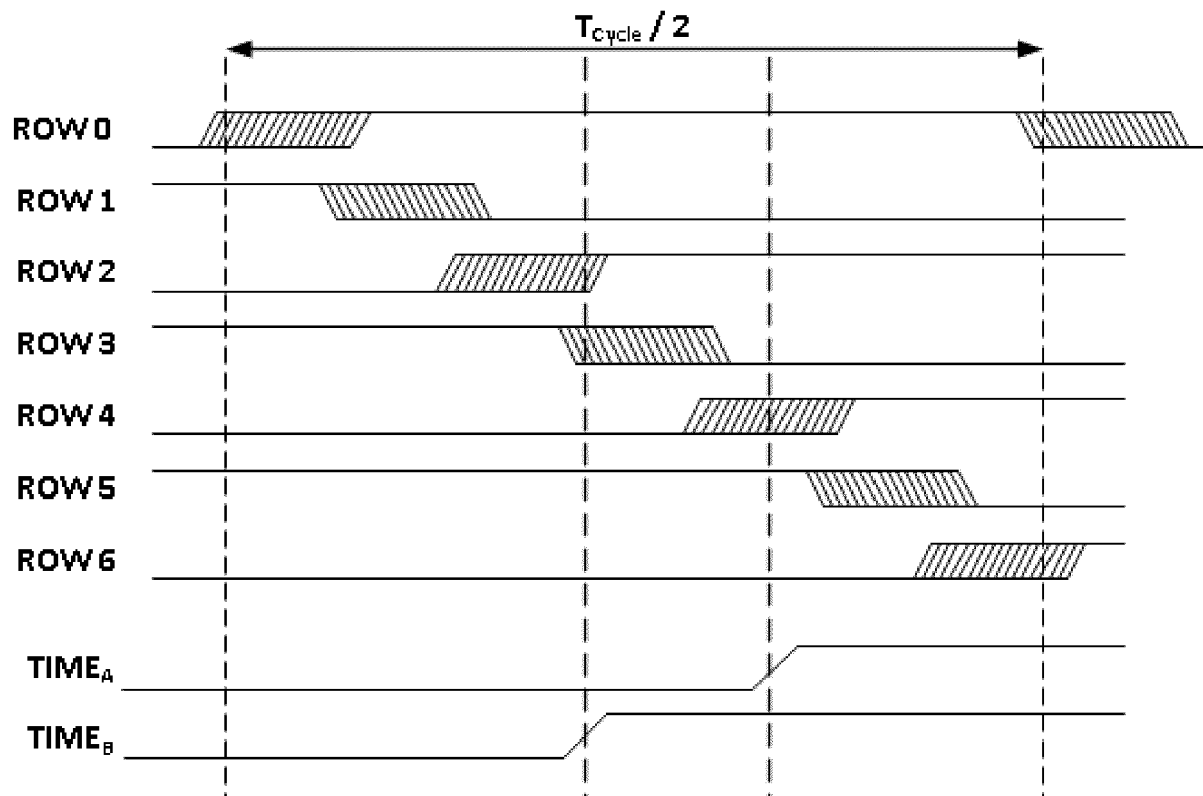


FIG. 3

**FIG. 4**

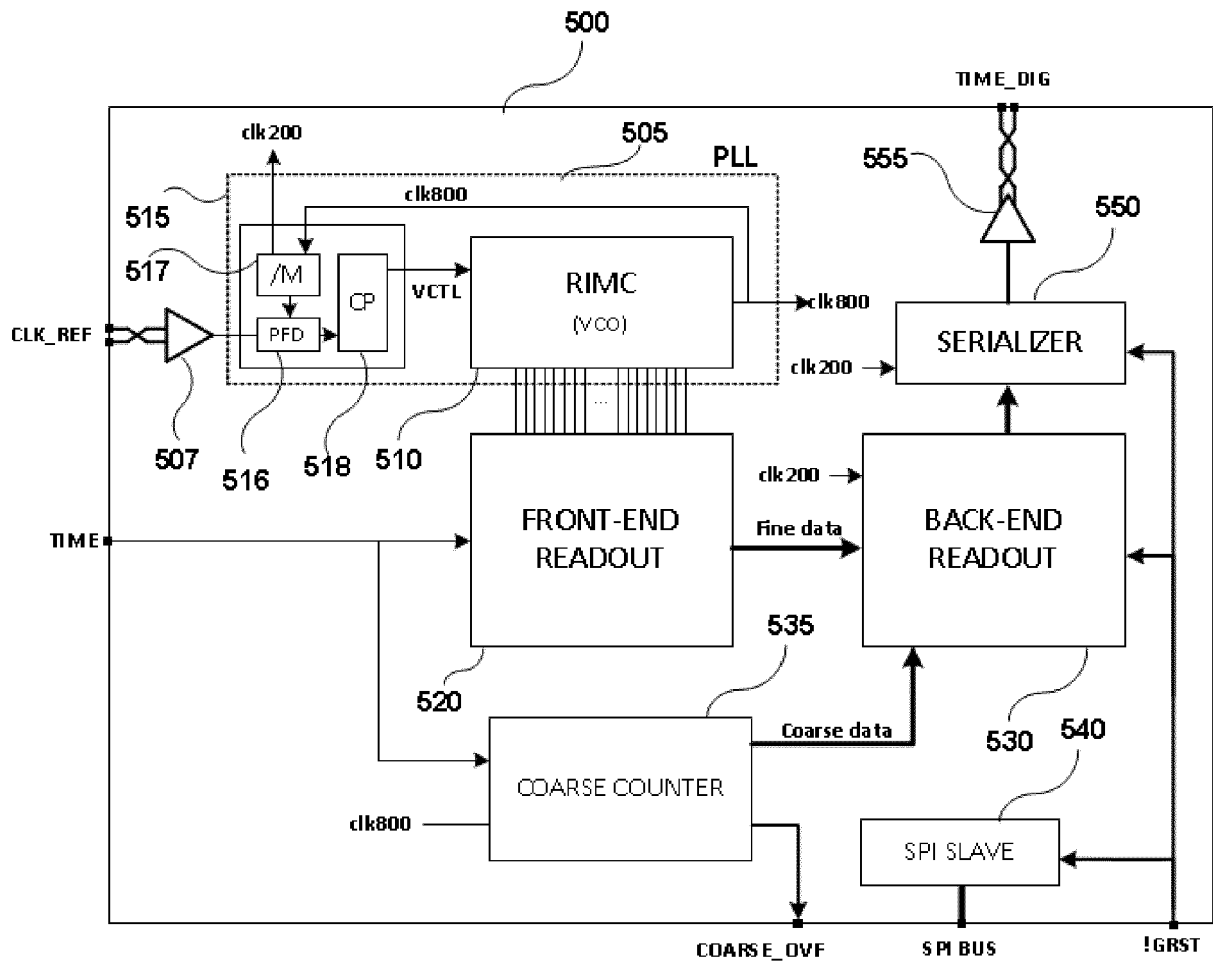


FIG. 5

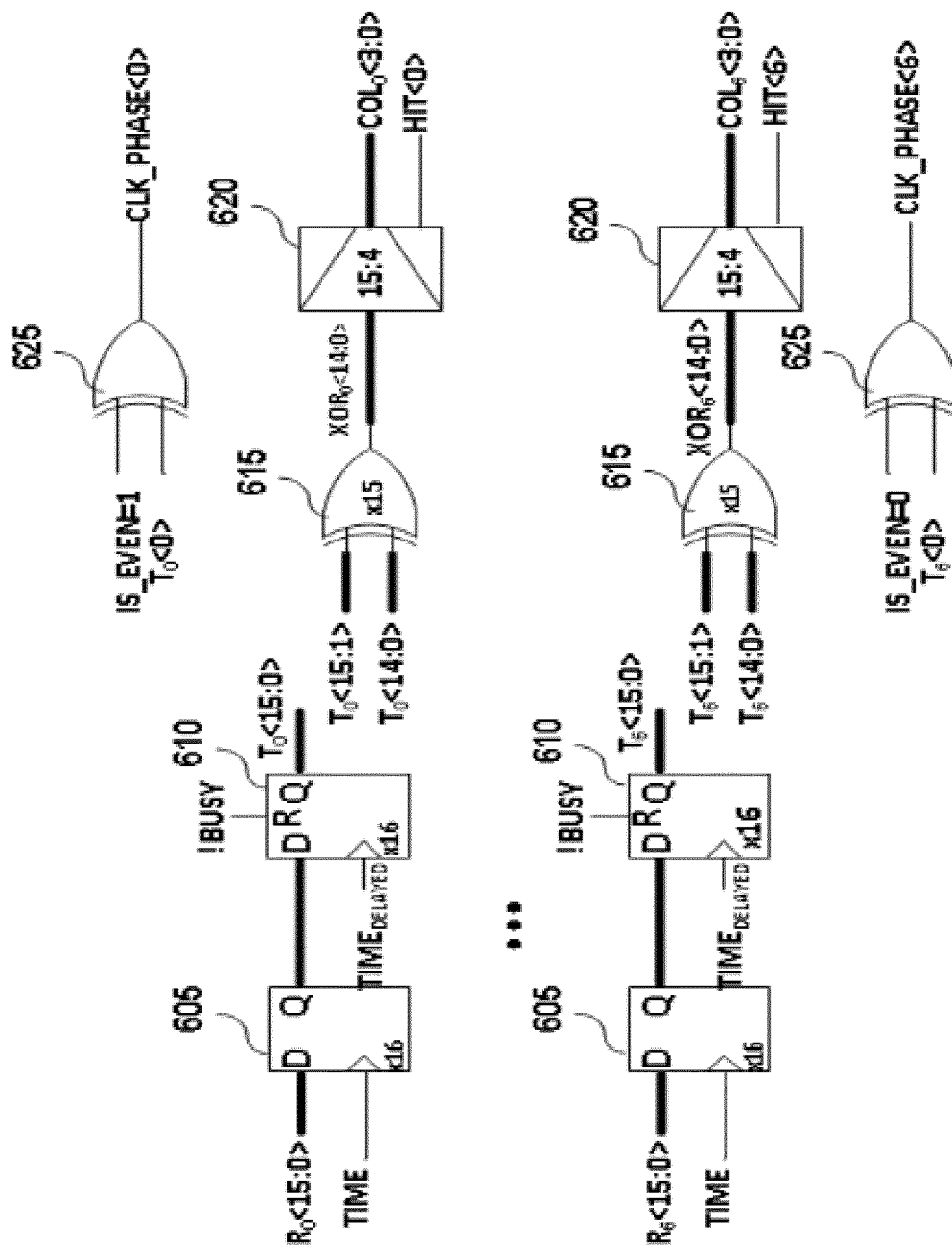
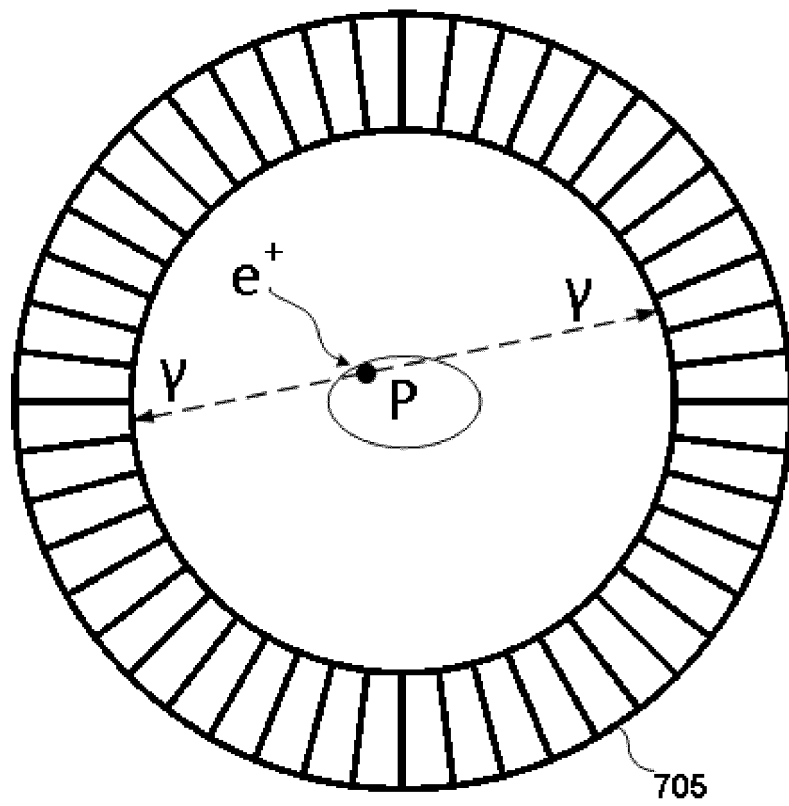


FIG. 6



700

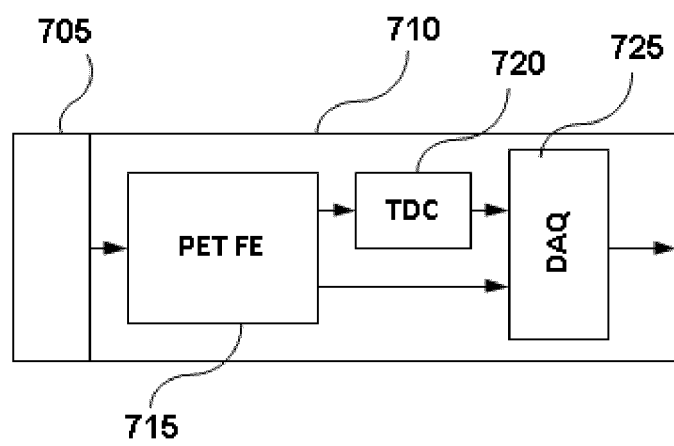


FIG. 7



EUROPEAN SEARCH REPORT

Application Number
EP 16 38 2039

5

10

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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Place of search The Hague		Date of completion of the search 7 July 2016	Examiner Pirozzi, Giuseppe
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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