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(54) **METHOD FOR CONTROLLING A CHARGE AND DISCHARGE CIRCUIT AND DIRECT POWER CONVERTER**

VERFAHREN ZUR STEUERUNG EINER LADE- UND ENTLADESCHALTUNG UND DIREKTLEISTUNGSWANDLER

MÉTHODE DE CONTRÔLE D'UN CIRCUIT DE CHARGE ET DE DÉCHARGE ET CONVERTISSEUR DIRECT DE PUISSANCE

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- **YOSHIYA OHNUMA ET AL: "A control method for a single-to-three-phase power converter with an active buffer and a charge circuit", ENERGY CONVERSION CONGRESS AND EXPOSITION (ECCE), 2010 IEEE, IEEE, PISCATAWAY, NJ, USA, 12 September 2010 (2010-09-12), pages 1801-1807, XP031787347, ISBN: 978-1-4244-5286-6**

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- YUKI NAKATA ET AL: "Fundamental verification of a single-to-single phase direct power converter for wireless power transfer systems", POWER ELECTRONICS AND DRIVE SYSTEMS (PEDS), 2013 IEEE 10TH INTERNATIONAL CONFERENCE ON, IEEE, 22 April 2013 (2013-04-22), pages 1003-1008, XP032420900, DOI: 10.1109/PEDS.2013.6527166 ISBN: 978-1-4673-1790-0

Description

Technical Field

[0001] This invention relates to a method for controlling a charge and discharge circuit and to a direct power converter.

Background Art

[0002] Patent Documents 1, 3, and 4 disclose direct power converters. The direct power converters disclosed by these include a booster circuit and a capacitor that maintains a voltage boosted by the booster circuit. In the DC power to be supplied to an inverter, the power from the capacitor and the power obtained from a diode rectifier are appropriately processed. Consequently, the inverter receives increased DC voltage.

[0003] Although Patent Document 2 also discloses a direct power converter, the direct power converter includes neither the booster circuit nor the capacitor. On the other hand, the direct power converter includes, at an input side of the inverter, an LC filter that suppresses a carrier current of the inverter.

[0004] The direct power converter disclosed by Patent Document 1 includes not only the booster circuit and the capacitor but also the LC filter. Furthermore, the direct power converter includes a diode between the capacitor and the LC filter to prevent a current from flowing from the capacitor to the LC filter.

[0005] In any of Patent Documents 1, 2, and 5, a current for suppressing resonance of the LC filter (hereinafter referred to as a "suppressing current") is obtained from a voltage generated in a reactor of the LC filter (or a voltage generated in a capacitor of the LC filter), and is superimposed on a current flowing through the inverter (hereinafter referred to as an "inverter current").

[0006] Patent Document 6 provides a direct-type power conversion device capable of preventing an unnecessary increase in a voltage across a capacitor even if the capacitor forming a filter is provided on an output side of a rectifier. A first capacitor C3 is provided between a first power-supply line LH and a second power-supply line LL. A charge and discharge circuit 4 is provided on the opposite side of a diode rectifier 2 from the first capacitor 3 and on the first power-supply line LH and the second power-supply line LL. The charge and discharge circuit 4 includes a second capacitor C4 provided between the first power-supply line LH and the second power-supply line LL, and a first switch Sc connected in series to the second capacitor C4 on the first power-supply line LH side. A step-up circuit 4b steps up a rectified voltage from the diode rectifier and charges the second capacitor C4. A current-blocking section 4c is provided on the first power-supply line LH or the second power-supply line LL between the first capacitor C3 and the second capacitor C4, and prevents a current from flowing from the second capacitor C4 to the first capacitor C3.

[0007] Patent Document 7 provides a power converter that suppresses high-frequency disturbance to an alternating-current power supply. A controller (10) includes subtracters (101, 105), a command value corrector (103), and a control block (102). The subtracter (101) obtains a deviation (Δv_0) of an output voltage (v_0) applied from a switching power-supply circuit (61) to a second load ($C_{dc} + \text{Load}$) with respect to its command value (v_0^*). The control block (102) performs PI control on the basis of the deviation (Δv_0) to generate a command value (id_c^*) for a current (id_c) flowing in a coil (d). The command value corrector (103) corrects the command value (id_c^*) such that high-frequency components of a current (i_L) flowing in a first power-supply line (21), with respect to the fundamental frequency of an input current (i_{u1} , i_{v1}), are consumed in the switching power-supply circuit (61). The subtracter (105) obtains a deviation (Δid_c) between the corrected command value (id_c^*) and the current (id_c). Commands (r_1 , r_2) for switches are generated on the basis of the deviation (Δid_c).

Prior-Art Documents

Patent Documents

[0008]

Patent Document 1: Japanese Patent Application Laid-Open No. 2014-96976

Patent Document 2: Japanese Patent No. 4067021

Patent Document 3: Japanese Patent Application Laid-Open No. 2011-193678

Patent Document 4: Japanese Patent Application Laid-Open No. 2014-82926

Patent Document 5: Japanese Patent No. 5257533

Patent Document 6: JP 2014 096976 A

Patent Document 7: EP 2 009 774 A1

Summary

Problems to be Solved by the Invention

[0009] The LC filter is provided for attenuating, in the current flowing through the inverter, a carrier frequency component of the inverter. Thus, the resonance frequency of the LC filter is preferably set to a fraction of the carrier frequency.

[0010] In such a case, when the suppressing current is superimposed on the inverter current, delay in sampling of a control system that controls the inverter and in updating of a command value is not negligible.

[0011] In Patent Document 1, changing, in a DC voltage to be input from a DC link to the inverter, a value indicating a ratio of a voltage to be applied from the diode rectifier is accompanied by a change in the DC voltage, thus reducing an average of the DC voltage.

[0012] The present invention has an object of providing a technique for preventing the sampling of the control

system that controls the inverter and the updating of a command value from being degraded, even when the resonance of the LC filter is suppressed using the suppressing current.

Means to Solve the Problems

[0013] The method for controlling a charge and discharge circuit according to the present invention is a method for controlling a charge and discharge circuit in a direct power converter according to claim 1. Preferred embodiments of the method of claim 1 are set forth in the dependent claims 2 to 6.

[0014] Further, the present invention relates to a direct power converter having the features of claim 7. Preferred embodiments of the direct power converter are set forth in the dependent claims 8 to 10.

Effects of the Invention

[0015] The method for controlling a charge and discharge circuit and the direct power converter according to this invention prevent sampling of a control system that controls an inverter and updating of a command value from being degraded, even when the resonance of an LC filter is suppressed using a suppressing current.

[0016] The object, features, aspects and advantages of the present invention will become more apparent from the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0017]

FIG. 1 illustrates an example schematic configuration of a direct power converter;
 FIG. 2 is a block diagram illustrating an example schematic configuration of a control device that controls the direct power converter;
 FIG. 3 is a circuit diagram illustrating an equivalent circuit of the direct power converter in FIG. 1;
 FIG. 4 is a block diagram of the equivalent circuit of FIG. 3 when the equivalent circuit is understood as configuring a control system;
 FIG. 5 is a block diagram illustrating a modification of the block diagram in FIG. 4;
 FIG. 6 is a block diagram illustrating a modification of the block diagram in FIG. 5;
 FIG. 7 is a block diagram illustrating a modification of the block diagram in FIG. 6;
 FIGS. 8 to 11 are graphs representing waveforms of an input current, a reactor voltage, and a current;
 FIG. 12 is a circuit diagram illustrating a modified positional relationship between a reactor and a diode rectifier;
 FIG. 13 is a circuit diagram illustrating a modified positional relationship between a capacitor, the re-

actor, and the diode rectifier;

FIG. 14 is a circuit diagram illustrating a modification of the diode rectifier; and

FIG. 15 is a block diagram exemplifying a structure of a resonance suppression controller and the surroundings of the reactor.

Description of Embodiments

10 A. Structure of direct power converter

[0018] Before specifically describing the distinctive technique of an embodiment, a structure of a direct power converter to which the technique is to be applied will be described. Since basic operations of the structure itself are known by Patent Document 1, the details will be omitted herein.

[0019] As illustrated in FIG. 1, the direct power converter includes a diode rectifier 2, an LC filter 3, a charge and discharge circuit 4, and an inverter 5. DC power lines LH and LL function as a DC link between the inverter 5 and the charge and discharge circuit 4. A potential higher than a potential applied to the DC power line LL is applied to the DC power line LH.

[0020] The diode rectifier 2 has an input side to which a single-phase AC voltage (V_{in}) is applied from a single-phase AC power source 1, and an output side.

[0021] The diode rectifier 2 single-phase full-wave rectifies the single-phase AC voltage V_{in} to convert the single-phase AC voltage V_{in} into a voltage $V_r (= |V_{in}|)$, and outputs the voltage V_r from the output side.

[0022] Furthermore, an AC current i_{in} (hereinafter referred to as an "input current i_{in} ") flows from the single-phase AC power source 1 into the input side of the diode rectifier 2.

[0023] The diode rectifier 2 includes diodes D21 to D24. The diodes D21 to D24 form a bridge circuit.

[0024] The LC filter 3 includes a reactor L3 and a capacitor C3. The capacitor C3 is provided between the DC power lines LH and LL. The reactor L3 is connected in series with the DC power line LH or LL (the DC power line LH closer to the output side of the diode rectifier 2 in the example of FIG. 1), while being more distant from the inverter 5 than the capacitor C3 is.

[0025] The capacitor C3 is, for example, a film capacitor, and has a capacitance smaller than that of an electrolytic capacitor. The capacitor C3 hardly smoothes the voltage V_r output by the diode rectifier 2. Thus, although a both-end voltage V_3 across the capacitor C3 is a DC voltage, it ripples with the same period as that with which the voltage V_r ripples.

[0026] The combination of the diode rectifier 2 and the LC filter 3 can be understood as a rectifying circuit 203 having the input side to which the single-phase AC voltage V_{in} is applied and the output side connected between the DC power lines LH and LL. Although the voltage V_r is applied between the reactor L3 and the capacitor C3 that are connected in series in FIG. 1, output of the diode

rectifier 2 is applied to the capacitor C3 without through the reactor L3, depending on a structure of the rectifying circuit 203. Such modifications of the rectifying circuit will be described later.

[0027] The charge and discharge circuit 4 is provided closer to the inverter 5 with respect to the capacitor C3, and includes a buffer circuit 4a, a booster circuit 4b, and a current blocking unit 4c. The buffer circuit 4a includes a capacitor C4, and provides and receives powers to and from the DC power lines LH and LL.

[0028] The buffer circuit 4a further includes a transistor (here, an insulated gate bipolar transistor: hereinafter abbreviated as an "IGBT") Sc connected in antiparallel to a diode D42. The transistor Sc is connected in series with the capacitor C4 between the DC power lines LH and LL, where the transistor Sc is closer to the DC power line LH with respect to the capacitor C4. The antiparallel connection herein means parallel connection in which forward directions are opposite to each other. Specifically, the forward direction of the transistor Sc is a direction from the DC power line LL to the DC power line LH. The forward direction of the diode D42 is a direction from the DC power line LH to the DC power line LL. The transistor Sc and the diode D42 can collectively be understood as one switch element (a first switch). In other words, the capacitor C4 is provided between the DC power lines LH and LL through the first switch.

[0029] The booster circuit 4b boosts the both-end voltage V3 across the capacitor C3 (a rectified voltage output by the rectifying circuit 203 in the structure of FIG. 1) to charge the capacitor C4. The charge circuit 4b includes, for example, a diode D40, a reactor L4, and a transistor (here, an IGBT) SI. The diode D40 has a cathode and an anode. The cathode is connected between the first switch and the capacitor C4. The reactor L4 is connected between the DC power line LH and the anode of the diode D40. The transistor SI is connected between the DC power line LL and the anode of the diode D40. The transistor SI is connected in antiparallel to a diode D41. The transistor SI and the diode D41 can collectively be understood as one switch element (a second switch). This structure is known as a generally-called boost chopper.

[0030] The capacitor C4 is charged by the charge circuit 4b, and maintains a both-end voltage Vc higher than the both-end voltage V3. Specifically, a current IL2 is caused to flow from the DC power line LH to the DC power line LL through the second switch to accumulate energy in the reactor L4. Then, the second switch is turned OFF, so that this energy is accumulated in the capacitor C4 through the diode D40. Since the current IL2 flows from the DC power line LH to the DC power line LL and the polarity is not reversed, the current IL2 is a direct current.

[0031] The both-end voltage Vc is higher than the both-end voltage V3, so that a current basically does not flow through the diode D42. Thus, whether the first switch is conducting or non-conducting depends solely on whether the transistor Sc is conducting or non-conducting.

Thus, the first switch including not only the transistor Sc but also the diode D42 may be referred to as a switch Sc.

[0032] Upon conduction of the switch Sc, the capacitor C4 discharges to the DC link. A duty ratio at which this switch Sc is brought into conduction will be referred to as a discharge duty dc. The discharge duty dc is controllable.

[0033] Furthermore, since the DC power line LH is higher in potential than the DC power line LL, a current basically does not flow through the diode D41. Thus, whether the second switch is conducting or non-conducting depends solely on whether the transistor SI is conducting or non-conducting. Thus, the second switch including not only the transistor SI but also the diode D41 may be referred to as a switch SI.

[0034] The booster circuit 4b determines whether the current IL2 is caused to flow through the capacitor C4. Specifically, the switch SI chops the current IL2 at a boost duty dl that is a duty ratio. This chopping is performed by comparison between the boost duty dl and a carrier C2 to be described later.

[0035] The current blocking unit 4c is provided in the DC power line LH or LL between the capacitors C3 and C4, and blocks the current from flowing from the capacitor C4 to the capacitor C3. The booster circuit 4b makes the both-end voltage Vc across the capacitor C4 higher than the both-end voltage V3 across the capacitor C3. However, the current blocking unit 4c blocks the current from flowing from the capacitor C4 to the capacitor C3. Thus, the both-end voltage V3 avoids an influence of the both-end voltage Vc.

[0036] The current blocking unit 4c is materialized by, for example, a diode D43. The diode D43 is provided in the DC power line LH in the example of FIG. 1. The forward direction of the diode D43 is a direction from the diode rectifier 2 to the inverter 5.

[0037] The inverter 5 converts, to an AC voltage, a DC voltage Vdc generated between the DC power lines LH and LL closer to the inverter 5 than to the charge and discharge circuit 4, and outputs the AC voltage to output terminals Pu, Pv, and Pw.

[0038] The inverter 5 includes six switching elements Sup, Svp, Swp, Sun, Svn, and Swn. The switching elements Sup, Svp, and Swp are connected between the DC power line LH and the output terminals Pu, Pv, and Pw, respectively. The switching elements Sun, Svn, and Swn are connected between the DC power line LL and the output terminals Pu, Pv, and Pw, respectively. The inverter 5 forms a generally-called voltage source inverter, and includes six diodes.

[0039] Each of the six diodes is arranged such that its cathode is directed toward the DC power line LH and its anode is directed toward the DC power line LL. One of the six diodes is connected in parallel to the switching element Sup between the output terminal Pu and the DC power line LH. Likewise, the other five diodes are connected in parallel to the switching elements Svp, Swp, Sun, Svn, and Swn, respectively.

[0040] For example, IGBTs are used as the switching elements Sup, Svp, Swp, Sun, Svn, and Swn. The six diodes are connected in antiparallel to the IGBTs that are used as the switching elements Sup, Svp, Swp, Sun, Svn, and Swn, respectively.

[0041] An inductive load 6 is, for example, a rotary machine, and rotates according to an AC voltage from the inverter 5.

B. Control based on both-end voltage VL across reactor L3

[0042] FIG. 2 is a block diagram illustrating an example schematic configuration of a control device 10 that controls the direct power converter. The control device 10 includes a block 10a functioning as a control device for the charge and discharge circuit 4, and a block 10b functioning as a control device for the inverter 5.

[0043] The block 10a includes a current distribution factor generator 11, a resonance suppression controller 15, an adder 13, a subtractor 17, a chopper controller 16, comparators 12 and 14, and carrier generators 23 and 24.

[0044] The block 10b includes an output voltage command generator 31, arithmetic units 32 and 33, comparators 34 and 35, and an OR/AND operation unit 36.

[0045] The current distribution factor generator 11 receives an amplitude Vm of the single-phase AC voltage Vin, an amplitude Im of the input current Iin, a command value Idc* of a DC current Idc to be input to the inverter 5, a command value Vc* of the both-end voltage Vc, and a power angular velocity ω . The amplitudes Vm and Im and the power angular velocity ω are sensed by, for example, a known sensor provided, and are input to the current distribution factor generator 11. The command values Idc* and Vc* are input by an external configuration that is not illustrated.

[0046] The current distribution factor generator 11 outputs a rectifying duty drec, a discharge duty dc, a zero duty dz, and a current command value Ib*.

[0047] The rectifying duty drec is a duty ratio at which the power is supplied from the rectifying circuit 203 (to put it differently, this can be "from the diode rectifier 2" because the LC filter 3 is normally a low-pass filter having a cut-off frequency significantly higher than that of the power angular velocity ω) to the DC link. Since the both-end voltage Vc is higher than the both-end voltage V3, no current flows from the rectifying circuit 203 to the DC link during the conduction of the switch Sc. Thus, a sum of the rectifying duty drec and the discharge duty dc is smaller than 1. The zero duty dz is a duty ratio at which neither the rectifying circuit 203 nor the charge and discharge circuit 4 supplies power to the DC link. A sum of the zero duty dz, the rectifying duty drec, and the discharge duty dc is equal to 1.

[0048] The current command value Ib* is a command value of the current IL2 to be input to the booster circuit 4b, specifically, the current IL2 that is caused to flow

through the reactor L4, when no consideration is given to suppression of the resonance of the LC filter 3.

[0049] Since Patent Documents 1, 3, and 4 describe a method for determining the rectifying duty drec, the discharge duty dc, the zero duty dz, and the current command value Ib* in detail, the details will be omitted herein.

[0050] The resonance suppression controller 15 receives a both-end voltage VL across the reactor L3 (hereinafter referred to as a "reactor voltage VL"). As illustrated in FIG. 1, when the reactor L3 is provided in series with the DC power line LH to be closer to the capacitor C3 than to the diode rectifier 2, an end of the reactor L3 that is closer to the capacitor C3 is used as a reference for the reactor voltage VL. The reactor voltage VL is sensed by a known technique. The resonance suppression controller 15 outputs a larger correction value as the reactor voltage VL is higher. The resonance suppression controller 15 outputs, for example, a product of the reactor voltage VL and a predetermined value k (>0) as a correction value k·VL. This correction value k·VL can be understood as being directly proportional to the reactor voltage VL.

[0051] The subtractor 17 subtracts the correction value k·VL from the current command value Ib*, and outputs a corrected current command value (Ib* - k·VL). This corresponds to use of the value (-k·VL) as a command value of the suppressing current that is caused to flow through the reactor L4.

[0052] The current command value (Ib* - k·VL) to be a target value of the current IL2 is reduced more as the reactor voltage VL is higher. Accordingly, control for reducing the current IL2 is performed. When the reactor L3 is provided in series with the DC power line LL to be closer to the capacitor C3 than to the diode rectifier 2, an end of the reactor L3 that is closer to the diode rectifier 2 is used as a reference for the reactor voltage VL. In other words, when the reactor L3 is provided between the diode rectifier 2 and the capacitor C3, a direction opposite to the direction in which the current flows through the reactor L3 is used as a positive polarity of the reactor voltage VL.

[0053] The adder 13 adds the rectifying duty drec and the zero duty dz, and the comparator 12 compares the result (drec + dz) with a carrier C1. The carrier C1 is generated by the carrier generator 23.

[0054] A result of the comparator 12 is output as a switching signal SSc to be provided to the switch Sc. The comparator 12 outputs as the switching signal SSc, for example, a signal activated while the carrier C1 is larger than or equal to the value (drec + dz). The switch Sc is turned ON with activation of the switching signal SSc.

[0055] The chopper controller 16 receives the both-end voltage Vc and the single-phase AC voltage Vin (more precisely, respective values of the voltages), and outputs the boost duty dl on the basis of the corrected current command value (Ib* - k·VL). Since a technique for determining the boost duty dl from the both-end voltage Vc, the single-phase AC voltage Vin, and the induct-

ance L_m of the reactor L_4 on the basis of the given current command value is also a known technique from, for example, Patent Documents 1, 3, and 4, the details will be omitted herein.

[0056] The comparator 14 compares the boost duty d_l with the carrier C_2 . The carrier C_2 is generated by the carrier generator 24. A result of the comparator 14 is output as a control signal SSI for controlling the closing and opening of the switch SI . The comparator 14 outputs as the control signal SSI , for example, a signal activated while the carrier C_2 is smaller than or equal to the boost duty d_l . The switch SI is turned ON with activation of the switching signal SSI .

[0057] The output voltage command generator 31 generates phase voltage commands V_u^* , V_v^* , and V_w^* . The output voltage command generator 31 receives a rotational velocity ω_m of the inductive load 6, and a command value ω_m^* of the rotational velocity ω_m in the example of FIG. 2. The rotational velocity ω_m is sensed by a known sensor, and the command value ω_m^* is input by an external configuration that is not illustrated. The output voltage command generator 31 generates the phase voltage commands V_u^* , V_v^* , and V_w^* using a known method to reduce a deviation between the rotational velocity ω_m and the command value ω_m^* .

[0058] The arithmetic unit 32 receives the rectifying duty d_{rec} , the zero duty d_z , the discharge duty d_c , and the phase voltage commands V_u^* , V_v^* , and V_w^* . The arithmetic unit 32 calculates and outputs values $(d_{rec} + d_z + d_c \cdot V_x^*)$ (x represents u , v , and w). The arithmetic unit 33 receives the rectifying duty d_{rec} and the phase voltage commands V_u^* , V_v^* , and V_w^* , and calculates and outputs values $(d_{rec} \cdot (1 - V_x^*))$.

[0059] The comparator 34 compares the values $(d_{rec} + d_z + d_c \cdot V_x^*)$ with the carrier C_1 , whereas the comparator 35 compares the values $(d_{rec} \cdot (1 - V_x^*))$ with the carrier C_1 . The comparator 34 outputs, for example, signals activated while the carrier C_1 is larger than or equal to the values $(d_{rec} + d_z + d_c \cdot V_x^*)$, whereas the comparator 35 outputs, for example, signals activated while the carrier C_1 is smaller than or equal to the values $(d_{rec} \cdot (1 - V_x^*))$.

[0060] Accordingly, since the carrier C_1 can be used for any of the blocks 10a and 10b, the carrier generator 23 is illustrated across the boundary between the blocks 10a and 10b d in FIG. 2.

[0061] The OR/AND operation unit 36 receives results of the comparison by the comparator 34 and 35. ORs of the results of the comparison by the comparator 34 and 35 are output as switching signals $SSup$, $SSvp$, and $SSwp$ to be provided, respectively, to the switching elements Sup , Svp , and Swp , and negation of these are output as switching signals $SSun$, $SSvn$, and $SSwn$ to be provided, respectively, to the switching elements Sun , Svn , and Swn .

[0062] The following will describe that correction of the current command value using the correction value $k \cdot V_L$ suppresses the resonance of the LC filter 3.

[0063] FIG. 3 is a circuit diagram illustrating an equivalent circuit of the direct power converter of FIG. 1. Here, a current I_L that flows through the reactor L_3 and a current I_3 that flows through the capacitor C_3 were introduced.

5 The current I_L is output from the diode rectifier 2. Thus, considering the reference of the reactor voltage V_L (or a direction of a positive polarity of the reactor voltage V_L), it is clear that this equivalent circuit holds even when the reactor L_3 is connected in series with any one of the DC power lines LH and LL between the diode rectifier 2 and the capacitor C_3 .

10 **[0064]** As understood from FIG. 1, the current flowing from the LC filter 3 branches into the booster circuit 4b and the current blocking unit 4c. Thus, with introduction of an inverter current I_4 that flows through the inverter 5, the direct current I_{L2} that flows through the booster circuit 4b and the inverter current I_4 to be output to the inverter 5 can be equivalently illustrated as current sources that are both connected in parallel to the capacitor C_3 . Here, the current I_{L2} is understood as a value obtained by subtracting the correction value $k \cdot V_L$ from a current I_b . Under the assumption of $k = 0$, the current I_b is understood as a current that flows through the reactor L_4 using the current command value I_b^* as a command value.

20 **[0065]** FIG. 4 is a block diagram of the equivalent circuit of FIG. 3 when the equivalent circuit is understood as configuring a control system. This block diagram can be modified into block diagrams in FIGS. 5, 6, and 7 in order according to Patent Document 2. In order to materialize the control system for suppressing the resonance, the command value V_L^* is 0.

30 **[0066]** The block diagram of FIG. 7 shows that the direct power converter in FIG. 1 can be understood as a feedback system on the reactor voltage V_L using the voltage V_r as a disturbance. FIG. 7 also shows that the command value V_L^* is used as a target value of the reactor voltage V_L and that the both-end voltage V_3 is controlled to be identical to the voltage V_r because the reactor voltage V_L follows the command value $V_L^* = 0$ without depending on the voltage V_r . Accordingly, fluctuations in voltage subject to the resonance of the LC filter 3 are suppressed.

35 **[0067]** Under the control according to the embodiment, the suppressing current (this corresponds to the correction value $k \cdot V_L$ of the current I_b) is not superimposed on the inverter current I_4 but the current I_{L2} is controlled by the reactor voltage V_L . Since the current I_{L2} is controlled by an operation of the booster circuit 4b, that is, chopping by the switch SI , a control period of the current I_{L2} is shorter than a control period of the inverter 5. According to FIG. 2, the carrier C_2 is shorter in period than the carrier C_1 , and the current I_{L2} is controlled by the reactor voltage V_L at a frequency higher than that at which the inverter 5 is controlled.

40 **[0068]** It is clear that sampling of the control system that controls the inverter 5 and updating of a command value are prevented from being degraded even when the resonance of the LC filter 3 is suppressed using the sup-

pressing current according to the embodiment.

[0069] FIGS. 8 to 11 are graphs representing waveforms of the input current i_{in} , the reactor voltage V_L , and the current i_{L2} when the DC voltage V_{dc} is controlled at a constant value.

[0070] FIGS. 8 and 9 illustrate application of a control method (hereinafter provisionally referred to as "half-period control") for alternating between a period for charging the capacitor C4 (a "receiving period" according to Patent Document 3 where the discharge duty d_c is zero and the boost duty d_l is positive) and a period for discharging the capacitor C4 (a "providing period" according to Patent Document 3 where the discharge duty d_c is positive) per half period of the voltage V_r (i.e., per quarter period of the single-phase AC voltage V_{in}) as disclosed by Patent Document 3.

[0071] With introduction of a phase ωt of the single-phase AC voltage V_{in} , the providing period and the receiving period can be regarded as a period in which a cosine value $\cos(2\omega t)$ that is a cosine of a value twice the phase ωt is positive and a period in which this cosine value $\cos(2\omega t)$ is negative, respectively.

[0072] FIGS. 10 and 11 illustrate application of a control method for charging the capacitor C4 (hereinafter provisionally referred to as "charge-discharge control") with the current i_{L2} during at least a part of a period in which the discharge duty d_c is larger than 0 as disclosed by Patent Document 4.

[0073] Both FIGS. 8 and 10 illustrate that the correction using the correction value $k \cdot V_L$ is not performed. FIG. 8 illustrates that the current i_{L2} flows not during a proving period T1 but only during a receiving period T2 with the half-period control reflected. FIG. 10 illustrates that with the charge-discharge control reflected, the current i_{L2} flows not during a discharge period T4 (a period in which the boost duty d_l is zero) according to Patent Document 4 but only during a period T3 that is a sum of a charge period and a charge-discharge period (a period in which the boost duty d_l is positive) according to Patent Document 4.

[0074] Both FIGS. 9 and 11 illustrate that the correction using the correction value $k \cdot V_L$ is performed. FIG. 9 illustrates that the current i_{L2} flows also during the proving period T1 in FIG. 8. Furthermore, FIG. 11 illustrates that the current i_{L2} flows also during the discharge period T4 in FIG. 10.

[0075] Thus, the boost duty d_l is influenced by the correction value $k \cdot V_L$ with the process of the chopper controller 16 (see FIG. 2), and is not necessarily set according to the definitions defined on the proving period and the receiving period in Patent Document 3 and defined on the charge period, the discharge period, and the charge-discharge period in Patent Document 4. However, the "half-period control" and the "charge-discharge control" will be provisionally used for the sake of simplicity in the following description, regardless of the presence or absence of the correction using the correction value $k \cdot V_L$.

[0076] As understood from the comparison between FIG. 8 and FIG. 9, ringing in the input current i_{in} is reduced with introduction of the correction using the correction value $k \cdot V_L$ under the half-period control. Similarly, as understood from the comparison between FIG. 10 and FIG. 11, ringing in the input current i_{in} is reduced with introduction of the correction using the correction value $k \cdot V_L$ under the charge-discharge control.

[0077] It is visually identified that such introduction of the correction using the correction value $k \cdot V_L$ enables reduction in the influence of the resonance of the LC filter 3, regardless of whether the half-period control or the charge-discharge control is applied.

[0078] When the half-period control is applied, the current command value i_b^* is set to zero during the proving period T1. Thus, only when the reactor voltage V_L is negative, the suppressing current flows during the proving period T1.

[0079] When the charge-discharge control is applied, the current command value i_b^* is larger than the correction value $k \cdot V_L$ during many periods. Thus, the corrected current command value ($i_b^* - k \cdot V_L$) is also positive during many periods. Accordingly, an advantageous effect of causing the suppressing current to flow through the reactor L4 and suppressing the resonance of the LC filter 3 is enhanced, regardless of whether the reactor voltage V_L that is a both-end voltage across the reactor L3 is positive or negative.

C. Modification

[0080] In the rectifying circuit 203, the positional relationship between the diode rectifier 2, the capacitor C3, and the reactor L3 is not limited to the one in the examples. Since the reactor component and the capacitor component of the diode rectifier 2 itself are negligible, various modifications to be described below are possible.

[0081] FIG. 12 is a circuit diagram illustrating a modified positional relationship between the reactor L3 and the diode rectifier 2. In the examples above, the reactor L3 is more distant from the inverter 5 than the capacitor C3 is, and is directly connected in series with the DC power line LH (obviously, the reactor L3 may be directly connected to the DC power line LL). However, the reactor L3 is more distant from the inverter 5 than the capacitor C3 is, and is indirectly connected in series with the DC power line LH through the diode rectifier 2. Specifically, the reactor L3 is connected in series with the single-phase AC power source 1 with respect to the input side of the diode rectifier 2.

[0082] With the structure, the reactor L3 is more distant from the inverter 5 than the diode rectifier 2 is, and the voltage V_r is a rectified voltage V_{rec} output by the rectifying circuit 203. In these cases, the reactor L3 is connected in series with the single-phase AC power source 1 with respect to the input side of the diode rectifier 2. Thus, it is clear that the equivalent circuit in FIG. 3 also applies to such a structure similarly as the above stated

embodiment, and the same functions and advantages above can be obtained by regarding a positive direction of the reactor voltage VL (polarity of the reactor voltage VL) as a direction of the single-phase AC voltage Vin from the high potential to the low potential.

[0083] Such a modification adopts a structure for determining the reactor voltage VL with reference to a value obtained by measuring a potential difference across the reactor L3 in a fixed direction and to the direction of the single-phase AC voltage Vin from the high potential to the low potential and outputting a correction value on the basis of the reactor voltage VL, as a replacement for the resonance suppression controller 15 (see FIG. 2),

[0084] FIG. 15 is a block diagram exemplifying a structure of a resonance suppression controller 151 adopted as a replacement for the resonance suppression controller 15 illustrated in FIG. 2, and the surroundings of the reactor L3 (see FIG. 1) when the reactor L3 is more distant from the inverter 5 than the diode rectifier 2 is.

[0085] Here, a potential difference VL1 across the reactor L3 is used with reference to the potential of the end of the reactor L3 that is closer to the diode rectifier 2. Specifically, a potential at a connection point between the reactor L3, an anode of the diode D21, and a cathode of the diode D22 serves as a reference of the potential difference.

[0086] The resonance suppression controller 151 receives the potential difference VL1 and the single-phase AC voltage Vin (more precisely, respective values thereof). The resonance suppression controller 151 includes a polarity determining unit 15b that determines a polarity of the single-phase AC voltage Vin in one direction (for example, a direction of the single-phase AC voltage Vin indicated by an arrow in FIG. 15) and outputs a value 1 or -1 according to the positive sign or the negative sign, respectively. The positive or negative sign or the phase of the single-phase AC voltage Vin may be used for the determination. Here, a potential at a connection point between an anode of the diode D23 and a cathode of the diode D24 is used as a reference of the single-phase AC voltage Vin.

[0087] The resonance suppression controller 151 includes multipliers 15a and 15c. The multiplier 15a multiplies output of the polarity determining unit 15b by the potential difference VL1. Accordingly, the multiplier 15a yields the reactor voltage VL according to the embodiment. The multiplier 15c multiplies the reactor voltage VL by the predetermined value k to yield the correction value k·VL.

[0088] Obviously, the polarity determining unit 15b can determine the polarity of the single-phase AC voltage Vin and output a value k or -k according to the positive sign or the negative sign, respectively, which does not require the multiplier 15c. Furthermore, the resonance suppression controller 15 according to the embodiment can be regarded as having a structure in which the multiplier 15a and the polarity determining unit 15b are eliminated. Such a structure obviously obtains the same functions

and advantages of each embodiment.

[0089] FIG. 13 is a circuit diagram of a circuit further modified from FIG. 12, and illustrates a modified positional relationship between the reactor L3, the capacitor C3, and the diode rectifier 2. The capacitor C3 is directly connected between the DC power lines LH and LL in the above examples. However, the capacitor C3 is indirectly connected between the DC power lines LH and LL through the diode rectifier 2 in the structure illustrated in FIG. 13. Furthermore, the reactor L3 is more distant from the inverter 5 than the capacitor C3 is, and is indirectly connected in series with the DC power line LH through the diode rectifier 2. Specifically, the reactor L3 is connected in series with the single-phase AC power source 1 with respect to the input side of the diode rectifier 2 as well as the capacitor C3.

[0090] Such a structure obtains the functions and advantages of the embodiment similarly as the structure of FIG. 12, though the current I3 flowing through the capacitor C3 becomes an alternating current and thus the polarity of the both-end voltage V3 alternates. This is because in view of FIG. 7, the reactor voltage VL remains controlled at zero, regardless of whether the polarity of the current I3 flowing through the capacitor C3 and the polarity of the both-end voltage V3 are made different by the polarity of the single-phase AC voltage Vin, or even in the presence of the voltage Vr that acts as a disturbance.

[0091] Moreover, since the diode rectifier 2 also functions as the current blocking unit 4c, for example, the diode D43 in the structure of FIG. 13, an advantage of eliminating the need for the current blocking unit 4c is produced.

[0092] FIG. 14 is a circuit diagram of a circuit further modified from FIG. 13, and illustrates a modification of the diode rectifier 2. The diode rectifier 2 is divided into two groups one of which has a pair of diodes on a higher potential side input to the charge and discharge circuit 4 and the other of which is connected to the inverter 5.

[0093] Specifically, the diode rectifier 2 includes diodes D21a, D21b, D22, D23a, D23b, and D24. Anodes of the diodes D21a and D21b are connected to one end of the capacitor C3 in common, and anodes of the diodes D23a and D23b are connected to the other end of the capacitor C3 in common. Cathodes of the diodes D21a and D23a are connected to the DC power line LH in common, and both cathodes of the diodes D21b and D23b are connected to the switch SI through the reactor L4. In other words, the diode D21 doubles as the diode D21a and D21b and the diode D23 doubles as the diode D23a and D23b in the structure illustrated in FIG. 14 with respect to the circuit illustrated in FIG. 13. However, the reactor L4 is not directly connected to the DC power line LH in the charge and discharge circuit 4.

[0094] In such a structure, the diodes D21a, D23a, D22, and D24 form a bridge circuit that applies the voltage Vr to the DC power line LH, and the D21b, D23b, D22, and D24 form a bridge circuit that applies the voltage Vr

to the DC power line LH. Thus, the diode rectifier 2 can be understood as including these two bridge circuits. The structure obviously obtains the same functions and advantages of each embodiment.

[0095] While this invention has been described in detail, the foregoing description is in all aspects illustrative and does not restrict the invention. The scope of the invention is defined by the appended claims.

Claims

1. A method for controlling a charge and discharge circuit (4) in a direct power converter, said direct power converter including:

a first power supply line (LH);
 a second power supply line (LL) to which a potential lower than a potential applied to said first power supply line (LH) is applied;
 a rectifying circuit (203) having an input side to which a single-phase AC voltage (V_{in}) is applied, and an output side to be connected to said first and second power supply lines (LH, LL);
 an inverter (5) that receives a DC voltage (V_{dc}) that is a voltage between said first and second power supply lines (LH, LL); wherein said charge and discharge circuit (4) is provided between said first and second power supply lines (LH, LL) and between said output of the rectifying circuit (203) and the input of the inverter (5); and
 said rectifying circuit (203) includes:

a diode rectifier (2) that performs single-phase full-wave rectification;
 a first capacitor (C3) to be connected between said first and second power supply lines (LH, LL) directly or indirectly through said diode rectifier (2); and
 a first reactor (L3) to be connected in series with said first power supply line (LH) or said second power supply line (LL) directly or indirectly through said diode rectifier (2), said first reactor (L3) being connected between the output of the diode rectifier (2) and the first capacitor (C3) or between the output of the single-phase AC-voltage (V_{in}) and the input of the diode rectifier (2),
 said charge and discharge circuit (4) includes:

a buffer circuit (4a) including a second capacitor (C4) provided between said first and second power supply lines (LH, LL), said buffer circuit (4a) discharging said second capacitor (C4) at a controllable first duty ratio (dc), charg-

ing said second capacitor (C4) during a period in which a cosine value ($\cos(2\omega t)$) is negative, and discharging said second capacitor (C4) during a period in which said cosine value is positive, said cosine value being a cosine of a value twice a phase (ωt) of said single-phase AC voltage (V_{in}); and
 a booster circuit (4b) that boosts a rectified voltage (V_3 , V_r) output by said rectifying circuit (2) to charge said second capacitor (C4), and
 said method controls a DC current (I_{L2}) to be input to said booster circuit (4b) by a voltage (V_L) across said first reactor (L3) such that a control period of said DC current (I_{L2}) is shorter than a control period of said inverter (5) and such that said DC current (I_{L2}) is reduced with increasing voltage across said first inductor (L3).

2. The method for controlling a charge and discharge circuit according to claim 1, wherein said first reactor (L3) is provided between said diode rectifier (2) and said first capacitor (C3), and a direction opposite to a direction of a current flowing through said first reactor (L3) is used as a positive polarity of said voltage (V_L) across said first reactor (L3).
3. The method for controlling a charge and discharge circuit according to claim 1, wherein said first reactor (L3) is connected to the input side of said diode rectifier (2), and a direction of said single-phase AC voltage (V_{in}) from a high potential to a low potential is used as a positive polarity of said voltage (V_L) across said first reactor (L3).
4. The method for controlling a charge and discharge circuit according to one of claims 1 to 3, wherein said DC current (I_{L2}) is controlled using a second command value ($I_b^* - k \cdot V_L$) as a target value, said second command value being obtained by subtracting a correction value ($k \cdot V_L$) from a first command value (I_b^*) determined by an amplitude (I_m) of an AC current (i_{in}) to be input to said diode rectifier (2) and a voltage (V_r) to be output by said diode rectifier (2), said correction value being directly proportional to said voltage (V_L) across said first reactor (L3).
5. The method for controlling a charge and discharge circuit according to claim 4,

wherein said booster circuit (4b) includes a second reactor (L4) through which said DC current (I_{L2}) flows, and chops said DC current to deter-

mine whether to output said DC current to said second capacitor (C4), and
 said chopping is performed based on a result of comparison between a second duty ratio (dl) and a predetermined carrier (C2), said second duty ratio being determined using said second command value ($I_b^* - k \cdot V_L$), a voltage (V_c) across said second capacitor (C4), said single-phase AC voltage (V_{in}), and an inductance (L_m) of said second reactor (L4).

6. The method for controlling a charge and discharge circuit according to one of claims 1 to 5, wherein said buffer circuit (4a) charges said second capacitor (C4) during at least a part of a period in which said first duty ratio (dc) is larger than 0.
7. A direct power converter, including:

a first power supply line (LH);
 a second power supply line (LL) to which a potential lower than a potential applied to said first power supply (LH) line is applied;
 a rectifying circuit (203) having an input side to which a single-phase AC voltage (V_{in}) is applied, and an output side to be connected to said first and second power supply lines (LH, LL);
 an inverter (5) configured to receive a DC voltage (V_{dc}) that is a voltage between said first and second power supply lines (LH, LL); and
 a charge and discharge circuit (4) that is provided between the output of the rectifying circuit (203) and the input of the inverter (5) and between said first and second power supply lines (LH, LL); wherein
 said rectifying circuit (203) includes:

a diode rectifier (2) configured to perform single-phase full-wave rectification;
 a first capacitor (C3) connected between said first and second power supply lines (LH, LL) directly or indirectly through said diode rectifier (2); and
 a first reactor (L3) connected in series with said first power supply line (LH) or said second power supply line (LL) directly or indirectly through said diode rectifier (2), said first reactor (L3) being connected between the output of the diode rectifier (2) and the first capacitor (C3) or to the input side of the diode rectifier (2), and
 said charge and discharge circuit (4) including:

a buffer circuit (4a) including a second capacitor (C4) provided between said first and second power supply lines (LH, LL), said buffer circuit (4a) being

configured to discharge said second capacitor (C4) at a controllable first duty ratio (dc), wherein said buffer circuit (4a) is configured to charge said second capacitor (C4) during a period in which a cosine value ($\cos(2\omega t)$) is negative, and discharges said second capacitor (C4) during a period in which said cosine value is positive, said cosine value being a cosine of a value twice a phase (ωt) of said single-phase AC voltage (V_{in}); and
 a booster circuit (4b) configured to boost a rectified voltage (V_3 , V_r) output by said rectifying circuit (2) to charge said second capacitor (C4),
 said power converter further including a control device (10) for controlling said charge and discharge circuit (4) being configured to control a current (IL2) to be input to said booster circuit (4b) by a reactor voltage (V_L) across said first reactor (L3) in the rectifying circuit (203) such that a control period of said DC current (IL2) is shorter than a control period of said inverter (5) and such that said DC current (IL2) is reduced with increasing voltage across said first inductor (L3).

8. The direct power converter according to claim 7, wherein the control device (10) is configured to control said DC current (IL2) using a second command value ($I_b^* - k \cdot V_L$) as a target value, and said second command value being obtained by subtracting a correction value ($k \cdot V_L$) from a first command value (I_b^*) determined by an amplitude (I_m) of an AC current (i_{in}) to be input to said diode rectifier (2) and a voltage (V_r) to be output by said diode rectifier (2) and said correction value is directly proportional to said voltage (V_L) across said first reactor (L3), wherein said control device (10) comprises a subtractor (17) configured to subtract said correction value ($k \cdot V_L$) from said first command value (I_b^*) to obtain said second command value ($I_b^* - k \cdot V_L$).
9. The direct power converter according to claim 8, wherein said booster circuit (4b) includes a second reactor (L4) through which said DC current (IL2) flows, and is configured to chop said DC current to determine whether to output said DC current to said second capacitor (C4), and the control device (10) comprises:

a chopper controller (16) configured to determine a second duty ratio (dl); and
 a comparator (14) configured to compare said second duty ratio (dl) and a predetermined car-

rier (C2) to output a control signal (SS1) for controlling said chopping, wherein said chopper controller (16) is configured to determine said second duty ratio (dl) using said second command value ($I_b^* - k \cdot V_L$), a voltage (V_c) across said second capacitor (C4), said single-phase AC voltage (V_{in}), and an inductance (L_m) of said second reactor (L4).

10. The direct power converter according to one of the claims 7 to 9, further including a current blocking unit (4c) provided in said first power supply line (LH) or said second power supply line (LL), said current blocking unit (4c) being configured to block a current from flowing from said buffer circuit (4a) to said first capacitor (C3).

Patentansprüche

1. Verfahren zum Steuern einer Lade- und Entladeschaltung (4) in einem Direktleistungswandler, wobei der Direktleistungswandler einschließt:

eine erste Leistungsversorgungsleitung (LH);
eine zweite Leistungsversorgungsleitung (LL), an der ein Potential anliegt, das niedriger ist als ein an der ersten Leistungsversorgungsleitung (LH) anliegendes Potential;
eine Gleichrichterschaltung (203) mit einer Eingangsseite, an der eine einphasige Wechselspannung (V_{in}) anliegt, und einer Ausgangsseite, die mit der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) verbunden werden soll;
einen Wechselrichter (5), der eine Gleichspannung (V_{dc}) empfängt, bei der es sich um eine Spannung zwischen der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) handelt; wobei die Lade- und Entladeschaltung (4) zwischen der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) und zwischen dem Ausgang der Gleichrichterschaltung (203) und dem Eingang des Wechselrichters (5) vorgesehen ist; und die Gleichrichterschaltung (203) einschließt:

einen Diodengleichrichter (2), der einphasige Vollwellengleichrichtung durchführt; einen ersten Kondensator (C3), der direkt oder indirekt durch den Diodengleichrichter (2) zwischen die erste und die zweite Leistungsversorgungsleitung (LH, LL) geschaltet werden soll; und eine erste Drossel (L3), die direkt oder indirekt durch den Diodengleichrichter (2) mit der ersten Leistungsversorgungsleitung

(LH) oder der zweiten Leistungsversorgungsleitung (LL) in Reihe geschaltet werden soll, wobei die erste Drossel (L3) zwischen den Ausgang des Diodengleichrichters (2) und den ersten Kondensator (C3) oder zwischen den Ausgang der einphasigen Wechselspannung (V_{in}) und den Eingang des Diodengleichrichters (2) geschaltet wird, die Lade- und Entladeschaltung (4) einschließt:

eine Pufferschaltung (4a) mit einem zweiten Kondensator (C4), der zwischen der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) vorgesehen ist, wobei die Pufferschaltung (4a) den zweiten Kondensator (C4) mit einem steuerbaren ersten Tastverhältnis (dc) entlädt, den zweiten Kondensator (C4) während einer Periode, in der ein Kosinuswert ($\cos(2\omega t)$) negativ ist, lädt, und den zweiten Kondensator (C4) während einer Periode, in der der Kosinuswert positiv ist, entlädt, wobei der Kosinuswert ein Kosinus eines Werts ist, der doppelt so groß ist wie eine Phase (ωt) der einphasigen Wechselspannung (V_{in}); und eine Verstärkerschaltung (4b), die eine von der Gleichrichterschaltung (2) ausgegebene gleichgerichtete Spannung (V_3, V_r) verstärkt, um den zweiten Kondensator (C4) zu laden, und das Verfahren einen Gleichstrom (I_{L2}), der in die Verstärkerschaltung (4b) eingegeben werden soll, durch eine Spannung (V_L) über der ersten Drossel (L3) derart steuert, dass eine Steuerperiode des Gleichstroms (I_{L2}) kürzer ist als eine Steuerperiode des Wechselrichters (5), und derart, dass der Gleichstrom (I_{L2}) mit zunehmender Spannung über der ersten Drossel (L3) abnimmt.

2. Verfahren zum Steuern einer Lade- und Entladeschaltung nach Anspruch 1, wobei die erste Drossel (L3) zwischen dem Diodengleichrichter (2) und dem ersten Kondensator (C3) vorgesehen ist und eine Richtung, die einer Richtung eines durch die erste Drossel (L3) fließenden Stroms entgegengesetzt ist, als positive Polarität der Spannung (V_L) über der ersten Drossel (L3) verwendet wird.
3. Verfahren zum Steuern einer Lade- und Entladeschaltung nach Anspruch 1, wobei die erste Drossel (L3) mit der Eingangsseite des Di-

odengleichrichters (2) verbunden ist, und eine Richtung der einphasigen Wechselspannung (V_{in}) von einem hohen Potential zu einem niedrigen Potential als positive Polarität der Spannung (VL) über der ersten Drossel (L3) verwendet wird.

4. Verfahren zum Steuern einer Lade- und Entladeschaltung nach einem der Ansprüche 1 bis 3, wobei der Gleichstrom (IL2) unter Verwendung eines zweiten Sollwerts ($I_b^* - k \cdot VL$) als Zielwert gesteuert wird, wobei der zweite Sollwert durch Subtrahieren eines Korrekturwerts ($k \cdot VL$) von einem ersten Sollwert (I_b^*) erhalten wird, der durch eine Amplitude (I_m) eines Wechselstroms (i_{in}), der in den Diodengleichrichter (2) eingegeben werden soll, und eine Spannung (V_r), die von dem Diodengleichrichter (2) ausgegeben werden soll, bestimmt wird, wobei der Korrekturwert zu der Spannung (VL) über der ersten Drossel (L3) direkt proportional ist.
5. Verfahren zum Steuern einer Lade- und Entladeschaltung nach Anspruch 4,
 - wobei die Verstärkerschaltung (4b) eine zweite Drossel (L4) einschließt, durch die der Gleichstrom (IL2) fließt, und den Gleichstrom zerhackt, um zu bestimmen, ob der Gleichstrom an den zweiten Kondensator (C4) ausgegeben werden soll, und
 - das Zerhacken auf Basis eines Vergleichsergebnisses zwischen einem zweiten Tastverhältnis (d_l) und einem vorbestimmten Träger (C2) durchgeführt wird, wobei das zweite Tastverhältnis unter Verwendung des zweiten Sollwerts ($I_b^* - k \cdot VL$), einer Spannung (V_c) über dem zweiten Kondensator (C4), der einphasigen Wechselspannung (V_{in}) und einer Induktivität (L_m) der zweiten Drossel (L4) bestimmt wird.
6. Verfahren zum Steuern einer Lade- und Entladeschaltung nach einem der Ansprüche 1 bis 5, wobei die Pufferschaltung (4a) den zweiten Kondensator (C4) während mindestens eines Teils einer Periode, in der das erste Tastverhältnis (d_c) größer ist als 0, lädt.
7. Direktleistungswandler, der Folgendes einschließt:

eine erste Leistungsversorgungsleitung (LH);
 eine zweite Leistungsversorgungsleitung (LL),
 an der ein Potential anliegt, das niedriger ist als ein an der ersten Leistungsversorgungsleitung (LH) anliegendes Potential;
 eine Gleichrichterschaltung (203) mit einer Eingangsseite, an der eine einphasige Wechselspannung (V_{in}) anliegt, und einer Ausgangsseite, die mit der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) verbunden werden

soll;

einen Wechselrichter (5), der so konfiguriert ist, dass er eine Gleichspannung (V_{dc}) empfängt, bei der es sich um eine Spannung zwischen der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) handelt; und
 eine Lade- und Entladeschaltung (4), die zwischen dem Ausgang der Gleichrichterschaltung (203) und dem Eingang des Wechselrichters (5) und zwischen der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) vorgesehen ist; wobei
 die Gleichrichterschaltung (203) einschließt:

einen Diodengleichrichter (2), der so konfiguriert ist, dass er einphasige Vollwellengleichrichtung durchführt;
 einen ersten Kondensator (C3), der direkt oder indirekt durch den Diodengleichrichter (2) zwischen die erste und die zweite Leistungsversorgungsleitung (LH, LL) geschaltet ist; und
 eine erste Drossel (L3), die direkt oder indirekt durch den Diodengleichrichter (2) mit der ersten Leistungsversorgungsleitung (LH) oder der zweiten Leistungsversorgungsleitung (LL) in Reihe geschaltet ist, wobei die erste Drossel (L3) zwischen den Ausgang des Diodengleichrichters (2) und den ersten Kondensator (C3) geschaltet oder mit der Eingangsseite des Diodengleichrichters (2) verbunden ist, und
 wobei die Lade- und Entladeschaltung (4) einschließt:

eine Pufferschaltung (4a) mit einem zweiten Kondensator (C4), der zwischen der ersten und der zweiten Leistungsversorgungsleitung (LH, LL) vorgesehen ist, wobei die Pufferschaltung (4a) so konfiguriert ist, dass sie den zweiten Kondensator (C4) mit einem steuerbaren ersten Tastverhältnis (d_c) entlädt, wobei die Pufferschaltung (4a) so konfiguriert ist, dass sie den zweiten Kondensator (C4) während einer Periode, in der ein Kosinuswert ($\cos(2\omega t)$) negativ ist, lädt, und den zweiten Kondensator (C4) während einer Periode, in der der Kosinuswert positiv ist, entlädt, wobei der Kosinuswert ein Kosinus eines Werts ist, der doppelt so groß ist wie eine Phase (ωt) der einphasigen Wechselspannung (V_{in}); und
 eine Verstärkerschaltung (4b), die so konfiguriert ist, dass sie eine von der Gleichrichterschaltung (2) ausgegebene gleichgerichtete Spannung (V_3 , V_r)

verstärkt, um den zweiten Kondensator (C4) zu laden, wobei der Leistungswandler weiter eine Steuervorrichtung (10) zum Steuern der Lade- und Entladeschaltung (4) einschließt, die so konfiguriert ist, dass sie einen Strom (IL2), der in die Verstärkerschaltung (4b) eingegeben werden soll, durch eine Drosselspannung (VL) über der ersten Drossel (L3) in der Gleichrichterschaltung (203) derart steuert, dass eine Steuerperiode des Gleichstroms (IL2) kürzer ist als eine Steuerperiode des Wechselrichters (5), und derart, dass der Gleichstrom (IL2) mit zunehmender Spannung über der ersten Drossel (L3) abnimmt.

8. Direktleistungswandler nach Anspruch 7, wobei die Steuervorrichtung (10) so konfiguriert ist, dass sie den Gleichstrom (IL2) unter Verwendung eines zweiten Sollwerts ($I_b^* - k \cdot VL$) als Zielwert steuert, und wobei der zweite Sollwert durch Subtrahieren eines Korrekturwerts ($k \cdot VL$) von einem ersten Sollwert (I_b^*) erhalten wird, der durch eine Amplitude (I_m) eines Wechselstroms (i_{in}), der in den Diodengleichrichter (2) eingegeben werden soll, und eine Spannung (V_r), die von dem Diodengleichrichter (2) ausgegeben werden soll, bestimmt wird, und der Korrekturwert zu der Spannung (VL) über der ersten Drossel (L3) direkt proportional ist, wobei die Steuervorrichtung (10) einen Subtrahierer (17) umfasst, der so konfiguriert ist, dass er den Korrekturwert ($k \cdot VL$) von dem ersten Sollwert (I_b^*) subtrahiert, um den zweiten Sollwert ($I_b^* - k \cdot VL$) zu erhalten.
9. Direktleistungswandler nach Anspruch 8, wobei die Verstärkerschaltung (4b) eine zweite Drossel (L4) einschließt, durch die der Gleichstrom (IL2) fließt, und so konfiguriert ist, dass sie den Gleichstrom zerhackt, um zu bestimmen, ob der Gleichstrom an den zweiten Kondensator (C4) ausgegeben werden soll, und die Steuervorrichtung (10) umfasst:

eine Zerhacker-Steuereinheit (16), die so konfiguriert ist, dass sie ein zweites Tastverhältnis (dl) bestimmt; und einen Komparator (14), der so konfiguriert ist, dass er das zweite Tastverhältnis (dl) und einen vorbestimmten Träger (C2) vergleicht, um ein Steuersignal (SS1) zum Steuern des Zerhackens auszugeben, wobei die Zerhacker-Steuereinheit (16) so konfiguriert ist, dass sie das zweite Tastverhältnis (dl) unter Verwendung des zweiten Sollwerts ($I_b^* - k \cdot VL$), einer Spannung (V_c) über dem zweiten Kondensator (C4), der einphasigen Wechselspannung (V_{in}) und einer Induktivität (L_m) der zweiten Drossel (L4)

bestimmt.

10. Direktleistungswandler nach einem der Ansprüche 7 bis 9, weiter einschließend eine Stromsperreinheit (4c), die in der ersten Leistungsversorgungsleitung (LH) oder der zweiten Leistungsversorgungsleitung (LL) vorgesehen ist, wobei die Stromsperreinheit (4c) so konfiguriert ist, dass sie einen Stromfluss von der Pufferschaltung (4a) zum ersten Kondensator (C3) sperrt.

Revendications

1. Procédé de commande d'un circuit de charge et de décharge (4) dans un convertisseur de courant continu, ledit convertisseur de courant continu incluant :

une première ligne d'alimentation électrique (LH) ;
une seconde ligne d'alimentation électrique (LL) à laquelle un potentiel inférieur à un potentiel appliqué à ladite première ligne d'alimentation électrique (LH) est appliqué ;
un circuit redresseur (203) présentant un côté d'entrée auquel une tension CA monophasée (V_{in}) est appliquée, et un côté de sortie devant être connecté auxdites première et seconde lignes d'alimentation électrique (LH, LL) ;
un onduleur (5) qui reçoit une tension CC (V_{dc}) qui est une tension entre lesdites première et seconde lignes d'alimentation électrique (LH, LL) ; dans lequel
ledit circuit de charge et de décharge (4) est prévu entre lesdites première et seconde lignes d'alimentation électrique (LH, LL) et entre ladite sortie du circuit redresseur (203) et l'entrée de l'onduleur (5) ; et
ledit circuit redresseur (203) inclut :

un redresseur à diode (2) qui réalise un redressement à onde entière monophasée ;
un premier condensateur (C3) devant être connecté entre lesdites première et seconde lignes d'alimentation électrique (LH, LL) directement ou indirectement à travers ledit redresseur à diode (2) ; et
une première bobine de réactance (L3) devant être connectée en série avec ladite première ligne d'alimentation électrique (LH) ou ladite seconde ligne d'alimentation électrique (LL) directement ou indirectement à travers ledit redresseur à diode (2), ladite première bobine de réactance (L3) étant connectée entre la sortie du redresseur à diode (2) et le premier condensateur (C3) ou entre la sortie de la tension CA monophasée (V_{in}) et l'entrée du redresseur à dio-

de (2),
ledit circuit de charge et de décharge (4)
inclut :

un circuit tampon (4a) incluant un second condensateur (C4) prévu entre lesdites première et seconde lignes d'alimentation électrique (LH, LL), ledit circuit tampon (4a) déchargeant ledit second condensateur (C4) à un premier facteur de marche (de) pouvant être commandé, chargeant ledit second condensateur (C4) durant une période au cours de laquelle une valeur de cosinus ($\cos(2\omega t)$) est négative, et déchargeant ledit second condensateur (C4) durant une période au cours de laquelle ladite valeur de cosinus est positive, ladite valeur de cosinus étant un cosinus d'une valeur de deux fois une phase (ωt) de ladite tension CA monophasée (V_{in}) ; et

un circuit survolteur (4b) qui élève une tension redressée (V_3 , V_r) émise en sortie par ledit circuit redresseur (2) pour charger ledit second condensateur (C4), et

ledit procédé commande un courant CC (IL2) devant entrer dans ledit circuit survolteur (4b) au moyen d'une tension (VL) aux bornes de ladite première bobine de réactance (L3) de sorte qu'une période de commande dudit courant CC (IL2) soit plus courte qu'une période de commande dudit onduleur (5) et de sorte que ledit courant CC (IL2) soit réduit avec une augmentation de tension aux bornes de ladite première bobine d'inductance (L3).

2. Procédé de commande d'un circuit de charge et de décharge selon la revendication 1, dans lequel ladite première bobine de réactance (L3) est prévue entre ledit redresseur à diode (2) et ledit premier condensateur (C3), et un sens opposé à un sens d'un courant circulant à travers ladite première bobine de réactance (L3) est utilisé comme polarité positive de ladite tension (VL) aux bornes de ladite première bobine de réactance (L3).

3. Procédé de commande d'un circuit de charge et de décharge selon la revendication 1, dans lequel ladite première bobine de réactance (L3) est connectée au côté d'entrée dudit redresseur à diode (2), et un sens de ladite tension CA monophasée (V_{in}) d'un haut potentiel à un bas potentiel est utilisé comme polarité positive de ladite tension (VL) aux bornes de ladite première bobine de réactance (L3).

4. Procédé de commande d'un circuit de charge et de décharge selon l'une des revendications 1 à 3, dans lequel ledit courant CC (IL2) est commandé en utilisant une seconde valeur de commande ($I_{b^*} - k \cdot VL$) comme valeur cible, ladite seconde valeur de commande étant obtenue en soustrayant une valeur de correction ($k \cdot VL$) d'une première valeur de commande (I_{b^*}) déterminée par une amplitude (I_m) d'un courant CA (lin) devant entrer dans ledit redresseur à diode (2) et une tension (V_r) devant être émise en sortie par ledit redresseur à diode (2), ladite valeur de correction étant directement proportionnelle à ladite tension (VL) aux bornes de ladite première bobine de réactance (L3).

5. Procédé de commande d'un circuit de charge et de décharge selon la revendication 4,

dans lequel ledit circuit survolteur (4b) inclut une seconde bobine de réactance (L4) à travers laquelle ledit courant CC (IL2) circule, et hache ledit courant CC pour déterminer s'il faut émettre en sortie ledit courant CC vers ledit second condensateur (C4), et

ledit hachage est réalisé sur la base d'un résultat de comparaison entre un second facteur de marche (dl) et une porteuse prédéterminée (C2), ledit second facteur de marche étant déterminé en utilisant ladite seconde valeur de commande ($I_{b^*} - k \cdot VL$), une tension (V_c) aux bornes dudit second condensateur (C4), ladite tension CA monophasée (V_{in}) et une inductance (L_m) de ladite seconde bobine de réactance (L4).

6. Procédé de commande d'un circuit de charge et de décharge selon l'une des revendications 1 à 5, dans lequel ledit circuit tampon (4a) charge ledit second condensateur (C4) durant au moins une partie d'une période au cours de laquelle ledit premier facteur de marche (dc) est supérieur à 0.

7. Convertisseur de courant continu, incluant :

une première ligne d'alimentation électrique (LH) ;

une seconde ligne d'alimentation électrique (LL) à laquelle un potentiel inférieur à un potentiel appliqué à ladite première ligne d'alimentation électrique (LH) est appliqué ;

un circuit redresseur (203) présentant un côté d'entrée auquel une tension CA monophasée (V_{in}) est appliquée, et un côté de sortie devant être connecté auxdites première et seconde lignes d'alimentation électrique (LH, LL) ;

un onduleur (5) configuré pour recevoir une tension CC (V_{dc}) qui est une tension entre lesdites première et seconde lignes d'alimentation électrique (LH, LL) ; et

un circuit de charge et de décharge (4) qui est prévu entre la sortie du circuit redresseur (203) et l'entrée de l'onduleur (5) et entre lesdites première et seconde lignes d'alimentation électrique (LH, LL) ; dans lequel

ledit circuit redresseur (203) inclut :

un redresseur à diode (2) configuré pour réaliser un redressement à onde entière monophasée ;

un premier condensateur (C3) connecté entre lesdites première et seconde lignes d'alimentation électrique (LH, LL) directement ou indirectement à travers ledit redresseur à diode (2) ; et

une première bobine de réactance (L3) connectée en série avec ladite première ligne d'alimentation électrique (LH) ou ladite seconde ligne d'alimentation électrique (LL) directement ou indirectement à travers ledit redresseur à diode (2), ladite première bobine de réactance (L3) étant connectée entre la sortie du redresseur à diode (2) et le premier condensateur (C3) ou au côté d'entrée du redresseur à diode (2), et

ledit circuit de charge et de décharge (4) incluant :

un circuit tampon (4a) incluant un second condensateur (C4) prévu entre lesdites première et seconde lignes d'alimentation électrique (LH, LL), ledit circuit tampon (4a) étant configuré pour décharger ledit second condensateur (C4) à un premier facteur de marche (de) pouvant être commandé, dans lequel ledit circuit tampon (4a) est configuré pour charger ledit second condensateur (C4) durant une période au cours de laquelle une valeur de cosinus ($\cos(2\omega t)$) est négative, et décharge ledit second condensateur (C4) durant une période au cours de laquelle ladite valeur de cosinus est positive, ladite valeur de cosinus étant un cosinus d'une valeur de deux fois une phase (ωt) de ladite tension CA monophasée (V_{in}) ; et

un circuit survolteur (4b) configuré pour élever une tension redressée (V_3 , V_r) émise en sortie par ledit circuit redresseur (2) pour charger ledit second condensateur (C4),

ledit convertisseur de courant incluant en outre un dispositif de commande (10) pour commander ledit circuit de charge et de décharge (4) qui est configuré pour commander un courant

(IL2) devant entrer dans ledit circuit survolteur (4b) au moyen d'une tension de bobine de réactance (VL) aux bornes de ladite première bobine de réactance (L3) dans le circuit redresseur (203), de sorte qu'une période de commande dudit courant CC (IL2) soit plus courte qu'une période de commande dudit onduleur (5) et de sorte que ledit courant CC (IL2) soit réduit avec une augmentation de tension aux bornes de ladite première bobine d'inductance (L3).

8. Convertisseur de courant continu selon la revendication 7, dans lequel le dispositif de commande (10) est configuré pour commander ledit courant CC (IL2) en utilisant une seconde valeur de commande ($I_b^* - k \cdot VL$) comme valeur cible, et ladite seconde valeur de commande étant obtenue en soustrayant une valeur de correction ($k \cdot VL$) d'une première valeur de commande (I_b^*) déterminée par une amplitude (I_m) d'un courant CA (I_{in}) devant entrer dans ledit redresseur à diode (2) et une tension (V_r) devant être émise en sortie par ledit redresseur à diode (2) et ladite valeur de correction est directement proportionnelle à ladite tension (VL) aux bornes de ladite première bobine de réactance (L3), dans lequel ledit dispositif de commande (10) comprend un soustracteur (17) configuré pour soustraire ladite valeur de correction ($k \cdot VL$) de ladite première valeur de commande (I_b^*) pour obtenir ladite seconde valeur de commande ($I_b^* - k \cdot VL$).
9. Convertisseur de courant continu selon la revendication 8, dans lequel ledit circuit survolteur (4b) inclut une seconde bobine de réactance (L4) à travers laquelle ledit courant CC (IL2) circule, et est configuré pour hacher ledit courant CC pour déterminer s'il faut émettre en sortie ledit courant CC vers ledit second condensateur (C4), et le dispositif de commande (10) comprend :

un dispositif de commande de hacheur (16) configuré pour déterminer un second facteur de marche (dl) ; et

un comparateur (14) configuré pour comparer ledit second facteur de marche (dl) et une porteuse prédéterminée (C2) pour émettre en sortie un signal de commande (SS1) pour commander ledit hachage, dans lequel ledit dispositif de commande de hacheur (16) est configuré pour déterminer ledit second facteur de marche (dl) en utilisant ladite seconde valeur de commande ($I_b^* - k \cdot VL$), une tension (V_c) aux bornes dudit second condensateur (C4), ladite tension CA monophasée (V_{in}) et une inductance (L_m) de ladite seconde bobine de réactance (L4).

10. Convertisseur de courant continu selon l'une quelconque des revendications 7 à 9, incluant en outre une unité de blocage de courant (4c) prévue dans ladite première ligne d'alimentation électrique (LH) ou ladite seconde ligne d'alimentation électrique (LL), ladite unité de blocage de courant (4c) étant configurée pour bloquer un courant afin qu'il ne circule pas dudit circuit tampon (4a) audit premier condensateur (C3).

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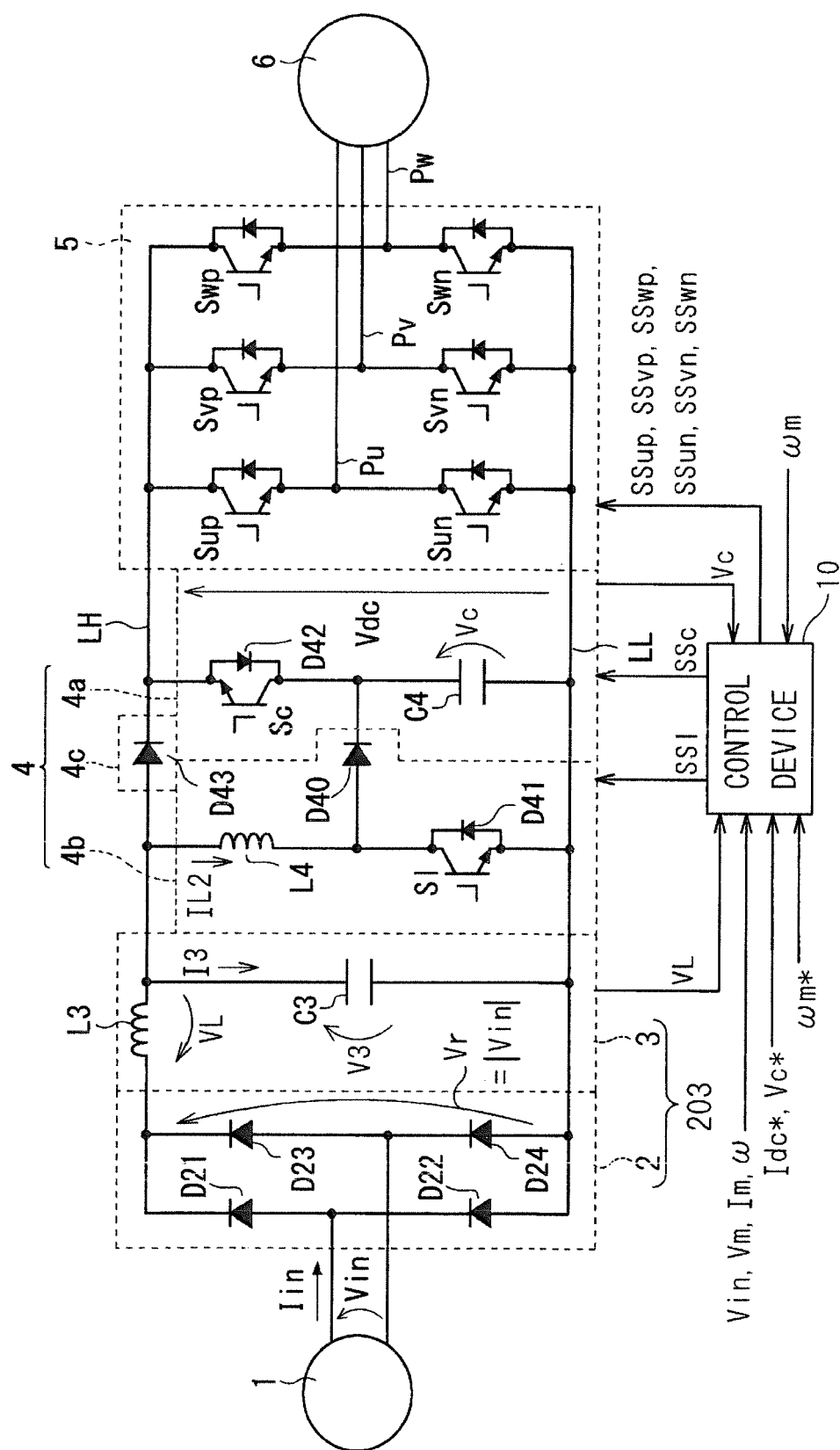
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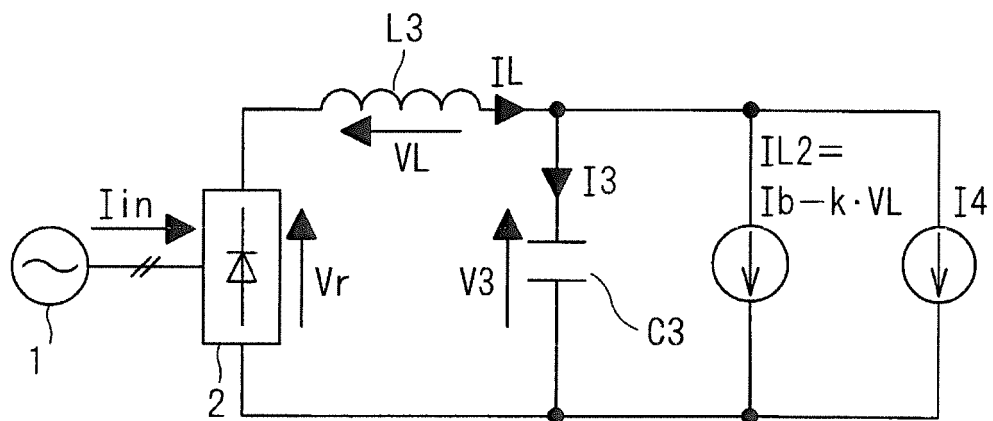
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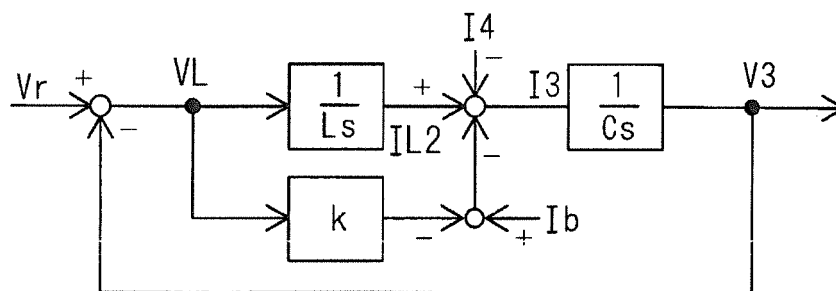
FIG. 1



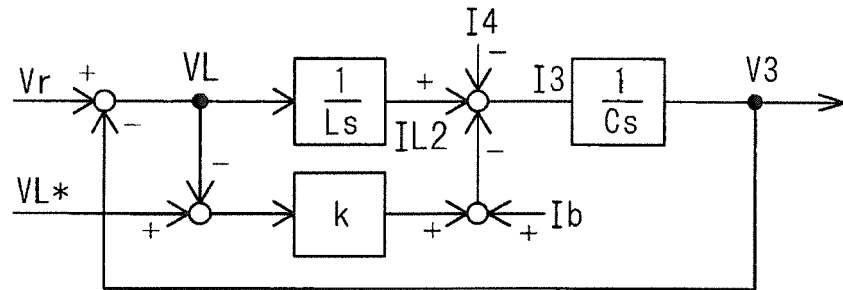
F I G . 3



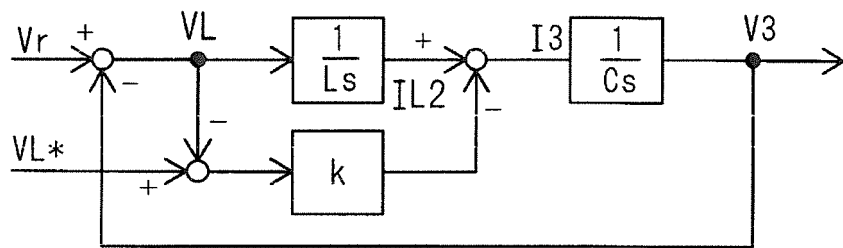
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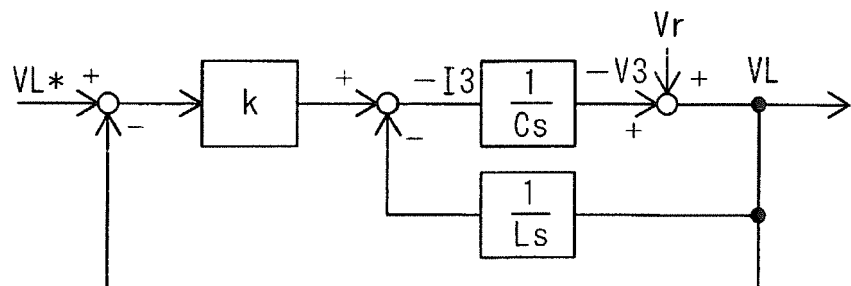
F I G . 5



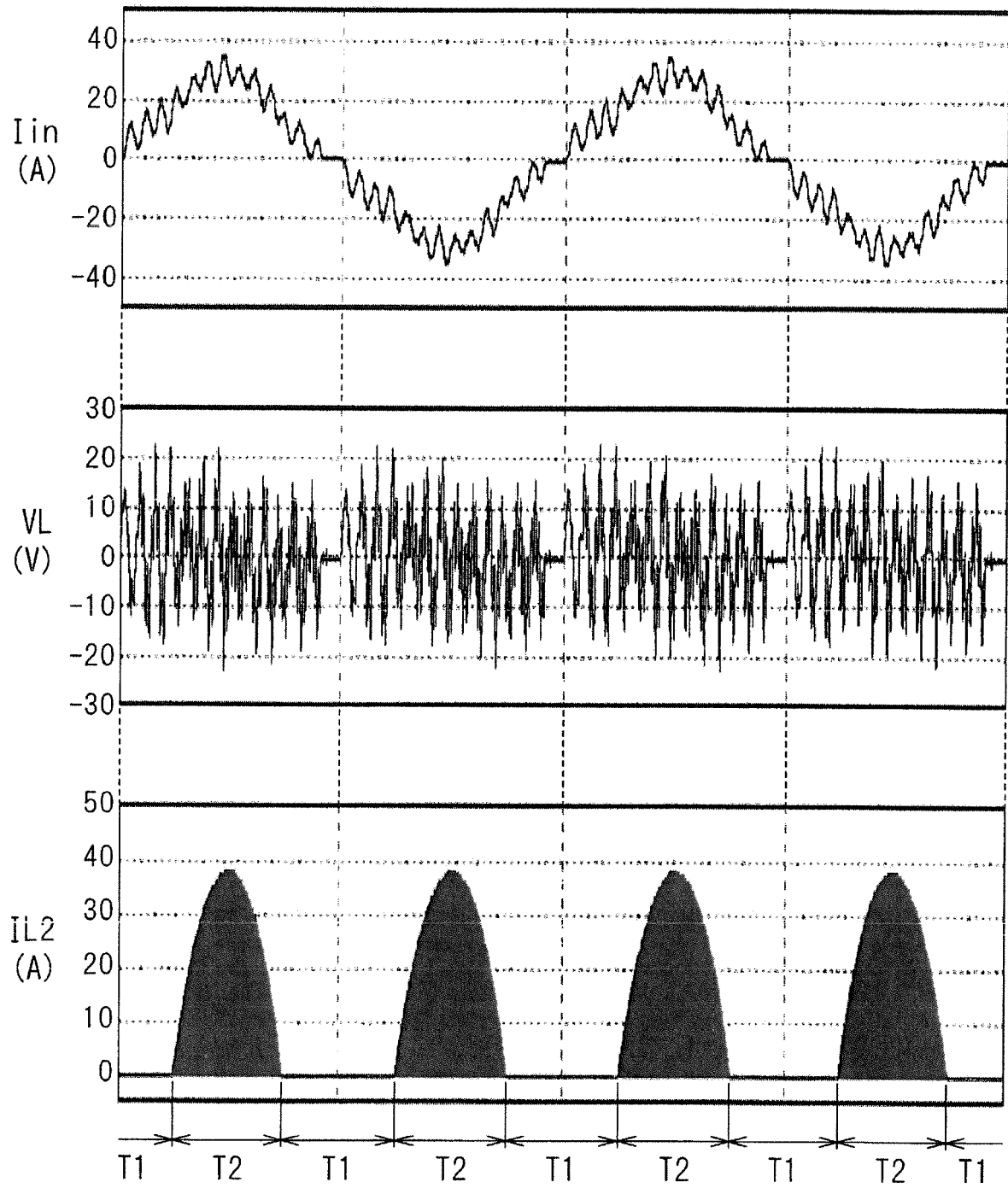
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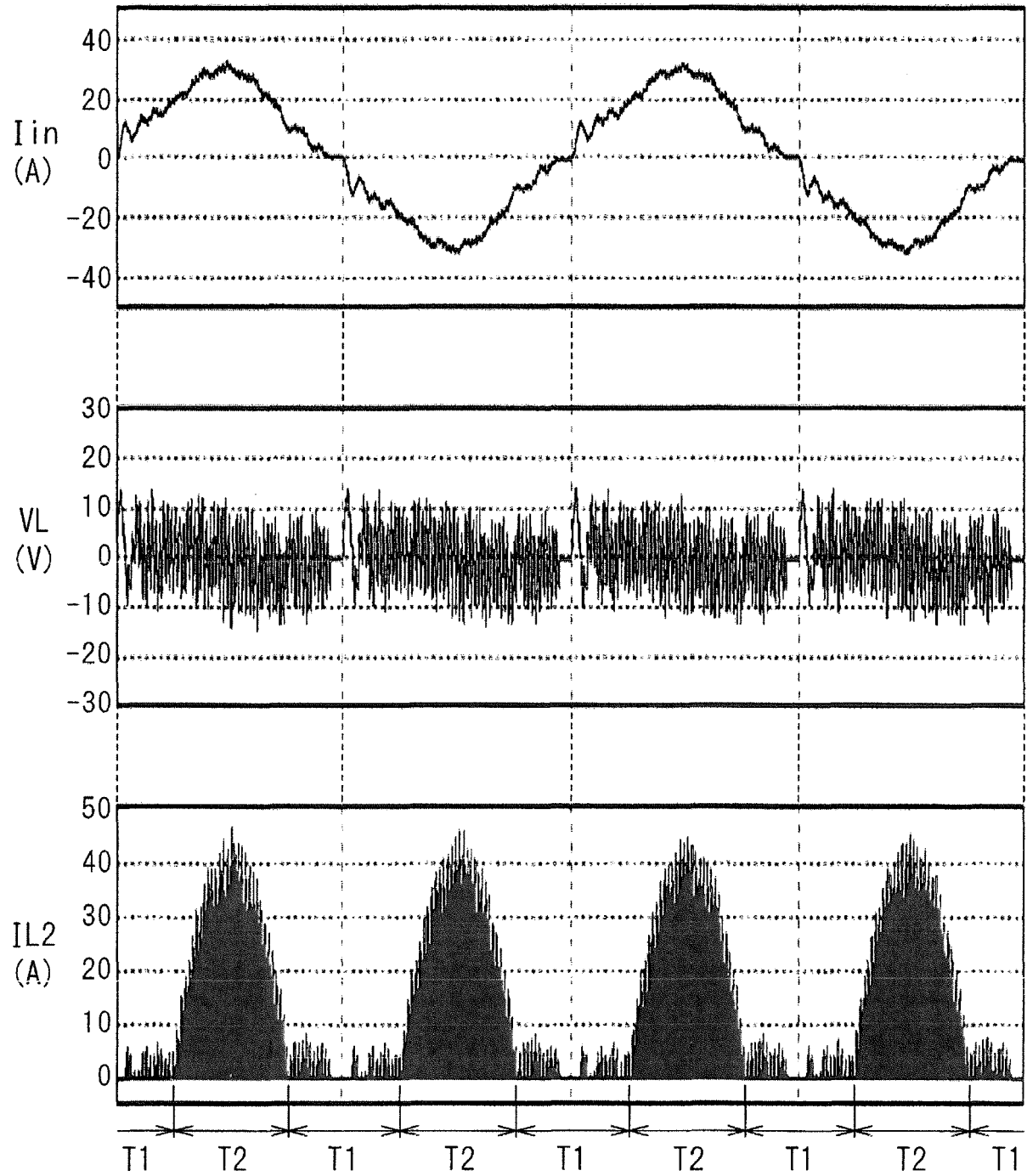
F I G . 7



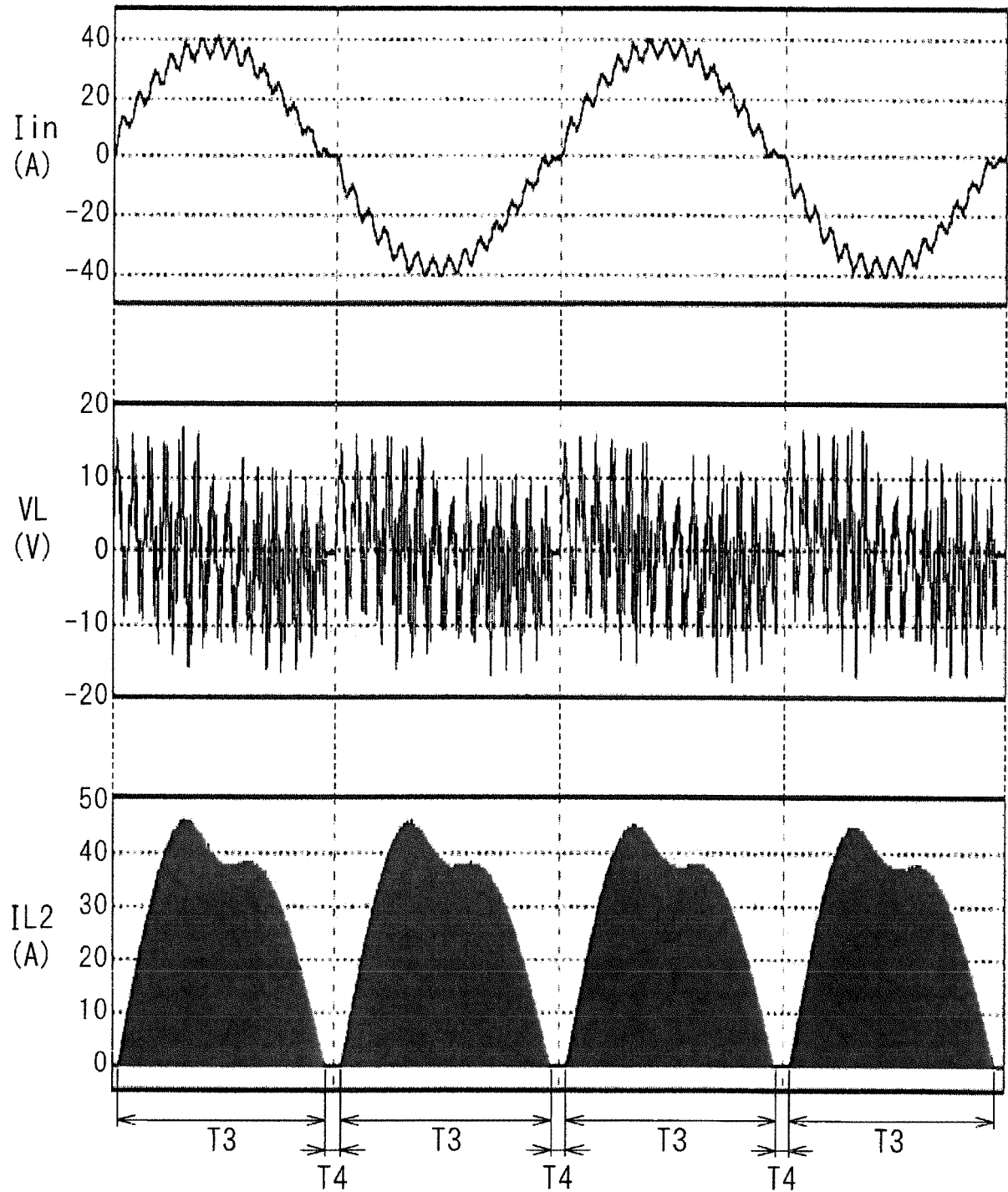
F I G . 8



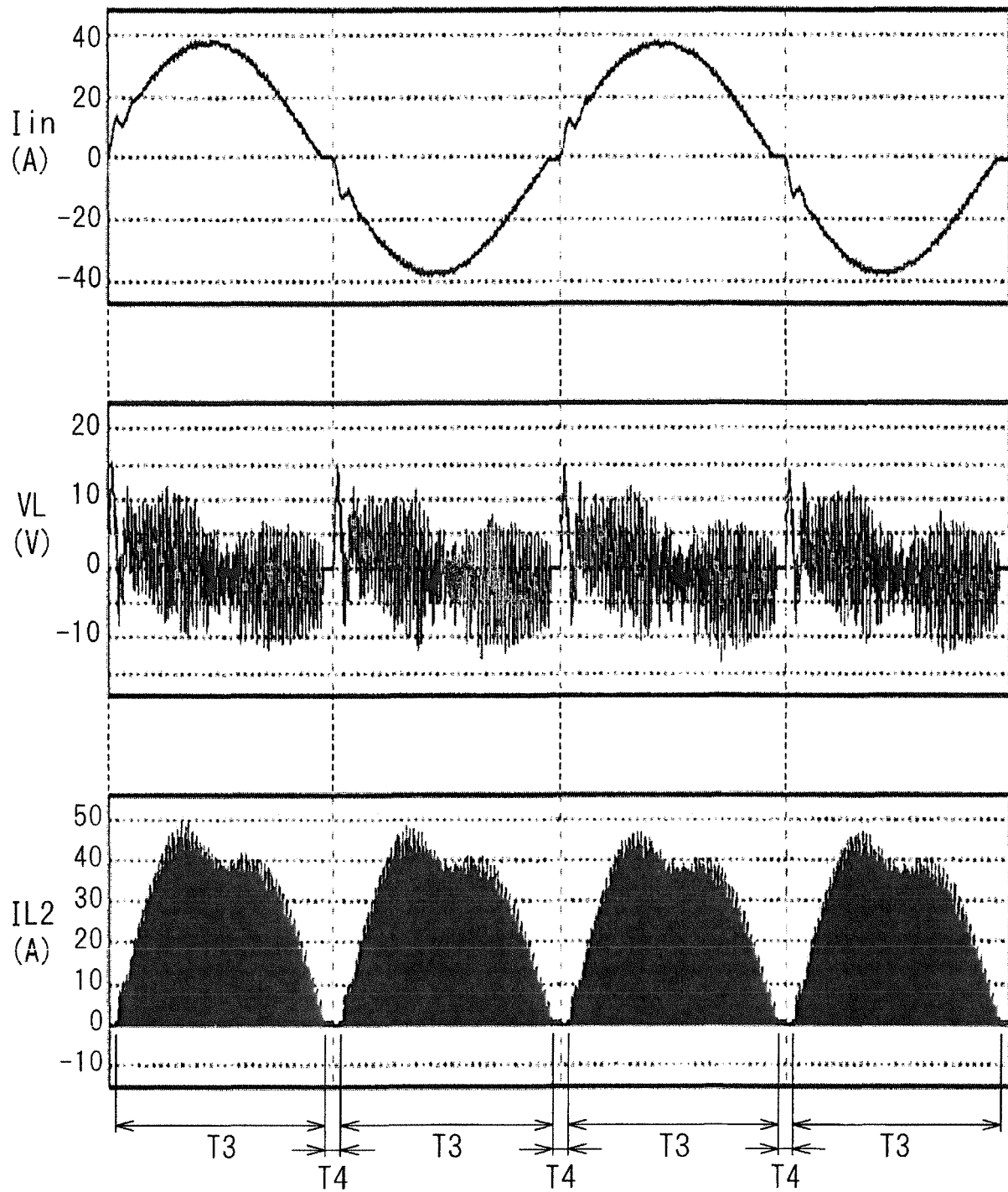
F I G . 9



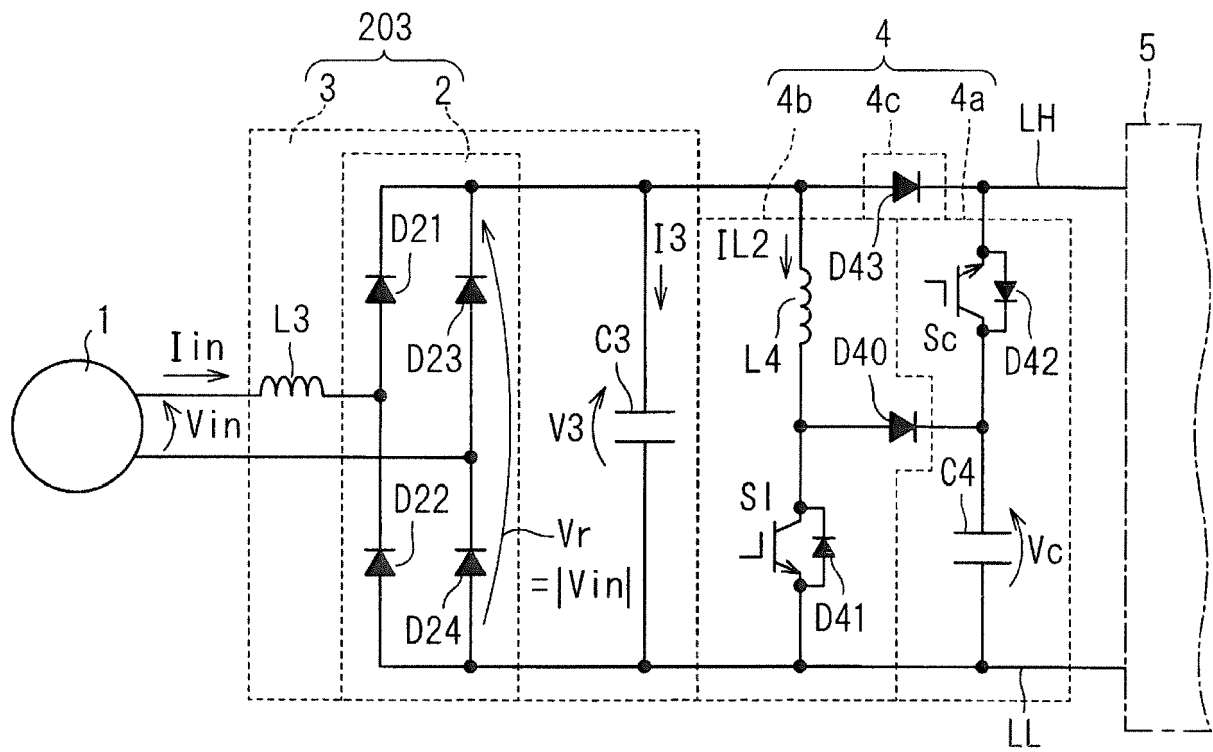
F I G . 1 0



F I G . 1 1



F I G . 1 2



F I G . 1 3

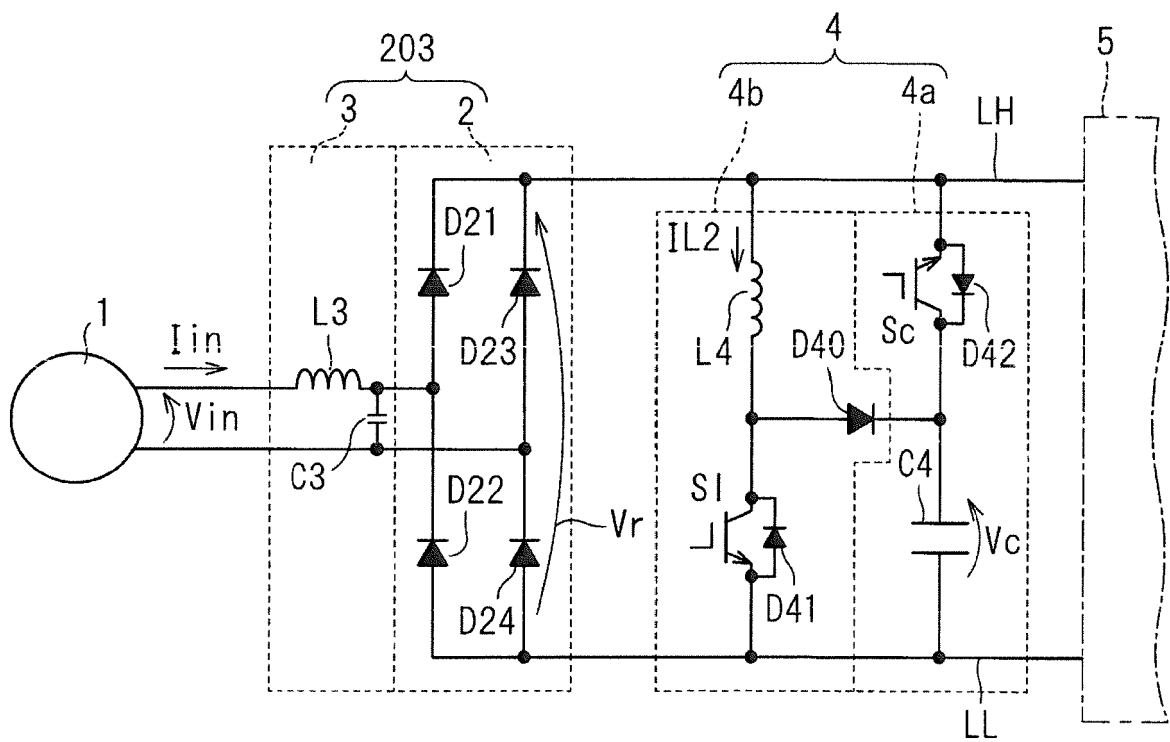


FIG. 14

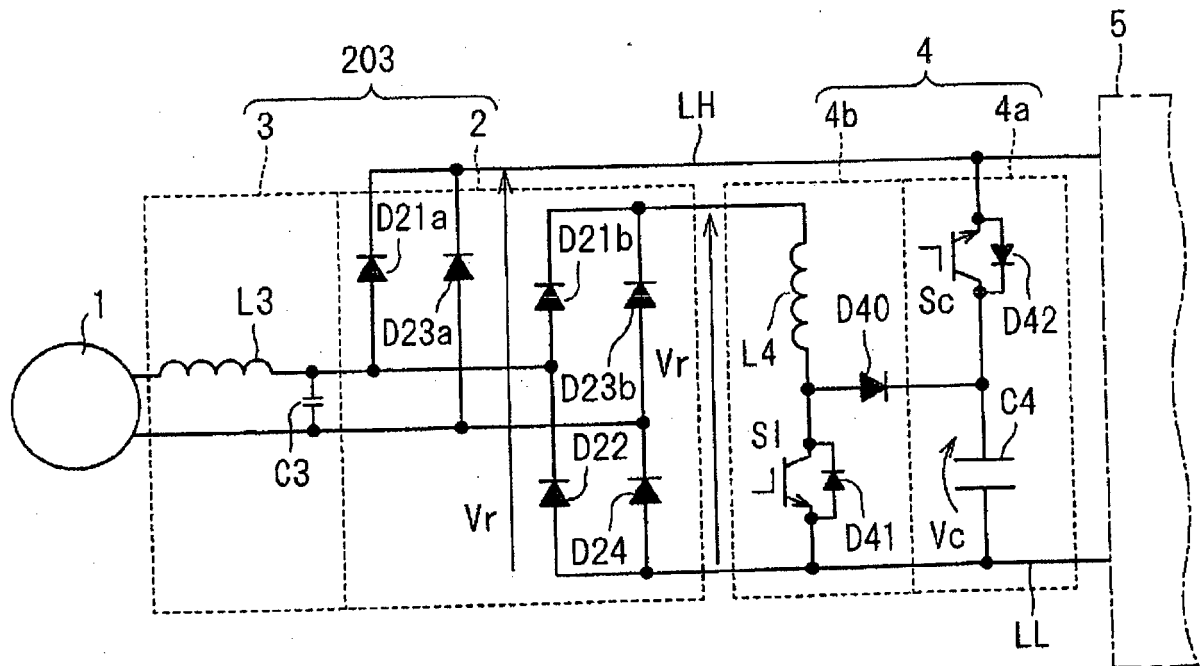
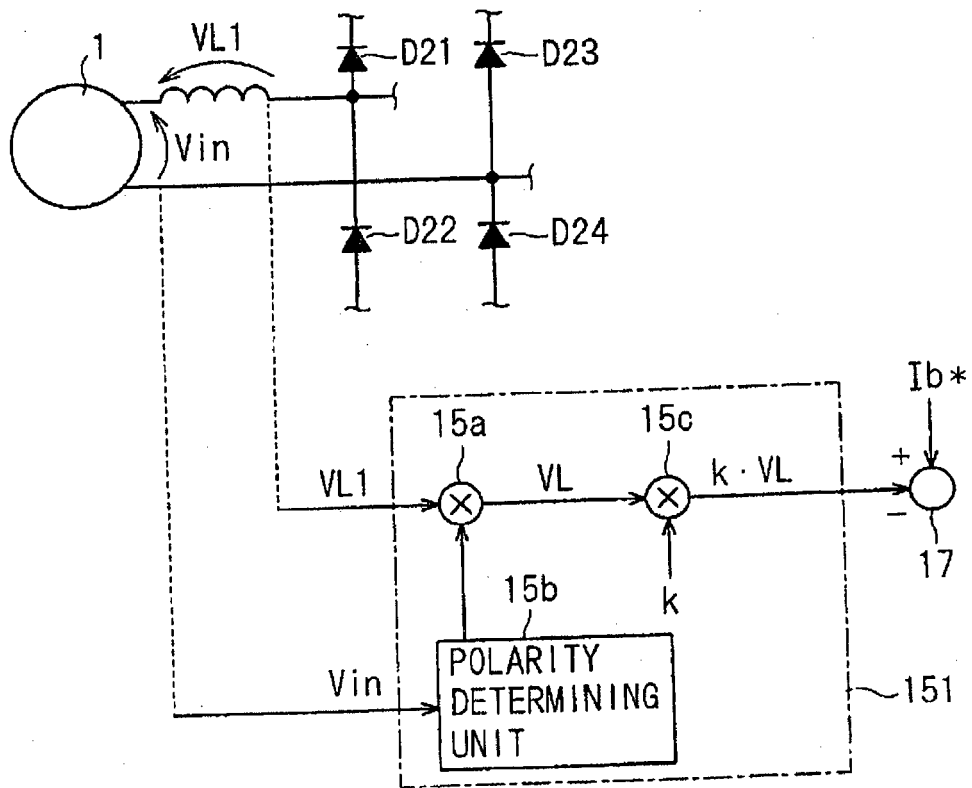


FIG. 15



REFERENCES CITED IN THE DESCRIPTION

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