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# (54) ARRAY SUBSTRATE AND METHOD FOR FABRICATION THEREOF AND DISPLAY DEVICE

(57) An array substrate, a manufacturing method thereof and a display device are disclosed. The array substrate comprises a gate electrode layer (2), an active layer (4) and a source-drain electrode layer (6) that are disposed on a substrate (1). The substrate comprises a storage capacitance region thereon II. In the storage capacitance region II, projections of the gate electrode layer (2) and the active layer (4) on the substrate (1) are at least partially overlapped, and projections of the active layer (4) and the source-drain electrode layer (6) on the substrate (1) are at least partially overlapped. The array substrate can effectively increase the storage capacitance without increasing an area occupied by the storage capacitance region, which is advantageously to reduce a pixel area and increase PPI.

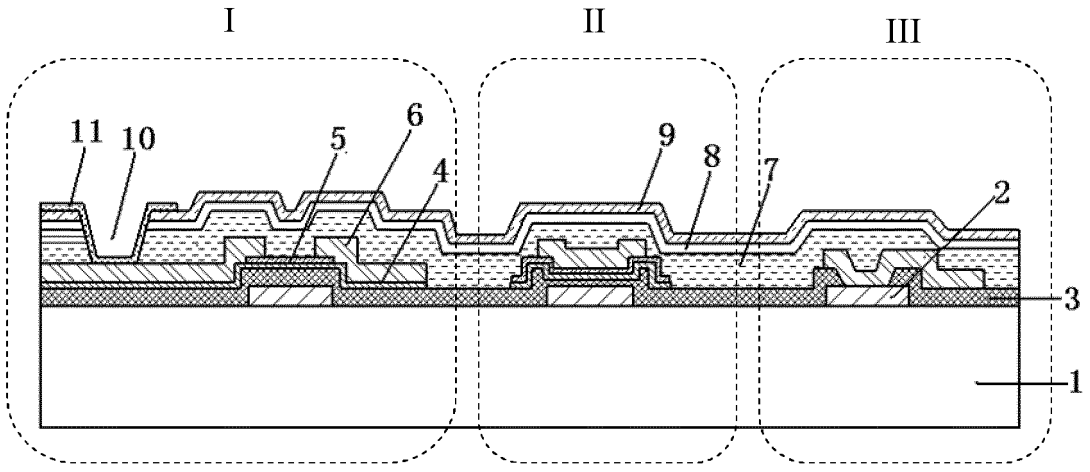


Fig. 8

EP 3 276 663 A1

## Description

### TECHNICAL FIELD

**[0001]** Embodiments of the present disclosure relate to an array substrate, a manufacturing method thereof and a display device.

### BACKGROUND

**[0002]** Recently, display technologies have been developed rapidly. For example, Thin film transistor (simply referred as TFT) technologies have been developed from amorphous silicon thin-film transistors in the past to low temperature Poly-Si thin film transistors, metal oxide semiconductor thin film transistors and so on currently, . Phosphor technologies have been developed from liquid crystal display (simply referred as LCD) technologies in the past to organic light emitting diode (simply referred as OLED) technologies currently.

**[0003]** Oxide semiconductors are highly regarded. Large-sized oxide panels are currently in a phase of mass production and backplane performance promotion. Mass produced oxide backplanes are substantially etch-stopper layer (simply referred as ESL) structures. Because a display screen is required to have a high definition all the time, it requires a pixel area to be reduced continuously and Pixels Per Inch (simply referred as PPI) to be increased. However, the pixel area being reduced continuously would lead to a problem of process complexity and reliability, and storage capacitance being continuously decreased.

### SUMMARY

**[0004]** An embodiment of the disclosure provides an array substrate, comprising a gate electrode layer, an active layer and a source-drain electrode layer that are disposed on a substrate, wherein: the substrate comprises a storage capacitance region thereon, in the storage capacitance region, projections of the gate electrode layer and the active layer on the substrate are at least partially overlapped, and projections of the active layer and the source-drain electrode layer on the substrate are at least partially overlapped.

**[0005]** For example, the array substrate further comprises a gate insulation layer between the gate electrode layer and the active layer and a etch-stopper layer between the active layer and the source-drain electrodes layer, wherein the gate electrode layer comprises a portion in the storage capacitance region, the gate insulation layer comprises a portion in the storage capacitance region; the active layer comprises a portion in the storage capacitance region; the etch-stopper layer comprises a portion in the storage capacitance region; the source-drain electrode layer comprises a portion in the storage capacitance region.

**[0006]** For example, the substrate further comprises a thin film transistor region, and a thickness of the gate insulation layer formed in the storage capacitance is smaller than a thickness of the gate insulation layer formed in the thin film transistor region.

**[0007]** For example, the gate insulation layer at a contact hole in the gate insulation layer is in contact with the source-drain electrode layer.

**[0008]** For example, at least one passivation layer is formed on the source-drain electrode layer, and a material of the passivation layer is one or more of silicon oxide, silicon nitride, silicon oxynitride, or alumina.

**[0009]** For example, a pixel electrode layer is formed on the passivation layer, and the pixel electrode layer is in contact with the source-drain electrode layer by a contact hole in the passivation layer which runs through the passivation layer.

**[0010]** An embodiment of the disclosure provides a method of manufacturing an array substrate, the method comprising: forming a gate electrode layer, an active layer and a source-drain electrode layer on a substrate, wherein the substrate comprises a storage capacitance region thereon; in the capacitance storage region, projections of the gate electrode layer and the active layer on the substrate are at least partially overlapped, and projections of the active layer and the source-drain electrode layer on the substrate are at least partially overlapped.

**[0011]** For example, a gate insulation layer is formed between the gate electrode layer and the active layer, and an etch-stopper layer is formed between the active layer and the source-drain electrode layer, wherein when the gate electrode layer is formed, a portion in the storage capacitance region is formed; when the gate insulation layer is formed, a portion in the storage capacitance region is formed; when the active layer is formed, a portion in the storage capacitance region is formed; when the etch-stopper layer is formed, a portion in the storage capacitance region is formed; and when the source-drain electrode layer is formed, a portion in the storage capacitance region is formed.

**[0012]** For example, the method further comprises etching the gate insulation layer in the storage capacitance region to be thinned, after the gate insulation layer is formed.

**[0013]** For example, a thickness of the gate insulation layer in the storage capacitance region is controlled by controlling an etching time when the gate insulation layer in the storage capacitance is etched to be thinned.

**[0014]** For example, the method further comprises etching the gate insulation layer at a contact hole predetermined to be formed in the gate insulation layer to thinned, while etching the gate insulation layer in the storage capacitance region to be thinned.

**[0015]** For example, the method further comprises etching the gate insulation layer at the contact hole predetermined to be formed in the gate insulation layer again so as to reach the gate electrode layer, while forming the etch-stopper layer on the active layer, and the gate insu-

lation layer at the contact hole in the gate insulation layer is in contact with the source-drain electrode layer.

**[0016]** For example, the method further comprises: at least one passivation layer being formed on the source-drain electrode layer, and a material of the passivation layer being one or more of silicon oxide, silicon nitride, silicon oxynitride, or alumina.

**[0017]** For example, the method further comprises: forming a contact hole in the at least one passivation layer which runs through the at least one passivation layer and forming a pixel electrode on the at least one passivation layer, and the pixel electrode is in contact with the source-drain electrode layer by the contact hole in the passivation layer.

**[0018]** For example, the pixel electrode layer is cured and annealed, after the pixel electrode layer is formed .

**[0019]** An embodiment of the disclosure provides a display device, comprising the above-mentioned array substrate.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** In order to clearly illustrate the technical solution of the embodiments of the disclosure, the drawings of the embodiments will be briefly described in the following; it is obvious that the described drawings are only related to some embodiments of the disclosure and thus are not limitative of the disclosure.

Figure 1 is a schematic diagram of forming a gate electrode layer of an array substrate provided by an embodiment of the disclosure;

Figure 2 is a schematic diagram of forming a gate insulation layer provided by the embodiment of the disclosure;

Figure 3 is a schematic diagram of forming an active layer provided by the embodiment of the disclosure;

Figure 4 is a schematic diagram of forming an etch-stopper layer provided by the embodiment of the disclosure;

Figure 5 is a schematic diagram of forming a source-drain electrode layer provided by the embodiment of the disclosure;

Figure 6 is a schematic diagram of forming a plurality of passivation layers provided by the embodiment of the disclosure;

Figure 7 is a schematic diagram of forming a contact hole provided by the embodiment of the disclosure;

Figure 8 is a schematic diagram of forming a pixel electrode layer provided by the embodiment of the disclosure; and

Figure 9 is a flow chart of a method of manufacturing the array substrate provided by the embodiment of the disclosure.

## DETAILED DESCRIPTION

**[0021]** In order to make objects, technical details and advantages of the embodiments of the disclosure apparent, the technical solutions of the embodiments will be described in a clearly and fully understandable way in connection with the drawings related to the embodiments of the disclosure. Apparently, the described embodiments are just a part but not all of the embodiments of the disclosure. Based on the described embodiments herein, those skilled in the art can obtain other embodiment(s), without any inventive work, which should be within the scope of the disclosure.

**[0022]** An embodiment of the present disclosure provides an array substrate. As shown in Figure 8, the array substrate comprises a gate electrode layer 2, an active layer 4 and a source-electrode layer 6 that are disposed on a substrate 1 sequentially.

**[0023]** The substrate 1 comprises a storage capacitance region II thereon.

**[0024]** In the storage region II, projections of the gate electrode layer 2 and the active layer 4 on the substrate 1 are at least partially overlapped. The projections of the active layer 4 and the source-drain electrode layer 6 on the substrate 1 are at least partially overlapped, so that the active layer 4, the gate electrode layer 2, the source-drain electrode layer 6 form a dual-capacitor structure on the storage capacitance region II.

**[0025]** In the embodiment, as shown in Figure 8, a gate insulation layer 8 is further comprised between the gate electrode layer 2 and the active layer 4, and an etch-stopper layer 5 is further comprised between the active layer 4 and the source-drain electrode layer 6. The gate electrode layer 2 comprises a portion in the storage capacitance region II, the gate insulation layer 3 comprises a portion in the storage capacitance region II, the active layer 4 comprises a portion in the storage capacitance region II, the etch-stopper layer 5 comprises a portion in the storage capacitance region II, and the source-drain electrode layer 6 comprises a portion in the storage capacitance region II. In this way, the storage capacitance region II forms a dual-capacitor structure (i.e., the gate electrode layer 2, the gate insulation layer 3 and the active layer 4 form a capacitor and the source-drain electrode layer 6, the etch-stopper layer 5 and the active layer 4 form another capacitor). Storage capacitance is effectively increased when an area occupied by the storage capacitance region II is not increased, which is advantageously to reduce a pixel area and increase PPI.

**[0026]** It should be noticed that the etch-stopper layer 5 can be an insulating layer in any forms.

**[0027]** In this embodiment, the gate insulation layer 3 in the storage capacitance region II is a thinned gate insulation layer. The thinned gate insulation layer can increase the storage capacitance effectively.

**[0028]** In this embodiment, the gate electrode layer 2 at the contact hole 12 in the gate insulation layer 6 is in contact with the source-drain electrode layer 6. The gate electrode layer 2 at the contact hole in the gate insulation layer is in contact with the source-drain electrode layer 6 directly by etching the gate insulation layer 3 at the

contact hole in the gate insulation layer, so as to achieve a hole contact between the source-drain electrode layer 6 and the gate electrode layer 2.

**[0029]** Further, at least one passivation layer is formed on the source-drain electrode layer 6. As shown in Figure 8, a first passivation layer 7, a second passivation layer 8 and a third passivation layer 9 are formed on the source-drain electrode layer 6 sequentially. A material of the passivation layers can be one or more of silicon oxide ($SiO_x$), silicon nitride ($SiN_x$), silicon oxynitride (SiON) or alumina ($Al_2O_3$).

**[0030]** Further, a pixel electrode layer 11 is formed on the passivation layer. The pixel electrode layer 11 is in contact with the source-drain electrode layer 6 by a contact hole 10 in the passivation layers which runs through the passivation layers. A material of the pixel electrode layer 11 is indium tin oxides (ITO) with good conductivity and transparency.

**[0031]** Another embodiment of the disclosure provides a method of manufacturing an array substrate. The method comprises: forming a gate electrode layer 2, an active layer 4 and a source-drain electrode layer 6 on the substrate; the substrate comprises a storage capacitance region thereon.

**[0032]** In the storage region II, projections of the gate electrode layer 2 and the active layer 4 on the substrate 1 are at least partially overlapped, and the projections of the active layer 4 and the source-drain electrode layer 6 on the substrate 1 are at least partially overlapped, so that the active layer 4, the gate electrode layer 2, the source-drain electrode layer 6 form a dual-capacitor structure on the storage capacitance region II.

**[0033]** In this embodiment, the method further comprises forming a gate insulation layer 3 between the gate electrode layer 2 and the active layer 4, and forming an etch-stopper layer 5 between the active layer 4 and the source-drain electrodes layer 6.

**[0034]** When the gate electrode layer 2 is formed, a portion in the storage capacitance region II is formed; When the gate insulation layer 3 is formed, a portion in the storage capacitance region II is formed; when the active layer 4 is formed, a portion in the storage capacitance region II is formed; when the etch-stopper layer 5 is formed, a portion in the storage capacitance region II is formed; and when the source-drain electrodes layer 6 is formed, a portion in the storage capacitance region II is formed . It should be understood that these portions are also comprised in the storage capacitance region II by designing mask patterns for etching.

**[0035]** It is noticed that other forms of the insulation layer rather than the etch-stopper layer 5 can be formed between the active layer 4 and the source-drain electrodes layer 6 according the type of a device.

**[0036]** As is shown, the disclosure comprises forming the dual-capacitor structure in the storage capacitance region II, so that the storage capacitance is effectively increased when an area occupied by the storage capacitance region II is not increased. It is advantageously to reduce a pixel area and increase PPI. At the same time, a new process does not need to be added because of using the active layer 4 and the etch-stopper layer 5 simultaneously.

**[0037]** In this embodiment, the method further comprises a step of: etching the gate insulation layer 3 in the storage capacitance region II to be thinned.

**[0038]** For example, the gate insulation layer 3 in the storage capacitance region II is etched by an etch mask for the insulation layer, and a thickness of the gate insulation layer 3 in the storage capacitance region II is controlled by controlling an etching time. In this way, the thickness of the insulation layer 3 of the storage capacitance region II is thinned, to increase the storage capacitance and improve the flatness of the storage capacitance region II, which is advantageously to improve performance of a back plate.

**[0039]** Further, while the gate insulation layer 3 of the storage capacitance region II is etched to be thinned, the gate insulation layer 3 at the contact hole to be formed predeterminedly in the gate insulation layer is etched to be thinned. For example, the storage capacitance region II and the gate insulation layer 3 at the contact hole in the gate insulation layer are etched by the etch mask for the insulation layer simultaneously. Because both of them are etched simultaneously, only one mask is needed.

**[0040]** In this embodiment, the method further comprises a step of: forming the etch-stopper layer 5 on the active layer, while etching the gate insulation layer 3 at the contact hole predetermined to be formed in the gate insulation layer again, to reach the gate electrode layer 2. As it can be seen, the insulation layer 3 at the contact hole in the gate insulation layer is formed by two steps. A first step etches the insulation layer 3 at the contact hole in the gate insulation layer while etching the insulation layer in the storage capacitance region II by the etch mask for the insulation layer, so as to thin the thickness of the insulation layer, and a second step etches the insulation layer 3 at the contact hole in the gate insulation layer again to reach the gate electrode layer 2 while forming the etch-stopper layer 5 on the active layer 4.

**[0041]** In this embodiment, the method further comprises: forming at least one passivation layer on the source-drain electrode layer 6.

**[0042]** For example, forming the passivation layer comprises steps of: forming a plurality of passivation layers sequentially by manufacturing methods, such as thermal growth, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, plasma chemical vapor deposition, or sputtering, and a material of the passivation layers is one or more of silicon oxide ($SiO_x$), silicon nitride ($SiN_x$), silicon oxynitride (SiON) or alumina ($Al_2O_3$).

**[0043]** In this embodiment, the method further comprises: forming a contact hole in the at least one passivation layer, the contact hole running through the at least one passivation layer, and forming a pixel electrode layer

11 on the at least one passivation layer. The passivation layer is in contact with the source-drain electrode layer 6 by the contact hole in the passivation layer.

**[0044]** In this embodiment, after forming the pixel electrode layer 11, the method further comprises: curing and annealing the pixel electrode layer 11. For example, the pixel electrode layer 11 is annealed in vacuum, nitrogen, atmosphere or oxygen environment. An annealing temperature is between 120°C and 450°C. An annealing time lasts 0.5 to 3 hours.

**[0045]** The display device provided by another embodiment of the disclosure comprises above-mentioned array substrate. The display device may be a TV set, a display panel, a tablet computer, a cell phone, a navigator, a camera, or a video camera or any product having a display function.

First embodiment

**[0046]** In order to make technique solutions of the at least one embodiment of the disclosure more clearly, the at least one embodiment will be described in a clearly and fully understandable way in connection with a cross-section schematic view of a structure of a device formed by various steps. In this embodiment, in a final product structure as shown Figure 8, an array substrate comprises a thin film transistor region I, a storage capacitance region II and a source-drain contact hole region III, i.e. three regions corresponding to three gate electrode layers 2 from left to right in Figure 8. Of course, the array substrate can comprise other structures, and description of which will be omitted herein. It should be understood that the structures shown herein are only exemplary, and other structures can be adopted according to a scope and spirit defined in claims of the disclosure. As shown in Figure 9, a manufacturing method of the embodiment can comprises steps of:

S1: a metal layer on the substrate 1 is formed, and the metal layer is etched to form the gate electrode layer 2, as shown in Figure 1.

**[0047]** For example, the substrate 1 can be a material of glass, plastics, silicon and the like. The metal layer is formed by sputtering metal or alloy, such as molybdenum (Mo), aluminum /neodymium(Al/Nd), aluminum/neodymium/molybdenum (Al/Nd/Mo), molybdenum/aluminum/neodymium/molybdenum (Mo/Al/Nd/Mo), gold/titanium(Au/Ti), platinum/titanium(Pt/Ti) and the like, and the metal layer is lithographed, to form the g ate electrode layer 2.

**[0048]** S2: the gate insulation layer 3 is formed, and the storage capacitance region II and the gate insulation layer at the contact hole 12 in the gate insulation layer are etched by a etch mask for the insulation layer, as shown in Figure 2.

**[0049]** For example, oxides, such as silicon oxide ($SiO_X$), silicon nitride ($SiN_X$), silicon oxynitride (SiON), alumina ($Al_2O_3$), hafnium oxide ($HfO_2$), zirconium oxide ($ZrO_2$), titanium oxide($TiO_2$), Yttrium oxide ($Y_2O_3$), lanthanum oxide ($La_2O_3$), tantalum oxide ($Ta_2O_5$) or the like are deposited by manufacturing methods, such as atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, plasma chemical vapor deposition, or sputtering, so as to form one or more gate insulation layers, and the storage capacitance region II and the gate insulation layer at the contact hole 12 in the gate insulation layer are etched simultaneously by the etching mask for the insulation layer.

**[0050]** S3: a first oxide layer is formed, and the oxide layer is etched to form an active layer 4, as shown in Figure 3;

**[0051]** For example, oxides, such as indium gallium zinc oxide (IGZO), nitride zinc oxide (ZnON), indium tin zinc oxide (ITZO), zinc tin oxide (ZTO), zinc indium oxide (ZIO), indium gallium oxide (IGO), aluminum zinc tin oxide (AZTO) or the like are deposited by manufacturing methods, such as sputtering, sol-gel, vacuum evaporation, spraying, ink-jet printing to form the first oxide layer, and the first oxide layer is etched to form an active layer 4.

**[0052]** S4: a second oxide layer is formed, the second oxide layer is etched to form an etch-stopper layer 5, and the gate insulation layer 3 at the contact hole 12 in the gate insulation layer 3 is etched again at the same time to reach the gate electrode layer 2, as shown in Figure 4.

**[0053]** For example, oxides, such as silicon oxide ($SiO_x$), silicon nitride ($SiN_x$), silicon oxynitride (SiON), alumina ($Al_2O_3$), tetraethyl orthosilicate (TEOS) or the like is deposited by manufacturing methods, such as atomic layer deposition, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, plasma chemical vapor deposition, sputtering, sol-gel or the like, so as to form one or more second oxide layer, and the second oxide layer is etched to form an etch-stopper layer 5 and at the same time, the gate insulation layer 3 at the contact hole 12 in the gate insulation layer is etched to reach the gate electrode layer 2.

**[0054]** S5: a metal layer is formed, and the metal layer is etched to form a source-drain electrode layer 6, as shown in Figure 5.

**[0055]** For example, metal or alloy, such as molybdenum (Mo), aluminum/neodymium (Al/Nd), aluminum/neodymium/molybdenum (Al/Nd/Mo), molybdenum/aluminum/ neodymium/molybdenum (Mo/Al/Nd/Mo), gold/titanium(Au/Ti), platinum/titanium(Pt/Ti) and the like is deposited by sputtering to form the metal layer, and the metal layer is lithographed, to form the gate electrode layer 2.

**[0056]** S6:a first passivation layer 7, a second passivation layer 8 and a third passivation layer 9 are formed sequentially, as shown in Figure 6.

**[0057]** For example, the passivation layers are continuously grown by manufacturing method, such as thermal growth, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, plasma chemical vapor deposition, sputtering or the like, and a

material of the passivation layers is one or more of silicon oxide $SiO_x$, silicon nitride $SiN_x$, silicon oxynitride SiON, or alumina $Al_2O_3$.

**[0058]** S7: the first passivation layer 7, the second passivation layer 8 and the third passivation layer 8 are etched, to form a contact hole 10 in passivation layers, as shown in Figure 7.

**[0059]** S8: an ITO metal electrode layer is formed by sputtering, and the ITO metal electrode is etched to form a pixel electrode layer 11, as shown in Figure 8.

**[0060]** For example, the pixel electrode 11 is in contact with the source-drain electrode layer 6 by the contact hole in the passivation layers.

**[0061]** S9: the pixel electrode layer 11 is cured and annealed.

**[0062]** For example, the pixel electrode layer 11 is annealed in vacuum, nitrogen, atmosphere, oxygen environment. An annealing temperature is between 120°C and 450°C. An annealing time lasts 0.5 to 3 hours.

**[0063]** The above descriptions are merely exemplary embodiments of the disclosure, and do not restrict the scope of the disclosure. The scope of the disclosure should be defined by accompanying claims.

**[0064]** This application claims the priority of Chinese Patent Application No. 201510132293.3 filed on March 25, 2015, which is hereby incorporated entirely herein by reference.

## Claims

1. An array substrate, comprising a gate electrode layer, an active layer and a source-drain electrode layer that are disposed on a substrate, wherein
the substrate comprises a storage capacitance region thereon, in the storage capacitance region, projections of the gate electrode layer and the active layer on the substrate are at least partially overlapped, and projections of the active layer and the source-drain electrode layer on the substrate are at least partially overlapped.

2. The array substrate of claim 1, further comprising a gate insulation layer between the gate electrode layer and the active layer and an etch-stopper layer between the active layer and the source-drain electrodes layer, wherein
the gate electrode layer comprises a portion in the storage capacitance region;
the gate insulation layer comprises a portion in the storage capacitance region;
the active layer comprises a portion in the storage capacitance region;
the etch-stopper layer comprises a portion in the storage capacitance region; and
the source-drain electrode layer comprises a portion in the storage capacitance region.

3. The array substrate of claims 1 or 2, wherein the substrate further comprises a thin film transistor region, and a thickness of the gate insulation layer formed in the storage capacitance is smaller than a thickness of the gate insulation layer formed in the thin film transistor region.

4. The array substrate of any one of claims 1-3, wherein the gate insulation layer at a contact hole in the gate insulation layer is in contact with the source-drain electrode layer.

5. The array substrate of any one of claims 1-4, wherein at least one passivation layer is formed on the source-drain electrode layer, and a material of the passivation layer is one or more of silicon oxide, silicon nitride, silicon oxynitride, or alumina.

6. The array substrate of claim 5, wherein a pixel electrode layer is formed on the passivation layer, and the pixel electrode layer is in contact with the source-drain electrode layer by a contact hole in the passivation layer which runs through the passivation layer.

7. A method of manufacturing an array substrate, comprising: forming a gate electrode layer, an active layer and a source-drain electrode layer on a substrate, wherein
the substrate comprises a storage capacitance region thereon, in the capacitance storage region, projections of the gate electrode layer and the active layer on the substrate are at least partially overlapped, and projections of the active layer and the source-drain electrode layer on the substrate are at least partially overlapped.

8. The method of claim 7, further comprising: forming a gate insulation layer between the gate electrode layer and the active layer, and forming an etch-stopper layer between the active layer and the source-drain electrode layer, wherein
upon the gate electrode layer being formed, a portion in the storage capacitance region is formed,
upon the gate insulation layer being formed, a portion in the storage capacitance region is formed,
upon the active layer being formed, a portion in the storage capacitance region is formed,
upon the etch-stopper layer being formed, a portion in the storage capacitance region is formed, and
upon the source-drain electrode layer being formed, a portion in the storage capacitance region is formed.

9. The array substrate of claim 8, further comprising etching the gate insulation layer in the storage capacitance region to be thinned, after the gate insulation layer is formed.

10. The array substrate of claim 9, wherein a thickness

of the gate insulation layer in the storage capacitance region is controlled by controlling an etching time when the gate insulation layer in the storage capacitance region is etched to be thinned.

**11.** The method of claim 9, further comprising etching the gate insulation layer at a contact hole predetermined to be formed in the gate insulation layer to be thinned, while etching the gate insulation layer in the storage capacitance region to be thinned.

**12.** The method of claim 11, further comprising: etching the gate insulation layer at the contact hole predetermined to be formed in the gate insulation layer again to reach the gate electrode layer, while forming the etch-stopper layer on the active layer,
wherein the gate insulation layer at the contact hole in the gate insulation layer is in contact with the source-drain electrode layer.

**13.** The method of any one of claims 7-12, wherein at least one passivation layer is formed on the source-drain electrode layer, and a material of the passivation layer is one or more of silicon oxide, silicon nitride, silicon oxynitride, or alumina.

**14.** The method of claim 13, further comprising:

forming a contact hole in the at least one passivation layer which runs through the at least one passivation layer, and
forming a pixel electrode on the at least one passivation layer, wherein the pixel electrode is in contact with the source-drain electrode layer by the contact hole in the passivation layer.

**15.** The method of claim 14, wherein the pixel electrode layer is cured and annealed, after the pixel electrode layer is formed.

**16.** A display device, comprising the array substrate of any one of claims 1-6.

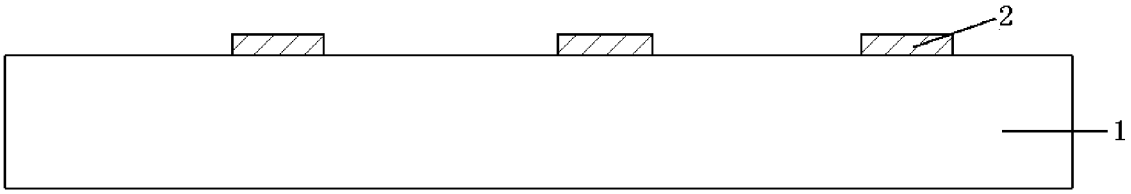


Fig. 1

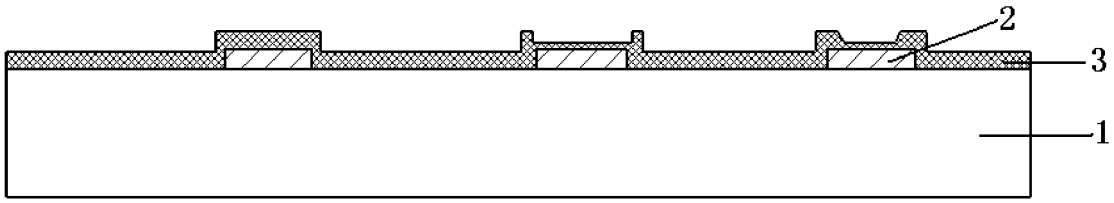


Fig. 2

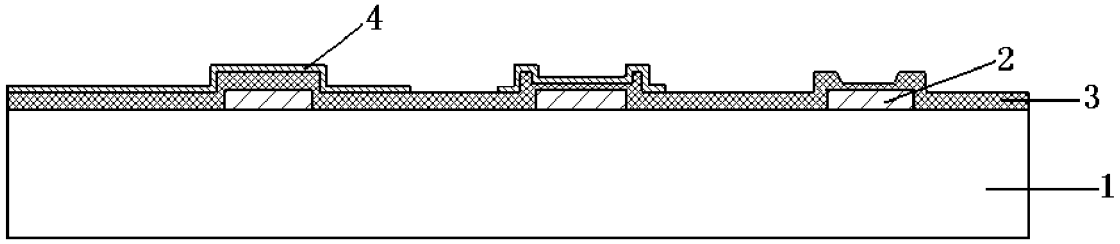


Fig. 3

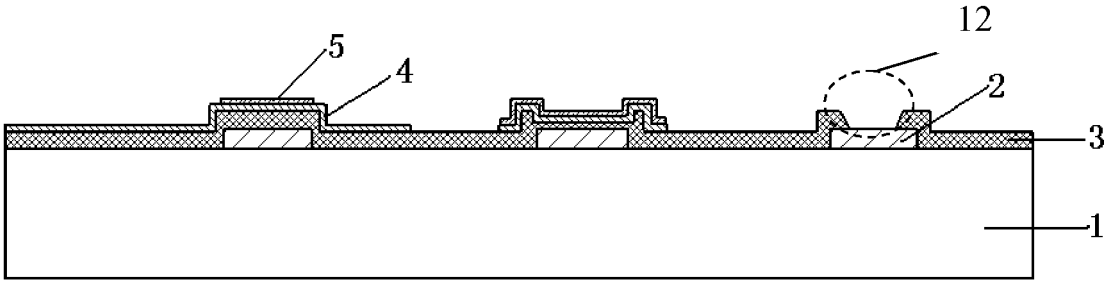


Fig. 4

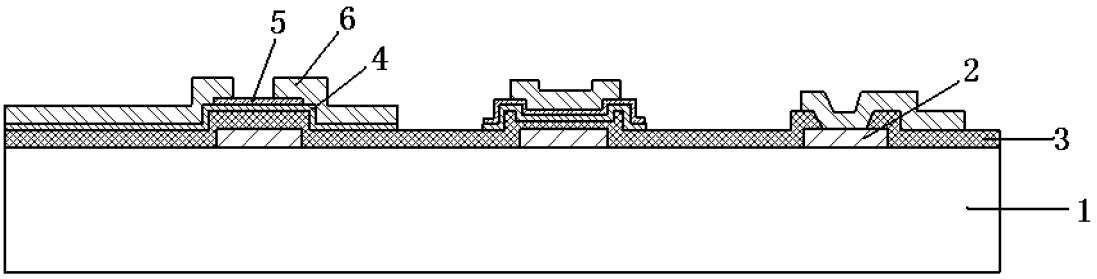


Fig. 5

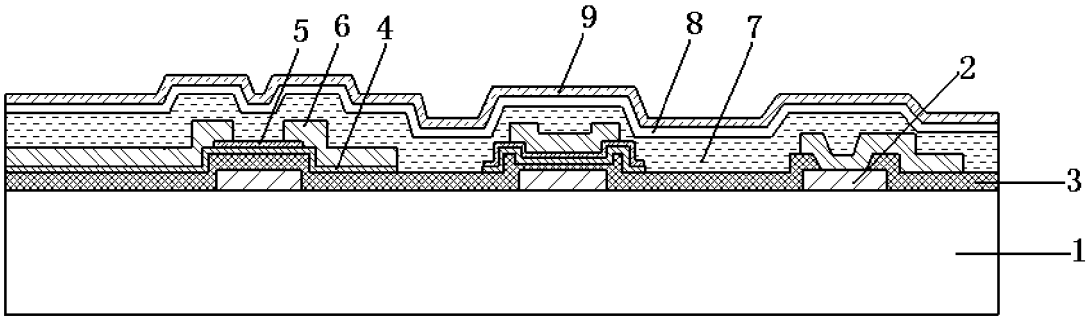


Fig. 6

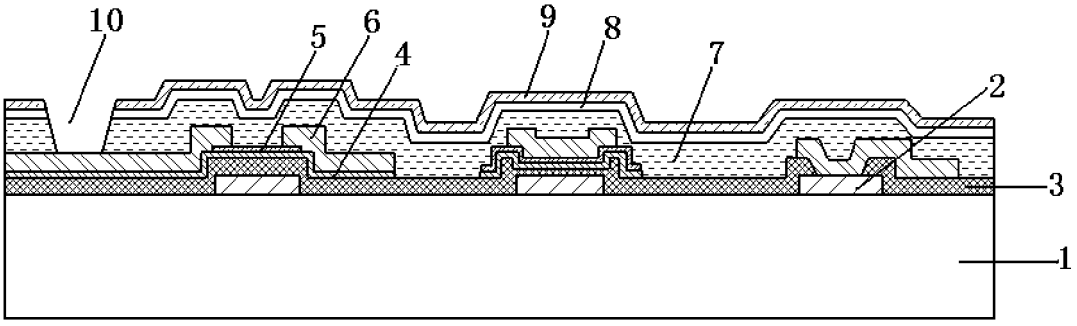


Fig. 7

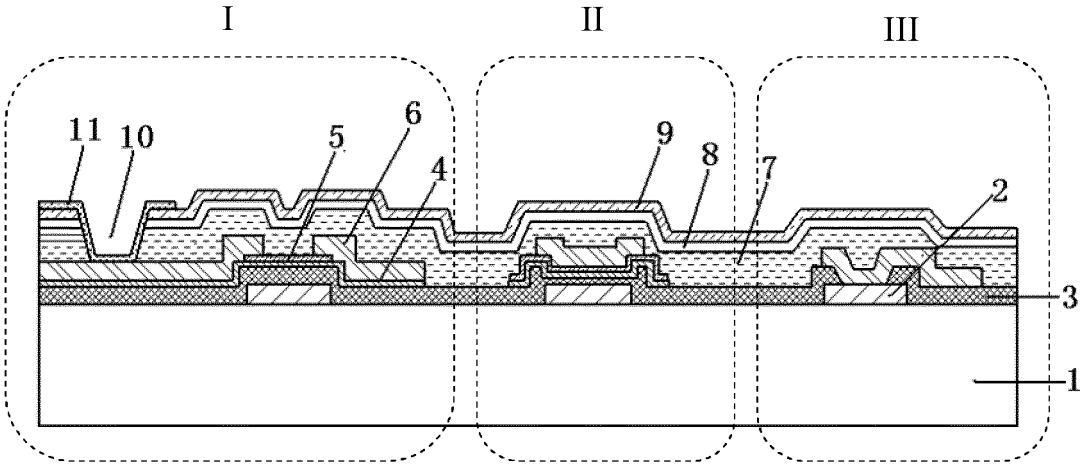


Fig. 8

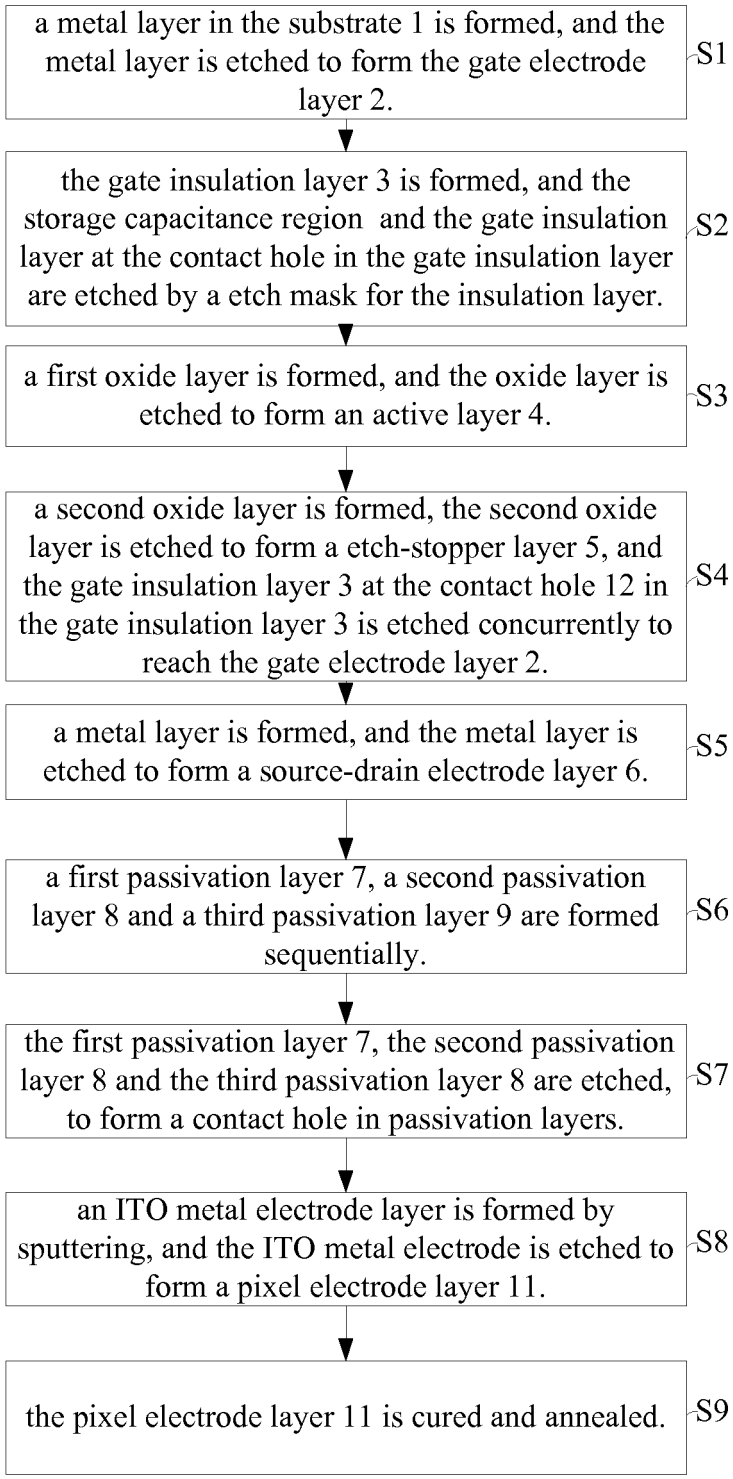
a metal layer in the substrate 1 is formed, and the metal layer is etched to form the gate electrode layer 2.
S1
the gate insulation layer 3 is formed, and the storage capacitance region and the gate insulation layer at the contact hole in the gate insulation layer are etched by a etch mask for the insulation layer.
S2
a first oxide layer is formed, and the oxide layer is etched to form an active layer 4.
S3
a second oxide layer is formed, the second oxide layer is etched to form a etch-stopper layer 5, and the gate insulation layer 3 at the contact hole 12 in the gate insulation layer 3 is etched concurrently to reach the gate electrode layer 2.
S4
a metal layer is formed, and the metal layer is etched to form a source-drain electrode layer 6.
S5
a first passivation layer 7, a second passivation layer 8 and a third passivation layer 9 are formed sequentially.
S6
the first passivation layer 7, the second passivation layer 8 and the third passivation layer 8 are etched, to form a contact hole in passivation layers.
S7
an ITO metal electrode layer is formed by sputtering, and the ITO metal electrode is etched to form a pixel electrode layer 11.
S8
the pixel electrode layer 11 is cured and annealed.
S9

Fig.9

# INTERNATIONAL SEARCH REPORT

International application No.
**PCT/CN2015/089997**

**A. CLASSIFICATION OF SUBJECT MATTER**

H01L 27/12 (2006.01) i; H01L 21/77 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI: semiconductor layer; metal level; barrier layer; gate; source; drain; activ???; insulat+; electrode?; capacit+; substrate; layer

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| PX | CN 104701328 A (BOE TECHNOLOGY GROUP CO., LTD.), 10 June 2015 (10.06.2015), description, paragraphs 0050-0094, and figures 8-9 | 1-16 |
| X | CN 102945828 A (GUANGZHOU NEW VISION OPTO-ELECTRONIC TECHNOLOGY CO., LTD.), 27 February 2013 (27.02.2013), description, paragraphs 0056-0066, and figures 1-6 | 1-2, 4-8, 13-16 |
| Y | CN 102945828 A (GUANGZHOU NEW VISION OPTO-ELECTRONIC TECHNOLOGY CO., LTD.), 27 February 2013 (27.02.2013), description, paragraphs 0056-0066, and figures 1-6 | 3, 9-12 |
| Y | CN 103928470 A (SHANGHAI TIANMA MICRO-ELECTRONICS CO., LTD. et al.), 16 July 2014 (16.07.2014), description, paragraphs 0031-0032, and figure 3 | 3, 9-12 |
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| A | CN 102768992 A (GUANGZHOU NEW VISION OPTO-ELECTRONIC TECHNOLOGY CO., LTD.), 07 November 2012 (07.11.2012), the whole document | 1-16 |

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 01 December 2015 (01.12.2015) | **14 December 2015 (14.12.2015)** |
| Name and mailing address of the ISA/CN:<br>State Intellectual Property Office of the P. R. China<br>No. 6, Xitucheng Road, Jimenqiao<br>Haidian District, Beijing 100088, China<br>Facsimile No.: (86-10) 62019451 | Authorized officer<br>**ZHANG, Miao**<br>Telephone No.: (86-10) **62414429** |

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# INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
**PCT/CN2015/089997**

| Patent Documents referred in the Report | Publication Date | Patent Family | Publication Date |
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| CN 102945828 A | 27 February 2013 | None | |
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## REFERENCES CITED IN THE DESCRIPTION

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