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(54) INTEGRATED CIRCUIT DIE AND MANUFACTURING METHOD THEREFOR

(57) Embodiments of the present invention provide an IC die and a preparation method thereof, so as to resolve a problem that a currently used heat dissipation method of an IC chip has a limited effect in an aspect of reducing a temperature of a heat point on a surface of the IC chip. The IC die includes an underlay; an active component; an interconnection layer, covering the active component, where the interconnection layer includes multiple metal layers and multiple dielectric layers, the multiple metal layers and the multiple dielectric layers are alternately arranged, a metal layer whose distance to the active component is the farthest in the multiple metal layers includes metal cabling and a metal welding pad; and a heat dissipation layer, where the heat dissipation layer covers a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer is located under a package layer, the package layer includes a plastic packaging material, and the heat dissipation layer includes an electrical-insulating material whose heat conductivity is greater than a preset value.

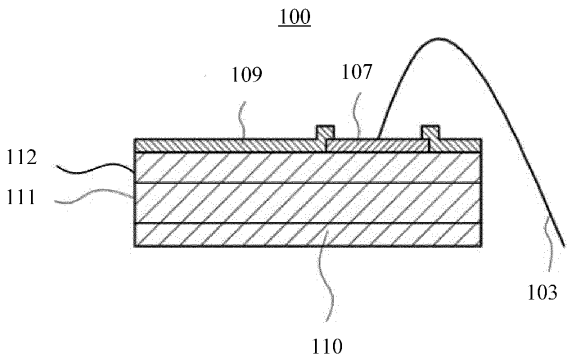

FIG. 4a

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Description

[0001] This application claims priority to Chinese Patent Application No. 201510221081.2, filed with the Chinese Patent Office on April 30, 2015 and entitled "INTEGRATED CIRCUIT DIE AND PREPARATION METHOD THEREOF", which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates to the field of integrated circuits, and in particular, to an integrated circuit die and a preparation method thereof.

BACKGROUND

[0003] As an integration level of an integrated circuit (IC, Integrated Circuit) chip is increasingly high, power density of the chip is higher. In addition, the power density is also unevenly distributed across the entire IC chip. In a region whose power density is relatively high, a large amount of heat is generated within a range with an extremely small area, and consequently, a heat point with an extremely high temperature is formed on a surface of the chip. Temperatures of these "heat points" are much higher than an average temperature of the entire IC chip. If heat in heat-point regions cannot be rapidly spread because effective heat management and an effective heat dissipation design are not performed on the IC chip, temperatures in the heat-point regions of the chip easily become excessively high, and consequently, the chip cannot normally work.

[0004] Currently, a heat dissipation design of an IC chip is mainly adding a heat sink on an IC chip package. FIG. 1 shows a die-up plastic ball grid array package body 10 on which a heat sink 12 is integrated. In the package body 10, an IC die 11 is mounted on a underlay 15 by using a die bonding material 13, and is connected to a leading wire 17. The package body 10 can be connected to a printed circuit board (not shown in FIG. 1) by using a solder ball 14. The heat sink 12 is disposed on the underlay 15, and is configured to dissipate heat of the die 11. A plastic packaging material 16 seals the package body 10. In FIG. 1, a material of the heat sink 12 is a conductive material. Therefore, the heat sink 12 and the die 11 need to be insulated from each other by using the insulating plastic packaging material 16. In FIG. 1, the heat sink 12 is mostly located on the plastic packaging material 16, that is, the heat sink 12 is mostly located at a package layer formed by the plastic packaging material 16.

[0005] A heat dissipation method used for the package body shown in FIG. 1 is to design a heat path in an IC chip package structure, so as to spread heat of heat points by using the heat sink. According to this heat dissipation method, cooling is indiscriminately performed on the entire chip to remove the heat from the entire package body, so as to maintain a temperature of the chip under an upper limit of working.

[0006] However, the added heat sink still cannot be infinitely close to the IC die due to some physical limitations of an IC chip package technology and the IC chip package structure, and the IC die is a heat source. Therefore, a method for adding a heat sink to an IC chip package is not enough for reducing the temperatures of the heat points on the surface of the IC chip, or has a limited effect in an aspect of reducing the temperatures of the heat points. As a result, working of the IC chip is still limited by the temperatures of the heat points on the surface of the IC chip.

[0007] In conclusion, in a current heat dissipation method of an IC chip, because a heat sink is mainly added to an IC chip package structure, and the heat sink cannot be infinitely close to an IC die, this heat dissipation method has a limited effect in an aspect of reducing a temperature of a heat point on a surface of the IC chip.

SUMMARY

[0008] Embodiments of the present invention provide an integrated circuit die and a preparation method thereof, so as to resolve a problem that a currently used heat dissipation method of an IC chip has a limited effect in an aspect of reducing a temperature of a heat point on a surface of the IC chip.

[0009] According to a first aspect, an integrated circuit die is provided, including:

an underlay;
an active component;
an interconnection layer, covering the active component, where the interconnection layer includes multiple metal layers and multiple dielectric layers, the multiple metal layers and the multiple dielectric layers are alternately arranged, a metal layer whose distance to the active component is the farthest in the multiple metal layers includes metal cabling and a metal welding pad; and
a heat dissipation layer, where the heat dissipation layer covers a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer is located under a package layer, the package layer includes a plastic packaging material, and the heat dissipation layer includes an electrical-insulating material whose heat conductivity is greater than a preset value.

[0010] With reference to the first aspect, in a first possible implementation manner, the heat dissipation layer covers the metal layer whose distance to the active component is the farthest.

[0011] With reference to the first aspect, in a second possible implementation manner, the interconnection layer further includes a passivation layer; the passivation layer covers a region, above the metal layer whose dis-

tance to the active component is the farthest, except the position corresponding to the metal welding pad; and the heat dissipation layer covers the passivation layer.

[0012] With reference to the first aspect, in a third possible implementation manner, an integrated circuit chip including the integrated circuit die is a wire bonding chip, the heat dissipation layer is formed after a wire bonding technology is applied, and the heat dissipation layer further covers the position corresponding to the metal welding pad.

[0013] With reference to the first aspect, the first possible implementation manner of the first aspect, or the second possible implementation manner of the first aspect, in a fourth possible implementation manner, an integrated circuit chip including the integrated circuit die is a wire bonding chip or a flip chip.

[0014] According to a second aspect, a preparation method of an integrated circuit die is provided, including:

forming an active component on an underlay;
forming multiple metal layers and multiple dielectric layers on a surface of the active component in a manner of alternate arrangement, where the multiple metal layers and the multiple dielectric layers constitute an interconnection layer, and a metal layer whose distance to the active component is the farthest in the multiple metal layers includes metal cabling and a metal welding pad; and
forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, a heat dissipation layer that includes an electrical-insulating material whose heat conductivity is greater than a preset value, where the heat dissipation layer is located under a package layer that includes a plastic packaging material.

[0015] With reference to the second aspect, in a first possible implementation manner, the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer includes:

forming the heat dissipation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer; and
disposing an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad.

[0016] With reference to the second aspect, in a second possible implementation manner, the integrated circuit die further includes a passivation layer, and the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer includes:

forming the passivation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer;
disposing an opening at a position that is at the passivation layer and that is corresponding to the metal welding pad;
forming the heat dissipation layer on a surface of the passivation layer; and
disposing an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad.

[0017] With reference to the second aspect, in a third possible implementation manner, the integrated circuit die further includes a passivation layer, and if an integrated circuit chip including the integrated circuit die is a wire bonding chip, and the heat dissipation layer is formed after a wire bonding technology is applied, the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer includes:

forming the passivation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer;
disposing an opening at a position that is at the passivation layer and that is corresponding to the metal welding pad; and
forming the heat dissipation layer on a surface of the passivation layer.

[0018] Beneficial effects of the embodiments of the present invention include:

According to the integrated circuit die and the preparation method thereof provided in the embodiments of the present invention, because a heat dissipation layer covers a region above an interconnection layer in the IC die except a position corresponding to the metal welding pad, and is located under a package layer, the heat dissipation layer can be closer to the IC die. Because a material of the heat dissipation layer is an electrical-insulating material whose heat conductivity is greater than a preset value, the heat dissipation layer can rapidly spread heat in a region whose power density is relatively high in the IC die to a surface of the entire die, thereby increasing a heat dissipation area of an IC chip including the IC die, and improving a heat dissipation capability of the chip.

BRIEF DESCRIPTION OF DRAWINGS

[0019] To describe the technical solutions in the embodiments of the present invention more clearly, the following briefly describes the accompanying drawings required for describing the embodiments. Apparently, the accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still

derive other drawings from these accompanying drawings without creative efforts.

FIG. 1 is a cross-sectional view of an IC chip according to the prior art;

FIG. 2 is a cross-sectional view of a wire bonding chip according to an embodiment of the present invention;

FIG. 3 is a cross-sectional view of a flip chip according to an embodiment of the present invention;

FIG. 4a is a first cross-sectional view of an IC die in a wire bonding chip according to an embodiment of the present invention;

FIG. 4b is a first cross-sectional view of an IC die in a flip chip according to an embodiment of the present invention;

FIG. 5a is a second cross-sectional view of an IC die in a wire bonding chip according to an embodiment of the present invention;

FIG. 5b is a third cross-sectional view of an IC die in a wire bonding chip according to an embodiment of the present invention;

FIG. 6a is a second cross-sectional view of an IC die in a flip chip according to an embodiment of the present invention;

FIG. 6b is a third cross-sectional view of an IC die in a flip chip according to an embodiment of the present invention; and

FIG. 7 is a top view of an IC die according to an embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0020] According to the IC die and the preparation method thereof provided in embodiments of the present invention, a heat dissipation layer formed by an electrical-insulating material whose heat conductivity is greater than a preset value covers a region above an interconnection layer in the IC die except a position corresponding to a metal welding pad, and the heat dissipation layer is located under a package layer. Therefore, heat in a region whose power density is relatively high in the IC die is rapidly spread to a surface of the entire die, thereby increasing a heat dissipation area of an IC chip, and improving a heat dissipation capability of the chip.

[0021] With reference to the accompanying drawings of the specification, the following describes specific implementation manners of the IC die and the preparation method thereof provided in the embodiments of the present invention.

[0022] When the IC die provided in the embodiments of the present invention is packaged by using an existing package technology, an IC chip obtained after packaging compries two types: one is a wire bonding chip shown in FIG. 2, and the other is a flip chip shown in FIG. 3.

[0023] The wire bonding chip shown in FIG. 2 includes an IC die 102, a die bonding material 101, a leading wire 103, a plastic packaging material 104, a substrate 105, and a solder ball 106. A general technological process of packaging the wire bonding chip is as follows: first, manufacturing the IC die 102; then, fastening the IC die 102 to the substrate 105 by using the die bonding material 101; next, welding the leading wire 103 to the IC die 102 and the substrate 105 in a manner of wire bonding; afterwards, plastically packaging the IC die 102 by using the plastic packaging material 104; and last, welding the solder ball 106 to the substrate 105, thereby completing packaging of the entire wire bonding chip.

[0024] The flip chip shown in FIG. 3 includes an IC die 202, a metal bump (BUMP) 201, an underfill material 203, a plastic packaging material 204, a substrate 205, and a solder ball 206. A general technological process of packaging the flip chip is as follows: first, manufacturing the IC die 202, where the bump 201 is formed on the IC die 202; then, inverting and attaching the IC die 202 to the substrate 205, so as to physically and electrically connect the IC die 202 to the substrate 205 by using the bump 201; next, filling in the underfill material 203 to protect the bump 201; afterwards, plastically packaging the IC die 202 by using the plastic packaging material 204; and last, welding the solder ball 206 to the substrate 205, thereby completing packaging of the entire flip chip.

[0025] An embodiment of the present invention provides an IC die, and the IC die includes:

an underlay;

an active component, where the active component covers the underlay;

an interconnection layer, covering the active component, where the interconnection layer includes multiple metal layers and multiple dielectric layers, the multiple metal layers and the multiple dielectric layers are alternately arranged, a metal layer whose distance to the active component is the farthest in the multiple metal layers includes metal cabling and a metal welding pad; and

a heat dissipation layer, where the heat dissipation layer covers a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer is located under a package layer, the package layer includes a plastic packaging material, and the heat dissipation layer includes an electrical-insulating material whose heat conductivity is greater than a preset value, where the preset value may be 10 W/m-k.

[0026] That the multiple metal layers and the multiple dielectric layers are alternately arranged means that a first dielectric layer is formed above the active component first, the first metal layer is formed above the first dielectric layer next, a second dielectric layer is formed above the first metal layer next, and the second metal layer is formed above the second dielectric layer next, ..., until a quantity of metal layers and that of dielectric layers meet a requirement. Materials of all dielectric layers can be different materials, but are all electrical-insulating mate-

rials.

[0027] The metal cabling of the metal layer in the interconnection layer is to connect an electrode of the active component to a corresponding position, and the metal welding pad of the metal layer in the interconnection layer is to lead, for convenience of practical application, the electrode of the active component out of a package body that packages the IC die.

[0028] The heat dissipation layer may cover a part of the region above the interconnection layer in the IC die except the metal welding pad, or may cover the entire region above the interconnection layer in the IC die except the metal welding pad.

[0029] Optionally, as shown in FIG. 4a and FIG. 4b, the heat dissipation layer covers a region, above the metal layer whose distance to the active component in the IC die is the farthest in the interconnection layer in the IC die, except the position corresponding to the metal welding pad, where the heat dissipation layer may cover a part of a region of the metal welding pad in the IC die. In this case, because the material of the heat dissipation layer is an insulating material, the heat dissipation layer in FIG. 4a and FIG. 4b replaces a passivation layer in an IC die in the prior art.

[0030] FIG. 4a is a schematic structural diagram of an IC die in which a heat dissipation layer is used to replace a passivation layer when an IC chip is a wire bonding chip. FIG. 4a is a cross-sectional view of a dashed-line block 100 in FIG. 2. In FIG. 4a, the leading wire 103, a metal welding pad 107 that is located at a metal layer whose distance to an active component 111 is the farthest in an interconnection layer 112, a heat dissipation layer 109, and a underlay 110 are included. In FIG. 4a, the heat dissipation layer 109 further has a function of a passivation layer.

[0031] When the IC die shown in FIG. 4a is being produced, first, the active component 111 is formed on the underlay 110; then, multiple metal layers and multiple dielectric layers are alternately formed above the active component 111, where the multiple metal layers and the multiple dielectric layers constitute the interconnection layer 112, and the metal layer whose distance to the active component 111 is the farthest in the interconnection layer 112 contains the metal welding pad 107; and last, the heat dissipation layer 109 is formed above the metal layer that contains the metal welding pad 107, and an opening is disposed in a region that is at the heat dissipation layer and that directly faces the metal welding pad, where the opening may be smaller than the metal welding pad directly faced by the opening, provided that the IC die can be connected to a substrate in a heat dissipation enhanced IC chip by using a region that is on the metal welding pad and that directly faces the opening.

[0032] FIG. 4b is a schematic structural diagram of an IC die in which a heat dissipation layer is used to replace a passivation layer when an IC chip is a flip chip. FIG. 4b is a cross-sectional view of a dashed-line block 200 in FIG. 3. In FIG. 4b, the metal bump 201, a heat dissipation layer 207, under bump metal (UBM, under bump metal) 209, a metal welding pad 210 that is located at a metal layer whose distance to an active component 212 is the farthest in an interconnection layer 213, and a underlay 211 are included. In FIG. 4b, the heat dissipation layer 207 further has a function of the passivation layer.

[0033] When the IC die shown in FIG. 4b is being produced, first, the active component 212 is formed on the underlay 211; then, multiple metal layers and multiple dielectric layers are alternately formed above the active component 212, where the multiple metal layers and the multiple dielectric layers constitute the interconnection layer 213, and the metal layer whose distance to the active component 212 is the farthest in the interconnection layer 213 contains the metal welding pad 210; last, the heat dissipation layer 207 is formed above the metal layer that contains the metal welding pad 210, and an opening is disposed in a region that is at the heat dissipation layer 207 and that directly faces the metal welding pad 210, where the opening may be smaller than the metal welding pad directly faced by the opening, provided that the IC die can be connected to a substrate in a heat dissipation enhanced IC chip by using a region that is at the metal welding pad and directly faces the opening; and next, the UBM 209 and the metal bump 201 are sequentially produced upon the metal welding pad 210.

[0034] Optionally, when the interconnection layer in the IC die further includes a passivation layer, the passivation layer covers a region, above the metal layer whose distance to the active component is the farthest, except the position corresponding to the metal welding pad, and the heat dissipation layer covers the passivation layer. In this case, when an IC chip is a wire bonding chip, the IC die provided in this embodiment of the present invention is shown in FIG. 5a and FIG. 5b. When an IC chip is a flip chip, the IC die provided in this embodiment of the present invention is shown in FIG. 6a and FIG. 6b.

[0035] The IC die 102 shown in FIG. 5a includes a underlay 110, an active component 111, an interconnection layer 112, a passivation layer 108, and a metal welding pad 107 that is located at a metal layer whose distance to the active component 111 is the farthest in the interconnection layer 112. A heat dissipation layer 109 covers the passivation layer 108. An opening that is at the passivation layer 108 and that directly faces the metal welding pad 107 is smaller than or equal to an opening that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107. In FIG. 5a, description is made by using an example that the opening that is at the passivation layer 108 and that directly faces the metal welding pad 107 is smaller than the opening that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107. In FIG. 5a, the leading wire 103 is further included. FIG. 5a is a cross-sectional view of a dashed-line block 100 in FIG. 2.

[0036] In a process of producing the IC die shown in FIG. 5a, first, the active component 111 is formed on the

underlay 110; then, multiple metal layers and multiple dielectric layers are alternately formed above the active component 111, where the multiple metal layers and the multiple dielectric layers constitute the interconnection layer 112, and the metal layer whose distance to the active component 111 is the farthest in the interconnection layer 112 contains the metal welding pad 107; next, the passivation layer 108 is formed above the metal layer that contains the metal welding pad 107, and an opening is disposed in a region that is at the passivation layer 108 and that directly faces the metal welding pad; afterwards, the heat dissipation layer 109 is formed above the passivation layer 108, and an opening is disposed in a region that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107; and last, wire bonding is performed. The opening that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107 is not smaller than the opening that is at the passivation layer 108 and that directly faces the metal welding pad 107. That is, in the process of producing the IC die shown in FIG. 5a, the heat dissipation layer 109 is formed before wire bonding is performed.

[0037] The IC die 102 shown in FIG. 5b includes a underlay 110, an active component 111, an interconnection layer 112, a passivation layer 108, and a metal welding pad 107 that is located at a metal layer whose distance to the active component 111 is the farthest in the interconnection layer 112. A heat dissipation layer 109 covers the passivation layer 108. In FIG. 5b, the leading wire 103 is further included. FIG. 5b is a cross-sectional view of a dashed-line block 100 in FIG. 2.

[0038] In a process of producing the IC die shown in FIG. 5b, first, the active component 111 is formed on the underlay 110; then, multiple metal layers and multiple dielectric layers are alternately formed above the active component 111, where the multiple metal layers and the multiple dielectric layers constitute the interconnection layer 112, and the metal layer whose distance to the active component 111 is the farthest in the interconnection layer 112 contains the metal welding pad 107; next, the passivation layer 108 is formed above the metal layer that contains the metal welding pad 107, and an opening is disposed in a region that is at the passivation layer 108 and that directly faces the metal welding pad 107; afterwards, wire bonding is performed; and last, the heat dissipation layer 109 is formed on an active surface of the IC die. That is, in the process of producing the IC die shown in FIG. 5b, wire bonding is performed before the heat dissipation layer is formed. After the heat dissipation layer is formed, the heat dissipation layer 109 on the metal welding pad 107 can be removed, that is, an opening (shown in FIG. 5b) is disposed at a position that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107. A size relationship between the opening that is at the passivation layer 108 and that directly faces the metal welding pad 107 and the opening that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107 is not limited. Certainly, after the heat dissipation layer 109 is formed, the heat dissipation layer on the metal welding pad 107 may also not be removed. In addition, in FIG. 5b, description is made by using an example that the opening that is at the passivation layer 108 and that directly faces the metal welding pad 107 is larger than the opening that is at the heat dissipation layer 109 and that directly faces the metal welding pad 107.

[0039] The IC die 202 shown in FIG. 6a includes a underlay 211, an active component 212, an interconnection layer 213, where a UBM 209 is electroplated on a metal welding pad 210, the bump 201 is electroplated on the UBM 209, a heat dissipation layer 207 covers a passivation layer 208, and the metal welding pad 210 is located at a metal layer whose distance to the active component 212 is the farthest in the interconnection layer 213. FIG. 6a is a cross-sectional view of a dashed-line block 200 in FIG. 3.

[0040] In a process of producing the IC die shown in FIG. 6a, first, the active component 212 is formed on the underlay 110; then, multiple metal layers and multiple dielectric layers are alternately formed above the active component 212, where the multiple metal layers and the multiple dielectric layers constitute the interconnection layer 213, and the metal layer whose distance to the active component 212 is the farthest in the interconnection layer 213 contains the metal welding pad 210; next, the passivation layer 208 is formed above the metal layer that contains the metal welding pad 210, an opening is disposed in a region that is at the passivation layer 208 and that directly faces the metal welding pad 210, and the UBM 209 is electroplated in the opening region; afterwards, the heat dissipation layer 207 is formed above the passivation layer 208, and an opening is disposed in a region that is at the heat dissipation layer 207 and that directly faces the metal welding pad 210; and last, the bump 201 is electroplated on the UBM 209. The opening that is at the heat dissipation layer 207 and that directly faces the metal welding pad 210 is not smaller than the opening that is at the passivation layer 208 and that directly faces the metal welding pad 210.

[0041] The IC die 202 shown in FIG. 6b includes a underlay 211, an active component 212, an interconnection layer 213, where a UBM 209 is electroplated on a metal welding pad 210, the bump 201 is electroplated on the UBM 209, a heat dissipation layer 207 covers a passivation layer 208, and the metal welding pad 210 is located at a metal layer whose distance to the active component 212 is the farthest in the interconnection layer 213. FIG. 6b is a cross-sectional view of a dashed-line block 200 in FIG. 3.

[0042] In a process of producing the IC die shown in FIG. 6b, first, the active component 212 is formed on the underlay 110; then, multiple metal layers and multiple dielectric layers are alternately formed above the active component 212, where the multiple metal layers and the multiple dielectric layers constitute the interconnection layer 213, and the metal layer whose distance to the ac-

tive component 212 is the farthest in the interconnection layer 213 contains the metal welding pad 210; next, the passivation layer 208 is formed above the metal layer that contains the metal welding pad 210, an opening is disposed in a region that is at the passivation layer 208 and that directly faces the metal welding pad 210, and the UBM 209 is electroplated in the opening region; afterwards, the bump 201 is electroplated on the UBM 209, and the heat dissipation layer 207 is formed above the passivation layer 208; and last, because the IC die in the flip chip is connected to the substrate in the IC chip by using the bump 201, the heat dissipation layer 207 on a surface of the bump 201 further needs to be removed. The opening that is at the heat dissipation layer 207 and that directly faces the metal welding pad 210 is not smaller than the opening that is at the passivation layer 208 and that directly faces the metal welding pad 210.

[0043] A top view of the IC die in the chip shown in FIG. 2 or FIG. 3 may be shown in FIG. 7, and each includes an underlay, an active component, an interconnection layer, and a heat dissipation layer. When the interconnection layer in FIG. 7 further includes a passivation layer, FIG. 7 is a top view of any IC die of the IC dies shown in FIG. 5a, FIG. 5b, FIG. 6a, and FIG. 6b. When the interconnection layer in FIG. 7 does not include a passivation layer, FIG. 7 is a top view of the IC die shown in FIG. 4a or FIG. 4b.

[0044] In FIG. 7, a metal layer 31 whose distance to the active component is the farthest in the interconnection layer covering the active component in the IC die, and a heat dissipation layer 32 are included. The metal layer 31 may be further divided into metal cabling 311 and metal welding pads 312 in the metal layer. Some openings are disposed at positions that are at the heat dissipation layer 32 and that directly face the metal welding pads 312 of the metal layer 31, where each opening may be smaller than a corresponding metal welding pad. That is, the passivation layer covering the opening positions above the metal welding pads 312 needs to be removed, so that the IC die can be connected to a substrate in the IC chip by using the metal welding pads 312 that is not covered by the passivation layer.

[0045] In practice, a shape of the metal layer whose distance to the active component is the farthest in the interconnection layer covering the active component in the IC die is not limited to a shape shown in FIG. 7.

[0046] An embodiment of the present invention provides a preparation method of an IC die, and the method includes:

forming an active component on an underlay;

forming multiple metal layers and multiple dielectric layers on a surface of the active component in a manner of alternate arrangement, where the multiple metal layers and the multiple dielectric layers constitute an interconnection layer, and a metal layer whose distance to the active component is the farthest in the multiple metal layers includes metal cabling and a metal welding pad; and

forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, a heat dissipation layer that includes an electrical-insulating material whose heat conductivity is greater than a preset value, where the heat dissipation layer is located under a package layer that includes a plastic packaging material.

[0047] The position corresponding to the metal welding pad may be a region directly facing the metal welding pad.

[0048] In practice, the heat dissipation layer may be formed in a part of the region above the interconnection layer in the IC die except the metal welding pad, or the heat dissipation layer may be formed in the entire region above the interconnection layer in the IC die except the metal welding pad.

[0049] In this way, the heat dissipation layer can be in direct contact with the IC die, and can rapidly spread heat on the IC die to an entire chip, thereby increasing a heat dissipation area of the IC chip, and improving a heat dissipation capability of the chip.

[0050] Optionally, the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer includes:

forming the heat dissipation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer; and

disposing an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad.

[0051] In this way, the IC die can be connected, in a manner of wire bonding or a bump or in another manner, to the substrate in the IC chip by using a region that is on the metal welding pad and that is not covered by the heat dissipation layer. When the IC die is connected, in the manner of wire bonding, to the substrate in the IC chip by using the region that is on the metal welding pad and that is not covered by the heat dissipation layer, a schematic structural diagram of the IC die is shown in FIG. 4a. When the IC die is connected, in the manner of the bump, to the substrate in the IC chip by using the region that is on the metal welding pad and that is not covered by the heat dissipation layer, a schematic structural diagram of the IC die is shown in FIG. 4b.

[0052] When the interconnection layer of the IC die further includes a passivation layer, the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer includes:

forming the passivation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer;

disposing an opening at a position that is at the pas-

sivation layer and that is corresponding to the metal welding pad, that is, removing the passivation layer at the position corresponding to the metal welding pad;
forming the heat dissipation layer on a surface of the passivation layer; and
disposing an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad, that is, removing the heat dissipation layer at the position corresponding to the metal welding pad.

[0053] In this way, the IC die can be connected, in a manner of wire bonding or a bump or in another manner, to the substrate in the IC chip by using a region that is at the metal welding pad and that is not covered by the heat dissipation layer and the passivation layer. When the IC die is connected, in the manner of wire bonding, to the substrate in the IC chip by using the region that is at the metal welding pad and that is not covered by the heat dissipation layer and the passivation layer, a schematic structural diagram of the IC die is shown in FIG. 5a or FIG. 5b. When the IC die is connected, in the manner of the bump, to the substrate in the IC chip by using the region that is at the metal welding pad and that is not covered by the heat dissipation layer, a schematic structural diagram of the IC die is shown in FIG. 6a or FIG. 6b.

[0054] Optionally, when an IC chip is a wire bonding chip, and the heat dissipation layer is formed after wire bonding is performed, the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer includes:

forming a passivation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer;
disposing an opening at a position that is at the passivation layer and that is corresponding to the metal welding pad; and
forming the heat dissipation layer on a surface of the passivation layer, where in this technology, an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad may not need to be disposed.

[0055] The IC die and the preparation method thereof provided in the embodiments of the present invention are applicable to a wire bonding chip and a flip chip, and are further applicable to a chip in another package form.

[0056] According to a heat dissipation enhanced IC chip and a preparation method thereof provided in the embodiments of the present invention, a material of a heat dissipation layer is an electrical-insulating material whose heat conductivity is high, thickness of the heat dissipation layer may be any thickness required in this technology, and a method for forming the heat dissipation layer is not limited to methods such as physical sputtering, chemical deposition, electroplating, and coating.

[0057] A person skilled in the art may understand that the accompanying drawings are merely schematic diagrams of preferred embodiments, and modules or processes in the accompanying drawings are not necessarily required for implementing the present invention.

[0058] A person skilled in the art may understand that the modules in the apparatuses provided in the embodiments may be arranged in the apparatuses in a distributed manner according to the description of the embodiments, or may be arranged in one or more apparatuses that are different from those described in the embodiments. The modules in the foregoing embodiments may be combined into one module, or split into a plurality of submodules.

[0059] The sequence numbers of the foregoing embodiments of the present invention are merely for illustrative purposes, and are not intended to indicate priorities of the embodiments.

[0060] Obviously, a person skilled in the art can make various modifications and variations to the present invention without departing from the spirit and scope of the present invention. The present invention is intended to cover these modifications and variations provided that they fall within the scope of protection defined by the following claims and their equivalent technologies.

Claims

1. An integrated circuit die, comprising:

an underlay;
an active component;
an interconnection layer, covering the active component, wherein the interconnection layer comprises multiple metal layers and multiple dielectric layers, the multiple metal layers and the multiple dielectric layers are alternately arranged, a metal layer whose distance to the active component is the farthest in the multiple metal layers comprises metal cabling and a metal welding pad; and
a heat dissipation layer, wherein the heat dissipation layer covers a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer is located under a package layer, the package layer comprises a plastic packaging material, and the heat dissipation layer comprises an electrical-insulating material whose heat conductivity is greater than a preset value.

2. The integrated circuit die according to claim 1, wherein the heat dissipation layer covers the metal layer whose distance to the active component is the farthest.

3. The integrated circuit die according to claim 1, wherein the interconnection layer further comprises a passivation layer; the passivation layer covers a region, above the metal layer whose distance to the active component is the farthest, except the position corresponding to the metal welding pad; and the heat dissipation layer covers the passivation layer.

4. The integrated circuit die according to claim 1, wherein an integrated circuit chip comprising the integrated circuit die is a wire bonding chip, the heat dissipation layer is formed after a wire bonding technology is applied, and the heat dissipation layer further covers the position corresponding to the metal welding pad.

5. The integrated circuit die according to any one of claims 1 to 3, wherein an integrated circuit chip comprising the integrated circuit die is a wire bonding chip or a flip chip.

6. A preparation method of an integrated circuit die, comprising:

forming an active component on an underlay;
forming multiple metal layers and multiple dielectric layers on a surface of the active component in a manner of alternate arrangement, wherein the multiple metal layers and the multiple dielectric layers constitute an interconnection layer, and a metal layer whose distance to the active component is the farthest in the multiple metal layers comprises metal cabling and a metal welding pad; and
forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, a heat dissipation layer that comprises an electrical-insulating material whose heat conductivity is greater than a preset value, wherein the heat dissipation layer is located under a package layer that comprises a plastic packaging material.

7. The method according to claim 6, wherein the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer comprises:

forming the heat dissipation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer; and
disposing an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad.

8. The method according to claim 6, wherein the integrated circuit die further comprises a passivation layer, and the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer comprises:

forming the passivation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer;
disposing an opening at a position that is at the passivation layer and that is corresponding to the metal welding pad;
forming the heat dissipation layer on a surface of the passivation layer; and
disposing an opening at a position that is at the heat dissipation layer and that is corresponding to the metal welding pad.

9. The method according to claim 6, wherein the integrated circuit die further comprises a passivation layer, and if an integrated circuit chip comprising the integrated circuit die is a wire bonding chip, and the heat dissipation layer is formed after a wire bonding technology is applied, the forming, in a region above the interconnection layer except a position corresponding to the metal welding pad, the heat dissipation layer comprises:

forming the passivation layer above the metal layer whose distance to the active component is the farthest in the interconnection layer;
disposing an opening at a position that is at the passivation layer and that is corresponding to the metal welding pad; and
forming the heat dissipation layer on a surface of the passivation layer.

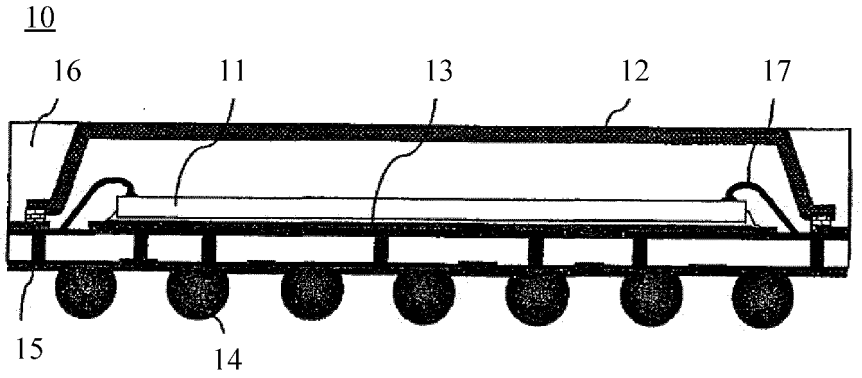

FIG. 1

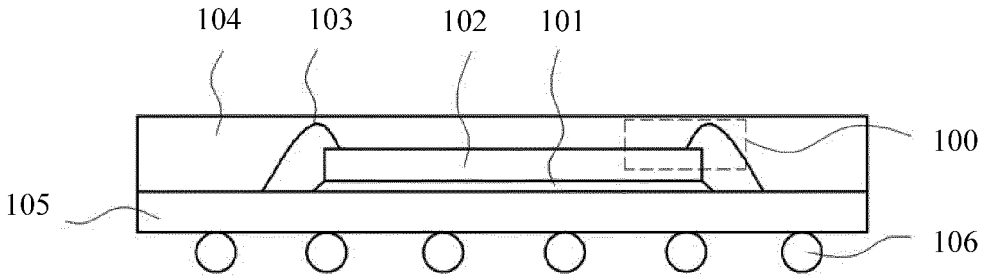

FIG. 2

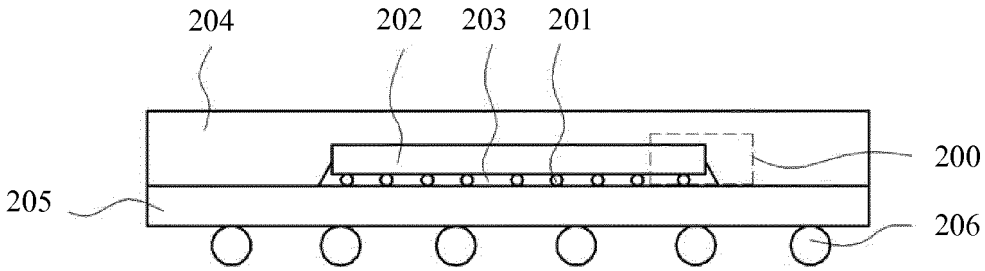

FIG. 3

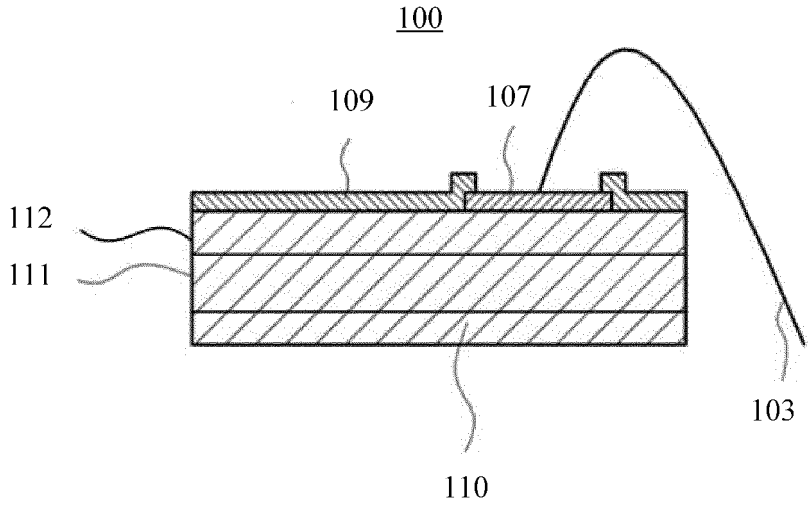

FIG. 4a

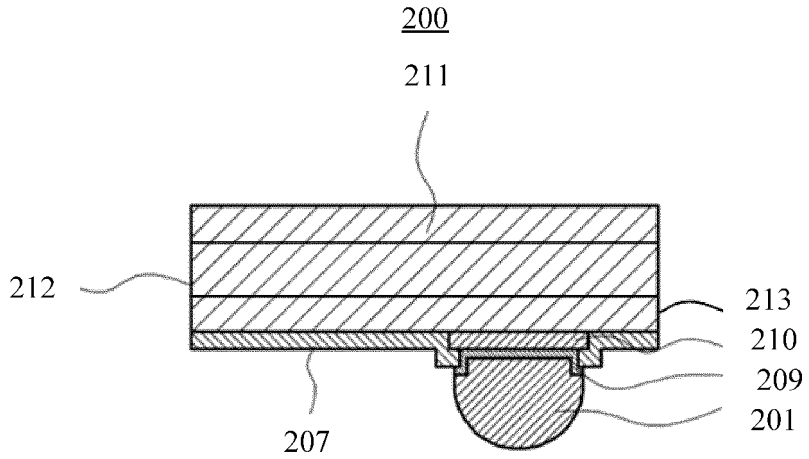

FIG. 4b

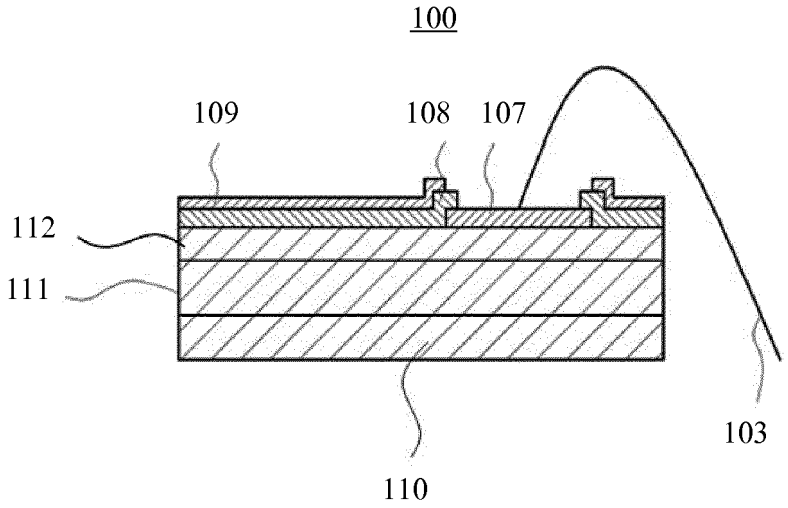

FIG. 5a

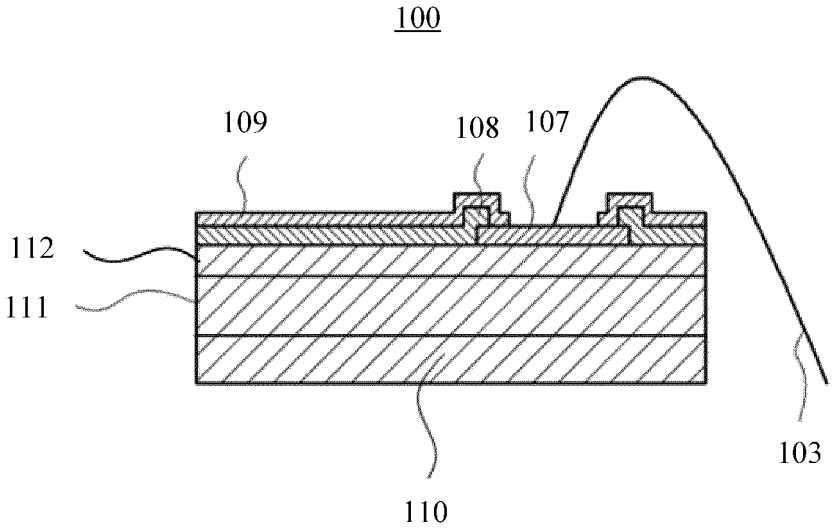

FIG. 5b

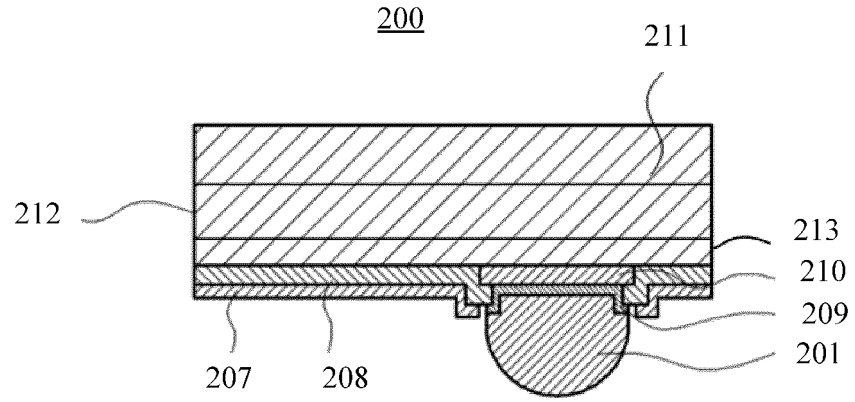
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FIG. 6a

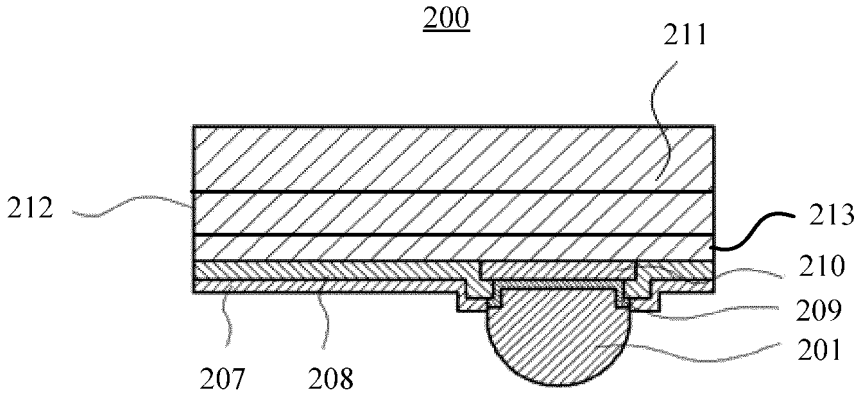
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FIG. 6b

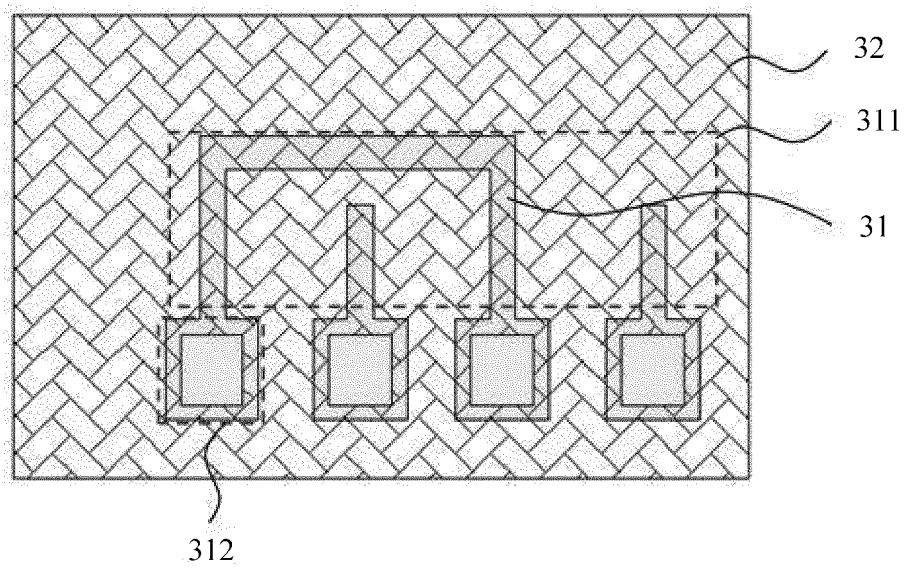

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/080514

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/485 (2006.01) i; H01L 23/367 (2006.01) i; H01L 21/60 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, DWPI: heat dissipation, insulation, dielectric layer, interconnect, pad, radiator, insulator, wiring, package, dielectric, substrate, die, chip

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104851860 A (HUAWEI TECHNOLOGIES CO., LTD.), 19 August 2015 (19.08.2015), the whole document	1-9
Y	CN 101026148 A (ADVANCED SEMICONDUCTOR ENGINEERING INC.), 29 August 2007 (29.08.2007), description, pages 4-9, and figure 2	1-9
Y	CN 103855109 A (INFINEON TECHNOLOGIES AG), 11 June 2014 (11.06.2014), description, paragraphs 18-20	1-9
A	CN 101980360 A (ADVANCED SEMICONDUCTOR ENGINEERING INC.), 23 February 2011 (23.02.2011), the whole document	1-9

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 July 2016 (27.07.2016)	**02 August 2016 (02.08.2016)**
Name and mailing address of the ISA/CN: State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No.: (86-10) 62019451	Authorized officer **DOU, Mingsheng** Telephone No.: (86-10) **62411819**

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/080514

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN 104851860 A	19 August 2015	None	
CN 101026148 A	29 August 2007	None	
CN 103855109 A	11 June 2014	US 2014151856 A1	05 June 2014
		US 9117786 B2	25 August 2015
		DE 102013113464 A1	05 June 2014
CN 101980360 A	23 February 2011	CN 101980360 B	29 August 2012

Form PCT/ISA/210 (patent family annex) (July 2009)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 201510221081 **[0001]**