(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 293 889 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
27.02.2019 Bulletin 2019/09

(21) Application number: **17190974.0**

(22) Date of filing: **13.09.2017**

(51) Int Cl.:
H04B 5/00 *(2006.01)* ***H04B 5/02*** *(2006.01)*

(54) SIGNAL ISOLATOR HAVING BIDIRECTIONAL DIAGNOSTIC SIGNAL EXCHANGE

SIGNALISOLATOR MIT BIDIREKTIONALEM DIAGNOSTISCHEM SIGNALAUSTAUSCH

ISOLATEUR DE SIGNAL À ÉCHANGE DE SIGNAUX DE DIAGNOSTIC BIDIRECTIONNELS

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **13.09.2016 US 201662393805 P**

(43) Date of publication of application:
14.03.2018 Bulletin 2018/11

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EP 3 293 889 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND

[0001] As is known in the art, signal isolators can be used to transfer information without a physical connection. For example, optocouplers can include a LED that emits light through an optically transparent insulating film (or dielectric) and strikes a photo detector that generates a current flow that corresponds to the emitted light. RF carriers can also be used to transmit information through a barrier. Data can be transferred from input to output using on/off keying (OOK) or other techniques.

[0002] US 2014/266332 A1 relates to a multi-channel isolation system that has N+1 isolators for N channels of communication data. N of the isolators may transfer data signals across an isolation barrier, one for each of the N channels of data. An N+1st isolator transfers refresh signals representing state of the data signals on the N isolators. Receiver circuitry, therefore, may receive signals from the N isolation channels without risk for collision with refresh signals. If reception of the refresh signals becomes necessary, circuitry on a receive side of the isolator may switch over to the N+1st receive path to output state data contained in the refresh signals.

[0003] US 2012/508820 A1 discloses a USB-based isolator system that conveys USB signals between a pair of galvanically isolated circuit systems and supports controlled enumeration by a downstream device on upstream USB signal lines. The isolator system provides a multi-mode voltage regulator to support multiple voltage supply configurations. The isolator system further provides control systems for each of the isolated circuit systems and provides robust control in a variety of start up conditions. Additionally, the isolator system includes refresh timers and watchdog mechanisms to support persistent operation but manage possible communication errors that can arise between the isolated circuit systems.

SUMMARY

[0004] The present invention provides a method and a signal isolator IC package according to independent claims 1 and 10. Preferred embodiments of the invention are stipulated in the dependent claims. While several embodiments and/or examples have been disclosed in this description, the subject matter for which protection is sought is strictly and solely limited to those embodiments and/or examples encompassed by the scope of the appended claims. Embodiments and/or examples mentioned in the description that do not fall under the scope of the claims are useful for understanding the invention. In embodiments, a non-optical signal isolator includes first and second dies, which may be matched, mounted on a split-paddle leadframe. In embodiments, the dies may be rotated 180 degrees from each other in order to allow for relatively direct connections between the dies. The signal isolator may comprise pairs of transmitters (TX) and receivers (RX), where each of the die contain both the drive (TX) and receive (RX) circuitry for each channel. With this arrangement, each functional channel can be set to convey signals in either direction, such as by selective wire-bonding, device programming, or the like.

[0005] In one particular embodiment, wire-bonding both the transmit and receive circuits for any given channel allows for bidirectional communication in that channel. This can be used to implement bidirectional channels for hand-shaking, error checking, etc., across the isolation barrier. For example, the receiver can communicate to the transmitter that it received a signal. In this way, the transmitter can be informed that transmitted messages have been received.

[0006] In illustrative embodiments, a signal isolator includes channels having transistor bridges on a first die driving coils on the second die, which generate a signal across a barrier that is picked up by magnetic sensors on the second die. In other embodiments, capacitive and/or inductive elements can be used to transmit and receive information across a barrier.

[0007] A device comprises: a first die; and a second die with a voltage barrier region between the first and second die, wherein transmit and receive paths of the first and second dies provide data transfer and bi-directional communication between the first and second die for feedback and/or diagnostic signals.

[0008] The device can further include one or more of the following features: the first path includes a first transmit path comprising, in order, a first transmitter bridge, a first coil, a first voltage isolation barrier and a first magnetic sensing element and a first receive path comprising, in order, a second magnetic sensing element, a second voltage isolation barrier, a second coil, and a second transmitter bridge, the magnetic sensing element of the ordered transmit path comprises a magnetoresistive (MR) element, the magnetic sensing element of the ordered transmit path comprises a giant magnetoresistive (GMR) element, the magnetic sensing element of the ordered transmit path comprises a tunneling magnetoresistive (TMR) element, the first and second dies are substantially identical, the first and second dies are identical and rotated one-hundred and eighty degrees with respect to each other, the first and second paths are programmable to transfer information in either direction, the first die is disposed on a first leadframe portion and the second die is disposed on a second leadframe portion, wherein the first and second leadframe portions are physically separated and electrically isolated from each other, the first leadframe portion includes a dimple array on which the first die is disposed, the device comprises an IC package, the first coil is wirebonded to the first bridge, the first transmitter bridge is located on or about the first die, the first coil is located on or about the second die, and the first magnetic sensing element is located on or about the second die, the second transmitter bridge is located on or about the second die, the second coil is

located on or about the first die, and the second magnetic sensing element is located on or about the first die, and/or the transmit path of the first die comprises the first transmitter bridge, and the transmit path of the second die comprises the first coil and the first magnetic sensing element.

[0009] A device comprises: a first die; a second die; and a voltage barrier means between the first and second die; and an encoding/decoding means for providing transmit and receive paths between the first and second sets of input/output pins, wherein the transmit and receive paths of the first and second dies provide bi-directional feedback and/or diagnostic signal transfer between the first and second die.

[0010] The device can further include one or more of the following features: the first path includes a first transmit path comprising, in order, a first transmitter bridge, a first coil, a first voltage isolation barrier and a first magnetic sensing element and a first receive path comprising, in order, a second magnetic sensing element, a second voltage isolation barrier, a second coil, and a second transmitter bridge, the first magnetic sensing element of the ordered transmit path comprises a magnetoresistive (MR) element, the first and second dies are substantially identical, the first and second dies are rotated one-hundred and eighty degrees with respect to each other, and/or a leadframe including a first leadframe portion having a dimple array on which the first die is disposed.

[0011] A method comprises: employing a first die; employing a second die; configuring the first and second dies for a voltage barrier region between the first and second dies; and selectively configuring the transmit and receive paths of the first and second dies to provide data transfer and bi-directional feedback and/or diagnostic signal transfer between the first and second die.

[0012] The method can further include one or more of the following features: the first path includes a first transmit path comprising, in order, a first transmitter bridge, a first coil, a first voltage isolation barrier and a first magnetic sensing element and a first receive path comprising, in order, a second magnetic sensing element, a second voltage isolation barrier, a second coil, and a second transmitter bridge, the first magnetic sensing element of the ordered transmit path comprises a magnetoresistive (MR) element, the first and second dies are substantially identical, the first and second dies are rotated one-hundred and eighty degrees with respect to each other, the first transmitter bridge is located on or about the first die, the first coil is located on or about the second die, and the first magnetic sensing element is located on or about the second die, the second transmitter bridge is located on or about the second die, the second coil is located on or about the first die, and the second magnetic sensing element is located on or about the first die, and/or the transmit path of the first die comprises the first transmitter bridge, and the transmit path of the second die comprises the first coil and the first magnetic sensing element.

[0013] The method can further include one or more of the following features: the transmitter data valid signal transitions state when the transmitter has a fault, the fault comprises loss of power, the receiver data valid signal transitions state when the receiver has a fault, intervals between the transmitter refresh signals increase when the receiver refresh signals have not been detected by the transmitter for a period of time, the transmitter data valid signal transitions state when transmit refresh signals are not received by the receiver and the receiver does not send receiver refresh signals, transitioning a state of the receiver data valid signal when the transmitter refresh signals are not received by the receiver for some period of time, after a communication failure between the transmitter and the receiver, re-establishing transmission of transmitter refresh signals and receiver refresh signals, the transmitter includes a transmitter transistor bridge and a transmitter coil in the first path, the receiver includes a receiver sensing element in the first path coupled with the transmitter coil, the receiver includes a receiver transistor bridge and a receiver coil, and/or the transmitter further includes a transmitter sensing element coupled to the receiver coil.

[0014] An IC package can further include one or more of the following features: the transmitter data valid signal transitions state when the transmitter has a fault, intervals between the transmitter refresh signals increase when the receiver refresh signals have not been detected by the transmitter for a period of time, the transmitter data valid signal transitions state when transmit refresh signals are not received by the receiver and the receiver does not send receiver refresh signals, transitioning a state of the receiver data valid signal when the transmitter refresh signals are not received by the receiver for some period of time, after a communication failure between the transmitter and the receiver, re-establishing transmission of transmitter refresh signals and receiver refresh signals, the transmitter includes a transmitter transistor bridge and a transmitter coil in the first path, the receiver includes a receiver sensing element in the first path coupled with the transmitter coil, the receiver includes a receiver transistor bridge and a receiver coil, and/or the transmitter further includes a transmitter sensing element coupled to the receiver coil.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following description of the drawings in which:

FIG. 1 is a schematic representation of a signal isolator having bidirectional data transfer in accordance with example embodiments of the invention;

FIG. 2 is a schematic representation of the isolator of FIG. 1 having matching first and second dies;

FIG. 3 is a cross-sectional side view of the isolator

of FIG. 1;

FIG. 4 is a pictorial representation of a prior art isolation having multiple dies and different dies;

FIGs. 5A and 5B are a schematic representation of a signal isolator having a coil/GMR sensing in accordance with example embodiments of the invention;

FIG. 6 is a perspective representation of a signal isolator having matching dies on a split leadframe in accordance with example embodiments of the invention;

FIG. 6A is a top view of a leadframe for a signal isolator having matching dies on a split leadframe in accordance with example embodiments of the invention;

FIG. 6B shows a perspective representation of matching dies of a signal isolator on the split leadframe of FIG. 6A;

FIG. 7 is a schematic representation of a signal isolator coupled to systems that may want to communicate with each other;

FIGs. 8A-F are example waveform diagrams showing fault detection and reporting in accordance with embodiments of the invention; and

FIG. 9 is a schematic representation of an example computer that may perform at least a portion of the processing described herein.

DETAILED DESCRIPTION

[0016] FIG. 1 shows an example of a signal isolator 100 including first and second dies 102, 104 that form part of an integrated circuit package 106 providing signal isolation. In an embodiment, the IC package 106 includes a first input/output (I/O) signal I/OA and a second I/O signal I/OB connected to the first die 102. The IC package 106 further includes a third I/O signal I/OC and a fourth I/O signal I/OD connected to the second die 104. The first and second dies 102, 104 are separated by a barrier region 108, such as a high voltage barrier.

[0017] In embodiments, the first and second I/O signals I/OA,B are coupled to respective transmit/receive modules 110, 112, each of which includes a transmitter 114, 116 and a receiver 118, 120. The transmit/receive modules 110, 112 are located on, in, or about the first die 102. The third and fourth I/O signals I/OC,D are coupled to respective transmit/receive modules 122, 124, each of which includes a transmitter 126, 128 and a receiver 130, 132. The transmit/receive modules 122, 124 are located on, in, or about the second die 104.

[0018] The first transmit/receive module 110 can function as a transmitter or a receiver. Similarly, the third transmit/receive module 122 can function as a transmitter or a receiver. In embodiments, the first I/O signal I/OA can be provided as an input signal to the IC 106 and the third I/O signal I/OC can be provided as an output signal of the IC for communication in a first direction, and vice-versa for communication in the opposite direction. In this configuration, an input signal to I/OA can be received by the IC 106 and output on I/OC with isolation across the barrier region 108. In embodiments, an input signal to I/OD can be received by the IC 106 and output on I/OB and vice-versa.

[0019] It is understood that any practical number of transmit, receive, and transmit/receive modules can be formed on the first and/or second die to meet the needs of a particular application. It is further understood that transmit, receive, and transmit/receive modules can comprise the same or different components.

[0020] FIG. 2 shows an example implementation of the IC 106 in which the first die 102 and the second die 104 are substantially identical and rotated 180 degrees in order to facilitate connections between the transmitters 114, 116 of the first die 102 and the receivers 130, 132 of the second die 104, as well as transmitters 126, 128 of the second die 104 and receivers 118, 120 of the first die 102. As can be seen, if the second die 104 is rotated 180 degrees, the pinout (VCC, GND I/Os, VCC) of the IC 106 and transmit and receive modules will line up so as to facilitate a series of relatively direct connections, such as wirebonds, between the first and second dies 102, 104. While the first and second die 102, 104 may be identical and rotated 180 degrees from each other, with the correct designation of transmit and receive channels, one can achieve a desired transfer of information to each die with connections nearly straight across the barrier between the dies.

[0021] In embodiments, the IC 106 can include a split die paddle in which a leadframe includes a first portion 130a on which the first die 102 is disposed and a second portion 130b on which the second die 104 is disposed. It will be appreciated that the first and second portions 130a,b of the leadframe isolates the first and second dies 102, 104. In embodiments, the first and second portions of the leadframe 130a,b are physically and electrically isolated. In embodiments, separate voltage supply signals and ground connections can be provided to each of the first and second dies 102, 104 of the IC 106 to promote isolation.

[0022] With this arrangement, digital signals can be provided as inputs to the IC 106 which can generate digital output signals that are isolated to enable systems to communicate with each other via the IC, for example. It is understood that the ground potential connections to the first and second dies can vary by hundreds of volts, for example. Isolation can be provided by capacitive, inductive, and/or coil to magnetic sensing elements for transferring information across the barrier.

[0023] FIG. 3 shows one particular implemention of an IC 106 having first and second dies 102, 104 on separate leadframe portions 130a,b. Polyimide, SiO2 or other insulating layer(s) 140, 142 for example, can be disposed on the dies 102, 104. Wirebonds 146 can connect the first and second dies 102, 104 to form the transmit/receive paths across the barrier. In embodiments, the wirebonds go up and down in opposite directions, as shown.

[0024] In embodiments, a die can be wire-bonded to terminals of a transmitter, such as a coil, which can be driven to create signals that are picked up by a sensing element, such as a GMR. In the illustrated embodiment, the left die 102 is transmitting to the right die 104. In the illustrated embodiment, the wire bond 146 is oriented to achieve a desired spacing between the wire bond and the edge of the die to mitigate breakdown from the wirebond to the edge of the die.

[0025] In conventional isolators, dies are either a receive die or a transmit die, as shown in FIG. 4, which shows a NVE digital isolator that uses coil to GMR for isolated signal transfer. Four die are used to create a device with signals going in both directions. The top left and bottom right die are receiver dies, and the bottom left and top right are transmitter dies.

[0026] FIGs. 5A and 5B show an embodiment of an IC package 500 for a signal isolator having matched dies with transmit/receive programmability in accordance with example embodiments of the invention. A first power supply input VDD1 provides power to a first die 502 and a second power supply input VDD2 provides power to a second die 504. A first ground pin GND1 provides a ground reference for the first die 502 and a second ground pin GND2 provides a ground references for the second die 504. In embodiments, the ground pins GND1, GND2 are isolated from each other.

[0027] Signal pins include IN/OUTA and OUT/INB connected to the first die 502 and OUT/INA and IN/OUTB connected to the second die 504. In the illustrated embodiment, each of IN/OUTA OUT/INB, OUT/INA and IN/OUTB, can be programmed as an input or output signal. In embodiments, these signals may be programmed in pairs to provide a signal path through the barrier region 508 between the first and second dies 502, 504.

[0028] The first die 502 can include a first encoding/decoding module 510 coupled to signal pins include IN/OUTA and OUT/INB and the second die 504 can include a second encoding/decoding module 511 coupled to signal pins include OUT/INA and IN/OUTB. The first die 502 includes a first transmitter 512 that can be provided as a transistor bridge circuit coupled to the first encoding/decoding module 510. The first die 502 can further include a second transmitter 514. The first die includes a first receiver 516 that can be provided as a sensing element, such as a magnetic sensing element, which is shown as a GMR bridge. The first die 502 can further include a second receiver 518.

[0029] The second die 504 includes a third transmitter 520 that can be provided as a transistor bridge circuit coupled to the second encoding/decoding module 511. The second die 504 can further include a fourth transmitter 522. The second die 504 includes a third receiver 524 that can be provided as a sensing element, such as a GMR bridge. The first die can further include a fourth receiver 526.

[0030] In embodiments, the first die 502 includes a first coil 530 positioned in relation to the first GMR bridge 516 to detect signal information from the coil 530 and a second coil 532 for the second GMR bridge. The second die 504 can include coils 534, 536 for respective bridges 524, 526 on the die for detecting signals from transmitters 512, 514 on the first die 502.

[0031] In an example for the illustrated embodiment, the coil 530 is energized by the first transmitter 520 of the second die 504 and sensed by the GMR bridge 516. In one particular configuration, an input signal received on OUT/INA is received and provided to transmitter 520 in accordance with a path configuration of the second encoding/decoding module 511. The transmitter 520 energizes the coil 530 on the first die 502 for sensing by bridge 516. In accordance with path configuration data in the first encoding/decoding module 510, the sensed signal is provided to the IN/OUTA pin of the IC 500.

[0032] The first and second encoding/decoding modules 510, 511 selectively configure a path between one of IN/OUTA and OUT/INB for the first die 502 and one of OUT/INA and IN/OUTB for the second die 504. The programmability of the paths enables each of IN/OUTA, OUT/INB, OUT/INA and IN/OUTB to be an input signal or an output signal with desired signal isolation.

[0033] The first and second encoding/decoding modules 510, 511 can each include a respective diagnostic module 560, 561 for generating refresh signals, such as pulses between transmit and receive paths, as described more fully below. In embodiments, transmitter 512, coil 534, and sensing element 524, and transmitter 520, coil 530 and sensing element 516 can provide bi-directional communication between the first and second die for feedback and diagnostic signals, as described below.

[0034] FIG. 6 shows a schematic representation of first and second die 602, 604 on a split leadframe having isolated first and second portions 606, 608 with wirebonds 610 providing transmit/receive paths between the dies and power/ground connections. As can be seen, the first and second die 602, 604 are substantially identical and rotated 180 degrees with respect to each other to facilitate the transmitter-receiver wirebond connections between the first and second dies.

[0035] Embodiments of the invention may allow for a single die configuration to be used to provide isolated transmitter-receiver channels between first and second dies housed in a single IC package. With this arrangement, a single die design can be developed, produced, and tested to simplify and lower the cost of the process and the supply chain. In contrast to conventional isolator ICs that require multiple die designs, embodiments of the invention may utilize two substantially identical die for a

bidirectional isolator IC package.

[0036] In embodiments, wire bonds can be connected across a barrier between first and second die to enable selection of a direction of each channel through programming, such as during final test. This simplifies the supply chain since all of the versions of the IC package may be the same up until final test. In alternative embodiments, directionality can be determined during assembly, for example by the wire bonds. In further embodiments, pull up/down wire-bonding can be used to program the devices instead of configuration data in non-volatile memory, for example.

[0037] It will be appreciated that bi-directionality on each channel allows for hand-shaking and error checking as data is transmitted and received. For example, a transmitter can receive information from a receiver that data is being received. It is understood that conventional isolators, such as optical isolators, do not allow for a receiver to send information to the transmitter.

[0038] FIG. 6A shows an example split leadframe 650 having isolated first and second portions 652a,b and FIG. 6B shows the split leadframe 650 having matched first and dies 654a,b disposed on the respective first and second leadframe portions 652a,b. The first portion 652a of the leadframe can include dimples 656 in an array configuration. In the illustrated embodiment, the dimple array is a 3 x 6 array. It is understood that dimples 656 comprise a protrusion of some sort above the planar surface of the leadframe to mitigate delamination of the die from the leadframe. It is further understood that the array can include columns and rows of dimples, a random distribution of dimples, and/or a combination thereof.

[0039] In the illustrated embodiment, pin numbers are shown from pin 1 in the top right to pin 16 in the bottom right. In one particular embodiment, pins 2, 8, 9, and 15 are configured for connection to ground. In one embodiment, pins 2 and 8 form one ground that is different from another ground formed by pins 9 and 16

[0040] In embodiments, the leadframe portions can include respective tails 658a, b to enhance clamping during wirebonding 662 to the leadframe fingers. In some embodiments, one or more anchor holes 660 can be stamped or etched in one or more pins to facilitate mold adhesion on floating leads, for example.

[0041] FIG. 6B shows connections 664 between transmitters and receivers on the respective dies 654a,b as shown and described above.

[0042] FIG. 7 shows an example isolator 700 IC in accordance with illustrative embodiments coupled to first, second, third, and fourth systems S1, S2. S3, S4. The first system S1 can transmit and receive data with the second system S2 and the third system S3 can communicate with the fourth system S4. In embodiments, the first system S1 can communicate with the fourth system S4 with control of the data paths by the first and second encoding/decoding modules 510, 511 (FIG. 5). Similarly, the third system S3 can communicate with the second system S2 and/or fourth system S4. In embodiments, the second system S2 can communicate with the first and/or third systems S1, S3, and the fourth system S4 can communicate with the first and/or third systems S1, S3. In embodiments, a system can communicate with one or more systems coupled across the barrier via first and second dies.

[0043] In another aspect of the invention, a signal isolator includes diagnostic functionality to determine if signals are transferring correctly. In embodiments, an internal return communication channel on a unidirectional external communication channel can be used for implementing diagnostics to determine if signals are transferring correctly. Diagnostic results may be provided to systems coupled to the isolation IC package on each side the isolation barrier. In embodiments, an isolator IC package can include a data valid pin associated with each of the first and second dies to provide diagnostic results indicating whether data was successfully transferred over the channels. A diagnostic failure can be communicated via one of the communication channels on one or both sides of the barrier. In embodiments, a diagnostic failure can cause the signal isolator to enter a pre-determined state, such as data transmission/reception stoppage. Output(s) may enter a predetermined state or signal level or become high-impedance.

[0044] Referring again to FIG. 5, first and second data valid pads 550, 552 may be provided for the respective first and second dies 502, 504. Data valid signals can be provided as pins DVA and DVB on the IC package and controlled by the respective first and second encoding/decoding modules 510, 511, which can monitor transmit and receive signal, as described more fully below.

[0045] In embodiments, for each channel between the first and second dies, there is a driver, coil, and GMR signal path in each direction. For example, channel A (upper channel) may transfer information from left to right, such that bridge 512 to coil 534 to GMR 524 can be used for signal transfer. The path of bridge 520 to coil 530 to GMR 516 for channel A (the lower path for channel A), provides data flow in the opposite direction for enabling a receiver to indicate to the transmitter that the message was received. Similar upper and lower paths can be formed for channel B to enable bi-directional data flow.

[0046] The receiver can indicate that the message was received and/or echo the message back and/or periodically indicate that messages are being received. Through handshaking, the transmitter and receiver can both determine that communications are flowing between the first and second die. In embodiments, the status of the data flows for the upper and lower channel A is indicated with the respective data valid pins DVA, DVB. In this way, the systems on both sides of the isolation barrier are able to know whether the information they are sending is being received and/or whether information is being sent.

[0047] In example embodiments, signal edges are transmitted across the barrier between the first and second dies. When the input transitions, a pulse of current is injected in the coil in the direction of change in order

to indicate this change to the receiver. For example, a high to low transition results in a negative pulse of current. In embodiments, the transmitter repeats the last transition at a fixed interval Trefresh if there is no change on the input. The receiver sends a similar refresh pulse. In example embodiments, every 1.5*Trefresh, as long as the receiver has received a pulse from the transmitter, the receiver issues a pulse to the transmitter. The receiver issues a positive pulse if its output is high and a negative pulse if its output is low.

[0048] In embodiments, receiver and transmitter refresh signals and example times and edges are monitored to determine the health of the transmit and receive paths between the die. It is understood that a wide range of signal types, characteristics, timing, durations, etc., can be used to monitors signals along the transmit and receive paths without departing from the scope of the invention.

[0049] In other embodiments, the receiver constantly reflects received pulses back to the transmitter to allow for fast checking of the communication, as well as bit by bit correctness. In the event that the receiver does not receive a pulse from the transmitter in 1.5*Trefresh, for example, the receiver may de-assert its data valid pin to indicate to the system on that side that the receiver has stopped receiving information from the transmitter. In the event that the transmitter does not see a pulse back from the receiver in 2*Trefresh, for example, the transmitter de-asserts its data valid pin, indicating to the system on that side that the information being sent is no longer being received. In embodiments, the transmitter can also slow its refresh pulses to 3*Trefresh, for example.

[0050] In embodiments, if the transmitter determines that one of its inputs is floating, the transmitter may stop transmitting pulses on that channel and de-assert its data valid pin. Similarly, if any type of built-in self-test (BIST) on either the transmitter or receiver fails, the IC may stop sending pulses across the barrier and de-assert its data valid pin.

[0051] FIG. 8A shows an example waveform in which refresh pulses are generated by a transmitter with an edge at a given intervals t_refresh and receiver refresh pulses are generated at intervals of 1.5*t_refresh. A transmitter data valid signal and a receiver data valid signal are initially at a level corresponding to valid data while the data and refresh pulses are being timely transmitted.

[0052] In embodiments, a transmitter may refer to a signal source, such as bridge 512 in FIG. 5, which may include coil 534, and a receiver may refer to a sensing element, such as sensing element 524 in FIG. 5, which is coupled to coil 534. In embodiments, data may go in one direction from a transmitter to a receiver and refresh/diagnostic signals flow in both directions. In embodiments, refresh signals are transmitted by a transmitter when there is no data to be transmitted to the receiver.

[0053] At a given time t_{TPL}, the transmitter loses power causing the transmitter data valid signal to transition indicating that data is no longer valid. Refresh pulses cease being transmitted and nothing is transmitted to the receiver. At time t_{TRL}, which is 1.5*Trefresh from the last transmitter refresh pulse edge, the receiver de-asserts its data-valid pin.

[0054] FIG. 8B shows the same signals as FIG. 8A when the receiver loses power or enable pin is logic low at time t_{RPL} : In this case, the transmitter will not receive any return pulses from the receiver. After time 2*Trefresh, for example, from the last receiver refresh pulse edge, the transmitter de-asserts its data-valid pin at time t_{RRL}. The transmitter may also slow down its refresh pulses to 3*t_refresh but continue to issue them, in order to recover in the case that the receiver regains power.

[0055] FIG. 8C shows waveforms corresponding to broken transmit/receive circuitry on the forward path (e.g., wire bond breaks, GMR breaks, etc...): The transmitter is not aware that the transmitted pulses are not being received. The receiver does not receive any information. At time t_{BRK}, which corresponds to 1.5*Trefresh, for example, from the last transmitter refresh pulse edge, the receiver de-asserts its data-valid pin. Also, the receiver does not send any reverse refresh pulses, so that the transmitter de-asserts its data-valid pin at time t_{DA} and slows down its refresh rate. A reverse pulse may refer to a situation in which the receiver is looking for refresh pulses every Trefresh, and the transmitter is looking for refresh pulses (reverse refresh pulse) every 2*Trefresh, for example. If the transmitter does not see a reverse pulse, for example, it is determined that the receiver is having problems.

[0056] FIG. 8D shows waveforms corresponding to a break in the transmit/receive circuitry on the reverse path (e.g., wire bond breaks, GMR breaks, etc.). In this case, the receiver is receiving the correct information, but the receiver is not able to provide an indication of this to the transmitter. In this situation, the transmitter will not receive any reverse pulses, so it will de-assert its data-valid pin at time t_{RBRK} and start sending pulses at 3*Trefresh, for example. In this way, the receiver will then time-out on the other side and de-assert its data-valid pin at time t_{RDA}.

[0057] FIG. 8E shows waveforms corresponding to the transmitter input not being driven. The transmitter detects this situation at time t_{TP}, stops sending refresh pulses across the barrier, and de-asserts its data valid pin. The receiver does not see any transmitter refresh pulses and de-asserts its data valid pin at time t_{RDA}, which can correspond to 1,5*t_refresh from the edge of the last transmitter refresh pulse.

[0058] The waveforms can also correspond to a failure of built-in-self-test (BIST) of the transmitter. The transmitter stops sending pulses and de-asserts its data valid pin. The receiver will not see any pulses and de-asserts its data valid pin.

[0059] FIG. 8F shows waveforms corresponding to BIST failure on the receiver. The receiver detects a problem at time t_{RDB} and stops sending refresh pulses and

de-asserts its data valid pin. The transmitter stops seeing pulses in return and de-assert its data valid pin at time t_{TDA}, which can correspond to 2*t_refresh since the edge of the last receiver refresh pulse. The transmitter may also slow down its refresh pulses until it sees a return pulse.

[0060] While embodiments of the invention are shown in described in conjunction with coil and GMR-based sensing, it is understood that other components, such as capacitor and/or inductive elements, can be used in other embodiments In addition, a variety of magnetic field sensing elements can be used.

[0061] As used herein, the term "magnetic field sensing element" is used to describe a variety of electronic elements that can sense a magnetic field. The magnetic field sensing element can comprise, but is not limited to, a Hall Effect element, a magnetoresistance element, and/or a magnetotransistor. As is known, there are different types of Hall Effect elements, for example, a planar Hall element, a vertical Hall element, and a Circular Vertical Hall (CVH) element. As is also known, there are different types of magnetoresistance elements, for example, a semiconductor magnetoresistance element such as Indium Antimonide (InSb), a giant magnetoresistance (GMR) element, for example, a spin valve, an anisotropic magnetoresistance element (AMR), a tunneling magnetoresistance (TMR) element, a magnetic tunnel junction (MTJ), and a spin-valve. The magnetic field sensing element may be a single element or, alternatively, may include two or more magnetic field sensing elements arranged in various configurations, e.g., a half bridge or full (Wheatstone) bridge. Depending on the device type and other application requirements, the magnetic field sensing element may be a device made of a type IV semiconductor material such as Silicon (Si) or Germanium (Ge), or a type III-V semiconductor material like Gallium-Arsenide (GaAs) or an Indium compound, e.g., Indium-Antimonide (InSb).

[0062] As is known, some of the above-described magnetic field sensing elements tend to have an axis of maximum sensitivity parallel to a substrate that supports the magnetic field sensing element, and others of the above-described magnetic field sensing elements tend to have an axis of maximum sensitivity perpendicular to a substrate that supports the magnetic field sensing element. In particular, planar Hall elements tend to have axes of sensitivity perpendicular to a substrate, while metal based or metallic magnetoresistance elements (e.g., GMR, TMR, AMR) and vertical Hall elements tend to have axes of sensitivity parallel to a substrate.

[0063] As used herein, the term "magnetic field sensor" is used to describe a circuit that uses a magnetic field sensing element, generally in combination with other circuits. Magnetic field sensors are used in a variety of applications, including, but not limited to, an angle sensor that senses an angle of a direction of a magnetic field, a current sensor that senses a magnetic field generated by a current carried by a current-carrying conductor, a magnetic switch that senses the proximity of a ferromagnetic object, a rotation detector that senses passing ferromagnetic articles, for example, magnetic domains of a ring magnet or a ferromagnetic target (e.g., gear teeth) where the magnetic field sensor is used in combination with a back-biased or other magnet, and a magnetic field sensor that senses a magnetic field density of a magnetic field.

[0064] FIG. 9 shows an exemplary computer 900 that can perform at least part of the processing described herein. The computer 900 includes a processor 902, a volatile memory 904, a non-volatile memory 906 (e.g., hard disk), an output device 907 and a graphical user interface (GUI) 908 (e.g., a mouse, a keyboard, a display, for example). The non-volatile memory 906 stores computer instructions 912, an operating system 916 and data 918. In one example, the computer instructions 912 are executed by the processor 902 out of volatile memory 904. In one embodiment, an article 920 comprises non-transitory computer-readable instructions.

[0065] Processing may be implemented in hardware, software, or a combination of the two. Processing may be implemented in computer programs executed on programmable computers/machines that each includes a processor, a storage medium or other article of manufacture that is readable by the processor (including volatile and non-volatile memory and/or storage elements), at least one input device, and one or more output devices. Program code may be applied to data entered using an input device to perform processing and to generate output information.

[0066] The system can perform processing, at least in part, via a computer program product, (e.g., in a machine-readable storage device), for execution by, or to control the operation of, data processing apparatus (e.g., a programmable processor, a computer, or multiple computers). Each such program may be implemented in a high level procedural or object-oriented programming language to communicate with a computer system. However, the programs may be implemented in assembly or machine language. The language may be a compiled or an interpreted language and it may be deployed in any form, including as a stand-alone program or as a module, component, subroutine, or other unit suitable for use in a computing environment. A computer program may be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a communication network. A computer program may be stored on a storage medium or device (e.g., CD-ROM, hard disk, or magnetic diskette) that is readable by a general or special purpose programmable computer for configuring and operating the computer when the storage medium or device is read by the computer. Processing may also be implemented as a machine-readable storage medium, configured with a computer program, where upon execution, instructions in the computer program cause the computer to operate.

[0067] Processing may be performed by one or more

programmable processors executing one or more computer programs to perform the functions of the system. All or part of the system may be implemented as, special purpose logic circuitry (e.g., an FPGA (field programmable gate array) and/or an ASIC (application-specific integrated circuit)).

[0068] Having described exemplary embodiments of the invention, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may also be used. The embodiments contained herein should not be limited to disclosed embodiments but rather should be limited only by the scope of the appended claims.

Claims

1. A method, comprising:

employing first (102, 502, 602) and second (104, 504, 604) dies having a voltage barrier region (108, 508) between the first and second dies, and wherein transmit and receive paths of the first and second dies provide data transfer and bi-directional transfer of feedback and/or diagnostic signals between the first and second die; and

sending, by a transmitter (114, 116, 512,514) on the first die, transmitter refresh signals to a receiver (130, 132, 524, 526) on the second die;

sending, by the receiver, receiver refresh signals to the transmitter in response to the transmitter refresh signals;

determining that the transmitter refresh signals have not been received by the receiver for a first period of time;

transitioning a receiver data valid signal after determining that the transmitter refresh signals have not been received for the first period of time, and

further including transitioning a transmitter data valid signal after detecting that the receiver refresh signals have not been received by the transmitter for a second period of time.

2. The method according to claim 1, wherein the transmitter data valid signal transitions state when the transmitter has a fault.

3. The method according to claim 2, wherein the fault comprises loss of power.

4. The method according to claim 2, wherein the receiver data valid signal transitions state when the receiver has a fault.

5. The method according to claim 1, wherein intervals between the transmitter refresh signals increase when the receiver refresh signals have not been detected by the transmitter for a period of time.

6. The method according to claim 1, wherein the transmitter data valid signal transitions state when transmit refresh signals are not received by the receiver and the receiver does not send receiver refresh signals.

7. The method according to claim 6, further including transitioning a state of the receiver data valid signal when the transmitter refresh signals are not received by the receiver for some period of time.

8. The method according to claim 1, further including, after a communication failure between the transmitter and the receiver, re-establishing transmission of transmitter refresh signals and receiver refresh signals.

9. The method according to claim 1, wherein the transmit refresh signals are sent in the absence of data to transfer.

10. A signal isolator IC package, comprising:

first (102, 502, 602) and second (104, 504, 604) dies having a voltage barrier region (108, 508) between the first and second dies, and wherein transmit and receive paths of the first and second dies provide bi-directional data transfer between the first and second dies; and

a diagnostic module configured to:

send, by a transmitter (114, 116, 512,514) on the first die, transmitter refresh signals to a receiver (130, 132, 524, 526) on the second die;

send, by the receiver, receiver refresh signals to the transmitter in response to the transmitter refresh signals;

determine that the transmitter refresh signals have not been received by the receiver for a first period of time;

transition a receiver data valid signal after determining that the transmitter refresh signals have not been received for the first period of time, and transition a transmitter data valid signal after detecting that the receiver refresh signals have not been received by the transmitter for a second period of time.

11. The IC package according to claim 10, wherein the diagnostic module is further configured to carry out the method steps of any of claims 2 to 9.

12. The IC package according to claim 10 or 11, wherein the transmitter includes a transmitter transistor

bridge (512) and a transmitter coil (534) in the transmit path.

13. The IC package according to claim 12, wherein the receiver includes a receiver sensing element (524) coupled with the transmitter coil.

14. The IC package according to claim 13, wherein the receiver includes a receiver transistor bridge (520) and a receiver coil (530).

15. The IC package according to claim 14, wherein the transmitter further includes a transmitter sensing element (516) coupled to the receiver coil.

Patentansprüche

1. Verfahren, das Folgendes umfasst:

Anwenden von einer ersten (102, 502, 602) und einer zweiten (104, 504, 604) Matrize, die einen Spannungsbarriere-Bereich (108, 508) zwischen der ersten und der zweiten Matrize aufweisen, und wobei die Übertragung und der Empfang der ersten und der zweiten Matrize Datenübertragung und bidirektionale Übertragung von Feedback und/oder Diagnosesignalen zwischen der ersten und der zweiten Matrize bereitstellen; und
Senden von Sender-Refresh-Signalen durch einen Sender (114, 116, 512, 514) auf der ersten Matrize an einen Empfänger (130, 132, 524, 526) auf der zweiten Matrize;
Senden von Empfänger-Refresh-Signalen durch den Empfänger an den Sender als Reaktion auf die Sender-Refresh-Signale;
Bestimmen, dass die Sender-Refresh-Signale durch den Empfänger für eine erste Zeitspanne nicht empfangen worden sind;
Wandeln von einem gültigen Empfängerdatensignal nach Bestimmen, dass die Sender-Refresh-Signale für die erste Zeitspanne nicht empfangen worden sind, und
ferner Einschließen des Wandeins eines gültigen Senderdatensignals nach Erfassen, dass die Empfänger-Refresh-Signale durch den Sender für eine zweite Zeitspanne nicht empfangen worden sind.

2. Verfahren nach Anspruch 1, wobei das gültige Senderdatensignal den Zustand wandelt, wenn der Sender eine Störung aufweist.

3. Verfahren nach Anspruch 2, wobei die Störung einen Stromverlust umfasst.

4. Verfahren nach Anspruch 2, wobei das gültige Empfängerdatensignal den Zustand wandelt, wenn der Empfänger eine Störung aufweist.

5. Verfahren nach Anspruch 1, wobei Intervalle zwischen den Sender-Refresh-Signalen sich vergrößern, wenn die Empfänger-Refresh-Signale durch den Sender für eine erste Zeitspanne nicht erfasst worden sind.

6. Verfahren nach Anspruch 1, wobei das gültige Senderdatensignal den Status wandelt, wenn Sender-Refresh-Signale durch den Empfänger nicht empfangen werden und der Empfänger keine Empfänger-Refresh-Signalen sendet.

7. Verfahren nach Anspruch 6, das ferner das Wandeln eines Zustands der gültigen Empfängerdatensignale einschließt, wenn die Sender-Refresh-Signale durch den Empfänger für eine gewisse Zeitspanne nicht empfangen werden.

8. Verfahren nach Anspruch 1, das ferner nach einer Kommunikationsstörung zwischen dem Sender und dem Empfänger den Wiederaufbau der Übertragung von Sender-Refresh-Signalen und Empfänger-Refresh-Signalen einschließt.

9. Verfahren nach Anspruch 1, wobei die Sender-Refresh-Signale bei Fehlen von zu übertragenden Daten gesendet werden.

10. Signaltrenner-IC-Paket, das Folgendes umfasst:

eine erste (102, 502, 602) und eine zweite (104, 504, 604) Matrize, die einen Spannungsbarriere-Bereich (108, 508) zwischen der ersten und der zweiten Matrize aufweisen, und wobei Übertragungs- und Empfangspfade von der ersten und der zweiten Matrize bidirektionale Datenübertragung zwischen der ersten und der zweiten Matrize bereitstellen; und
ein Diagnosemodul, das für Folgendes ausgestaltet ist:

Senden von Sender-Refresh-Signalen durch einen Sender (114, 116, 512, 514) auf der ersten Matrize an einen Empfänger (130, 132, 524, 526) auf der zweiten Matrize;
Senden durch den Empfänger von Empfänger-Refresh-Signalen an den Sender als Reaktion auf die Sender-Refresh-Signale;
Bestimmen, dass die Sender-Refresh-Signale durch den Empfänger für eine erste Zeitspanne nicht empfangen worden sind;
Wandeln von einem gültigen Empfängerdatensignal nach Bestimmen, dass die Sender-Refresh-Signale für die erste Zeitspan-

ne nicht empfangen worden sind, und Wandeln von einem gültigen Senderdatensignal nach Erfassen, dass die Empfänger-Refresh-Signale durch den Sender für eine zweite Zeitspanne nicht empfangen worden sind.

11. IC-Paket nach Anspruch 10, wobei das Diagnosemodul ferner dazu ausgestaltet ist, die Verfahrensschritte nach einem der Ansprüche 2 bis 9 auszuführen.

12. IC-Paket nach einem der Ansprüche 10 oder 11, wobei der Sender eine Sendertransistorbrücke (512) und eine Sendespule (534) im Übertragungspfad einschließt.

13. IC-Paket nach Anspruch 12, wobei der Empfänger ein Empfängersensorelement (524) einschließt, das mit der Sendespule gekoppelt ist.

14. IC-Paket nach Anspruch 13, wobei der Empfänger eine Empfängertransistorbrücke (520) und eine Empfängerspule (530) einschließt.

15. IC-Paket nach Anspruch 14, wobei der Sender ferner ein Sendersensorelement (516) einschließt, das mit der Empfängerspule gekoppelt ist.

Revendications

1. Procédé, comprenant :

l'emploi des première (102, 502, 602) et seconde (104, 504, 604) puces présentant une région de barrière de tension (108, 508) entre les première et seconde puces et dans lequel les chemins de transmission et de réception des première et seconde puces fournissent le transfert de données et le transfert bidirectionnel de rétroaction et/ou des signaux de diagnostic entre les première et seconde puces ; et

l'envoi, par un émetteur (114, 116, 512, 514) sur la première puce, des signaux de rafraîchissement de l'émetteur à un récepteur (130, 132, 524, 526) sur la seconde puce ;

l'envoi, par le récepteur, des signaux de rafraîchissement du récepteur à l'émetteur en réponse aux signaux de rafraîchissement de l'émetteur ;

la détermination que les signaux de rafraîchissement de l'émetteur n'ont pas été reçus par le récepteur pendant une première période de temps ;

le passage d'un signal valide de données du récepteur après avoir déterminé que les signaux de rafraîchissement de l'émetteur n'ont pas été reçus pendant la première période de temps et comprenant en outre la transition d'un signal valide de données de l'émetteur après avoir détecté que les signaux de rafraîchissement du récepteur n'ont pas été reçus par l'émetteur pendant une seconde.

2. Procédé selon la revendication 1, dans lequel l'état des passages du signal valide de données de l'émetteur lorsque l'émetteur présente un défaut.

3. Procédé selon la revendication 2, dans lequel le défaut comprend la perte de puissance.

4. Procédé selon la revendication 2, dans lequel l'état des passages du signal valide de données du récepteur lorsque le récepteur présente un défaut.

5. Procédé selon la revendication 1, dans lequel les intervalles entre les signaux de rafraîchissement de l'émetteur augmentent lorsque les signaux de rafraîchissement du récepteur n'ont pas été détectés par l'émetteur pendant une période de temps.

6. Procédé selon la revendication 1, dans lequel l'état des passages du signal valide de données de l'émetteur lorsque les signaux de rafraîchissement transmis ne sont pas reçus par le récepteur et le récepteur n'envoie pas de signaux de rafraîchissement du récepteur.

7. Procédé selon la revendication 6, comprenant en outre le passage d'un état du signal valide de données du récepteur lorsque les signaux de rafraîchissement de l'émetteur ne sont pas reçus par le récepteur pendant une certaine période de temps.

8. Procédé selon la revendication 1, comprenant en outre, après une défaillance de communication entre l'émetteur et le récepteur, le rétablissement de la transmission des signaux de rafraîchissement de l'émetteur et des signaux de rafraîchissement du récepteur.

9. Procédé selon la revendication 1, dans lequel les signaux de rafraîchissement transmis sont envoyés en l'absence de données à transférer.

10. Boîtier à circuits intégrés (CI) d'isolateur de signal, comprenant les étapes suivantes :

des première (102, 502, 602) et seconde (104, 504, 604) puces présentant une région de barrière de tension (108, 508) entre les première et seconde puces et dans lequel les voies de transmission et de réception des première et seconde puces fournissent le transfert de données bidirectionnel entre les première et seconde puces ;

et
un module de diagnostic configuré pour :

envoyer, par un émetteur (114, 116, 512, 514) sur la première puce, des signaux de rafraîchissement de l'émetteur à un récepteur (130, 132, 524, 526) sur la seconde puce ;
envoyer, par le récepteur, des signaux de rafraîchissement du récepteur à l'émetteur en réponse aux signaux de rafraîchissement de l'émetteur ;
déterminer que les signaux de rafraîchissement de l'émetteur n'ont pas été reçus par le récepteur pendant une première période de temps ;
passer un signal valide de données du récepteur après avoir déterminé que les signaux de rafraîchissement de l'émetteur n'ont pas été reçus pendant la première période de temps et passer un signal valide de données de l'émetteur après avoir détecté que les signaux de rafraîchissement du récepteur n'ont pas été reçus par l'émetteur

11. Boîtier à CI selon la revendication 10, dans lequel le module de diagnostic est configuré en outre pour effectuer les étapes du procédé de l'une quelconque des revendications 2 à 9.

12. Boîtier à CI selon la revendication 10 ou 11, dans lequel l'émetteur comprend un pont de transistors d'émetteur (512) et une bobine d'émetteur (534) dans le chemin de transmission.

13. Boîtier à CI selon la revendication 12, dans lequel le récepteur comprend un élément de détection de récepteur (524) couplé avec la bobine d'émetteur.

14. Boîtier à CI selon la revendication 13, dans lequel le récepteur comprend un pont de transistors de récepteur (520) et une bobine de récepteur (530).

15. Boîtier à CI selon la revendication 14, dans lequel l'émetteur comprend en outre un élément de détection d'émetteur (516) couplé à la bobine de récepteur, pendant une seconde période de temps.

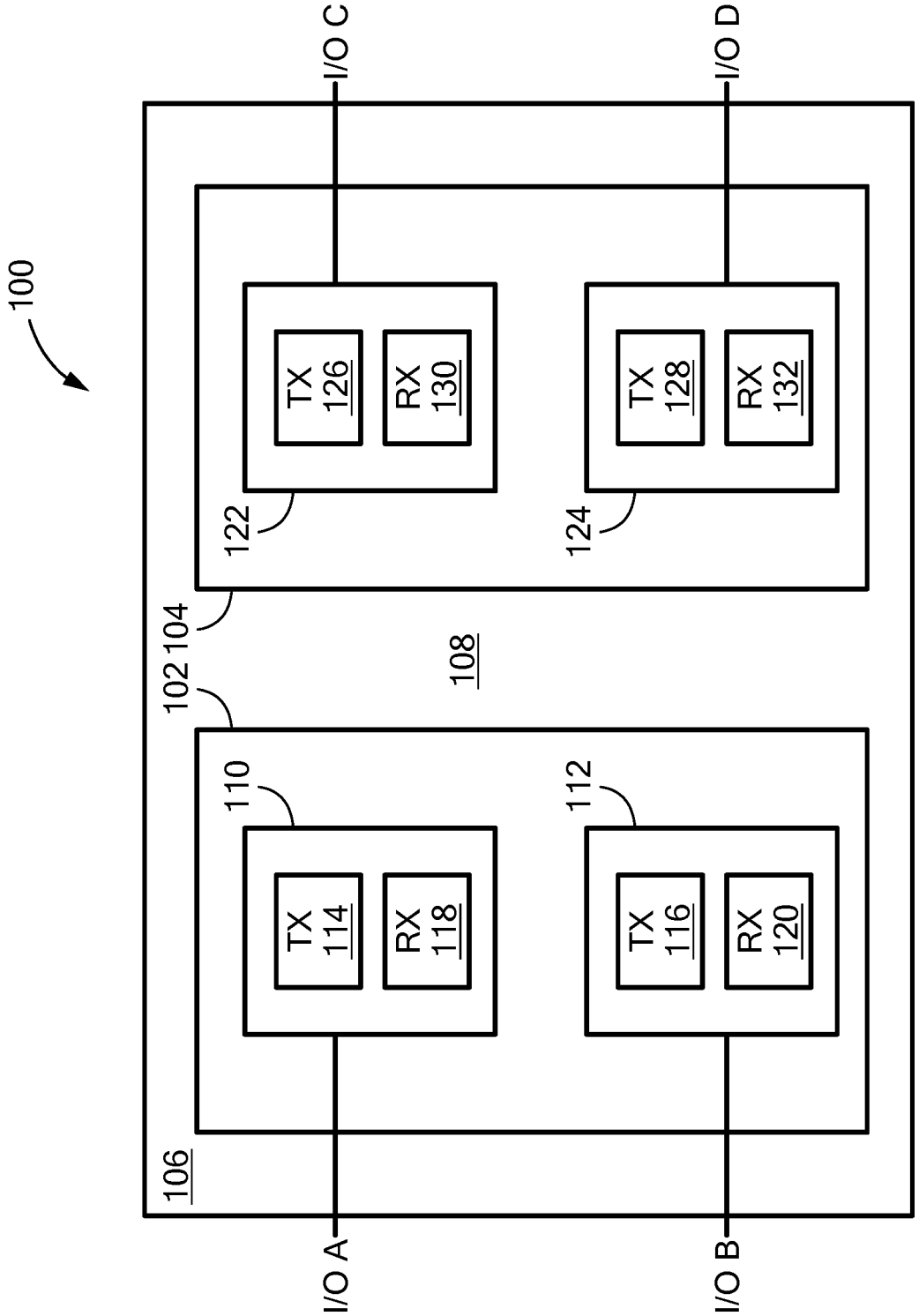
100
I/O C
I/O D
TX 126
RX 130
TX 128
RX 132
122
124
102 104
108
110
112
TX 114
RX 118
TX 116
RX 120
106
I/O A
I/O B

FIG. 1

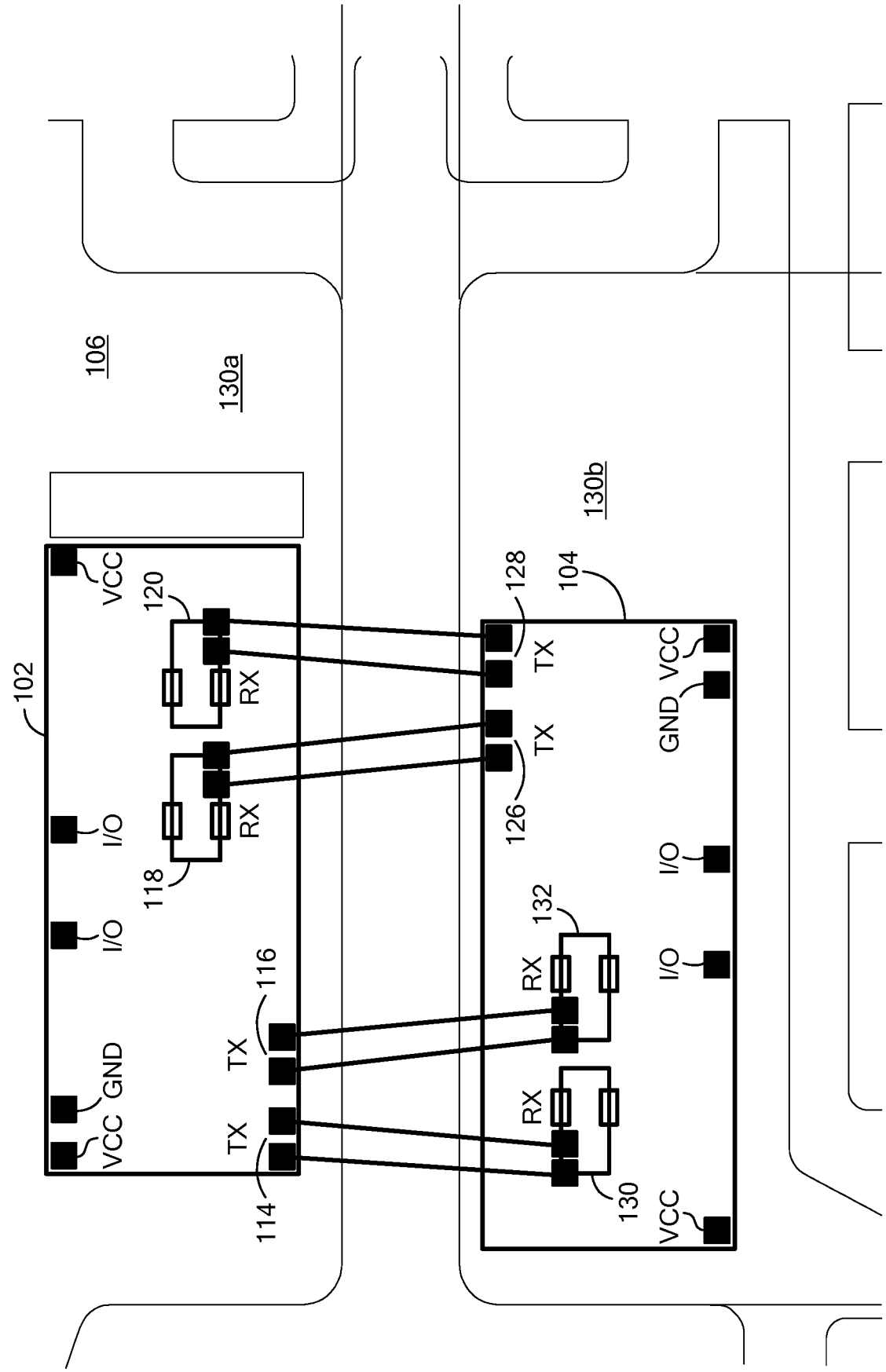
106
130a
130b
102
104
VCC
120
RX
I/O
118
128
TX
126
GND
116
114
132
130

FIG. 2

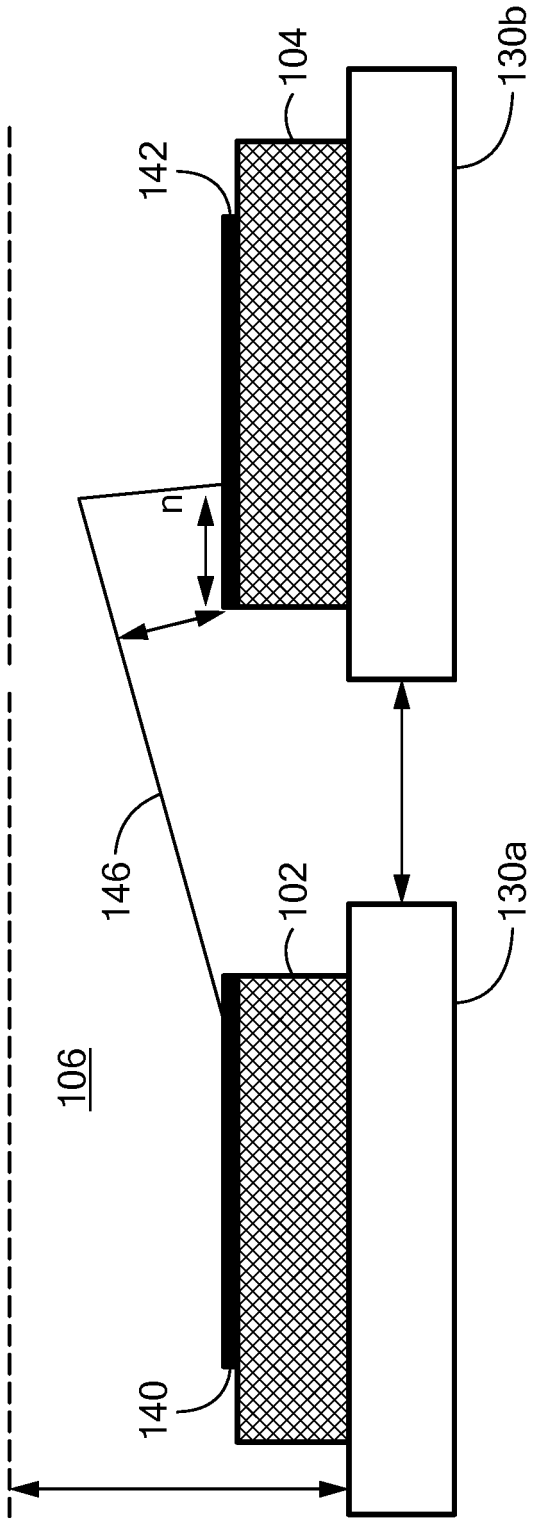

FIG. 3

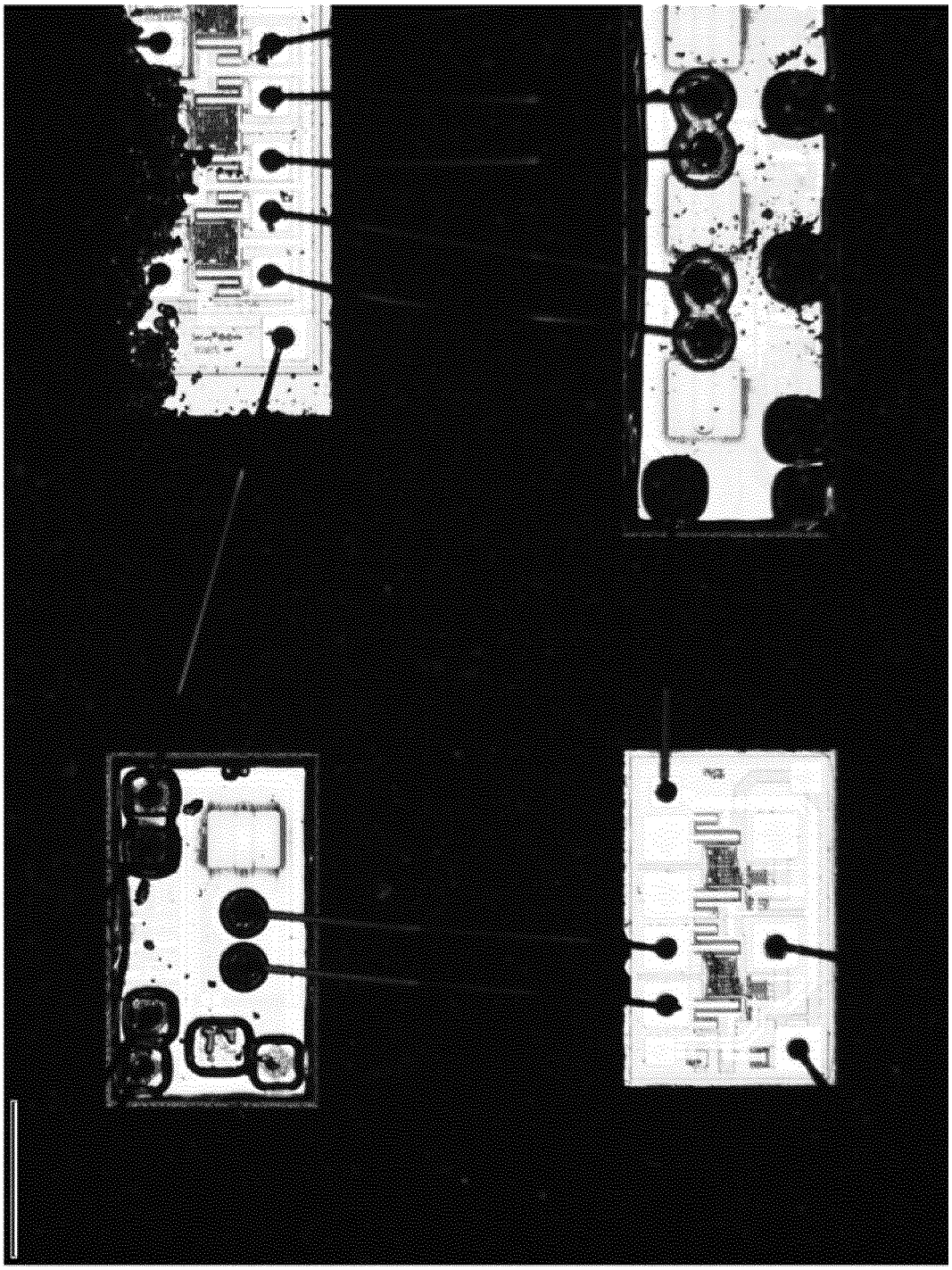

FIG. 4
PRIOR ART

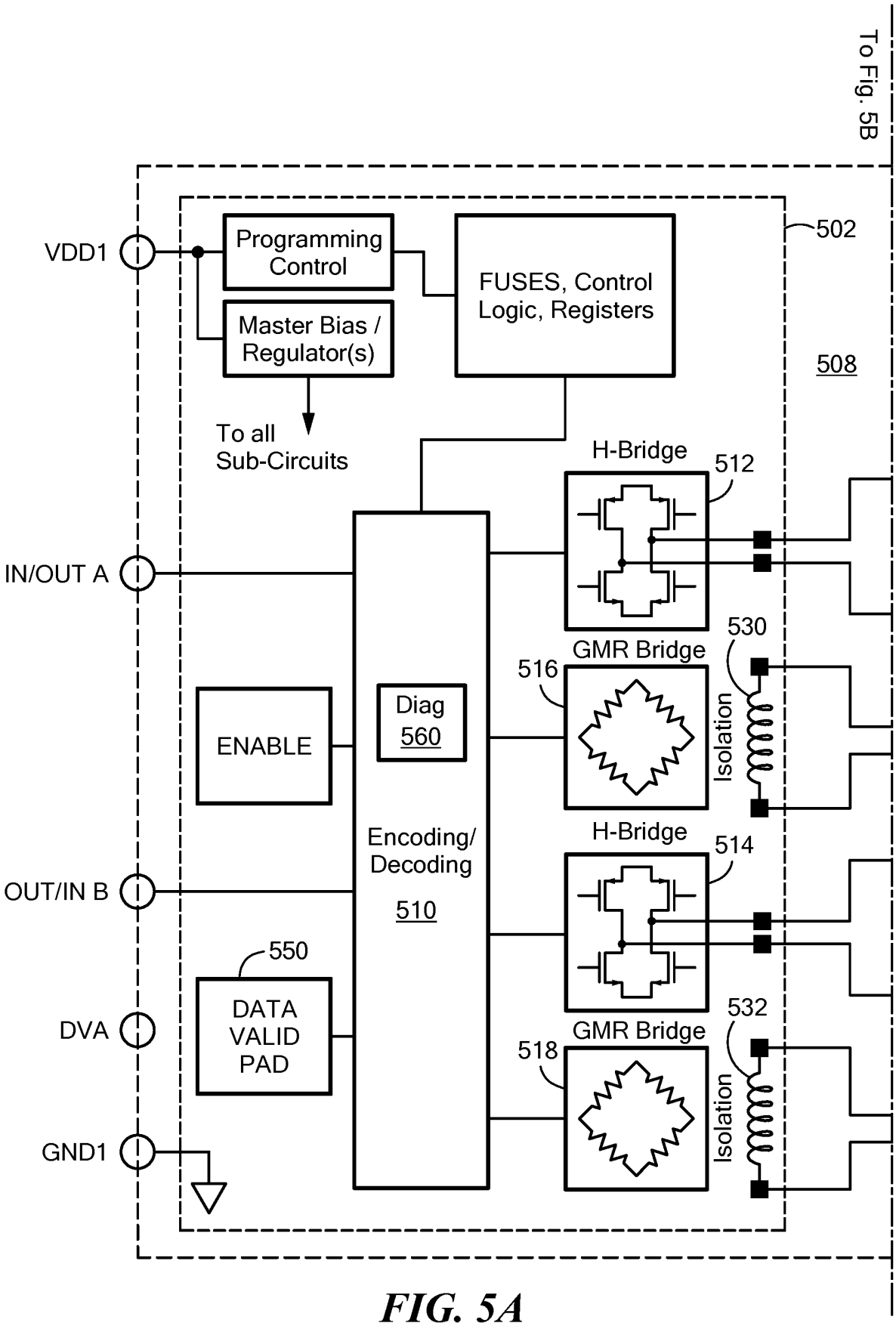
To Fig. 5B
VDD1
Programming Control
Master Bias / Regulator(s)
FUSES, Control Logic, Registers
502
508
To all Sub-Circuits
H-Bridge
512
IN/OUT A
GMR Bridge
530
516
ENABLE
Diag 560
Isolation
Encoding/ Decoding 510
H-Bridge
514
OUT/IN B
550
DATA VALID PAD
DVA
GMR Bridge
532
518
Isolation
GND1

FIG. 5A

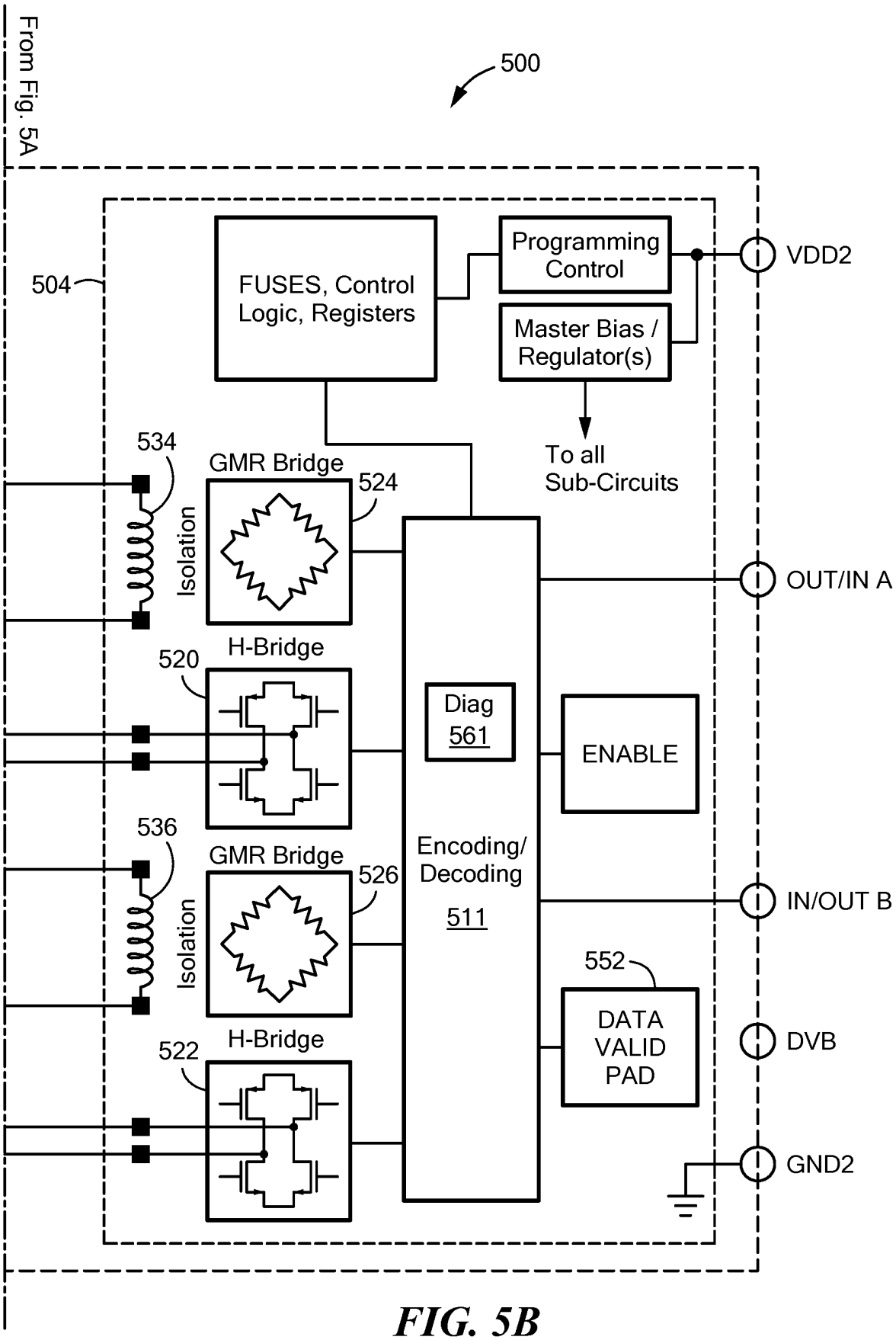
From Fig. 5A
500
504
FUSES, Control Logic, Registers
Programming Control
Master Bias / Regulator(s)
VDD2
To all Sub-Circuits
534
GMR Bridge
524
Isolation
OUT/IN A
520
H-Bridge
Diag 561
ENABLE
536
GMR Bridge
526
Encoding/ Decoding 511
IN/OUT B
552
DATA VALID PAD
DVB
522
H-Bridge
GND2

FIG. 5B

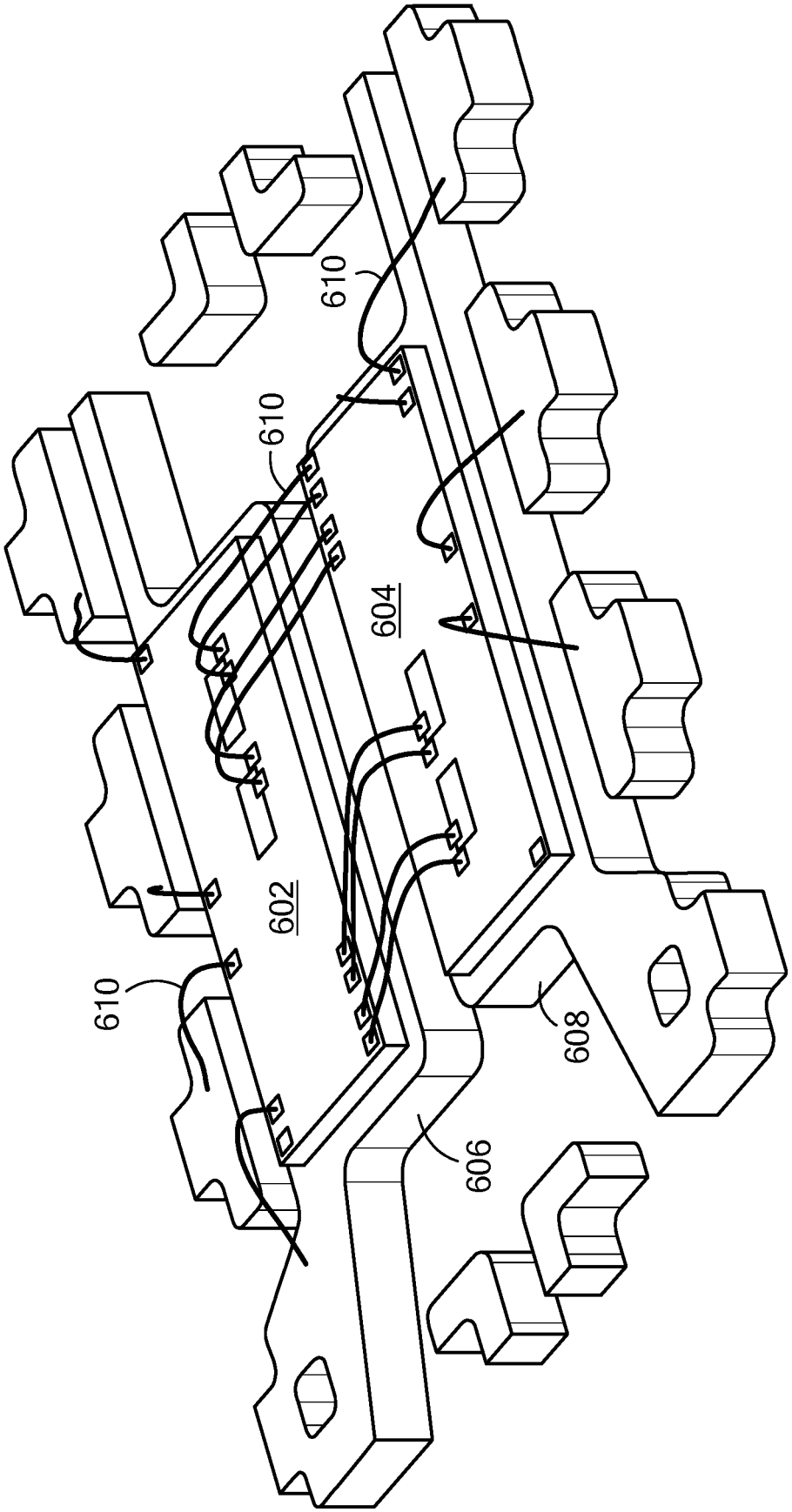

FIG. 6

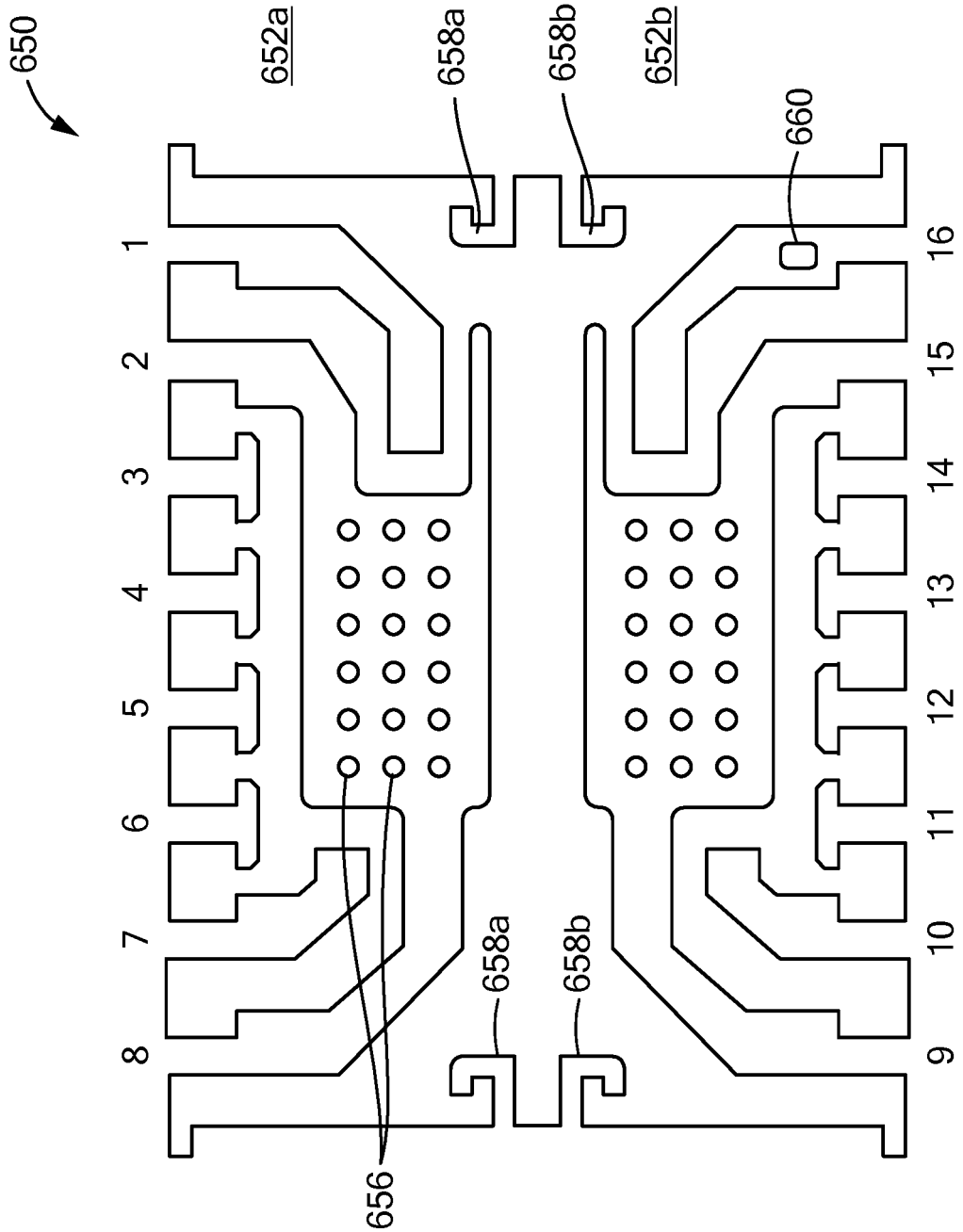
650
652a
658a
658b
652b
660
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
658a
658b
656

FIG. 6A

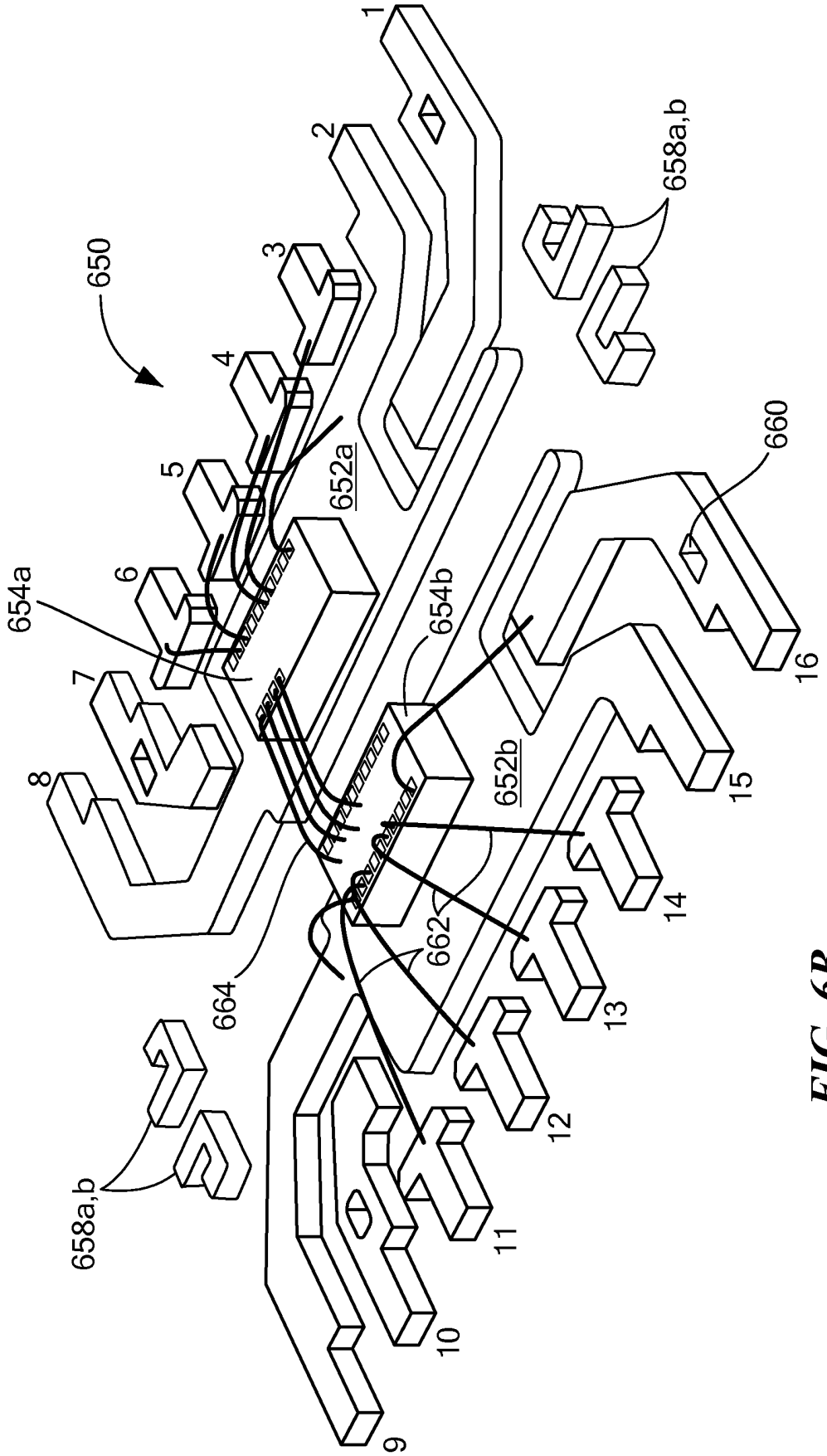
650
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
652a
652b
654a
654b
658a,b
658a,b
660
662
664

FIG. 6B

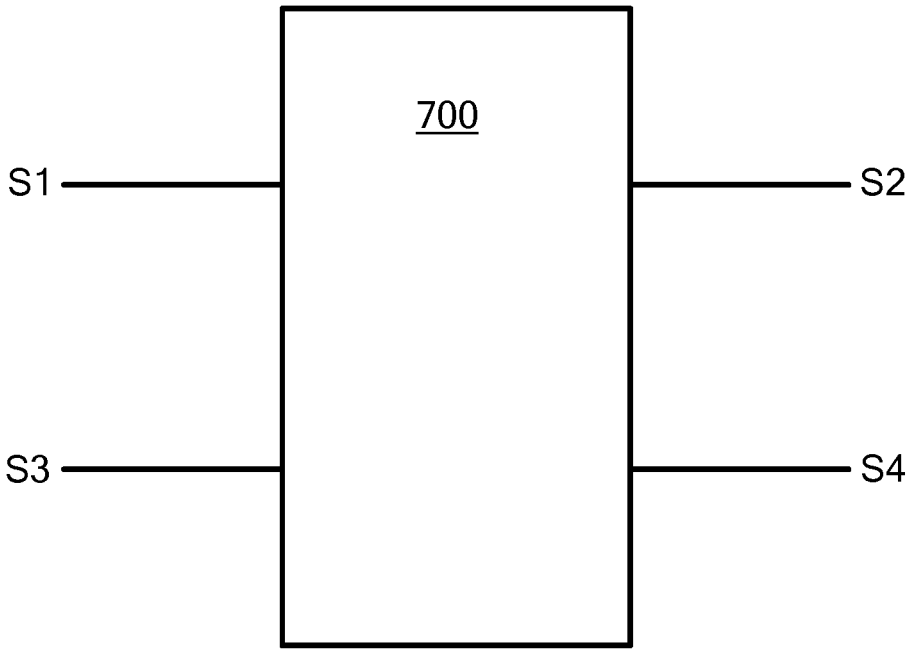

FIG. 7

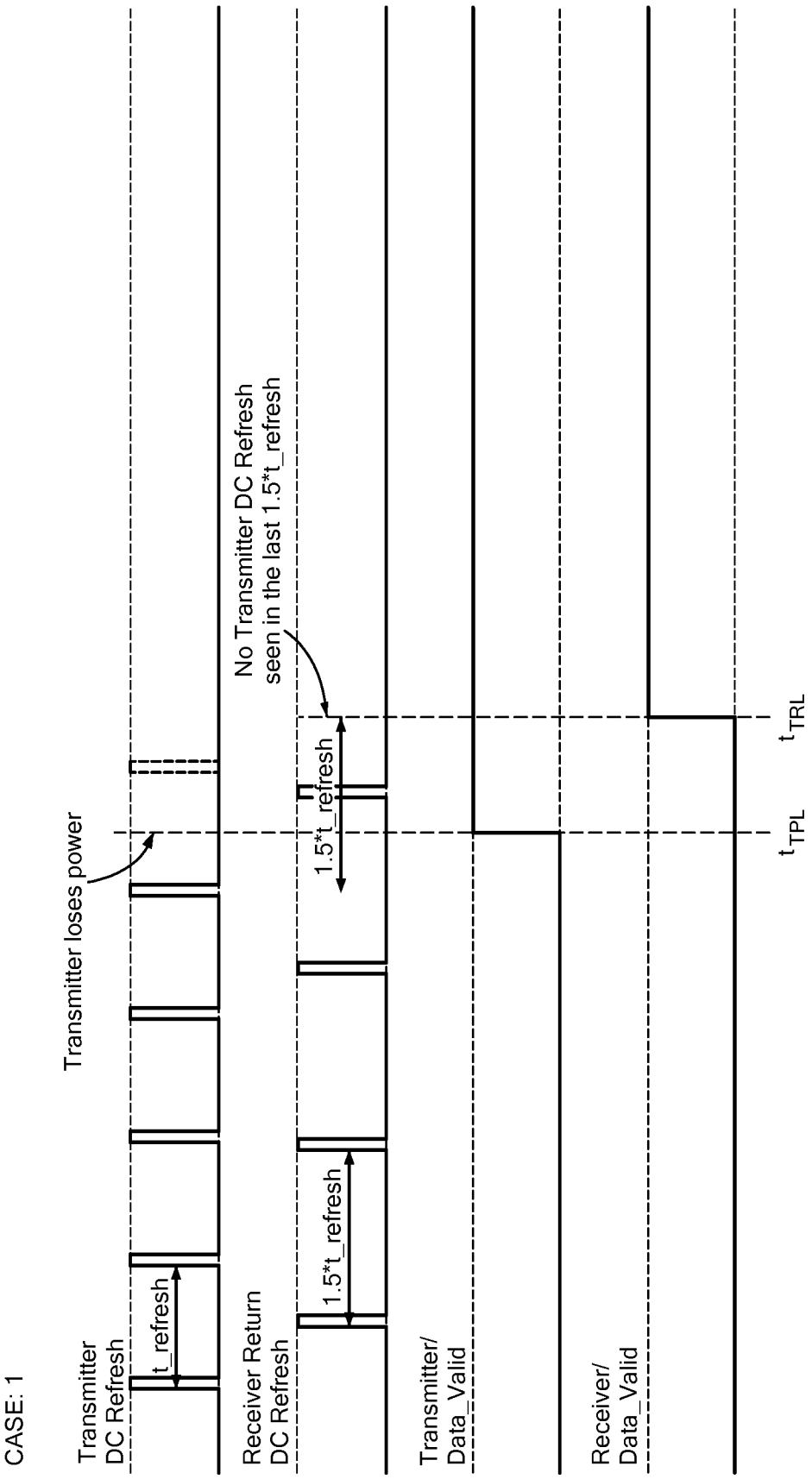
CASE: 1
Transmitter DC Refresh
t_refresh
Receiver Return DC Refresh
1.5*t_refresh
Transmitter loses power
No Transmitter DC Refresh seen in the last 1.5*t_refresh
1.5*t_refresh
Transmitter/ Data_Valid
Receiver/ Data_Valid
t_{TPL}
t_{TRL}

FIG. 8A

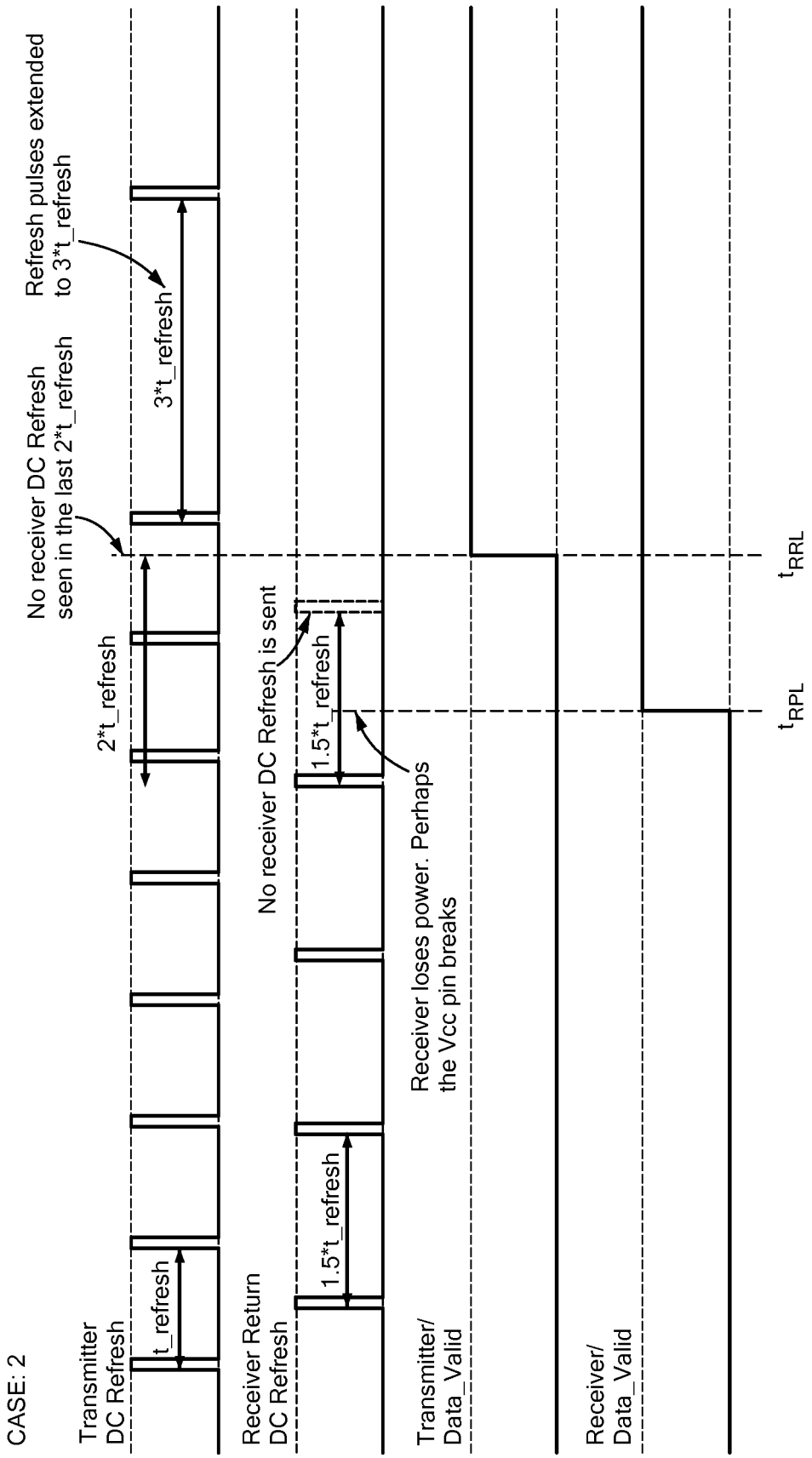
CASE: 2
Transmitter DC Refresh
t_refresh
Receiver Return DC Refresh
1.5*t_refresh
Transmitter/ Data_Valid
Receiver/ Data_Valid
No receiver DC Refresh seen in the last 2*t_refresh
2*t_refresh
Refresh pulses extended to 3*t_refresh
3*t_refresh
No receiver DC Refresh is sent
1.5*t_refresh
Receiver loses power. Perhaps the Vcc pin breaks
tRRL
tRPL

FIG. 8B

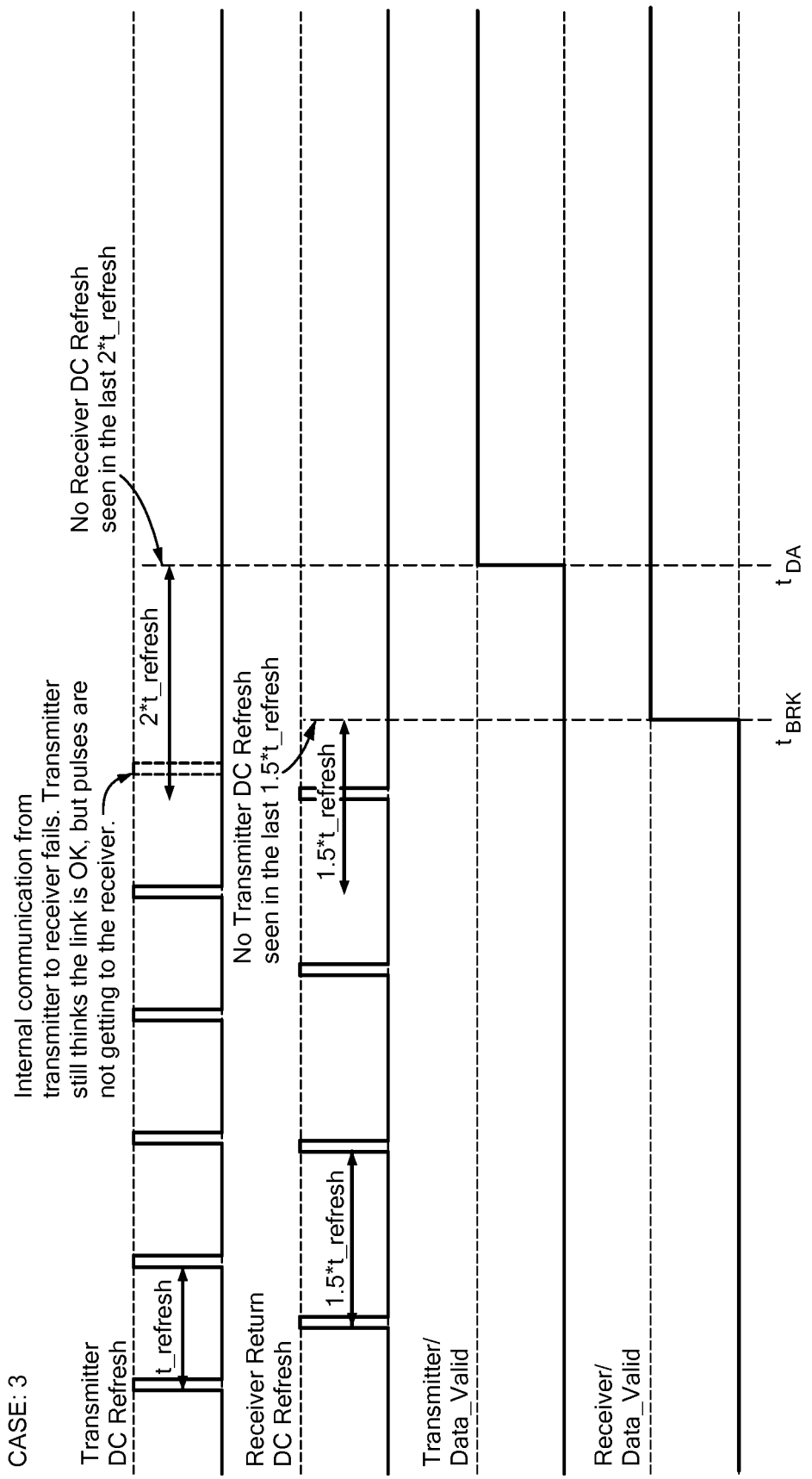
CASE: 3
Transmitter DC Refresh
t_refresh
Internal communication from transmitter to receiver fails. Transmitter still thinks the link is OK, but pulses are not getting to the receiver.
2*t_refresh
No Receiver DC Refresh seen in the last 2*t_refresh
Receiver Return DC Refresh
1.5*t_refresh
No Transmitter DC Refresh seen in the last 1.5*t_refresh
1.5*t_refresh
Transmitter/ Data_Valid
Receiver/ Data_Valid
t DA
t BRK

FIG. 8C

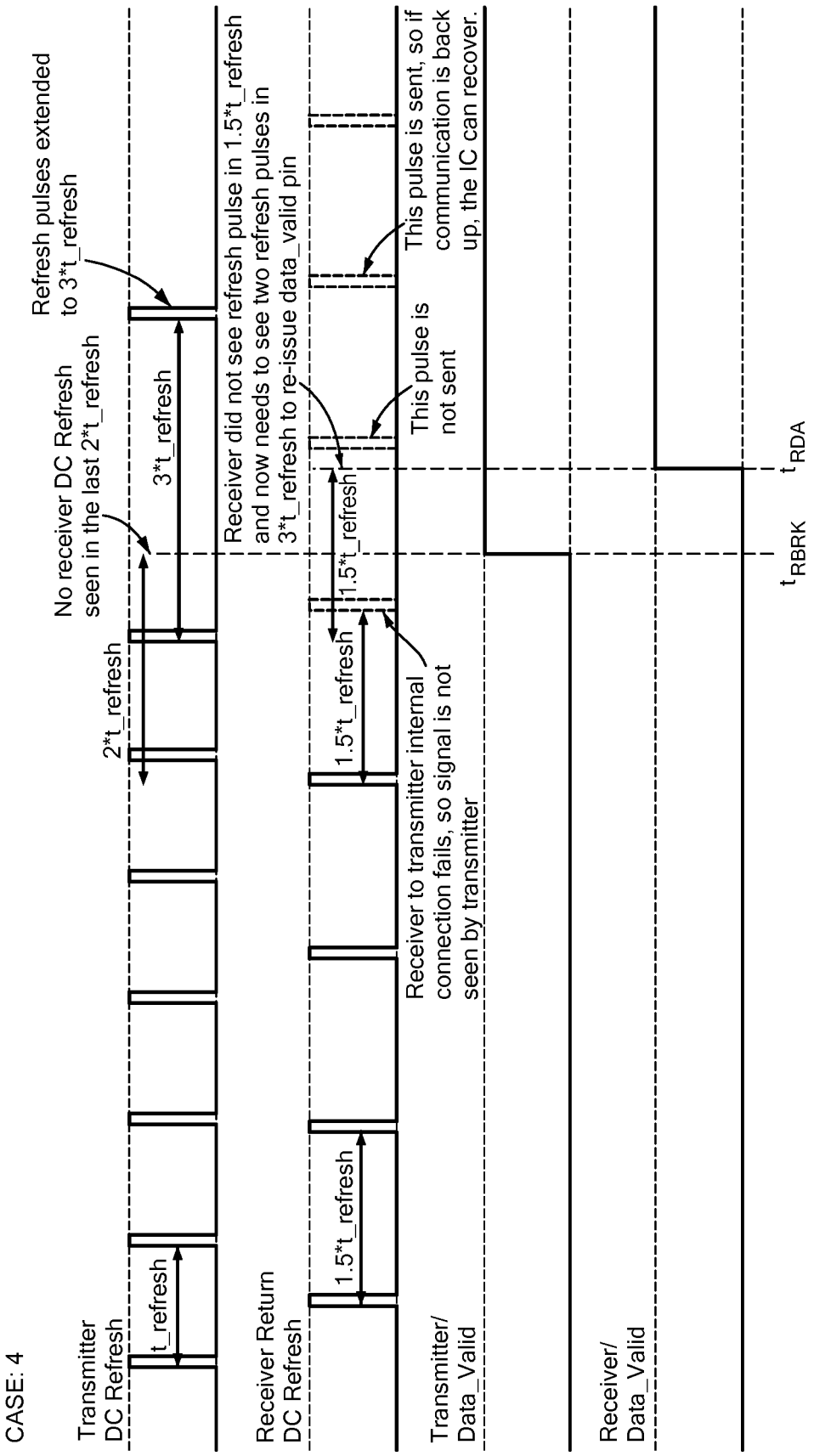
CASE: 4
Transmitter DC Refresh
t_refresh
2*t_refresh
3*t_refresh
No receiver DC Refresh seen in the last 2*t_refresh
Refresh pulses extended to 3*t_refresh
Receiver Return DC Refresh
1.5*t_refresh
1.5*t_refresh
1.5*t_refresh
Receiver did not see refresh pulse in 1.5*t_refresh and now needs to see two refresh pulses in 3*t_refresh to re-issue data_valid pin
This pulse is not sent
This pulse is sent, so if communication is back up, the IC can recover.
Transmitter/ Data_Valid
Receiver to transmitter internal connection fails, so signal is not seen by transmitter
Receiver/ Data_Valid
t_{RBRK}
t_{RDA}

FIG. 8D

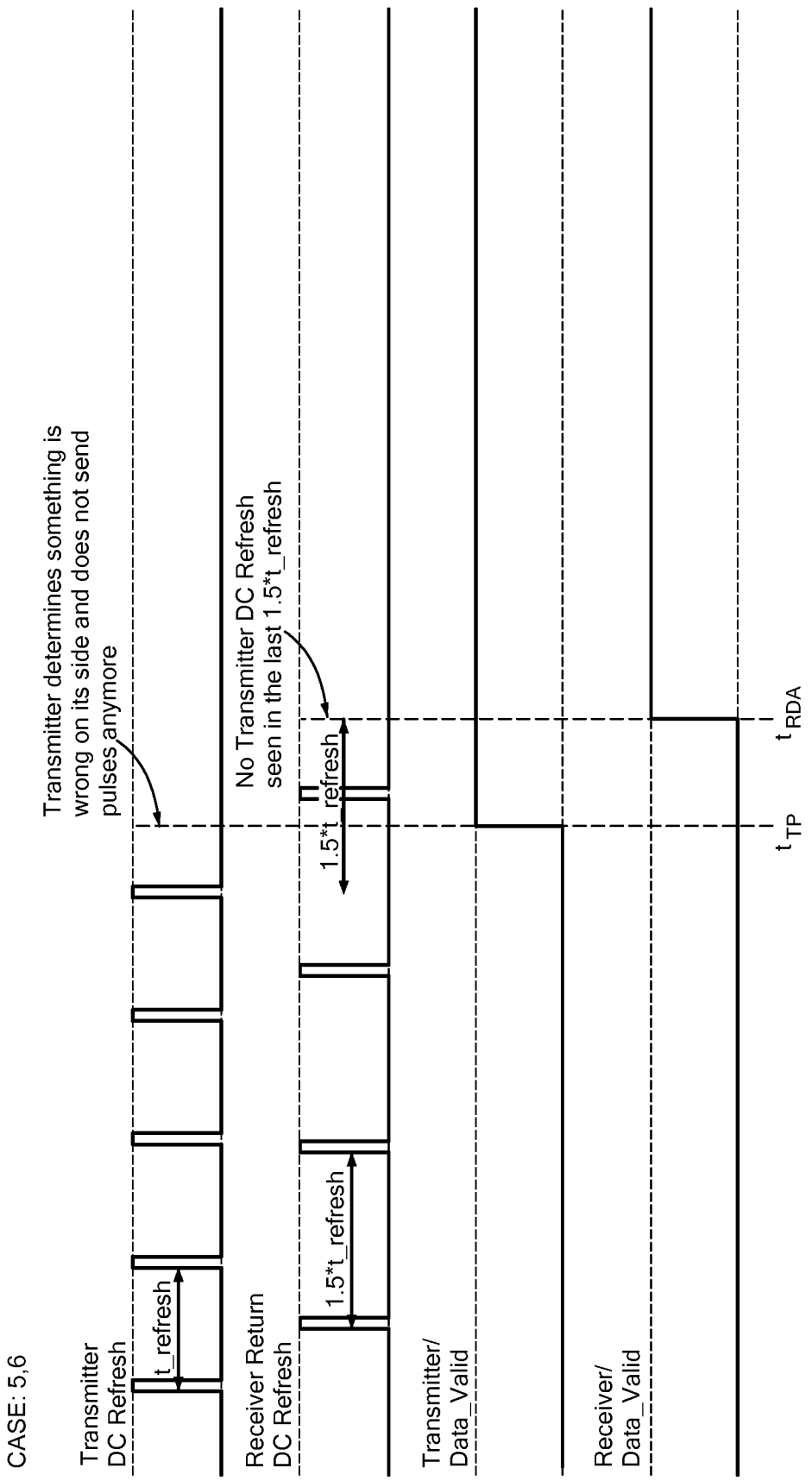
CASE: 5,6
Transmitter DC Refresh
t_refresh
Transmitter determines something is wrong on its side and does not send pulses anymore
Receiver Return DC Refresh
1.5*t_refresh
No Transmitter DC Refresh seen in the last 1.5*t_refresh
1.5*t_refresh
Transmitter/ Data_Valid
Receiver/ Data_Valid
t TP
t RDA

FIG. 8E

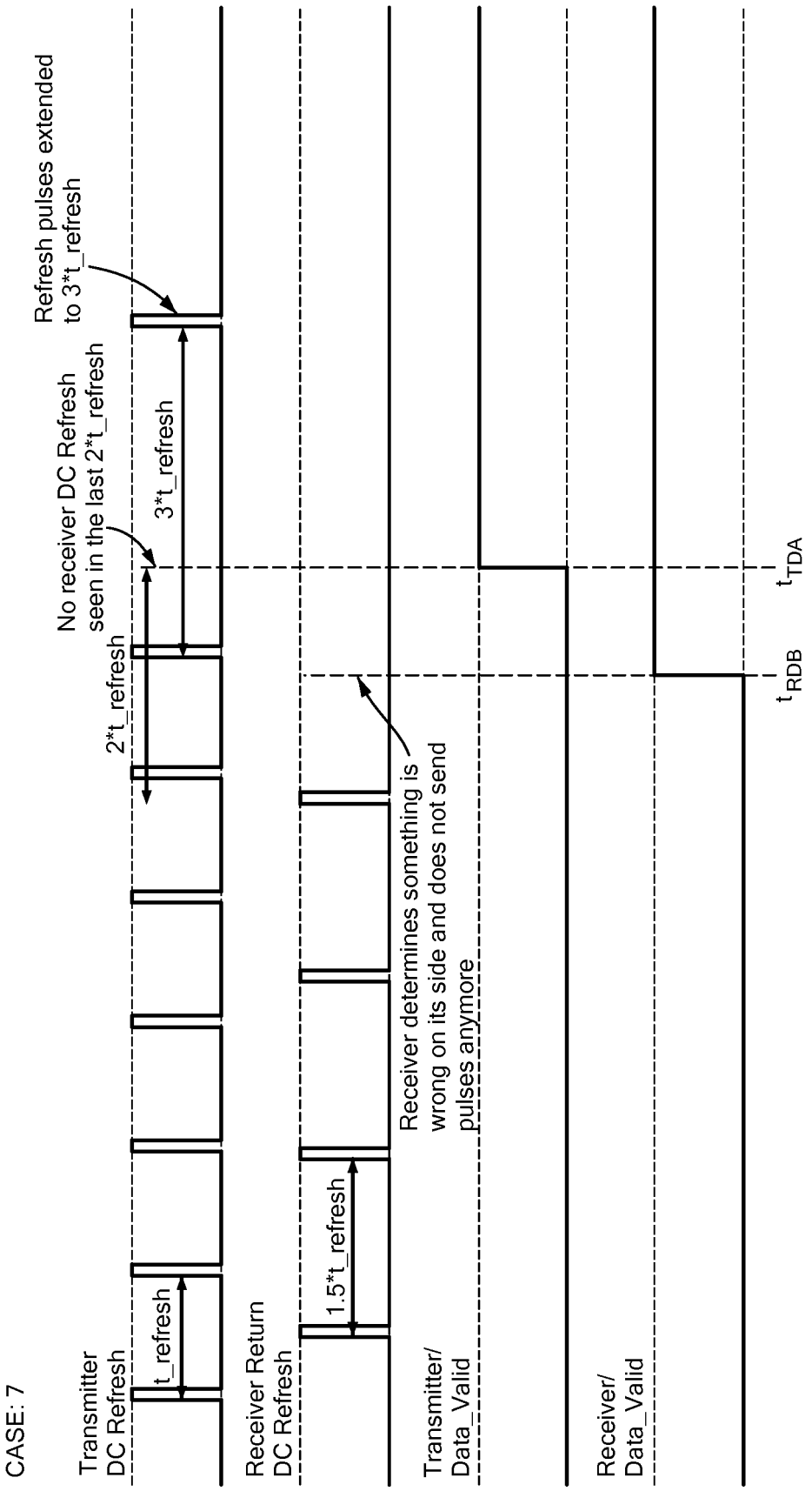
CASE: 7
Transmitter DC Refresh
t_refresh
Receiver Return DC Refresh
1.5*t_refresh
Transmitter/ Data_Valid
Receiver/ Data_Valid
2*t_refresh
3*t_refresh
No receiver DC Refresh seen in the last 2*t_refresh
Refresh pulses extended to 3*t_refresh
Receiver determines something is wrong on its side and does not send pulses anymore
t_RDB
t_TDA

FIG. 8F

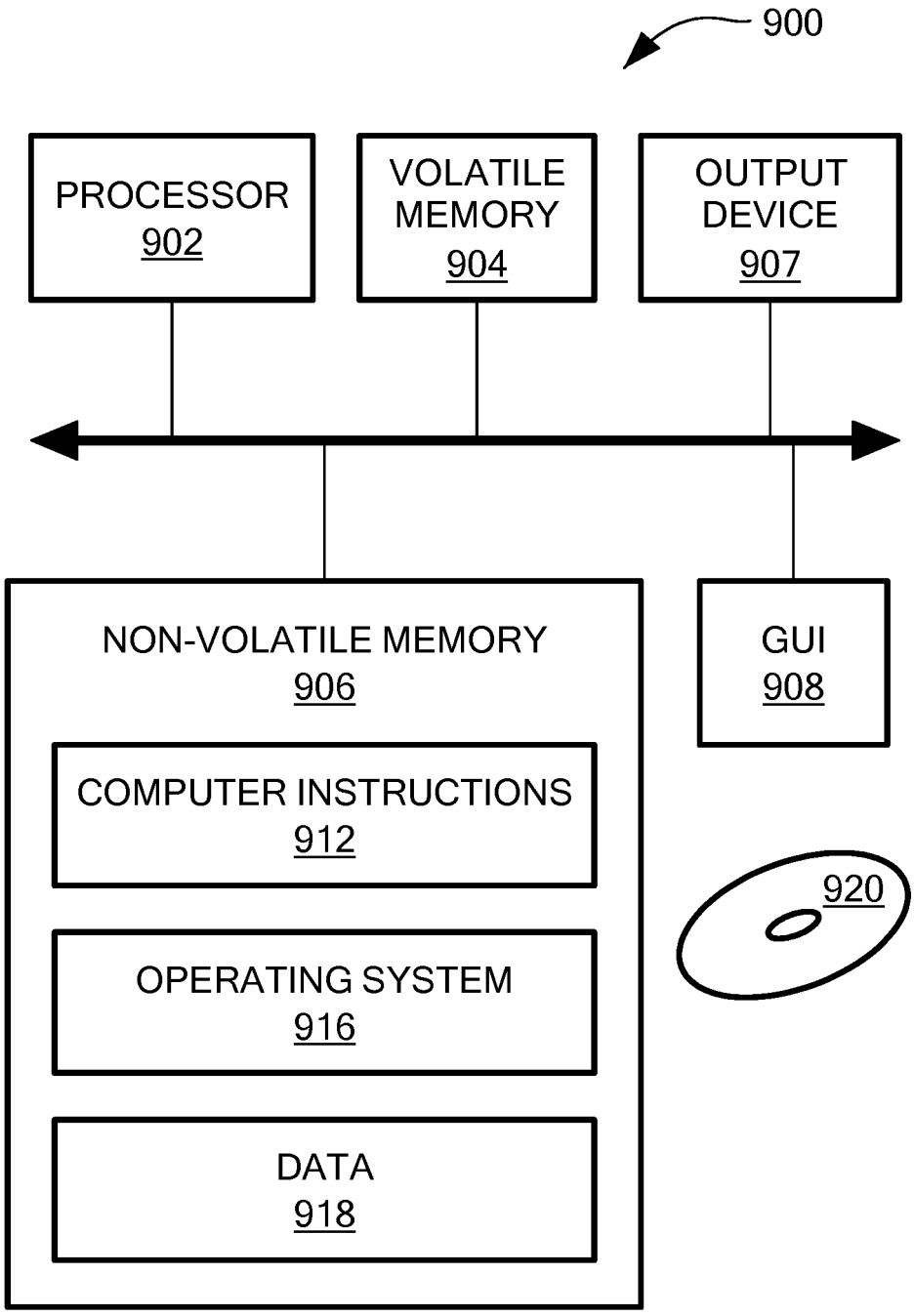
900
PROCESSOR
902
VOLATILE
MEMORY
904
OUTPUT
DEVICE
907
NON-VOLATILE MEMORY
906
COMPUTER INSTRUCTIONS
912
OPERATING SYSTEM
916
DATA
918
GUI
908
920

FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2014266332 A1 **[0002]**
- US 2012508820 A1 **[0003]**