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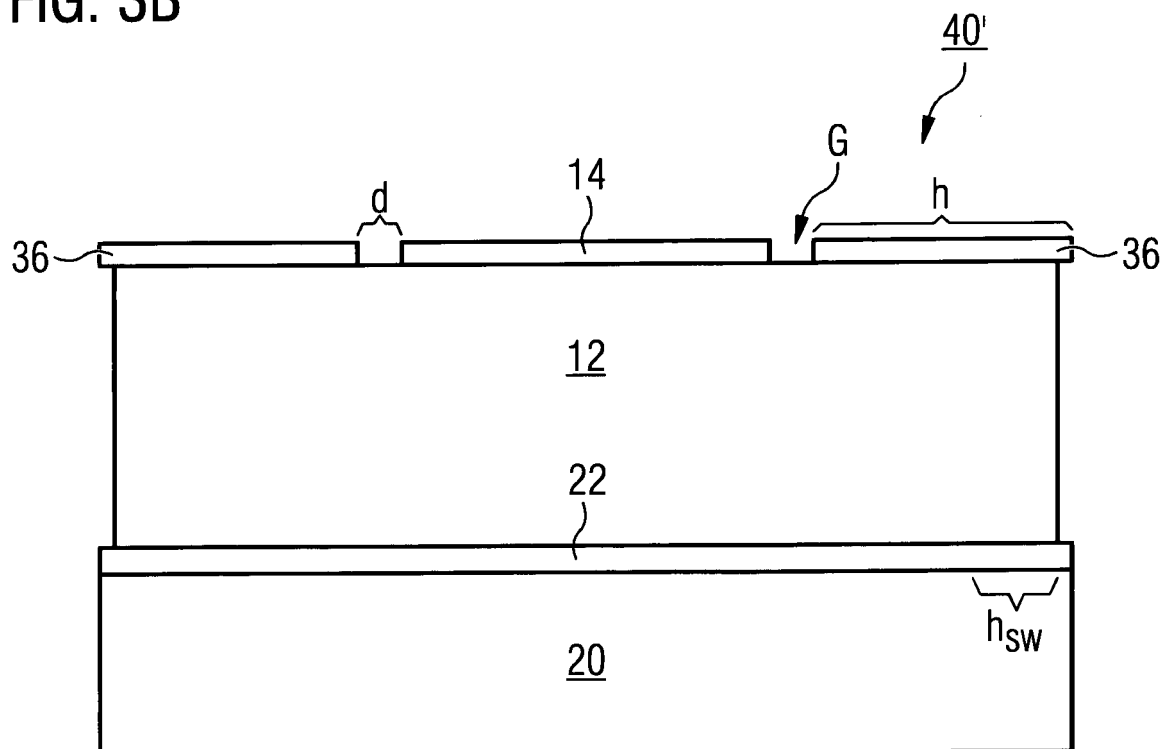
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(54) **PATCH ANTENNA ELEMENT AND METHOD FOR MANUFACTURING A PATCH ANTENNA ELEMENT**

(57) The present disclosure relates to a patch antenna element comprising a substrate (12; 20), patch (14; 26) disposed on the substrate, a ground plane (22) disposed on the substrate below the patch, wherein the

ground plane horizontally extends beyond the patch and a conductive planar arrangement (24; 36; 36') at least partially laterally surrounding the patch.

**FIG. 3B**



<b>Description</b>	Fig. 3B	shows a side view of a patch antenna element without cavity according to an example;
<b>Field</b>	Fig. 4A	shows a side view of a cavity backed patch antenna element according to a further example;
<b>[0001]</b> The present disclosure relates to antennas for telecommunications and, more particularly, to patch antennas, which, for example, can be used in antenna arrays for wireless communication systems.	5 Fig. 4B	shows a side view of a patch antenna element without cavity according to an example;
<b>Background</b>	10 Fig. 5A	shows a side view of a cavity backed patch antenna element according to a further example;
<b>[0002]</b> A patch antenna is a type of radio antenna with a low profile, which can be mounted on a flat surface. It comprises a flat sheet or "patch" of metal, mounted over a larger sheet of metal called a ground plane. Note that the patch can be of many shapes, such as rectangular, circular, triangular, etc. The two metal sheets together form a resonant piece which can be thought of a microstrip transmission line with a length of approximately half a wavelength. The radiation mechanism arises from discontinuities at each truncated edge of the microstrip transmission line. Patch antennas are commonly used in telecommunication devices because they can be extremely compact. However, one issue of conventional patch antennas is their relatively narrow bandwidth.	Fig. 5B 15 Fig. 6A	shows a side view of a patch antenna element without cavity according to an example; shows a side view of a cavity backed patch antenna element according to yet a further example;
<b>[0003]</b> Multiple-Input Multiple-Output (MIMO) could be integrated in the upcoming standard of "5G". In order to benefit from the MIMO technique, the channel matrix has to fulfill some requirements, whereas one of them is that the component channels are uncorrelated. An advantageous way to get two uncorrelated channels in the mm-wave region (i.e., the wavelength is in the mm region) is to use dual polarized patch antennas since through dual polarization these antennas need less space than single polarized antennas (when all other antenna requirements stay the same, e.g. realized gain). A disadvantage of introducing a second polarization is that the patch antenna design loses a parameter to tune (e.g., the parameter "patch-width" for a simple patch antenna) which makes it harder to fulfill the ambitious bandwidth requirements in the mm-wave range (~10% relative bandwidth).	20 Fig. 6B Fig. 7 Fig. 8 25	shows a side view of a patch antenna element without cavity according to an example; show side views of a conventional stacked patch antenna element; show side views of a stacked patch antenna element according to an example implementation;
<b>[0004]</b> Thus it is desirable to improve existing patch antenna designs with respect to achievable bandwidth.	Fig. 9A, B 30 Fig. 10A, B Fig. 11A, B 35	show perspective views of an enhanced cavity backed stacked patch antenna element according to an example implementation; illustrate a bandwidth of a conventional patch antenna element; illustrate a bandwidth of an enhanced cavity backed stacked patch antenna element according to an example implementation;
<b>Brief description of the Figures</b>	FIG. 11C 40 Fig. 12A, B Fig. 13A 45	compares the radiation efficiency and total efficiency of conventional and enhanced antenna structures illustrate bandwidths of different enhanced cavity backed stacked patch antenna designs according to different examples; illustrates a flowchart of a manufacturing method for an enhanced cavity backed stacked patch antenna designs according to the present disclosure;
<b>[0005]</b> Some examples of apparatuses and/or methods will be described in the following by way of example only, and with reference to the accompanying figures, in which	Fig. 13B 50	illustrates a flowchart of a manufacturing method for an enhanced patch antenna designs according to the present disclosure;
Figs. 1A, B	Fig. 14	shown a patch antenna array comprising four enhanced cavity backed stacked patch antenna elements according to the present disclosure; and
Figs. 2A, B	55 Fig. 15	shows a mobile device implementing examples of the present disclosure.
Fig. 3A		

## Detailed Description

**[0006]** Various examples will now be described more fully with reference to the accompanying drawings in which some examples are illustrated. In the figures, the thicknesses of lines, layers and/or regions may be exaggerated for clarity.

**[0007]** Accordingly, while further examples are capable of various modifications and alternative forms, some particular examples thereof are shown in the figures and will subsequently be described in detail. However, this detailed description does not limit further examples to the particular forms described. Further examples may cover all modifications, equivalents, and alternatives falling within the scope of the disclosure. Like numbers refer to like or similar elements throughout the description of the figures, which may be implemented identically or in modified form when compared to one another while providing for the same or a similar functionality.

**[0008]** It will be understood that when an element is referred to as being "connected" or "coupled" to another element, the elements may be directly connected or coupled or via one or more intervening elements. If two elements A and B are combined using an "or", this is to be understood to disclose all possible combinations, i.e. only A, only B as well as A and B. An alternative wording for the same combinations is "at least one of A and B". The same applies for combinations of more than 2 Elements.

**[0009]** The terminology used herein for the purpose of describing particular examples is not intended to be limiting for further examples. Whenever a singular form such as "a," "an" and "the" is used and using only a single element is neither explicitly or implicitly defined as being mandatory, further examples may also use plural elements to implement the same functionality. Likewise, when a functionality is subsequently described as being implemented using multiple elements, further examples may implement the same functionality using a single element or processing entity. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including," when used, specify the presence of the stated features, integers, steps, operations, processes, acts, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, processes, acts, elements, components and/or any group thereof.

**[0010]** Unless otherwise defined, all terms (including technical and scientific terms) are used herein in their ordinary meaning of the art to which the examples belong. Note that terms such as vertical and horizontal as used in this specification are merely relative terms and do not signify a particular orientation relative to the earth or anything else. Rather, the term "horizontal" or "horizontal direction" generally refers to the direction parallel to a patch plane defined by a large (e.g. square) surface of the patch and the term "vertical" or "vertical direction" generally refers to the direction perpendicular to the large surface of the patch.

**[0011]** FIGS. 1A and 1B are top and side views of a patch antenna element 10.

**[0012]** Patch antenna element 10 comprises a dielectric substrate 12 (for example, Bakelite, FR4 Glass Epoxy, RO4003, Taconic TLC or RT Duroid) bearing a metal patch 14 on the top surface thereof, wherein patch 14 has length  $l$  and width  $w$ . The length  $l$  of patch 14 typically is selected to be  $\frac{1}{2}$  of the wavelength  $\lambda$  of the signal that patch 14 is intended to radiate (or receive), so that patch 14 resonates at the frequency of the signal and thereby transmits the desired wireless signal. The "length" of a patch antenna generally refers to the distance between the radiating edges of the patch. Thus, for example, in a square patch, this would be the length of a side of the square. For a circular patch, this would be the diameter of the patch. For a rectangular patch, it would be the orthogonal distance between the two radiating edges of the patch (which could be either the short or the long edges depending on the design).

**[0013]** In the example of FIGS. 1A and 1B, metal patch 14 is peripherally surrounded by a frame structure 16, which will also be referred to as top ground plane. Metal patch 14 is separated from top ground plane 16 by gap G. Top ground plane 16 can be implemented in the same metal layer as metal patch 14. Patch 14 and top ground plane 16 may be created by conventional manufacturing techniques such as depositing one or more metal layers on the substrate 12 by any of a number of techniques known in semiconductor fabrication industry and etching them by any of a number of techniques known in the semiconductor fabrication industry to create the two distinct metallizations, i.e., the top ground plane 16 and the patch 14.

**[0014]** A feed line 18 may be etched on the opposite side of the substrate 12 or could be etched on a second substrate 20 disposed below the first substrate 12 and bonded thereto. Feed line 18 is coupled to a drive signal (not shown). In the illustrated example, feedline 18 is directly coupled to patch 14 by a feedline via (vertical interconnect access) 18'. In other examples, via 18' could also be omitted so that feed line 18 capacitively drives a signal on patch 14. The feed line of a patch antenna may be coupled directly to the patch in order to directly drive (or receive) the signal. However, a patch antenna also may be excited using a proximity coupled feed line. Particularly, the feed line, whether it is a microstrip or a stripline, may be electrically separated from patch 14 by a dielectric material, including air, and may drive (or receive) the waves on the patch capacitively.

**[0015]** In the illustrated example, another dielectric substrate 20 is disposed below feed line 18. Feed line 18 alternately may be deposited on the top surface of the second substrate 20, rather than the bottom surface of the first substrate 12. A bottom ground plane 22 is deposited on the bottom of the second substrate 20. Side walls 24 through the substrates 12 and 20 conductively connect the top ground plane 16 to the bottom ground plane 22. Side walls 24 may be implemented using plated

through vias, for example. Note that feed line 18 alternately could also be deposited below bottom ground plane 22 for better isolating it from patch 14. For more than one antenna polarization, more than one feed line and/or feed points may be provided to drive patch 14.

**[0016]** In the illustrated example, vias 24 electrically couple the top and bottom ground planes 16 and 22 to each other and thus form a shielded cavity around the patch 14. Thus, vias 24 may also be regarded as vertically extending side walls of the cavity laterally surrounding patch 14. This helps to minimize coupling between adjacent patch antenna elements in an array of patch antenna elements. Particularly, patch antennas elements of this type may be arranged in arrays of hundreds or even thousands of patch antennas elements. More particularly, multiple patch antennas elements may be fabricated on large substrates, such as substrates 12 and 20, that contain multiple patch antenna elements. The fields surrounding the vias help isolate the patch antenna elements from each other.

**[0017]** As previously noted, patch antennas of this type tend to have relatively narrow bandwidth and, therefore, have somewhat limited applications. Within limits, the bandwidth of the antenna can be increased by increasing the volume of the antenna. The volume generally can be understood as the space between the two ground planes 16, 22 and the side walls 24, generally called the cavity of the antenna. For this reason, the antenna structure of Figs. 1A and 1B is also sometimes referred to as "cavity backed patch antenna". The bandwidth of a cavity backed patch antenna can be increased by decreasing the substrate's 12, 22 permittivity and/or by increasing the distance between the patch 14 and the bottom ground plane 22, i.e., by increasing the vertical dimension of the antenna. The bandwidth also can be increased by increasing the horizontal dimension of the antenna, but this is undesirable in an antenna array environment for several reasons, most notably because it would increase the spacing between the elements which directly impacts the performance of an antenna array (like steering capability, grating lobes, ...). However, varying these distances can affect the bandwidth only within a limited range. Furthermore, it is desirable to reduce the size and weight of electronic components, particularly electronic components in telecommunication devices, such as mobile terminals, for example.

**[0018]** Another known technique to increase the frequency bandwidth is to add an additional or parasitic patch above the first patch 14, resulting in a so-called "stacked patch antenna". A perspective view of a simple stacked patch antenna 30 is shown in **FIGS. 2A and 2B**. While Fig. 2A shows the antenna with substrate layers, Fig. 2B shows the metal layers of antenna 30 without any substrate layers. Note that stacked patch antenna 30 may also be implemented as cavity backed stacked patch antenna, similar to the cavity structure described with respect to Figs. 1A and 1B.

**[0019]** For instance, a second (parasitic) patch 26 can

be placed above the first patch 14 and separated therefrom by a dielectric material (for example, a dielectric substrate) having a permittivity similar to air. The second patch 26 can have approximately similar dimensions as first patch 14. A signal to be transmitted can be input to the antenna through feed line 18, which then can drive both patches 14, 26 simultaneously. The second patch 26 parasitically couples to the drive signal by parasitically capacitively coupling to the first patch 14. The additional resonance provided by the second patch can increase the frequency bandwidth of the antenna. It can also enhance its gain. However, when a second linear polarization is introduced (e.g., by a dual-polarized patch antenna) the antenna loses a tuning parameter and thus loses bandwidth.

**[0020]** The present disclosure proposes to bring a tuning parameter back by capacitive coupling of the cavity to a patch and thus achieving a higher bandwidth than without the coupling effect. Turning now to **FIG. 3A**, it is illustrated an enhanced patch antenna design according to an example of the present disclosure, which can provide an increased bandwidth compared to the examples described above.

**[0021]** **FIG. 3A** is a side view of a patch antenna element 40 according to an example. It comprises a substrate 20, a patch 14 disposed on the substrate 20, and a ground plane 22 disposed on the substrate 20 below the patch 14. The skilled person having benefit from the present disclosure will appreciate that patch 14 can be of many shapes, including circular, triangular, and rectangular shapes. In this example, ground plane 22 horizontally extends beyond patch 14 (i.e., has a larger horizontal extension) and conductively connects to vertically extending electrically conductive side walls 24 laterally surrounding patch 14. Side walls 24 comprise or conductively connect to a conductive planar arrangement in form of protrusions or projections 36 horizontally extending from the side walls 24 toward the patch 14. Thus, electrically conductive protrusions 36 extend inwardly from side walls 24 to patch 14.

**[0022]** The skilled person having benefit from the present disclosure will appreciate that patch antenna element 40 can be manufactured with an adequate manufacturing method. An example flowchart of a corresponding manufacturing method 130 is illustrated in **FIG. 13A**.

**[0023]** Method 130 includes disposing 132 an antenna ground plane 22 on a substrate 20, wherein the ground plane horizontally extends beyond an area of a patch 14. Method 130 further includes disposing 134 vertically extending side walls 24 on the ground plane 22, wherein the side walls laterally surround the area of the patch. Method 130 further includes forming 136 a conductive planar arrangement in form of protrusions 36 which horizontally extend from the side walls toward the patch 14, and disposing 138 the patch 14 on the substrate 20 above the ground plane 22 such that the patch, the ground plane, the side walls, and the protrusions circumscribe a

volume  $V$  between the patch and the ground plane. Antenna element 40 may be created by conventional semiconductor manufacturing techniques such as depositing one or more metal layers on one or more substrate layers 12, 20 by any of a number of techniques known in Printed Circuit Board (PCB)/ semiconductor fabrication industry and etching them by any of a number of techniques known in the semiconductor fabrication industry.

**[0024]** Turning back to FIG 3, a horizontal distance  $d$  between protrusions 36 and patch 14 may be smaller than a horizontal distance between side walls 24 and patch 14. Or, to put it differently, a horizontal extension  $h$  of the protrusions 36 may be larger than a horizontal extension or width  $h_{SW}$  of the side walls 24 extending between the protrusions 36 and ground plane 22, i.e.  $h \geq h_{SW}$ . Side walls 24 may connect to protrusions 36 at a horizontally outer end of protrusions 36, the outer end facing away from patch 14. Thereby, the horizontally inner end of protrusions 36 faces patch 14. The distance  $d$  is measured between the horizontally inner end of protrusions 36 and the horizontally outer end of patch 14. In some examples, protrusions 36 can form a peripheral protruding frame at least partially surrounding patch 14.

**[0025]** Protrusions 36 reaching close to patch 14 increase the capacitive coupling between patch 14 and the surrounding cavity formed by protrusions 36, side walls 24, and ground plane 22. This capacitive coupling between protrusions 36 and patch 14 can yield an additional tuning parameter which can be used to enhance the bandwidth of patch antenna element 40 with respect to conventional designs. The protrusions 36 also help to streamline radiating electric field lines in the horizontal direction. A stronger horizontal electric field means more "voltage" over the radiation resistance and this in turn can lead to more radiated power and to a larger bandwidth.

**[0026]** Similar to top ground plane 16 of FIGS. 1A and 1B, protrusions 36 can be formed by a metallic frame structure peripherally surrounding patch 14. This protruding frame structure may also be regarded as an upper ground plane, since it is short circuited with bottom ground plane 22 via side walls 24. However, in contrast to the conventional patch antenna element 10 illustrated in FIGS. 1A and 1B, the horizontal or lateral gap between protrusions 36 and patch 14 is considerably smaller in FIG. 3A. In other words, protrusions 36 reach closer to patch 14 compared to the conventional design of FIGS. 1A and 1B. That is, the capacitive coupling can be implemented by a closely spaced annular or peripheral ring around patch 14 that is connected to ground. Patch 14, ground plane 22, side walls 24, and protrusions 36 may all be formed of one or more metal layers.

**[0027]** In the illustrated example of FIG. 3A, protrusions 36 extend horizontally toward the patch 14 from an upper end of side walls 24. In this example, protrusions 36 may thus also be considered as a top ground plane. In general, a horizontal extension  $h$  of the protrusions 36 may be equal to or smaller than  $\lambda/4$ , i.e.  $0 < h \leq \lambda/4$ ,

wherein  $h \geq h_{SW}$ . The protrusions could also be larger than  $\lambda/4$ , but when the antenna is used in an array a good configuration is  $\leq \lambda/4$ . Edges of the patch 14 and of the protrusions 36 facing each other are separated by a gap  $G$  having width  $d$ . According to examples of the present disclosure, the width  $d$  of the gap can be smaller than  $\lambda/5$ . It has been found that  $d \leq \lambda/10$  can lead to good bandwidth performance of patch antenna element 40. Here,  $\lambda$  denotes the wavelength (in free space) of the Radio Frequency (RF) signal to be emitted or received.

**[0028]** In some examples, protrusions 36 and patch 14 can be implemented in the same metal layer of a layer stack. Patch 14 and protrusions 36 may be created by conventional PCB/ semiconductor manufacturing techniques such as depositing one or more metal layers on the substrate 20 by any of a number of techniques known in semiconductor fabrication industry and etching them by any of a number of techniques known in the semiconductor fabrication industry to create the two distinct metallizations, i.e., protrusions 36 and patch 14.

**[0029]** In the illustrated example, ground plane 22, side walls 24, and protrusions 36 circumscribe a volume  $V$  or a cavity between patch 14 and ground plane 22. The volume  $V$  may comprise dielectric substrate material 12, for example. Dielectric substrate material 12 can extend underneath the protrusions 36, such that the volume or area 38 directly underneath the protrusions 36 also comprises dielectric substrate material 12. As has been explained above, side walls 24, which may be formed by vias, and ground plane 22 form a shielded cavity around the patch 14, which helps to minimize coupling between adjacent patch antenna elements in an array of patch antenna elements.

**[0030]** The skilled person having benefit from the present disclosure will appreciate that patch antenna element 40 will further comprise at least one feedline (not shown) which can be coupled (e.g. by an ohmic contact) to the patch 14 in various ways. It may be directly coupled to the patch 14 via at least one feedpoint. In other examples, the feedline and patch 14 may be capacitively coupled. In the first case, the at least one feedline may be guided to the at least one feedpoint of the patch 14 through the ground plane 22. In examples related to multipolarized patch antennas, patch antenna element 40 may optionally comprise a first feedline coupled to patch 14 via a first feedpoint configured for a first antenna polarization and a second feedline coupled to patch 14 via a second feedpoint configured for a second antenna polarization.

**[0031]** As shown in FIG. 3B, the side walls 24 of FIG. 3A could also be omitted, leading to an example patch antenna element 40' without cavity but merely with a conductive planar arrangement or frame structure 36 above ground plane 22, wherein the conductive planar arrangement 36 at least partially laterally surrounds patch 14. Edges of the patch 14 and of the conductive planar arrangement 36 facing each other are separated by gap  $G$  having width  $d$ . According to examples of the present

disclosure, the width  $d$  gap G can be smaller than  $\lambda/5$ . It has been found that  $d \leq \lambda/10$  can lead to good bandwidth performance of patch antenna element 40'. A horizontal extension  $h$  of the conductive planar arrangement 36 may be equal to or smaller than  $\lambda/4$ , i.e.  $0 < h \leq \lambda/4$ , wherein  $h \geq h_{SW}$ . However, horizontal extension  $h$  of the conductive planar arrangement 36 could also be larger than  $\lambda/4$ .

**[0032]** The skilled person having benefit from the present disclosure will appreciate that patch antenna element 40' can be manufactured with an adequate manufacturing method. An example flowchart of a corresponding manufacturing method 130' is illustrated in **FIG. 13B**.

**[0033]** Method 130' includes disposing 132 an antenna ground plane 22 on a substrate 20, wherein the ground plane horizontally extends beyond an area of a patch 14. Method 130' further includes disposing 138 the patch 14 on the substrate 20 above the ground plane 22, and forming or disposing 139 a conductive planar arrangement or frame structure 36 on the substrate 20 above the ground plane 22, wherein the conductive planar arrangement or frame structure 36 at least partially laterally surrounds the patch 14. Antenna element 40' may be created by conventional semiconductor manufacturing techniques such as depositing one or more metal layers on one or more substrate layers 12, 20 by any of a number of techniques known in Printed Circuit Board (PCB)/ semiconductor fabrication industry and etching them by any of a number of techniques known in the semiconductor fabrication industry.

**[0034]** **FIG. 4A** shows a further example of a patch antenna element 50 according to the present disclosure.

**[0035]** In addition to patch antenna element 40 of **FIG. 3A**, patch antenna element 50 comprises a second parasitic patch 26 disposed above the first patch 14 to form a cavity backed stacked patch antenna. Parasitic patch 26 is separated from the first patch 14 by dielectric substrate material 52 disposed between parasitic patch 26 and the first patch 14 for capacitive coupling between parasitic patch 26 and patch 14. In the illustrated example, side walls 24 extend up to parasitic patch 26 in order to isolate the patch antenna element 50 from adjacent ones. Thus, here, protrusions 36 do not extend horizontally toward the patch 14 from an upper end of the side walls but from a portion of the side walls 24 in essentially the same vertical height as the first patch 14. The skilled person having benefit from the present disclosure will appreciate that the side walls 24 could also end in the height of the first patch 14, similar to **FIG. 3**.

**[0036]** As shown in **FIG. 4B**, the side walls 24 of **FIG. 4A** could also be omitted, leading to an example patch antenna element 50' without cavity but merely with a conductive planar arrangement or frame structure 36 at least partially laterally surrounding patch 14 vis-à-vis the radiating edges of patch 14. Edges of the patch 14 and of the conductive planar arrangement 36 facing each other are separated by gap G having width  $d$ . According to examples of the present disclosure, the width  $d$  gap G

can be smaller than  $\lambda/5$  or even smaller than  $\lambda/10$ . A horizontal extension  $h$  of the conductive planar arrangement 36 may be equal to or smaller than  $\lambda/4$ , i.e.  $0 < h \leq \lambda/4$ , wherein  $h \geq h_{SW}$ . However, horizontal extension  $h$  of the conductive planar arrangement 36 could also be larger than  $\lambda/4$ .

**[0037]** **FIGS. 5 and 6** show further examples of the present disclosure.

**[0038]** In the example of **FIG. 5A**, side walls 24 comprise or conductively connect to protrusions 36 and 36' horizontally extending toward patch 14 and parasitic patch 26, respectively. Protrusions 36' related to parasitic patch 26 can be formed by a metallic frame structure peripherally surrounding parasitic patch 26. In the illustrated example, protrusions 36' extend horizontally toward the parasitic patch 26 from an upper end of side walls 24. Edges of the parasitic patch 26 and the protrusions 36' facing each other are separated by a gap. According to examples of the present disclosure, a width  $d'$  of the gap is smaller than  $\lambda/5$ . It has been found that  $d' \leq \lambda/10$  can lead to good performance of patch antenna element 60. Note that widths  $d$  and  $d'$  can be different from each other in some examples. For example, protrusions 36' and parasitic patch 26 can be implemented in the same metal layer of a layer stack. Parasitic patch 26 and corresponding protrusions 36' may be created by conventional PCB/ semiconductor manufacturing techniques such as depositing one or more metal layers on the substrate 20, 12, 52 by any of a number of techniques known in semiconductor fabrication industry and etching them by any of a number of techniques known in the PCB/ semiconductor fabrication industry to create the distinct metallizations.

**[0039]** As shown in **FIG. 5B**, the side walls 24 of **FIG. 5A** could also be omitted, leading to an example patch antenna element 60' without cavity but merely with a first conductive planar arrangement or frame structure 36 at least partially laterally surrounding patch 14 vis-à-vis the radiating edges of patch 14 and a second conductive planar arrangement or frame structure 36' at least partially laterally surrounding parasitic patch 26 vis-à-vis the radiating edges of parasitic patch 26.

**[0040]** In the example of **FIG. 6A**, side walls 24 only comprise or conductively connect to protrusions 36' horizontally extending toward parasitic patch 26. The protrusions 36 of the previous examples are omitted here. Due to the protrusions 36' related to parasitic patch 26 still a better bandwidth of patch antenna element 70 may be achieved compared to conventional solutions.

**[0041]** As shown in **FIG. 6B**, the side walls 24 of **FIG. 6A** could also be omitted, leading to an example patch antenna element 70' without cavity but merely with a conductive planar arrangement or frame structure 36' at least partially laterally surrounding parasitic patch 26 vis-à-vis the radiating edges of parasitic patch 26.

**[0042]** The skilled person having benefit from the present disclosure will appreciate that yet further examples are possible. For example, protrusions may be lo-

cated below or above patch 14 or parasitic patch 26. That is to say, patch and related protrusions do not necessarily have to be implemented in the same metal layer. Examples also allow for an implementation in different metal layers, leading to a different vertical position of patch and related protrusions.

**[0043]** FIGS. 7 and 8 provide a comparison between a conventional cavity backed stacked patch antenna 80, which is similar to the example discussed with respect to FIGS. 1A and 1B, and an enhanced cavity backed stacked patch antenna 90 according to an example of the present disclosure.

**[0044]** The enlarged view of FIG. 7 shows a substrate 20 which can comprise a plurality of substrate layers. A ground metal layer 82 is formed on substrate 20 and separated from a feed line 84 by substrate material. Above feedline 84 antenna ground plane 22 is deposited. Electrically conductive sidewalls 24 electrically couple the top and bottom ground planes 16 and 22 to each other and thus form a shielded cavity around patch 14. Further dielectric layers 52 and a parasitic patch 26 are bonded on top of patch 14. Due to the larger gap (here: in the mm range) between top ground plane 16 and patch 14 there is only a relatively weak capacitive coupling between top ground plane 16 and patch 14 in the conventional device 80.

**[0045]** In the device 90 illustrated in FIG. 8, top ground plane 16 additionally comprises protrusion portions 36 extending inwardly toward patch 14, thus leading to a considerably smaller gap between protrusion portions 36 and patch 14. In the illustrated example, the protrusion portions 36 are only implemented in the top metal layer of a metal layer stack forming the side walls 24. The gap between protrusion portions 36 and patch 14 only has a horizontal width of 200  $\mu\text{m}$  compared to a horizontal extension of patch 14 in the mm range. This smaller gap leads to higher capacitive coupling between protrusion portions 36 and patch 14 in the device 90. Thus, the ground metal 22 is strongly coupled to the adjacent patch 14. This coupling can take place on all four sides of the patch 14 in some embodiments, and can thus enable a broadband matching of the antenna.

**[0046]** A perspective view the stacked patch antenna 90 of FIG. 8 is shown in FIGS. 9A and 9B. While FIG. 9A shows the antenna 90 with substrate layers, FIG. 9B shows antenna 90 without substrate layers.

**[0047]** A comparison of FIGS. 10A, B and 11A, B shows a possible improvement between a conventional stacked patch antenna design without improved metal cavity surrounding and a stacked patch antenna design with metal cavity surrounding according to an example of the present disclosure. As can be seen from both figures, a significant antenna bandwidth improvement can be achieved with metal cavity surrounding and protrusions. In the illustrated examples, the antenna bandwidth (for example, where the antenna reflection is less than -10dB) has been improved from 2,032 GHz for the conventional case to 3,173 GHz, which is a substantial in-

crease in bandwidth. FIG. 11C depicts the radiation efficiency and total efficiency of both conventional and enhanced antenna structures. It can be seen that the increase in bandwidth of the enhanced design does not originate from a decrease in radiation efficiency. In fact a slight increase in radiation efficiency can be recognized for the enhanced metal cavity backed stacked patch antenna (EMCBSPA).

**[0048]** FIGS. 12A and 12B illustrate the influence of a horizontal thickness of the sidewalls  $h_{SW}$  relative to the horizontal extension of the protrusions  $h_P$ , given the same vertical and horizontal extensions of the patch antenna element  $h_{PA}$  and the same minimum gap width  $d$  between sidewalls and patch.

**[0049]** It can be seen from FIG. 12B that the bandwidth of the antenna decreases with decreasing ratio  $h_P/h_{SW}$  (in the example Prototype Sim\_23 the protrusions completely vanish, thus  $h_P/h_{SW} = 0$ ). This is because the effective volume of the cavity circumscribed by ground plane side walls and protrusions decreases with decreasing ratio  $h_P/h_{SW}$ . This means that the ratio  $h_P/h_{SW}$  should be chosen as large as possible (given a predetermined fixed horizontal extension of the patch antenna element  $h_{PA}$  and a predetermined fixed gap width  $d$  (e.g.,  $d = \lambda/10$ ) between protrusions 36 and patch 14). Thus, in some examples the ratio  $h_P/h_{SW}$  may be chosen larger than 1 (i.e.,  $h_P > h_{SW}$ ) or even larger than 2 (i.e.,  $h_P > 2h_{SW}$ ).

**[0050]** The proposed capacitive coupling of the metal cavity to the main and/or parasitic patch can bring back a tuning parameter which can be used to enhance the bandwidth. The proposed metal cavity can ensure a good metal density on every layer (> 50%) which may be crucial for the lamination process. The higher metallization density may on top of that be very helpful for heat dissipation generated by an Radio Frequency Integrated Circuit (RFIC) which can be flip-chip mounted to the other side of the antenna. The proposed metal cavity can attenuate the coupling between neighboring elements in an antenna array due to the fact that the metal walls damp the propagation of surface waves in the dielectric substrate. An example of an antenna array 140 comprising a plurality (here: four) of enhanced cavity backed patch antenna elements according to the present disclosure is shown FIG. 14.

**[0051]** FIG. 15 is a more detailed block diagram of an example of a device, e.g. a telecommunication device, in which enhanced cavity backed patch antenna elements according to example implementations can be implemented. Device 1500 can represent a mobile computing device, such as a computing tablet, a mobile phone or smartphone, a wireless-enabled e-reader, wearable computing device, or other telecommunication device. It will be understood that certain of the components are shown generally, and not all components of such a device are shown in device 1500.

**[0052]** Device 1500 includes processor 1510, which performs the primary processing operations of device 1500. Processor 1510 can include one or more physical

devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1510 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting device 1500 to another device. The processing operations can also include operations related to audio I/O and/or display I/O.

**[0053]** In one embodiment, device 1500 includes audio subsystem 1520, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into device 1500, or connected to device 1500. In one embodiment, a user interacts with device 1500 by providing audio commands that are received and processed by processor 1510.

**[0054]** Display subsystem 1530 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device. Display subsystem 1530 includes display interface 1532, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1532 includes logic separate from processor 1510 to perform at least some processing related to the display. In one embodiment, display subsystem 1530 includes a touchscreen device that provides both output and input to a user. In one embodiment, display subsystem 1530 includes a high definition (HD) display that provides an output to a user. High definition can refer to a display having a pixel density of approximately 100 PPI (pixels per inch) or greater, and can include formats such as full HD (e.g., 1080p), retina displays, 4K (ultra high definition or UHD), or others.

**[0055]** I/O controller 1540 represents hardware devices and software components related to interaction with a user. I/O controller 1540 can operate to manage hardware that is part of audio subsystem 1520 and/or display subsystem 1530. Additionally, I/O controller 1540 illustrates a connection point for additional devices that connect to device 1500 through which a user might interact with the system. For example, devices that can be attached to device 1500 might include microphone devices, speaker or stereo systems, video systems or other display device, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

**[0056]** As mentioned above, I/O controller 1540 can interact with audio subsystem 1520 and/or display subsystem 1530. For example, input through a microphone or other audio device can provide input or commands for

one or more applications or functions of device 1500. Additionally, audio output can be provided instead of or in addition to display output. In another example, if display subsystem includes a touchscreen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1540. There can also be additional buttons or switches on device 1500 to provide I/O functions managed by I/O controller 1540.

**[0057]** In one embodiment, I/O controller 1540 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, gyroscopes, global positioning system (GPS), or other hardware that can be included in device 1500. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features). In one embodiment, device 1500 includes power management 1550 that manages battery power usage, charging of the battery, and features related to power saving operation.

**[0058]** Memory subsystem 1560 includes memory device(s) 1562 for storing information in device 1500. Memory subsystem 1560 can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory 1560 can store application data, user data, music, photos, documents, or other data, as well as system data (whether longterm or temporary) related to the execution of the applications and functions of system 1500. In one embodiment, memory subsystem 1560 includes memory controller 1564 (which could also be considered part of the control of system 1500, and could potentially be considered part of processor 1510). Memory controller 1564 includes a scheduler to generate and issue commands to memory device 1562.

**[0059]** Connectivity 1570 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable device 1500 to communicate with external devices. The external device could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

**[0060]** Connectivity 1570 can include multiple different types of connectivity. To generalize, device 1500 is illustrated with cellular connectivity 1572 and wireless connectivity 1574. Cellular connectivity 1572 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, LTE (long term evolution - also referred to as "4G"), or other cellular service standards. Wireless connectivity 1574 refers to wireless connectivity that is not cellular, and can include personal area networks



(such as Bluetooth), local area networks (such as WiFi), and/or wide area networks (such as WiMax), or other wireless communication, such as NFC. Wireless communication refers to transfer of data through the use of modulated electromagnetic radiation through a non-solid medium. Wired communication occurs through a solid communication medium. Cellular connectivity 1572 and/or wireless connectivity 1574 can implement example patch antennas of the present disclosure.

**[0061]** Peripheral connections 1580 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that device 1500 could both be a peripheral device ("to" 1582) to other computing devices, as well as have peripheral devices ("from" 1584) connected to it. Device 1500 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on device 1500. Additionally, a docking connector can allow device 1500 to connect to certain peripherals that allow device 1500 to control content output, for example, to audiovisual or other systems.

**[0062]** In addition to a proprietary docking connector or other proprietary connection hardware, device 1500 can make peripheral connections 1580 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other type.

**[0063]** The following examples pertain to further embodiments:

Example 1 is a patch antenna element comprising a substrate, a patch disposed on the substrate, a ground plane disposed on the substrate below the patch, the ground plane horizontally extending beyond the patch, and a conductive planar arrangement at least partially laterally surrounding the patch.

In Example 2, the conductive planar arrangement of Example 1 comprises a metal layer or sheet at least partially surrounding the patch.

In Example 3, the patch antenna element of any of the previous Examples can further optionally comprise vertically extending side walls laterally surrounding the patch are disposed on the ground plane. The side walls can comprise, as conductive planar arrangement, planar protrusions horizontally extending toward the patch.

In Example 4, the patch antenna element of any of the previous Examples can further optionally comprise a parasitic patch disposed above the patch.

In Example 5, the parasitic patch of Example 4 can optionally be separated from the patch by dielectric substrate material disposed between the parasitic patch and the patch for capacitive coupling between the parasitic patch and the patch.

In Example 6, a horizontal extension of the parasitic patch of any one of Examples 4 or 5 can optionally be smaller than a horizontal extension of the patch.

In Example 7, the ground plane, the side walls, and the protrusions of any one of Examples 3 to 6 can optionally circumscribe a volume between the patch and the ground plane.

In Example 8, the volume of Example 7 can further optionally comprise dielectric substrate material.

In Example 9, edges of the patch and of the conductive planar arrangement facing each other can optionally be separated by a gap.

In Example 10, a horizontal extension of the gap of Example 9 can optionally be less than  $\lambda/10$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element.

In Example 11, the gap of Examples 9 or 10 can further optionally comprise dielectric substrate material.

In Example 12, the protrusions of any one of the Examples 3 to 11 can optionally extend horizontally toward the patch from an upper end of the side walls.

In Example 13, a volume underneath the protrusions of any one of the Examples 3 to 12 can further optionally comprise dielectric substrate material.

In Example 14, a horizontal extension of the protrusions of any one of Examples 3 to 13 can be larger than a horizontal extension of the side walls between the protrusions and the ground plane.

In Example 15, a horizontal extension of the protrusions of any one of Examples 3 to 14 can be equal to or less than  $\lambda/4$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element.

In Example 16, the patch antenna element of any one of the previous Examples can further optionally comprise at least one feedline coupled to the patch.

In Example 17, the at least one feedline of Example 16 can optionally be guided to at least one feedpoint of the patch through the ground plane.

In Example 18, the patch antenna element of any one of Examples 16 or 17 optionally comprises a first feedline coupled to the patch via a first feedpoint configured for a first antenna polarization and a second feedline coupled to the patch via a second feedpoint configured for a second antenna polarization.

In Example 19, the patch antenna element of any one of the previous Examples can be of rectangular, circular, or triangular shape.

In Example 20, the patch and the conductive planar arrangement of any one of the previous Examples can optionally be implemented in the same metal layer of a layer stack.

In Example 21, the patch, the ground plane, the side walls, and the protrusions of any one of the previous Examples can optionally be formed of metal.

Example 22 is an antenna array comprising a plurality of patch antenna elements of any one of the previous Examples..

Example 23 is a patch antenna element comprising a dielectric substrate, a first patch disposed on the dielectric substrate, a second patch disposed on the dielectric substrate underneath the first patch, a ground plane disposed on the dielectric substrate underneath the second patch. The ground plane horizontally extends beyond the second patch and is conductively connected to vertically extending side walls surrounding at least the second patch. A horizontal distance between the side walls and at least one of the first and second patch is less than  $\lambda/10$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element. The second patch, the ground plane, and the side walls circumscribe a volume comprising dielectric substrate material between the second patch and the ground plane.

In Example 24, the side walls of Example 23 further optionally comprise projections horizontally extending toward at least one of the first and second patch.

In Example 25, a horizontal extension of the projections of Example 24 is equal to or less than  $\lambda/4$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element.

Example 26 is a method for manufacturing a patch antenna element. The method includes disposing an antenna ground plane on a substrate, the ground plane horizontally extending beyond an area of a patch. The method further includes disposing the patch on the substrate above the ground plane, and

forming a conductive planar arrangement on the substrate above the ground plane, wherein the conductive planar arrangement at least partially laterally surrounds the patch.

In Example 27, the method of Example 26 can further optionally include disposing vertically extending side walls on the ground plane, the side walls laterally surrounding the area of the patch. The method can further optionally include forming, as conductive planar arrangement, planar protrusions horizontally extending from the side walls toward the patch, such that the patch, the ground plane, the side walls, and the protrusions circumscribe a volume between the patch and the ground plane.

In Example 28, forming the conductive planar arrangement on and disposing the patch of Example 26 or 27 can be performed such that edges of the patch and the conductive planar arrangement on facing each other are separated by a gap.

In Example 29, the gap of Example 28 is formed to less than  $\lambda/10$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element.

In Example 30, the protrusions of any one of Examples 27 to 29 can be formed to have a horizontal extension larger than a horizontal extension of the side walls between the protrusions and the ground plane.

In Example 31, the protrusions of any one of Examples 27 to 30 can be formed to have a horizontal extension equal to or less than  $\lambda/4$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element.

In Example 32, the side walls of any one of Examples 27 to 31 can be disposed by forming vias through the substrate.

In Example 33, the method of any one of Examples 26 to 32 further includes disposing a parasitic patch above the patch.

In Example 34, disposing the parasitic patch of Example 30 can further optionally comprise separating the parasitic patch from the patch by disposing dielectric substrate material between the parasitic patch and the patch for capacitive coupling between the parasitic patch and the patch.

**[0064]** The skilled person having benefit from the present disclosure will appreciate that the various examples described herein can be implemented individually

or in combination.

**[0065]** The aspects and features mentioned and described together with one or more of the previously detailed examples and figures, may as well be combined with one or more of the other examples in order to replace a like feature of the other example or in order to additionally introduce the feature to the other example.

**[0066]** The description and drawings merely illustrate the principles of the disclosure. Furthermore, all examples recited herein are principally intended expressly to be only for pedagogical purposes to aid the reader in understanding the principles of the disclosure and the concepts contributed by the inventor(s) to furthering the art. All statements herein reciting principles, aspects, and examples of the disclosure, as well as specific examples thereof, are intended to encompass equivalents thereof.

**[0067]** A functional block denoted as "means for ..." performing a certain function may refer to a circuit that is configured to perform a certain function. Hence, a "means for s.th." may be implemented as a "means configured to or suited for s.th.", such as a device or a circuit configured to or suited for the respective task.

**[0068]** Functions of various elements shown in the figures, including any functional blocks labeled as "means", "means for providing a sensor signal", "means for generating a transmit signal.", etc., may be implemented in the form of dedicated hardware, such as "a signal provider", "a signal processing unit", "a processor", "a controller", etc. as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which or all of which may be shared. However, the term "processor" or "controller" is by far not limited to hardware exclusively capable of executing software, but may include digital signal processor (DSP) hardware, network processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), read only memory (ROM) for storing software, random access memory (RAM), and non-volatile storage. Other hardware, conventional and/or custom, may also be included.

**[0069]** A block diagram may, for instance, illustrate a high-level circuit diagram implementing the principles of the disclosure. Similarly, a flow chart, a flow diagram, a state transition diagram, a pseudo code, and the like may represent various processes, operations or steps, which may, for instance, be substantially represented in computer readable medium and so executed by a computer or processor, whether or not such computer or processor is explicitly shown. Methods disclosed in the specification or in the claims may be implemented by a device having means for performing each of the respective acts of these methods.

**[0070]** It is to be understood that the disclosure of multiple acts, processes, operations, steps or functions disclosed in the specification or claims may not be construed as to be within the specific order, unless explicitly or im-

plicitly stated otherwise, for instance for technical reasons. Therefore, the disclosure of multiple acts or functions will not limit these to a particular order unless such acts or functions are not interchangeable for technical reasons. Furthermore, in some examples a single act, function, process, operation or step may include or may be broken into multiple sub-acts, -functions, -processes, -operations or -steps, respectively. Such sub acts may be included and part of the disclosure of this single act unless explicitly excluded.

**[0071]** Furthermore, the following claims are hereby incorporated into the detailed description, where each claim may stand on its own as a separate example. While each claim may stand on its own as a separate example, it is to be noted that - although a dependent claim may refer in the claims to a specific combination with one or more other claims - other examples may also include a combination of the dependent claim with the subject matter of each other dependent or independent claim. Such combinations are explicitly proposed herein unless it is stated that a specific combination is not intended. Furthermore, it is intended to include also features of a claim to any other independent claim even if this claim is not directly made dependent to the independent claim.

## Claims

1. A patch antenna element (40; 50; 60; 70; 90) comprising:
  - a substrate (12; 20);
  - a patch (14; 26) disposed on the substrate;
  - a ground plane (22) disposed on the substrate below the patch, the ground plane horizontally extending beyond the patch; and
  - a conductive planar arrangement (24; 36; 36') at least partially laterally surrounding the patch.
2. The patch antenna element (40; 50; 60; 70; 90) of any one of the previous claims, wherein the ground plane (22) is conductively connected to vertically extending side walls (24) laterally surrounding the patch, the side walls comprising planar protrusions (36; 36') horizontally extending toward the patch.
3. The patch antenna element (40; 50; 60; 70; 90) of any one of the previous claims, further comprising
  - a parasitic patch (26) disposed above the patch (14).
4. The patch antenna element (40; 50; 60; 70; 90) of claim 3, wherein the parasitic patch (26) is separated from the patch (14) by dielectric substrate material disposed between the parasitic patch (26) and the patch (14) for capacitive coupling between the parasitic patch and the patch.

5. The patch antenna element (40; 50; 60; 70; 90) of any one of claims 3 or 4 wherein a horizontal extension of the parasitic patch (26) is smaller than a horizontal extension of the patch (14). 5
6. The patch antenna element (40; 50; 60; 70; 90) of any one of claims 2 to 5, wherein the ground plane (22), the side walls (24), and the protrusions (36; 36') circumscribe a volume between the patch (14; 26) and the ground plane (22). 10
7. The patch antenna element (40; 50; 60; 70; 90) of any one of the previous claims, wherein edges of the patch (14; 26) and the conductive planar arrangement (24; 36; 36') facing each other are separated by a gap (G). 15
8. The patch antenna element (40; 50; 60; 70; 90) of claim 7, wherein a horizontal extension ( $d$ ,  $d'$ ) of the gap (G) is less than  $\lambda/10$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element. 20
9. The patch antenna element (40; 50; 60; 70; 90) of claim 7 or 8, wherein the gap comprises dielectric substrate material. 25
10. The patch antenna element (40; 50; 60; 70; 90) of any one of claims 2 to 9, wherein the protrusions (36; 36') extend horizontally toward the patch (14; 26) from an upper end of the side walls (24). 30
11. The patch antenna element (40; 50; 60; 70; 90) of any one of claims 2 to 10, wherein a horizontal extension (36; 36') of the protrusions is larger than a horizontal extension of the side walls (24) between the protrusions (36; 36') and the ground plane (22). 35
12. The patch antenna element (40; 50; 60; 70; 90) of any one of claims 2 to 11, wherein a horizontal extension of the protrusions (36; 36') is equal to or less than  $\lambda/4$ , wherein  $\lambda$  denotes a wavelength of a radio frequency signal to be transmitted or received via the patch antenna element. 40
13. The patch antenna element (40; 50; 60; 70; 90) of any one of the previous claims, further comprising: 45
  - at least one feedline coupled to the patch (14; 26); 50
14. The patch antenna element (40; 50; 60; 70; 90) of claim 13, comprising a first feedline coupled to the patch (14; 26) via a first feedpoint configured for a first antenna polarization and a second feedline coupled to the patch (14; 26) via a second feedpoint configured for a second antenna polarization. 55
15. The patch antenna element (40; 50; 60; 70; 90) of any one of the previous claims, wherein the patch (14; 26) and the conductive planar arrangement (24; 36; 36') are implemented in the same metal layer of a layer stack.

FIG. 1A

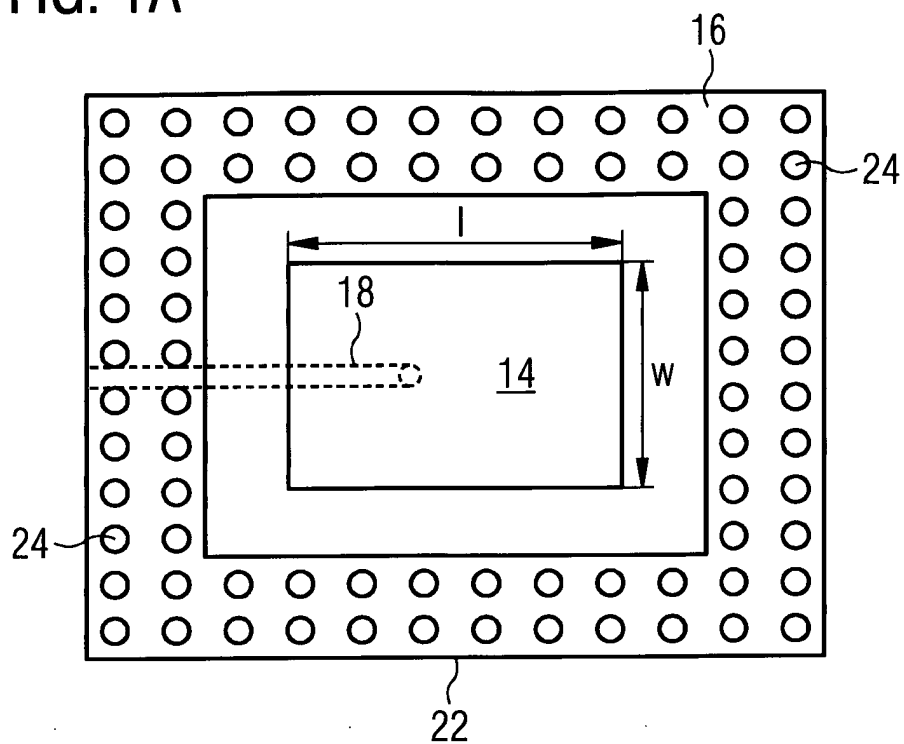


FIG. 1B

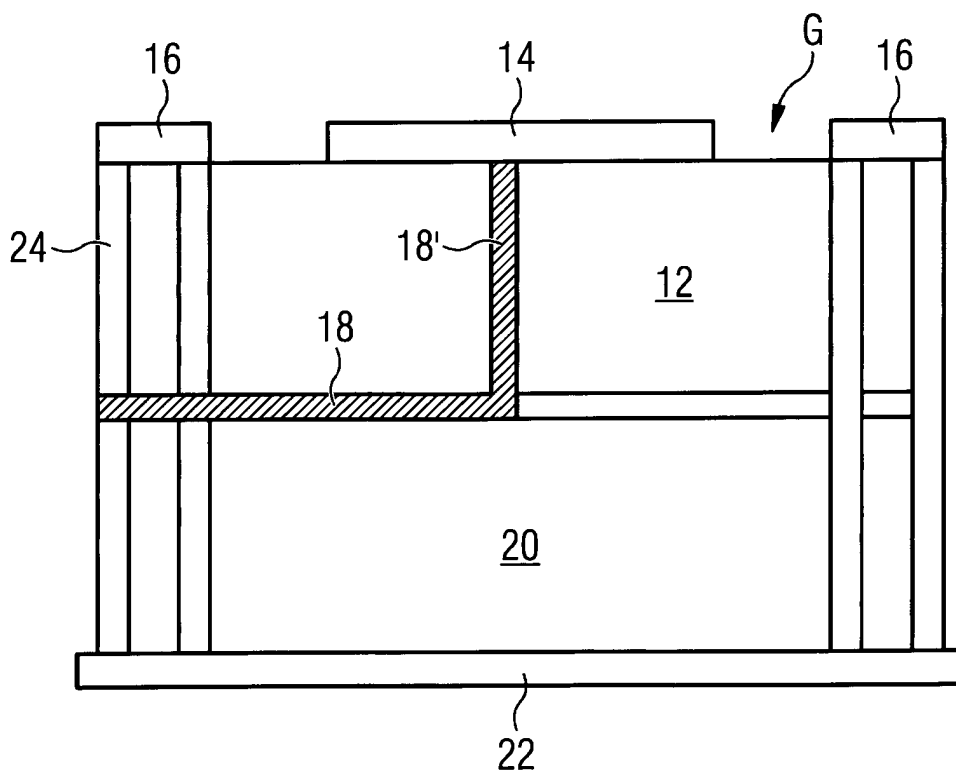


FIG. 2A

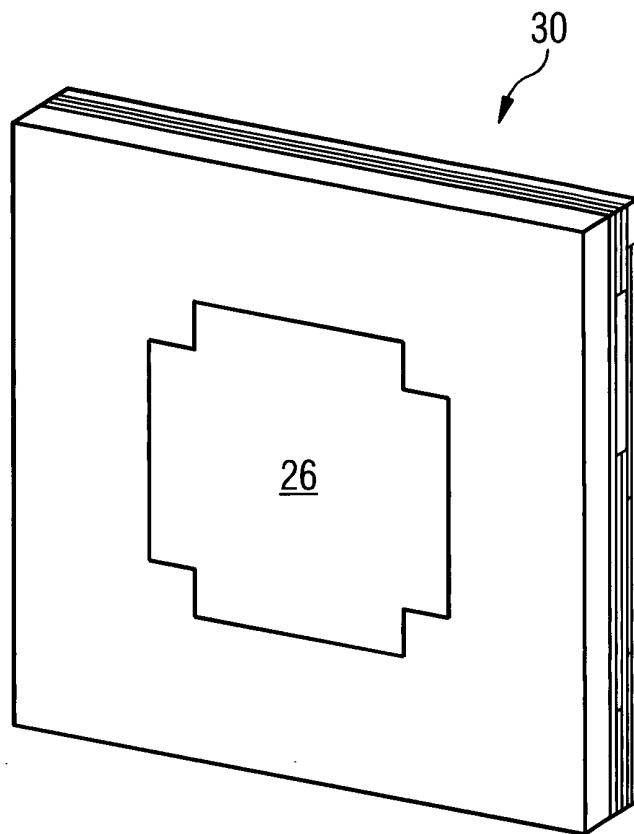


FIG. 2B

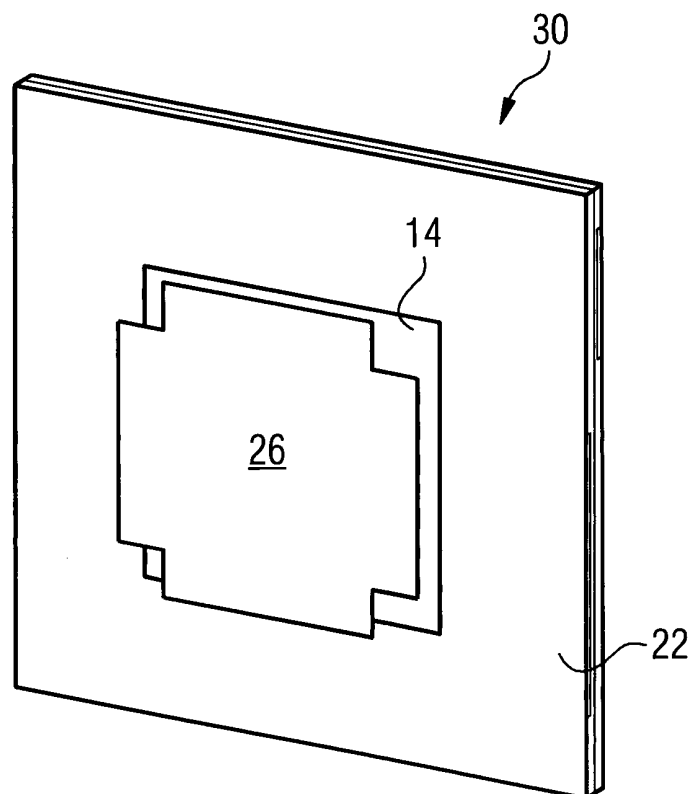


FIG. 3A

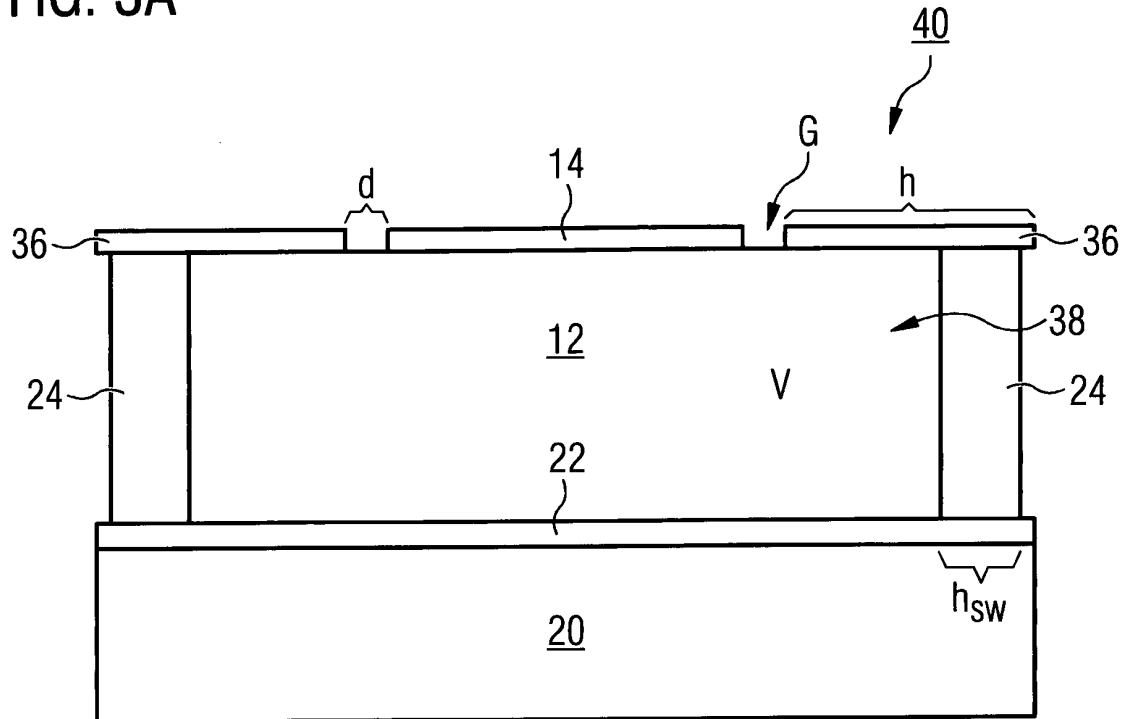


FIG. 3B

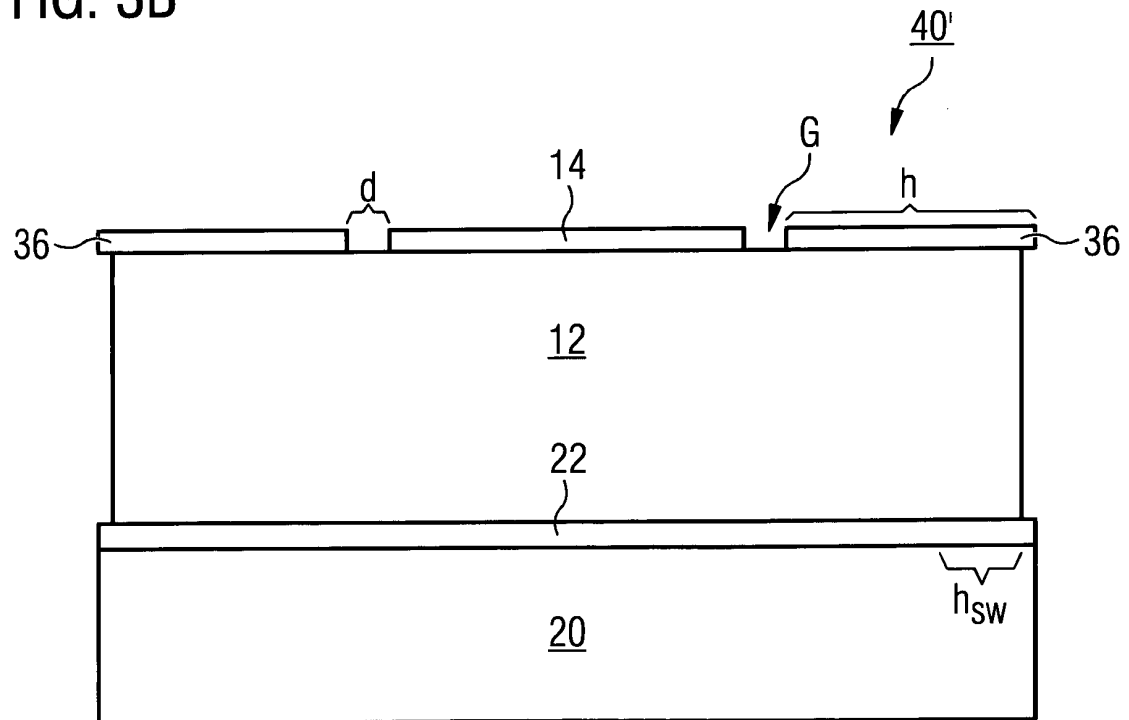


FIG. 4A

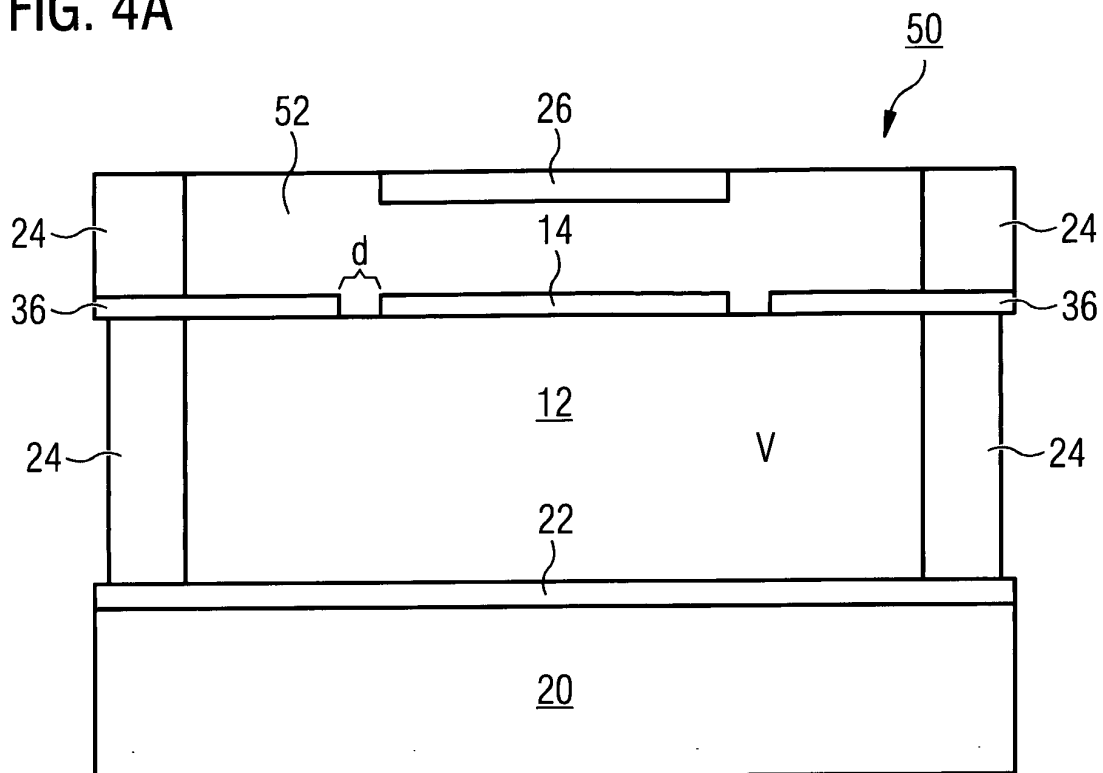


FIG. 4B

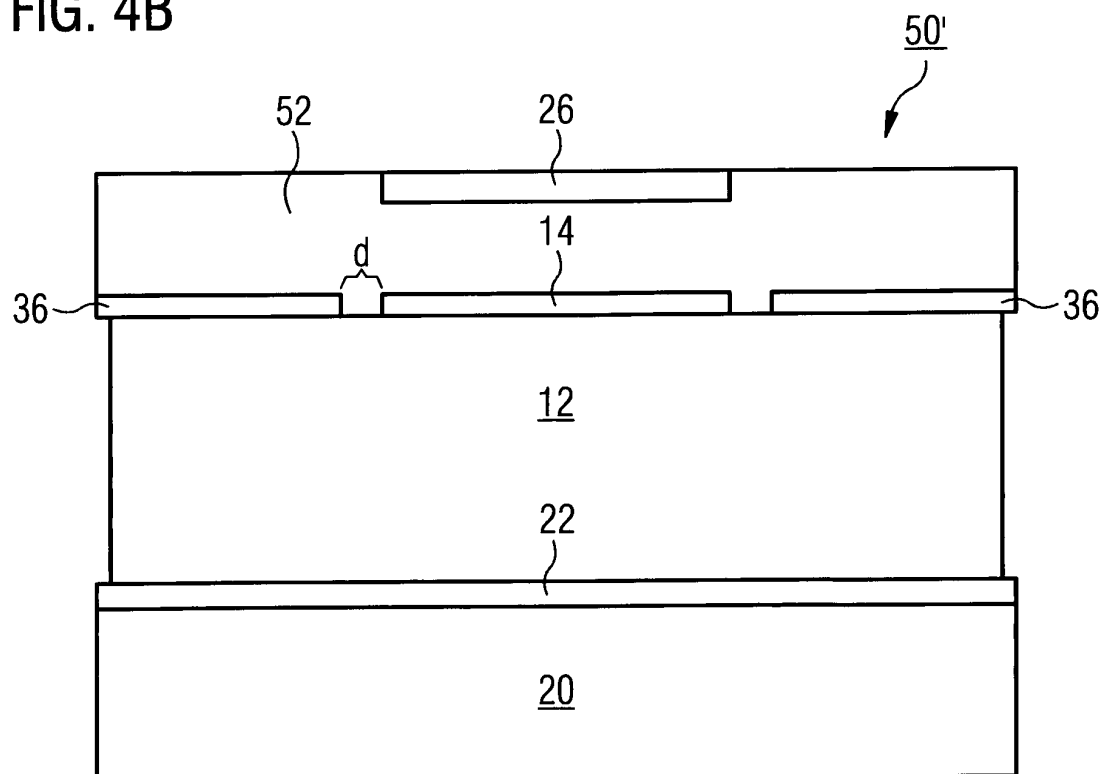




FIG. 5A

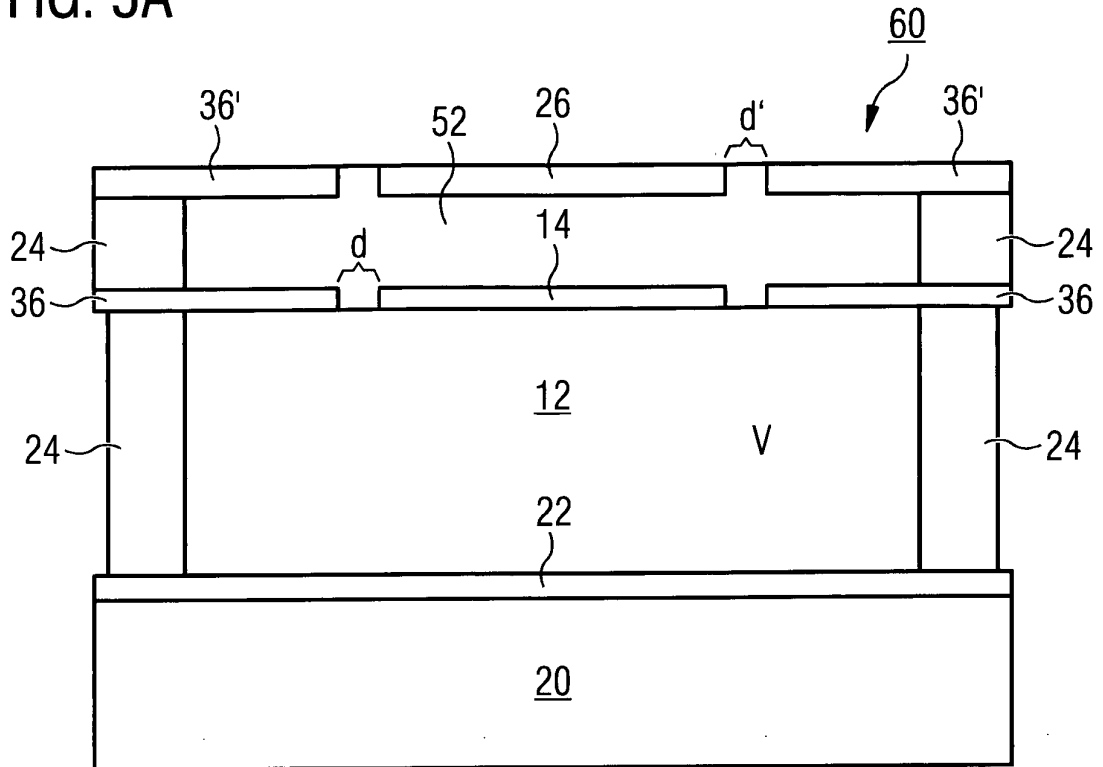


FIG. 5B

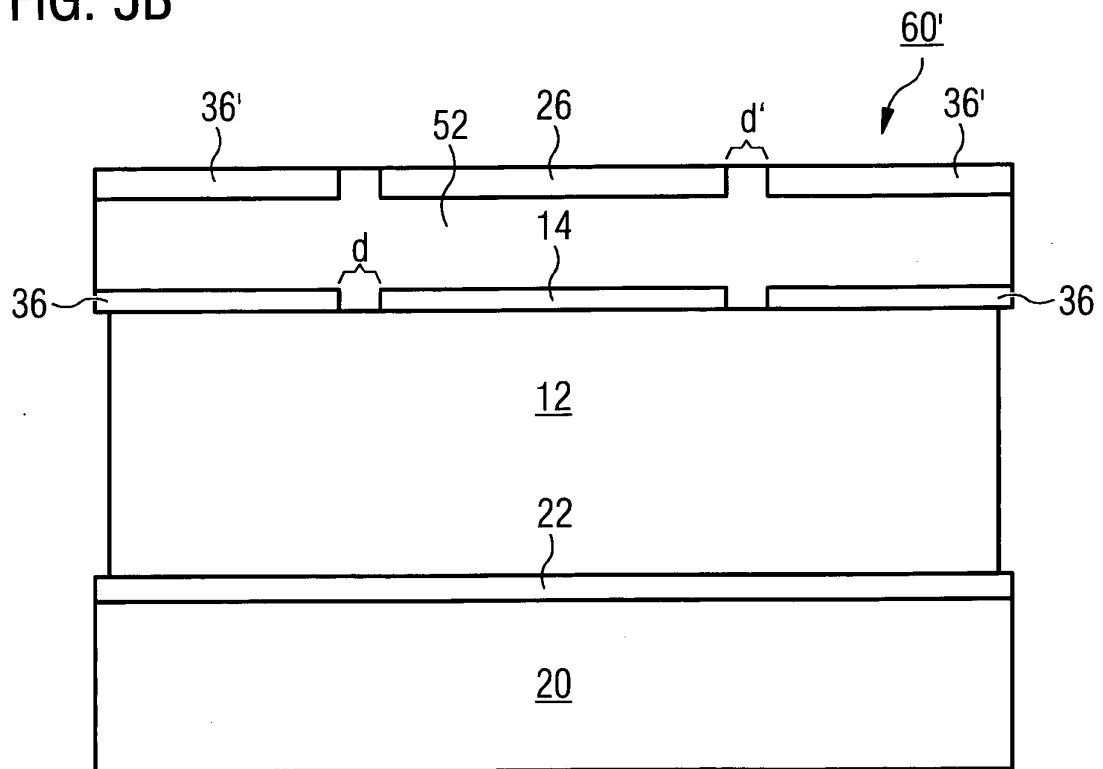


FIG. 6A

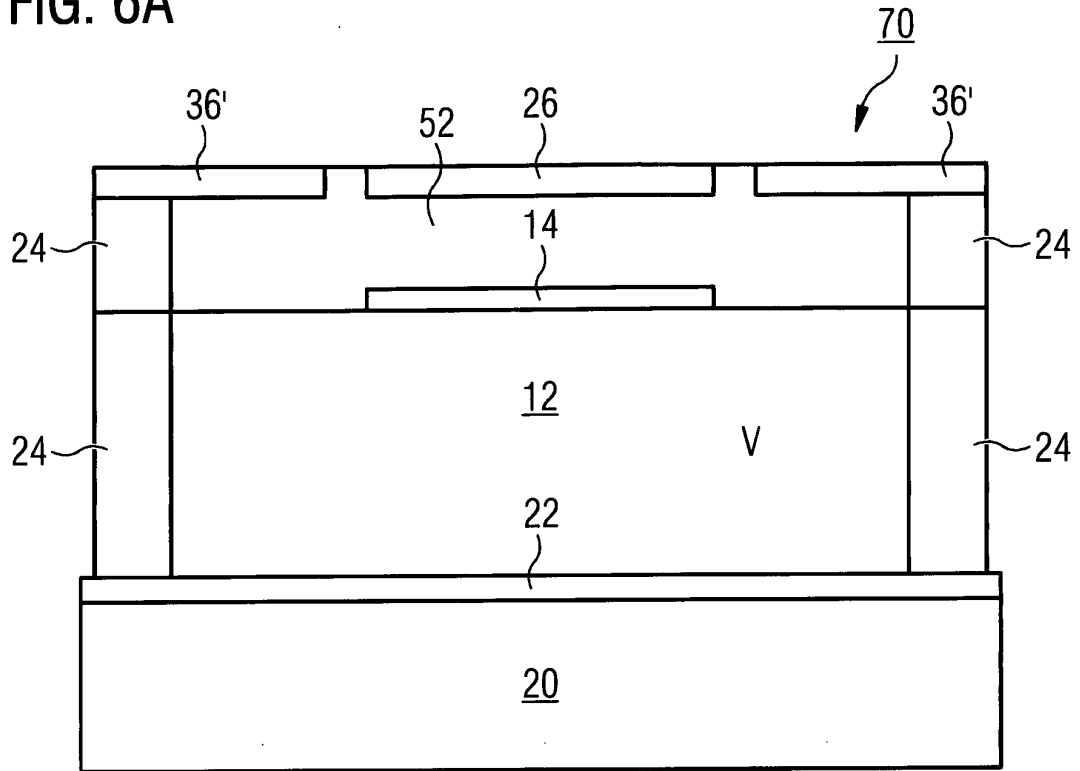


FIG. 6B

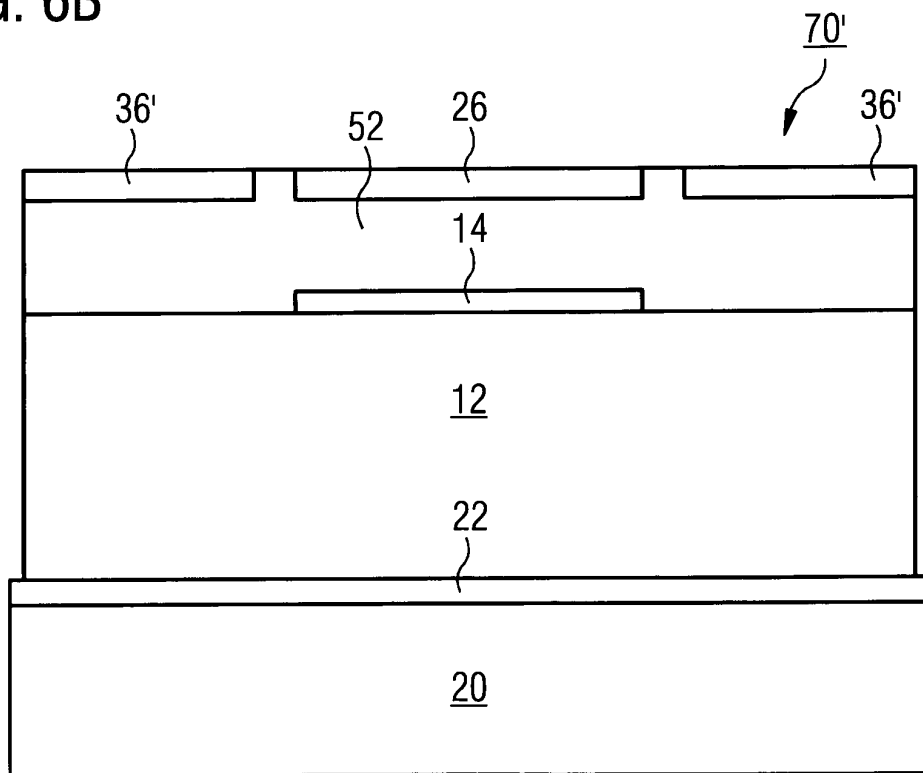


FIG. 7

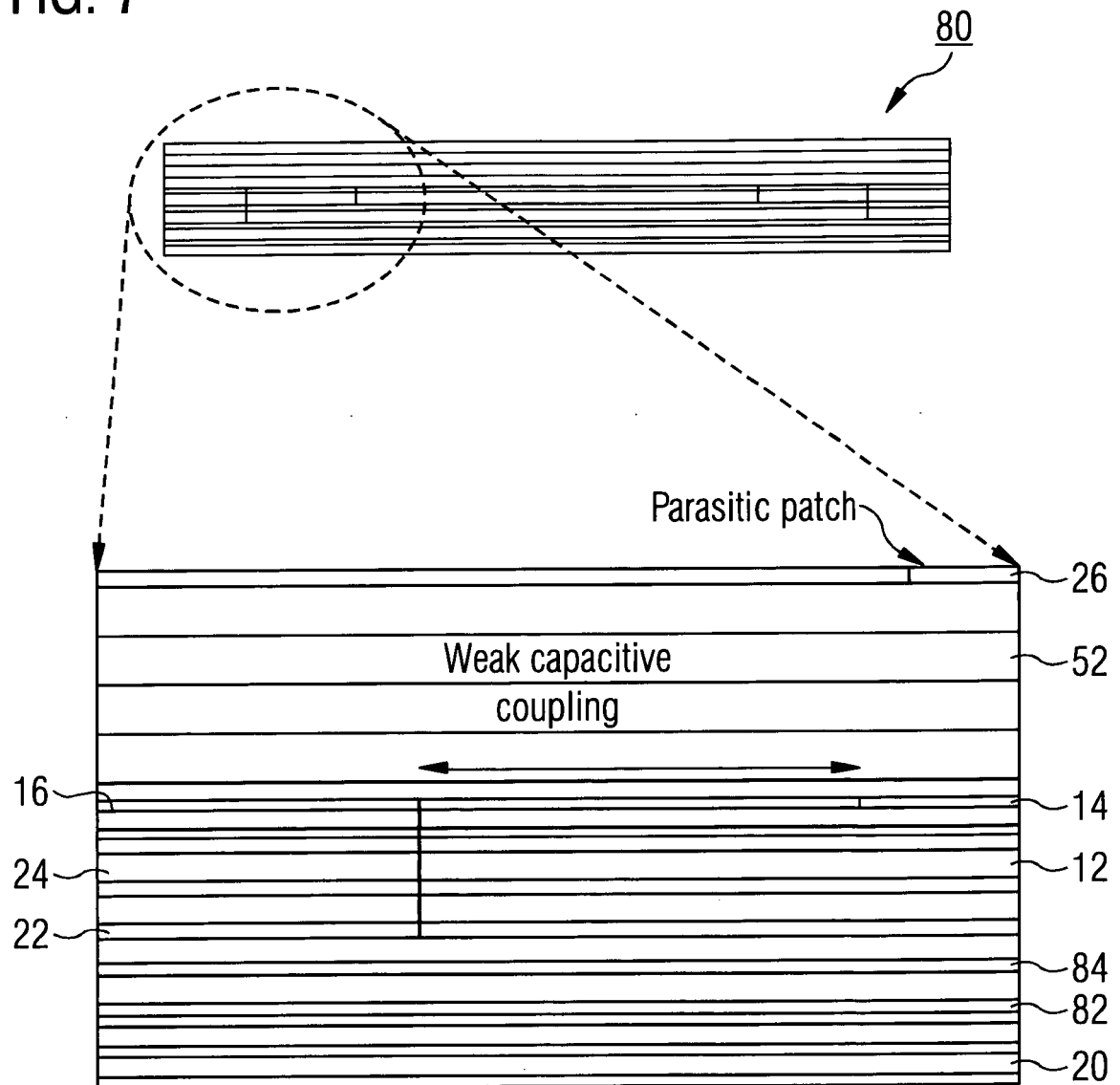


FIG. 8

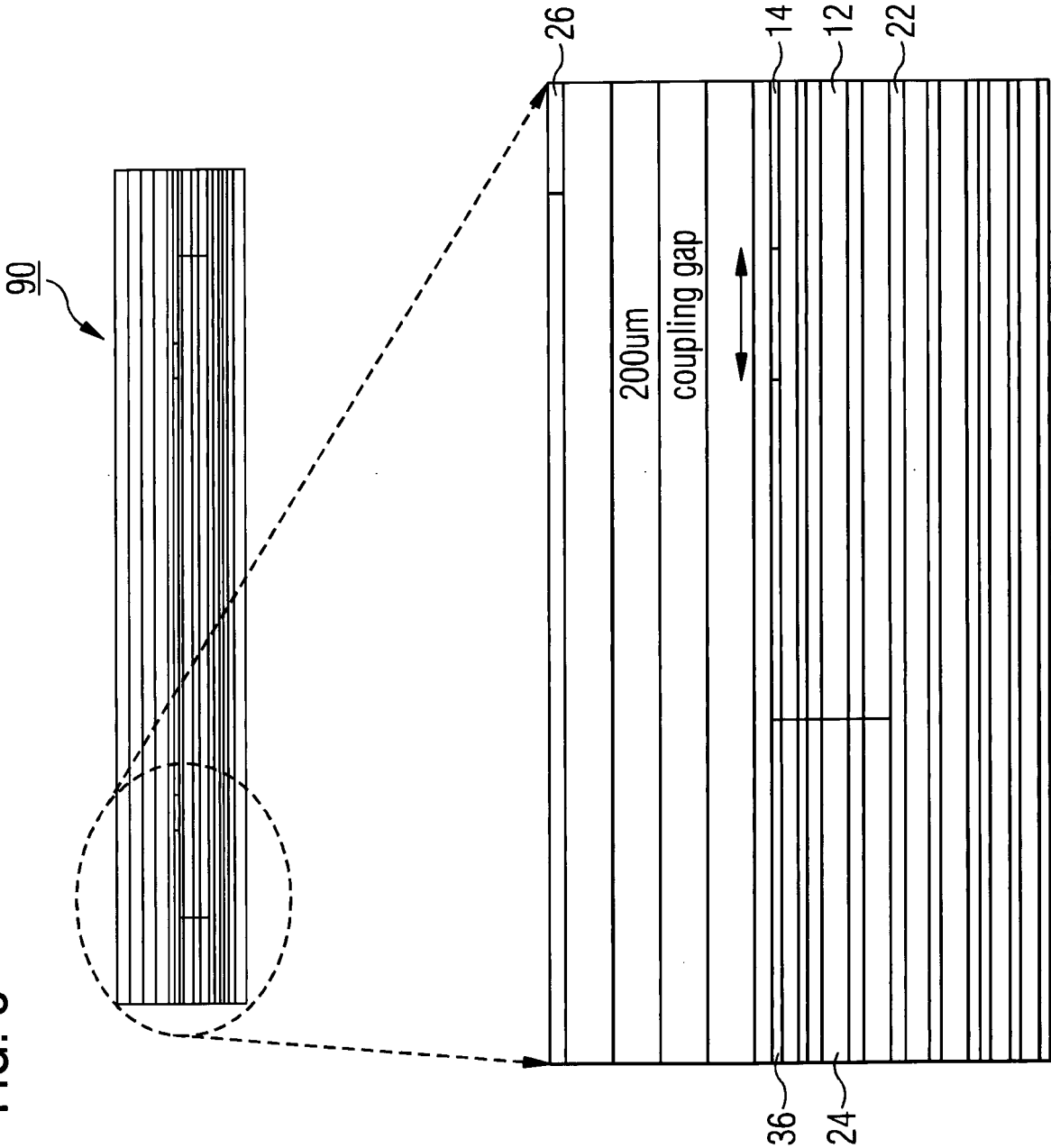


FIG. 9A

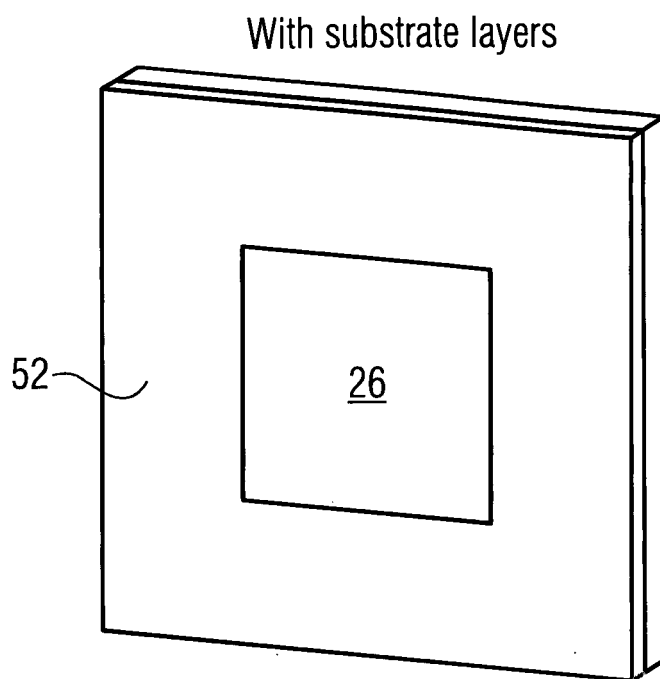


FIG. 9B

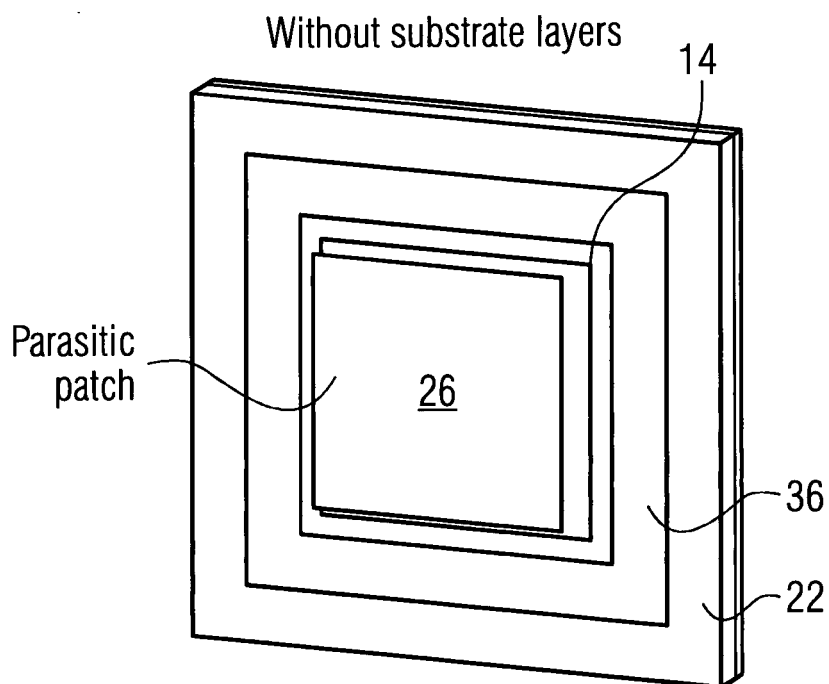


FIG. 10A

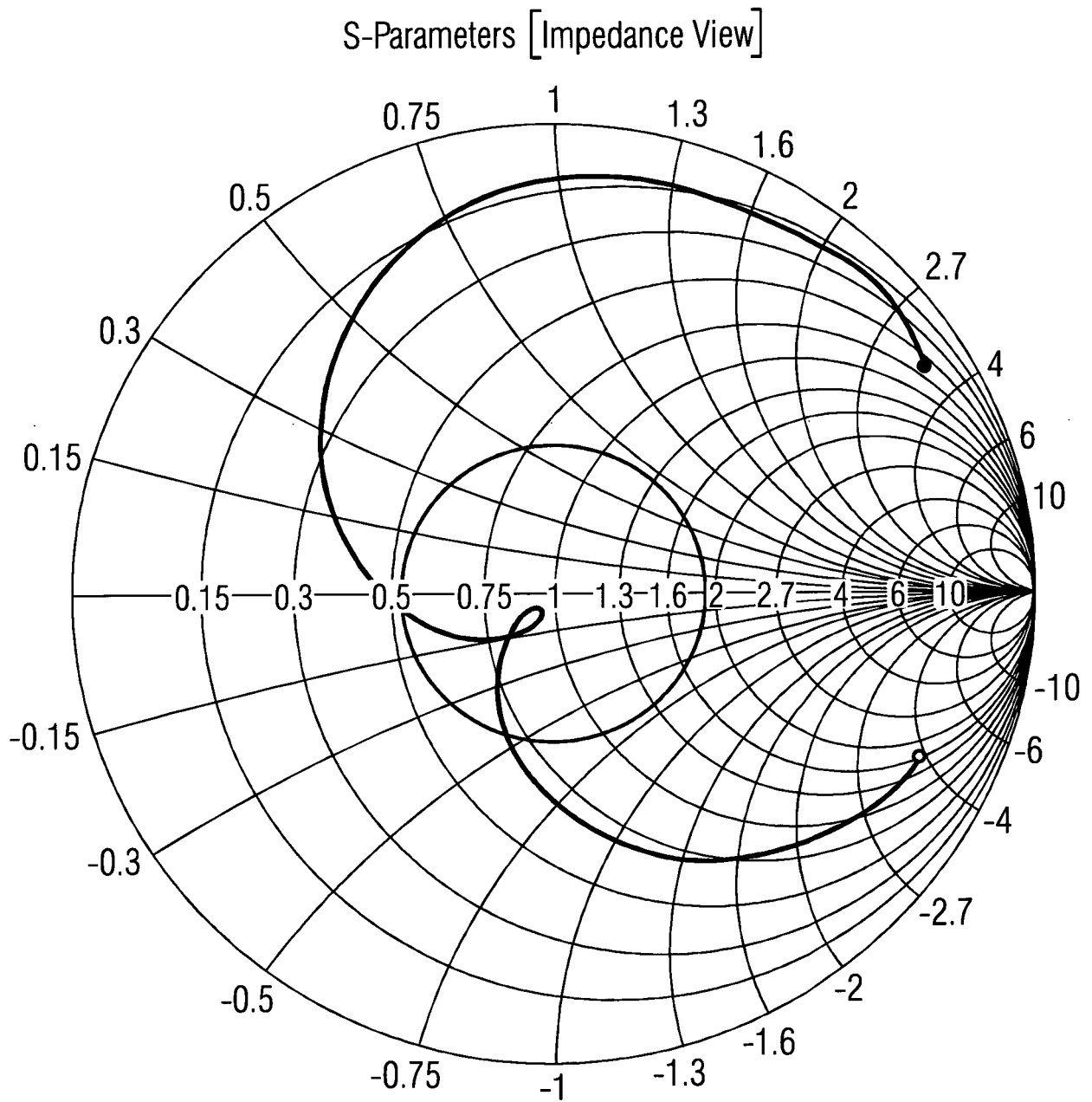


FIG. 10B

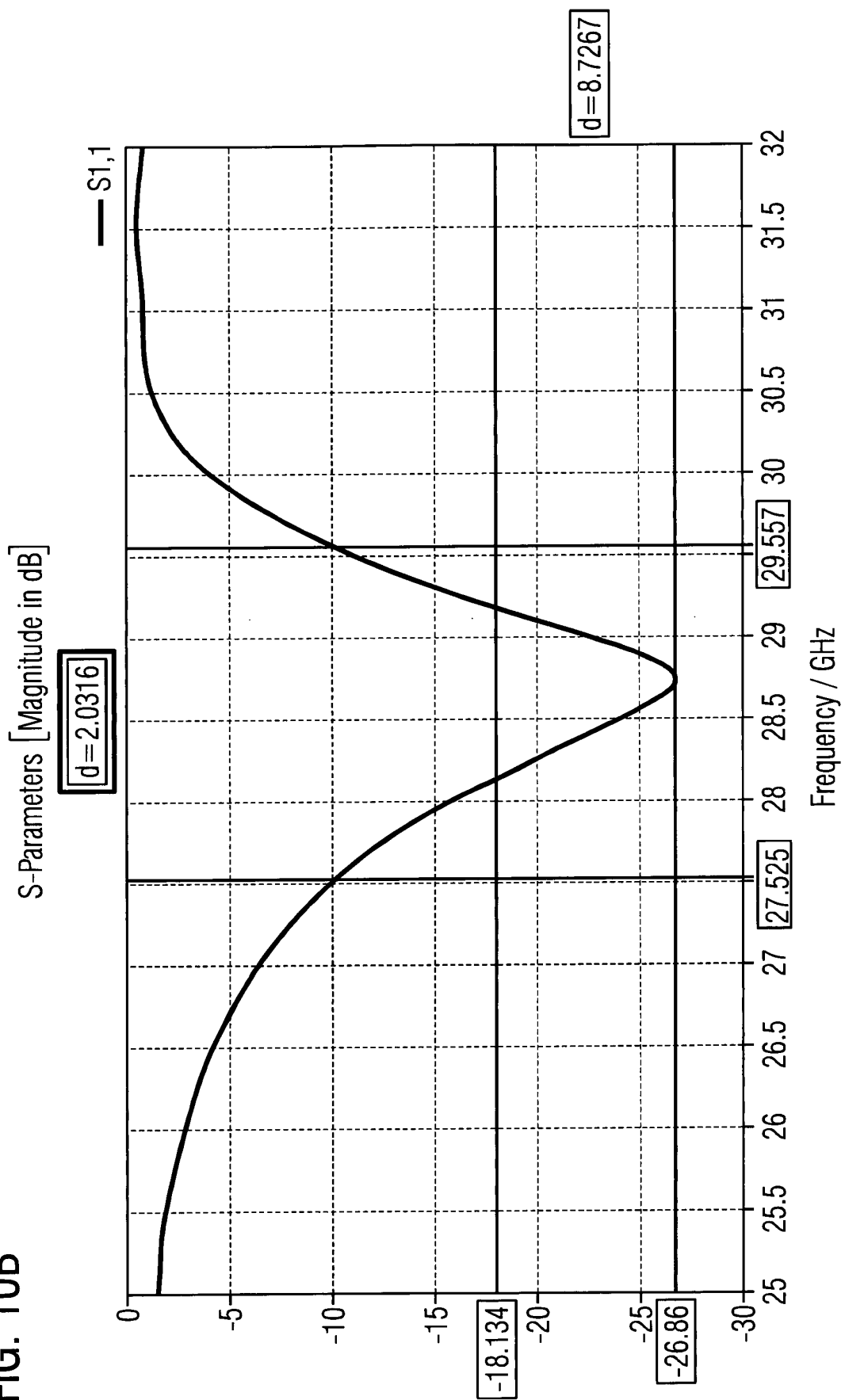


FIG. 11A

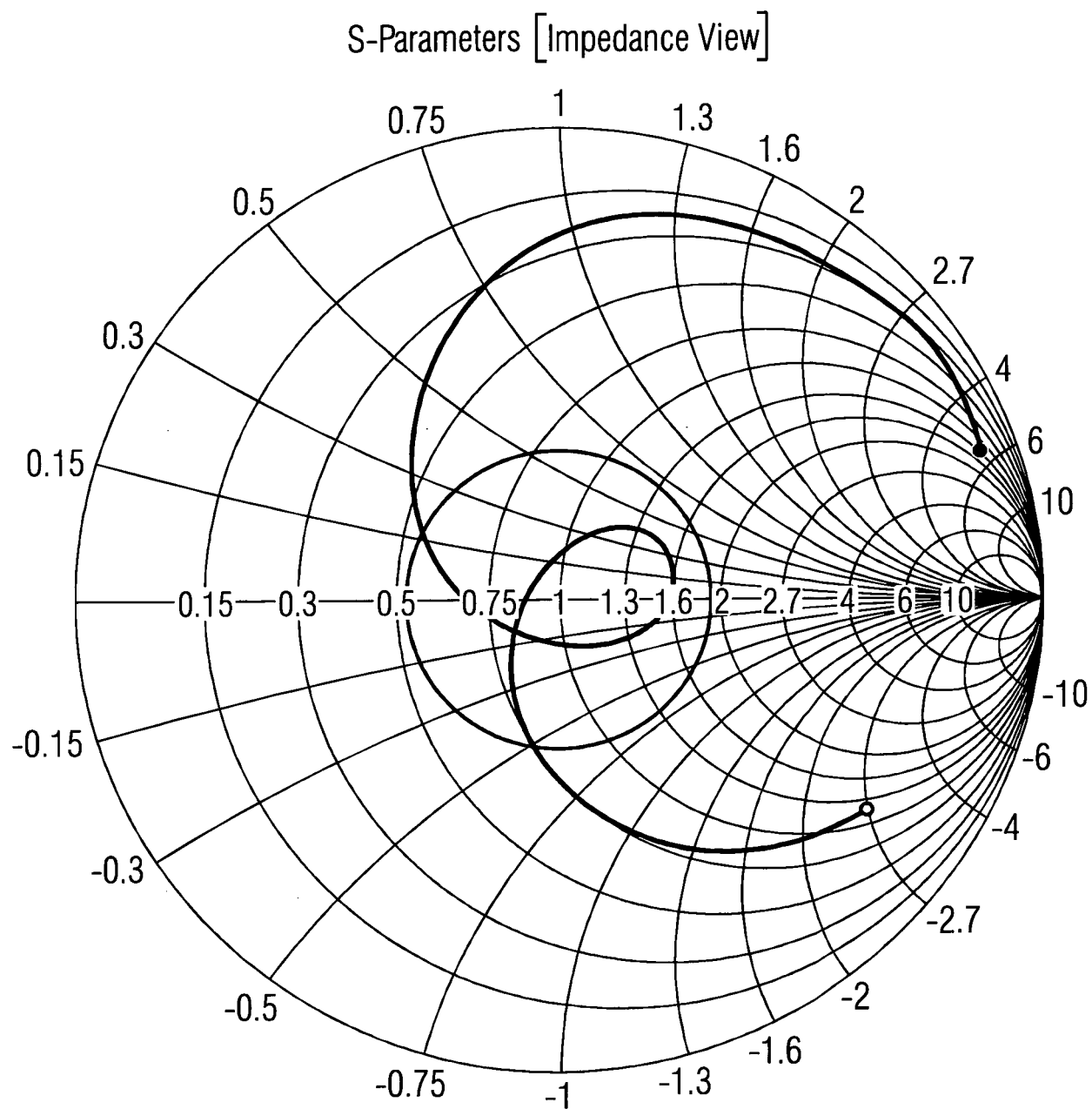




FIG. 11B

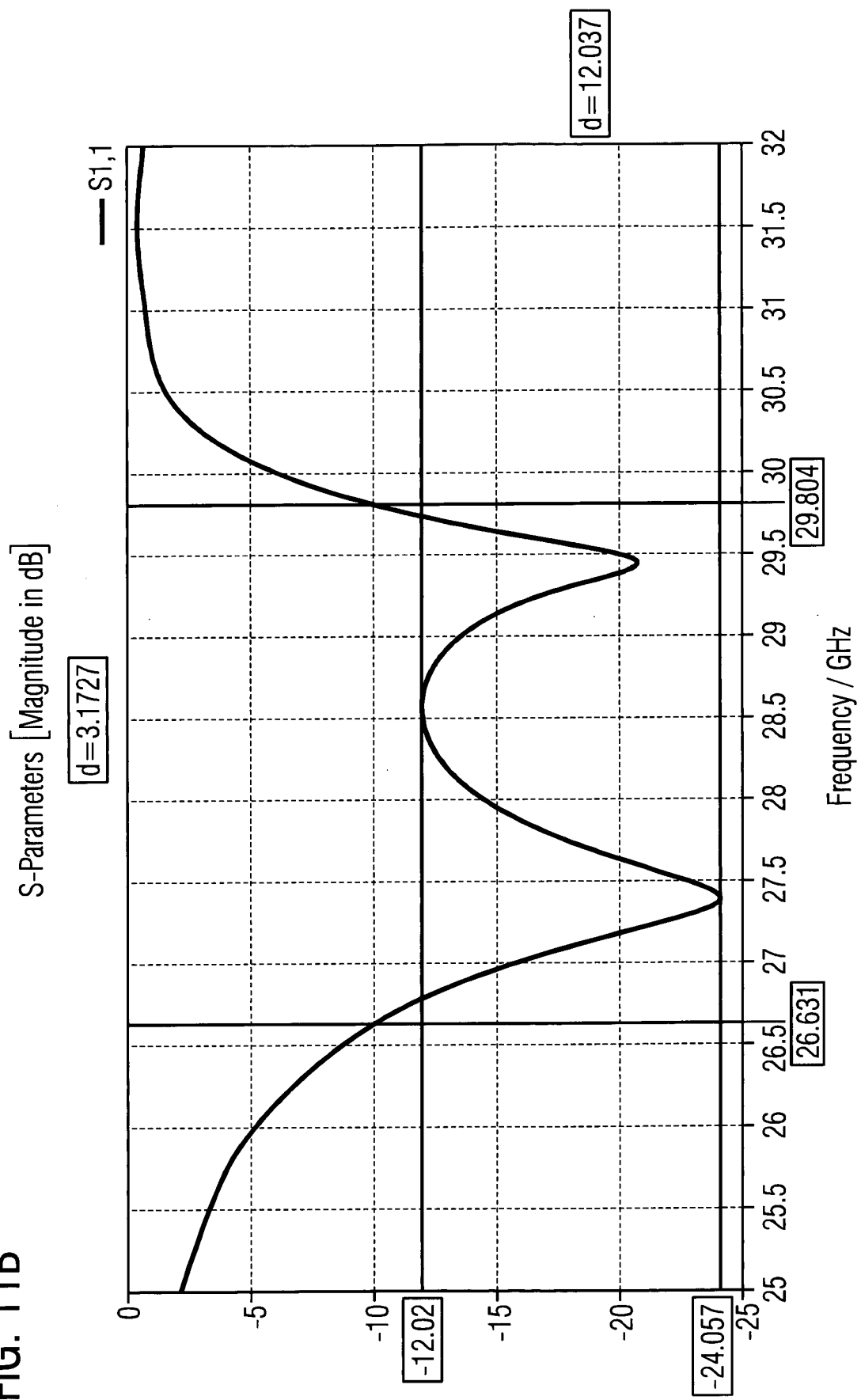


FIG. 11C

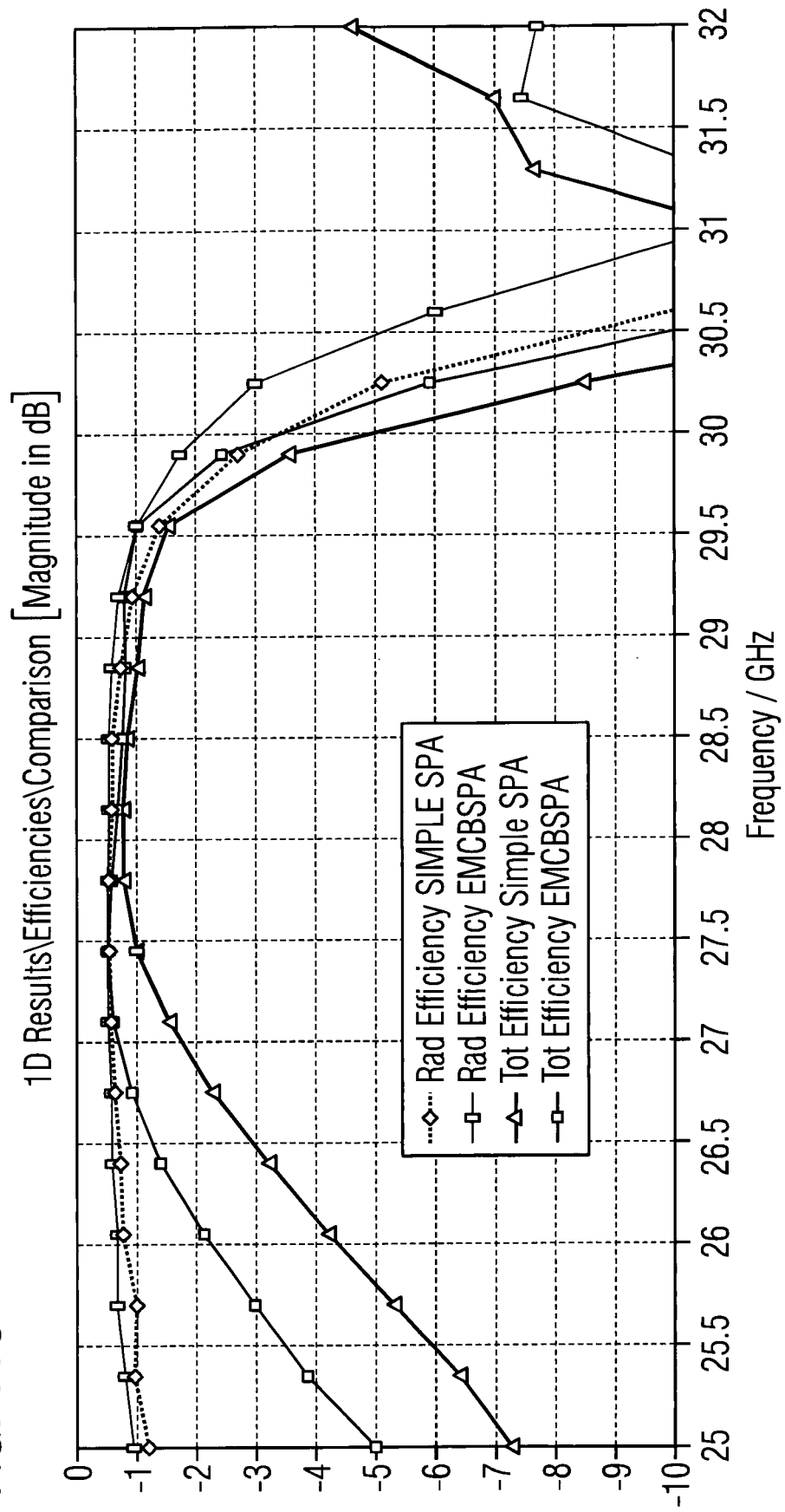


FIG. 12A

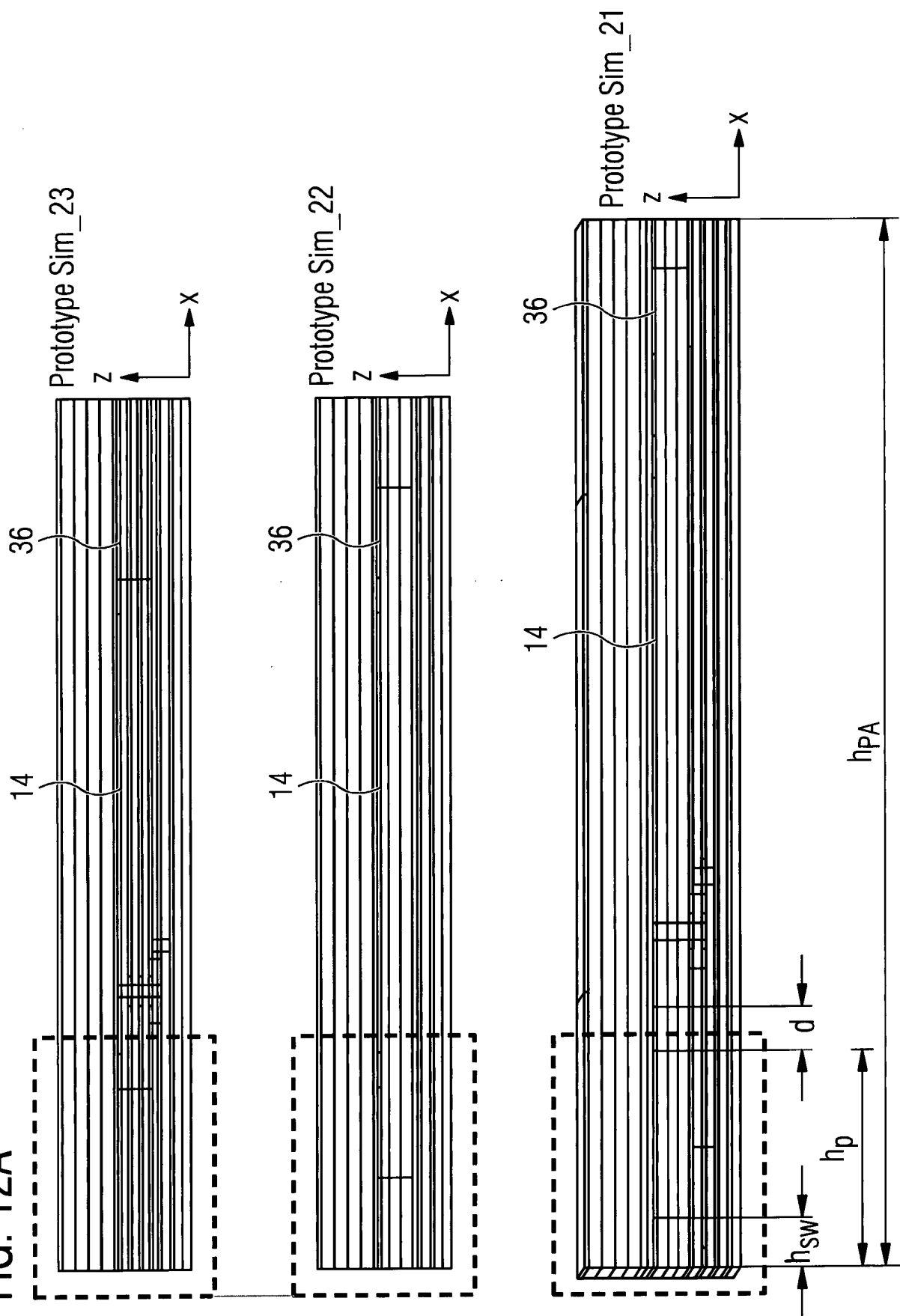


FIG. 12B

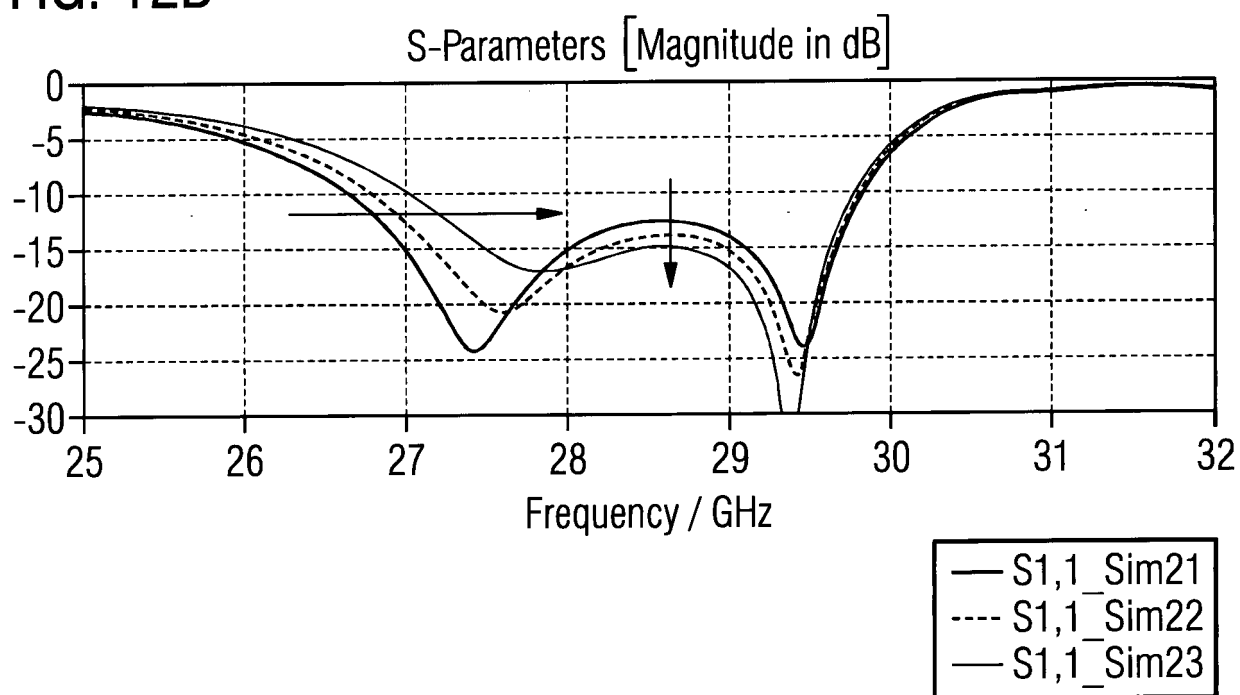


FIG. 13A

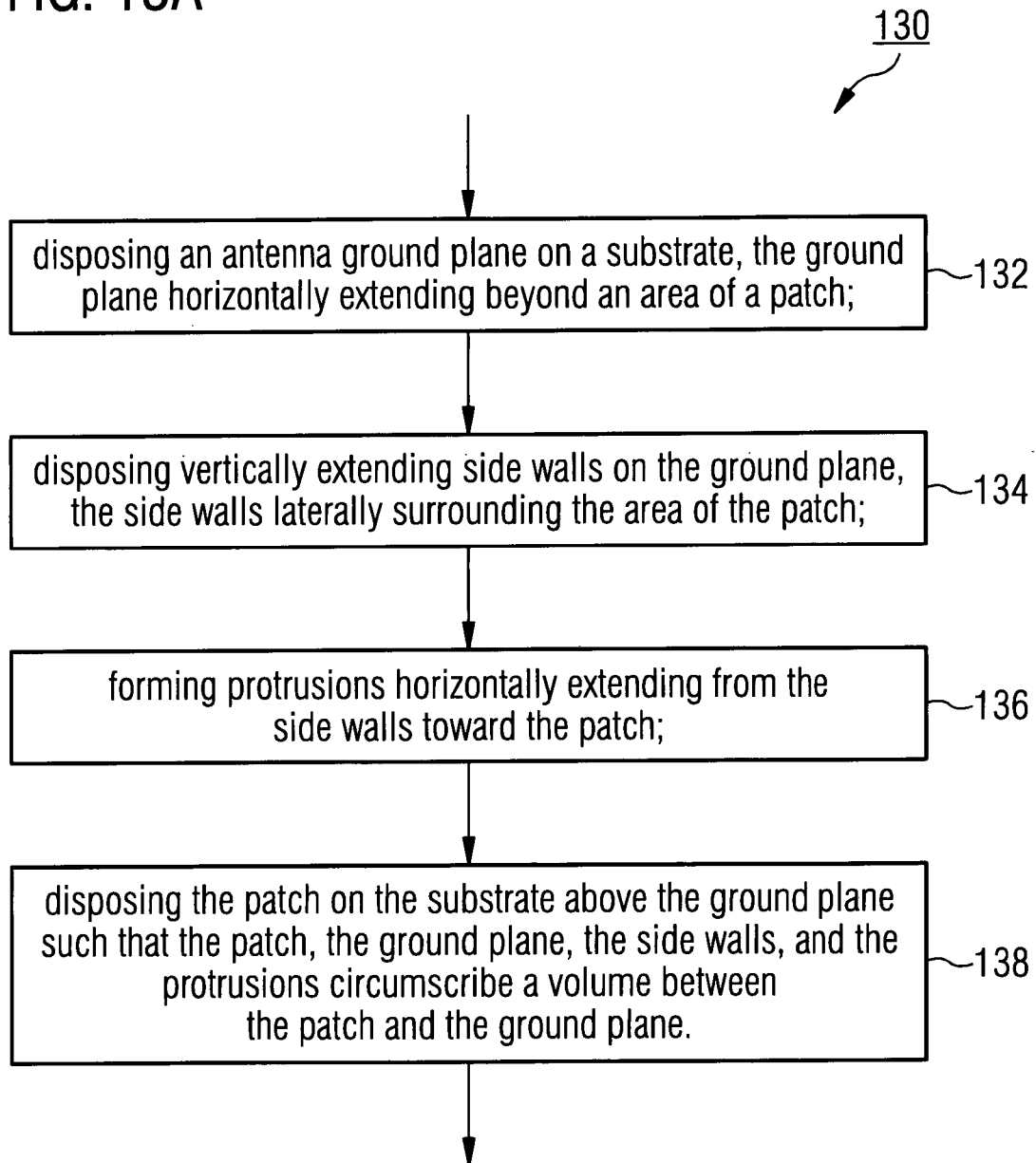


FIG. 13B

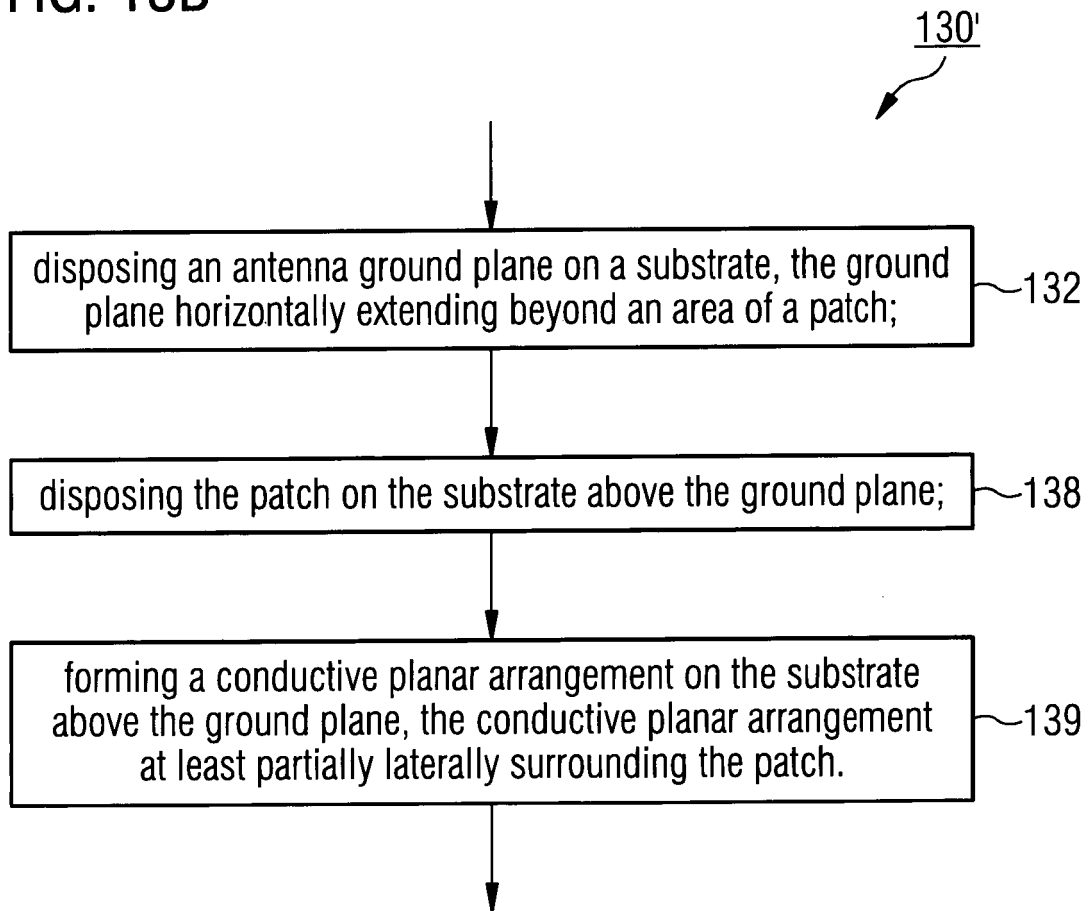


FIG. 14

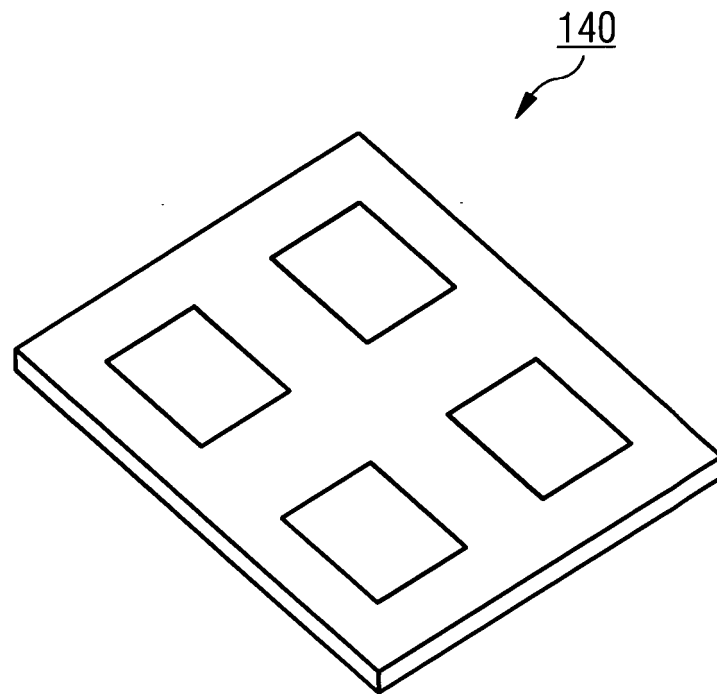
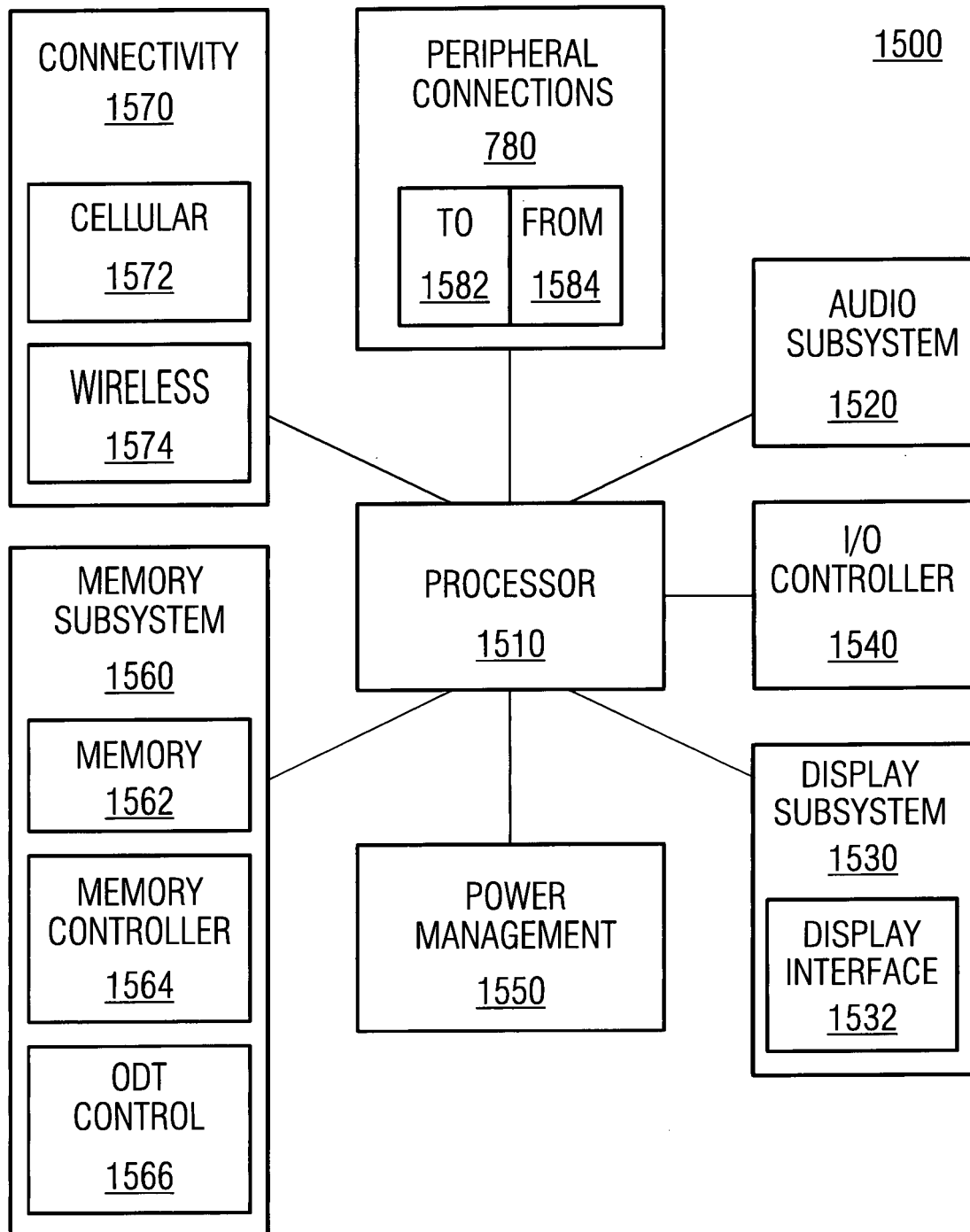


FIG. 15







## EUROPEAN SEARCH REPORT

Application Number  
EP 16 19 1341

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2016/276751 A1 (UEDA HIDEKI [JP]) 22 September 2016 (2016-09-22)	1-13,15	INV. H01Q1/48 H01Q9/04
Y	* abstract; figures 1-5 * * paragraphs [0017] - [0063] *	14	
X	EP 1 775 795 A1 (MA COM INC [US]) 18 April 2007 (2007-04-18) * abstract; figures 1-4 * * paragraphs [0005] - [0041] *	1,3,4,7, 9,13,15	
Y	US 2016/197404 A1 (HASHIMOTO KOH [JP] ET AL) 7 July 2016 (2016-07-07) * abstract; figure 1 *	14	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (IPC)
			H01Q
Place of search		Date of completion of the search	Examiner
The Hague		10 March 2017	Hüschelrath, Jens
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03/02 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 16 19 1341

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.  
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