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(54) **SEMICONDUCTOR DEVICE STRUCTURE WITH NON PLANAR SIDE WALL AND METHOD OF MANUFACTURING USING A DOPED DIELECTRIC**

HALBLEITERBAUELEMENTSTRUKTUR MIT NICHTPLANARER SEITENWAND UND VERFAHREN ZUR HERSTELLUNG MITTELS EINES DOTIERTEN DIELEKTRIKUMS

STRUCTURE DE DISPOSITIF SEMI-CONDUCTEUR AYANT UNE PAROI LATÉRALE NON PLANE ET MÉTHODE DE FABRICATION UTILISANT UN DIÉLECTRIQUE DOTÉ

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- **RÉMY CHARAVEL ET AL: "Tuning of Etching Rate by Implantation: Silicon, Polysilicon and Oxide", AIP CONFERENCE PROCEEDINGS, vol. 866, 1 January 2006 (2006-01-01), pages 325-328, XP055208729, ISSN: 0094-243X, DOI: 10.1063/1.2401523**

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates in general to a semiconductor device and more specifically to a structure of a semiconductor device with a non planar sidewall.

Description of the Related Art

[0002] A semiconductor device such as a transistor utilizes regions of doped semiconductor material to form the structures of the device. For example, a bipolar transistor may include an intrinsic base of doped semiconductor material in contact with an intrinsic collector and intrinsic emitter.

[0003] For instance, US 2008 / 026 623 A1 and WO 2009 / 158 054 A1 disclose high frequency bipolar devices with stacks comprising two different oxide layers with different etch rates. In Rémy Charavel et. al.: "Tuning of Etching Rate by Implantation: Silicon, Polysilicon and Oxide", AIP Conference Proceedings, vol. 866, pp. 325-328, 1 Jan. 2006, DOI: 10.1063/1.2401523 and US 2012 / 0 009 748 A1, ion implantation process is described to alter a wet etching rate due to bond breaking caused by ion implantation process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0005] Figures 1-10 show partial cutaway side views at various stages in the manufacture of a semiconductor device according to one embodiment of the present invention.

[0006] Figure 11 is a partial cut away side view of the semiconductor device shown in Figure 10.

[0007] The use of the same reference symbols in different drawings indicates identical items unless otherwise noted. The Figures are not necessarily drawn to scale.

DETAILED DESCRIPTION

[0008] The present invention concerns a method of forming a semiconductor device according to claim 1, as well as a semiconductor device according to claim 9.

[0009] The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

[0010] Described herein is a semiconductor structure of a semiconductor device that has a side wall that is non planar and that extends farther outward at an upper portion than at a lower portion of the side wall. The semiconductor structure extends underneath a semiconductor layer wherein a top portion of the structure contacts the semiconductor layer. The bottom portion of the semiconductor structure contacts an oppositely doped second semiconductor structure below. In one embodiment, having the upper portion of the semiconductor structure extend out further than the lower portion allows for an increase in the surface area of the semiconductor structure in contact with the semiconductor layer above to reduce the resistance between the two while minimizing the area of the bottom surface of the semiconductor structure to reduce the capacitance with the oppositely doped semiconductor structure below.

[0011] The sidewall is formed by providing an upper portion of a layer of a dielectric material with a faster etch property than a lower portion of the layer. In the claimed invention, the faster etch property is provided by changing the doping profile of the upper portion versus the lower portion by in-situ doping. The semiconductor layer is formed over the layer of dielectric material. An opening is formed in the layer of semiconductor material wherein the layer of dielectric material is exposed through the opening. The layer of dielectric material is isotropically etched through the opening wherein a portion of the layer of dielectric material underneath the layer of semiconductor material is removed. The upper portion of the layer of dielectric material is etched at a faster rate due to the dopants such that a side wall of the remaining portion of the layer of dielectric material underneath the layer of semiconductor material has an upper portion that extends laterally farther from the opening than the lower portion of the wall. Semiconductor material is formed in a void formed by the etching of the layer of dielectric material such that the newly formed semiconductor material contacts the wall underneath the layer of semiconductor material. Thus, the newly formed semiconductor material extends out farther at an upper portion than at a lower portion underneath the semiconductor layer.

[0012] In one embodiment, the newly formed layer of semiconductor material is utilized as an intrinsic base for a bipolar transistor. The semiconductor layer is utilized as base electrode structure that couples the intrinsic base to a base contact. Maximizing the upper portion increases the area of contact between the intrinsic base and the base electrode structure to reduce the resistance between the two structures. In some embodiments, the semiconductor structure below the base is utilized as an intrinsic collector. In some embodiments, reducing the lateral width of the lower portion of the semiconductor structure reduces the capacitance between the intrinsic base and the intrinsic collector below.

[0013] Figure 1 sets forth a partial cutaway side view of a semiconductor wafer according to one embodiment of the present invention. In one embodiment, wafer 101 includes a substrate 103 of bulk monocrystalline silicon with regions implanted with dopants and dielectric isolation structures formed therein. In one embodiment, sub-

strate 103 has a light P type dopant concentration that is formed in-situ with the formation of the substrate or implanted subsequently. Region 107 is formed by implanting substrate 103 with N type conductivity dopants (e.g. arsenic, phosphorous). In one embodiment region 107 is implanted with arsenic ion dopants at a dosage of $2.5e^{14}$ /cm^2 and an energy of 450keV, but may be implanted with other dopants, at other dosages, and/or at other energies in other embodiments. Region 107 is located over region 105 of substrate 103. At this time, the layers above region 107 (e.g. 135) and region 105 retain the light P dopant profile of substrate 103.

[0014] Next, a mask (not shown) is formed over wafer 101 with an opening for implanting collector diffusion region 117. In one embodiment, region 117 is formed by implanting an N type conductivity dopants (e.g. arsenic) into substrate 103. The arsenic ion dopants for forming region 117 are implanted at a dosage of $6.2e^{15}$ /cm^2 and an energy of 90keV, but may be implanted with other dopants, at other dosages, and/or at other energies in other embodiments. Afterwards, the opening in the mask is used to form a shallow trench isolation structure 109 of a dielectric material (e.g. silicon dioxide). The dielectric material may be deposited or thermally grown followed by a planarization of substrate 103. The partial cross sectional view of Figure 1 shows four different portions for each of isolation structure 109 and diffusion region 117. However, at other cross sections of wafer 101, (located into or out of the page from the view of Figure 1), structure 109 and region 117 would be contiguous across the view of Figure 1 (e.g. at end regions of a transistor). However, in other cross sectional views, the portions of structure 109 and/or the portions of region 117 shown in Figure 1 maybe physically separate from each other.

[0015] After the formation of isolation structure 109, collector regions 133, 137, 127, and 131 are formed. 2. Regions 127 and 131 are selectively implanted (through a patterned mask not shown) with a first N type dopant implant followed by a second N type dopant implant to form regions 133 and 137. Regions 133 and 137 are formed by implanting arsenic at a dosage of $6.0e^{15}$ /cm^2 and an energy of 20keV, but may be implanted with other dopants, at other dosages, and/or at other energies. Regions 127 and 131 are formed by implanting phosphorous at a dosage of $1.3e^{15}$ /cm^2 and an energy of 100keV, but may be implanted with other dopants, at other dosages, and/or at other energies. Regions 133 and 137 may also be formed separately at a later step.

[0016] Figure 2 shows a partial cutaway side view of wafer 101 after oxide layer 201 has been formed on substrate 103 and is implanted with dopants. In this example, silicon oxide layer 201 is 600 angstroms thick and is deposited by a TEOS process. However, layer 201 may have other thicknesses, be deposited by other processes, and/or be made of other dielectric materials. For example, layer 201 may be formed by a thermal oxidation process.

[0017] In one example not falling under the scope of the present invention, the implanted dopants 203 are arsenic dopants. In another example not falling under the scope of the present invention, arsenic dopant ions 203 are implanted into the top third of layer 201 as shown by dashed line 205. However, the arsenic dopant ions may be implanted to other depths. The arsenic dopants implanted into the upper portion of layer 201 make the upper portion etch faster than a lower portion of layer 202 during a subsequent selective etching of layer 201. See Figure 5 and its discussion thereof. As an example, the arsenic dopant ions are implanted at a dosage of $5.5e^{15}$ /cm^2 and at an energy of 10keV, but may be implanted at other dosages and/or at other energies as well. For example, the dosage of the dopants may be in the range of 3.0 - $10.0e^{15}$ /cm^2. Alternatively, types of dopants (e.g. phosphorous) may be implanted into layer 201 to increase the etching rate.

[0018] In the claimed invention, the dopants (e.g. arsenic) are introduced in-situ with the formation of layer 201. An arsenic precursor is introduced in the deposition chamber during the latter portion of the deposition of layer 201. The deposition chamber process conditions during the deposition of layer 201 may also be modified to increase the etch rate of the upper portion of layer 201 with respect to the lower portion. For example, a lower deposition temperature during the deposition of the upper portion of layer 201 may result in a less dense oxide with a higher etch in the upper portion of layer 201.

[0019] In other examples not falling under the scope of the present invention, non-conductivity dopants (e.g. xenon, fluorine) may be implanted or introduced into the upper portion of layer 201 to change the etch rate of the upper portion.

[0020] Still in other examples not falling under the scope of the present invention, dopants could be implanted or introduced in-situ in the lower portion of layer 201 so that the lower portion of layer 201 etches at a slower rate than the upper portion. For example, boron may be introduced in the lower portion of layer 201 to slow the etch rate relative to the upper portion of layer 201.

[0021] Figure 3 shows a partial cutaway side view of wafer 101 after a layer 301 of polysilicon is formed on layer 201 followed by the deposition of dielectric layers 303, 305, and 307. Layer 301 may be 600 angstroms thick, but may be of other thicknesses. Layer 301 is doped with conductivity dopants (e.g. boron) either in-situ or ion implanted (e.g. at a dosage of $1.4e^{16}$ /cm^2 and at an energy of 15 keV).

[0022] In the device layer 303 is an oxide layer (e.g. silicon oxide), layer 305 is a nitride layer (e.g. silicon nitride), layer 307 is an oxide layer, layers 303 and 307 have a thickness of 150 angstroms and layer 305 has a thickness of 500 angstrom, but may have other thicknesses.

[0023] Figure 4 shows a partial cutaway side view of wafer 101 after an opening 401 is formed in layers 305, 303, 301, and 307 and a nitride spacer 403 is formed on the opening side walls. The opening is formed by pat-

terning a layer of photo resist or other masking material (not shown) with a corresponding opening and etching layers 301, 303, 305, and 307. Layer 201 is exposed through opening 401. The opening 401 is formed by etching layers 301, 303, 305, and 307 with the appropriate etchants.

[0024] In the example shown, spacer 403 is made of silicon nitride. Spacer 403 is formed by forming a layer of silicon nitride (not shown) over wafer 101 and then performing a reactive ion etch to remove the portions of the silicon nitride layer located on the horizontal surfaces of wafer 101. Oxide layer 307 remains on the horizontal surfaces of wafer 101. Spacer 403 may be made by other processes and/or other materials.

[0025] Figure 5 shows a partial cutaway side view of wafer 101 after a void 500 is formed in layer 201 and collector region 503 is selectively implanted through opening 401. Void 500 is formed in layer 201 by performing a wet etch (isotropic) through opening 401 to etch the exposed portions of layer 201. Alternatively, this wet etch is performed with hydrofluoric (HF) acid. This wet etch etches out the portion of layer 201 underneath spacer 403 and layer 301 in proximity to opening 401. Because the upper portion of layer 201 was implanted with dopants that change the etch rate, the upper portion of layer 201 (that is shown by dashed line 205 etches faster than the lower portion of layer 201 (below line 205). In an example not falling under the scope of the present invention, in which layer 201 is silicon oxide, where the upper portion of layer 201 has been implanted with arsenic at a dosage of $5.5e^{15}$ /cm^2, and where the etchant is HF acid, the upper portion of layer 201 etches at a rate of 1.7 times faster than the undoped portion of layer 201. In an embodiment of the invention, the upper portion of layer 201 is etched at a rate that is in the range of 1.3 to 2.5 times faster than the lower portion. However, the etch rates may be different for different layer materials, different etch chemistries, or different dopants. During the etching of layer 201, layer 307 is also removed.

[0026] In the embodiment shown, the profile of side wall 501 at the upper portion of layer 201 is shown as generally planar along the upper portion above dashed line 205. However, with some embodiments, the sidewall of the top surface of the upper portion of layer 201 may not laterally extend as far away from opening 401 as the sidewall at a lower level of the upper portion. Consequently, the widest portion of void 500 may be at a level in the upper portion of layer 201 just below the level of the top surface of layer 201. The doping profile in the upper portion of layer 201 may be non-uniform, with a higher concentration just below the top surface of layer 201 leading to a higher etch rate and wider void 500 just below the level of the top surface of layer 201.

[0027] Lightly doped (or undoped) region 135 is implanted through opening 401 with N type dopant ions (e.g. arsenic, prosperous) to form an intrinsic collector region 503. For example, the dopant ions may be implanted at an energy of 200keV with a dose of $7.0e^{13}$ /cm^2 such that region 503 extends down to region 107. Afterwards, wafer 101 is annealed to activate the dopants of region 503. The formation of region 503 occurs after the formation of void 500, but may be performed before the formation of void 500 as an alternative.

[0028] Figure 6 shows a partial cutaway side view of wafer 101 after a structure 601 of monocrystalline silicon germanium is grown in void 500 including underneath the portions of layer 301. Structure 601 may be formed by an epitaxial growth process where the silicon germanium is grown from the exposed portions of regions 135, 503 and layer 301 by the epitaxial process. Structure 601 may also be in-situ doped with a P type dopant (e.g. boron) at a dose of $4.7e^{13}$ /cm^2. Structure 601 may also be in-situ doped with carbon at a level of 0.04%. The germanium content varies from 0% to 30% within structure 601. However, structure 601 may also be formed without carbon or germanium (i.e. only P type silicon). Structure 601 can be formed by other processes and/or be made of other materials (e.g. silicon carbon). Prior to forming structure 601, wafer 101 is subjected to an HF precleaning process.

[0029] Figure 7 shows a partial cutaway side view of wafer 101 after the formation of emitter spacer 701 and polysilicon emitter layer 703. In the embodiment shown, spacer 701 is formed on structure 601 next to spacer 403. Spacer 701 may be formed by depositing layers of oxide, nitride, and the oxide (none shown) over wafer 101 and then performing a reactive ion etch to form the spacer. The first deposited oxide layer may be 150 angstroms, the nitride layer 200 angstroms, and the second deposited oxide layer 500 angstroms thick, but the layers may be of other thicknesses. After the reactive ion etching, wafer 101 is subjected to an HF pre-clean that removes from spacer 701, the portion formed from the second deposited oxide layer (not shown) and the remainder of the first deposited oxide layer on structure 601.

[0030] After the formation of spacer 701, a layer 703 of polysilicon is deposited on wafer 101. Layer 703 may have a thickness of 800 angstroms, but may be of other thicknesses.

[0031] Figure 8 shows a partial cutaway side view of wafer 101 after structures of wafer 101 have been patterned twice. The first patterning removes the portions of layers 703, 305 and 303, shown in the view of Figure 8, outside of area 801. Although not shown in the view of Figure 8, similar portions of these layers would remain in other areas of wafer 101, e.g. where other semiconductor devices are being formed on wafer 101. These layers may be patterned by forming a patterned mask (not shown) over wafer 101 with openings outside of area 801. Layers 703, 305, and 303 are then etched (e.g. by a reactive ion etch) through the openings. Intrinsic emitter 803 is formed from poly silicon layer 703 as a result of the etching.

[0032] The second patterning of wafer 101 removes the portions of layers 301 and 201 shown in the view of Figure 7, outside of area 805. Although not shown in the

view of Figure 8, similar portions of these layers would remain in other areas of wafer 101, e.g. where other semiconductor devices are being formed on wafer 101. These layers may be patterned by forming a patterned mask (not shown) over wafer 101 with openings outside of area 805. Layers 301 and 201 are then etched (e.g. by a reactive ion etch to etch layer 301 followed by an HF wet etch to etch layer 201) through the openings. Base electrode structure 807 is formed by the patterning of layer 301. In the cutaway view of Figure 8, structure 807 includes two portions located on the left and right of spacer 701 where spacer 701 and a portion of emitter 803 are located in an opening of structure 807 such that structure 807 surrounds spacer 701.

[0033] At this point, regions 133 and 137 are formed by selectively implanting (through a patterned mask not shown) with an N type dopant implant arsenic at a dosage of $6.0e^{15}$ /cm^2 and an energy of 20keV. Other dopants, at other dosages, and/or at other energies may be implanted, alternatively. Wafer 101 may be annealed at high temperate to activate and diffuse all the dopants (e.g. of intrinsic base structure 601 and intrinsic emitter 803).

[0034] Figure 9 shows a partial cutaway side view of wafer 101 after silicide structures (901, 902, 903, and 905) are formed on the exposed silicon areas of wafer 101. The silicide structures are formed by depositing a layer of metal (e.g. nickel, cobalt) over wafer 101 and heating wafer 101 wherein the metal reacts with the exposed silicon to form the silicide. Afterwards, the unreacted metal is removed. In Figure 9, silicide structure 901 is formed on collector contact region 133, structure 902 is formed on base electrode structure 807, silicide structure 903 is formed on intrinsic emitter 803, and silicide structure 905 is formed on collector contact region 137.

[0035] Figure 10 shows a partial cutaway side view of wafer 101 after the formation of interconnects to the silicide structures. After the formation of silicide structures 901, 902, 903, and 905, a conformal layer 1002 of dielectric material (e.g. nitride) is formed over wafer 101. As an example, layer 1002 has a thickness of 500 angstroms, but may be of other thicknesses. Afterwards a relatively thick layer 1003 of oxide (e.g. formed by a TEOS process) is formed over layer 1002 and planarized (e.g. using chemical mechanical polishing). Openings are then formed in layers 1003 and 1002 to expose silicide structures 901, 902, 903, and 905. A layer of contact material (e.g. tungsten, copper) is formed over wafer 101 including in the openings and then planarized to form isolated plugs 1005, 1007, 1009, 1011, and 1013. The plugs may include barrier metal layers. A second dielectric layer 1015 is formed over wafer 101. Openings are formed in layer 1015 to expose conductive plugs 1005, 1007, 1009, 1011, and 1013. A layer of interconnect conductive material (e.g. copper) is formed over layer 1015 and subsequently planarized to form interconnect 1017, 1019, 1021, 1023, and 1025. The conductive material may include barrier metal layers under the copper. Other examples may have other conductive structures and/or may be formed in other ways. Alternatively, the conductive interconnect structures may electrically couple two or more plugs of plugs 1005, 1007, 1009, 1011, and 1013. Collector plugs 1005 and 1013 may be electrically coupled.

[0036] In the embodiment shown, the transistor formed in wafer 101 is a bipolar NPN transistor where region 503 is the intrinsic collector and structure 601 is the intrinsic base along with intrinsic emitter 803. Intrinsic base structure 601 is electrically accessible from interconnect 1023 via plug 1011, silicide structure 902, and base electrode structure 807 as well as from interconnect 1019 via plug 1007 and silicide structure 902. Intrinsic emitter 803 is accessible by interconnect 1021, plug 1009, and silicide structure 903. Intrinsic collector region 503 is electrically accessible from interconnect 1025 by plug 1013, silicide structure 905, collector contact region 137, and intermediate collector regions 131, 107, and 117. Intrinsic collector region 503 is also electrically accessible from interconnect 1017 by plug 1005, silicide structure 901, collector contact region 133, and intermediate collector regions 127, 107, and 117. Regions 113 and 137 (as well as regions 127 and 131 and silicide structures 901 and 905) are physically separated from each other and are implemented in "finger structures" located along isolation structure 109 opposite each side of collector region 503. However, regions 133 and 137 (as well as regions 127 and 131 and silicide structures 901 and 905) may also be physically connected at other locations of wafer 101 (e.g. at an end region of the transistor).

[0037] The processes herein may be utilized in forming other types of semiconductor devices such as a PNP bipolar transistor, MOSFET, or diode. In one embodiment of forming a PNP bipolar transistor, the P type doped regions and the N type doped regions would be switched from the device of Figure 10.

[0038] After the stage of Figure 10, further interconnect structures may be formed over layer 1015. External connectors such as bond pads would be formed on wafer 101. Afterwards, wafer 101 is singulated into multiple die with each die including one or more transistors as shown in Figure 10. Afterwards, the die are packaged in semiconductor packages (e.g. leaded, leadless, BGA, QFN, QFP, or wafer level package).

[0039] Figure 11 shows a close up view of the partial cutaway view of Figure 10. Figure 11 shows the distance 1111 that intrinsic base structure 601 extends underneath base electrode structure 807. The base resistance between base electrode structure 807 and intrinsic base structure 601 is dependent upon distance 1111, with a greater distance providing for a decrease in resistance. The capacitance between the intrinsic base structure 601 and collector region 503 is dependent upon the width 1113 with a smaller width providing for a decrease in capacitance. Thus, minimizing the width may improve transistor performance in some embodiments by decreasing the base collector capacitance.

[0040] Providing a layer of dielectric material with an upper portion and a lower portion having different etch rate properties enables for the formation of an intrinsic base structure with a wider upper portion to decrease the base resistance and a narrower lower portion to decrease the base collector capacitance. Such an intrinsic base region is formed with a sacrificial dielectric layer having an upper portion and a lower portion that are each etched with the same etchant as opposed to using two layers of different materials. Such methods may reduce the complexity of manufacture of such devices.

[0041] The transistors structures described herein can be formed with BICMOS processes, but may be formed by other processes in other embodiments.

[0042] As used herein, the term "underneath" means directly below. For example, in the view of Figure 11, region 503 is underneath structure 601. Although region 503 is at a level of being below the level of layer 201, it is not underneath layer 201.

[0043] The terms "intrinsic emitter," "intrinsic base," and "intrinsic collector" are the structures of a bipolar device that form the PN junctions (the collector/base junction and the base/emitter junction) of the bipolar transistor.

[0044] In the claimed invention, the forming of the layer of dielectric material includes in-situ doping the upper portion with dopants to provide the upper portion of the layer of dielectric material with a higher concentration of the dopants than the lower portion of the layer of dielectric material to provide the upper portion with the first etch rate property with respect to the second etch rate property. In an example, the semiconductor device includes a second structure of semiconductor material underneath and in contact with the structure of semiconductor material, wherein the structure of semiconductor material has a first conductivity doping profile that is opposite a conductivity doping profile of the second structure of semiconductor material. In an example, the structure of semiconductor material is characterized as an intrinsic base of the semiconductor device and the second structure of semiconductor material is characterized as an intrinsic collector of the semiconductor device. In an example, the second structure of semiconductor material includes conductivity dopants implanted into a layer of semiconductor material through the opening.

[0045] While particular embodiments of the present invention have been shown and described, it will be recognized to those skilled in the art that, based upon the teachings herein, further changes and modifications may be made without departing from the invention as defined by the appended claims.

Claims

1. A method of forming a semiconductor device, comprising:

forming a layer (201) of dielectric material, wherein an upper portion of the layer (201) of dielectric material has a first etch rate with respect to an etchant and a lower portion of the layer (201) of dielectric material has a second etch rate with respect to the etchant;

forming a layer (301) of semiconductor material over the layer (201) of dielectric material;

forming an opening (401) in the layer (301) of semiconductor material and exposing the layer (201) of dielectric material through the opening;

etching with the etchant, the layer (201) of dielectric material through the opening to remove a portion of the layer (201) of dielectric material underneath the layer (301) of semiconductor material with the etchant, wherein the upper portion of the layer (201) of dielectric material is removed by etching with the etchant at a faster rate than the lower portion of the layer (201) of dielectric material is removed by the etching with the etchant such that a remaining side wall (501) of the layer (201) of dielectric material defined by the etching underneath the layer (301) of semiconductor material is non planar with an upper portion of the remaining side wall (501) extending laterally farther from the opening than a lower portion of the remaining side wall (501) extending laterally from the opening;

forming a structure (601) of semiconductor material in a location where the layer (201) of dielectric material was removed by the etching, wherein the structure extends underneath the layer (301) of semiconductor material to contact a bottom surface of the layer (301) of semiconductor material underneath the layer (301) of semiconductor material, the structure having a structure side wall with an upper portion corresponding to the upper portion of the remaining side wall (501) that extends farther underneath the layer (301) of semiconductor material than a lower portion of the structure side wall that corresponds to the lower portion of the remaining side wall (501),

characterized in that forming the layer (201) of dielectric material includes:

in-situ introducing dopants during the latter part of the deposition of said layer of dielectric material (201), to provide the upper portion of the layer (201) of dielectric material with a higher concentration of the dopants (203) than the lower portion of the layer (201) of dielectric material, such that the first etch rate is faster than the second etch rate.

2. The method of claim 1, wherein the semiconductor device includes a second structure (503) of semiconductor material underneath and in contact with the structure (601) of semiconductor material,

wherein the structure (601) of semiconductor material has a first conductivity doping profile that is opposite a conductivity doping profile of the second structure (503) of semiconductor material.

3. The method of claim 2, wherein the structure (601) of semiconductor material is characterized as an intrinsic base of the semiconductor device and the second structure (503) of semiconductor material is characterized as an intrinsic collector of the semiconductor device.

4. The method of claim 2 or claim 3, wherein the second structure (503) of semiconductor material includes conductivity dopants (203) implanted into a layer (301) of semiconductor material through the opening.

5. The method of any preceding claim, wherein the structure (601) of semiconductor material is characterized as an intrinsic base of the semiconductor device wherein a portion of the layer (301) of semiconductor material in which the structure (601) of semiconductor material is located underneath is characterized as a base electrode of the semiconductor device.

6. The method of any preceding claim, wherein the first etch rate is in a range 1.3 to 2.5 times faster than the second etch rate.

7. The method of any preceding claim, wherein the dielectric material is silicon oxide and the dopants (203) include arsenic.

8. The method of any preceding claim, wherein after forming the structure (601) of semiconductor material, forming a third structure (803) of semiconductor material over and in contact with the structure, wherein at least a portion of the third structure (803) is located in the opening, wherein the structure (601) of semiconductor material is characterized as an intrinsic base of the semiconductor device and the third structure (803) is characterized as an intrinsic emitter of the semiconductor device.

9. A semiconductor device, comprising:

a first semiconductor structure (601);
a second semiconductor structure (301) having a first side wall, a portion of the first semiconductor structure (601) extending underneath the second semiconductor structure (301) from the first side wall and having a top surface in contact with a bottom surface of the second semiconductor structure (301) underneath the second semiconductor structure (301);
a layer (201) of dielectric material underneath the second semiconductor structure (301), the layer (201) of dielectric material having a second side wall (501) laterally in contact with the portion of the first semiconductor structure (601), wherein the first semiconductor structure (601) has an upper portion and a lower portion, wherein the upper portion is wider than the lower portion, wherein the upper portion of the first semiconductor structure (601) contacts an upper portion of the layer (201) of dielectric material at the second side wall (501) and the lower portion of the first semiconductor structure (601) contacts a lower portion of the layer (201) of dielectric material at the second side wall (501), wherein the upper portion of the layer (201) of dielectric material etches at a first etch rate with an etchant and the lower portion of the layer (201) of dielectric material etches at a second etch rate with the etchant
characterized in that the upper portion of the layer (201) of dielectric material has a higher concentration of dopants (203) than the lower portion of the layer (201) of dielectric material, such that the first etch rate is faster than the second etch rate, the higher dopant concentration resulting from an in-situ introduction of dopants with the formation of layer (201) during the latter portion of the deposition of the layer of dielectric material (201).

10. A semiconductor device of claim 9, wherein the dielectric material is silicon oxide and the dopants (203) include arsenic.

11. The semiconductor device of claim 9 or claim 10, wherein the first semiconductor structure (601) is characterized as an intrinsic base of a bipolar transistor and the second semiconductor structure (301) is characterized as a base electrode (807) of the semiconductor device, wherein the semiconductor device includes an intrinsic collector (503) located underneath the intrinsic base.

Patentansprüche

1. Verfahren zum Ausbilden einer Halbleitervorrichtung, das Folgendes umfasst:

Ausbilden einer Schicht (201) von dielektrischem Material, wobei ein oberer Abschnitt der Schicht (201) von dielektrischem Material eine erste Ätzgeschwindigkeit in Bezug auf ein Ätzmittel aufweist und ein unterer Abschnitt der Schicht (201) von dielektrischem Material eine zweite Ätzgeschwindigkeit in Bezug auf das Ätzmittel aufweist;
Ausbilden einer Schicht (301) von Halbleiterma-

terial über der Schicht (201) von dielektrischem Material;
Ausbilden einer Öffnung (401) in der Schicht (301) von Halbleitermaterial und Belichten der Schicht (201) von dielektrischem Material durch die Öffnung;
Ätzen der Schicht (201) von dielektrischem Material mit dem Ätzmittel durch die Öffnung, um einen Abschnitt der Schicht (201) von dielektrischem Material unterhalb der Schicht (301) von Halbleitermaterial mit dem Ätzmittel zu entfernen, wobei der obere Abschnitt der Schicht (201) von dielektrischem Material durch Ätzen mit dem Ätzmittel bei einer schnelleren Geschwindigkeit entfernt wird als der untere Abschnitt der Schicht (201) von dielektrischem Material durch das Ätzen mit dem Ätzmittel entfernt wird, so dass eine verbleibende Seitenwand (501) der Schicht (201) von dielektrischem Material, die durch das Ätzen unterhalb der Schicht (301) von Halbleitermaterial definiert wird, nicht planar mit einem oberen Abschnitt der verbleibenden Seitenwand (501) ist, der sich lateral weiter von der Öffnung erstreckt als sich ein unterer Abschnitt der verbleibenden Seitenwand (501) lateral von der Öffnung erstreckt;
Ausbilden einer Struktur (601) von Halbleitermaterial an einer Stelle, an der die Schicht (201) von dielektrischem Material durch das Ätzen entfernt wurde, wobei sich die Struktur unterhalb der Schicht (301) von Halbleitermaterial erstreckt, um mit einer unteren Fläche der Schicht (301) von Halbleitermaterial unterhalb der Schicht (301) von Halbleitermaterial in Kontakt zu sein, wobei die Struktur eine Strukturseitenwand mit einem oberen Abschnitt aufweist, der dem oberen Abschnitt der verbleibenden Seitenwand (501) entspricht, der sich weiter unterhalb der Schicht (301) von Halbleitermaterial als ein unterer Abschnitt der Strukturseitenwand erstreckt, der dem unteren Abschnitt der verbleibenden Seitenwand (501) entspricht,
dadurch gekennzeichnet, dass das Ausbilden der Schicht (201) von dielektrischem Material umfasst:
in-situ Einbringen von Dotierstoffen während des letzteren Teils der Abscheidung der Schicht von dielektrischem Material (201), um den oberen Abschnitt der Schicht (201) von dielektrischem Material mit einer höheren Konzentration der Dotierstoffe (203) als den unteren Abschnitt der Schicht (201) von dielektrischem Material bereitzustellen, so dass die erste Ätzgeschwindigkeit schneller als die zweite Ätzgeschwindigkeit ist.

2. Verfahren nach Anspruch 1, wobei die Halbleitervorrichtung eine zweite Struktur (503) von Halbleitermaterial unterhalb und in Kontakt mit der Struktur (601) von Halbleitermaterial umfasst, wobei die Struktur (601) von Halbleitermaterial ein erstes Leitfähigkeitsdotierungsprofil aufweist, das entgegengesetzt zu einem Leitfähigkeitsdotierungsprofil der zweiten Struktur (503) von Halbleitermaterial ist.

3. Verfahren nach Anspruch 2, wobei die Struktur (601) von Halbleitermaterial als eine intrinsische Basis der Halbleitervorrichtung gekennzeichnet ist, und die zweite Struktur (503) von Halbleitermaterial als ein intrinsischer Kollektor der Halbleitervorrichtung gekennzeichnet ist.

4. Verfahren nach Anspruch 2 oder Anspruch 3, wobei die zweite Struktur (503) von Halbleitermaterial Leitfähigkeitsdotierstoffe (203) umfasst, die in eine Schicht (301) von Halbleitermaterial durch die Öffnung implantiert werden.

5. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Struktur (601) von Halbleitermaterial als eine intrinsische Basis der Halbleitervorrichtung gekennzeichnet ist, wobei ein Abschnitt der Schicht (301) von Halbleitermaterial, in der sich die Struktur (601) von Halbleitermaterial unterhalb befindet, als eine Basiselektrode der Halbleitervorrichtung gekennzeichnet ist.

6. Verfahren nach einem der vorhergehenden Ansprüche, wobei die erste Ätzgeschwindigkeit in einem Bereich von 1,3 bis 2,5 Mal schneller als die zweite Ätzgeschwindigkeit ist.

7. Verfahren nach einem der vorhergehenden Ansprüche, wobei das dielektrische Material Siliziumoxid ist und die Dotierstoffe (203) Arsen umfassen.

8. Verfahren nach einem der vorhergehenden Ansprüche, wobei nach Ausbilden der Struktur (601) von Halbleitermaterial Ausbilden einer dritten Struktur (803) von Halbleitermaterial über und in Kontakt mit der Struktur, wobei sich zumindest ein Abschnitt der dritten Struktur (803) in der Öffnung befindet, wobei die Struktur (601) von Halbleitermaterial als eine intrinsische Basis der Halbleitervorrichtung gekennzeichnet ist und die dritte Struktur (803) als ein intrinsischer Emitter der Halbleitervorrichtung gekennzeichnet ist.

9. Halbleitervorrichtung, die Folgendes umfasst:

eine erste Halbleiterstruktur (601);
eine zweite Halbleiterstruktur (301), die eine erste Seitenwand aufweist, wobei sich ein Abschnitt der ersten Halbleiterstruktur (601) unterhalb der zweiten Halbleiterstruktur (301) von der ersten Seitenwand erstreckt und eine obere Flä-

che aufweist, die in Kontakt mit einer unteren Fläche der zweiten Halbleiterstruktur (301) unterhalb der zweiten Halbleiterstruktur (301) ist;
eine Schicht (201) von dielektrischem Material unterhalb der zweiten Halbleiterstruktur (301), wobei die Schicht (201) von dielektrischem Material eine zweite Seitenwand (501) aufweist, die lateral in Kontakt mit dem Abschnitt der ersten Halbleiterstruktur (601) ist, wobei die erste Halbleiterstruktur (601) einen oberen Abschnitt und einen unteren Abschnitt aufweist, wobei der obere Abschnitt breiter als der untere Abschnitt ist, wobei der obere Abschnitt der ersten Halbleiterstruktur (601) mit einem oberen Abschnitt der Schicht (201) von dielektrischem Material an der zweiten Seitenwand (501) in Kontakt ist und der untere Abschnitt der ersten Halbleiterstruktur (601) mit einem unteren Abschnitt der Schicht (201) von dielektrischem Material an der zweiten Seitenwand (501) in Kontakt ist, wobei der obere Abschnitt der Schicht (201) von dielektrischem Material bei einer ersten Ätzgeschwindigkeit mit einem Ätzmittel ätzt und der untere Abschnitt der Schicht (201) von dielektrischem Material bei einer zweiten Ätzgeschwindigkeit mit dem Ätzmittel ätzt,
dadurch gekennzeichnet, dass der obere Abschnitt der Schicht (201) von dielektrischem Material eine höhere Konzentration von Dotierstoffen (203) als der untere Abschnitt der Schicht (201) von dielektrischem Material aufweist, so dass die erste Ätzgeschwindigkeit schneller als die zweite Ätzgeschwindigkeit ist, wobei die höhere Dotierstoffkonzentration aus einem in-situ Einbringen von Dotierstoffen mit der Ausbildung der Schicht (201) während des letzteren Abschnitts der Abscheidung der Schicht von dielektrischem Material (201) resultiert.

10. Halbleitervorrichtung nach Anspruch 9, wobei das dielektrische Material Siliziumoxid ist und die Dotierstoffe (203) Arsen umfassen.

11. Halbleitervorrichtung nach Anspruch 9 oder Anspruch 10, wobei die erste Halbleiterstruktur (601) als eine intrinsische Basis eines bipolaren Transistors gekennzeichnet ist und die zweite Halbleiterstruktur (301) als eine Basiselektrode (807) der Halbleitervorrichtung gekennzeichnet ist, wobei die Halbleitervorrichtung einen intrinsischen Kollektor (503) umfasst, der sich unterhalb der intrinsischen Basis befindet.

Revendications

1. Procédé de formation d'un dispositif à semi-conducteur, comprenant :

former une couche (201) de matériau diélectrique, où une partie supérieure de la couche (201) de matériau diélectrique a une première vitesse de gravure par rapport à un agent de gravure et une partie inférieure de la couche (201) de matériau diélectrique a une seconde vitesse de gravure par rapport à l'agent de gravure ;
former une couche (301) de matériau semi-conducteur sur la couche (201) de matériau diélectrique ;
former une ouverture (401) dans la couche (301) de matériau semi-conducteur et exposer la couche (201) de matériau diélectrique à travers l'ouverture ;
graver, avec l'agent de gravure, la couche (201) de matériau diélectrique à travers l'ouverture pour enlever une partie de la couche (201) de matériau diélectrique sous la couche (301) de matériau semi-conducteur avec l'agent de gravure, où la partie supérieure de la couche (201) de matériau diélectrique est enlevée par gravure avec l'agent de gravure à une vitesse plus rapide que la partie inférieure de la couche (201) de matériau diélectrique est enlevée par la gravure avec l'agent de gravure de sorte qu'une paroi latérale restante (501) de la couche (201) de matériau diélectrique définie par la gravure sous la couche (301) de matériau semi-conducteur est non plane, avec une partie supérieure de la paroi latérale restante (501) s'étendant latéralement plus loin de l'ouverture qu'une partie inférieure de la paroi latérale restante (501) s'étendant latéralement de l'ouverture ;
former une structure (601) de matériau semi-conducteur dans un emplacement où la couche (201) de matériau diélectrique a été retirée par la gravure, où la structure s'étend sous la couche (301) de matériau semi-conducteur pour entrer en contact avec une surface inférieure de la couche (301) de matériau semi-conducteur sous la couche (301) de matériau semi-conducteur, la structure ayant une paroi latérale de structure avec une partie supérieure correspondant à la partie supérieure de la paroi latérale restante (501) qui s'étend plus loin sous la couche (301) de matériau semi-conducteur qu'une partie inférieure de la paroi latérale de structure qui correspond à la partie inférieure de la paroi latérale restante (501),
caractérisé en ce que la formation de la couche (201) de matériau diélectrique comprend :
l'introduction in situ de dopants pendant la dernière partie du dépôt de ladite couche de matériau diélectrique (201), pour fournir à la partie supérieure de la couche (201) de matériau diélectrique une concentration plus élevée de dopants (203) que la partie inférieure de la couche (201) de matériau diélectrique, de sorte que

la première vitesse de gravure est plus rapide que la seconde vitesse de gravure.

2. Procédé selon la revendication 1, dans lequel le dispositif à semi-conducteur comprend une deuxième structure (503) de matériau semi-conducteur en dessous et en contact avec la structure (601) de matériau semi-conducteur, où la structure (601) de matériau semi-conducteur a un premier profil de dopage de conductivité qui est opposé à un profil de dopage de conductivité de la deuxième structure (503) de matériau semi-conducteur.

3. Procédé selon la revendication 2, dans lequel la structure (601) de matériau semi-conducteur est **caractérisée** comme une base intrinsèque du dispositif à semi-conducteur et la deuxième structure (503) de matériau semi-conducteur est **caractérisée** comme un collecteur intrinsèque du dispositif à semi-conducteur.

4. Procédé selon la revendication 2 ou la revendication 3, dans lequel la deuxième structure (503) de matériau semi-conducteur comprend des dopants de conductivité (203) implantés dans une couche (301) de matériau semi-conducteur à travers l'ouverture.

5. Procédé selon l'une quelconque des revendications précédentes, dans lequel la structure (601) de matériau semi-conducteur est **caractérisée** comme une base intrinsèque du dispositif à semi-conducteur, où une partie de la couche (301) de matériau semi-conducteur dans laquelle la structure (601) de matériau semi-conducteur est située en dessous est **caractérisée** comme une électrode de base du dispositif à semi-conducteur.

6. Procédé selon l'une quelconque des revendications précédentes, dans lequel la première vitesse de gravure se situe dans une plage 1,3 à 2,5 fois plus rapide que la seconde vitesse de gravure.

7. Procédé selon l'une quelconque des revendications précédentes, dans lequel le matériau diélectrique est de l'oxyde de silicium et les dopants (203) comprennent de l'arsenic.

8. Procédé selon l'une quelconque des revendications précédentes, dans lequel, après avoir formé la structure (601) de matériau semi-conducteur, il est formé une troisième structure (803) de matériau semi-conducteur sur la structure et en contact avec celle-ci, où au moins une partie de la troisième structure (803) est située dans l'ouverture, où la structure (601) de matériau semi-conducteur est **caractérisée** comme une base intrinsèque du dispositif à semi-conducteur et la troisième structure (803) est **caractérisée** comme un émetteur intrinsèque du dispositif à semi-conducteur.

9. Dispositif à semi-conducteur, comprenant :

une première structure semi-conductrice (601) ;
une deuxième structure semi-conductrice (301) ayant une première paroi latérale, une partie de la première structure semi-conductrice (601) s'étendant sous la deuxième structure semi-conductrice (301) depuis la première paroi latérale et ayant une surface supérieure en contact avec une surface inférieure de la deuxième structure semi-conductrice (301) sous la deuxième structure semi-conductrice (301) ;
une couche (201) de matériau diélectrique sous la deuxième structure semi-conductrice (301), la couche (201) de matériau diélectrique ayant une deuxième paroi latérale (501) en contact latéral avec la partie de la première structure semi-conductrice (601), où la première structure semi-conductrice (601) a une partie supérieure et une partie inférieure, où la partie supérieure est plus large que la partie inférieure, où la partie supérieure de la première structure semi-conductrice (601) est en contact avec une partie supérieure de la couche (201) de matériau diélectrique au niveau de la deuxième paroi latérale (501) et la partie inférieure de la première structure semi-conductrice (601) est en contact avec une partie inférieure de la couche (201) de matériau diélectrique au niveau de la deuxième paroi latérale (501), où la partie supérieure de la couche (201) de matériau diélectrique est attaquée à une première vitesse d'attaque avec un agent d'attaque et la partie inférieure de la couche (201) de matériau diélectrique est attaquée à une seconde vitesse d'attaque avec l'agent d'attaque,
caractérisé en ce que la partie supérieure de la couche (201) de matériau diélectrique a une concentration plus élevée de dopants (203) que la partie inférieure de la couche (201) de matériau diélectrique, de sorte que la première vitesse de gravure est plus rapide que la seconde vitesse de gravure, la concentration plus élevée de dopants résultant d'une introduction in situ de dopants avec la formation de la couche (201) pendant la dernière partie du dépôt de la couche de matériau diélectrique (201).

10. Dispositif à semi-conducteur selon la revendication 9, dans lequel le matériau diélectrique est de l'oxyde de silicium et les dopants (203) comprennent de l'arsenic.

11. Dispositif à semi-conducteur selon la revendication 9 ou la revendication 10, dans lequel la première structure semi-conductrice (601) est **caractérisée**

comme une base intrinsèque d'un transistor bipolaire, et la deuxième structure semi-conductrice (301) est **caractérisée** comme une électrode de base (807) du dispositif à semi-conducteur, où le dispositif à semi-conducteur comprend un collecteur intrinsèque (503) situé sous la base intrinsèque.

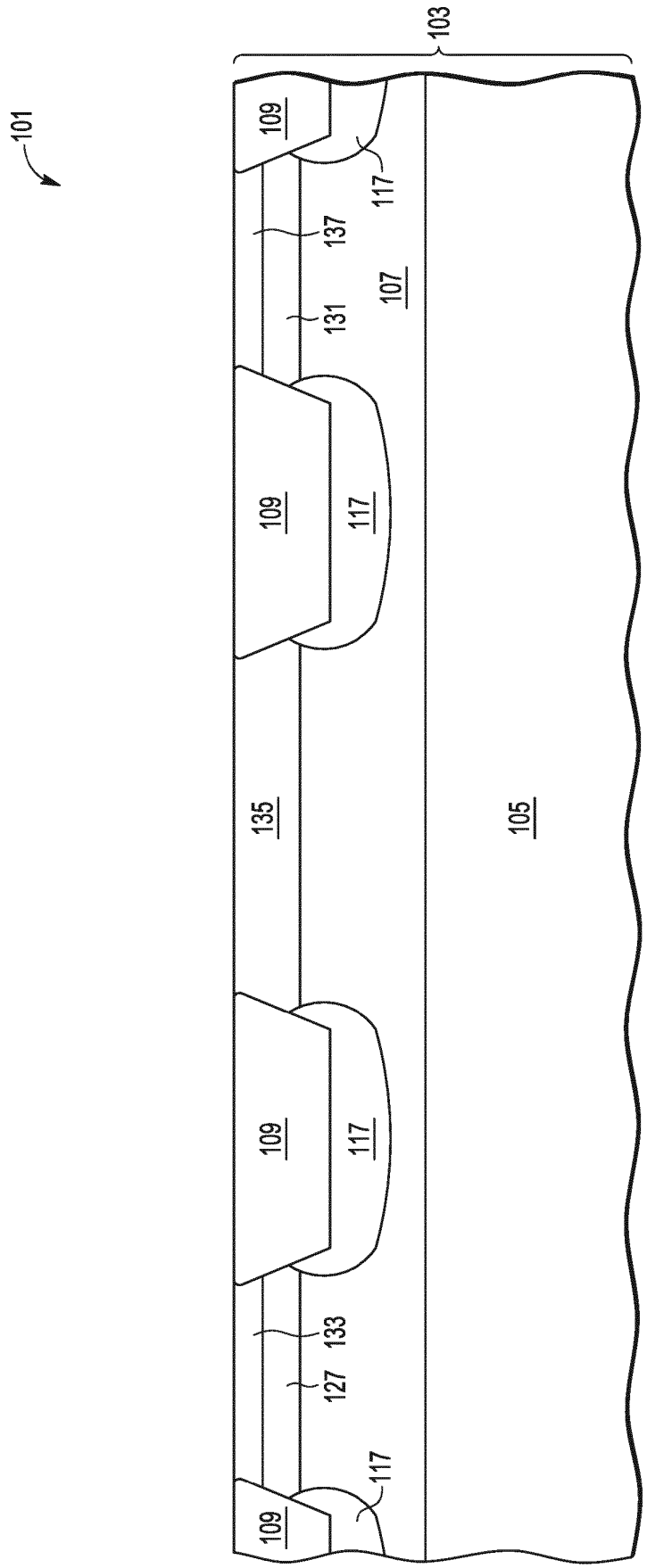
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FIG. 1

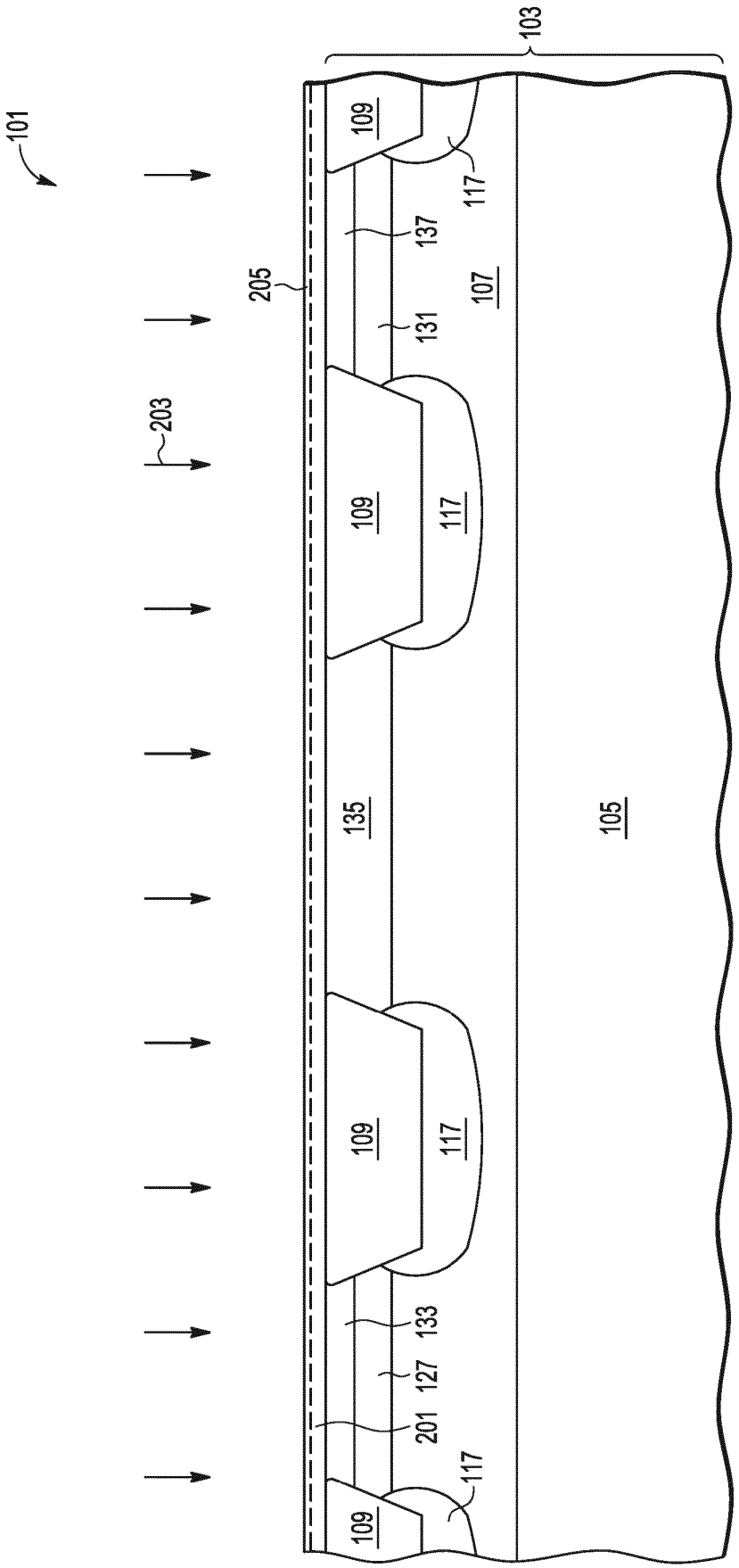
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FIG. 2

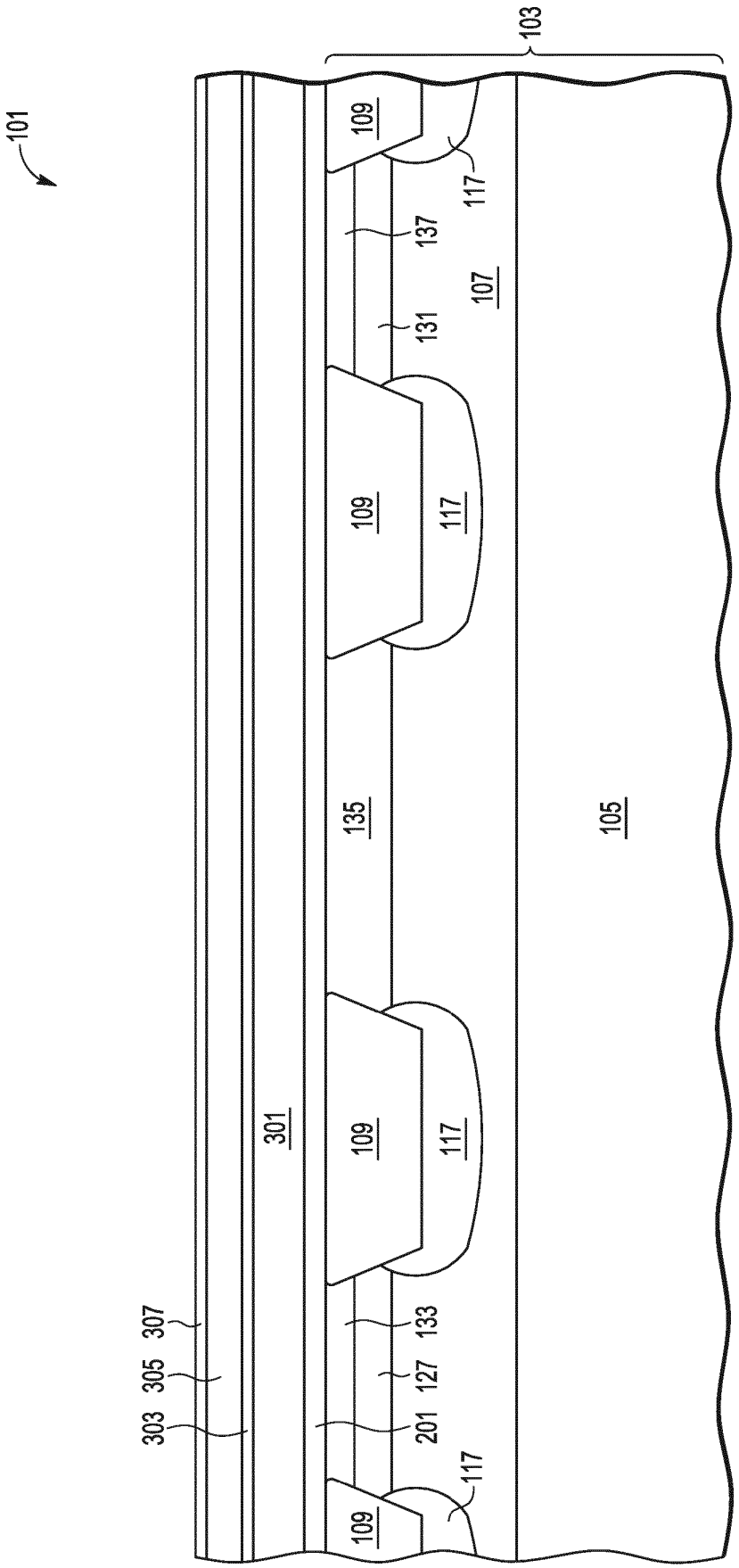
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FIG. 3

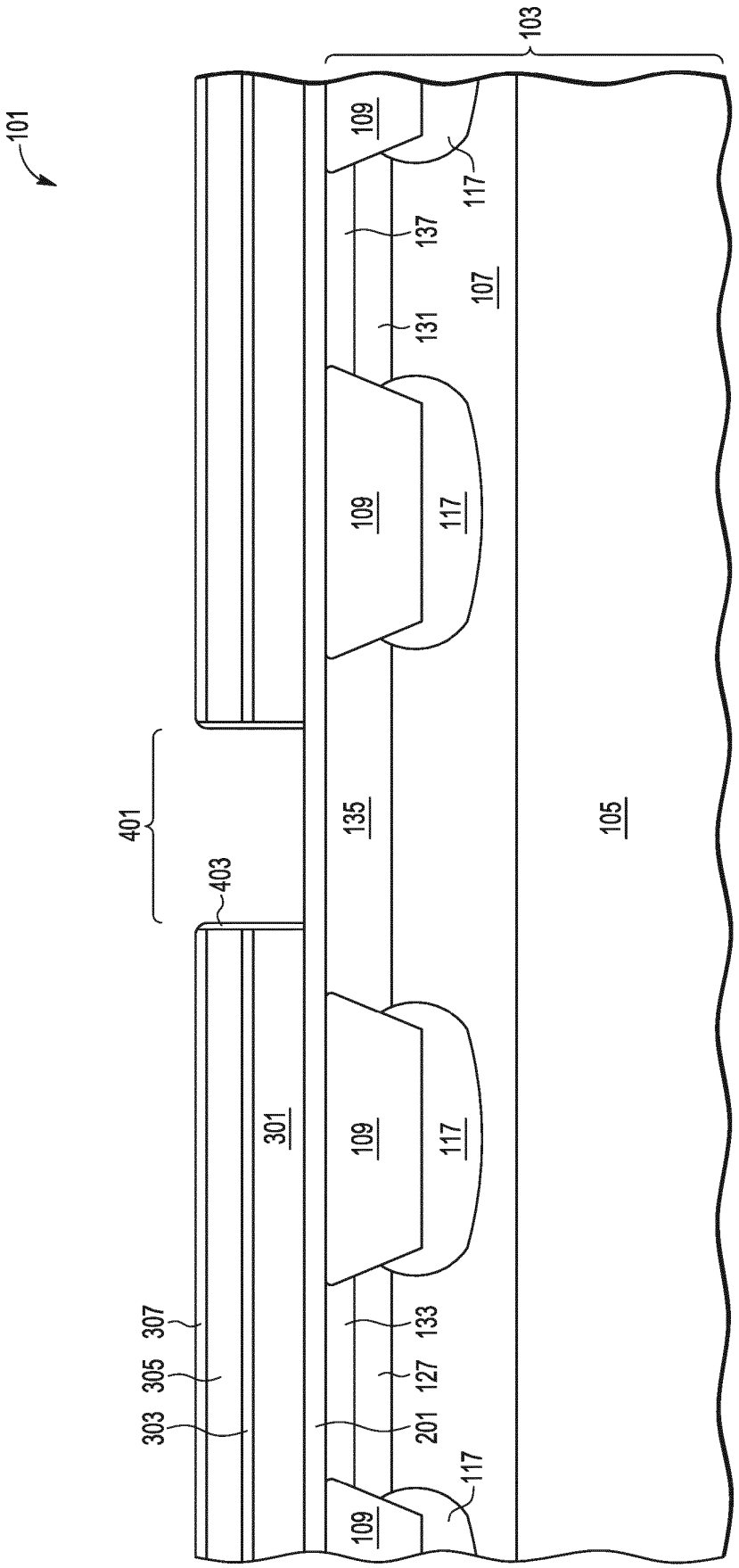
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FIG. 4

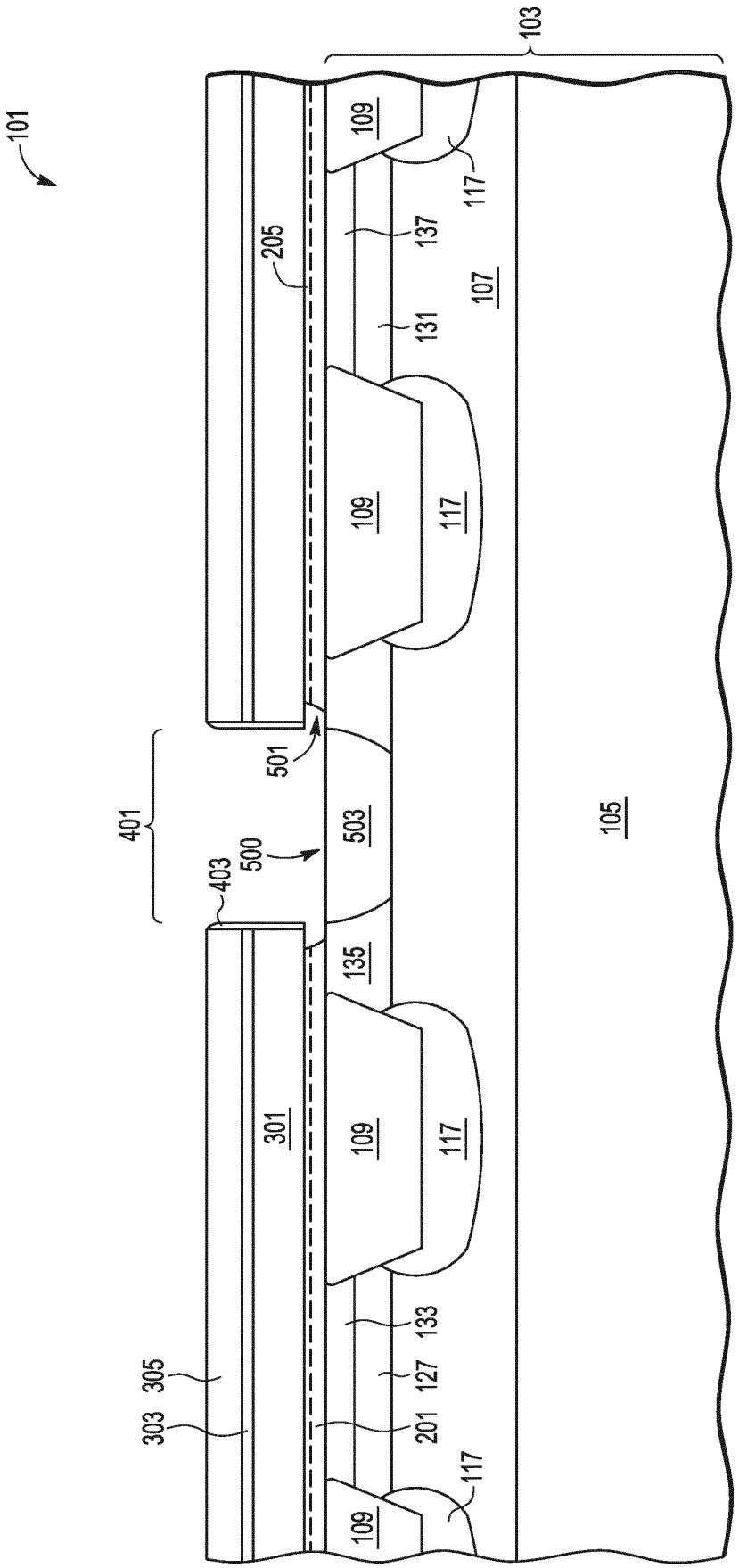
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FIG. 5

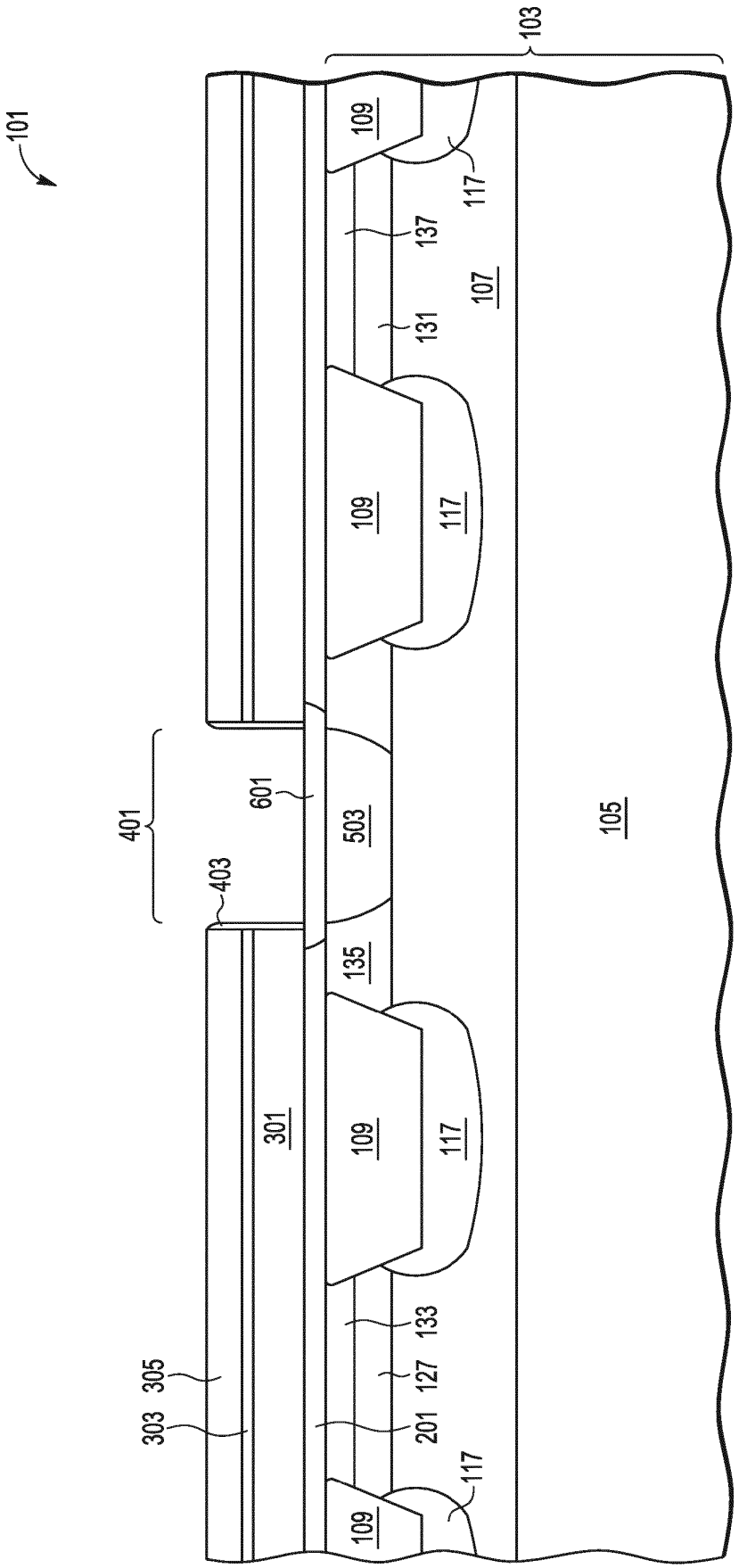
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FIG. 6

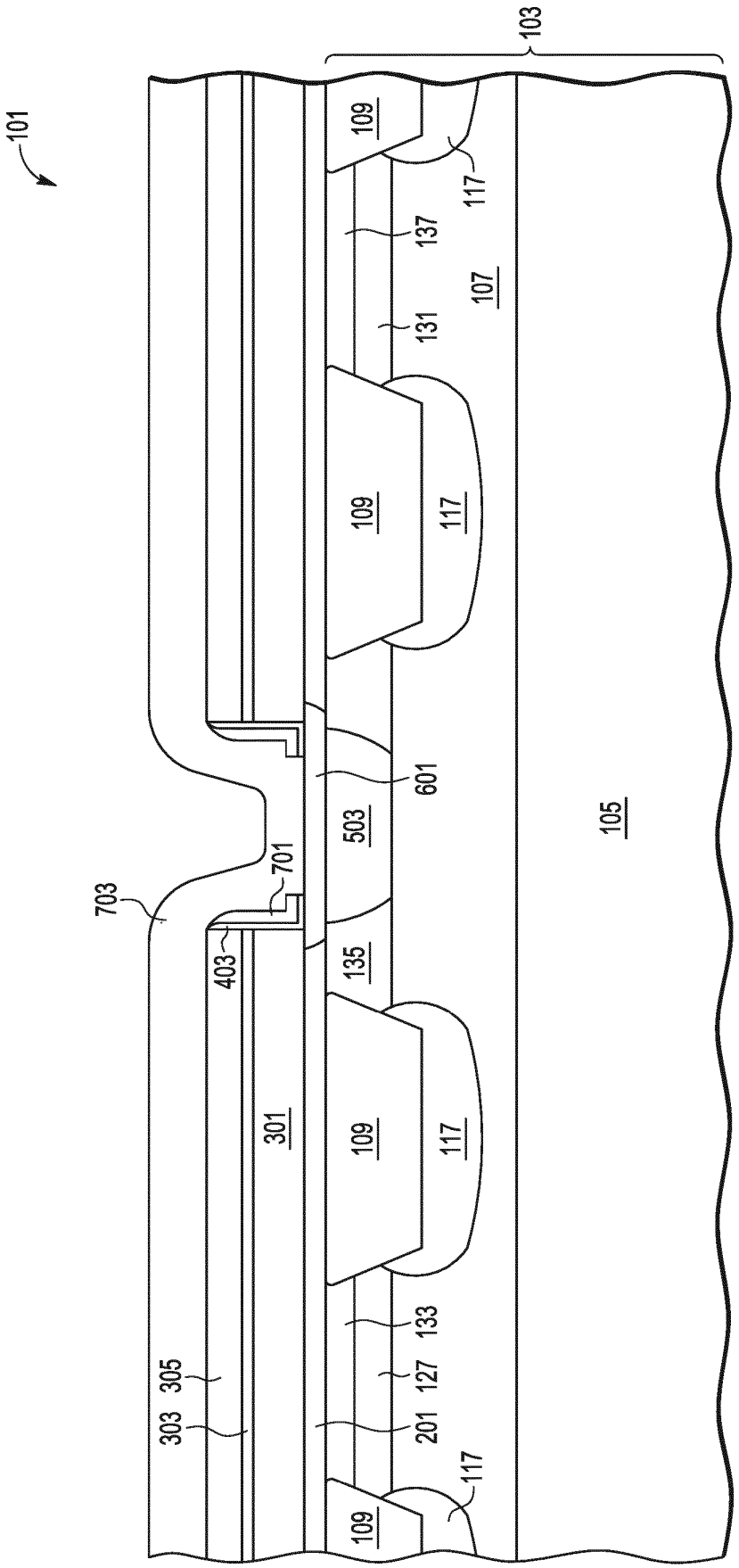
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FIG. 7

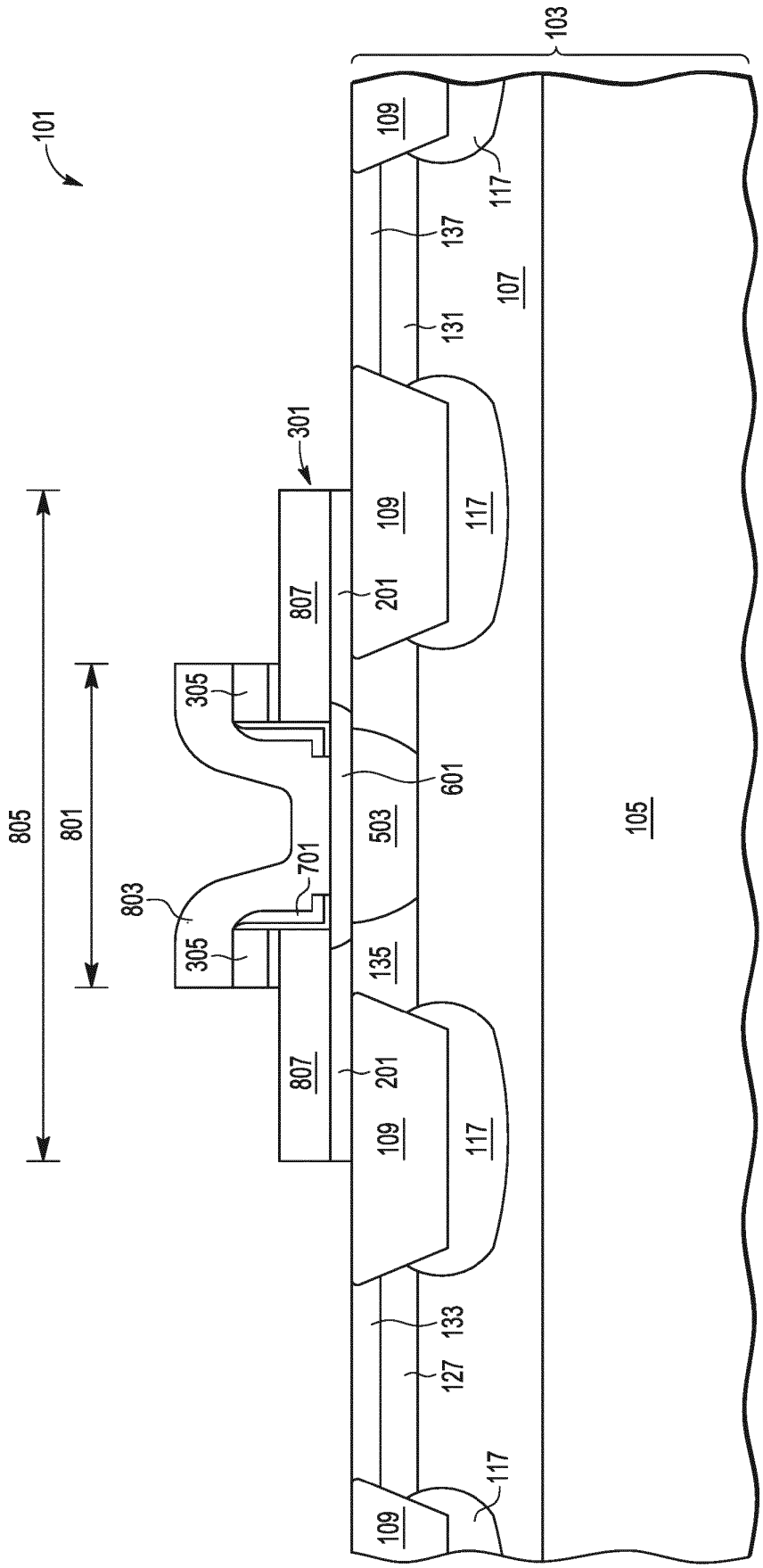
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FIG. 8

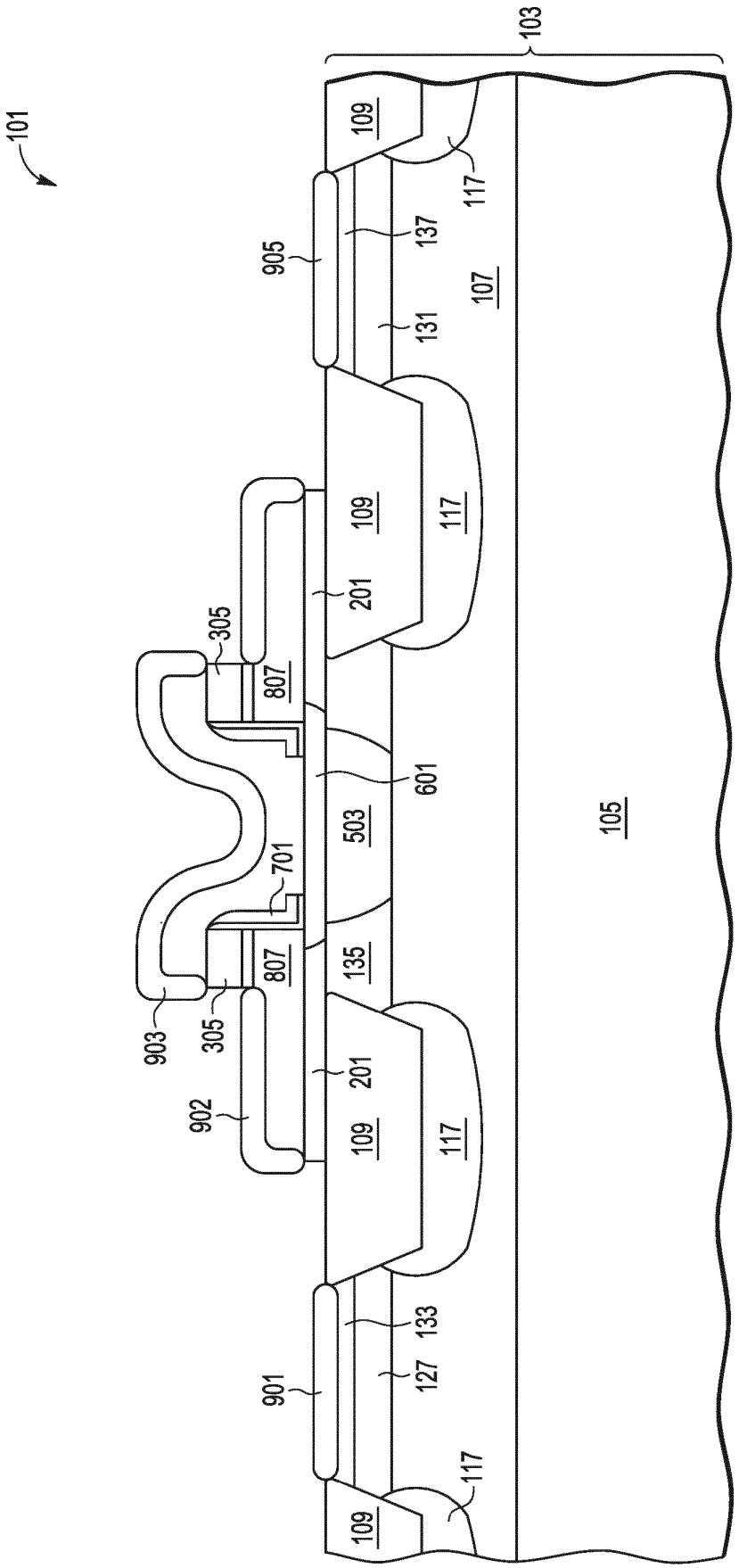
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FIG. 9

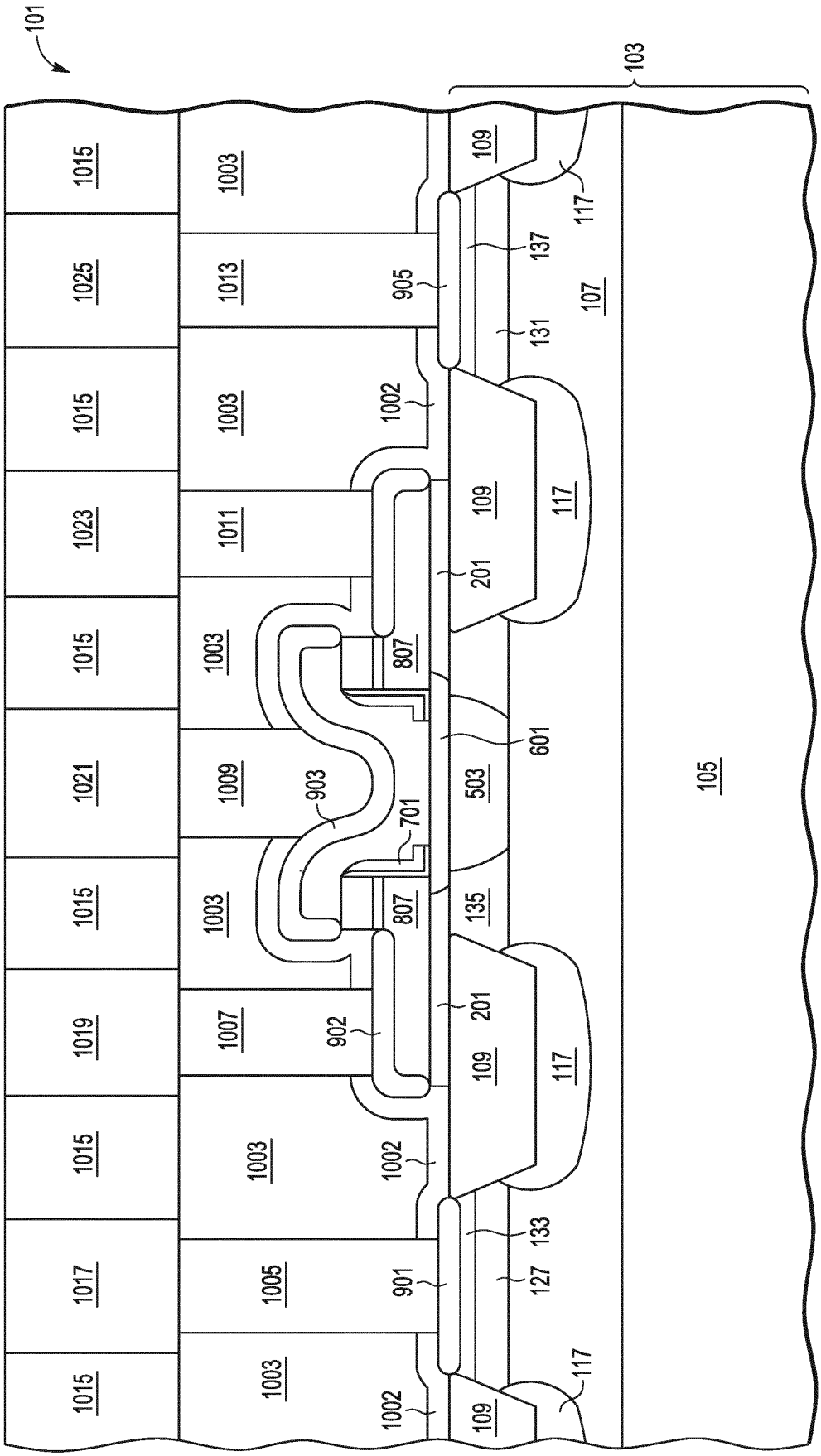
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FIG. 10

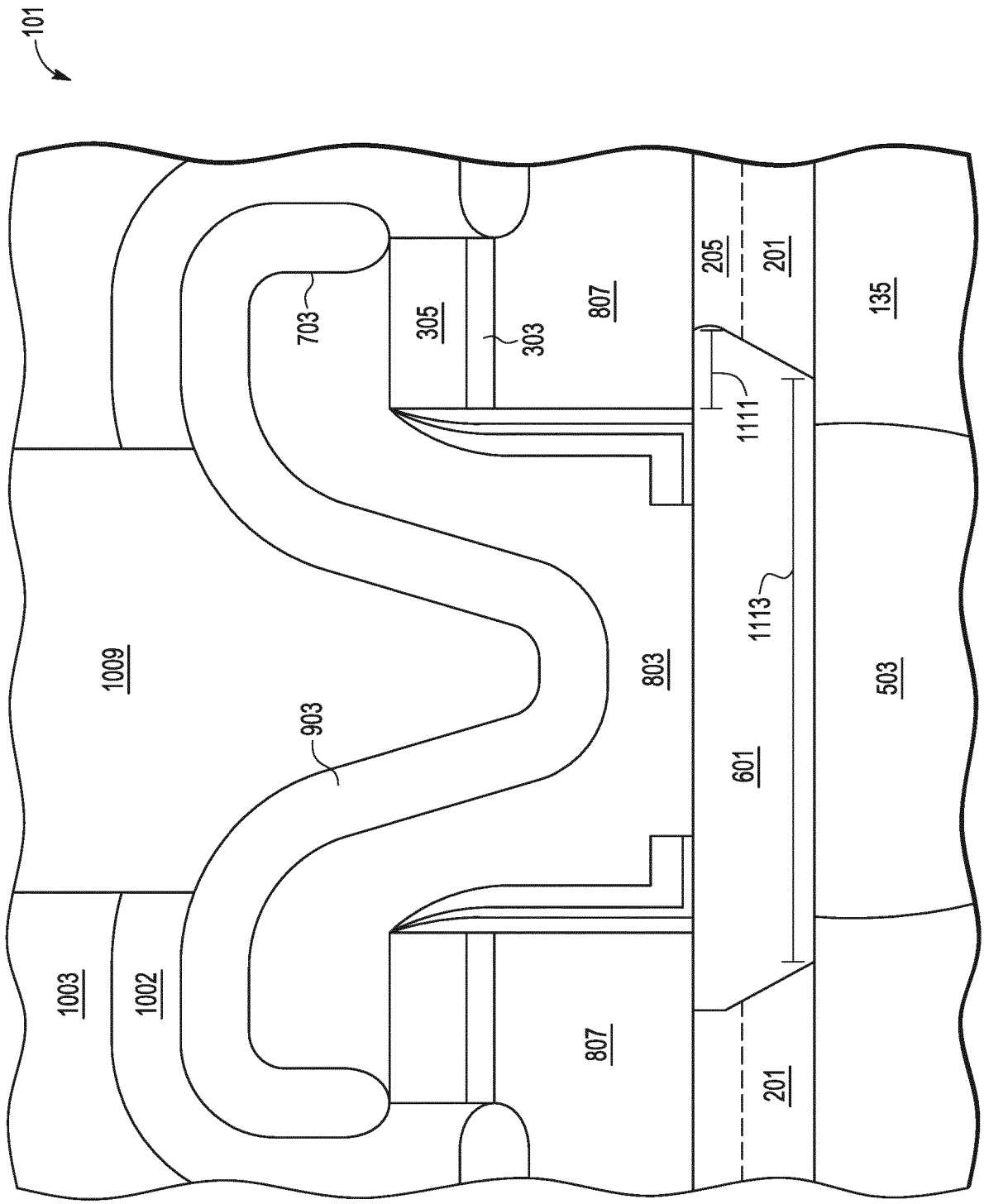
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FIG. 11

REFERENCES CITED IN THE DESCRIPTION

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