(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 3 343 310 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
04.07.2018 Bulletin 2018/27

(51) Int Cl.:
G05F 3/30 *(2006.01)*

(21) Application number: **16207413.2**

(22) Date of filing: **29.12.2016**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
MA MD

(71) Applicant: **ROHM CO., LTD.**
Kyoto 615-8585 (JP)

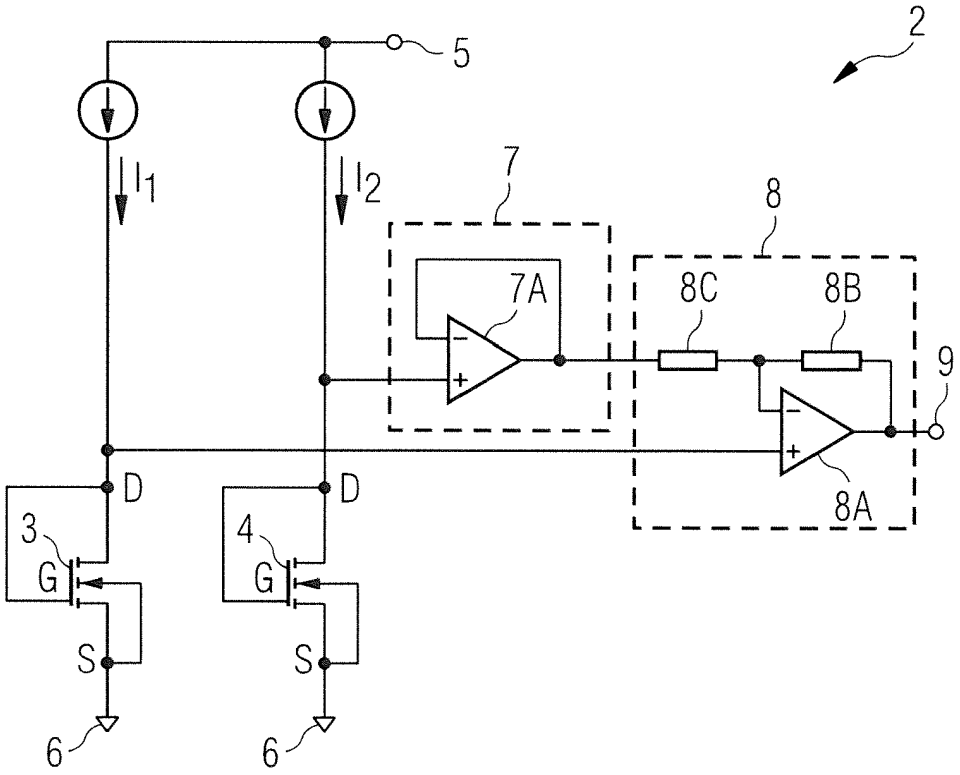
(72) Inventor: **MLADENOVA, Irina**
Kyoto, 615-8585 (JP)

(74) Representative: **Isarpatent**
Patent- und Rechtsanwälte Behnisch Barth Charles
Hassa Peckmann & Partner mbB
Friedrichstrasse 31
80801 München (DE)

(54) **ON-CHIP VOLTAGE GENERATION CIRCUIT**

(57) An on-chip voltage generation circuit (2) integrated on a chip (1), wherein said on-chip voltage generation circuit (2) is adapted to generate a voltage equivalent to a threshold voltage of MOSFETs integrated on said chip (2).

FIG 2



EP 3 343 310 A1

Description

[0001] The invention relates to an on-chip voltage generation circuit integrated on a chip.

[0002] In conventional semiconductor chips, different circuits can be used for on-chip generation of a reference voltage. These conventional on-chip voltage generation circuits can be based on band gaps and/or Zener diodes and comprise different electronic components connected in different configurations comprising transistors, diodes, resistors. Depending on the needed reference voltage, temperature, supply voltage or process variations behaviour, one of the listed above solution can be chosen. A Semiconductor chip comprises in most cases a plurality of integrated MOSFET transistors comprising a threshold voltage. The knowledge of the exact value of the threshold voltage of the MOSFET transistors integrated on the chip is mandatory for trimming the internal chip circuitry for reaching a best performance of the electronic circuits on the chip.

[0003] Accordingly, it is an object of the present invention to provide information about the threshold voltage of MOSFET transistors integrated on a semiconductor chip.

[0004] This object is achieved by an on-chip voltage generation circuit according to the first aspect of the present invention.

[0005] The invention provides according to the first aspect of the present invention an on-chip voltage generation circuit integrated on a chip, wherein said on-chip voltage generation circuit is adapted to generate a voltage equivalent to a threshold voltage of MOSFETs integrated on said chip.

[0006] In a possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the voltage generated by said on-chip voltage generation circuit is equal to the threshold voltage of MOSFETs implemented in the on-chip voltage generation circuit and other MOSFETs of electronic circuits integrated on the same chip.

[0007] In a possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, a bias current is generated by an on-chip bias current generation circuit of said chip depending on the voltage generated by said on-chip voltage generation circuit of said chip.

[0008] In a possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the voltage generated by said on-chip voltage generation circuit is output to a test pin of said chip.

[0009] In a further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, an external measurement circuit is connected to the test pin of the chip and is adapted to measure the voltage generated by said on-chip voltage generation circuit of said chip.

[0010] In a further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, a processing unit is adapted to analyse the voltage measured by said external measurement circuit to derive information about process parameters.

[0011] In a still further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the voltage generated by said on-chip voltage generation circuit is measured by an on-chip measurement circuit integrated on said chip.

[0012] In a still further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the on-chip voltage generation circuit comprises identical MOSFET diode connected transistors operated in a strong inversion and saturation region.

[0013] In a possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, a first electrical current is passed through a first MOSFET of said on-chip voltage generation circuit and a second electrical current is passed through a second MOSFET of said on-chip voltage generation circuit,
wherein the second electrical current is a current replica of the first electrical current and has a current strength being four times the current strength of the first electrical current.

[0014] In a possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the on-chip voltage generation circuit comprises a buffer circuit adapted to buffer a gate-source voltage of the second MOSFET of said on-chip voltage generation circuit.

[0015] In a still further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the on-chip voltage generation circuit comprises a subtracting circuit adapted to subtract the difference voltage between the gate-source voltage of the second MOSFET and first MOSFET from the gate-source voltage of the first MOSFET to generate an output voltage being equivalent to the threshold voltage of the MOSFET on chip transistors implemented in the on-chip voltage generation circuit of said chip.

[0016] In a still further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the buffer circuit comprises a first operational amplifier having an output fed back directly to an inverting input of the first operational amplifier and having a non-inverting input connected to a drain terminal of the second MOSFET of said on-chip voltage generation circuit.

[0017] In a still further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the subtracting circuit comprises a second operational amplifier having an output fed back via a

resistor to an inverting input of said second operational amplifier and having a non-inverting input connected to a drain terminal of the first MOSFET of said on-chip voltage generation circuit.

[0018] In a further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the output of the first operational amplifier is connected via a further resistor to the inverting input of the second operational amplifier.

[0019] In a further possible embodiment of the on-chip voltage generation circuit according to the first aspect of the present invention, the resistance of both resistors is equal.

[0020] The invention further provides according to a second aspect a chip comprising an on-chip voltage generation circuit according to the first aspect of the present invention being adapted to generate an output voltage corresponding to a threshold voltage of MOSFETs integrated in said chip and applied to a test pin of said chip for measurement by an external measurement circuit and/or applied to an internal on-chip measurement circuit integrated on said chip.

[0021] In a possible embodiment of the chip according to the second aspect of the present invention, the chip further comprises at least one on-chip bias current generation circuit integrated on the chip adapted to generate a bias current.

[0022] The invention further provides according to a third aspect a method for deriving information about a threshold voltage of MOSFETs integrated on the chip, the method comprising the steps of:

generating a voltage corresponding to a threshold voltage of MOSFETs integrated on said chip by an on-chip voltage generation circuit of the chip; and
measuring the generated voltage by a measurement circuit.

[0023] In a possible embodiment of the method for deriving information about a threshold voltage of MOSFETs integrated on the chip, the generated voltage measured by said measurement circuit is further analysed to derive information about process parameters.

[0024] In the following, possible embodiments of different aspects of the present invention are described in more detail with reference to the enclosed figures.

Fig. 1 shows a block diagram for illustrating a possible exemplary embodiment of an on-chip voltage generation circuit according to the first aspect of the present invention;

Fig. 2 shows a circuit diagram for illustrating a possible exemplary embodiment of an on-chip voltage generation circuit according to the first aspect of the present invention;

Fig. 3 shows a further circuit diagram for illustrating a further possible implementation of an on-chip voltage generation circuit according to the first aspect of the present invention;

Fig. 4 shows a block diagram for illustrating a further possible exemplary embodiment of an on-chip voltage generation circuit according to the first aspect of the present invention;

Fig. 5 shows a further diagram for illustrating a further possible exemplary embodiment of an on-chip voltage generation circuit according to the first aspect of the present invention;

Fig. 6 shows a flowchart for illustrating a possible exemplary embodiment of a method for deriving information about a threshold voltage according to the third aspect of the present invention;

Fig. 7 shows a further flowchart for illustrating a further possible exemplary embodiment of a method for deriving information according to the third aspect of the present invention.

[0025] As can be seen in Fig. 1, a chip 1 comprises in the illustrated embodiment at least one on-chip voltage generation circuit 2 integrated on the chip 1. The chip 1 can be a semiconductor chip fabricated in a manufacturing process and can comprise a plurality of electronic circuits each having MOSFET transistors. The MOSFET transistors integrated on the chip 1 can be characterized by their threshold voltage V_{th}. The threshold voltage V_{th} of the MOSFET transistors depends on process parameters and can vary from chip to chip and from wafer to wafer. PCM data provided during the fabrication process do not always correspond to the real values of the threshold voltage because they can be measured for instance on a test structure. Further, the measurement conditions for measuring the threshold voltage V_{th} may not correspond to the conditions which the integrated circuit 1 faces during normal usage or operation. The knowledge of the threshold voltage V_{th} of the MOSFETs integrated on the chip 1 is necessary for trimming any internal chip circuitry of electronic components or electronic circuits integrated on the same chip for reaching an optimal performance of the electronic circuits. As can be seen in the embodiment illustrated in Fig. 1, the chip 1 comprises an on-chip voltage

generation circuit 2, the on-chip voltage generation circuit 2 which is fabricated in the same manufacturing process as the remaining electronic circuits of the chip 1 and is implemented by circuits comprising the same MOSFETs as used in the remaining electronic circuits of the chip 1. The on-chip voltage generation circuit 2 integrated on the chip 1 is configured to generate an output voltage V_{out} equivalent to the threshold voltage V_{th} of the MOSFETs implemented on the chip 1. In the illustrated embodiment of Fig. 1, the chip 1 comprises a single on-chip voltage generation circuit 2. In further possible embodiments, the chip 1 can comprise more than one on-chip voltage generation circuit 2 located at different positions on the integrated chip 1. The voltage V_{out} generated by the on-chip voltage generation circuit 2 is equivalent to the threshold voltage V_{th} of MOSFETs implemented in the on-chip voltage generation circuit 2 itself and equivalent to the threshold voltage of MOSFETs used in other electronic circuits integrated on the same chip 1. In a possible embodiment, the generated voltage of the on-chip voltage generation circuit 2 can be passed to an associated test pin of the chip 1. The voltage V_{out} generated by the on-chip voltage generation circuit 2 applied to the test pin of the integrated circuit 1 can then be measured by an external measurement circuit to derive information about the threshold voltage V_{th} of the MOSFETs integrated on the chip 1. The output threshold voltage applied to the test pin of the integrated chip 1 can also be used for an external power supply and/or generating a bias current used for the electronic circuitry within the integrated chip 1. The measured threshold voltage V_{th} of the MOSFETs integrated on the chip 1 further allows a designer of the integrated chip 1 to use the information for debugging faults in the chip design.

[0026] Fig. 2 shows a possible embodiment of an on-chip voltage generation circuit 2 integrated on a chip 1. In the illustrated embodiment of Fig. 2, the on-chip voltage generation circuit 2 comprises two identical MOSFET transistors 3, 4. The MOSFETs 3, 4 are connected in diode configuration as load of a corresponding PMOS current source as illustrated in Fig. 2. The MOSFETs 3, 4 are operated in a strong inversion and saturation region. As illustrated in Fig. 2, the gate terminals G of the MOSFETs 3, 4 are connected directly to the respective drain terminals D of the MOSFETs 3, 4. Further, the source terminals S of the MOSFETs 3, 4 are connected to a common ground 6. As shown in Fig. 2, a first electric current I1 is passed through the first MOSFET 3 and a second electrical current I2 is passed to the second MOSFET 4 of the on-chip voltage generation circuit 2. The second electrical current I2 is in a possible embodiment a current replica of the first electrical current I1 and comprises a current strength being four times the current strength of the first electrical current I1. In the illustrated embodiment of Fig. 2, the on-chip voltage generation circuit 2 further comprises a buffer circuit 7 adapted to buffer a gate-source voltage V_{gs} of the second MOSFET 4 of the on-chip voltage generation circuit 2. The on-chip voltage generation circuit 2 further comprises in the illustrated embodiment a subtracting circuit 8 implemented by an inverting amplifier adapted to subtract the difference voltage between the gate-source voltage of the second MOSFET and first MOSFET from the gate-source voltage of the first MOSFET 4 to generate an output voltage V_{out} being equivalent to the threshold voltage V_{th} of the all identical MOSFETs on the chip 1 as the threshold voltage is a common parameter for all identical MOSFETs in one chip. The generated output voltage V_{out} is applied in the illustrated embodiment to an output terminal 9 of the on-chip voltage generation circuit 2.

[0027] The working principle of the on-chip voltage generation circuit 2 as illustrated in Fig. 2 is described in the following. The MOSFET transistors 3, 4 operate in a strong inversion and saturation region. The electrical current flowing through such a MOSFET device I_{dsat} can be described by the following formula:

$$\text{Idsat} = \frac{\mu * Cox}{2} * \frac{W}{L} * (Vgs - Vth)^2 * (1 + \lambda * Vds) \quad (1)$$

wherein

μ is the charge carrier effective mobility,
W is the gate width,
L is the gate length,
C_{ox} is the gate oxide capacitance per unit area,
V_{th} is the transistor threshold voltage,
V_{gs} is the voltage applied to the gate terminal,
V_{ds} is the drain-source voltage and
λ is the channel length modulation parameter.

[0028] From equation (1), the gate-source voltage V_{gs} of the MOSFET transistor can be derived as follows:

$$Vgs = \sqrt{\frac{2 * Idsat * L}{\mu * Cox * W * (1 + \lambda * Vds)}} + Vth \quad (2)$$

[0029] The two identical MOSFET transistors 3, 4 are connected in diode configuration. Through the first MOSFET 3, a first current I1 is passed through. Through the MOSFET 4, a second electrical current I2 is passed having a current strength being four times the current strength of the first electrical current I1:

$$I2 = 4 * I1 \tag{3}$$

[0030] Based on the formula (2), the gate-source voltage of MOSFET 3 can be described as follows:

$$Vgs_1 = \sqrt{\frac{2*I_1*L}{\mu*Cox*W*(1+\lambda*Vds_1)}} + Vth \tag{4}$$

[0031] From the configuration illustrated in Fig. 2, the drain-source voltages V_{ds} of both MOSFET transistors 3, 4 can be set to be equal:

$$Vds1 = Vds2 \tag{5}$$

[0032] Accordingly,

$$Vgs_2 = 2 * \sqrt{\frac{2*I_1*L}{\mu*Cox*W*(1+\lambda*Vds_2)}} + Vth = Vgs_1 + \sqrt{\frac{2*I_1*L}{\mu*Cox*W*(1+\lambda*Vds_2)}} \tag{6}$$

[0033] The drain-source voltages V_{DS} of both MOSFET transistors 3, 4 can be set to be equal (see equation (5)) or the MOSFET transistors 3, 4 can be designed such that they are long enough to make the channel length modulation parameter negligible. For this case, one can replace

$$\sqrt{\frac{2*I_1*L}{\mu*Cox*W*(1+\lambda*Vds_1)}} = \sqrt{\frac{2*I_2*L}{\mu*Cox*W*(1+\lambda*Vds_2)}} \; with \; Vov \tag{7}$$

to get:

$$Vgs_1 = V_{ov} + Vth, \; Vgs_2 = V_{ov} + V_{ov} + Vth \; or \; Vgs_2 - Vgs_1 = V_{ov} \tag{8}$$

[0034] Accordingly, the gate-source voltage V_{gs1} of the first MOSFET 3 is higher than the threshold voltage V_{th} by voltage V_{0v} and the gate-source voltage V_{gs2} of the second MOSFET transistor 4 is higher than V_{th} by twice the voltage V_{0v}. Consequently, the gate-source voltage V_{gs1} of the first MOSFET transistor 3 differs from the gate-source voltage V_{gs2} of the second MOSFET transistor 4 by the voltage V_{0v}. Consequently, by calculating the difference between the gate-source voltage V_{gs2} of the second MOSFET 4 and the gate-source voltage V_{gs1} of the first MOSFET 3, the threshold voltage V_{th} of the MOSFETs 3, 4 is achieved. This is performed by means of the buffer circuit 7 and the subtracting circuit 8 as illustrated in the embodiment of Fig. 2. The buffer circuit 7 can be implemented by an operational amplifier as illustrated in Fig. 2 and acts as a buffer for the gate-source voltage V_{gs2} of the second MOSFET 4. The subtracting circuit 8 comprises an operational amplifier 8A. The subtracting circuit 8 is adapted to subtract the difference voltage between the gate-source voltage of the second MOSFET 4 and first MOSFET 3 to generate an output voltage V_{out} being equivalent to the threshold voltage V_{th} of the on-chip MOSFET transistors.The on-chip voltage generation circuit 2 does output the output voltage V_{out} at its output terminal 9. The threshold voltage V_{th} of the MOSFETs 3, 4 also corresponds to the threshold voltages V_{th} of other MOSFETs integrated on the same chip 1. In the illustrated embodiment of Fig. 2, the buffer circuit 7 comprises a first operational amplifier 7A having an output being fed back directly to an inverting input (-) of the first operational amplifier 7A and having a non-inverting input (+) connected directly to the drain terminal D of the second MOSFET 4 of the on-chip voltage generation circuit 2. Further, in the illustrated embodiment of Fig. 2, the subtracting circuit 8 comprises a second operational amplifier 8A having an output fed back via a resistor 8B to an

inverting input (-) of the second operational amplifier 8A and having a non-inverting input (+) being connected directly to the drain terminal D of the first MOSFET 3 of the on-chip voltage generation circuit 2 as illustrated in Fig. 2. As can be seen in Fig. 2, the output of the first operational amplifier 7A of the buffer circuit 7 is connected via a further resistor 8C of the subtracting circuit 8 to the inverting input (-) of the second operational amplifier 8A.

[0035] In a possible embodiment, the resistance of the resistor 8C is equal to the resistance of the resistor 8B. In this embodiment, the output voltage V_{out} of the on-chip voltage generation circuit 2 is given as follows:

$$V_{out} = Vgs_1 - V_{0v} * (R/R) = Vth$$

[0036] Fig. 3 shows a possible exemplary embodiment of an on-chip voltage generation circuit 2 according to the first aspect of the present invention.

[0037] In the illustrated embodiment of Fig. 3, the on-chip voltage generation circuit 2 comprises bias terminals 10, 11, 12 used for operating the on-chip voltage generation circuit 2. The first bias terminal 10 provides a bias for generating a current replica. The current replica is generated by the current mirroring PMOS transistors 13, 14 as illustrated in Fig. 3. The second bias terminal 11 is adapted to receive a bias for the cascoding PMOS transistors 15, 16. The on-chip voltage generation circuit 2 further comprises a third bias terminal 12 for cascoding NMOS transistors 17, 18 as shown in Fig. 3. The on-chip voltage generation circuit 2 shown in Fig. 3 comprises a buffer circuit 7 having a first operational amplifier 7A comprising a non-inverting input connected to the cascaded diode connected NMOS FET 4. Further, the on-chip voltage generation circuit 2 comprises a subtracting circuit 8 including an operational amplifier 8A having a non-inverting input connected to the cascaded diode connected NMOS FET 3. The generated output voltage V_{out} output at the output terminal 9 of the on-chip voltage generation circuit 2 is equivalent to the threshold voltages V_{th} of the used NMOS transistors.

[0038] Fig. 4 shows a possible further embodiment of an integrated chip 1. In the illustrated embodiment, the output voltage V_{out} generated by the on-chip voltage generation circuit 2 which is equivalent to the threshold voltage V_{th} of the MOSFETs implemented on the chip 1 is applied internally to an on-chip bias current generation circuit 19. The on-chip bias current generation circuit 19 is also integrated on the chip 1 and is adapted to generate bias currents I_{BIAS}. In the illustrated exemplary embodiment, the generated bias current I_{BIAS} can be supplied to a further electronic circuitry 20 also integrated on the chip 1. Further, in the illustrated embodiment of the chip 1 as shown in Fig. 4, the chip 1 comprises an integrated measurement circuit 21 adapted to measure and/or to store the generated voltage output by the integrated on-chip voltage generation circuit 2. The measured voltage can then be output via an external pin 22 of the chip 1 or used for other purposes.

[0039] In a preferred embodiment, the on-chip voltage generation circuit 2 applies the generated voltage V_{th} directly to a test pin 23 of the integrated circuit 1 as illustrated in Fig. 5. The integrated circuits implemented on chip 1 can comprise a further electronic circuitry besides the on-chip voltage generation circuit 2 as illustrated in Fig. 5. The voltage generated by the on-chip voltage generation circuit 2 is applied to the test pin 23 of the chip 1. In a possible embodiment, an external measurement circuit 24 can be connected to the test pin 23 of the chip 1, wherein the external measurement circuit 24 is adapted to measure the voltage generated by the on-chip voltage generation circuit 2 of the chip 1. In a possible embodiment, the external measurement circuit 24 can be integrated in a test apparatus 25 having a processing unit 26 adapted to analyse the voltage measured by the external measurement circuit 24 to derive information about process parameters. These process parameters can for instance comprise manufacturing process parameters of manufacturing processes for manufacturing the integrated chip 1. The information or data derived by the processing unit 26 can be output to a user such as a chip designer and/or to an operator during a manufacturing process and/or during quality control. Further, the information and data derived by the processing unit 26 can be used to generate automatically control signals in a manufacturing process for fabricating electronic chips 1. The monitoring or test apparatus 25 as illustrated in Fig. 5 can be used to monitor and/or control a manufacturing process. Further, the apparatus 25 can be used for supporting a chip designer when designing an electronic chip 1. In the illustrated embodiment, the external measurement circuit 24 integrated in the apparatus 25 monitors a single voltage generated by a single on-chip voltage generation circuit 2 of the chip 1. In a further possible embodiment, the integrated chip 1 can comprise several on-chip voltage generation circuits 2 located at different locations each connected to an associated test pin 23 to output a voltage monitored and evaluated by the test apparatus 25. In a further possible embodiment, the processing apparatus 26 can also generate control signals in response to the measured voltage being equivalent to the threshold voltage used for trimming a further internal chip circuitry of the integrated chip 1.

[0040] Fig. 6 shows a flowchart of a possible exemplary embodiment of a method for deriving information about a threshold voltage of MOSFETs integrated on a chip 1 according to a further aspect of the present invention.

[0041] In a first step S1, a voltage is generated corresponding to a threshold voltage of MOSFETs integrated on the chip 1 by an on-chip voltage generation circuit 2 of the chip 1. In a further step S2, the generated voltage is measured

by a measurement circuit. The measurement circuit can be either integrated on the same chip 1 or implemented by an external measurement circuit such as the measurement circuit 24 illustrated in the embodiment of Fig. 5.

[0042] Fig. 7 shows a flowchart of a further possible exemplary embodiment, wherein the measured voltage is further processed in step S3 to derive information about process parameters. As can be seen in Fig. 7, the voltage measured in step S2 is further processed in step S3 to derive information about the process parameters and/or operation parameters of the chip under test. The derived information and data can further be processed to generate automatically control signals used for controlling the manufacturing process of the chip 1 and/or the operation process of the chip 1. The derived information can also be used for trimming an internal circuitry of the monitored chip 1. In a possible embodiment, the derived information can be passed to a chip designer or chip design tool which uses the information for the right setting of chip control registers. Accordingly, the voltage generated by the on-chip voltage generation circuit 2 and measured by the measurement circuit can be used for many different purposes.

REFERENCE SIGN LIST

[0043]

1	integrated chip
2	on-chip voltage generation circuit
3	first MOSFET
4	second MOSFET
5	power supply terminal
6	reference potential
7	buffering circuit
7A	operational amplifier
8	subtracting circuit
8A	operational amplifier
8B	resistor
8C	resistor
9	output terminal
10, 11, 12	bias terminals
13, 14	PMOS transistors
15, 16	cascoding PMOS transistors
17, 18	cascoding NMOS transistors
19	on-chip bias current generation circuit
20	integrated electronic circuitry
21	on-chip measurement circuit
22	output terminal
23	test pin
24	external measurement circuit
25	test apparatus
26	processing unit

Claims

1. An on-chip voltage generation circuit (2) integrated on a chip (1),
wherein said on-chip voltage generation circuit (2) is adapted to generate a voltage equivalent to a threshold voltage, V_{th}, of MOSFETs integrated on said chip (1).

2. The on-chip voltage generation circuit according to claim 1 wherein the voltage generated by said on-chip voltage generation circuit (2) is equal to the threshold voltage, V_{th}, of MOSFETs implemented in the on-chip voltage generation circuit (2) and of MOSFETs of other electronic circuits integrated on the same chip (1).

3. The on-chip voltage generation circuit according to claim 1 or 2 wherein a bias current is generated by an on-chip bias current generation circuit (19) of said chip (1).

4. The on-chip voltage generation circuit according to any of the preceding claims 1 to 3 wherein the voltage generated by said on-chip voltage generation circuit (2) is output at a test pin (23) of said chip (1).

5. The on-chip voltage generation circuit according to claim 4 wherein an external measurement circuit (24) connected to the test pin (23) of said chip (1) is adapted to measure the voltage generated by said on-chip voltage generation circuit (2) of said chip (1).

6. The on-chip voltage generation circuit according to claim 5 wherein a processing unit (26) is adapted to analyse the voltage measured by said external measurement circuit (24) to derive information about process parameters.

7. The on-chip voltage generation circuit according to any of the preceding claims 1 to 3 wherein the voltage generated by said on-chip voltage generation circuit (2) is measured by an on-chip measurement circuit (21) integrated on said chip (1).

8. The on-chip voltage generation circuit according to any of the preceding claims 1 to 7 wherein said on-chip voltage generation circuit (2) comprises identical MOSFET diode connected transistors (3, 4) operated in a strong inversion and saturation region.

9. The on-chip voltage generation circuit according to claim 8 wherein a first electrical current (I1) is passed through a first MOSFET (3) of said on-chip voltage generation circuit (2) and a second electrical current (I2) is passed through a second MOSFET (4) of said on-chip voltage generation circuit (2),
wherein the second electrical current (I2) is a current replica of the first electrical current (I1) and has a current strength being four times the current strength of the first electrical current (I1).

10. The on-chip voltage generation circuit according to claim 9 wherein the on-chip voltage generation circuit (2) comprises a buffer circuit (7) adapted to buffer a gate-source voltage of the second MOSFET (4) of said on-chip voltage generation circuit (2).

11. The on-chip voltage generation circuit according to claim 10 wherein the on-chip voltage generation circuit (2) comprises a subtracting circuit (8) adapted to subtract the difference voltage between the gate-source voltage of the second MOSFET (4) and first MOSFET (3) to generate an output voltage being equivalent to the threshold voltage, V_{th}, of the on-chip MOSFET transistors.

12. The on-chip voltage generation circuit according to claim 10 or 11 wherein the buffer circuit (7) comprises a first operational amplifier (7A) having an output fed back directly to an inverting input (-) of said first operational amplifier (7A) and having a non-inverting input (+) connected to a drain terminal (D) of the second MOSFET (4) of said on-chip voltage generation circuit (2).

13. The on-chip voltage generation circuit according to any of the preceding claims 10 to 12 wherein the subtracting circuit (8) comprises a second operational amplifier (8A) having an output fed back via a resistor (8B) to an inverting input (-) of said second operational amplifier (8A) and having a non-inverting input (+) connected to a drain terminal (D) of said first MOSFET (3) of said on-chip voltage generation circuit (2).

14. The on-chip voltage generation circuit according to claim 12 or 13 wherein the output of the first operational amplifier (7A) is connected via a further resistor (8C) to the inverting input (-) of the second operational amplifier (8A).

15. The on-chip voltage generation circuit according to claim 13 or 14 wherein the resistance of both resistors (8B, 8C) is equal.

16. A chip (1) comprising an on-chip voltage generation circuit (2) according to any of the preceding claims 1 to 15 adapted to generate an output voltage corresponding to a threshold voltage, V_{th}, of MOSFETs integrated on said chip (1) and applied to a test pin (23) of said chip (1) for measurement by an external measurement circuit (24) and/or applied to an internal on-chip measurement circuit (21) integrated on said chip (1).

17. The chip according to claim 16 further comprising at least one on-chip bias current generation circuit (19) integrated on said chip (1) and adapted to generate a bias current in response to the voltage generated by said on-chip voltage generation circuit (2) of said chip (1).

18. A method for deriving information about process parameters of a chip (1) comprising the steps of:

- generating (S1) a voltage corresponding to a threshold voltage, V_{th}, of MOSFETs integrated on said chip (1)

by an on-chip voltage generation circuit (2) of said chip;
- measuring (S2) the generated voltage by a measurement circuit and
- analysing (3) the measured voltage to derive information about process parameters.

FIG 1

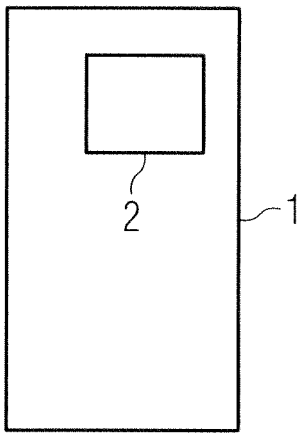


FIG 2

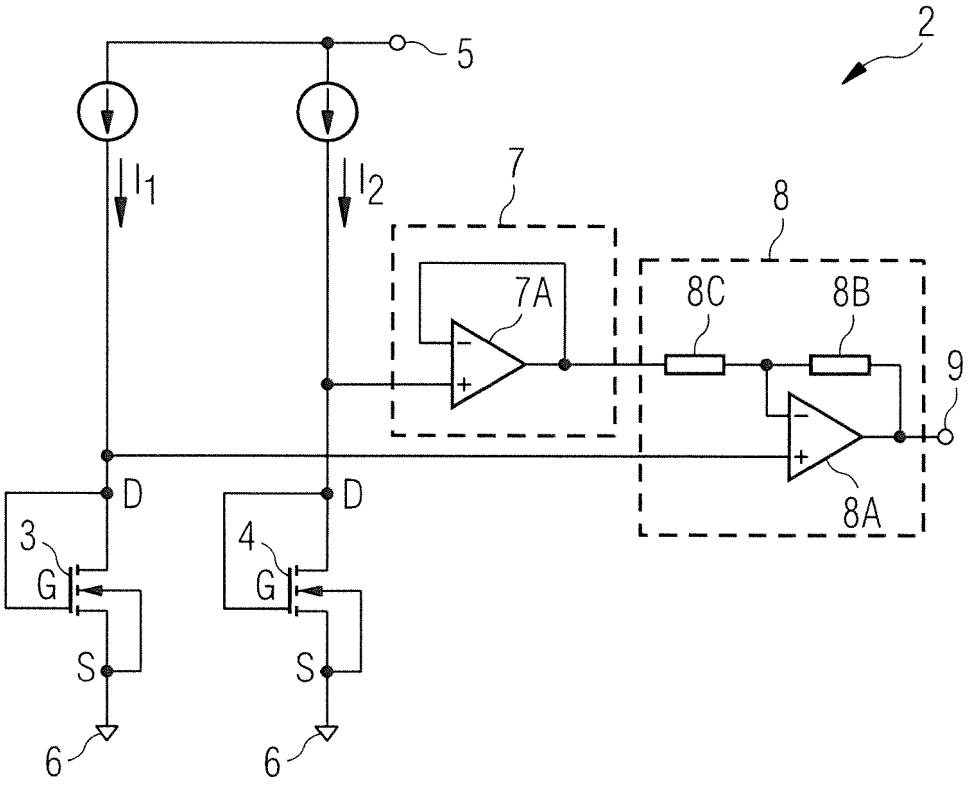


FIG 3

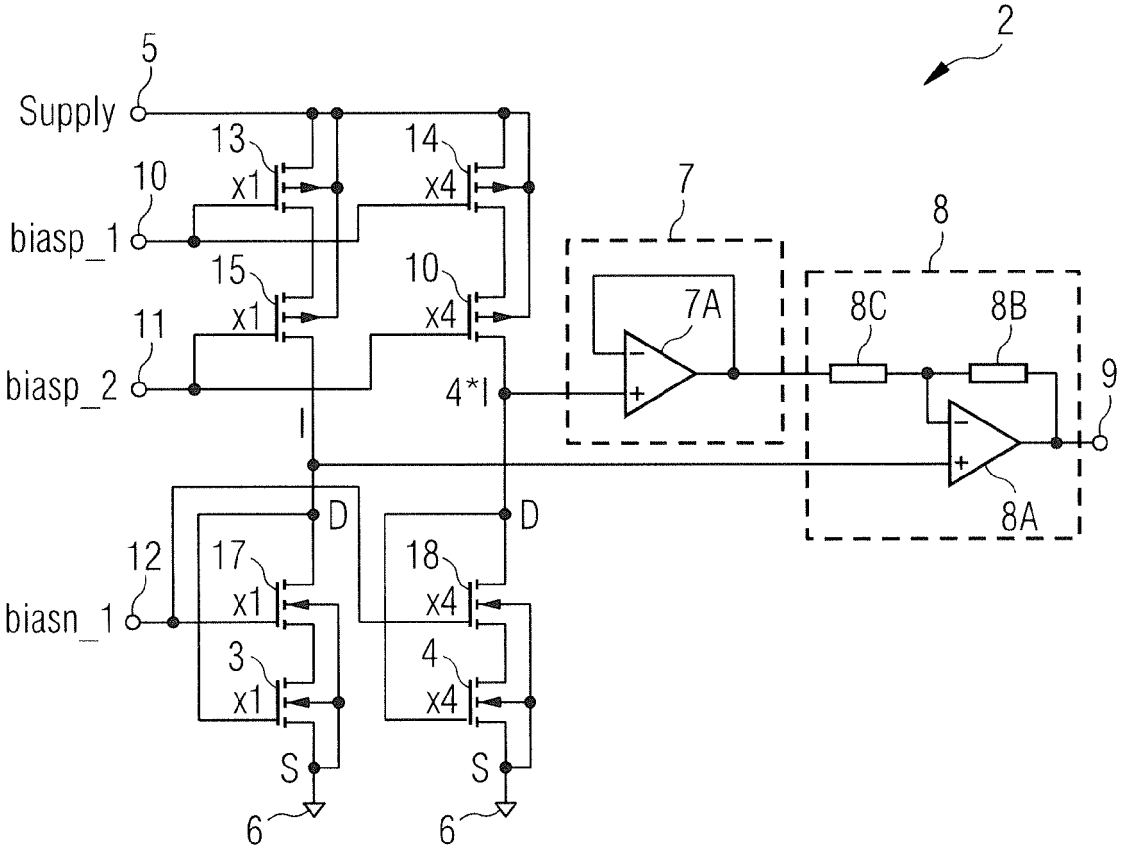

2
5
Supply
13
x1
14
x4
10
biasp_1
7
8
15
x1
10
x4
7A
8C
8B
11
biasp_2
4*I
9
I
D
D
8A
12
17
x1
18
x4
biasn_1
3
x1
4
x4
S
S
6
6

FIG 4

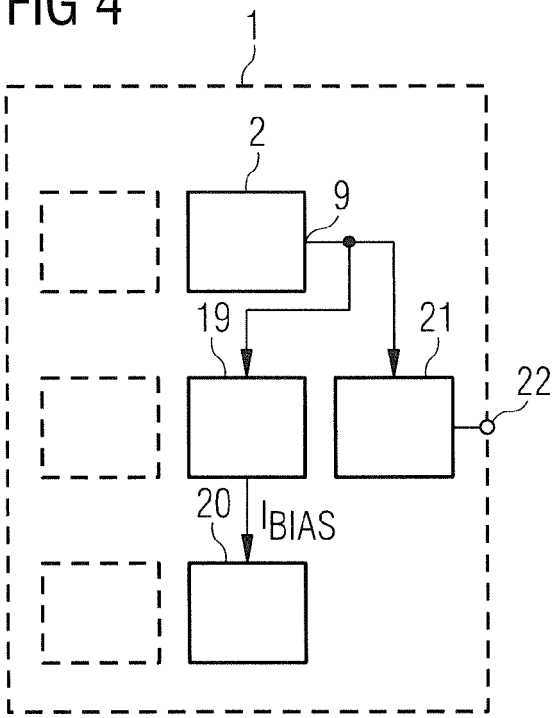

1
2
9
19
21
22
20
IBIAS

FIG 5

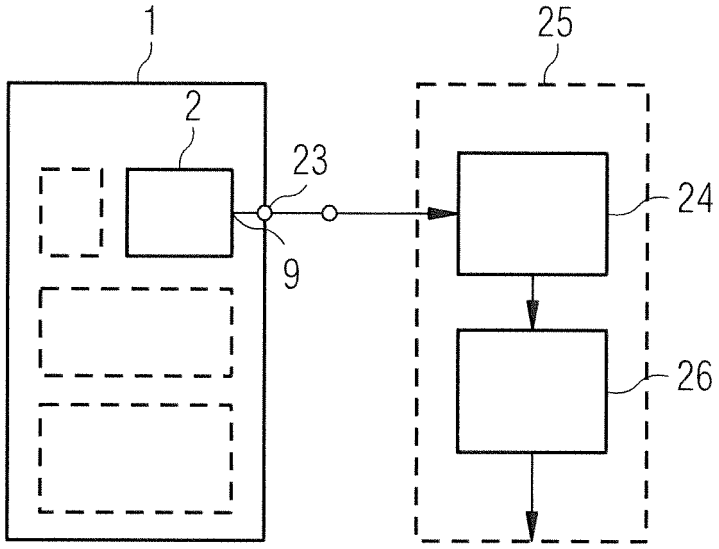


FIG 6

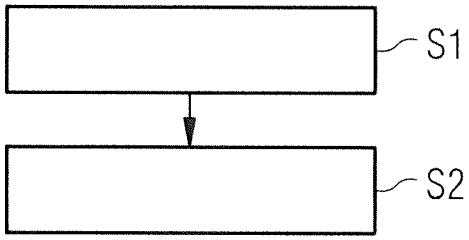
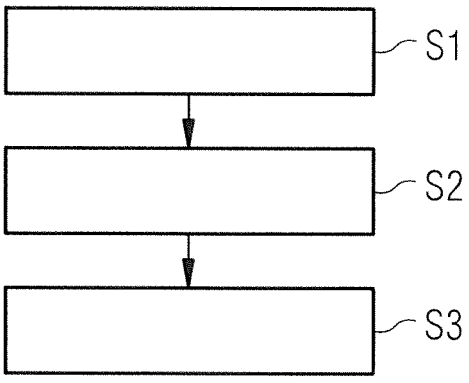


FIG 7



Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 16 20 7413

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2004/113682 A1 (HOON SIEW KUOK [US] ET AL) 17 June 2004 (2004-06-17)	1,2, 8-12,16, 18	INV. G05F3/30
A	* the whole document *	3-7, 13-15,17	

X	US 6 016 072 A (TERNULLO JR LUIGI [US] ET AL) 18 January 2000 (2000-01-18)	1,2,16, 18	
A	* the whole document *	3-15,17	

A	US 7 102 421 B1 (TERNULLO JR LUIGI [US] ET AL) 5 September 2006 (2006-09-05) * abstract *	1-18	

TECHNICAL FIELDS SEARCHED (IPC)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	31 May 2017	Schobert, Daniel

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 16 20 7413

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

31-05-2017

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004113682 A1	17-06-2004	NONE	
US 6016072 A	18-01-2000	NONE	
US 7102421 B1	05-09-2006	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82