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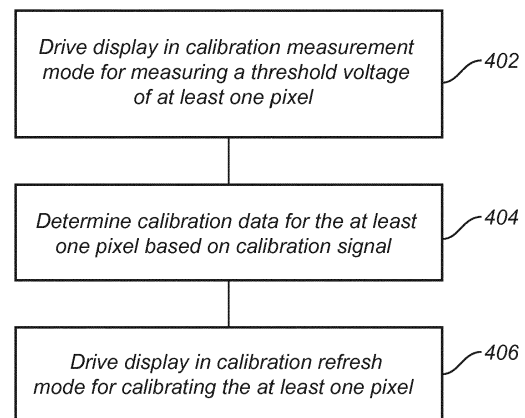
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(54) **AN ACTIVE MATRIX DISPLAY AND A METHOD FOR THRESHOLD VOLTAGE COMPENSATION IN AN ACTIVE MATRIX DISPLAY**

(57) A method for threshold voltage compensation in an active matrix display (200) is provided. The display (200) comprises pixels (100), each comprising a drive transistor (102) having a driver gate (104) and a calibration gate (106), a first dataline (110) selectively connected to the driver gate (104), a second dataline (114) selectively connected to the calibration gate (106). The method comprises: driving (402) the display (200) in a calibration measurement mode for measuring a threshold voltage of a pixel (100), wherein the first dataline (110) is connected to the driver gate (104) and the second dataline (114) is connected to the calibration gate (106), and a measurement signal is actively driven to one of the first and the second dataline (110; 114) and a calibration signal is measured on the other of the first and the second dataline (110; 114), determining (404) calibration data based on the measured calibration signal; and driving (406) the display (200) in a calibration refresh mode, wherein the second dataline (114) is connected to the calibration gate (106) of the drive transistor (102), and the determined calibration data is provided on the second dataline (114) to the calibration gate (106) of the drive transistor (102).



*Fig. 13*

**Description**Technical Field

5     **[0001]** The present inventive concept relates to an active matrix display and a method for threshold voltage compensation in an active matrix display.

Background

10    **[0002]** Active matrix displays comprise a plurality of pixels arranged in an array, wherein each pixel has a light emitting element. The light emitted by the light emitting elements of the pixels together forms an image presented by the display. The light emitting element may for instance be an Organic Light Emitting Diode (OLED) and the display may thus be an active matrix OLED (AMOLED) display.

15    **[0003]** Active matrix displays, such as AMOLED displays, may use a driving backplane, e.g. in the form of one or more thin-film transistor (TFT) arrays. The backplane may be manufactured in low temperature fabrication, which enables use of suitable substrates, e.g. to form flexible displays. Active matrix displays, such as AMOLED displays, are therefore frequently used in various applications and is also a promising technology for future applications.

20    **[0004]** A drive transistor may be used to drive a current through the OLED for emitting light from a pixel. The current through the OLED may depend on characteristics of the drive transistor. These characteristics, in particular a threshold voltage of the drive transistor, may vary over time and variations may differ from pixel to pixel. Hence, in order to avoid a non-uniform output from the display, calibration may be required to compensate for variations and degradation.

25    **[0005]** A dual-gate drive transistor may be used in order to provide compensation for variation in threshold voltage. In present AMOLED displays, it is common to measure the current through the OLED, of which the variation is the result of the variation in threshold voltage of the drive transistor and provide compensation in a current-programmed circuitry. For instance, WO 02/067327 discloses a pixel current driver comprising a plurality of TFTs each having dual gates and for driving OLED layers. The plurality of TFTs may be five TFTs formed in a current-programmed  $\Delta V_T$ -compensated manner. Such a current-programmed compensation yields complex circuits and therefore reduces maximal resolution of the AMOLED display.

30    **[0006]** In another approach, as discussed e.g. in C. Jeon et al, "AMOLED Pixel Circuit using Dual Gate a-IGZO TFTs for Simple Scheme and High Speed VTH Extraction", Society for Information Display Digest, Vol. 47, Issue 1, pages 65-68 (2016), a dual gate drive transistor is used with an operation scheme to compensate for variation in threshold voltage. The pixel may be driven independently of threshold voltage so that degradation due to variation of threshold voltage may be eliminated. However, the approach instead requires a scheme for performing compensation before data may be provided for driving the pixel.

Summary

35    **[0007]** An objective of the present inventive concept is to provide an improved manner for threshold voltage compensation. It is a particular objective of the present inventive concept to provide a threshold voltage compensation using a simple pixel circuitry (and a calibration scheme which is only needed to be intermittently applied).

40    **[0008]** These and other objectives of the present inventive concept are at least partially met by the invention as defined in the independent claims. Preferred embodiments are set out in the dependent claims.

45    **[0009]** According to a first aspect, there is provided a method for threshold voltage compensation in an active matrix display, the display comprising a plurality of pixels arranged in an array comprising a plurality of rows and a plurality of columns, wherein a pixel comprises a drive transistor having a driver gate and a calibration gate, a select transistor for selectively connecting a first dataline to the driver gate of the drive transistor, a calibrate transistor for selectively connecting a second dataline to the calibration gate of the drive transistor, wherein the method comprises: driving the display in a calibration measurement mode for measuring a threshold voltage of at least one pixel in order to enable calibration of the at least one pixel, wherein, in the calibration measurement mode, a gate of the select transistor of the at least one pixel is open to connect the first dataline to the driver gate of the drive transistor and a gate of the calibrate transistor of the at least one pixel is open to connect the second dataline to the calibration gate of the drive transistor, and a measurement signal is actively driven to one of the first and the second dataline and a calibration signal is measured on the other of the first and the second dataline, determining calibration data for the at least one pixel based on the measured calibration signal; and driving the display in a calibration refresh mode for calibrating at least one pixel, wherein, in the calibration refresh mode, a gate of the select transistor of the at least one pixel is closed to disconnect the first dataline from the driver gate of the drive transistor, and a gate of the calibrate transistor of the at least one pixel is open to connect the second dataline to the calibration gate of the drive transistor, and the determined calibration data is provided on the second dataline to the calibration gate of the drive transistor.

**[0010]** Thanks to the invention, the display may be driven in a calibration measurement mode for measuring a threshold voltage of the drive transistor of the at least one pixel. The measurement may then allow a determined calibration signal to be provided to the calibration gate of the drive transistor so as to compensate for the measured threshold voltage in the pixel and handle variations and/or non-uniformities between pixels. This may allow the drive transistor to be operated

by a simple drive signal in order to induce a desired output from a light emitting element driven by the drive transistor.  
**[0011]** Calibration may be performed for all pixels in the display, wherein calibration measurements for all pixels may be performed in a single session, e.g. a single frame, of a calibration measurement mode or a plurality of sessions of the calibration measurement mode, wherein calibration measurements are performed for different pixels in different sessions. Hence, once the active matrix display is calibrated and the threshold voltage is compensated for, driving data may be provided to respective drive transistors of the pixels without any need to take threshold voltage variations between the pixels into account.

**[0012]** The calibration data provided to the calibration gate of the drive transistor may be held at the calibration gate for a substantial period of time such that the display may only occasionally need to be operated in the calibration refresh mode.

**[0013]** Further, the calibration measurement mode may be used for measuring drift in the threshold voltage and may thus be applied at regular intervals in order to enable identifying changes in the threshold voltage and allowing the active matrix display to always compensate for changes to the threshold voltage of the drive transistors.

**[0014]** The invention also allows a simple pixel structure with few elements to be used. This implies that the active matrix display may be arranged with high resolution.

**[0015]** The active matrix display should be construed as any display comprising an active matrix for driving light output from light emitting elements associated with respective drive transistors of pixels of the display. The light emitting elements may for instance be OLED, whereby the active matrix display is an AMOLED display.

**[0016]** The pixels are arranged in an array comprising a plurality of rows and columns. This may imply that the pixels are logically organized in rows and columns and may be commonly addressed by lines for controlling pixels. The terms "row" or "column" do not need to refer to an actual physical direction of the display. As will be understood by the person skilled in the art, rows and columns may be easily interchanged and it is intended in this disclosure that the terms are interchangeable.

**[0017]** The measurement signal may be actively driven to the first dataline and the calibration signal may be measured on the second dataline. However, the measurement signal may alternatively be actively driven to the second dataline and the calibration signal may be measured on the first dataline.

**[0018]** The display may be arranged such that the measurement signals are provided on the first dataline for all pixels. However, in an alternative, the display may be arranged such that the measurement signal may be actively driven to the first dataline and the calibration signal may be measured on the second dataline for some pixels, whereas for other pixels, the measurement signal is actively driven to the second dataline and the calibration signal may be measured on the first dataline. If the datalines are shared between adjacent pixels, this may allow for using the same dataline for receiving the calibration signals for the adjacent pixels sharing the dataline (one pixel providing the calibration signal on its first dataline and the other pixel providing the calibration signal on its second dataline).

**[0019]** According to an embodiment, a first storage capacitor may be connected between the driver gate of the drive transistor and a source or a drain of the drive transistor. This implies that data provided to the driver gate may be maintained by the storage capacitor, e.g. to maintain an output by the pixel in the display while driving data is provided to other pixels. Although such a first storage capacitor may ensure a well-controlled driving of the pixel, use may alternatively be made of parasitic capacitance between the driver gate and the source or drain of the drive transistor.

**[0020]** According to another embodiment, a second storage capacitor may be connected between the calibration gate of the drive transistor and the source or drain of the drive transistor. This implies that data provided to the calibration gate may be maintained by the storage capacitor, e.g. to ensure that calibration data is held on the calibration gate for a substantial period of time without requiring a calibration refresh operation. Although such a second storage capacitor may ensure that the calibration data is held for a substantial period of time at the calibration gate, use may alternatively be made of parasitic capacitance between the calibration gate and the source or drain of the drive transistor. Also, the display may then be operated in the calibration refresh mode more frequently.

**[0021]** According to an embodiment, the driver gate is a front gate of the drive transistor and the calibration gate is a back gate of the drive transistor. However, the driver gate may alternatively be a back gate of the drive transistor and the calibration gate may be a front gate of the drive transistor. Also, the front gate and the back gate of a transistor are relative terms which may be used interchangeably depending on how the transistor is viewed. Thus, as used herein the terms "driver gate" and "calibration gate" should be construed as different gates of a transistor and each of the driver gate and the calibration gate may refer to either a front gate or a back gate of the transistor, respectively.

**[0022]** When a voltage at the driver gate of the drive transistor is below the threshold voltage, a channel of the drive transistor is not conductive and the driver gate and the calibration gate serve as two plates of a capacitor. Hence, there is a capacitive coupling between the driver gate and the calibration gate. When the voltage at the driver gate of the drive

transistor is above the threshold voltage, the channel of the drive transistor is conductive and thus the charges in the channel screen the capacitive coupling between the driver gate and the calibration gate. Thus, it is an insight that the threshold voltage may be determined by identifying a change in the capacitance between the driver gate and the calibration gate.

**[0023]** According to an embodiment, the measurement signal is a periodically varying signal having a first frequency. It is an insight of the invention that a periodically varying signal may be especially useful and may facilitate determination of the threshold voltage in a reliable manner. The periodically varying signal may allow extracting information relating to the threshold voltage from other parameters affecting the measured calibration signal.

**[0024]** According to an embodiment, the measurement signal is varied in relation to a constant signal, wherein the constant signal is chosen based on a highest possible or lowest possible threshold voltage. The determination of the threshold voltage may not be able to differentiate between the threshold voltage being above or below a DC voltage level provided by the constant signal (as the threshold voltage may be determined as an offset to the constant signal). By choosing the constant signal equal to or above a highest possible threshold voltage, it may be concluded that the threshold voltage may be determined by subtracting a determined offset in relation to the constant signal. Similarly, by choosing the constant signal equal to or below a lowest possible threshold voltage, it may be concluded that the threshold voltage may be determined by adding a determined offset in relation to the constant signal. This implies that the threshold voltage may be directly determined based on a single measurement signal and there is no need to provide different measurement signals (e.g. based on different DC voltage levels) in order to determine the threshold voltage.

**[0025]** According to an embodiment, at least a second or a third harmonic in relation to the first frequency is measured for the calibration signal. The parasitic capacitance between the first dataline and the second dataline may be large in relation to the capacitive coupling between the driver gate and the calibration gate, which implies that the parasitic capacitance may make it difficult to identify a change in the capacitance between the driver gate and the calibration gate when the voltage at the driver gate is changed above or below the threshold voltage. However, the second and third harmonics of the first frequency may not be influenced by the parasitic capacitance between the datalines. Thus, by measuring the second or the third harmonic, extraction of the threshold voltage may be enabled without the parasitic capacitance between the datalines affecting the ability to determine the threshold voltage.

**[0026]** As used herein, a "second harmonic" should be construed as a part of the measured calibration signal having a frequency two times the frequency of the measurement signal (i.e. the first frequency). Further, a "third harmonic" should be construed as a part of the measured calibration signal having a frequency three times the frequency of the measurement signal.

**[0027]** According to an embodiment, the threshold voltage is measured for a subset of pixels in a row simultaneously, and wherein a first and a second measurement signal are provided, the second measurement signal being phase-shifted 180° in relation to the first measurement signal, such that a pixel among the subset of pixels receiving the first measurement signal on the first dataline has adjacent pixels among the subset of pixels receiving the second measurement signal. In other words, the first and second measurement signals being phase-shifted 180° in relation to each other are alternately provided to every other pixel among the subset of pixels. This implies that the parasitic capacitive coupling between the datalines of adjacent pixels may be reduced so as to not influence determination of the threshold voltage of the drive transistors, while still enabling simultaneous measurement of the threshold voltage for a plurality of pixels.

**[0028]** All pixels in a row may be divided into a first and a second subset, such that the threshold voltage for all pixels in the first subset may be determined simultaneously in a first measurement period and the threshold voltage for all pixels in the second subset may be determined simultaneously in a second measurement period. It should be realized that more than two subsets may be used and, hence, more than two measurement periods may be used in order to determine the threshold voltage for all pixels in the row.

**[0029]** In an embodiment, the first subset of pixels may be even pixels in a row. Thus, the threshold voltage may be measured for even pixels in the row simultaneously. Similarly, the threshold voltage may be measured for odd pixels in the row simultaneously. This implies that the threshold voltage may be determined for all pixels in a row in two measurement periods, one for even pixels and one for odd pixels.

**[0030]** As used herein, "even pixels in a row" should be construed as pixels being arranged in a column having an even number, where the columns are numbered sequentially starting with 1 for a leftmost column. Similarly, "odd pixels in a row" should be construed as pixels being arranged in a column having an odd number.

**[0031]** According to another embodiment, the measurement signal is a linearly increasing or decreasing voltage. Thus, instead of applying a periodically varying signal, the measurement signal may be increased to sweep the voltage on the driver gate to switch from being below the threshold voltage to being above the threshold voltage. Alternatively, the measurement signal may be decreased to sweep the voltage on the driver gate to switch from being above the threshold voltage to being below the threshold voltage. Thus, when the measurement signal is shifted from below the threshold voltage to above the threshold voltage or vice versa, the shift may be determined in the measured calibration signal.

**[0032]** According to an embodiment, the determining of calibration data comprises identifying a shift in a linear slope of the calibration signal, extracting a threshold voltage based on the identified shift and determining calibration data

based on the extracted threshold voltage. The measured calibration signal at the calibration gate may have a linear dependence to the measurement signal. The threshold voltage may be determined based on a slope of increase of the measured calibration signal in relation to the measurement signal being smaller when the measurement signal is above the threshold voltage (as the capacitive coupling between the driver gate and the calibration gate is shielded above the threshold voltage).

**[0033]** Using a linearly increasing voltage as the measurement signal may provide a very fast manner of determining the threshold voltage. However, the parasitic capacitance between the datalines may make it difficult to identify a change in slope of the measured calibration signal, as the parasitic capacitance may be much larger than the capacitive coupling between the driver gate and the calibration gate and may therefore be a main factor affecting the slope.

**[0034]** According to an embodiment, the method further comprises storing the calibration data and using the stored calibration data in the calibration refresh mode. Thus, the calibration data determined in the calibration measurement may be stored in order to be re-used. This implies that the calibration refresh mode may be operated separately from the calibration measurement mode so as to perform refreshing of the calibration without necessarily performing the calibration measurement (which may be more time consuming). The voltage at the calibration gate may not be stably held for a very long period of time, e.g. due to gate dielectric leakage. Thus, by storing the calibration data, a refreshment of the threshold voltage compensating voltage at the calibration gate may be performed regularly to maintain a desired relation between emitted light in a pixel and a provided control signal.

**[0035]** According to an embodiment, the display is driven in the calibration refresh mode a plurality of times between two subsequent occasions of driving the display in the calibration measurement mode. The calibration measurement may only need to be performed at intervals based on a risk that the threshold voltage of the drive transistor has changed. The calibration refresh mode on the other hand may be performed to ensure that a desired voltage is held at the calibration gate and may therefore need to be performed more frequently.

**[0036]** According to an embodiment, a single row at a time is driven in the calibration refresh mode and calibration refresh is performed for the entire display in a normal video frame. This implies that the stored calibration data may be provided to the pixels of the display in a single frame such that the calibration refreshment will not affect the visual experience provided by the display. During calibration refresh mode, the select transistor may be turned off to maintain the image on the display unchanged during the frame in which calibration refreshment is performed.

**[0037]** According to an embodiment, at least one pixel in a single row is driven in the calibration measurement mode and for all other rows the gates of the select transistors and the calibrate transistors are closed to maintain an image of a former frame on the display. Thus, during calibration measurement, the image on all but one row may be maintained on the display in order to minimally affect the visual experience provided by the display. The calibration measurement may be performed for all pixels in the row before the display is driven to update the frame being displayed. Calibration measurement may be performed in separate frames for each row of the array so that a calibration period is not to be noticed by a user watching the display. One or more frame updates may thus be performed between calibration measurements for different rows of the array.

**[0038]** According to an embodiment, calibration measurement may be performed in separate frames for pixels within the same row of the array (such as odd and even pixels of a row being calibrated in different frames).

**[0039]** A combination of pixels being calibrated within a common frame may be varied in a large number of ways. According to one alternative, all pixels of one or more rows may be calibrated in one frame. According to another alternative, some pixels, e.g. odd pixels or even pixels, from several rows are calibrated within a common frame.

**[0040]** According to an embodiment, the method further comprises performing the calibration measurement mode for at least one row of pixels both in relation to a black display and in relation to an image being presented on the display, and using a difference from the calibration measurements to estimate a voltage drop of a ground plane of the display.

**[0041]** Thus, the method may both be used for compensation of threshold voltage variation of the drive transistors of the pixels and for compensation of voltage drop of the ground plane. Thus, the method estimates a profile of the ground across the display, such that any variations in the ground plane profile may be compensated for in the driving of the drive transistors of the pixels. According to an embodiment, data on the first dataline is compensated by the estimated voltage drop when the display is driven in a normal mode to display an image.

**[0042]** The calibration measurement in relation to the black display may be performed during start-up of the active matrix display before a first image is presented on the display. Then, the calibration measurement in relation to an image being presented on the display may be performed shortly after start-up of the display, such that it may be assumed that no other shift has occurred in the threshold voltage and that the difference from the calibration measurements may be attributed to ground resistive drop.

**[0043]** The calibration measurements to estimate a voltage drop of the ground plane may be performed for a few selected rows of the display. Thus, in this case the calibration measurements are not performed for all rows, as this may be too time consuming for certain display configurations and, hence, affect a visual experience of images presented on the display. The measurements performed for the few selected rows may be used for estimating a profile of the ground plane between the selected rows as well.

**[0044]** According to a second aspect, there is provided an active matrix display, comprising a plurality of pixels arranged in an array comprising a plurality of rows and a plurality of columns, wherein a pixel comprises a drive transistor having a driver gate and a calibration gate, a select transistor for selectively connecting a first dataline to the driver gate of the drive transistor, a calibrate transistor for selectively connecting a second dataline to the calibration gate of the drive transistor; datalines including the first and second datalines arranged along a direction of the rows or the columns of the array, wherein each dataline is connected to the select transistors of pixels along the row or column of the array such that the dataline is connected to the select transistors of pixels on one side of the dataline and to the calibrate transistors of pixels on an opposite side of the dataline; and control circuitry connected to the datalines, wherein the control circuitry is arranged to provide data on the datalines for displaying an image in a normal mode of the display, wherein the control circuitry is further arranged to provide calibration data on the datalines for providing calibration data to the calibration gate of the drive transistor of a pixel in a calibration refresh mode of the display, and wherein the control circuitry is further arranged to provide a measurement signal to one of the first and the second dataline and measure a calibration signal on the other of the first and the second dataline in a calibration measurement mode of the display.

**[0045]** Effects and features of this second aspect are largely analogous to those described above in connection with the first aspect. Embodiments mentioned in relation to the first aspect are largely compatible with the second aspect.

**[0046]** The control circuitry may thus control the display to drive the display in a normal mode, a calibration refresh mode and a calibration measurement mode, which are further described in relation to the method of the first aspect above.

**[0047]** Each dataline may be connected both to a select transistor at one side of the dataline and a calibrate transistor at an opposite side of the dataline. This implies that the datalines may be used both for providing data to the driver gate of drive transistors of pixels via the select transistors and for providing calibration data or measuring calibration signals for other pixels via the calibration transistors. Signals to gates of the select transistors and the calibration transistors may determine how the datalines are used.

**[0048]** According to an embodiment, the control circuitry is arranged to provide the measurement signal as a periodically varying signal having a first frequency.

**[0049]** According to an embodiment, the control circuitry is arranged to measure at least a second or a third harmonic for the calibration signal in relation to the first frequency.

**[0050]** According to an embodiment, the display further comprises an oscillator, which is used for providing a frequency of the measurement signal and is used for providing a reference frequency for extracting the at least second or the third harmonic. This implies that a single oscillator may be re-used both for providing the measurement signal and for measuring the calibration signal. Thus, the reference frequencies for measuring the second and third harmonic may be very accurately related to the first frequency of the measurement signal.

**[0051]** According to an embodiment, the control circuitry comprises a digital to analog converter for each dataline, which is arranged to provide an analog signal when driving the display in normal mode and is arranged as a component of a successive approximation analog to digital converter when driving the display in a calibration measurement mode. This implies that components of the control circuitry may be re-used such that a compact layout of the control circuitry may be provided.

#### Brief description of the drawings

**[0052]** The above, as well as additional objects, features and advantages of the present inventive concept, will be better understood through the following illustrative and non-limiting detailed description, with reference to the appended drawings. In the drawings like reference numerals will be used for like elements unless stated otherwise.

Figs 1 a-b are schematic views of pixel topologies of an active matrix display.

Fig. 2 is a schematic view of the active matrix display.

Figs 3-5 are schematic views illustrating driving of a pixel in a normal operation mode, a calibration refresh mode and a calibration measurement mode, respectively.

Figs 6a-b are schematic views of a capacitive model of a pixel when the voltage on a driver gate of a drive transistor is below a threshold voltage and above a threshold voltage, respectively.

Figs 7-8 is a chart illustrating first, second and third harmonics of measured calibration signals for different frequencies of a measurement signal.

Figs 9a-b are schematic views of a control circuitry and respectively illustrate driving the display in calibration measurement mode for odd pixels or even pixels simultaneously.

Fig. 10a is a schematic view of a control circuitry according to one embodiment.

Figs 10b-d are schematic views of the control circuitry of Fig. 10a and illustrate driving the display in a normal operation mode, in a calibration measurement mode for calibrating odd pixels, and in a calibration measurement mode for calibrating even pixels, respectively.

Figs 11a-b are schematic views of a row of pixels and illustrate driving the display in calibration measurement mode

for two of four pixels simultaneously.

Fig. 11c is a schematic view of a control circuitry according to one embodiment.

Fig. 12 is a schematic view of a display illustrating calibration measurements for ground resistive drop compensation.

Fig. 13 is a flow chart of a method according to an embodiment.

#### Detailed description

**[0053]** Figs 1a-b illustrate two different variants of a pixel topology of an active matrix display. Each pixel comprises an organic light emitting diode (OLED) for emitting light when a current is driven through the OLED. In Fig. 1a, an inverted OLED stack is illustrated. In the pixel topology of Fig. 1a, the OLEDs of each pixel have a common anode. In Fig. 1b, a normal OLED stack is illustrated, where the OLEDs of each pixel have a common cathode. Although the topology of Fig. 1b will be shown and discussed in the below embodiments, it should be realized that the inverted OLED stack topology of Fig. 1a may be used instead.

**[0054]** In case of light emission by the pixels is provided by OLEDs, an active matrix OLED (AMOLED) display is provided. Although OLEDs are mainly discussed here, it should be realized that the active matrix display may be applied to other types of light emitting elements arranged in an array and controlled by an active matrix. Light emitting elements driven by a current may be provided in a number of different manners as will be appreciated by a person skilled in the art, although an AMOLED display may be preferred in view of e.g. fast switching speeds of the pixels.

**[0055]** The pixel 100 comprises a drive transistor 102 having a driver gate 104 and a calibration gate 106. The pixel 100 further comprises a select transistor 108 for selectively connecting a first dataline 110 to the driver gate 104. The pixel 100 further comprises a calibrate transistor 112 for selectively connecting a second dataline 114 to the calibration gate 106.

**[0056]** A signal on the first dataline 110 may be provided through the select transistor 108 to the driver gate 104 of the drive transistor 102. The signal on the first dataline 110 may thus provide data for opening a channel in the drive transistor 102 and hence driving a current through the OLED 116, which is connected to a drain or source of the drive transistor 102. A light output by the OLED 116 may depend on a current level through the OLED 116, such that control circuitry may control the light output by a pixel by controlling data provided on the first dataline 110.

**[0057]** A signal on the second dataline 114 may be provided through the calibrate transistor 112 to the calibration gate 106 of the drive transistor 102. The signal on the second dataline 114 may thus provide data for setting a voltage at the calibration gate 106 of the drive transistor 102. This voltage at the calibration gate 106 may be adapted to compensate for a variation in threshold voltage of the drive transistor 102, such that the data provided on the first dataline 110 may disregard variations in the threshold voltage for controlling the light output by the pixel 100. The current driven through the OLED 116 may thus depend on the voltage difference between the voltage at the driver gate 104 and the source of the drive transistor 102 and depend also on the voltage difference between the voltage at the calibration gate 106 and the source of transistor 102, wherein the voltage level at the calibration gate 106 is provided in relation to a default threshold voltage assumed by the data provided on the first dataline 110.

**[0058]** The pixel 100 may further comprise a first storage capacitor 118, which may be connected between the driver gate 104 of the drive transistor 102 and a source of the drive transistor 102. This implies that data provided to the driver gate 104 may be maintained by the storage capacitor 118, e.g. to maintain an output by the pixel 100 in the display while driving data is provided to other pixels. The first storage capacitor 118 may alternatively be connected to a drain of the drive transistor 102.

**[0059]** Although such a first storage capacitor 118 may ensure a well-controlled driving of the pixel 100, use may alternatively be made of parasitic capacitance between the driver gate 104 and the source or drain of the drive transistor 102 to maintain data on the driver gate 104.

**[0060]** The pixel 100 may further comprise a second storage capacitor 120, which may be connected between the calibration gate 106 of the drive transistor 102 and the source of the drive transistor 102. This implies that data provided to the calibration gate 106 may be maintained by the storage capacitor 120, e.g. to ensure that calibration data is held on the calibration gate 106 for a substantial period of time without requiring that a new calibration signal is provided on the second dataline 114 to the calibration gate 106. The second storage capacitor 120 may alternatively be connected to a drain of the drive transistor 102.

**[0061]** Although such a second storage capacitor 120 may ensure that the calibration data is held for a substantial period of time at the calibration gate 106, use may alternatively be made of parasitic capacitance between the calibration gate 106 and the source or drain of the drive transistor 102 to maintain data on the calibration gate 106. Also, if no second storage capacitor 120 is provided, calibration data may instead be provided more frequently to the calibration gate 106 to refresh the calibration data and maintain the pixel 100 calibrated to the threshold voltage of the drive transistor 102 of the pixel 100.

**[0062]** The pixel 100 may thus be provided with three transistors 102, 108, 112 and two capacitors 118, 120 and the topology of the pixel 100 may thus be a so-called 3T2C (3 transistors, 2 capacitors) topology.

**[0063]** In Fig. 2, an active matrix display 200 comprising an array of pixels 100 arranged in rows and columns is

schematically illustrated. The display 200 comprises datalines 110, 114 which run along a direction of the columns of the array. The display 200 further comprises control circuitry 202, which is connected to the datalines 110, 114. The control circuitry 202 may be arranged to provide data on the datalines 110, 114 and also measure signals on the datalines 110, 114 as will be described in detail below.

**[0064]** The control circuitry 202 may be provided as a data driver integrated circuit, which provides components for generating data signals to the datalines and measuring data signals received on the datalines. The control circuitry 202 may further be connected to a memory for storing calibration data of the pixels 100 or may include an integrated memory in the data driver integrated circuit.

**[0065]** A multiplexer may be used for connecting multiple datalines to one output of the control circuitry 202. Thus, the control circuitry 202 may include multiplexers. If multiplexers are introduced, at least two multiplexers may be introduced for separately connecting to odd datalines and even datalines, respectively, as calibration measurements may require odd and even lines to be driven and measured simultaneously, as further explained below.

**[0066]** The display 200 may further comprise select lines 204 and calibrate lines 206, which run along a direction of the rows of the array, perpendicular to the datalines 110, 114. The select lines 204 may provide signals for selectively activating the select transistors 108 in a row of pixels 100. Similarly, the calibrate lines 206 may provide signals for selectively activating the calibrate transistors 112 in a row of pixels 100.

**[0067]** The display 200 may comprise a pair of select lines 204 for each row of pixels 100 in order to enable independent selection of pixels in even- or odd-numbered columns, respectively. Similarly, the display 200 may comprise a pair of calibrate lines 206 for each row of pixels 100. This may allow calibration measurements for even pixels to be separated from the calibration measurements for odd pixels such that calibration data determined for the even pixels may be maintained during calibration measurement for the odd pixels.

**[0068]** The datalines 110, 114, select lines 204 and calibrate lines 206 as well as the topology for driving the OLEDs 116 of the pixels may be arranged on a backplane of the display 200.

**[0069]** The display 200 may further comprise a driver circuitry 208 for driving the select lines 204 and the calibrate lines 206. The driver circuitry 208 may for instance be arranged as an integrated Gate-In-Panel (GIP) on the backplane. According to an alternative, the driver circuitry 208 may be provided as dedicated silicon drivers.

**[0070]** The transistors for controlling the light output by the pixels 100 may be p-type as well as n-type transistors. The backplane may comprise a thin-film transistor (TFT), for instance hydrogenated amorphous Si (a-Si:H), polycrystalline silicon, organic semiconductor, (amorphous) indium-gallium zinc oxide (a-IGZO, IGZO) TFT. The present invention may be applied to displays using active matrix, not being limited by a particular type of display. For instance, it may be applied to AMOLED displays, for instance RGB or RGBW AMOLED displays, which may comprise fluorescent or phosphorescent OLED, polymer or polydendrimers, high power efficiency phosphorescent polydendrimers, etc.

**[0071]** Referring now to Figs 3-5, three different modes of operating the pixel 100 will be discussed.

**[0072]** A first mode is a normal operation mode, illustrated in Fig. 3, which may be operated according to driving of state of the art AMOLED displays. In this mode, data is provided on the first dataline 110 of the pixel 100 for controlling light output by the pixel 100. In the normal operation mode, the calibrate signal on the calibrate line 206 is low and previously performed calibration of the pixel 100 is unchanged. A calibration value stored on the second storage capacitor 120 thus remains the same. Further, the select signal on the select line 204 is high to allow the driving data provided on the first dataline 110 to be applied to the driver gate 104 of the drive transistor 102. The driving data is stored on the first storage capacitor 118 so that the driving data on the driver gate 104 is maintained. The driving data controls the desired current to be driven through the OLED 116.

**[0073]** The select signals may be driven row by row at a rate of a horizontal synchronization (HSYNC), which may be synchronized with the data provided on the datalines 110 so that the correct driving data is applied to the driver gate 104 of each pixel 100.

**[0074]** If the display 200 comprises a pair of select lines 204 for each row of pixels 100, both the select lines 204 in the pair may be driven together in order to simultaneously provide a high select signal to the select transistors 108 of all the pixels 100 in the row.

**[0075]** A second mode is a calibration refresh mode, illustrated in Fig. 4. In this mode, data is provided on the second dataline 114 of the pixel 100 for providing calibration data to the pixel 100. In the calibration refresh mode, the select signal on the select line 204 is low and the light output by the pixel 100 is unchanged. A driving data value stored on the first storage capacitor 118 thus remains the same. This implies that an image presented by the display 200 will be maintained during 1 frame of calibration refreshment. Further, the calibrate signal on the calibrate line 206 is high to allow the calibration data provided on the second dataline 114 to be applied to the calibration gate 106 of the drive transistor 102. The calibration data is also stored on the second storage capacitor 120 so that the calibration data on the calibration gate 106 may then be maintained. The calibration data provides a compensation in relation to the threshold voltage of the drive transistor 102 such that the driving data provided in the normal operation mode will control the desired current to be driven through the OLED 116.

**[0076]** The calibrate signals may be driven row by row at a rate of HSYNC, which may be synchronized with the data

provided on the datalines 114 so that the correct calibration data is applied to the calibration gate 106 of each pixel 100.

**[0077]** Each dataline 110, 114 may be shared by adjacent pixels 100, such that a dataline may form the first dataline 110 for one pixel and the second dataline 114 for the adjacent pixel. This implies that a dataline providing calibration data for a pixel in column  $n$  when the display 200 is driven in the calibration refresh mode may be used for providing driving data for a pixel in column  $n+1$  when the display 200 is driven in normal operation mode. Thus, the control circuitry 202 may be arranged to provide calibration data with 1 column offset in relation to driving data for presenting an image on the display 200.

**[0078]** Also, if the display 200 comprises a pair of calibrate lines 206 for each row of pixels 100, both the calibrate lines 206 in the pair may be driven together in order to simultaneously provide a high select signal to the calibrate transistors 112 of all the pixels 100 in the row.

**[0079]** As the calibration refresh mode may be operated to refresh calibration data of all pixels 100 of the display 200 in one frame, the calibration refresh mode may be performed without affecting the visual experience to a user watching the display 200.

**[0080]** The calibration refresh mode should be performed sufficiently often so that the calibration data provided on the calibration gate 106 of the drive transistor 102 is maintained. For instance, the charge stored on the second storage capacitor 120 may change due to leakage and the calibration refresh mode may need to be performed before the calibration data on the calibration gate 106 has been significantly changed.

**[0081]** An interval between calibration refresh modes may depend on gate dielectric leakage and a magnitude of transistor current when turned off. A measurement of such parameters may be performed once, e.g. as a step during manufacturing of the display. A frequency of performing the calibration refresh mode may then be adapted to these parameters of the display, setting a default interval of performing the calibration refresh mode.

**[0082]** The calibration refresh mode could for instance be necessary to perform in one frame per minute, per 10 minutes or even per 1 hour of use of the display. Thus, the calibration refresh mode is not performed very often. Hence, not only will a user not be affected by a single frame performing calibration refreshment, the frames allocated to calibration refresh mode are so far apart that even if a single frame of calibration refresh mode would be noticed by a user, a total experience of images presented on the display would be minimally affected.

**[0083]** A third mode is a calibration measurement mode, illustrated in Fig. 5. In this mode, both the select signal on the select line 204 and the calibrate signal on the calibrate line 206 are high for the pixel 100. A measurement signal is actively driven on the first dataline 110 and a calibration signal induced by the measurement signal is measured on the second dataline 114. The measurement signal is provided in relation to a threshold voltage of the drive transistor 102 such that the measured calibration signal may be analyzed so as to extract the threshold voltage of the drive transistor 102. Different embodiments of measurement signals and associated determination of the threshold voltage of the drive transistor 102 will be further described below.

**[0084]** The threshold voltage for one pixel 100 may be determined using the first dataline 110 and the second dataline 114. As the datalines 110, 114 may be shared by adjacent pixels 100 implementing the first dataline 110 for one pixel and the second dataline 114 for a second pixel, the calibration measurement may be performed separately for adjacent pixels. Thus, the calibration measurement mode for one row may involve several operations of measuring the threshold voltage for the drive transistors 102 of different pixels 100 in the row. It is, however, possible to measure threshold voltages for several pixels simultaneously even if not for all pixels in a row, as will be further described below.

**[0085]** The calibration measurement mode may be performed for pixels in one row. For all other rows, the signal on both select lines 204 and calibrate lines 206 are low so that an image of a former frame is maintained on the display 200. To accommodate for losses in visual experience during the single frame of calibration measurement, an intensity of the row to be calibrated may be increased in the frame before calibration measurement and the frame after calibration measurement, e.g. by 40%.

**[0086]** As may be appreciated from the above, the calibration measurement mode may provide calibration measurements for pixels 100 in one row. The calibration measurement mode may thus be repeated a number of times in order to perform calibration measurements for all pixels 100 in all rows. Several normal operation mode frames may pass between two subsequent frames in which calibration measurement is performed, so that the visual experience of images presented on the display 200 is minimally affected.

**[0087]** The calibration measurement mode may be used for determining the threshold voltage of the drive transistor 102 of each pixel 100 so that each pixel 100 may be calibrated to the specific threshold voltage of the drive transistor 102 of the pixel 100. This allows for the display 200 to compensate for threshold voltage variations in the display 200. Such variations may be compensated for thanks to the calibration measurements allowing presenting images of high quality on the display 200.

**[0088]** The threshold voltage of the drive transistor 102 may be changed over time and may be differently changed for different pixels 100, e.g. depending on light output by each pixel 100 and the calibration measurement mode may thus need to be performed at regular intervals. While the calibration refresh mode may e.g. be performed in one frame per minute, the calibration measurement may be performed once per hour. The frequency of the calibration measurement

may be set in dependence of light output. If the display 200 is driven to provide a bright output, the calibration measurement may be performed more frequently.

**[0089]** The drive transistors 102 of the pixels 100 may experience a bias-stress effect, i.e. a time-dependent trapping of charges from the channel of the drive transistor into localized defect states in a semiconductor substrate, in gate dielectric, or at an interface between semiconductor and dielectric. The trapped charges do not contribute to the current through the drive transistor 102 but affect a charge balance of the drive transistor 102. Thus, in use of the drive transistor 102, there may be a time-dependent shift of the threshold voltage due to bias stress.

**[0090]** When a voltage at the driver gate 104 of the drive transistor 102 is below the threshold voltage, the channel of the drive transistor 102 is not conductive and the driver gate 104 and the calibration gate 106 serve as two plates of a capacitor. Hence, there is a capacitive coupling between the driver gate 104 and the calibration gate 106. When the voltage at the driver gate 104 of the drive transistor 102 is above the threshold voltage, the channel of the drive transistor 102 is conductive and thus the charges in the channel screen the capacitive coupling between the driver gate 102 and the calibration gate 104.

**[0091]** The measurement signal provided in the calibration measurement mode is arranged to enable the threshold voltage to be determined by identifying a change in the capacitance between the driver gate 104 and the calibration gate 106.

**[0092]** Referring now to Fig. 6a, a capacitive model of the pixel is illustrated, when a voltage  $V_{GS}$  on the driver gate 104 is below the threshold voltage. In this model, it is assumed that the OLED capacitance is sufficiently high so that it can be considered as a short for the frequencies under consideration. As indicated in Fig. 6a, there is a capacitive coupling  $C_{FGBG}$  between the driver gate 104 and the calibration gate 106.

**[0093]** When the voltage  $V_{GS}$  on the driver gate 104 is above the threshold voltage, as illustrated in Fig. 6b, the driver gate 104 is shielded from the calibration gate 106.

**[0094]** In one embodiment, the measurement signal provides a linear sweep of the voltage from a first voltage below an expected threshold voltage of the drive transistor 102 to a second voltage above the expected threshold voltage of the drive transistor 102. The measured calibration signal may also be an increasing signal, but a slope of increase of the measured calibration signal may be changed when the measurement signal crosses the threshold voltage of the drive transistor 102. When the driver gate 104 is shielded from the calibration gate 106, increase in the measured calibration signal is caused by a parasitic capacitance  $C_{N-N+1}$  between the first dataline 110 and the second dataline 114.

**[0095]** Similarly, the measurement signal may, according to an alternative, provide a linear sweep of the voltage from a first voltage above an expected threshold voltage of the drive transistor 102 to a second voltage below the expected threshold voltage of the drive transistor 102. The measured calibration signal may also be a decreasing signal, but a slope of decrease of the measured calibration signal may be changed when the measurement signal crosses the threshold voltage of the drive transistor 102.

**[0096]** In another embodiment, the measurement signal provides a periodically varying signal having a first frequency. For a first frequency below a maximum frequency, the capacitive model shown in Figs 6a-b is valid. The maximum frequency is a frequency in which charge in the channel is still able to screen the capacitive coupling between the driver gate 104 and the calibration gate 106. The maximum frequency is e.g. inversely related to a channel length of the drive transistor and a determination of a maximum frequency is discussed in Bhoolokam et al, "Analysis of frequency dispersion in amorphous In-Ga-Zn-O thin-film transistors", Journal of Information Display, Vol. 16, No. 1, pages 31-36 (2015).

**[0097]** The measured calibration signal may be analyzed to identify parts of the calibration signal in order to determine the threshold voltage for the drive transistor. The measured calibration signal may comprise a first harmonic, which is a part of the measured calibration signal having the same frequency as the measurement signal, i.e. the first frequency. The measured calibration signal may also comprise a second or a third harmonic (i.e. having a frequency of two or three times the first frequency). The measured calibration signal may further comprise even higher order harmonics, but the higher the order of the harmonic, the smaller the signal is. This also implies that higher order harmonics may be more difficult to measure.

**[0098]** Therefore, although higher order harmonics could be used, second and/or third harmonics may be preferred and use of second and/or third harmonics is described in more detail below.

**[0099]** An amplitude of the first harmonic  $H_1$  when the periodically varying signal is varying in relation to a DC voltage  $V_{GS}$  below the threshold voltage may be approximated as:

$$H_1 \cong \frac{C_{N-N+1} + C_{FGBG}}{C_{Data(N+1)}} A \quad (\text{eq. 1})$$

where  $C_{Data(N+1)}$  is capacitive coupling between the second dataline 114 and ground and A is the amplitude of the applied periodic signal.

**[0100]** An amplitude of the first harmonic  $H_1$  when the periodically varying signal is varying in relation to a DC voltage above the threshold voltage may be approximated as:

$$H_1 \cong \frac{C_{N-N+1}}{C_{Data(N+1)}} A. \quad (\text{eq. 2})$$

**[0101]** The capacitive coupling  $C_{FGBG}$  between the driver gate 104 and the calibration gate 106 may typically be small in relation to the parasitic capacitance  $C_{N-N+1}$  between the datalines and ground and  $A$  is the amplitude of the measurement signal. This implies that it may be difficult to identify whether the DC voltage is above or below the threshold voltage and hence to determine the threshold voltage from the first harmonic of the measured calibration signal.

**[0102]** However, when a DC voltage is provided which is close to the threshold voltage, and the measurement signal will swing across the threshold voltage, a second and a third harmonic may be identified in the measured calibration signal and may be used for determining the threshold voltage.

**[0103]** When the measurement signal crosses the threshold voltage a ratio of the difference between the DC voltage level  $V_{GS}$  and the threshold voltage  $V_T$  in relation to the amplitude  $A$  of the measurement signal is less than 1. In other words

$$x_0 = \frac{V_{GS} - V_T}{A} \quad (\text{eq. 3})$$

and  $|x_0| < 1$ .

**[0104]** In these circumstances, the amplitude of the first, second and third harmonics for an ideal screening of the capacitive coupling between the driver gate 104 and the calibration gate 106 are given by:

$$H_1 = \frac{\arccos[x_0] - x_0 \sqrt{1 - x_0^2}}{\pi} \frac{\Delta C_{FGBG}}{C_{Data(N+1)}} A + \frac{C_{N-N+1}}{C_{Data(N+1)}} A \quad (\text{eq. 4})$$

$$H_2 = \frac{2(1 - x_0^2)^{\frac{3}{2}}}{3\pi} \frac{\Delta C_{FGBG}}{C_{Data(N+1)}} A \quad (\text{eq. 5})$$

$$H_3 = \frac{2|x_0|(1 - x_0^2)^{\frac{3}{2}}}{3\pi} \frac{\Delta C_{FGBG}}{C_{Data(N+1)}} A. \quad (\text{eq. 6})$$

**[0105]** Thus, if the measurement signal is provided to cross the threshold voltage, the second and/or third harmonics may advantageously be used in order to determine the threshold voltage. As is clear from the above equations eq. 5-6, the amplitude of the second and third harmonics are not dependent on the parasitic capacitance between the datalines 110, 114 and may thus not be affected by this parasitic capacitance.

**[0106]** The relation between the amplitude of the second or third harmonic and the ratio  $x_0$  may be used to determine the threshold voltage. Fig. 7 illustrates the amplitude of the first, second and third harmonics (as a fraction of  $(\Delta C_{FGBG}/C_{Data(N+1)}) \cdot A$ ) as a function of  $x_0$  wherein influence of the parasitic capacitance is not included in the illustration of the first harmonic. By analyzing the measured calibration signal for a given DC voltage  $V_{GS}$  and amplitude  $A$  of the measurement signal,  $x_0$  may be determined and, hence, the threshold voltage of the drive transistor 102 may be extracted.

**[0107]** The analysis of the measured calibration signal may be performed in several different manners. For instance, the applied measurement signal may be iteratively changed in order to change  $x_0$ . A maximum of the amplitude of the second harmonic or a minimum of the third harmonic (or both) may then be identified, which corresponds to  $x_0 = 0$ . Thus, it may be determined that the threshold voltage equals the DC voltage  $V_{GS}$  that was used in the iteration for which  $x_0 = 0$ .

**[0108]** Thus, according to an embodiment, iterations of periodically varying signals in relation to a constant signal are provided as measurement signal, wherein the constant signal is changed between iterations.

**[0109]** According to an alternative, an iterative procedure is not necessary. Thus, a measurement signal is provided as a periodically varying signal in relation to a constant signal and the threshold voltage may be directly determined. In

this approach a ratio between the amplitude of the third harmonic and the amplitude of the second harmonic is used. As is clear from equations eq. 5-6, this ratio is given by

$$\frac{H_3}{H_2} = |x_0| = \left| \frac{V_{GS} - V_T}{A} \right|. \quad (\text{eq. 7})$$

**[0110]** Hence, by determining the amplitude of the second and third harmonic, the threshold voltage may be directly calculated as

$$V_T = V_{GS} \pm \frac{AH_3}{H_2}. \quad (\text{eq. 8})$$

**[0111]** This implies that the variation of the threshold voltage may be compensated for by changing a voltage on the calibration gate in relation to the voltage used during the calibration measurement. The change to the voltage at the calibration gate may thus be given by

$$\Delta V_{BG} = \frac{C_{FG}}{C_{BG}} V_T. \quad (\text{eq. 9})$$

**[0112]** The voltage to be used at the calibration gate as given by the voltage used during calibration measurement and the change  $\Delta V_{BG}$  determined in eq. 9 may be stored in a memory of the control circuitry 202 in order to store the calibration data. It should be realized that other information may be stored instead in order to enable determining the voltage to be applied to the calibration gate 106. Thus, the change  $\Delta V_{BG}$  may be stored, or even the difference between the applied DC voltage  $V_{GS}$  and the threshold voltage may be stored.

**[0113]** The above equation eq. 7 may no longer apply, if there is another voltage dependence of the capacitance  $C_{FGBG}$  within a voltage swing of the applied measurement signal. Thus, it may not be possible to use the non-iterative approach, as the determined threshold voltage may not be correct. However, using an iterative approach, a minimum of the amplitude of the third harmonic may still be determined and associated with  $V_{GS}=V_T$  in the iteration where the minimum is determined. Thus, it may still be possible to determine the threshold voltage.

**[0114]** As also discussed above, there is a maximum frequency of the first frequency, when ideal screening of the capacitive coupling between the driver gate 104 and the calibration gate 106 applies. For instance, if the drive transistor 102 has a channel length of 10  $\mu\text{m}$  and the applied DC voltage is 1 V, frequencies up to 5 MHz should be possible to use as the first frequency. Around and above this maximum frequency, oscillations around a driver gate voltage above the threshold voltage will also be coupled to the calibration gate. Thus, a difference in the measured calibration signal between a driver gate voltage above and below the threshold voltage will become smaller and, hence, it may be more difficult to determine the threshold voltage.

**[0115]** However, it may still be possible to use a first frequency above the maximum frequency. In Fig. 8, a simulation of the first, second and third harmonic response is illustrated for a 3dB frequency of the drive transistor. As evident in Fig. 8, it may still be possible to determine a maximum of the second harmonic and/or a minimum of the third harmonic and, hence, even using a higher frequency than the maximum frequency may allow the threshold voltage to be determined.

**[0116]** A choice of the first frequency to be used may take into account both the maximum frequency discussed above and frequencies of noise sources so as to avoid noise interference from such sources. For instance, there may be environmental noise (e.g. from lamps around the display) at frequencies up to almost 100 kHz. Further, charger noise and display noise may be large up to 100 kHz and may also occur up to and above 500 kHz. Also, measuring systems for capacitive touch may use 100-500 kHz frequencies generating noise in this frequency spectrum. Thus, the first frequency may be chosen above 100 kHz, above 500 kHz or above 1 MHz in order to avoid noise interference. For instance, the first frequency may be chosen in a range from 100 kHz-5 MHz, or 500 kHz-5 MHz.

**[0117]** In the above discussion, it has also been assumed that OLED capacitance is sufficiently high for the frequencies used such that the OLED may be considered to be shorted. If the OLED capacitance is not large, the measured calibration signal is affected.

**[0118]** For a driver gate voltage below the threshold voltage, an additional signal corresponding to  $(C_1 \cdot C_2) / (C_{\text{Data}(N+1)} \cdot C_{\text{OLED}}) \cdot A$  may be present in the measured calibration signal. Above the threshold voltage, a voltage at the OLED follows the driver gate voltage. A fraction  $C_2 / C_{\text{Data}(N+1)}$  is obtained in the measured calibration signal. Even in this situation, crossing from below the threshold voltage to above the threshold voltage yield second and third harmonics. Again, by iteratively determining a minimum of the amplitude of the third harmonic, the threshold voltage may be

determined.

**[0119]** The analytical equations for calculating the threshold voltage also depend on a correctness of the assumption that the OLED can be considered as a short for the frequencies under consideration. Thus, this assumption is based on the OLED having sufficient conductivity or a sufficiently high capacitance. In normal circumstances, the OLED will meet both having sufficient conductivity or a sufficiently high capacitance. Regardless, even if the OLED would not meet any of the assumptions, it may also from this perspective be more appropriate to perform an iterative procedure wherein the DC voltage level  $V_{GS}$  is varied in order to identify when the amplitude of the third harmonic is minimal and determine the threshold voltage based on this identification.

**[0120]** As discussed above, the measurement signal in calibration measurement mode is done at a selected DC voltage level  $V_{GS}$  close to the threshold voltage or at iterations of the DC voltage level  $V_{GS}$  around the threshold voltage. This implies that almost no output of light by the OLED 116 is induced by the measurement signal.

**[0121]** When a single iteration of the measurement signal is made, the DC voltage level may be selected to correspond to a highest possible or lowest possible threshold voltage. As indicated above, the ratio between the amplitude of the third harmonic and the second harmonic does only provide a difference between the DC voltage level and the threshold voltage. Thus, by choosing the DC voltage level to correspond to an anticipated highest possible or lowest possible threshold voltage, it may be directly concluded that the determined difference corresponds to a threshold voltage below the highest possible threshold voltage or above the lowest possible threshold voltage, whichever is used as the DC voltage level.

**[0122]** Thus, a calibration measurement may involve the following procedure.

**[0123]** First, a DC voltage is applied on the first dataline 110, wherein the DC voltage in one embodiment corresponds to the highest possible threshold voltage and in another embodiment corresponds to the lowest possible threshold voltage. Then, a DC voltage is applied on the second dataline 114 to provide a desired voltage at the calibration gate 106.

**[0124]** Then, signals on the select line 204 and the calibrate line 206 may be high to open gates of the select transistor 108 and the calibrate transistor 112 to provide the data on the first dataline 110 to the driver gate 104 of the drive transistor 102 and the data on the second dataline 114 to the calibration gate 106 of the drive transistor 102. The second dataline 114 is then made high impedance and calibration measurement may be initiated.

**[0125]** Now, a periodically varying signal is provided on the first dataline 110 providing an AC voltage of the first frequency. An amplitude of the AC voltage may correspond to double of the difference between the lowest possible and the highest possible threshold voltage. This implies that the voltage at the driver gate 104 will be varied above and below the threshold voltage so that second and third harmonics will be generated.

**[0126]** In the embodiment, when the DC voltage is at the highest possible threshold voltage, the AC voltage will for below-zero voltages bring the driver gate voltage below the threshold voltage. On the other hand, in the embodiment, when the DC voltage is at the lowest threshold voltage, the AC voltage will for above-zero voltages bring the driver gate voltage above the threshold voltage.

**[0127]** Second and third harmonics may be determined in the measured calibration signal. Based on determined amplitudes of the second and third harmonics, a corrected voltage of the calibration gate 106 may be calculated.

**[0128]** Then, the signal on the select line 204 may be turned low to close the gate of the select transistor 108. Then, signals may be actively provided on the datalines 114 for providing calibration signals correcting the voltage at the calibration gates 106 of the pixels 100. Finally, the signal on the calibrate line 206 may be turned low to close the gate of the calibrate transistor 112 and a next frame may be provided on the display 200 by driving the display in normal operation mode.

**[0129]** Referring now to Figs 9-11, driving architectures for providing the measurement signal and determining the measured calibration signal will be discussed.

**[0130]** The control circuitry 202 may comprise an oscillator 210, which may be used both for generating the measurement signal and for extracting the second and third harmonics.

**[0131]** The signal from the oscillator 210 may thus be provided to a first phase-locked loop (PLL) 212, where a frequency provided by the oscillator 210 is down-converted to a sixth of the oscillator frequency. This implies that signals for extracting the second and third harmonics may be generated as a third of the oscillator frequency and half the oscillator frequency, respectively, so that the oscillator 210 may be advantageously re-used.

**[0132]** The PLL 212 may provide modulations so as to output two different signals 214, 216 to adjacent pixels 100 on two datalines 218a, 218b. The modulations may preferably be with regard to a phase of the signal, but alternatively an amplitude modulation may be used. In one embodiment, a second measurement signal 216 is phase-shifted  $180^\circ$  in relation to a first measurement signal 214. This may reduce an overall external radiation and reflections at end of the datalines. Also, a capacitive coupling on the second dataline 114 to the first datalines 110 of adjacent pixels will be minimal, as the second dataline 114 may be coupled with opposite signals on both sides of the pixel 100.

**[0133]** In Fig. 9a, driving of odd pixels in a row simultaneously is illustrated. Thus, the first measurement signal is provided on a first dataline 218a, which is coupled to the first dataline 110 of a first pixel 100a in a row, and provided as a measurement signal on the driver gate 104 of the drive transistor 102 of the first pixel 100a. Further, the second

measurement signal is provided on a second dataline 218b, which is coupled to the first dataline 110 of the third pixel 100c in a row, and provided as a measurement signal on the driver gate 104 of the drive transistor 102 of the third pixel 100c. Thus, these odd pixels may be simultaneously driven in the calibration measurement mode.

**[0134]** The first dataline 110 of the second pixel 100b in the row may also function as the second dataline 114 of the first pixel 100a. Thus, this dataline 114 is used for measuring the calibration signal based on the measurement signal provided by the dataline 110 to the first pixel 100a. Hence, the dataline 114 may be coupled to an amplifier 220b to allow measuring of the calibration signal for the first pixel 100a. Similarly, a second dataline 114 of the third pixel 100c, which may also function as the first dataline 110 of the fourth pixel 100d, may be coupled to an amplifier 220d to allow measuring of the calibration signal for the third pixel 100c.

**[0135]** In Fig. 9b, driving of even pixels in a row simultaneously is illustrated. Now, the first measurement signal is coupled to the first dataline 110 of the second pixel 100b and the second measurement signal is coupled to the first dataline 110 of the fourth pixel 100d. The first datalines of the first and third pixels 100a, 100c, are now used for measurement of the calibration signal.

**[0136]** Thus, as illustrated by Figs 9a-b, all pixels in a row may be calibrated in two operations, wherein all odd pixels may be calibrated in a first operation and all even pixels may be calibrated in a second operation.

**[0137]** Referring now to Figs 10a-d, a control circuitry 202 for providing measurement signals and measuring calibration signals will be further described. In Fig. 10a, components related to pixels 100a-100d are shown with connections that may be switched depending on operation modes of the display 200 indicated by dashed lines. In Fig. 10b-d, the connections used in normal operation mode and in calibration measurement mode are shown.

**[0138]** As shown in Fig. 10a, the control circuitry 202 associated with one pixel may comprise a sampling latch 222, a holding latch 224, and a digital-to-analog converter (DAC) 226, which may be used to convert a digital signal providing data for desired light output by the pixel 100 of the display 200 to a corresponding analog signal that may be fed to the first dataline 110 of the pixel 100.

**[0139]** The control circuitry 202 associated with one pixel may further comprise components for analog-to-digital conversion of a measured calibration signal. The DAC 226 may be re-used for implementing a successive approximation analog-to-digital converter. Thus, the control circuitry 202 comprises a comparator 228, which may receive a part of a measured analog signal and a signal from the DAC 226. The output from the comparator 228 may be provided to the holding latch 224, which may function as a successive approximation register and provide an approximate digital code of the received analog signal to the DAC 226.

**[0140]** The control circuitry 202 may further comprise a band pass filter 230 for filtering out a second or third harmonic from the measured calibration signal, a mixer 232 for mixing this filtered signal with a reference signal provided by a PLL 234 generating a second harmonic frequency based on the oscillator frequency or a PLL 236 generating a third harmonic frequency based on the oscillator frequency. Thus, the mixer 232 may accurately extract the second or third harmonic, which may be further passed through a lowpass filter 238 for isolating the second or third harmonic from the mixer 232. The lowpass filter 238 may also perform a sample and hold of the analog signal in order to provide a constant signal to the comparator 228 that may be converted to digital form.

**[0141]** Thus, the control circuitry 202 associated with one pixel may be arranged to either extract a second harmonic or a third harmonic of the measured calibration signal and output the extracted signal through the sampling latch 222.

**[0142]** In Fig. 10b, driving the display 200 in a normal operation mode is illustrated. Data from the DACs 226 of the control circuitry 202 is driven to the datalines of each pixel 100 in order to output light by the pixels.

**[0143]** In Fig. 10c, driving the display 200 in a calibration measurement mode for calibrating odd pixels in a row is illustrated. Thus, the first measurement signal 214 is provided on the first dataline 110 of the first pixel and the second measurement signal 216 is provided on the first dataline 110 of the third pixel.

**[0144]** A calibration signal on the second dataline 114 of the first pixel is passed through the amplifier 220b and then further coupled to the control circuitry 202 associated both with the first pixel and with the second pixel.

**[0145]** The control circuitry 202 associated with the first pixel receives the calibration signal and passes the calibration signal through a band pass filter 230a for extracting a third harmonic. The mixer 232a associated with the first pixel then receives the signal from the band pass filter 230a and a signal from the PLL 236 generating a third harmonic frequency based on the oscillator frequency. Thus, the control circuitry 202 associated with the first pixel may extract a third harmonic signal from the measured calibration signal.

**[0146]** The control circuitry 202 associated with the second pixel also receives the calibration signal on the second dataline 114 and passes the calibration signal through a band pass filter 230b for extracting a second harmonic. The mixer 232b associated with the second pixel then receives the signal from the band pass filter 230b and a signal from the PLL 234 generating a second harmonic frequency based on the oscillator frequency. Thus, the control circuitry 202 associated with the second pixel may extract a second harmonic signal from the measured calibration signal.

**[0147]** The second and third harmonic thus extracted may further be passed to analyzing circuitry for calculating a ratio between the amplitude of the third harmonic and an amplitude of the second harmonic in order to determine the threshold voltage, as discussed above.

**[0148]** In Fig. 10d, driving the display 200 in a calibration measurement mode for calibrating even pixels in a row is illustrated. Here, the second and third harmonics are extracted and analyzed in the same way as discussed above for the odd lines. However, now the first measurement signal 214 is provided on the first dataline 110 of the second pixel and the second measurement signal 216 is provided on the first dataline 110 of the fourth pixel. The calibration signals are received on the second datalines 114 of the even pixels.

**[0149]** Referring now to Figs 11 a-c, another embodiment for providing measurement signals and measuring calibration signals will be further described.

**[0150]** In this embodiment, it is utilized that the capacitive coupling from the driver gate 104 to the calibration gate 106 is equal to the capacitive coupling from the calibration gate 106 to the driver gate 104. The measurement signal may be provided by the first dataline 110 to the driver gate 104 or by the second dataline 114 to the calibration gate 106. Then, the calibration signal may be measured on the other dataline. Thus, the same dataline may always be used for receiving the calibration signal.

**[0151]** The calibration measurement is repeated for every four pixels. In Fig. 11 a, four pixels 100a-d in a row are illustrated and the calibration measurement of the first and fourth pixels 100a, 100d is illustrated.

**[0152]** Here, the first measurement signal is provided on a first dataline 218a, which is coupled to the first dataline 110 of the first pixel 100a, and provided as a measurement signal on the driver gate 104 of the drive transistor 102 of the first pixel 100a. Further, the second measurement signal is provided on a second dataline 218b, which is coupled to the second dataline 114 of the fourth pixel 100d, and provided as a measurement signal on the calibration gate 106 of the drive transistor 102 of the fourth pixel 100d. Thus, these first and fourth pixels in the row may be simultaneously driven in the calibration measurement mode.

**[0153]** The first dataline 110 of the second pixel 100b in the row may also function as the second dataline 114 of the first pixel 100a. Thus, this dataline 114 is used for measuring the calibration signal based on the measurement signal provided by the first dataline 110 to the first pixel 100a. Hence, the dataline 114 may be coupled to an amplifier 220 to allow measuring of the calibration signal for the first pixel 100a. Also, a first dataline 110 of the fourth pixel 100d may be coupled to an amplifier 220 to allow measuring of the calibration signal for the fourth pixel 100d, wherein the calibration signal is acquired on the driver gate 104 of the drive transistor 102 of the fourth pixel 100d. The first dataline 110 of the third pixel 100c, which also functions as the second dataline 114 of the second pixel 100b, may be driven with a sufficiently high DC signal so that the channel of the drive transistor 102 for the second and third pixels 100b, 100c is conductive and thus screening the capacitive coupling between the driver gate 104 and the calibration gate 106 of the drive transistors 102 of these pixels. Thus, the capacitive coupling between the gates in these pixels does not affect calibration measurements of the first and fourth pixels 100a, 100d.

**[0154]** As described, a first 214 and a second measurement signal 216 may be used, wherein the second measurement signal 216 is phase-shifted  $180^\circ$  in relation to a first measurement signal 214. This may reduce an overall external radiation and reflections at end of the datalines.

**[0155]** In Fig. 11 b, the calibration measurement of the second and third pixels 100b, 100c is illustrated.

**[0156]** Here, a measurement signal is provided on a first dataline 218a, which is coupled to the first dataline 110 of the third pixel 100c, which also functions as the second dataline 114 of the second pixel 100b. The measurement signal is thus provided as a measurement signal on the driver gate 104 of the drive transistor 102 of the third pixel 100c and also provided as a measurement signal on the calibration gate 106 of the drive transistor 102 of the second pixel 100b. Thus, these second and third pixels in the row may be simultaneously driven in the calibration measurement mode using the same measurement signal.

**[0157]** The first dataline 110 of the second pixel 100b in the row may, similar to the measurement of the calibration signal for the first pixel 100a, again be used for measuring a calibration signal, but this time measuring the calibration signal for the second pixel 100b. Also, the first dataline 110 of the fourth pixel 100d, which also functions as the second dataline 114 of the third pixel 100c, may be used for measuring of the calibration signal for the third pixel 100c. The first dataline 110 of the first pixel 100a and second dataline 114 of the fourth pixel 100d may be driven with a sufficiently high DC signal so that the channel of the drive transistor 102 for the first and fourth pixels 100a, 100d is conductive and thus screening the capacitive coupling between the driver gate 104 and the calibration gate 106 of the drive transistors 102 of these pixels. Thus, the capacitive coupling between the gates in these pixels does not affect calibration measurements of the second and third pixels 100b, 100c.

**[0158]** In the calibration measurements of the second and third pixels 100b, 100c, the same measurement signal may be used for performing the calibration measurement of two signals. Still, a first and a second measurement signal, phase-shifted  $180^\circ$  in relation to each other, may be provided and actively driven to every other dataline in a row that receives the measurement signal (i.e. the first measurement signal is provided to every eighth dataline in the row of pixels).

**[0159]** Thus, as illustrated by Figs 11a-b, all pixels in a row may be calibrated in two operations, wherein two of every four pixels may be calibrated in a first operation and the remaining two of every four pixels may be calibrated in a second operation. Since the same datalines are used for measuring the calibration signal, the control circuitry 302 may be differently arranged.

**[0160]** In Fig. 11c, components related to pixels 100a-100d are shown with connections that may be switched depending on operation modes of the display 200 indicated by dashed lines. The control circuitry 302 is not described in detail as it may function in a similar way as the control circuitry 202 described above in relation to Figs 10a-d. As shown in Fig. 11c, it is not necessary to have an amplifier 220 associated with every dataline, as the same datalines are always used for measuring calibration signals.

**[0161]** As shown above, it is possible to measure the threshold voltage for the drive transistor 102 of each pixel 100 in a display 200. The threshold voltage may be measured in relation to a black display (no image being presented on the display) and in relation to an image being presented on the display. A difference in threshold voltages from two such calibration measurements may then be used to estimate a voltage drop of the ground plane of the display 200.

**[0162]** A first calibration measurement may thus be performed during start-up of the active matrix display 200 before a first image is presented on the display 200. The first calibration measurement may thus enable measuring a difference between a gate-to-source voltage  $V_{GS}$  on the driver gate 104 and the threshold voltage of the drive transistor 102 when no pixels 100 are active and, hence, no voltage drop may occur in the ground plane. Then, a second calibration measurement in relation to an image being presented on the display 200 may be performed shortly after start-up of the display, such that it may be assumed that no other shift has occurred in the threshold voltage. The second calibration measurement may then allow determining the same difference between the voltage  $V_{GS}$  on the driver gate 104 and the threshold voltage of the drive transistor 102 when pixels 100 of the display are active. A difference between the first and the second calibration measurements may then provide a difference in source voltage  $V_s$  of the drive transistor 102 in the first and second calibration measurements and may be attributed to ground resistive drop.

**[0163]** As illustrated in Fig. 12, the calibration measurements to estimate a voltage drop of the ground plane may be performed for a few selected rows 304 of the display 200. Thus, the calibration measurements are not necessarily performed for all rows, as this may be too time consuming and, hence, affect a visual experience of images presented on the display. The measurements performed for the few selected rows 304 may be used for determining a profile of the source voltage  $V_s$  for these rows 304 (and determine the ground resistive drop for these rows 304 as a consequence) and estimating a profile of the ground plane for the other rows in the display 200 as well.

**[0164]** For instance, three rows 304 may be recalibrated in a frame being presented on the display 200. This may be repeated a few times to perform calibration measurements for several rows. The determined profile of the ground plane for the selected rows 304 may also be used to estimate the profile of the ground plane across the entire display 200 (between the selected rows 304).

**[0165]** In normal operation mode of the display 200, the respective estimated value of the resistive drop  $V_s$  at a pixel may be added to a data value provided on the first dataline 110 of the pixel 100 in order to compensate for the ground resistive drop when driving the pixel 100.

**[0166]** In case of a normal OLED stack, as shown in Fig. 1 b, ground is typically an evaporated counter electrode of the OLEDs. The counter electrode is usually not patterned, which allows current to flow in all directions of the counter electrode. Hence, gradients in the voltage drop profile of the ground plane may be averaged across the ground plane. This implies that measuring the ground profile on a few selected reference rows enables a good assessment of the ground resistive drop across the entire display 200.

**[0167]** In case of an inverted OLED stack, as shown in Fig. 1 a, ground connections are typically implemented in metal wirings in a TFT of the display 200. The wirings may be independent and hence, if calibration of the ground plane in relation to a few ground wiring lines is made, it may be difficult to make an assessment of a ground resistive drop profile across the entire display 200.

**[0168]** Thus, the datalines 110, 114 of the display which may extend along columns of the array may preferably be arranged to be parallel to the ground wirings, which implies that calibration of a few selected rows of the display 200 provides for each column (along which the ground wirings extend) a few reference points for the voltage drop. Thus, a good assessment of the overall voltage drop of the column is possible.

**[0169]** If the ground wiring lines extend in both directions along rows of the display 200 and along columns of the display 200, it may be even more easy to assess the ground resistive drop profile across the entire display 200.

**[0170]** In case of the inverted OLED stack, the ground resistive profile may alternatively be estimated based on actual expected current in every pixel, which is given by the data provided on the first dataline 110 of each pixel, and a value for the resistance in every pixel, where the resistance is known and stable. The ground resistive drop may be determined if there are only ground wirings along a direction perpendicular to the datalines. The voltage drop  $\Delta V_n$  over the ground line (and thus the ground profile) can be calculated as a double-nested sum over the pixels  $k$ ,  $m$ , as a function of the pixel resistance  $R_m$  and pixel currents  $I_k$ :

$$\Delta V_n = \sum_{k=1}^n \sum_{m=1}^k I_k * R_m.$$

**[0171]** Referring now to Fig. 13, a method for threshold voltage compensation in an active matrix display will be briefly summarized.

**[0172]** The method comprises driving the display in a calibration measurement mode, step 402, for measuring a threshold voltage of at least one pixel in order to enable calibration of the at least one pixel 100. In the calibration measurement mode, a measurement signal is actively driven to one of the first and the second dataline 110, 114, and a calibration signal is measured on the other of the first and the second dataline 110, 114 of the pixel 100.

**[0173]** The method further comprises determining calibration data for the at least one pixel based on the measured calibration signal, step 404. Thus, calibration data may be determined which may be used for compensation of threshold voltage variation of the pixel 100.

**[0174]** The method further comprises driving the display in a calibration refresh mode, step 406, for calibrating at least one pixel. In the calibration refresh mode, calibration data may be provided on the second dataline 114 to the calibration gate 106 of the drive transistor 102. By driving the display in the calibration refresh mode, the pixels 100 may be maintained in a calibrated state.

**[0175]** The display may thus be driven in a normal operation mode, wherein data may be provided on first datalines 110 to drive output of light from each pixel, wherein the calibration of the pixels ensures that the desired output is received from the respective pixels.

**[0176]** In the above the inventive concept has mainly been described with reference to a limited number of examples. However, as is readily appreciated by a person skilled in the art, other examples than the ones disclosed above are equally possible within the scope of the inventive concept, as defined by the appended claims.

**[0177]** Although the calibration measurements have been mainly described above as being performed by driving an active measurement signal on the driver gate 104 and measuring a calibration signal on the calibration gate 106, the capacitive coupling from the calibration gate 106 to the driver gate 104 should be equal to the capacitive coupling from the driver gate 104 to the calibration gate 106, so the calibration measurements may alternatively be performed by driving an active measurement signal on the calibration gate 106 and measuring the calibration signal on the driver gate 104.

## Claims

1. A method for threshold voltage compensation in an active matrix display (200), the display (200) comprising a plurality of pixels (100) arranged in an array comprising a plurality of rows and a plurality of columns, wherein a pixel comprises a drive transistor (102) having a driver gate (104) and a calibration gate (106), a select transistor (108) for selectively connecting a first dataline (110) to the driver gate (104) of the drive transistor (102), a calibrate transistor (112) for selectively connecting a second dataline (114) to the calibration gate (106) of the drive transistor (102), wherein the method comprises:

driving (402) the display (200) in a calibration measurement mode for measuring a threshold voltage of at least one pixel (100) in order to enable calibration of the at least one pixel (100), wherein, in the calibration measurement mode, a gate of the select transistor (108) of the at least one pixel (100) is open to connect the first dataline (110) to the driver gate (104) of the drive transistor (102) and a gate of the calibrate transistor (112) of the at least one pixel (100) is open to connect the second dataline (114) to the calibration gate (106) of the drive transistor (102), and a measurement signal is actively driven to one of the first and the second dataline (110; 114) and a calibration signal is measured on the other of the first and the second dataline (110; 114), determining (404) calibration data for the at least one pixel (100) based on the measured calibration signal; and driving (406) the display (200) in a calibration refresh mode for calibrating at least one pixel (100), wherein, in the calibration refresh mode, a gate of the select transistor (108) of the at least one pixel (100) is closed to disconnect the first dataline (110) from the driver gate (104) of the drive transistor (102), and a gate of the calibrate transistor (112) of the at least one pixel (100) is open to connect the second dataline (114) to the calibration gate (106) of the drive transistor (102), and the determined calibration data is provided on the second dataline (114) to the calibration gate (106) of the drive transistor (102).

2. The method according to claim 1, wherein the measurement signal is a periodically varying signal having a first frequency.

3. The method according to claim 2, wherein the measurement signal is varied in relation to a constant signal, wherein the constant signal is chosen based on a highest possible or lowest possible threshold voltage.

4. The method according to claim 2 or 3, wherein at least a second or a third harmonic in relation to the first frequency

is measured for the calibration signal.

5. The method according to any one of claims 2-4, wherein the threshold voltage is measured for a subset of pixels (100b, 100d) in a row simultaneously, and wherein a first and a second measurement signal (214; 216) are provided, the second measurement signal (216) being phase-shifted 180° in relation to the first measurement signal (214), such that a pixel among the subset of pixels (100b, 100d) receiving the first measurement signal (214) on the first dataline (110) has adjacent pixels among the subset of pixels (100b, 100d) receiving the second measurement signal (216).
6. The method according to any one of the preceding claims, further comprising storing the calibration data and using the stored calibration data in the calibration refresh mode.
7. The method according to any one of the preceding claims, wherein the display (200) is driven in the calibration refresh mode a plurality of times between two subsequent occasions of driving the display (200) in the calibration measurement mode.
8. The method according to any one of the preceding claims, wherein at least one pixel (100) in a single row is driven in the calibration measurement mode and for all other rows the gates of the select transistors (108) and the calibrate transistors (112) are closed to maintain an image of a former frame on the display (200).
9. The method according to any one of the preceding claims, further comprising performing the calibration measurement mode for at least one row of pixels (100) both in relation to a black display and in relation to an image being presented on the display (200), and using a difference from the calibration measurements to estimate a voltage drop of a ground plane of the display (200).
10. The method according to claim 9, wherein data on the first dataline (110) is compensated by the estimated voltage drop when the display (200) is driven in a normal mode to display an image.
11. An active matrix display (200), comprising
  - a plurality of pixels (100) arranged in an array comprising a plurality of rows and a plurality of columns, wherein a pixel (100) comprises a drive transistor (102) having a driver gate (104) and a calibration gate (106), a select transistor (108) for selectively connecting a first dataline (110) to the driver gate (104) of the drive transistor (102), a calibrate transistor (112) for selectively connecting a second dataline (114) to the calibration gate (106) of the drive transistor (102);
  - datalines including the first and second datalines (110; 114) arranged along a direction of the rows or the columns of the array, wherein each dataline (110; 114) is connected to the select transistors (108) of pixels (100) along the row or column of the array such that the dataline (110; 114) is connected to the select transistors (108) of pixels (100) on one side of the dataline (110; 114) and to the calibrate transistors (112) of pixels (100) on an opposite side of the dataline (110; 114); and
  - control circuitry (202) connected to the datalines (110; 114), wherein the control circuitry (202) is arranged to provide data on the datalines (110; 114) for displaying an image in a normal mode of the display (200), wherein the control circuitry (202) is further arranged to provide calibration data on the datalines (110; 114) for providing calibration data to the calibration gate (106) of the drive transistor (102) of a pixel (100) in a calibration refresh mode of the display (200), and wherein the control circuitry (202) is further arranged to provide a measurement signal to one of the first and the second dataline (110; 114) and measure a calibration signal on the other of the first and the second dataline (110; 114) in a calibration measurement mode of the display (200).
12. The display according to claim 11, wherein the control circuitry (202) is arranged to provide the measurement signal as a periodically varying signal having a first frequency.
13. The display according to claim 12, wherein the control circuitry (202) is arranged to measure at least a second or a third harmonic for the calibration signal in relation to the first frequency.
14. The display according to claim 13, further comprising an oscillator (210), which is used for providing a frequency of the measurement signal and is used for providing a reference frequency for extracting the at least second or the third harmonic.
15. The display according to any one of claims 11-14, wherein the control circuitry (202) comprises a digital to analog

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converter (226) for each dataline (110; 114), which is arranged to provide an analog signal when driving the display (200) in normal mode and is arranged as a component of a successive approximation analog to digital converter when driving the display (200) in a calibration measurement mode.

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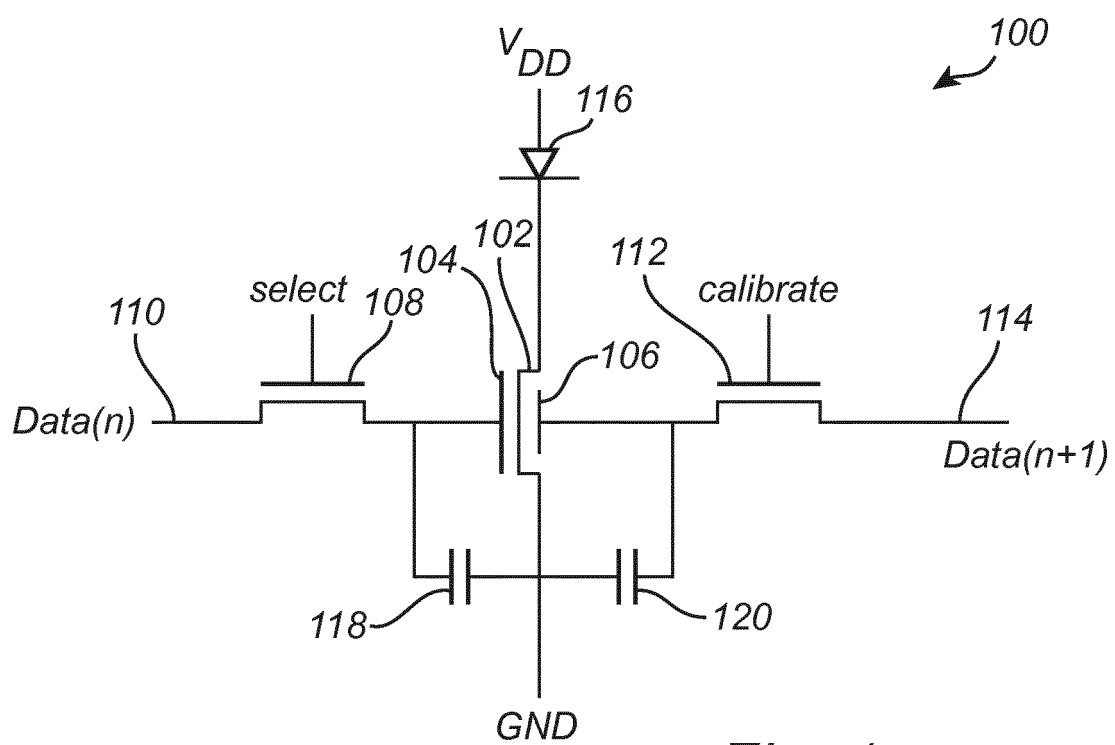


Fig. 1a

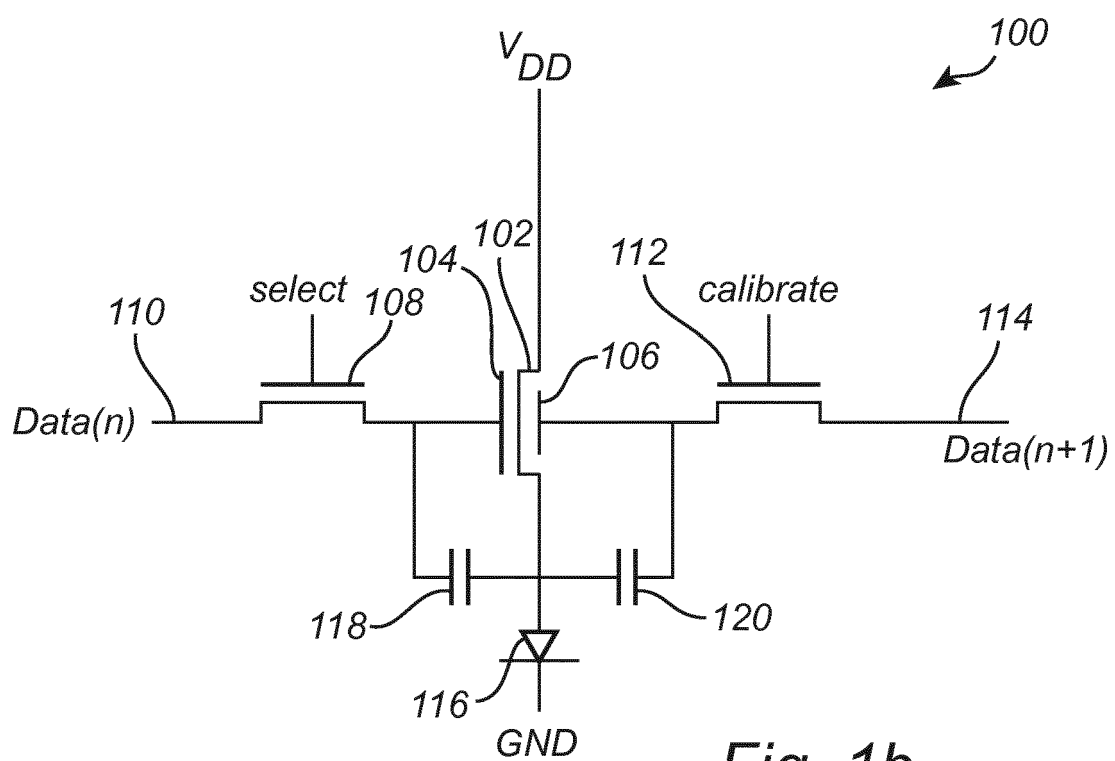


Fig. 1b

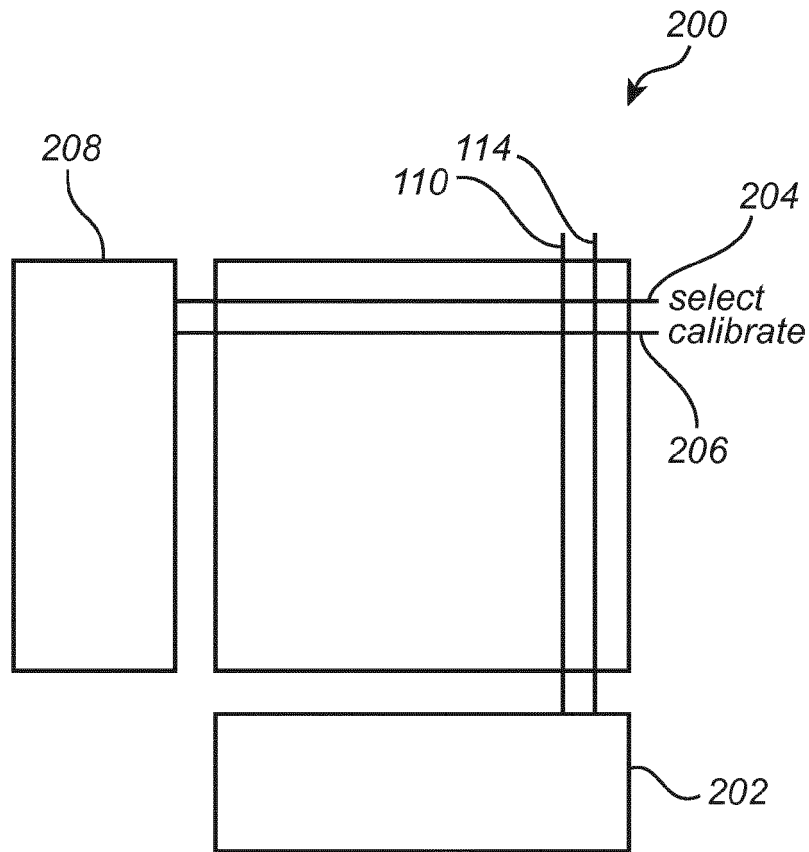


Fig. 2

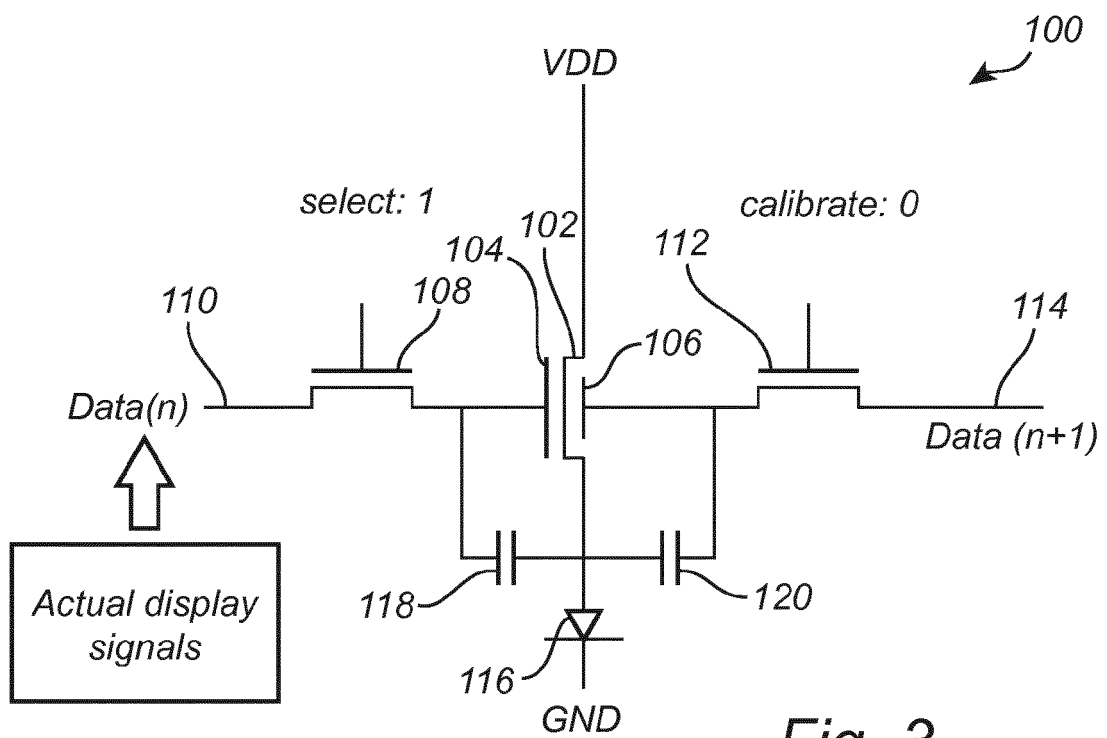


Fig. 3

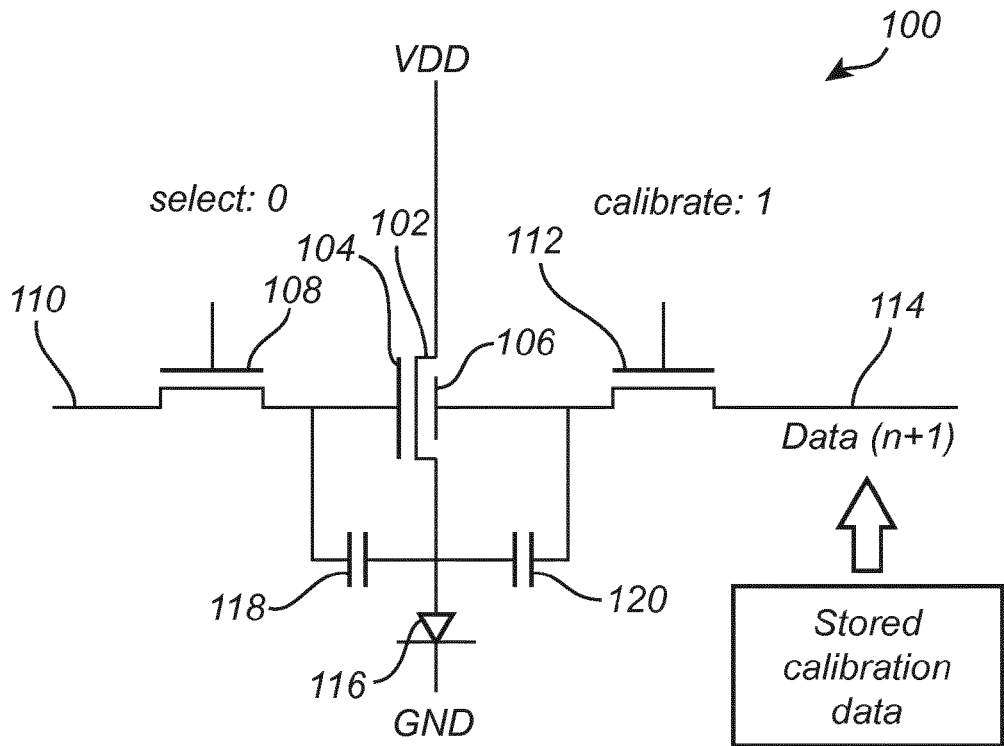


Fig. 4

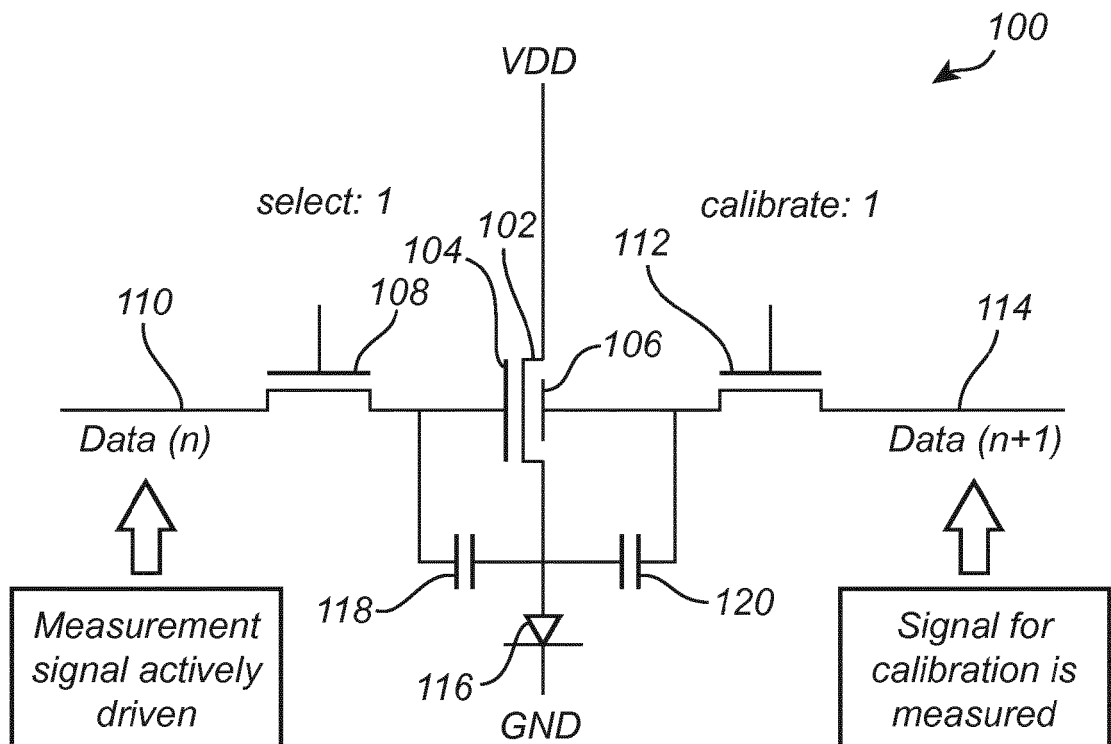


Fig. 5

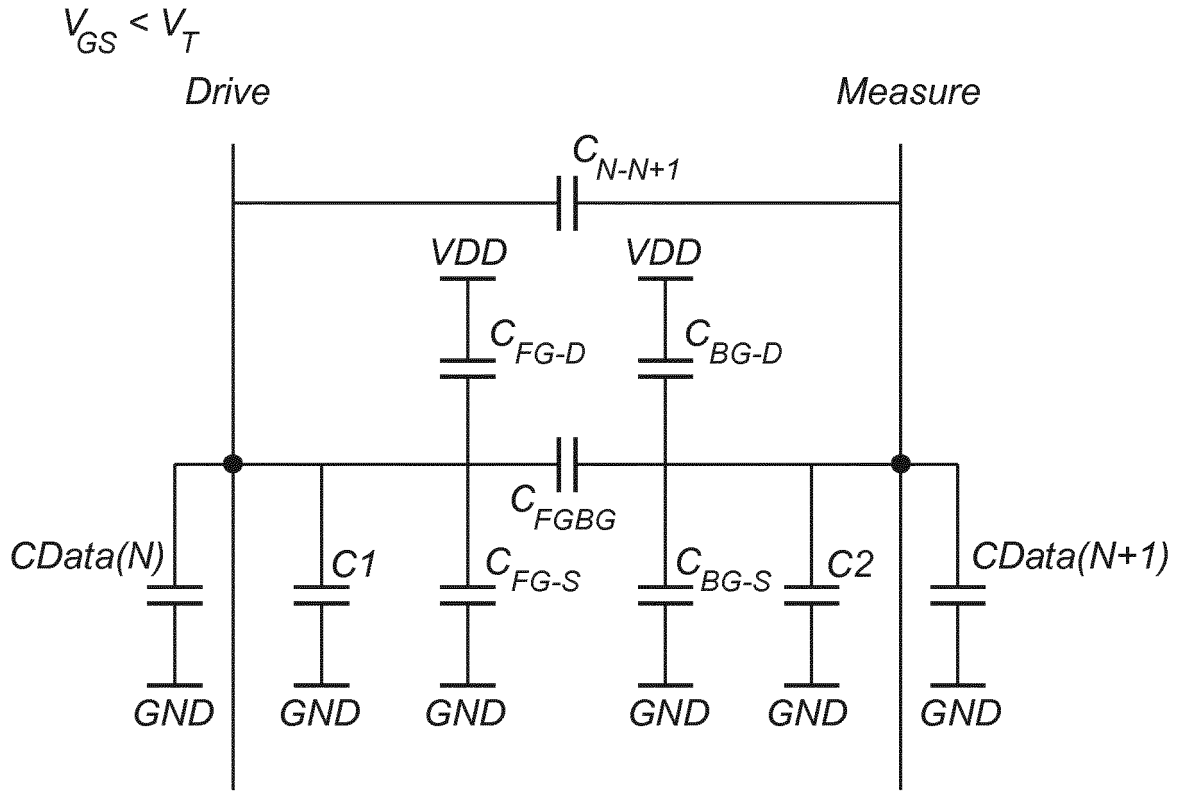


Fig. 6a

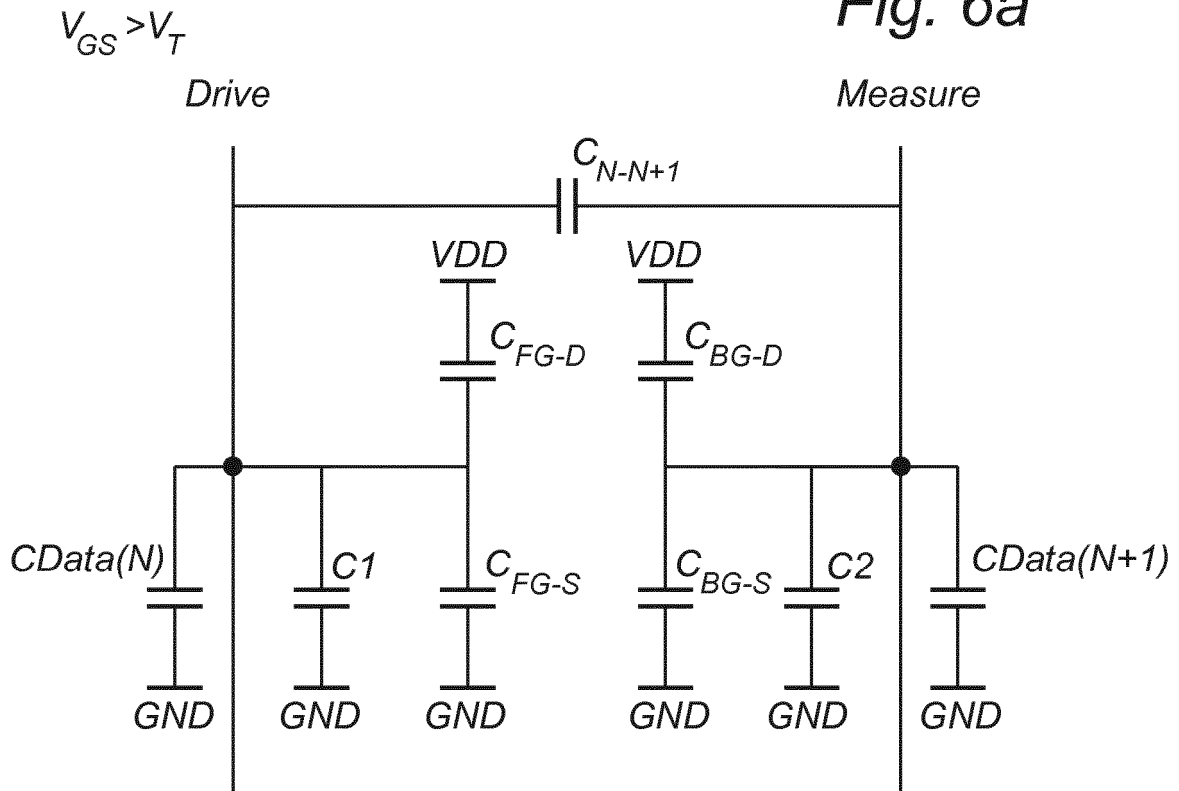


Fig. 6b

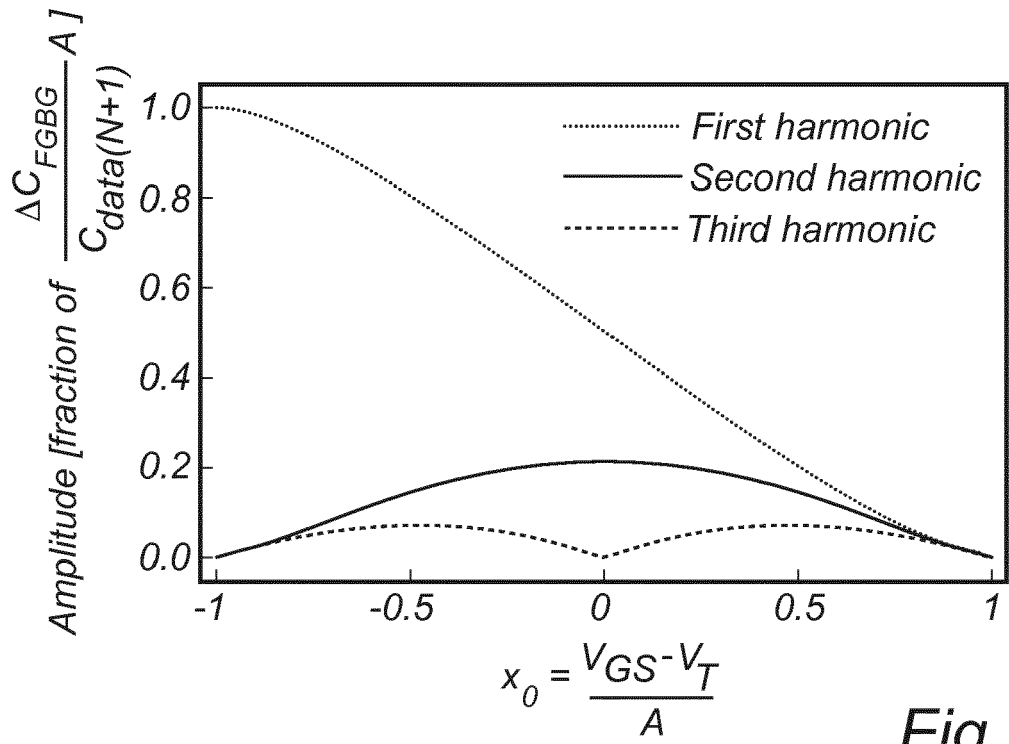


Fig. 7

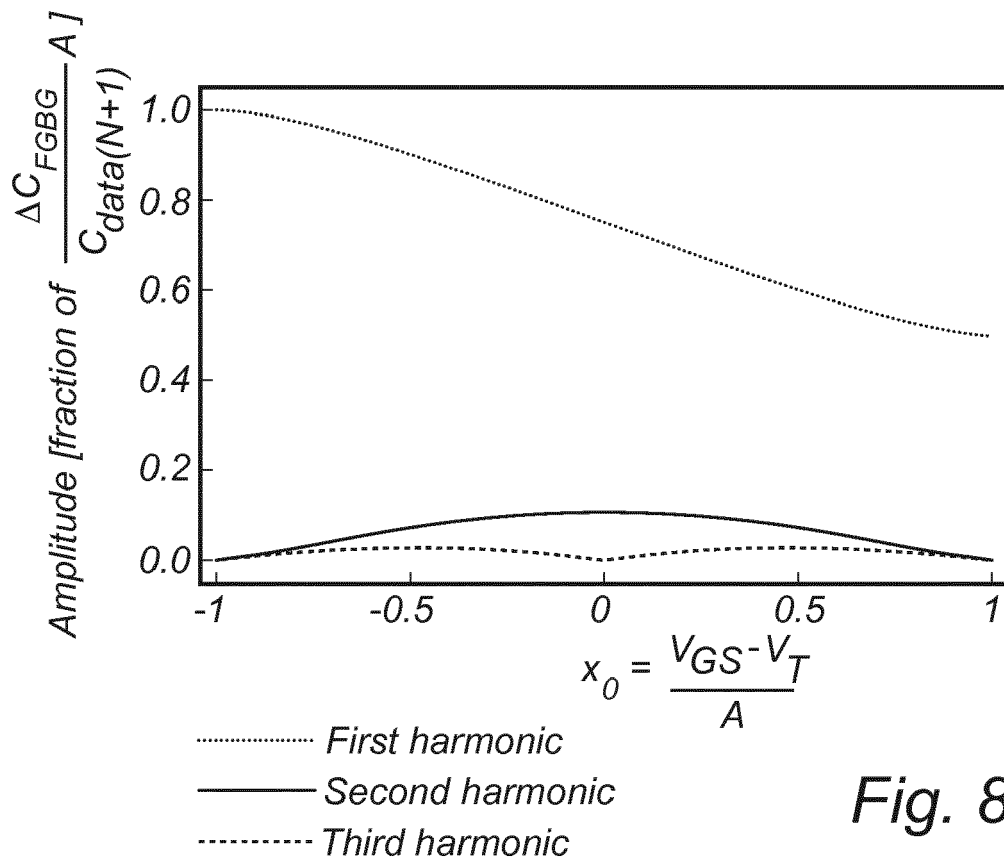


Fig. 8

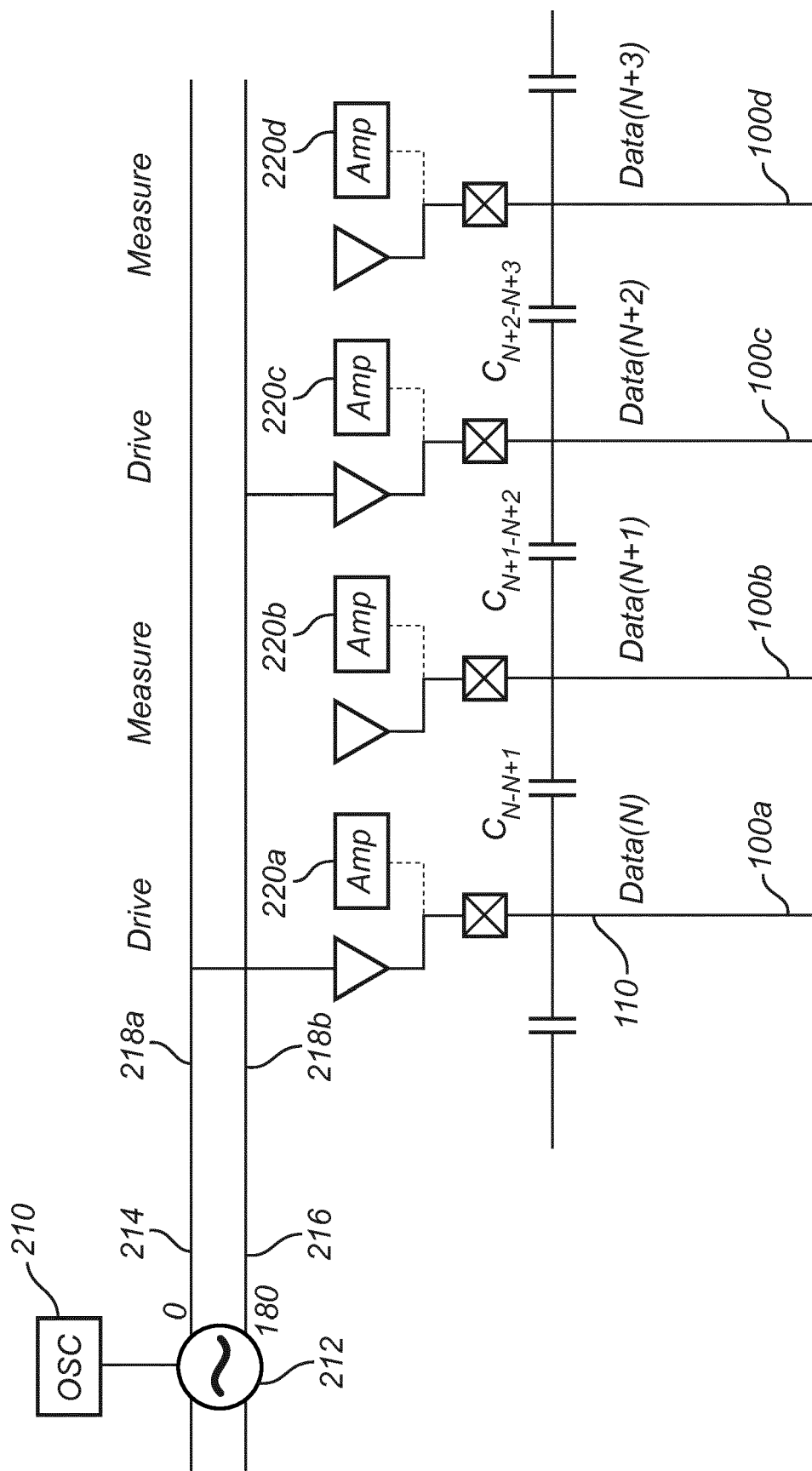


Fig. 9a

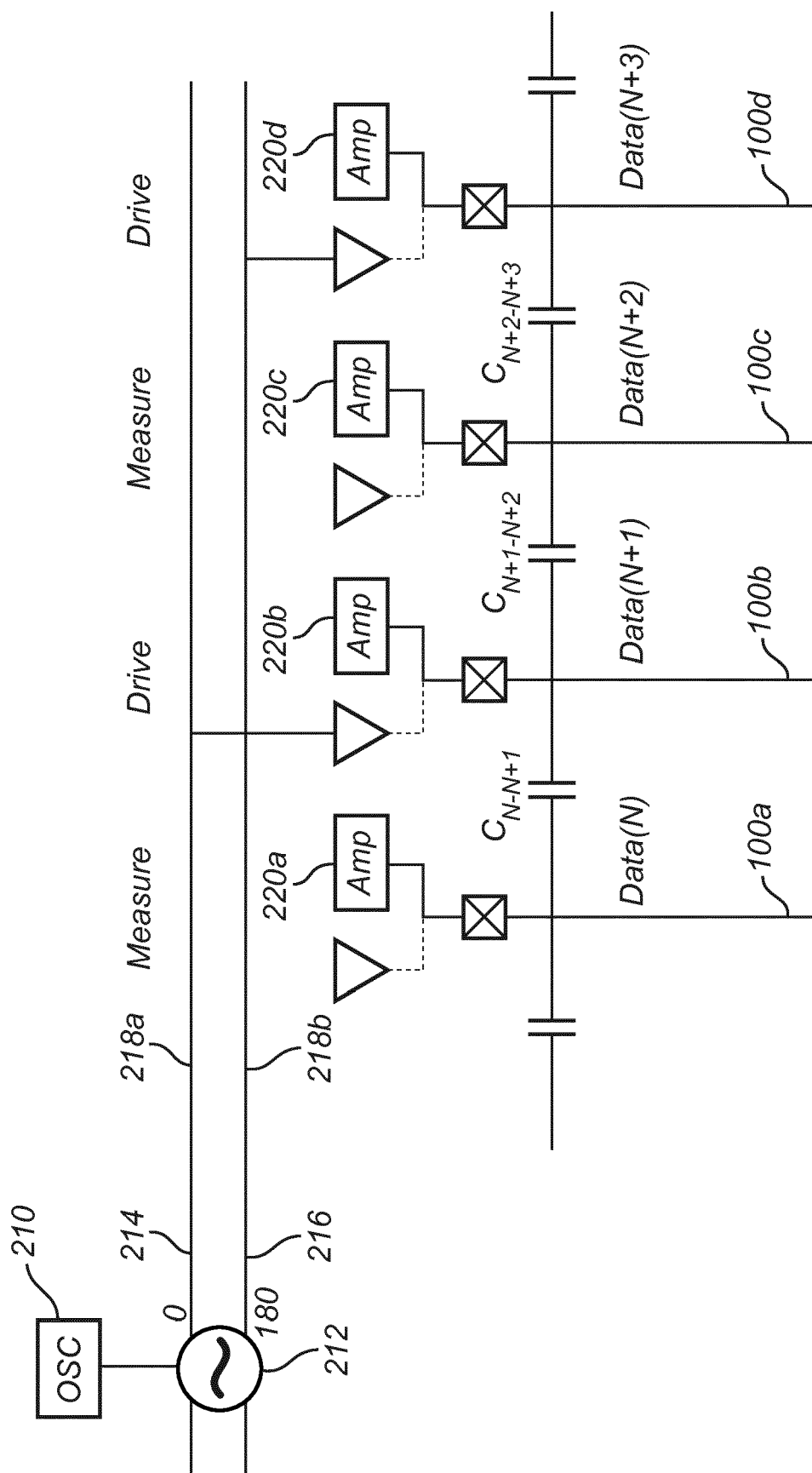
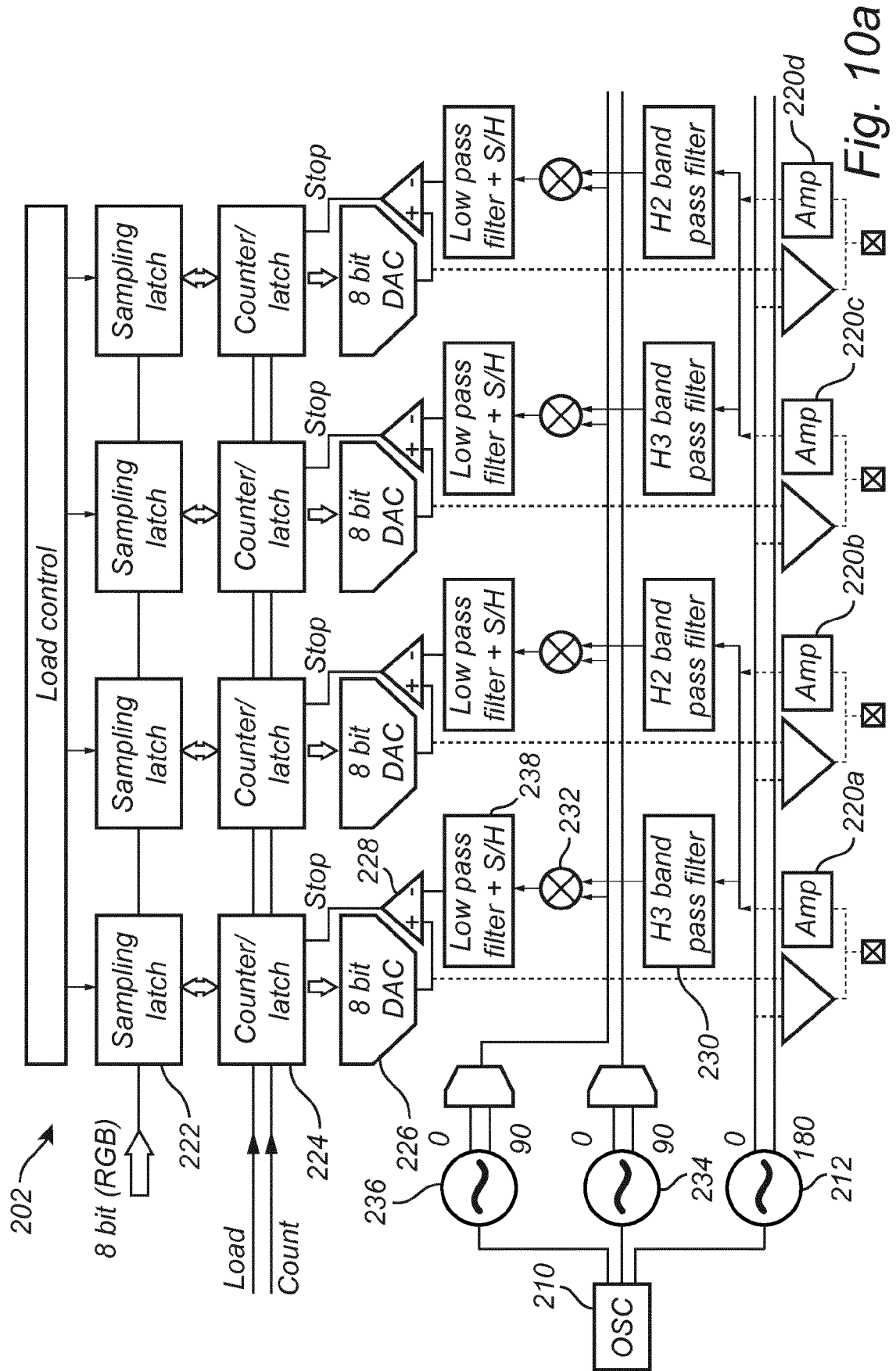


Fig. 9b



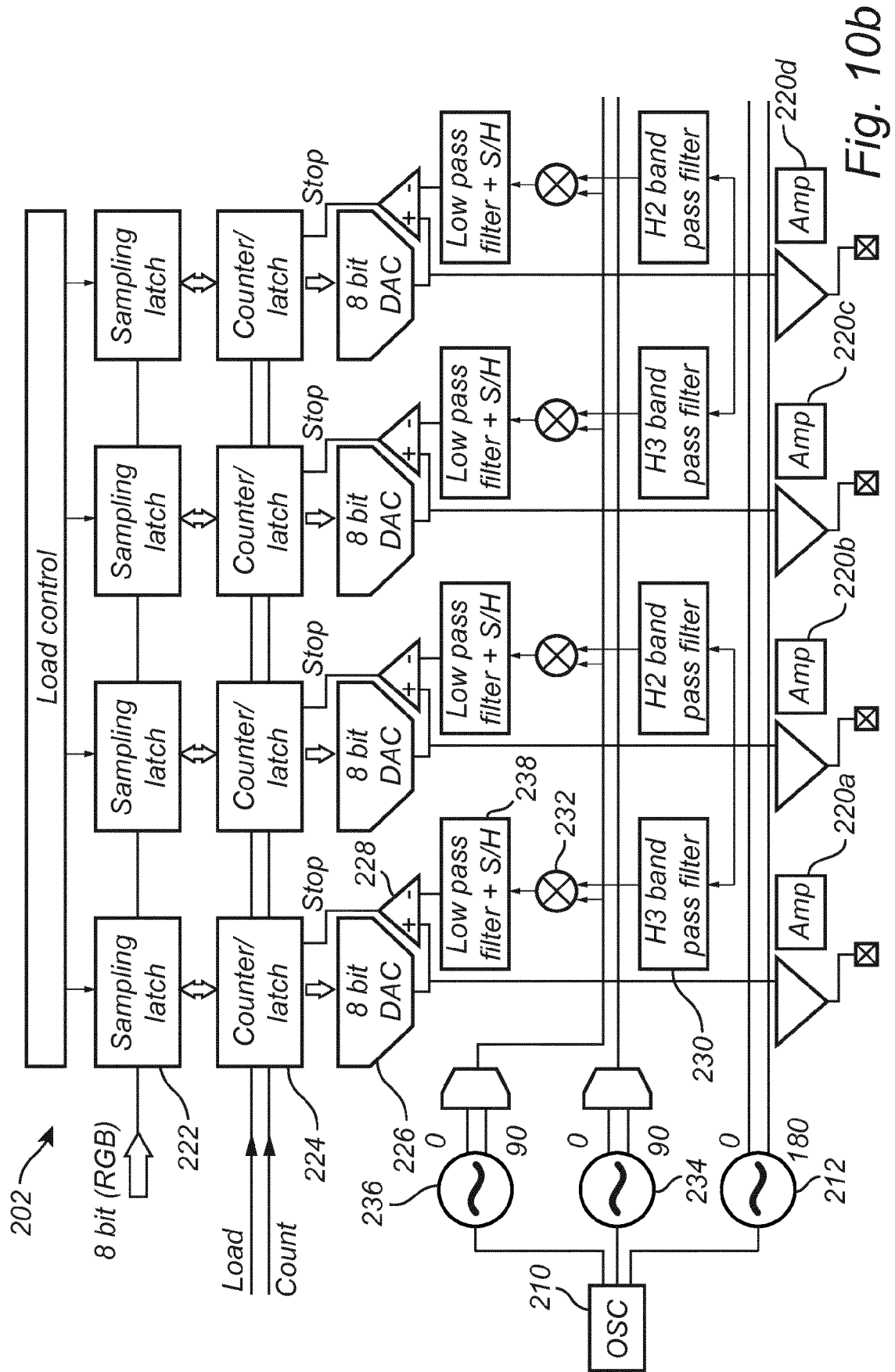


Fig. 10b

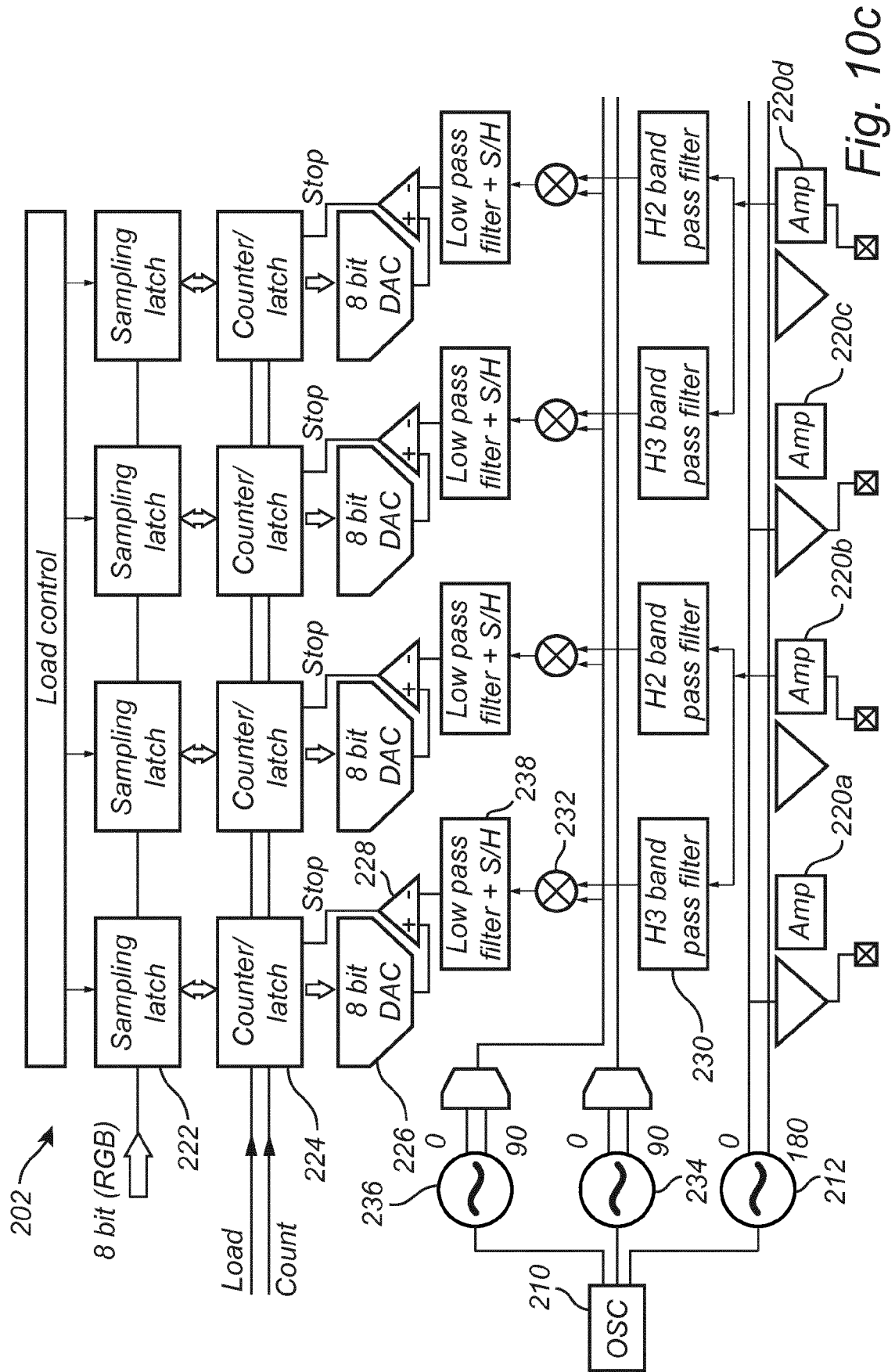
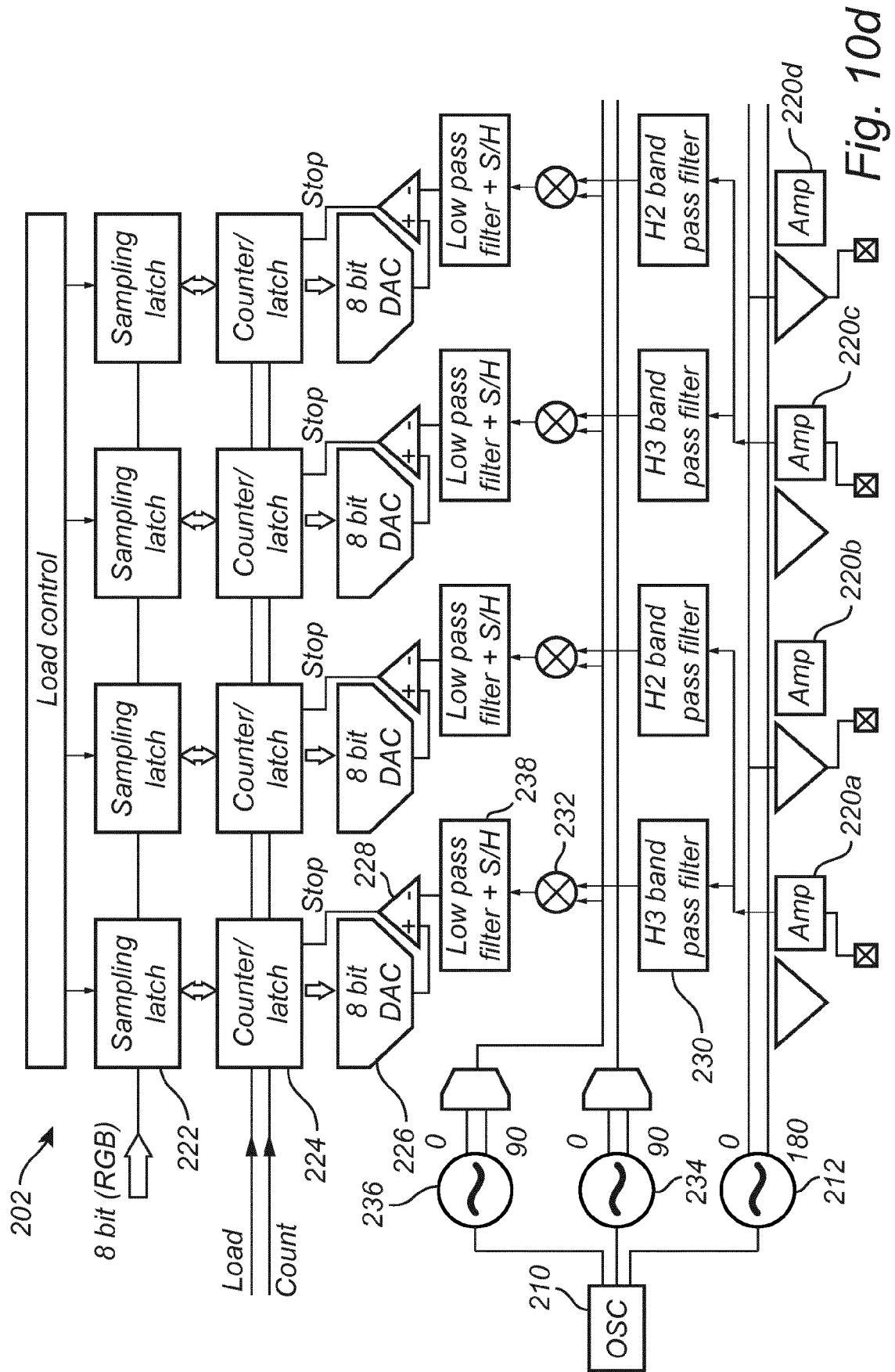


Fig. 10c



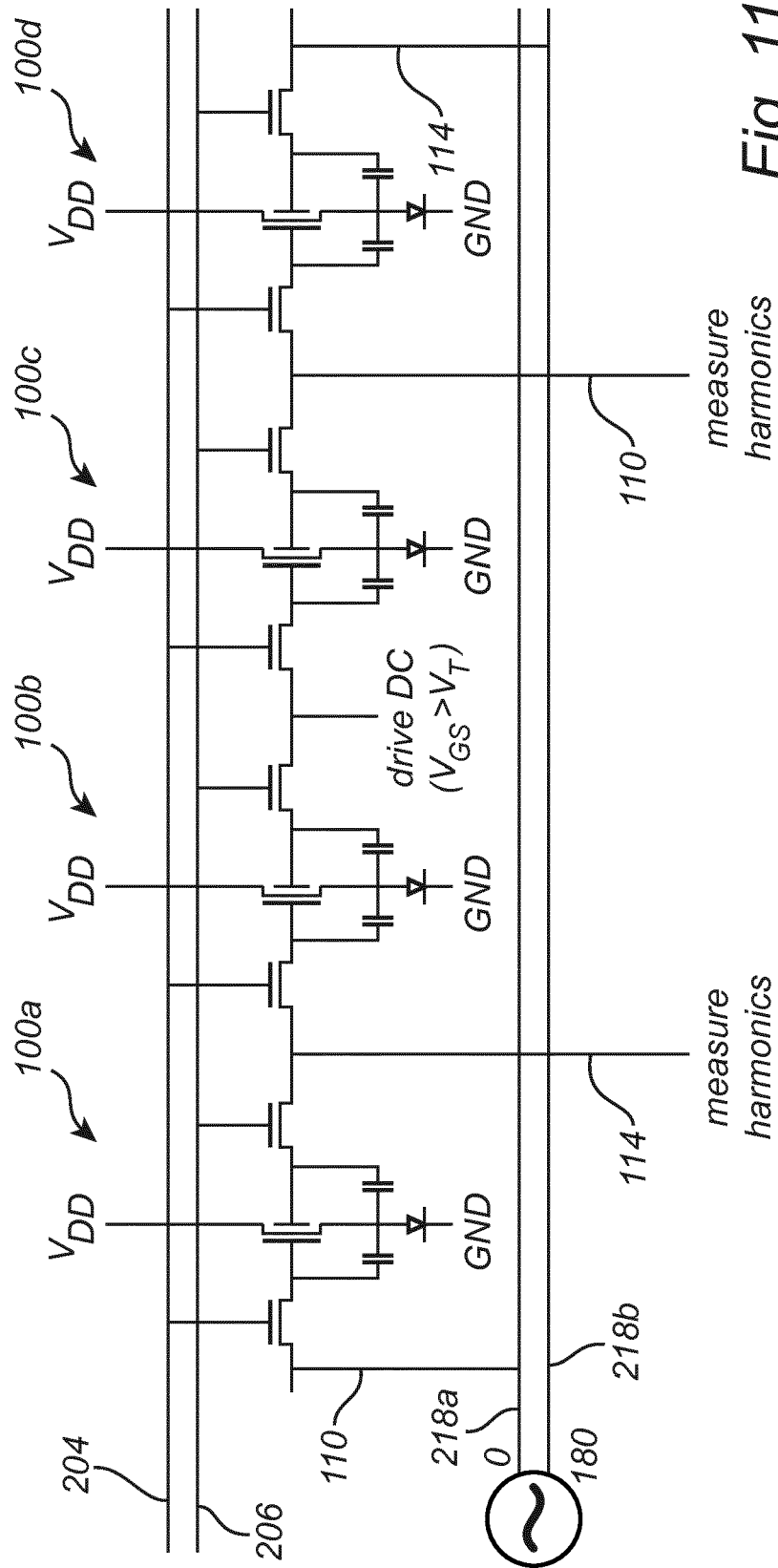
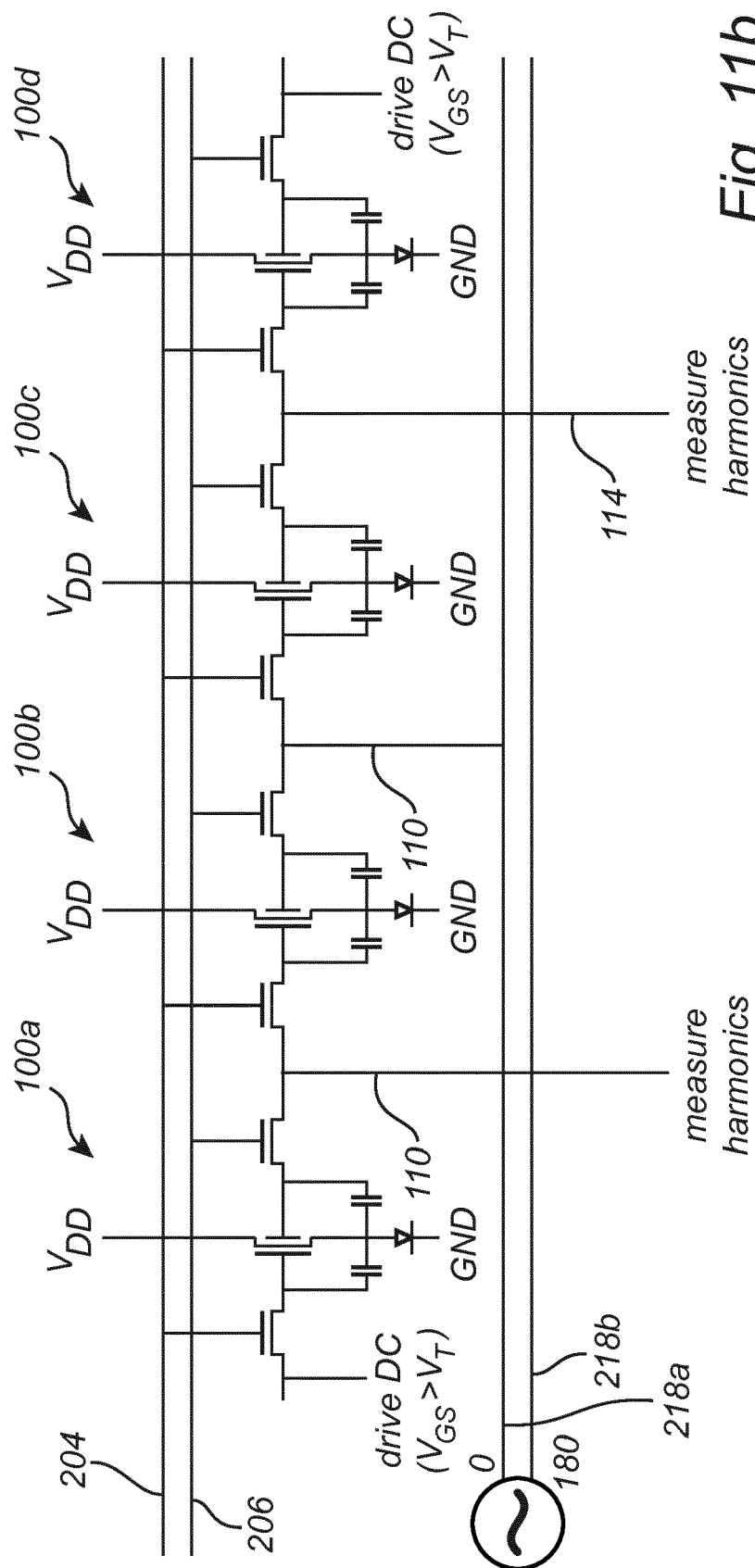
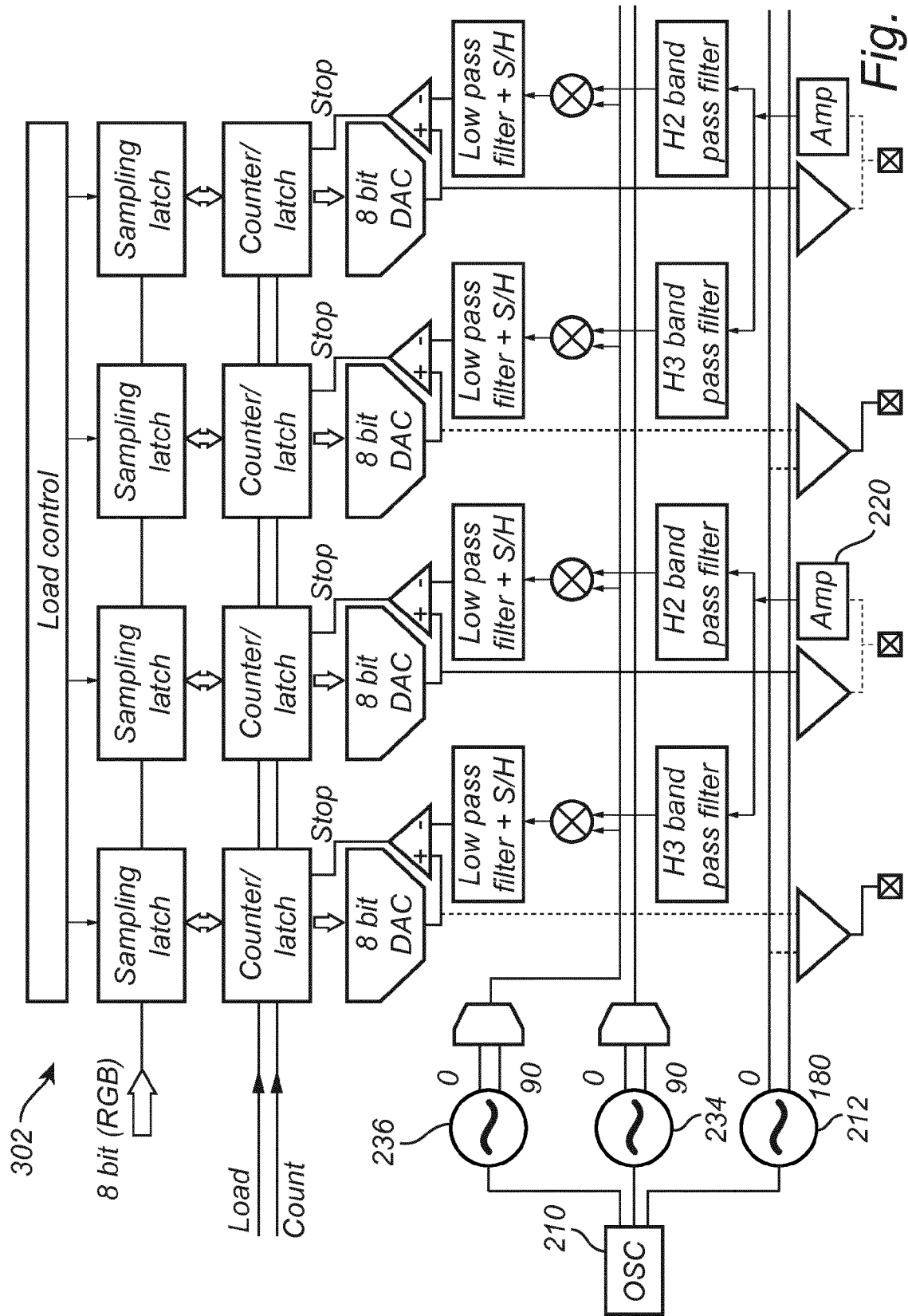
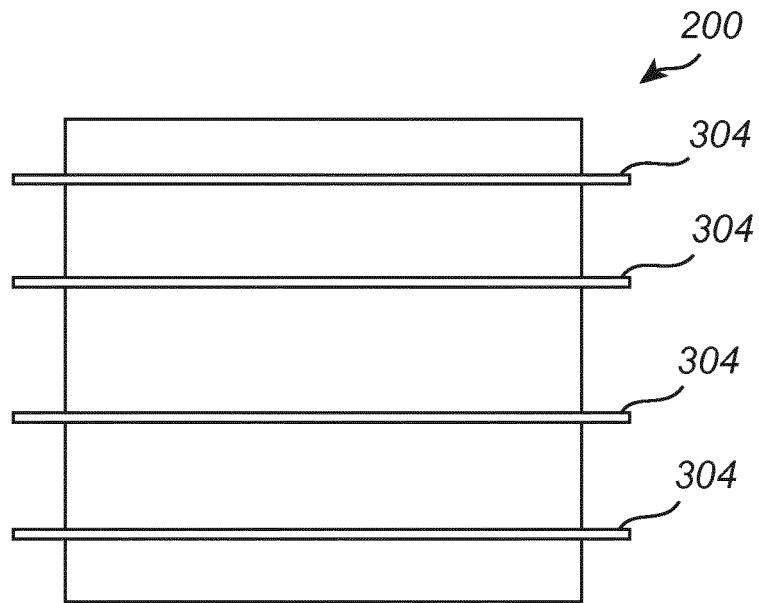


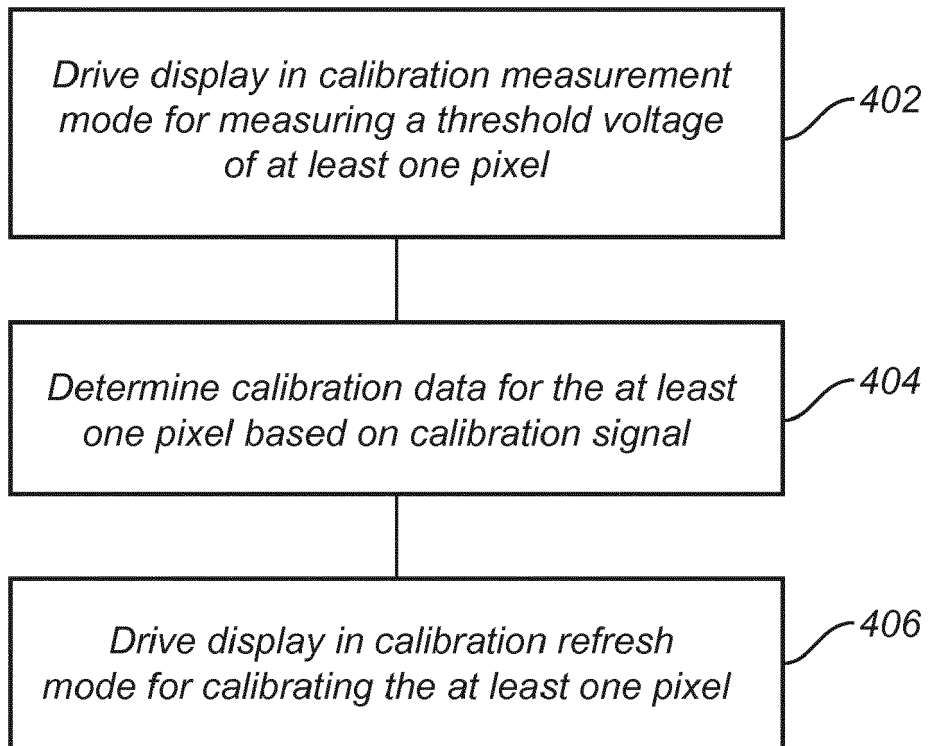
Fig. 11a







*Fig. 12*



*Fig. 13*



## EUROPEAN SEARCH REPORT

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| DOCUMENTS CONSIDERED TO BE RELEVANT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                           |                                  |                                         |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------|
| Category                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Citation of document with indication, where appropriate, of relevant passages             | Relevant to claim                | CLASSIFICATION OF THE APPLICATION (IPC) |
| X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | US 2015/317951 A1 (GENOE JAN [BE])<br>5 November 2015 (2015-11-05)                        | 11-15                            | INV.<br>G09G3/3275                      |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | * paragraphs [0002], [0010], [0017], [0018], [0061], [0071], [0072]; figures 2,6,7,9,10 * | 1-10                             |                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | -----                                                                                     |                                  |                                         |
| X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | US 2015/236687 A1 (SHIMADA YUKIMINE [JP] ET AL) 20 August 2015 (2015-08-20)               | 1-10                             |                                         |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | * paragraphs [0041], [0042], [0060], [0065] - [0067]; figures 3, 4 *                      | 11-15                            |                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | -----                                                                                     |                                  |                                         |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | US 2013/063413 A1 (MIYAKE HIROYUKI [JP])<br>14 March 2013 (2013-03-14)                    | 1-15                             |                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | * paragraphs [0004], [0033] - [0036], [0053]; figures 1, 3,4, 6A, 6B *                    |                                  |                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | -----                                                                                     |                                  |                                         |
| The present search report has been drawn up for all claims                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                           |                                  | TECHNICAL FIELDS SEARCHED (IPC)         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                           |                                  | G09G                                    |
| Place of search                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                           | Date of completion of the search | Examiner                                |
| The Hague                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                           | 3 August 2017                    | Fanning, Neil                           |
| CATEGORY OF CITED DOCUMENTS<br>X : particularly relevant if taken alone<br>Y : particularly relevant if combined with another document of the same category<br>A : technological background<br>O : non-written disclosure<br>P : intermediate document<br>T : theory or principle underlying the invention<br>E : earlier patent document, but published on, or after the filing date<br>D : document cited in the application<br>L : document cited for other reasons<br>& : member of the same patent family, corresponding document |                                                                                           |                                  |                                         |

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ON EUROPEAN PATENT APPLICATION NO.**

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5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.  
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03-08-2017

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