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(54) **INTEGRATED CIRCUIT, CIRCUIT ASSEMBLY AND A METHOD FOR ITS OPERATION**

INTEGRIERTE SCHALTUNG, SCHALTUNGSANORDNUNG UND VERFAHREN ZUM BETRIEB DAVON

CIRCUIT INTÉGRÉ, ENSEMBLE CIRCUIT ET SON PROCÉDÉ DE FONCTIONNEMENT

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## Description

**[0001]** The present invention relates to an integrated circuit comprising at least one supply voltage terminal, at least one input terminal configured to receive an analog input signal corresponding to an audio signal, and at least one output terminal, wherein the integrated circuit is configured to amplify the audio signal received from the input terminal and to output a corresponding amplified signal at the at least one output terminal. Furthermore, the invention relates to a circuit assembly comprising a signal source, a signal processing device and an amplifier circuit arranged in a signal path between the signal source and the signal processing device. Moreover, the present invention relates to a method for operating a circuit assembly comprising a signal source, an amplifier circuit, and a signal processing device.

**[0002]** Integrated circuits, circuit assemblies and corresponding methods for their operation are known from the field of signal processing in general. In particular, such circuit arrangements can be used at an analog stage for amplifying a signal provided by a microphone or similar transducer.

**[0003]** In many applications, processing of signals having a high dynamic range is desirable. For example, when recording an audio or audio-visual performance using a portable device, both quiet and loud passages of the performance should be recorded with high-fidelity. However, in particular when using battery operated, mobile devices, the dynamic range of a processing device is often limited. For example, the dynamic range of an analog-to-digital converter used to convert an analog audio signal for a subsequent digital signal processing device may be restricted by the supply voltage available from the battery. In order to maintain a reasonable resolution over the entire signal range, some form of signal preconditioning may be used. For example, an analog signal provided by a microphone may be preamplified using an amplifier having an automatic gain control circuit. In this way, quieter passages of the performance can be amplified using a higher amplification setting, resulting in a greater signal amplitude, while louder parts of the performance can be amplified using a lower amplification setting.

**[0004]** In this context, US 2014/0185832 A1 discloses an assembly including the signal processing unit SPU shown in Figure 4. A signal path SL guides from an analog signal input $IN_A$ to an analog signal output $OUT_A$. Within the signal path SL, an amplifier LNA is arranged to amplify the useful analog signal fed to the analog signal input $IN_A$ and guides the amplified signal to the analog signal output $OUT_A$. Coupled to the signal path SL and the amplifier LNA is an automatic gain control AGC controlling the gain of the amplifier LNA. Gain information about the current gain is provided by the automatic gain control AGC as a digital or analog signal which is delivered to a gain information output DGI. Thus, the signal processing unit SPU comprises an analog signal output $OUT_A$ and further the gain information output DGI.

**[0005]** The information provided at the gain information output DGI may be useful for further processing the amplified analog signal where information about the sensitivity of the signal processing unit SPU is needed. However, the circuit assembly disclosed in US 2014/0185832 A1 requires the provision of an additional terminal for providing the gain information. In particular in highly integrated circuits and miniaturized circuit design, the provision of an additional terminal may be problematic. Furthermore, such a circuit assembly may not be used in existing chip packages or circuit arrangements, which do not allow the provision of an additional terminal to supply the required gain information.

**[0006]** US 4,457,020 A shows a signal processor for processing communication signals by extracting amplitude information from an input signal and converting this amplitude information into two signal tones. US 4,944,024 A discloses a method and an apparatus for reducing noise fluctuation in a linked compressor-expander telecommunications system in which an artificial tone signal is injected into a demodulator of the communication system to bias the output toward self quieting. US 2012/250893 A1 describes a system for controlling a dynamic range of an audio signal.

**[0007]** It is therefore a challenge of the present invention to provide alternative devices, systems and methods, which allow signal processing with a high dynamic range and which are compatible with existing circuit arrangement. Preferably, they should be compatible with existing connection schemes, as given by the number and type of terminals of known integrated amplifier circuits.

**[0008]** The present invention discloses an integrated circuit in accordance with appended independent apparatus claim 1 and a method for operating a circuit assembly in accordance with appended independent method claim 12.

**[0009]** Further advantageous embodiments of the present invention are disclosed in the attached claims as well as the detailed description of the currently preferred embodiments.

**[0010]** Various embodiments of the present invention will be described with reference to the attached figures. Therein, the same reference symbols will be used with respect to similar features of different embodiments. Unless otherwise stated, the description of a particular feature described with respect to one embodiment equally applies to a corresponding feature of the other embodiments.

Figure 1A shows a simplified diagram of a first circuit assembly according to a first embodiment not covered by the scope of the claimed invention but useful for understanding the invention.

Figure 1B shows a first signaling diagram for the circuit assembly according to Figure 1A.

Figure 1C shows a second signaling diagram for the

circuit assembly according to Figure 1A.

Figure 2A shows a simplified diagram of a second circuit assembly according to a reference embodiment not covered by the scope of the claimed invention but useful for understanding the invention.

Figure 2B shows a signaling diagram for the circuit assembly according to Figure 2A.

Figure 3A shows a simplified diagram of a third circuit assembly according to a second embodiment.

Figure 3B shows a signal diagram for the circuit assembly according to Figure 3A.

Figure 4 shows a signal processing unit according to the prior art.

**[0011]** According to a first embodiment, not covered by the scope of the claimed invention but useful for understanding the invention, shown in Figure 1A, an additional high frequency signal is superimposed on an output signal of an amplifier circuit.

**[0012]** Figure 1A shows a circuit assembly 100 comprising a signal source 110, an application specific integrated circuit (ASIC) 120 implementing an amplifier circuit, and a signal processing device 190. In the described embodiment, the signaling source 110 comprises a differential microphone 112. The microphone 112 is connected to the ASIC 120 by means of two input terminals 122 and 124. For example, the first input terminal 122 may be a positive input terminal, and the second input terminal 124 may be a negative input terminal of a differential signal line. The analog signal provided via the input terminals 122 and 124 is amplified by an amplifier 126 and the output signal of the amplifier 126 is provided at two output terminals 132 and 134 of a differential signal output.

**[0013]** In the described embodiment, the amplifier 126 is a preamplifier with two different gain settings. The gain setting is selected based on a control signal High_SPL generated by signal strength detector in the form of a sound pressure monitor 136. If the detected sound pressure at the input terminals 122 and 124 exceeds a predetermined threshold, the control signal High_SPL is provided to the amplifier 126. If the sound pressure level lies below the predetermined threshold level, the corresponding control signal is not provided. The control signal High_SPL is also provided to a logic circuit 138 and used as a mask signal to mask a high frequency clock signal which is provided by a clock generator 140. For example, the clock generator 140 may provide a fixed frequency signal with a frequency of 25 kHz. If the control signal High_SPL is provided to the logic circuit 138, the signal generated by the clock generator 140 is used to operate a switch 142. The switch 142 connects the negative output terminal 134 over an internal resistor R with a terminal 144 for connecting the ASIC 120 to an electrical ground potential 146. In this way, an additional signal with a frequency of the clock signal generated by the clock generator 140 is superimposed onto the output signal provided by the ASIC 120.

**[0014]** In the described embodiment, the signal processing device 190 comprises an analog-to-digital converter 192 as well as a digital CODEC 194. Based on a frequency spectrum analysis performed by the CODEC 194, the additional signal generated by the signaling circuit of the ASIC 120 can be detected. Accordingly, the signal processing device 190 can be made aware of the amplification setting of the amplifier 126 and process the amplified signal accordingly.

**[0015]** Figure 1B shows a signal level of the control signal High_SPL over time together with a frequency response of the ASIC 120. As can be seen in the lower part of Figure 1B, in the time period between $t_1$ and $t_2$, in which a high sound pressure level is detected by the sound pressure monitor 136, an additional high frequency signal with a frequency f1 is provided. In the embodiment described with respect to Figure 1B, the additional signal is provided as long as the control signal High_SPL is high. The frequency f1 of the provided signal lies above the bandwidth of an audio signal provided by the microphone 112, which is amplified by the ASIC 190. In this way, the provision of the additional signal does not interfere with the useful signal provided to the signal processing device 190.

**[0016]** Figure 1C shows an alternative signaling scheme according to another embodiment. In this embodiment, the control signal High_SPL is also provided to the clock generator 140.

**[0017]** According to the control signal High_SPL, the clock generator 140 generates a clock frequency with either a first frequency or a second, different frequency, resulting in an additional signal tone with a first frequency f1 or a second frequency f2, respectively. Moreover, the logic circuit 138 according to this embodiment is configured to pass the clock signal only for a predetermined period of time after the control signal High_SPL has changed. Accordingly, after switching to a low gain setting for a high sound pressure at time $t_2$, a signal tone with a frequency f1 is superimposed on the output signal for a predetermined time period. After switching to a high gain setting for a low sound pressure at time $t_3$, a signal tone with the frequency f2 is superimposed on the output signal for the predetermined time period. In time periods, in which the control signal High_SPL is stable, e.g. at times $t_1$ and $t_4$, no additional signal tone is superimposed on the output signal.

**[0018]** Alternatively, in an embodiment not shown, a second signal tone with the same frequency as used before is superimposed on the output signal after switching the amplifier 126 back to the a high gain setting. In this embodiment, the ASIC 120 starts in a predefined normal mode on activation, e.g. with a high gain setting, and then, on each toggling of the amplification setting, super-

imposes a signal tone with the same frequency, e.g. frequency f1, on the output signal.

**[0019]** According to a reference embodiment shown in Figure 2A which is not within the scope of the present invention, a current signal is superimposed on a normal current consumption of an amplifier circuit. Moreover, instead of an adjustable amplifier, an adjustable bias voltage generator is used to change an amplification ratio of the amplifier circuit.

**[0020]** Figure 2A shows a circuit assembly 200 comprising an application specific integrated circuit (ASIC) 220 implementing an amplifier circuit and a load detection circuit 280. Its intended function and use is similar to that of the ASIC 120 according to the first embodiment. However, in the reference embodiment shown in Figure 2A, a signal provided by a single ended transducer (not shown) is provided at a single input terminal 222, amplified by an amplifier 126 and provided as an amplified signal at a single output terminal 232 for a subsequent signal processing device (not shown).

**[0021]** The ASIC 220 further comprises a bias voltage generator 228 for generating a bias voltage for a microphone (not shown in Figure 2A) connected to the input terminal 224. Depending on the microphone type, the bias voltage may be provided separately by means of a bias voltage terminal 230 as shown in Figure 2A or may be superimposed on the input signal and provided over the input terminal 222. Instead of changing an amplification ratio of the amplifier 126 directly, in the reference embodiment, the bias voltage provided by the bias voltage generator 228 is modified in accordance with a control signal High_SPL indicating a high sound pressure level. If a high sound pressure level is detected, a low bias voltage is supplied to the microphone resulting in a low amplification setting, and vice versa.

**[0022]** In the described reference embodiment, a supply voltage Vdd is provided to the ASIC 220 by means of a supply voltage terminal 262. The supply voltage Vdd supplied at supply voltage terminal 262 is used, among others, to power the bias voltage generator 228, the amplifier 126, a logic circuit 264, and a sound pressure monitor 136. In the reference embodiment shown in Figure 2A, the control signal High_SPL determined by the sound pressure monitor 136 is provided to the bias voltage generator 228 and the logic circuit 264. Depending on the control signal High_SPL the logic circuit 264 selectively closes a first switch 266 or a second switch 268. By closing the first switch 266, a first internal load R1 is connected to the supply voltage terminal 262. By closing the second switch 268, a second internal load R2 is connected to the supply voltage terminal 262.

**[0023]** The load detection circuit 280 comprises a detection resistor Rext. Based on the voltage drop across the detection resistor Rext, a current Idd through the ASIC 220 can be determined. Moreover, if the current consumption Idd0 of the ASIC 220 without activated loads R1 and R2 is known, based on the detected current Idd, activation of the loads R1 and R2 can be detected by the load detection circuit 280. Although not shown in Figure 2A, the load detection circuit 280 provides a corresponding control signal to any subsequent processing device which requires knowledge about the amplification setting of the ASIC 220.

**[0024]** The operation of the circuit assembly 200 according to Figure 2A can best be understood with reference to the signal diagram of Figure 2B. Therein, one can see that, immediately after a transition from a mode with high amplification to a mode with low amplification, i.e. a transition of the control signal High_SPL from a low state to a high state, a first peak on the input current signature of the ASIC 220 to an operating current Idd1 corresponding to the activation of the first load R1 can be observed for a predetermined period of time. After the predetermined time period, the first load R1 is disconnected by the logic circuit 264 using the first switch 266 and the current of the ASIC 220 returns to its nominal current Idd0. At the subsequent transition from a state with high sound pressure level to a state with low sound pressure level, a second peak is imprinted on the current signature of the ASIC 220. The peak current consumption in this period corresponds to Idd2. If the second peak differs in amplitude to the first peak as shown in Figure 2A, an absolute amplification setting may be communicated to the load detection circuit 280. Alternatively, the second peak may have the same amplitude as the first peak in order to encode a cyclic mode change or mode toggling as described above with respect to the first embodiment. Since the additional loads R1 and R2 are only activated for relatively short periods, they do not significantly affect the energy efficiency of the circuit assembly 200.

**[0025]** Of course, the additional load R1 may also be activated for the entire duration in which the amplifier 126 is operated in the first amplification setting. In this case, no additional load may be necessary to indicate the second amplification signal. Preferably, if the characteristics of the signal source 110 are known, the additional load is activated in the operation mode of the amplifier that is used less in order to improve the energy efficiency of the ASIC 220.

**[0026]** According to a second embodiment of the present invention shown in Figure 3A, a DC shift is applied to the output signal of an amplifier circuit.

**[0027]** Figure 3A shows a circuit assembly 300 comprising a signal source 110, an application specific integrated circuit (ASIC) 320 implementing an amplifier circuit and a signal processing device 390. Its intended function and use is similar to that of the ASIC 120 according to the first embodiment.

**[0028]** The ASIC 320 shown in Figure 3A is connected to a differential microphone 112. In order to signal an amplification setting of an adjustable amplifier 126, a DC shift is forced to the common mode output voltage at output terminals 132 and 134 of the ASIC 320. Typically, the output voltage of an amplifier circuit is centered on a mid-rail voltage, for example around 0.9 V for an ASIC

320 having a supply voltage Vdd of 1.8 V. In order to shift the DC component of the output terminals 132 and 134, the sound pressure monitor 136 provides a control signal High_SPL to a DC shifter 372. In the described embodiment, a bias voltage of for example 0.4 V is superimposed on the amplified output signal at the output terminals 132 and 134.

**[0029]** In the signal processing device 390, a DC detector 396 may be used to detect the DC shift. Moreover, a subsequent subtraction unit 398 will automatically cancel out any DC component provided by the DC shifter 372, such that the signal provided at the output tunnels 132 and 134 can be processed in the same way as in a conventional system.

**[0030]** As shown in Figure 3B, the DC shift may only be provided for a short period after the transition from one amplification setting to another amplification setting. For example, when changing from an amplification setting suitable for a low sound pressure level to an amplification setting suitable for a high sound pressure level, a negative DC shift to voltage level Vo1 may be provided for a predetermined period of time. Inversely, when switching back to the previous amplification setting, a DC voltage shift to the voltage potential of Vo2 may be provided. Alternatively, as described above, a "toggle" signal may be provided using only a positive or negative offset at changes of the amplification setting, or a corresponding signaling may be applied as long as a particular amplification setting is used by the amplifier 126.

**[0031]** Although the invention has been described with respect to amplifier circuits having only two different amplification settings, i.e. two different gain values or bias voltage levels, the invention can also be applied to signal strength detectors and corresponding automatic gain circuits or automatic bias controllers having a plurality of levels. For example, each amplification setting could be communicated by a corresponding DC shift. Moreover, even an analog gain setting or microphone bias voltage change may be indicated based on a corresponding DC offset.

**[0032]** While the embodiment has been described with respect to ASICs 120, 220 and 320, other integrated circuits or circuit arrangements may be used to implement the amplifier circuit. Any such circuit only needs to comprise a supply voltage terminal, a ground potential terminal, one or two input terminals and one or two output terminals. Thus, a conventional chip package having between 4 and 6 output pins can be used in accordance with the present invention.

List of References

**[0033]**

| | |
|---|---|
| 100 | circuit assembly |
| 110 | signal source |
| 112 | microphone |
| 120 | ASIC (amplifier circuit) |
| 122, 124 | input terminal |
| 126 | amplifier |
| 132, 134 | output terminal |
| 136 | sound pressure monitor |
| 138 | logic circuit |
| 140 | clock generator |
| 142 | switch |
| 144 | ground terminal |
| 146 | ground potential |
| 190 | signal processing device |
| 192 | analog digital converter (ADC) |
| 194 | CODEC |
| 200 | circuit assembly |
| 220 | ASIC (amplifier circuit) |
| 222 | input terminal |
| 228 | bias voltage generator |
| 230 | bias voltage terminal |
| 232 | output terminal |
| 262 | supply voltage terminal |
| 264 | logic circuit |
| 266 | switch |
| 268 | switch |
| 280 | load detection circuit |
| 300 | circuit assembly |
| 320 | ASIC (amplifier circuit) |
| 372 | DC shifter |
| 390 | signal processing device |
| 396 | DC detector |
| 398 | subtraction unit |

**Claims**

**1.** An integrated circuit, comprising

- at least one supply voltage terminal configured to receive a supply voltage (Vdd) for operation of the integrated circuit;
- at least one input terminal (122, 124) configured to receive an analog input signal corresponding to an audio signal;
- a differential signal output comprising two output terminals (132, 134) configured to provide an analog output signal; and
- a signal strength detector (136) configured to detect a signal strength of the analog input signal provided at the at least one input terminal (122, 124), wherein the integrated circuit is configured to amplify the audio signal wherein an amplification setting is selected based on the detected signal strength and to output a corresponding amplified signal corresponding to the analog output signal at the differential signal output;

wherein the integrated circuit further comprises a signaling circuit configured to indicate the amplification setting of the integrated circuit at the differential sig-

nal output wherein the signaling circuit comprises a DC shifter (372) and is connected to the two output terminals (132, 134), the signaling circuit being configured to generate a predetermined first offset voltage and to superimpose a common mode output voltage of the two output terminals (132, 134) with the predetermined first offset voltage corresponding to a DC shift if the amplification setting of the integrated circuit is a first amplification setting, and not to superimpose the common mode output voltage of the two output terminals (132, 134) with the predetermined offset voltage or to superimpose the common mode output voltage of the two output terminals (132, 134) with a predetermined second offset voltage, if the amplification setting of the integrated circuit is a second amplification setting.

**2.** The integrated circuit according to claim 1, wherein the signaling circuit is configured to provide a first control signal to indicate the first amplification setting for a first predetermined time period when the integrated circuit is switched into an operating mode using the first amplification setting, and to provide a second control signal to indicate the second amplification setting for a second predetermined time period when the integrated circuit is switched into an operating mode using the second amplification setting.

**3.** The integrated circuit according to claim 1, wherein the signaling circuit is configured to provide a first control signal to indicate the first amplification setting as long as the integrated circuit is operating using the first amplification setting, and not to provide the first control signal or to provide a second control signal to indicate the second amplification setting as long as the integrated circuit is operating using the second amplification setting.

**4.** The integrated circuit according to one of claims 1 to 3, further comprising an adjustable amplifier (126) configured to be operated with one of a plurality of different gain settings in accordance with the amplification setting.

**5.** The integrated circuit according to one of claims 1 to 3, further comprising a bias voltage generator (228) configured to be operated with one of a plurality of different microphone bias voltage settings in accordance with the amplification setting.

**6.** The integrated circuit according to one of claims 1 to 5, wherein the signal strength detector (136) is configured to determine a sound pressure level of the audio signal.

**7.** The integrated circuit according to one of claims 1 to 6, comprising a first input terminal (122) and a second input terminal (124), the first and the second input terminals (122, 124) being configured as an input for a differential signal source (110).

**8.** The integrated circuit according to one of claims 1 to 7, comprising a first output terminal (132) and a second output terminal (134), the first and the second output terminals (132, 134) being configured as a signal output for a differential signal processing device (390).

**9.** A circuit assembly (300) comprising the integrated circuit according to one of claims 1 to 8 and further comprising:

- a signal source (110) providing the audio signal;
- a signal processing device (390) configured to process the analog output signal; and
- wherein the integrated circuit further comprises an amplifier circuit (320) comprising the signal strength detector (136) and the signaling circuit (372), the amplifier circuit (120, 220, 320) being arranged in a signal path between the signal source (110) and the signal processing device (190);
- wherein the amplifier circuit (120, 220, 320) is configured to amplify the analog input signal.

**10.** The circuit assembly (100, 300) according to claim 9, wherein the signal source (110) comprises a high dynamic range analog microphone (112).

**11.** The circuit assembly according to any one of the claims 9 or 10, wherein the signal processing device (190, 390) comprises at least one of an analog-to-digital converter (192), an analog signal processor, a microcontroller, a digital signal processor, an audio codec (194), and a power amplifier.

**12.** A method for operating a circuit assembly (300) according to any of claims 9 to 11, the method comprising:

- detecting a signal strength of the analog input signal provided by the signal source (110);
- selecting the amplification setting based on the detected signal strength;
- amplifying the analog input signal based on the amplification setting and providing the amplified signal to the signal processing device (390); and
- signaling the amplification setting to the signal processing device (390) by modifying the amplified signal provided to the signal processing device ( 390) by generating a predetermined first offset voltage and superimposing a common mode output voltage of the two output terminals (132, 134) with the predetermined first

offset voltage corresponding to a DC shift if the amplification setting of the integrated circuit is a first amplification setting, and not superimposing the common mode output voltage of the two output terminals (132, 134) with the predetermined offset voltage or superimposing the common mode output voltage of the two output terminals (132, 134) with a predetermined second offset voltage, if the amplification setting of the integrated circuit is a second amplification setting.

**Patentansprüche**

**1.** Integrierte Schaltung, aufweisend:

- mindestens einen Versorgungsspannungsanschluss, der so ausgebildet ist, dass er eine Versorgungsspannung (Vdd) für den Betrieb der integrierten Schaltung erhält;
- mindestens einen Eingangsanschluss (122, 124), der so ausgebildet ist, dass er ein analoges Eingangssignal empfängt, das einem Audiosignal entspricht;
- einen Differenzsignalausgang, der zwei Ausgangsanschlüsse (132, 134) umfasst, die so ausgebildet sind, dass sie ein analoges Ausgangssignal liefern; und
- einen Signalstärkedetektor (136), der so ausgebildet ist, dass er eine Signalstärke des analogen Eingangssignals erfasst, das an dem mindestens einen Eingangsanschluss (122, 124) bereitgestellt wird, wobei die integrierte Schaltung ausgebildet ist, das Audiosignal zu verstärken, wobei eine Verstärkungseinstellung auf der Grundlage der erfassten Signalstärke ausgewählt wird, und um ein entsprechendes verstärktes Signal, das dem analogen Ausgangssignal entspricht, am Differenzsignalausgang auszugeben;

wobei die integrierte Schaltung ferner eine Signalisierungsschaltung umfasst, die so ausgebildet ist, dass sie die Verstärkungseinstellung der integrierten Schaltung am Differenzsignalausgang anzeigt, wobei die Signalisierungsschaltung einen DC-Shifter (372) umfasst und mit den beiden Ausgangsanschlüssen (132, 134) verbunden ist, wobei die Signalisierungsschaltung ausgebildet ist, eine vorbestimmte erste Offset-Spannung zu erzeugen und eine Gleichtakt-Ausgangsspannung der beiden Ausgangsanschlüsse (132, 134) mit der vorbestimmten ersten Offset-Spannung entsprechend einer DC-Verschiebung zu überlagern, wenn die Verstärkungseinstellung der integrierten Schaltung eine erste Verstärkungseinstellung ist, und die Gleichtakt-Ausgangsspannung der beiden Ausgangsanschlüsse (132, 134) nicht mit der vorbestimmten Offsetspannung zu überlagern oder die Gleichtakt-Ausgangsspannung der beiden Ausgangsanschlüsse (132, 134) mit einer vorbestimmten zweiten Offset-Spannung zu überlagern, wenn die Verstärkungseinstellung der integrierten Schaltung eine zweite Verstärkungseinstellung ist.

**2.** Integrierte Schaltung nach Anspruch 1, wobei die Signalisierungsschaltung so ausgebildet ist, dass sie ein erstes Steuersignal bereitstellt, um die erste Verstärkungseinstellung für eine erste vorbestimmte Zeitspanne anzuzeigen, wenn die integrierte Schaltung unter Verwendung der ersten Verstärkungseinstellung in einen Betriebsmodus geschaltet wird, und dass sie ein zweites Steuersignal bereitstellt, um die zweite Verstärkungseinstellung für eine zweite vorbestimmte Zeitspanne anzuzeigen, wenn die integrierte Schaltung unter Verwendung der zweiten Verstärkungseinstellung in einen Betriebsmodus geschaltet wird.

**3.** Integrierte Schaltung nach Anspruch 1, wobei die Signalisierungsschaltung so ausgebildet ist, dass sie ein erstes Steuersignal liefert, um die erste Verstärkungseinstellung anzuzeigen, solange die integrierte Schaltung mit der ersten Verstärkungseinstellung arbeitet, und dass sie das erste Steuersignal nicht liefert oder ein zweites Steuersignal liefert, um die zweite Verstärkungseinstellung anzuzeigen, solange die integrierte Schaltung mit der zweiten Verstärkungseinstellung arbeitet.

**4.** Integrierte Schaltung nach einem der Ansprüche 1 bis 3, die ferner einen einstellbaren Verstärker (126) aufweist, der so ausgebildet ist, dass er mit einer einer Vielzahl von unterschiedlichen Verstärkungsfaktoreinstellungen in Übereinstimmung mit der Verstärkungseinstellung betrieben werden kann.

**5.** Integrierte Schaltung nach einem der Ansprüche 1 bis 3, die ferner einen Vorspannungsgenerator (228) umfasst, der so ausgebildet ist, dass er mit einer einer Vielzahl von unterschiedlichen Mikrofon-Vorspannungseinstellungen in Übereinstimmung mit der Verstärkungseinstellung betrieben werden kann.

**6.** Integrierte Schaltung nach einem der Ansprüche 1 bis 5, wobei der Signalstärkedetektor (136) so ausgebildet ist, dass er einen Schalldruckpegel des Audiosignals bestimmt.

**7.** Integrierte Schaltung nach einem der Ansprüche 1 bis 6, die einen ersten Eingangsanschluss (122) und einen zweiten Eingangsanschluss (124) aufweist, wobei der erste und der zweite Eingangsanschluss (122, 124) als Eingang für eine Differenzsignalquelle (110) ausgebildet sind.

**8.** Integrierte Schaltung nach einem der Ansprüche 1 bis 7, die einen ersten Ausgangsanschluss (132) und einen zweiten Ausgangsanschluss (134) aufweist, wobei der erste und der zweite Ausgangsanschluss (132, 134) als Signalausgang für eine Differenzsignal-Verarbeitungsvorrichtung (390) ausgebildet sind.

**9.** Schaltungsanordnung (300), die die integrierte Schaltung nach einem der Ansprüche 1 bis 8 aufweist und ferner Folgendes umfasst:

- eine Signalquelle (110), die das Audiosignal liefert;
- eine Signalverarbeitungsvorrichtung (390), die zur Verarbeitung des analogen Ausgangssignals ausgebildet ist; und
- wobei die integrierte Schaltung ferner eine Verstärkerschaltung (320) umfasst, die den Signalstärkedetektor (136) und die Signalisierungsschaltung (372) umfasst, wobei die Verstärkerschaltung (120, 220, 320) in einem Signalpfad zwischen der Signalquelle (110) und der Signalverarbeitungsvorrichtung (190) angeordnet ist;
- wobei die Verstärkerschaltung (120, 220, 320) zur Verstärkung des analogen Eingangssignals ausgebildet ist.

**10.** Schaltungsanordnung (100, 300) nach Anspruch 9, wobei die Signalquelle (110) ein analoges Mikrofon (112) mit hohem Dynamikbereich umfasst.

**11.** Schaltungsanordnung nach einem der Ansprüche 9 oder 10, wobei die Signalverarbeitungsvorrichtung (190, 390) mindestens einen Analog-Digital-Wandler (192), einen analogen Signalprozessor, einen Mikrocontroller, einen digitalen Signalprozessor, einen Audiocodec (194) und einen Leistungsverstärker umfasst.

**12.** Verfahren zum Betreiben einer Schaltungsanordnung (300) nach einem der Ansprüche 9 bis 11, wobei das Verfahren Folgendes umfasst:

- Erkennen einer Signalstärke des analogen Eingangssignals, das von der Signalquelle (110) bereitgestellt wird;
- Auswählen der Verstärkungseinstellung auf der Grundlage der erkannten Signalstärke;
- Verstärken des analogen Eingangssignals basierend auf der Verstärkungseinstellung und Bereitstellen des verstärkten Signals an die Signalverarbeitungsvorrichtung (390); und
- Signalisieren der Verstärkungseinstellung an die Signalverarbeitungsvorrichtung (390) durch Modifizieren des verstärkten Signals, das der Signalverarbeitungsvorrichtung (390) zugeführt wird, durch Erzeugen einer vorbestimmten ersten Offset-Spannung und durch Überlagern einer Gleichtakt-Ausgangsspannung der beiden Ausgangsanschlüsse (132, 134) mit der vorbestimmten ersten Offset-Spannung entsprechend einer DC-Verschiebung, wenn die Verstärkungseinstellung der integrierten Schaltung eine erste Verstärkungseinstellung ist, und durch Nicht-Überlagern der Gleichtakt-Ausgangsspannung der beiden Ausgangsanschlüsse (132, 134) mit der vorbestimmten Offset-Spannung oder durch Überlagern der Gleichtakt-Ausgangsspannung der beiden Ausgangsanschlüsse (132, 134) mit einer vorbestimmten zweiten Offset-Spannung, wenn die Verstärkungseinstellung der integrierten Schaltung eine zweite Verstärkungseinstellung ist.

**Revendications**

**1.** Circuit intégré, comprenant

au moins une borne de tension d'alimentation configurée pour recevoir une tension d'alimentation (Vdd) pour le fonctionnement du circuit intégré ;
au moins une borne d'entrée (122, 124) configurée pour recevoir un signal d'entrée analogique correspondant à un signal audio ;
une sortie de signal différentiel comprenant deux bornes de sortie (132, 134) configurées pour fournir un signal de sortie analogique ; et
un détecteur de force de signal (136) configuré pour détecter une force de signal du signal d'entrée analogique fourni à l'au moins une borne d'entrée (122, 124), le circuit intégré étant configuré pour amplifier le signal audio, un paramètre d'amplification étant sélectionné sur la base de la force de signal détectée et pour délivrer un signal amplifié correspondant correspondant au signal de sortie analogique au niveau de la sortie de signal différentiel ;
le circuit intégré comprenant en outre un circuit de signalement configuré pour indiquer le paramètre d'amplification du circuit intégré au niveau de la sortie de signal différentiel, le circuit de signalement comprenant un décaleur CC (372) et étant connecté aux deux bornes de sortie (132, 134), le circuit de signalement étant configuré pour générer une première tension de décalage prédéterminée et superposer une tension de sortie en mode commun des deux bornes de sortie (132, 134) avec la première tension de décalage prédéterminée correspondant à un décalage CC si le paramètre d'amplification du circuit intégré est un premier paramètre d'amplification, et pour ne pas superposer la tension de sortie en mode commun des deux bornes de

sortie (132, 134) avec la tension de décalage prédéterminée ou pour superposer la tension de sortie en mode commun des deux bornes de sortie (132, 134) avec une deuxième tension de décalage prédéterminée, si le paramètre d'amplification du circuit intégré est un deuxième paramètre d'amplification.

**2.** Circuit intégré selon la revendication 1, le circuit de signalement étant configuré pour fournir un premier signal de commande afin d'indiquer le premier paramètre d'amplification pour une première période de temps prédéterminée lorsque le circuit intégré passe dans un mode de fonctionnement utilisant le premier paramètre d'amplification, et pour fournir un deuxième signal de commande afin d'indiquer le deuxième paramètre d'amplification pour une deuxième période de temps prédéterminée lorsque le circuit intégré passe dans un mode de fonctionnement utilisant le deuxième paramètre d'amplification.

**3.** Circuit intégré selon la revendication 1, le circuit de signalement étant configuré pour fournir un premier signal de commande afin d'indiquer le premier paramètre d'amplification tant que le circuit intégré fonctionne en utilisant le premier paramètre d'amplification, et pour ne pas fournir le premier signal de commande ou pour fournir un deuxième signal de commande afin d'indiquer le deuxième paramètre d'amplification tant que le circuit intégré fonctionne en utilisant le deuxième paramètre d'amplification.

**4.** Circuit intégré selon l'une des revendications 1 à 3, comprenant en outre un amplificateur ajustable (126) configuré pour fonctionner avec un parmi une pluralité de paramètres de gain différents en fonction du paramètre d'amplification.

**5.** Circuit intégré selon l'une des revendications 1 à 3, comprenant en outre un générateur de tension de polarisation (228) configuré pour fonctionner avec un parmi une pluralité de paramètres de tension de polarisation de microphone différents en fonction du paramètre d'amplification.

**6.** Circuit intégré selon l'une des revendications 1 à 5, le détecteur de force de signal (136) étant configuré pour déterminer un niveau de pression acoustique du signal audio.

**7.** Circuit intégré selon l'une des revendications 1 à 6, comprenant une première borne d'entrée (122) et une deuxième borne d'entrée (124), la première et la deuxième borne d'entrée (122, 124) étant configurées comme entrées pour une source de signal différentiel (110) .

**8.** Circuit intégré selon l'une des revendications 1 à 7, comprenant une première borne de sortie (132) et une deuxième borne de sortie (134), la première et la deuxième borne de sortie (132, 134) étant configurées comme bornes de sortie de signal pour un dispositif de traitement de signal différentiel (390).

**9.** Ensemble circuit (300) comprenant le circuit intégré selon l'une des revendications 1 à 8 et comprenant en outre :

une source de signal (110) fournissant le signal audio ; un dispositif de traitement de signal (390) configuré pour traiter le signal de sortie analogique ; et
le circuit intégré comprenant en outre un circuit amplificateur (320) comprenant le détecteur de force de signal (136) et le circuit de signalement (372), le circuit amplificateur (120, 220, 320) étant agencé dans un chemin de signal entre la source de signal (110) et le dispositif de traitement de signal (190) ;
le circuit amplificateur (120, 220, 320) étant configuré pour amplifier le signal d'entrée analogique.

**10.** Ensemble circuit (100, 300) selon la revendication 9, la source de signal (110) comprenant un microphone analogique à plage dynamique élevée (112).

**11.** Ensemble circuit selon l'une quelconque des revendications 9 ou 10, le dispositif de traitement de signal (190, 390) comprenant au moins un parmi un convertisseur analogique numérique (192), un processeur de signal analogique, un microcontrôleur, un processeur de signal numérique, un codec audio (194), et un amplificateur de puissance.

**12.** Procédé de fonctionnement d'un ensemble circuit (300) selon l'une quelconque des revendications 9 à 11, le procédé comprenant :

la détection d'une force de signal du signal d'entrée analogique fourni par la source de signal (110) ;
la sélection du paramètre d'amplification sur la base de la force de signal détectée ;
l'amplification du signal d'entrée analogique sur la base du paramètre d'amplification et la fourniture du signal amplifié au dispositif de traitement de signal (390) ; et
le signalement du paramètre d'amplification au dispositif de traitement de signal (390) en modifiant le signal amplifié fourni au dispositif de traitement de signal (390) en générant une première tension de décalage prédéterminée et en superposant une tension de sortie en mode commun des deux bornes de sortie (132, 134)

avec la première tension de décalage prédéterminée correspondant à un décalage CC si le paramètre d'amplification du circuit intégré est un premier paramètre d'amplification, et en ne superposant pas la tension de sortie en mode commun des deux bornes de sortie (132, 134) avec la tension de décalage prédéterminée ou en superposant la tension de sortie en mode commun des deux bornes de sortie (132, 134) avec une deuxième tension de décalage prédéterminée, si le paramètre d'amplification du circuit intégré est un deuxième paramètre d'amplification.

FIG 1A

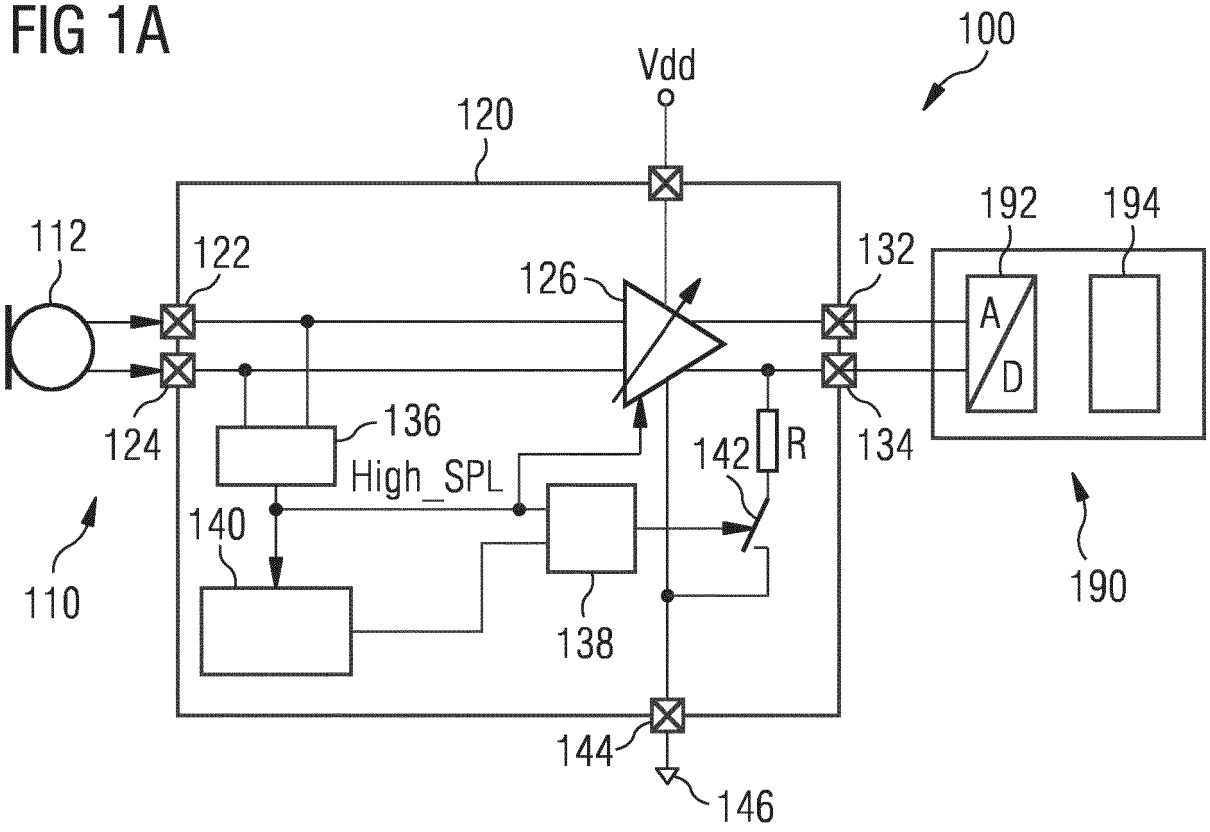

100
Vdd
120
112
122
126
132
192
194
A
D
124
136
High_SPL
142
R
134
140
110
190
138
144
146

FIG 1B

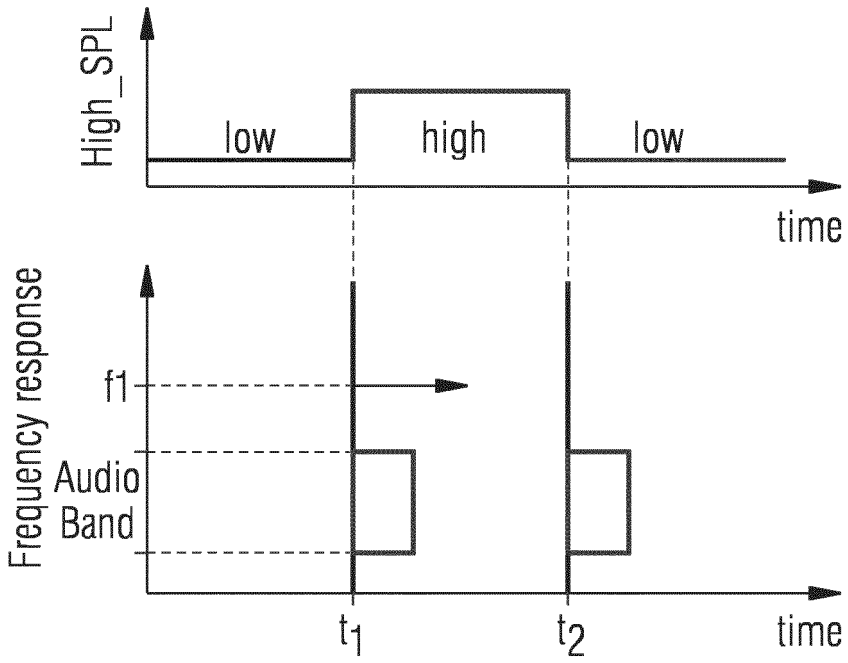

High_SPL
low
high
low
time
Frequency response
f1
Audio
Band
t1
t2
time

FIG 1C

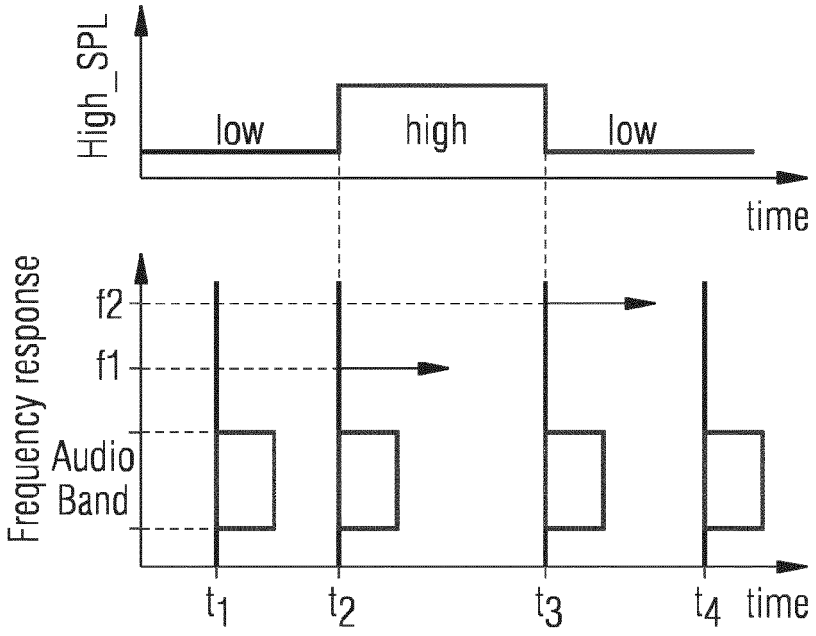

High_SPL
low
high
low
time
Frequency response
f2
f1
Audio
Band
t1
t2
t3
t4
time

FIG 2A

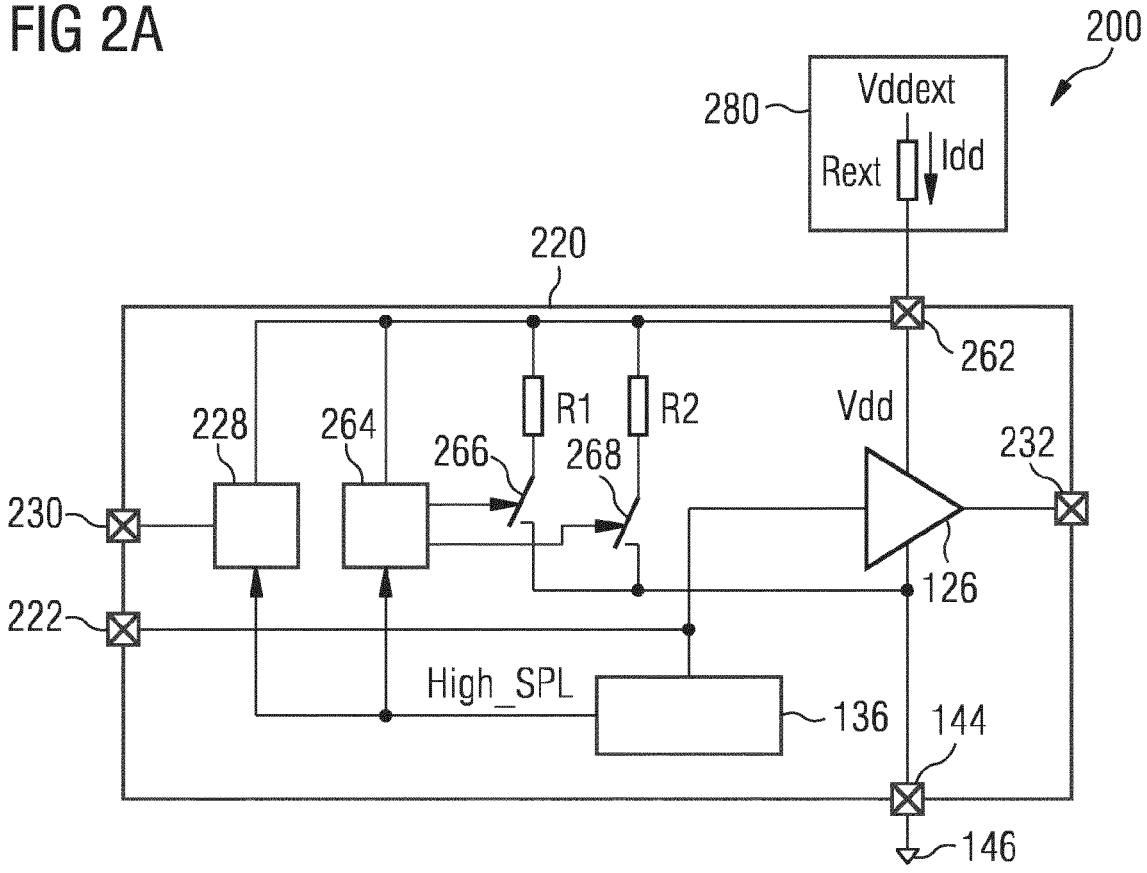

200
280
Vddext
Rext
Idd
220
262
228
264
R1
R2
266
268
Vdd
232
230
126
222
High_SPL
136
144
146

FIG 2B

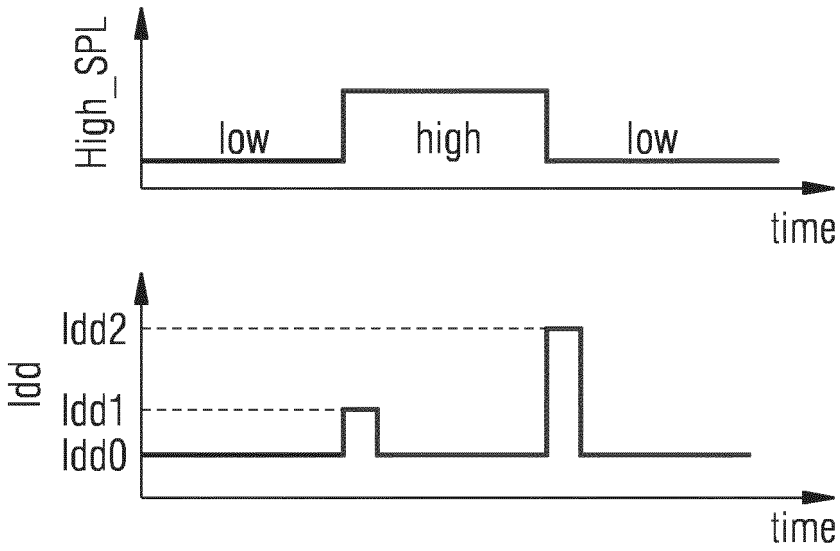

High_SPL
low
high
low
time
Idd
Idd2
Idd1
Idd0
time

FIG 3A

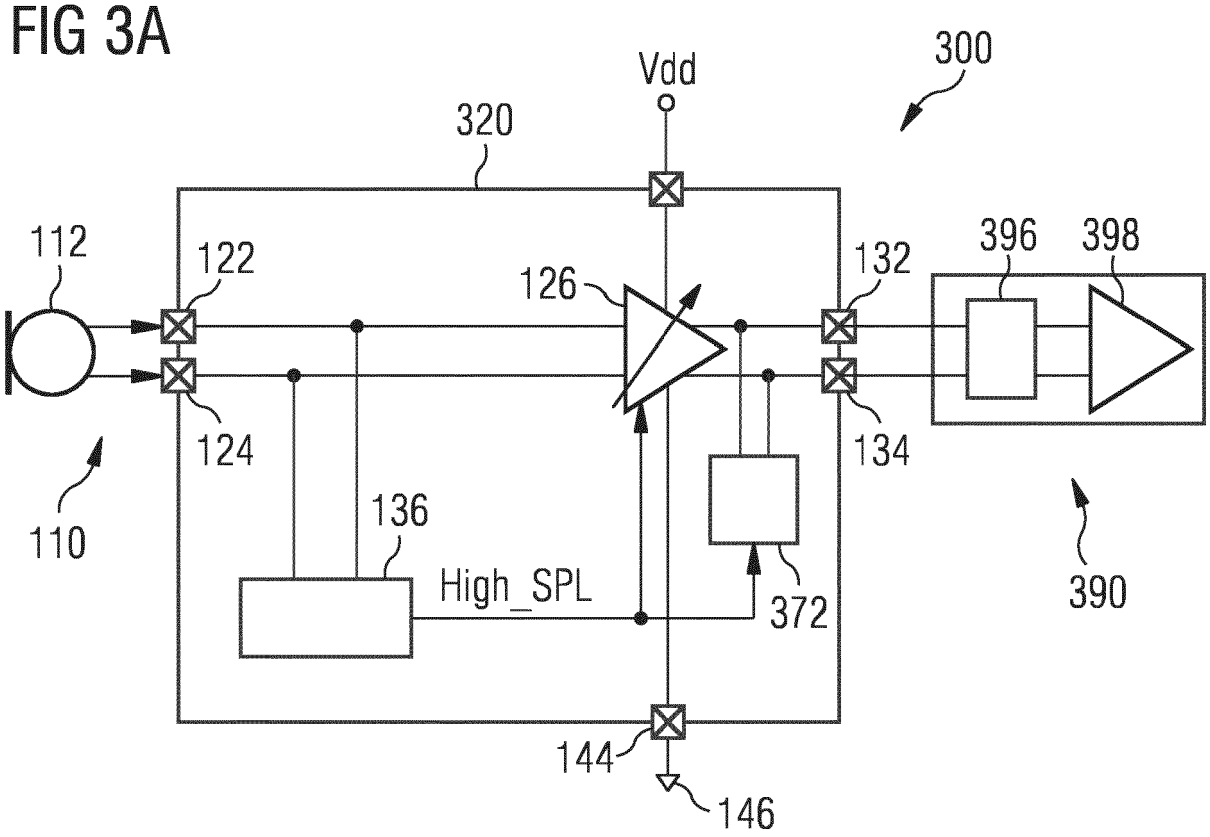

300
Vdd
320
112
122
126
132
396
398
124
134
110
136
High_SPL
372
390
144
146

FIG 3B

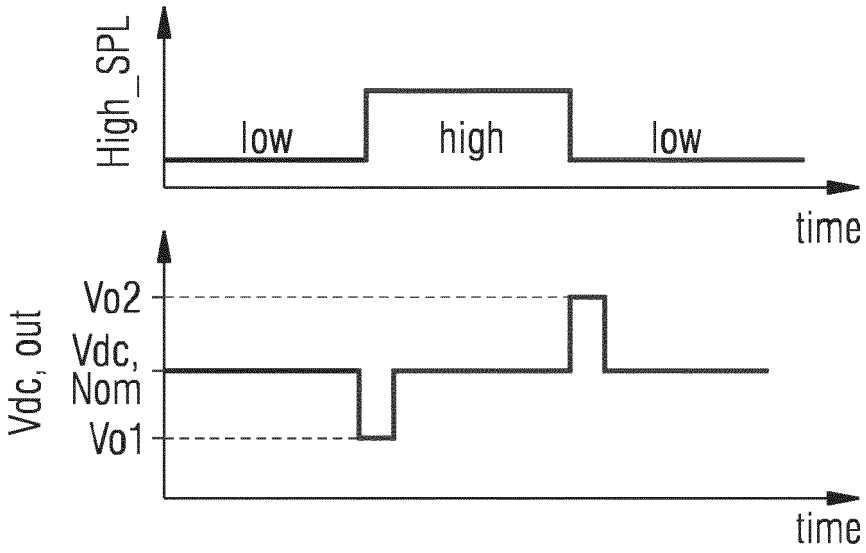
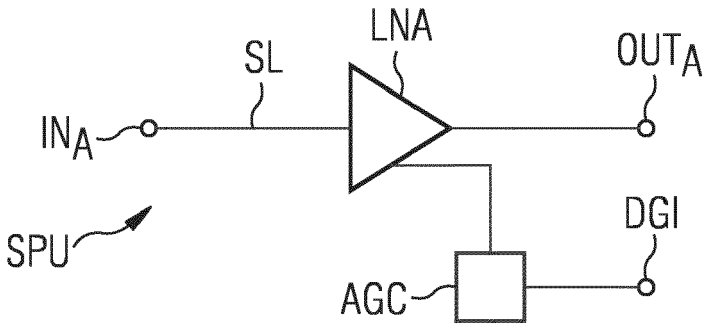



FIG 4 PRIOR ART



## REFERENCES CITED IN THE DESCRIPTION

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