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(54) INTEGRATION OF SILICON PHOTONICS IC FOR HIGH DATA RATE

INTEGRATION VON SILICIUM-PHOTONIK-IC FÜR HOHE DATENRATE

INTÉGRATION DE CIRCUIT INTÉGRÉ PHOTONIQUE EN SILICIUM À HAUT DÉBIT DE DONNÉES

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Description

BACKGROUND

[0001] Signal integrity in high-speed applications is dependent on both the underlying device performance and electronic packaging methods. For high-speed optical transceivers, it is valuable to minimize the radio frequency (RF) loss due to packaging. The maturity of chip-on-board (COB) packaging technology using wire bonding makes it a cost beneficial option for the mass production of high-speed optical transceivers. However, wire bonding introduces parasitic inductance associated with the length of the bond wires that limits the scalability of the system for higher data throughput.

[0002] Document US 2016/0124164 A1 refers to a photonic integrated circuit that may be coupled to an optical fiber and packaged. The optical fiber may be supported by a fiber holder during a solder reflow process performed to mount the packaged photonic integrated circuit to a circuit board or other substrate. The optical fiber may be decoupled from the fiber holder, and the fiber holder removed, after completion of the solder reflow process.

[0003] Document US 2005/0058408 A1 refers to an optoelectronic assembly for an electronic system includes a support electronic chip set configured for at least one of providing multiplexing, demultiplexing, coding, decoding and optoelectronic transducer driving and receive functions.

[0004] Document US 2003/0002770 A1 refers to a package allowing both electrical and optical coupling between one or more integrated circuits and a printed circuit board (PCB) has optical waveguide structures in addition to electrical connections.

[0005] Document US 2005/0135732 A1 refers to an optical interconnect module comprising a silicon carrier; a communication integrated circuit mounted on the silicon carrier and an optical integrated circuit flip chip mounted on the silicon carrier.

[0006] Document US 2002/0196997 A1 refers to a package allowing both electrical and optical coupling between one or more integrated circuits and a printed circuit board (PCB) has optical waveguide structures in addition to electrical connections.

[0007] Document US 8971676 B1 refers to chip package includes an optical integrated circuit (such as a hybrid integrated circuit) and an integrated circuit that are adjacent to each other on the same side of a substrate in the chip package.

[0008] Document US 2003/0141582 A1 refers to a prior art comprising a flip-chip package wherein a lower chip is suspended underneath an upper chip, the lower chip being packaged inside the substrate. Bumps and redistribution lines are also used.

SUMMARY

[0009] The present invention is defined in the independent claims. Preferred embodiments are defined in the dependent claims. According to one aspect, which is outside the scope of the present invention, the subject matter described relates to an integrated component package that includes a printed circuit board (PCB), a photonics integrated circuit (PIC) that is mechanically coupled to the PCB on a first side of the PIC and a driver integrated circuit (driver IC) having a first side. The first side of the driver IC is directly mechanically and electrically coupled to a second side of the PIC via a first set of bump bond connections. The first side of the driver IC is also electrically coupled to the PCB via a second set of bump bond connections.

[0010] The present invention relates to an integrated component package according to claim 1.

[0011] According to another aspect, also outside the scope of the present invention, the subject matter described in this disclosure relates to a method of assembling an integrated component package that includes mechanically coupling a photonics integrated circuit (PIC) to a printed circuit board (PCB) on a first side of the PIC, directly mechanically and electrically coupling a first side of a driver IC to a second side of the PIC via a first set of bump bond connections and electrically coupling the first side of a driver IC to the PCB via a second set of bump bond connections.

[0012] According to the invention this disclosure relates to a method of assembling an integrated component package according to claim 7.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The foregoing will be apparent from the following more particular description of example implementations, as illustrated in the accompanying drawings. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the implementations.

Figure 1A is a diagram of a top down view of a first integrated component package configuration according to an example implementation, not according to the invention.

Figure 1B is a diagram of a side view of the first integrated component package configuration shown in Figure 1A.

Figure 2A is a diagram of a top down view of a second integrated component package configuration according to an example implementation, not according to the invention.

Figure 2B is a diagram of a side view of the second integrated component package configuration shown in Figure 2A.

Figure 3A is a diagram of a side view of a third integrated package configuration according to an example implementation, not according to the invention.

Figure 3B is a diagram of a side view of a fourth integrated component package according to the invention.

Figure 4A is a diagram of a side view of a fifth integrated component package configuration according to an example implementation, not according to the invention.

Figure 4B is a diagram of a side view of a sixth integrated component package configuration according to the invention.

Figure 5 is a flow diagram of a method for assembling the integrated component packages shown in Figures 1A - 2B.

Figure 6 is a flow diagram of a method for assembling the integrated component packages shown in Figures 3A - 4B.

[0014] For purposes of clarity, not every component may be labeled in every figure. The drawings are not intended to be drawn to scale. Like reference numbers and designations in the various figures indicate like elements.

DETAILED DESCRIPTION

[0015] Signal integrity in high-speed applications is dependent on both the underlying device performance and electronic packaging methods. For high-speed optical transceivers, it is valuable to minimize the radio frequency (RF) loss due to packaging. The maturity of chip-on-board (COB) packaging technology using wire bonding makes it a cost beneficial option for the mass production of high-speed optical transceivers. However, wire bonding introduces parasitic inductance associated with the length of the bond wires that limits the scalability of the system for higher data throughput. The electrical issues due to wire bonding become a bottleneck as the on-board data rate of high-speed optical transceivers increases beyond 25 Gbps/channel.

[0016] Integrated component packages according to the present disclosure can be used for the optoelectronic package integration of high-speed optical transceivers. Typically, an integrated component package of a high-speed optical transceiver includes a driver integrated circuit (driver IC) electrically coupled to both a photonics integrated circuit (PIC) and a printed circuit board (PCB). In some conventional package configurations, the driver IC is interconnected to the PIC and the PCB via wire bonding. In other conventional package configurations, the driver IC may be interconnected to the PIC via bump bonding and to the PCB through the PIC via wire bonding. However, both of these configurations are electrically limited by the parasitic inductance associated with the length of the bond wires. Alternatively, the driver IC may be interconnected to the PIC via bump bonding and interconnected to the PCB through the PIC. The interconnection of the driver IC to the PCB through the PIC may use through-silicon vias (TSVs) integrated into the PIC. How-

ever, limitations of this configuration include the complexity of integrating TSVs through the PIC along with the parasitic inductance introduced by the TSV die stacking.

[0017] Certain high-speed optical transceiver packages and package assembly methods of the present disclosure reduce package related parasitic inductance with vertically stacked components and flip-chip bonding. Other high-speed optical transceiver packages and package assembly methods of the present disclosure reduce package related parasitic inductance with a combination of vertically stacked and horizontally tiled components. The integrated component packages disclosed herein include at least an electronic integrated circuit (EIC) such as a driver-chip or driver IC integrated with a photonic integrated circuit (PIC) on a printed circuit board (PCB). The integrated packages also include electrical and physical connections between the various components. The driver IC is electrically connected to both the PIC and the PCB. In some implementations, the PIC may be physically connected to the PCB.

[0018] Figure 1A is a diagram of a top down view of a first integrated component package configuration 100 according to an example implementation. Figure 1B is a diagram of a side view of the first integrated component package configuration 100 shown in Figure 1A. The first integrated component package configuration 100 includes a printed circuit board (PCB) 105, a photonics IC (PIC) 115, an electronic IC (EIC) such as a driver IC 110, and an interposer 130. The PCB 105 has a top side on which the components are located (also referred to as a first side or a component side of the PCB 105). The PCB 105 also has a bottom side or a second side. The PIC 115, driver IC 110, and interposer 130 each also have a first side and a second side. The driver IC 110 is directly electrically connected to both the PIC 115 and indirectly electrically connected to the PCB 105 via the interposer 130.

[0019] The PIC 115 is located on a top side or component side of the PCB 105. The first side of the PIC 115 is physically connected to the surface of the top side of the PCB 105. In some implementations, the first side of the PIC 115 is surface mounted onto the top side of the PCB 105. In some implementations, the PIC 115 may be an externally modulated laser (EML), a monolithic tunable laser, a widely tunable laser or other optical transmitter incorporating multiple photonic functions into a single device.

[0020] The driver IC 110 is vertically stacked on the second side of the PIC 115 such that a portion of the driver IC 110 overlaps the second side of the PIC 115 while a portion of the driver IC 110 overlaps the interposer 130.

[0021] As mentioned above, the driver IC 110 is electrically connected to both the PIC 115 and the PCB 105. The portion of the driver IC 110 that overlaps the second side of the PIC 115 is directly flip-chip connected to the second side of the PIC 115 with one or more bump bonds (BBs) 150. The BBs 150 provide an electrical interface

between the driver IC 110 and the PIC 115. The BBs 150 also provide a physical or mechanical interface between the driver IC 110 and the second side of the PIC 115. In addition to being electrically connected to the PIC 115, the driver IC 110 is also electrically connected to the PCB 105. The driver IC 110 is physically connected to the PCB 105 via the interposer 130. The portion of the driver IC 110 overlaps the interposer 130 is directly flip-chip connected to a first side of the interposer 130 with one or more bump bonds (BBs) 140. The second side of the interposer 130 is physically and electrically connected to the surface of the top side of the PCB 105 via one or more other bump bonds (BBs) 145. The interposer 130 along with the BBs 140 and BBs 145 provides an electrical and mechanical interface between the driver IC 110 and the PCB 105.

[0022] In some implementations, the interposer 130 may include a multi-layer substrate that further includes alternating layers of conductors and dielectrics. In some implementations, the interposer 130 may include glass. In some implementations, the interposer 130 may further include one or more plated thru-holes (PTHs) 160 and an electrical connection between the driver IC 110 and the PCB 105 via the interposer 130 may include the one or more of the PTHs 160. In some implementations, the interposer 130 may include silicon and the one or more PTHs 160 may be through-silicon vias (TSVs). The flip-chip vertical integration of the driver IC 110 with the PIC 115 and PCB 105, as shown in Figures 1A and 1B, reduces the length of the interconnections between the components and thereby reduces the packaging related parasitic inductance.

[0023] Figure 2A is a diagram of a top down view of a second integrated component package configuration 200 according to an example implementation. Figure 2B is a diagram of a side view of the second integrated component package configuration 200 shown in Figure 2A. The second integrated component package configuration 200 includes a printed circuit board (PCB) 205, a photonics IC (PIC) 215 and an electronic IC (EIC) such as a driver IC 210. The PCB 205 has a top side on which the components are located (also referred to as a first side or a component side of the PCB 205). The PCB 205 also has a bottom side or a second side. The PIC 215 has a first side and a second side. The driver IC 210 also has a first side and a second side. The driver IC 210 is electrically connected to both the PIC 215 and the PCB 205.

[0024] The top side of the PCB 205 includes a recess or cavity such as the cavity 125. The PIC 215 is located within the cavity 225. The first side of the PIC 215 is physically connected to the PCB 205 within the cavity 225. In some implementations, the first side of the PIC 215 may be surface mounted onto the floor of the cavity 225. As shown in Figure 2B, when the PIC 215 is located within the cavity 225 and the first side of the PIC 215 is physically connected to the floor of the cavity 225, the second side of the PIC 215 is aligned with the top side

of the PCB 205. The alignment is achieved either by varying the depth of the cavity or the height of the underfill used in surface mounting the PIC 215 to the floor of the cavity 225. As in Figures 1A and 1B, in some implementations, the PIC 215 may be an externally modulated laser (EML), a monolithic tunable laser, a widely tunable laser or other optical transmitter incorporating multiple photonic functions into a single device.

[0025] The driver IC 210 is vertically stacked on a second side of the PIC 215 such that a portion of the driver IC 210 overlaps the second side of the PIC 215 while a portion of the driver IC 210 overlaps the top side of the PCB 205.

[0026] As mentioned above, the driver IC 210 is electrically connected to both the PIC 215 and the PCB 205. The portion of the driver IC 210 that overlaps the second side of the PIC 215 is directly flip-chip connected to the second side of the PIC 215 with one or more bump bonds (BBs) 250. The BBs 250 provides an electrical interface between the driver IC 210 and the PIC 215. The BB 250 also provides a physical or mechanical interface between the driver IC 210 and the second side of the PIC 215.

[0027] As mentioned above, in addition to being electrically connected to the PIC 215, the driver IC 210 is also electrically connected to the PCB 205. The portion of the driver IC 210 that overlaps the PCB 205 is directly flip-chip connected to the surface of the component side of the PCB 205 with one or more bump bonds (BBs) 240. The BBs 240 provide an electrical interface between the driver IC 210 and the PCB 205. The BBs 240 also provide a physical or mechanical interface between the driver IC 210 and the component side of the PCB 205.

[0028] By directly flip-chip connecting the driver IC 210 to both the PCB 205 and the PIC 215, i.e., without using an interposer between the Driver IC 210 and the PCB 205, the second integrated component package 200 shown in Figures 2A and 2B may further reduce the packaging related parasitic inductance.

[0029] Figure 3A is a diagram of a side view of a third integrated component package configuration 300a according to an example implementation. The integrated component package configuration 300a includes a PCB 305a, an electronic IC (EIC) such as a driver IC 310, a photonic IC (PIC) 315 and a chip carrier such as the carrier 365. The PCB 305a has a top side on which the components are located (also referred to as a first side or a component side of the PCB 305). The PCB 305a also has a bottom side or a second side. The PIC 315 has a first side and a second side. The driver IC 310 also has a first side and a second side. The driver IC 310 is electrically connected to both the PIC 315 and the PCB 305a. The package configuration 300 also includes a plurality of ball grid array (BGA) connections such as the BGA connection 335. The BGA connection 335 is physically connected to the top side of the PCB 305a. The carrier 365 has a first side and a second side. The carrier 365 includes a redistribution layer (RDL) 380 disposed on a portion of the first side of the carrier 365.

[0030] As shown in Figure 3A, the package configuration 300a includes a combination of vertically stacked and horizontally tiled components. The carrier 365 is connected to the PCB 305a such that the first side of the carrier 365 is opposite the top side of the PCB 305a. The carrier 365 is physically and electrically connected to the PCB 305a via one or more of the BGA connections 335.

[0031] The driver IC 310 and the PIC 315 are horizontally tiled with respect to each other and physically connected to the first side of the carrier 365. Therefore, the driver IC 310 and the PIC 315 are located between the first side of the carrier 365 and the top side of the PCB 305a. The driver 310 and the PIC 315 are physically connected adjacent to one another on different portions of the first side of the carrier 365. In some implementations, the driver IC 310 and the PIC 315 are horizontally spaced on the carrier 365 according to the die spacing requirements of the driver IC 310 and PIC 315. A first side of the carrier 365 that includes the RDL 380. The first side of the driver IC 110 is directly flip-chip connected to the RDL 380 with one or more bump bonds (BBs) 340. The BBs 340 provide a mechanical interface between the driver IC 310 and the carrier 365. The first side of the PIC 315 is also directly flip-chip connected to the RDL 380 with one or more bump bonds (BBs) 350. The BBs 150 provide a mechanical interface between the first side of the PIC 315 and the first side of the carrier 365.

[0032] The driver IC 310 is electrically connected to both the PIC 315 and the PCB 305a. The driver IC 310 is electrically connected to the PIC 315 via the BBs 340, one or more RDL interconnections 360 and the BBs 350. The driver IC 310 is electrically connected to the PCB 305 via one or more RDL interconnections 360 and one or more of the BGA connections 335.

[0033] As shown in Figure 3A, a space 327 located adjacent to the PIC 315 and defined by the first side of the carrier 365 and the top side of the PCB 305a may not be sized to accept the optical fiber 320 thus preventing a direct optical coupling between the optical fiber 320 and the PIC 315 within the space 327. Accordingly, in Figure 3A, the optical fiber 320 is located above the second side of the carrier 365 and optically couples with the PIC 315 through the carrier 365. In some implementations, the carrier 365 may be comprised of a transparent material, such as glass, thereby enabling an optical coupling between the optical fiber 320 and the PIC 315 via the carrier 365.

[0034] Figure 3B is a diagram of a side view of a fourth integrated component package configuration 300b according to the invention. The fourth integrated package configuration 300b is similar to the third integrated component package configuration 300a. The integrated component package configuration 300b includes a PCB 305b, an electronic IC (EIC) such as a driver IC 310, a photonic IC (PIC) 315 and a chip carrier such as the carrier 365. The PCB 305b has a top side on which the components are located (also referred to as a first side or a

component side of the PCB 305). The PCB 305b also has a bottom side or a second side. The PIC 315 has a first side and a second side. The driver IC 310 also has a first side and a second side. The driver IC 310 is electrically connected to both the PIC 315 and the PCB 305b. The package configuration 300 also includes a plurality of ball grid array (BGA) connections such as the BGA connection 335. The BGA connection 335 is physically connected to the top side of the PCB 305a. The carrier 365 has a first side and a second side. The carrier 365 includes a redistribution layer (RDL) 380 disposed on a portion of the first side of the carrier 365.

[0035] As shown in Figure 3B, the package configuration 300b includes a combination of vertically stacked and horizontally tiled components. The carrier 365 is connected to the PCB 305b such that the first side of the carrier 365 is opposite the top side of the PCB 305b. The carrier 365 is physically and electrically connected to the PCB 305b via one or more of the BGA connections 335.

[0036] The driver IC 310 and the PIC 315 are horizontally tiled with respect to each other and physically connected to the first side of the carrier 365. Therefore, the driver IC 310 and the PIC 315 are located between the first side of the carrier 365 and the top side of the PCB 305b. The driver 310 and the PIC 315 are physically connected adjacent to one another on different portions of the first side of the carrier 365. In some implementations, the driver IC 310 and the PIC 315 are horizontally spaced on the carrier 365 according to the die spacing requirements of the driver IC 310 and PIC 315. A first side of the driver IC 310 is physically connected to a portion of the carrier 365 that includes the RDL 380. The first side of the driver IC 110 is directly flip-chip connected to the RDL 380 with one or more bump bonds (BBs) 340. The BBs 340 provide a mechanical interface between the driver IC 310 and the carrier 365. The first side of the PIC 315 is also directly flip-chip connected to the RDL 380 with one or more bump bonds (BBs) 350. The BBs 150 provide a mechanical interface between the first side of the PIC 315 and the first side of the carrier 365.

[0037] The driver IC 310 is electrically connected to both the PIC 315 and the PCB 305a. The driver IC 310 is electrically connected to the PIC 315 via the BBs 340, one or more RDL interconnections 360 and the BBs 350. The driver IC 310 is electrically connected to the PCB 305 via one or more RDL interconnections 360 and one or more of the BGA connections 335.

[0038] In some implementations, an optical fiber 320 is directly optically coupled with the PIC 315. In some implementations, the top side of the PCB 305a may further include a PCB cavity 325 located adjacent to the PIC 315 and opposite the first side of the carrier 365. In some implementations, the PCB cavity 325 may define a fiber cavity 326 adjacent to the PIC 315 between the first side of the carrier 365 and the PCB cavity 325. In some implementations, the fiber cavity 326 is sized to accept the optical fiber 320. The fiber cavity enables a direct optical coupling between the optical fiber 320 and the PIC 315

within the fiber cavity thereby reducing the overall height or form factor of the integrated component package configuration 300b.

[0039] The integrated component package configurations 300a and 300b provide straightforward electrical connections between the PIC 315 and driver IC 310, without the need for achieving vertical alignment between the components or portions of the PCB, thereby facilitating manufacturing of the package, while still avoiding wire bonds between the components, thereby reducing the inductive load of the package relative to traditional packages.

[0040] Figure 4A is a diagram of a side view of a fifth integrated component package configuration 400a according to an example implementation. The integrated component package configuration 400 includes a PCB 405a, an electronic IC (EIC) such as a driver IC 410, a photonic IC (PIC) 415 and a chip carrier such as the carrier 465. The PCB 405a has a top side on which the components are located (also referred to as a first side or a component side of the PCB 405). The PCB 405a also has a bottom side or a second side. The PIC 415 has a first side and a second side. The driver IC 410 also has a first side and a second side. The driver IC 410 is electrically connected to both the PIC 415 and the PCB 405. The package configuration 400 also includes a plurality of ball grid array (BGA) connections such as the BGA connection 435. The BGA connection 435 is physically and electrically connected to the top side of the PCB 405. The carrier 465 has a first side and a second side. The carrier 465 includes a redistribution layer (RDL) 480 disposed on a portion of the first side of the carrier 465. In some implementations, the carrier 465, driver IC 410 and PIC 415 may be integrated using package on package (PoP) technology and packaging formats such as fan-out wafer level packaging (FO-WLP), embedded die in laminate or modular embedded die. In some implementations, the carrier 465 can be formed from a mold compound, encasing the driver IC 410 die and the PIC 415 die.

[0041] The driver IC 410 and the PIC 415 are horizontally tiled with respect to each other and embedded within the carrier 465. A first side of the driver IC 410 is physically connected to a portion of the first side of the carrier 465 that is disposed with the RDL 480. The first side of the driver IC 410 is directly connected to the RDL 480. The first side of the PIC 415 is also directly connected to the RDL 380.

[0042] The driver IC 410 is electrically connected to the PIC 415 and the PCB 405. The driver 410 is electrically connected to the PIC 415 via one or more of the RDL interconnections 460. The driver IC 410 is electrically connected to the PCB 405 via one or more of the RDL interconnections 460, one or more through-mold vias (TMV) 470 and the BGA connection 435. The optical fiber 420 located above the second side of the carrier 465 may directly optically couple with the PIC 415.

[0043] Figure 4B is a diagram of a sixth integrated com-

ponent package configuration 400b, according to the invention. The sixth integrated package configuration 400b is similar to the fifth integrated component package configuration 400a. In contrast to the fifth integrated package configuration 400a, the sixth integrated package configuration 400b includes a PCB 405b that includes a PCB cavity 425. The PCB cavity 425 defines a fiber cavity 427 between the first side of the carrier 465 and PCB cavity 425. The fiber cavity 427 is sized to accept an optical fiber 420. In some implementations, when the carrier 465 is vertically stacked onto the PCB 405b, the fiber cavity 427 may be located adjacent to the PIC 415. In some implementations, a first portion of the first side of the PIC 415 may overlap the PCB cavity 425 and a second portion of the first side of the PIC 415 may overlap the top surface of the PCB 405b. In some implementations, the RDL 480 may be disposed across the second portion of the first side of the PIC 415 that overlaps the top portion of the PCB 405b. As shown in Figure 4B, the fiber cavity 427 enables a direct optical coupling between the optical fiber 420 and the PIC 415 within the fiber cavity 427, thereby reducing the overall height and form factor of the integrated component package configuration 400b.

[0044] As mentioned above, the integrated package configurations 100, 200, 300a and 300b shown in Figures 1A-3B may include flip-chip connections between the components using one or more bump bonds, such as the bump bonds (BBs) 140, 145, 150, 240, 250, 340 and 350. In some implementations, the bump bonds may be formed using solder. In some implementations, the bump bonds can be formed using materials other than solder, such as, without limitation copper, tin, or gold, alloys thereof, or other conductive materials or composites known by those of ordinary skill in the art to be useful in forming bump bonds.

[0045] Figure 5 is a flow diagram of a method 500 that when executed can result in the packages shown in Figures 1A - 2B. The method 500 includes vertically integrating a PCB, a PIC and a driver IC. The method 500 includes mechanically coupling a photonics integrated circuit (PIC) to a printed circuit board (PCB) on a first side of the PIC (stage 505), directly mechanically and electrically coupling a first side of a driver IC to a second side of the PIC via a first set of bump bond connections (stage 510) and electrically coupling a first side of a driver IC to the PCB via a second set of bump bond connections (stage 515).

[0046] An example implementation of the method 500 when executed results in a package having the first package configuration 100 shown in Figures 1A and 1B. As mentioned above, the method 500 includes mechanically coupling a photonics integrated circuit (PIC) 115 to a printed circuit board (PCB) 105 on a first side of the PIC 115 (stage 505). The method 500 further includes directly mechanically and electrically coupling a first side of a driver IC 110 to a second side of the PIC 115 via a first set of bump bond connections such as the BBs 150 (stage 510). The method 500 further includes electrically

coupling the first side of the driver IC 110 to the PCB 105 via a second set of bump bond connections such as the BBs 140 (stage 515). In some implementations, stage 515 of the method 500 may further include mechanically coupling a first side of an interposer 130 to the PCB 105 via a third set of bump bond connections such as the BBs 145. In some implementations, stage 515 of the method 500 may also include mechanically coupling a second side of the interposer 130 to the first side of the driver IC 110 via the second set of bump bond connections BBs 140. In some implementations, stage 515 of the method 500 may include electrically coupling the first side of the driver IC 110 to the PCB 105 via the second set of bump bond connections BBs 140, the interposer 130 and the third set of bump bond connections BBs 145.

[0047] An example implementation of the method 500 when executed results in a package having the second package configuration 200 shown in Figures 2A and 2B. The method 500 includes mechanically coupling a photonics integrated circuit (PIC) 215 to a printed circuit board (PCB) 205 on a first side of the PIC 215 (stage 505). In some implementations, stage 505 of the method 500 may include placing the PIC 215 within a PCB cavity 225 in a first side of the PCB 205 and surface bonding the PIC 215 to the floor of the PCB cavity 225 such that the first side of the PIC 215 faces a floor of the PCB cavity 225. The method 500 further includes directly mechanically and electrically coupling a first side of a driver IC 210 to a second side of the PIC 215 via a first set of bump bond connections such as the BBs 250 (stage 510). The method 500 further includes electrically coupling the first side of the driver IC 210 to the PCB 205 via a second set of bump bond connections such as the BBs 240 (stage 515). In some implementations, stage 515 of the method 500 may further include electrically coupling the first side of the driver IC 215 to the PCB 205 via the second set of bump bond connections such as the BBs 240, the interposer 230 and a third set of bump bond connections such as the BBs 245.

[0048] Figure 6 is a flow diagram of a method 600 that when executed can result in the fourth and sixth package configurations 300b and 400b according to the invention, as shown in Figures 3B and 4B. The method 600 includes horizontally tiling a PIC and a driver IC, relative to each other and vertically integrating the PIC and the driver IC with a PCB. The method 600 includes mechanically and electrically coupling a plurality of BGA connections to a printed circuit board (PCB) on the first side of the PCB (stage 605). The PCB has a PCB cavity sized to accept an optical fiber. The method 600 further includes mechanically coupling a carrier to the PCB on a first side of the carrier via at least one of the BGA connections, the carrier including a redistribution layer (RDL) disposed on the first side of the carrier and including a plurality of RDL interconnections (stage 610). The method 600 further includes mechanically coupling a photonics integrated circuit (PIC) to the carrier (stage 615) and mechanically coupling a driver IC to the carrier (stage 620). The method

600 further includes electrically coupling a first side of the driver IC to a first side of the PCB via at least one of the RDL connections and at least one of the BGA connections (stage 625). The method 600 includes electrically coupling the first side of the driver IC to the first side of the PIC via at least one of the RDL interconnections (stage 630).

[0049] An example implementation of the method 600 when executed results in a package having the fourth package configuration 300b shown in Figure 3B. The method 600 includes mechanically and electrically coupling a plurality of BGA connections such as the BGA connection 335 to a printed circuit board (PCB) 305b on the first side of the PCB 305b. The PCB 305b having a PCB cavity 325 sized to accept an optical fiber 320 (stage 605). The method 600 includes mechanically coupling a carrier 365 to the PCB 305b on a first side of the carrier 365 via at least one of the BGA 335, the carrier 365 including a redistribution layer (RDL) 380 disposed on the first side of the carrier 365 and including a plurality of RDL interconnections 360 (stage 610). The method 600 further includes mechanically coupling a photonics integrated circuit (PIC) 315 to the carrier 365 (stage 615) and mechanically coupling a driver IC 310 to the carrier 365 (stage 620). In some implementations, stage 620 of the method 600 may also include locating the photonics integrated circuit (PIC) 315 between a second side of the RDL 380 and the first side of the PCB 305b and mechanically coupling a first side of the PIC 315 to the second side of the RDL 380 via at least one first bump bond connection such as the BBs 350. The method includes electrically coupling a first side of the driver IC 310 to a first side of the PCB 305b via at least one of the RDL interconnections 360 and at least one of the BGA 335 (stage 625). In some implementations, stage 625 of the method 600 may include locating the driver IC 310 between a second side of the RDL 380 and the first side of the PCB 305b. The method 600 further includes electrically coupling the first side of the driver IC 310 to the first side of the PIC 315 via at least one of the RDL interconnections 360 (stage 630). In some implementations, stage 630 of the method 600 may also include mechanically and electrically coupling the first side of the driver IC 365 to the second side of the RDL 380 via a plurality of second bump bond connections such as the BBs 340. In some implementations, stage 630 of the method 600 may include electrically coupling the first side of the driver IC 310 to the first side of the PIC 315 via at least one of the first bump bond connections such as the BBs 340, at least one of the RDL interconnections 360 and at least one of the second bump bond connections such as the BBs 350.

[0050] In some implementations, the method 600 when executed results in the package having the sixth package configuration shown in Figure 4B. The method 600 includes mechanically and electrically coupling a plurality of BGA connections such as the BGA connection 435 to a printed circuit board (PCB) 405b on the first side

of the PCB 405b, the PCB 405b having a PCB cavity 425 sized to accept an optical fiber 420 (stage 605). The method 600 includes mechanically coupling a carrier 465 to the PCB 405b on a first side of the carrier 465 via at least one BGA connection 435, the carrier 465 including a redistribution layer (RDL) 480 disposed on the first side of the carrier 465 and including a plurality of RDL interconnections 460 (stage 610). The method 600 further includes mechanically coupling a photonics integrated circuit (PIC) 415 to the carrier 465 (stage 615) and mechanically coupling a driver IC 410 to the carrier 465 (stage 620). In some implementations, stage 620 of the method 600 may further include locating the photonics integrated circuit (PIC) 415 within the carrier 465 and locating the driver IC 410 within the carrier 465. In some implementations, stage 620 of the method 600 may further include locating the PIC 415 in the PCB cavity 425 in the first side of the PCB 415 such that a first portion of the first side of the PIC 415 overlaps the PCB cavity 425 and a second portion of the first side of the PIC 415 overlaps the first side of the PCB 405b. The RDL 480 is disposed across the first side of the PIC 415 and the first side of driver IC 410. The method includes electrically coupling a first side of the driver IC 410 to a first side of the PCB 405b via at least one of the RDL interconnections 460 and at least one BGA connection 435 (stage 625). The method 600 further includes electrically coupling the first side of the driver IC 410 to the first side of the PIC 415 via at least one of the RDL interconnections 460 (stage 630). In some implementations, the RDL 480 may be disposed across the second portion of the first side of the PIC 415 that overlaps the PCB 405b.

[0051] As mentioned above, the methods 500 and 600 may include establishing electrical and/or mechanical connections between components by flip-chip connecting the components with one or more bump bonds. In some implementations, the bump bonds may be formed using solder. In some implementations, the bump bonds can be formed using materials other than solder, such as, without limitation copper, tin, or gold, alloys thereof, or other conductive materials or composites known by those of ordinary skill in the art to be useful in forming bump bonds.

[0052] While this specification contains many specific implementation details, these should not be construed as limitations on the scope of the invention, whose scope of protection is defined by the claims. Certain features that are described in this specification in the context of separate implementations can also be implemented in combination in a single implementation.

[0053] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the imple-

mentations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

[0054] References to "or" may be construed as inclusive so that any terms described using "or" may indicate any of a single, more than one, and all of the described terms. The labels "first," "second," "third," and so forth are not necessarily meant to indicate an ordering and are generally used merely to distinguish between like or similar items or elements.

[0055] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the scope of the claims. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with their wording.

[0056] Signal integrity in high-speed applications is dependent on both the underlying device performance and electronic packaging methods. The maturity of chip-on-board (COB) packaging technology using wire bonding makes it a cost beneficial option for the mass production of high-speed optical transceivers. However, wire bonding introduces parasitic inductance associated with the length of the bond wires that limits the scalability of the system for higher data throughput. A high-speed optical transceiver package according to a first proposed configuration minimizes packaging related parasitic inductance by vertically integrating components using flip-chip bonding. A high-speed optical transceiver package according to a second proposed configuration and the invention, minimizes packaging related parasitic inductance with horizontal tiling of components using a chip carrier and flip-chip bonding.

Claims

1. An integrated component package (300b) comprising:

a printed circuit board, PCB, (305b) having a PCB cavity (325) in a first side of the PCB sized to accept an optical fiber (320);

a plurality of ball grid array, (335) connections mechanically and electrically coupled to the PCB on the first side of the PCB;

a carrier (365) directly mechanically coupled to the first side of the PCB on a first side of the carrier via at least one of the ball grid array (335) connections, wherein the first side of the carrier and the first side of the PCB face each other, the carrier including a redistribution layer, (380) disposed on the first side of the carrier and in-

cluding a plurality of redistribution layer (380) interconnections;
 a photonics integrated circuit, (315) mechanically coupled to the carrier; and
 a driver IC (310) mechanically coupled to the carrier and having a first side that is

- (i) electrically coupled to the first side of the PCB via at least one of the redistribution layer (380) connections and at least one of the ball grid array (335) connections, and
- (ii) electrically coupled to a first side of the photonics integrated circuit (315) via at least one of the redistribution layer (380) interconnections.

2. The package (300b) of claim 1 wherein:

the photonics integrated circuit, (315) is located between a second side of the redistribution layer (380) and the first side of the PCB and a first side of the photonics integrated circuit (315) is mechanically coupled to the second side of the redistribution layer (380) via at least one first bump bond connection;
 the driver IC is located between a second side of the redistribution layer (380) and the first side of the PCB and the first side of the driver IC is

- (i) mechanically and electrically coupled to the second side of the redistribution layer (380) via a plurality of second bump bond connections; and
- (ii) electrically coupled to the first side of the photonics integrated circuit (315) via at least one of the first bump bond connections, at least one of the redistribution layer (380) interconnections and at least one of the second bump bond connections.

3. The package (300b) of claim 1 or claim 2 wherein the PCB cavity is located adjacent to the photonics integrated circuit (315)

4. The package (300b) of any one of claims 1 to 3 wherein:

the photonics integrated circuit, (315) is located within the carrier;
 the driver IC is located within the carrier; and
 the redistribution layer (380) is further disposed across the first side of the photonics integrated circuit (315) and the first side of driver IC (310).

5. The package (300b) of claim 4 wherein the PCB cavity is located on the first side of the PCB such that a first portion of the first side of the photonics integrated circuit (315) overlaps the cavity and a second portion

of the first side of the photonics integrated circuit (315) overlaps the first side of the PCB.

6. The package (300b) of claim 5 wherein the redistribution layer (380) is disposed across the second portion of the first side of the photonics integrated circuit (315) that overlaps the PCB.

7. A method (600) of assembling an integrated component package (300b), the method comprising:

mechanically and electrically coupling (605) a plurality of ball grid array, (335) connections to a printed circuit board, PCB, (305b) on a first side of the PCB, the PCB having a PCB cavity (325) in the first side of the PCB sized to accept an optical fiber (320);
 mechanically coupling (610) a carrier to the first side of the PCB on a first side of the carrier via at least one of the ball grid array (335) connections, wherein the first side of the carrier and the first side of the PCB face each other, the carrier including a redistribution layer, (380) disposed on the first side of the carrier and including a plurality of redistribution layer (380) interconnections;
 mechanically coupling (615) a photonics integrated circuit, (315) to the carrier; and
 mechanically coupling (620) a driver IC (310) to the carrier;
 electrically coupling (625) a first side of the driver IC to the first side of the PCB via at least one of the redistribution layer (380) connections and at least one of the ball grid array (335) connections; and
 electrically coupling (630) the first side of the driver IC to the first side of the photonics integrated circuit (315) via at least one of the redistribution layer (380) interconnections.

8. The method (600) of claim 7 further comprising:

locating the photonics integrated circuit, (315) between a second side of the redistribution layer (380) and the first side of the PCB and mechanically coupling a first side of the photonics integrated circuit (315) to the second side of the redistribution layer (380) via at least one first bump bond connection;
 locating the driver IC between a second side of the redistribution layer (380) and the first side of the PCB;
 mechanically and electrically coupling the first side of the driver IC to the second side of the redistribution layer (380) via a plurality of second bump bond connections; and
 electrically coupling the first side of the driver IC to the first side of the photonics integrated circuit

(315) via at least one of the first bump bond connections, at least one of the redistribution layer (380) interconnections and at least one of the second bump bond connections.

9. The method (600) of claim 7 or claim 8 wherein the PCB cavity is located adjacent to the photonics integrated circuit (315) 5
10. The method (600) of any one of claims 7 to 9 further comprising: 10
- locating the photonics integrated circuit, (315) within the carrier; and
- locating the driver IC within the carrier, wherein the redistribution layer (380) is further disposed across the first side of the photonics integrated circuit (315) and the first side of driver IC (310). 15
11. The method (600) of claim 10 further comprising locating the photonics integrated circuit (315) in the PCB cavity in the first side of the PCB such that a first portion of the first side of the PIC overlaps the cavity and a second portion of the first side of the photonics integrated circuit (315) overlaps the first side of the PCB. 20 25
12. The method (600) of claim 11 further comprising disposing the redistribution layer (380) across the second portion of the first side of the photonics integrated circuit (315) that overlaps the PCB. 30

Patentansprüche

1. Gehäuse für integrierte Komponenten (300b), das umfasst: 35
- eine Leiterplatte, PCB, (305b) mit einem PCB-Hohlraum (325) in einer ersten Seite der PCB, der dimensioniert ist, eine optische Faser (320) aufzunehmen; 40
- mehrere Kugelgitteranordnungsverbindungen (335), die mechanisch und elektrisch an die PCB auf der ersten Seite der PCB gekoppelt sind; 45
- einen Träger (365), der an die erste Seite der PCB auf einer ersten Seite des Trägers über mindestens eine der Kugelgitteranordnungsverbindungen (335) unmittelbar mechanisch gekoppelt ist, wobei die erste Seite des Trägers und die erste Seite der PCB einander zugewandt sind, wobei der Träger eine Umverteilungsschicht (380) enthält, die auf der ersten Seite des Trägers angeordnet ist und mehrere Umverteilungsschichtverbindungen (380) enthält; 50
- eine integrierte Photonik-Schaltung (315), die an den Träger mechanisch gekoppelt ist; und 55

eine Ansteuerungs-IC (310), die an den Träger mechanisch gekoppelt ist und eine erste Seite besitzt, die

- (i) an die erste Seite der PCB über mindestens eine der Umverteilungsschichtverbindungen (380) und mindestens eine der Kugelgitteranordnungsverbindungen (335) elektrisch gekoppelt ist und
- (ii) an eine erste Seite der integrierten Photonik-Schaltung (315) über mindestens eine der Umverteilungsschichtverbindungen (380) elektrisch gekoppelt ist.

2. Gehäuse (300b) nach Anspruch 1, wobei:

sich die integrierte Photonik-Schaltung (315) zwischen einer zweiten Seite der Umverteilungsschicht (380) und der ersten Seite der PCB befindet und eine erste Seite der integrierten Photonik-Schaltung (315) an die zweite Seite der Umverteilungsschicht (380) über mindestens eine erste Lötsockerverbindung mechanisch gekoppelt ist;

sich die Ansteuerungs-IC zwischen einer zweiten Seite der Umverteilungsschicht (380) und der ersten Seite der PCB befindet und die erste Seite der Ansteuerungs-IC

- (i) an die zweite Seite der Umverteilungsschicht (380) über mehrere zweite Lötsockerverbindungen mechanisch und elektrisch gekoppelt ist; und
- (ii) an die erste Seite der integrierten Photonik-Schaltung (315) über mindestens eine der ersten Lötsockerverbindungen, mindestens eine der Umverteilungsschichtverbindungen (380) und mindestens eine der zweiten Lötsockerverbindungen elektrisch gekoppelt ist.

3. Gehäuse (300b) nach Anspruch 1 oder Anspruch 2, wobei sich der PCB-Hohlraum in der Nähe der integrierten Photonik-Schaltung (315) befindet.

4. Gehäuse (300b) nach einem der Ansprüche 1 bis 3, wobei:

sich die integrierte Photonik-Schaltung (315) innerhalb des Trägers befindet;

sich die Ansteuerungs-IC innerhalb des Trägers befindet; und

die Umverteilungsschicht (380) ferner über der ersten Seite der integrierten Photonik-Schaltung (315) und der ersten Seite der Ansteuerungs-IC (310) angeordnet ist.

5. Gehäuse (300b) nach Anspruch 4, wobei sich der

PCB-Hohlraum auf der ersten Seite der PCB befindet, derart, dass ein erster Teil der ersten Seite der integrierten Photonik-Schaltung (315) mit dem Hohlraum überlappt und ein zweiter Teil der ersten Seite der integrierten Photonik-Schaltung (315) mit der ersten Seite der PCB überlappt.

6. Gehäuse (300b) nach Anspruch 5, wobei die Umverteilungsschicht (380) über dem zweiten Teil der ersten Seite der integrierten Photonik-Schaltung (315), der mit der PCB überlappt, angeordnet ist.

7. Verfahren (600) zum Zusammenfügen eines Gehäuses für integrierte Komponenten (300b), wobei das Verfahren umfasst:

mechanisch und elektrisch Koppeln (605) mehrerer Kugelgitteranordnungsverbindungen an eine Leiterplatte, PCB, (305b) auf einer ersten Seite der PCB, wobei die PCB in der ersten Seite der PCB einen PCB-Hohlraum (325) besitzt, der dimensioniert ist, eine optische Faser (320) aufzunehmen;

mechanisch Koppeln (610) eines Trägers an die erste Seite der PCB auf einer ersten Seite des Trägers über mindestens eine der Kugelgitteranordnungsverbindungen (335), wobei die erste Seite des Trägers und die erste Seite der PCB einander zugewandt sind, wobei der Träger eine Umverteilungsschicht (380) enthält, die auf der ersten Seite des Trägers angeordnet ist und mehrere Umverteilungsschichtverbindungen (380) enthält;

mechanisch Koppeln (615) einer integrierten Photonik-Schaltung (315) an den Träger; und mechanisch Koppeln (620) einer Ansteuerungs-IC (310) an den Träger;

elektrisch Koppeln (625) einer ersten Seite der Ansteuerungs-IC an die erste Seite der PCB über mindestens eine der Umverteilungsschichtverbindungen (380) und mindestens eine der Kugelgitteranordnungsverbindungen (335); und

elektrisch Koppeln (630) der ersten Seite der Ansteuerungs-IC an die erste Seite der integrierten Photonik-Schaltung (315) über mindestens eine der Umverteilungsschichtverbindungen (380).

8. Verfahren (600) nach Anspruch 7, das ferner umfasst:

Anordnen der integrierten Photonik-Schaltung (315) zwischen einer zweiten Seite der Umverteilungsschicht (380) und der ersten Seite der PCB und mechanisch Koppeln einer ersten Seite der integrierten Photonik-Schaltung (315) an die zweite Seite der Umverteilungsschicht (380)

über mindestens eine erste Löthockerverbindung;

Anordnen der Ansteuerungs-IC zwischen einer zweiten Seite der Umverteilungsschicht (380) und der ersten Seite der PCB;

mechanisch und elektrisch Koppeln der ersten Seite der Ansteuerungs-IC an die zweite Seite der Umverteilungsschicht (380) über mehrere zweite Löthockerverbindungen; und

elektrisch Koppeln der ersten Seite der Ansteuerungs-IC an die erste Seite der integrierten Photonik-Schaltung (315) über mindestens eine der ersten Löthockerverbindungen, mindestens eine der Umverteilungsschichtverbindungen (380) und mindestens eine der zweiten Löthockerverbindungen.

9. Verfahren (600) nach Anspruch 7 oder Anspruch 8, wobei sich der PCB-Hohlraum in der Nähe der integrierten Photonik-Schaltung (315) befindet.

10. Verfahren (600) nach einem der Ansprüche 7 bis 9, das ferner umfasst:

Anordnen der integrierten Photonik-Schaltung (315) innerhalb des Trägers; und

Anordnen der Ansteuerungs-IC innerhalb des Trägers, wobei die Umverteilungsschicht (380) ferner über der ersten Seite der integrierten Photonik-Schaltung (315) und der ersten Seite der Ansteuerungs-IC (310) angeordnet ist.

11. Verfahren (600) nach Anspruch 10, das ferner umfasst, die integrierte Photonik-Schaltung (315) in dem PCB-Hohlraum in der ersten Seite der PCB anzuordnen, derart, dass ein erster Teil der ersten Seite der PCB mit dem Hohlraum überlappt und ein zweiter Teil der ersten Seite der integrierten Photonik-Schaltung (315) mit der ersten Seite der PCB überlappt.

12. Verfahren (600) nach Anspruch 11, das ferner umfasst, die Umverteilungsschicht (380) über dem zweiten Teil der ersten Seite der integrierten Photonik-Schaltung (315), der mit der PCB überlappt, anzuordnen.

Revendications

1. Un ensemble de composants intégrés (300b) comprenant :

une carte à circuit imprimé, ci-après PCB, (305b) ayant une cavité de PCB (325) dans un premier côté de la PCB dimensionné pour accepter une fibre optique (320) ;

une pluralité de connexions de réseau de grilles

à billes (335) reliées mécaniquement et électriquement à la PCB sur le premier côté de la PCB ; un support (365) directement relié mécaniquement au premier côté de la PCB sur un premier côté du support via au moins l'une des connexions du réseau de grilles à billes (335), le premier côté du support et le premier côté de la PCB étant tournés l'un vers l'autre, le support comprenant une couche de redistribution (380) disposée sur le premier côté du support et comprenant une pluralité d'interconnexions de couche de redistribution (380) ; un circuit intégré photonique (315) relié mécaniquement au support ; et un circuit intégré de commande (310) relié mécaniquement au support et ayant un premier côté qui est

(i) relié électriquement au premier côté de la PCB via au moins l'une des connexions de la couche de redistribution (380) et au moins l'une des connexions du réseau de grilles à billes (335), et

(ii) relié électriquement à un premier côté du circuit intégré photonique (315) via au moins l'une des interconnexions de la couche de redistribution (380).

2. L'ensemble (300b) selon la revendication 1, dans lequel :

le circuit intégré photonique (315) est situé entre un deuxième côté de la couche de redistribution (380) et le premier côté de la PCB, et un premier côté du circuit intégré photonique (315) est relié mécaniquement au deuxième côté de la couche de redistribution (380) via au moins une première connexion de liaison en relief ; le circuit intégré de commande est situé entre un deuxième côté de la couche de redistribution (380) et le premier côté de la PCB, et le premier côté du circuit intégré de commande est

(i) relié mécaniquement et électriquement au deuxième côté de la couche de redistribution (380) via une pluralité de deuxièmes connexions de liaison en relief ; et

(ii) relié électriquement au premier côté du circuit intégré photonique (315) via au moins l'une des premières connexions de liaison en relief, au moins une des interconnexions de la couche de redistribution (380) et au moins une des deuxièmes connexions en relief.

3. L'ensemble (300b) selon la revendication 1 ou la revendication 2, dans lequel la cavité de PCB est située de façon adjacente au circuit intégré photonique

(315).

4. L'ensemble (300b) selon l'une quelconque des revendications 1 à 3, dans lequel :

le circuit intégré photonique (315) est situé à l'intérieur du support ;

le circuit intégré de commande est situé dans le support ; et

la couche de redistribution (380) est en outre disposée à travers le premier côté du circuit intégré photonique (315) et le premier côté du circuit intégré de commande (310).

5. L'ensemble (300b) selon la revendication 4, dans lequel la cavité de PCB est située sur le premier côté de la PCB de telle sorte qu'une première partie du premier côté du circuit intégré photonique (315) chevauche la cavité et qu'une deuxième partie du premier côté du circuit intégré photonique (315) chevauche le premier côté de la PCB.

6. L'ensemble (300b) selon la revendication 5, dans lequel la couche de redistribution (380) est disposée à travers la deuxième partie du premier côté du circuit intégré photonique (315) qui chevauche la PCB.

7. Un procédé (600) d'assemblage d'un ensemble de composants intégrés (300b), le procédé comprenant :

le fait (605) de relier mécaniquement et électriquement une pluralité de connexions de réseau de grilles à billes (335) à une carte à circuit imprimé, ci-après PCB, (305b) sur un premier côté de la PCB, la PCB ayant une cavité de PCB (325) dans le premier côté de la PCB dimensionnée pour accepter une fibre optique (320) ; le fait (610) de relier mécaniquement un support au premier côté de la PCB sur un premier côté du support via au moins l'une des connexions du réseau de grilles à billes (335), le premier côté du support et le premier côté de la PCB étant tournés l'un vers l'autre, le support comprenant une couche de redistribution (380) disposée sur le premier côté du support et comprenant une pluralité d'interconnexions de couche de redistribution (380) ;

le fait (615) de relier mécaniquement un circuit intégré photonique (315) au support ; et

le fait (620) de relier mécaniquement un circuit intégré de commande (310) au support ;

le fait (625) de relier électriquement un premier côté du circuit intégré de commande au premier côté de la PCB via au moins une des connexions de la couche de redistribution (380) et au moins une des connexions du réseau à billes (335) ; et le fait (630) de relier électriquement le premier

- côté du circuit intégré de commande au premier côté du circuit intégré photonique (315) via au moins une des interconnexions de la couche de redistribution (380).
8. Le procédé (600) selon la revendication 7, comprenant en outre :
- le fait de placer le circuit intégré photonique (315) entre un deuxième côté de la couche de redistribution (380) et le premier côté de la PCB, et de relier mécaniquement un premier côté du circuit intégré photonique (315) au deuxième côté de la couche de redistribution (380) via au moins une première connexion de liaison en relief ;
 - le fait de placer le circuit intégré de commande entre un deuxième côté de la couche de redistribution (380) et le premier côté de la PCB ;
 - le fait de relier mécaniquement et électriquement le premier côté du circuit intégré de commande au deuxième côté de la couche de redistribution (380) via une pluralité de deuxième connexions de liaison en relief ; et
 - le fait de relier électriquement le premier côté du circuit intégré de commande au premier côté du circuit intégré photonique (315) via au moins l'une des premières connexions de liaison en relief, au moins une des interconnexions de la couche de redistribution (380) et au moins une des deuxième connexions de liaison en relief.
9. Le procédé (600) selon la revendication 7 ou la revendication 8, dans lequel la cavité de PCB est située de façon adjacente au circuit intégré photonique (315).
10. Le procédé (600) selon l'une quelconque des revendications 7 à 9, comprenant en outre :
- le fait de placer le circuit intégré photonique (315) à l'intérieur du support ; et
 - le fait de placer le circuit intégré de commande à l'intérieur du support, la couche de redistribution (380) étant en outre disposée en travers du premier côté du circuit intégré photonique (315) et le premier côté du circuit intégré de commande (310).
11. Le procédé (600) selon la revendication 10, comprenant en outre le fait de placer le circuit intégré photonique (315) dans la cavité de PCB dans le premier côté de la PCB de telle sorte qu'une première partie du premier côté du CIP chevauche la cavité et qu'une deuxième partie du premier côté du circuit intégré photonique (315) chevauche le premier côté de la PCB.
12. Le procédé (600) selon la revendication 11, comprenant en outre le fait de disposer la couche de redistribution (380) en travers de la deuxième partie du premier côté du circuit intégré photonique (315) qui chevauche la PCB.

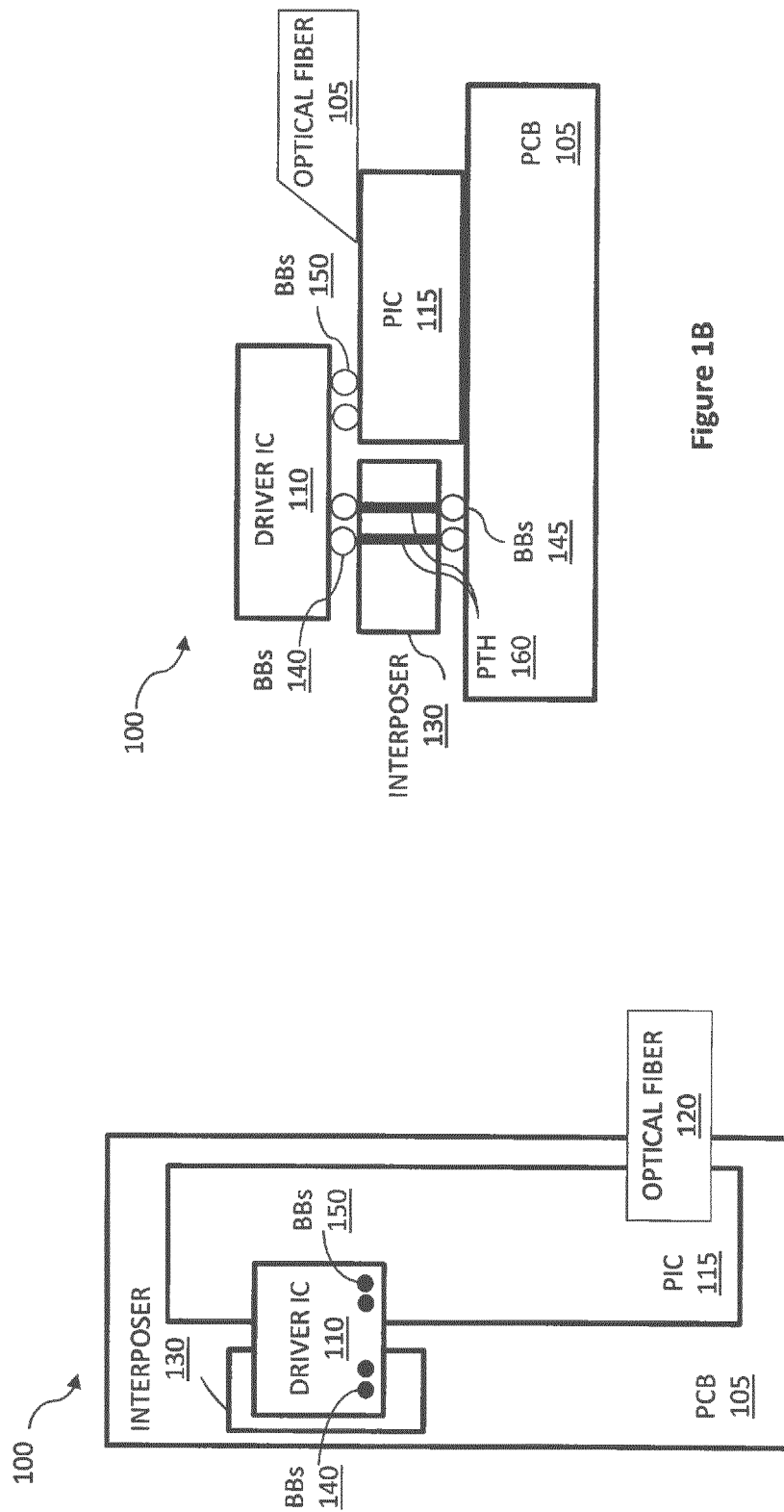


Figure 1B

Figure 1A

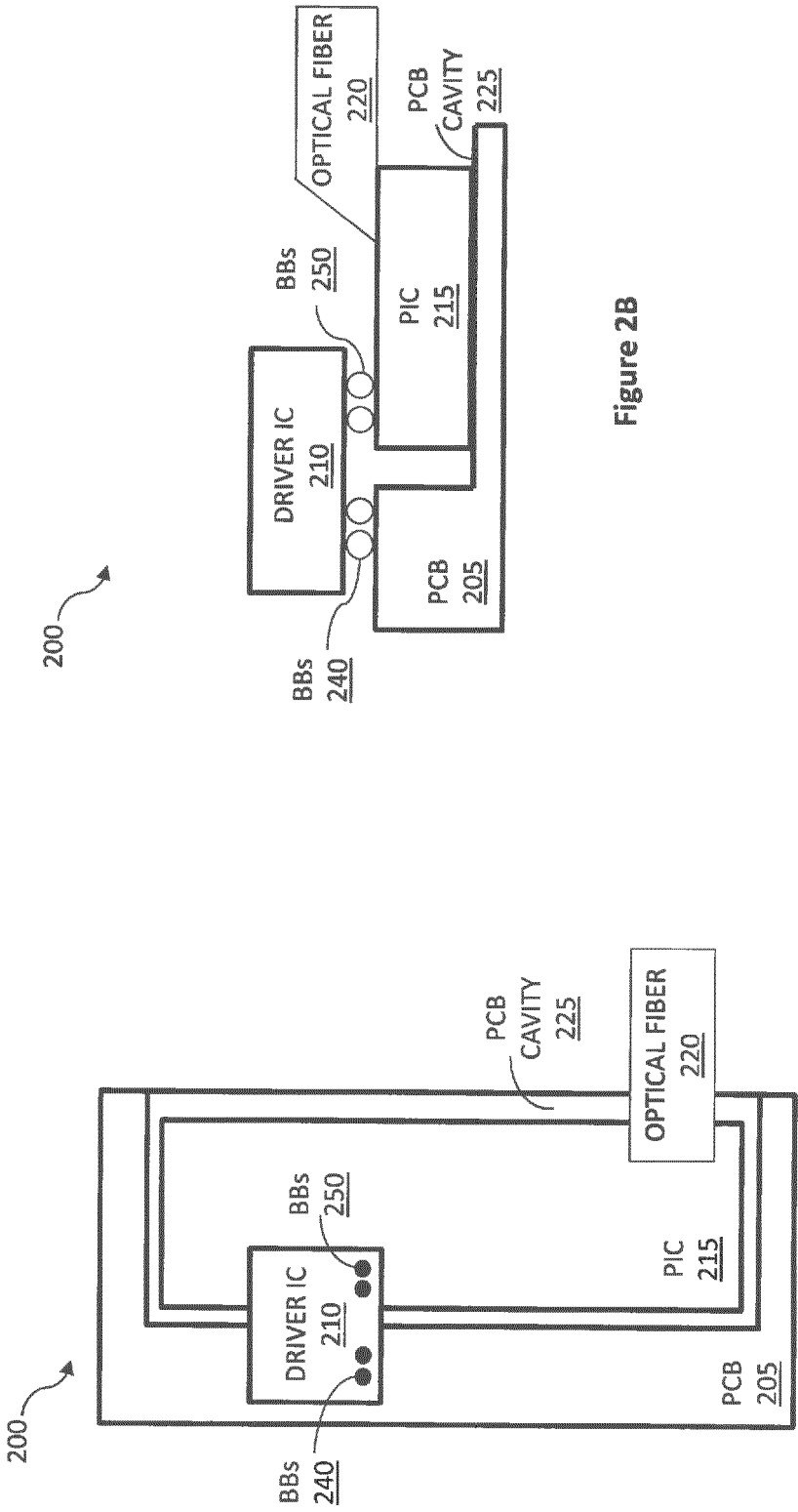
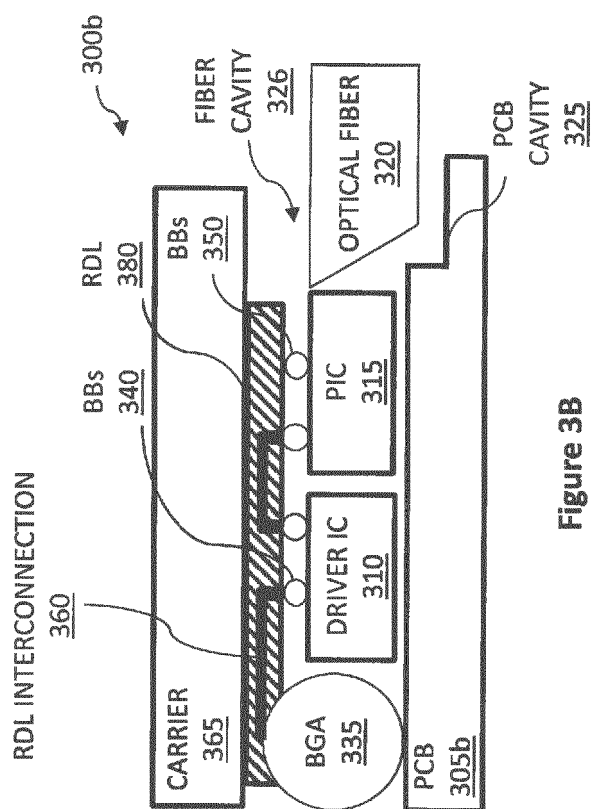
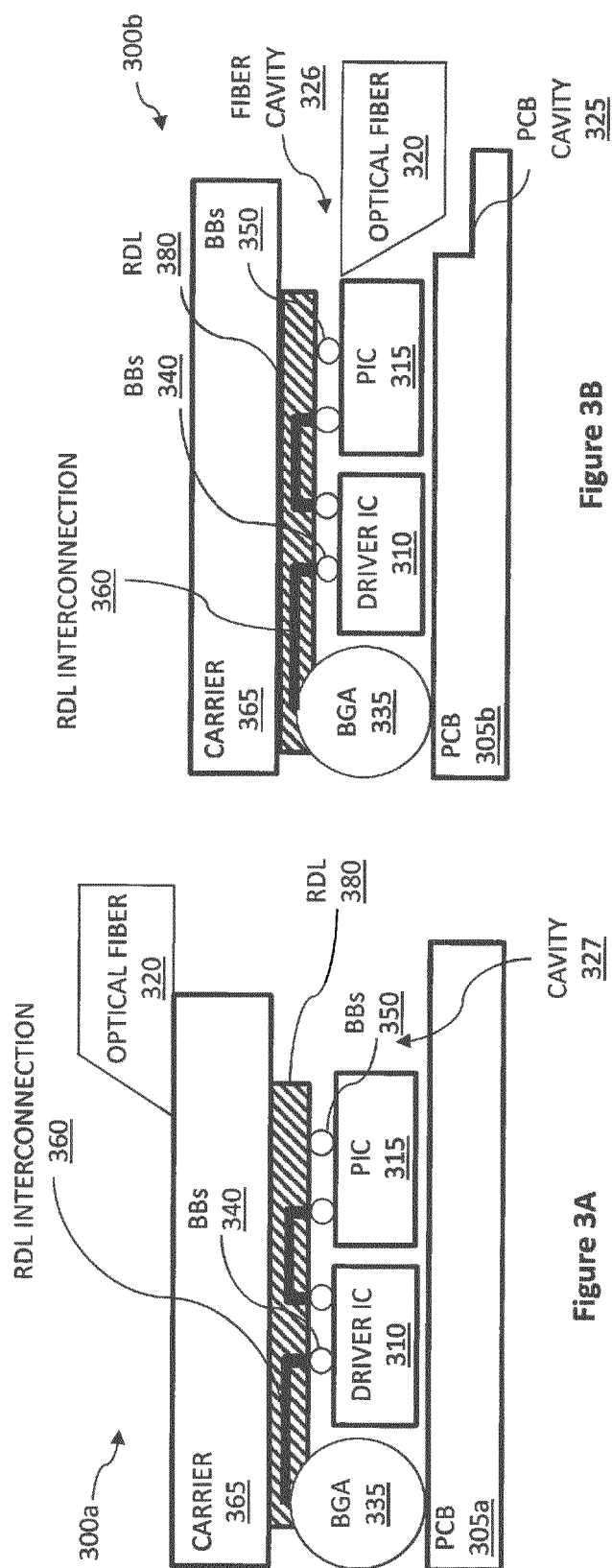


Figure 2B

Figure 2A



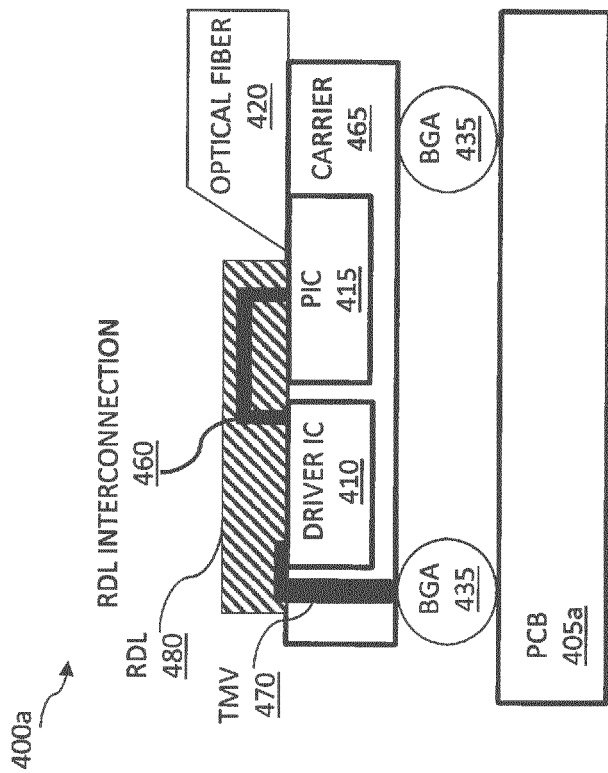


Figure 4A

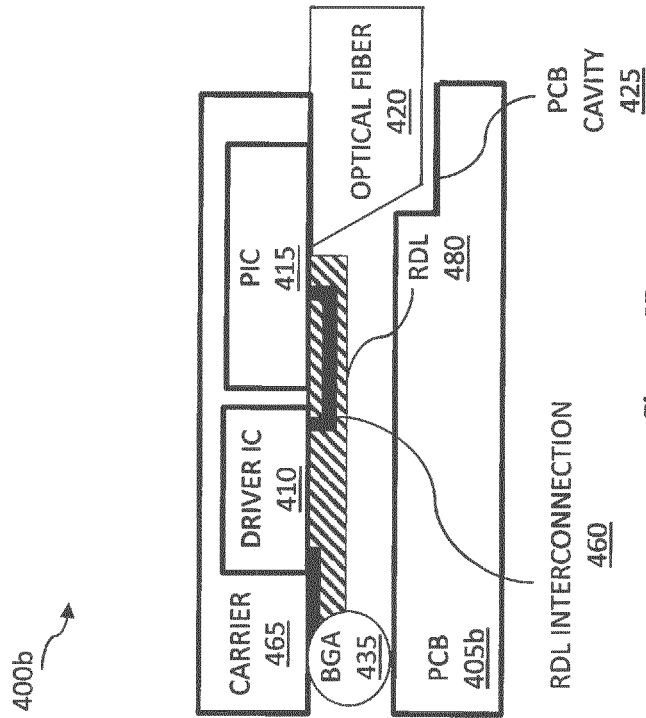


Figure 4B

500 ↗

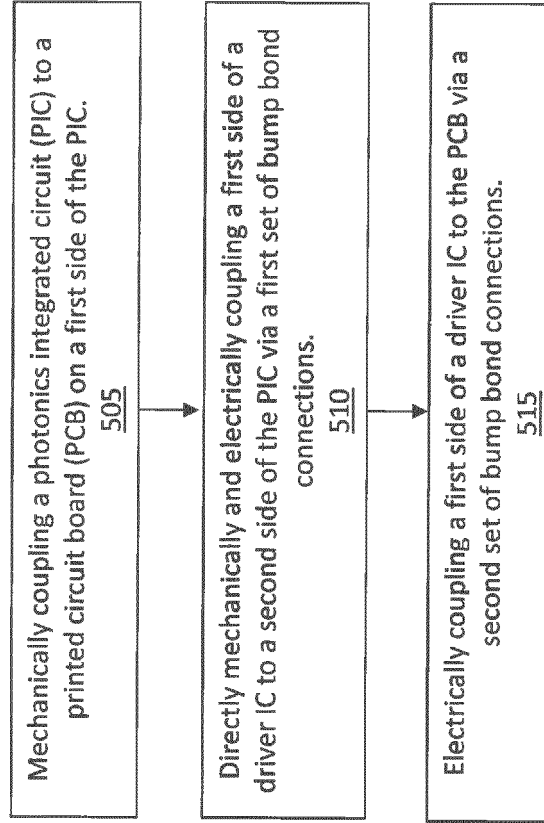


Figure 5

600 →

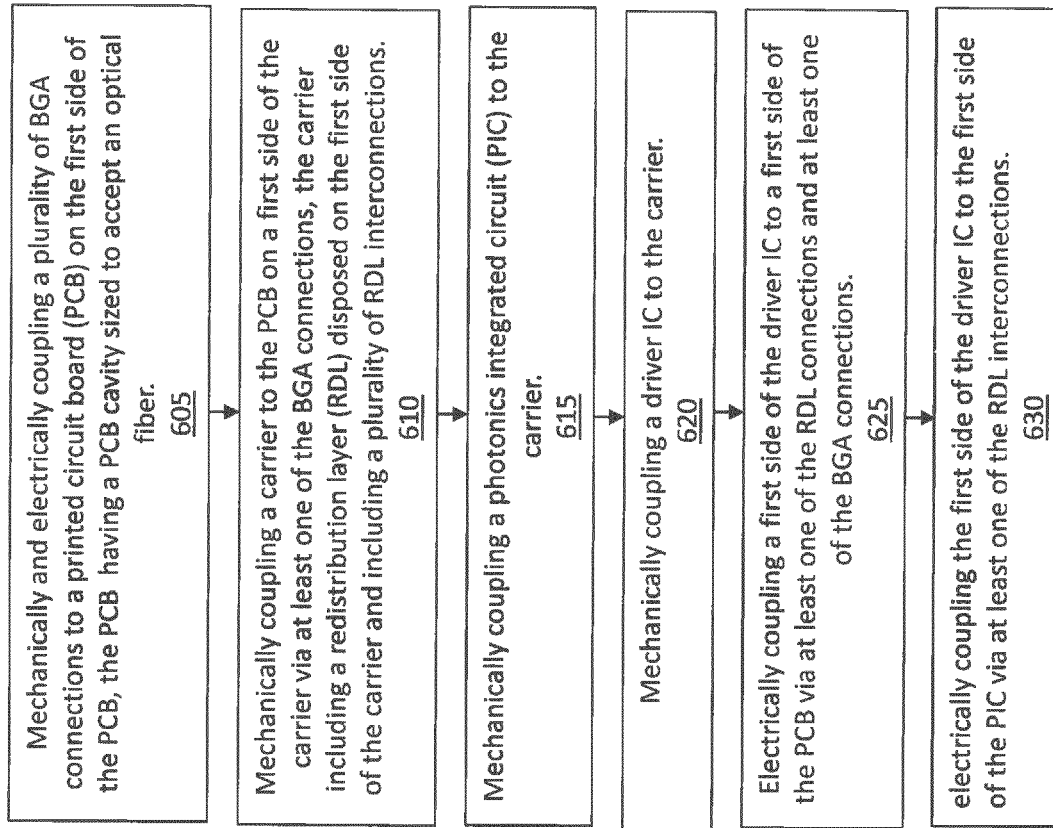


Figure 6

REFERENCES CITED IN THE DESCRIPTION

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