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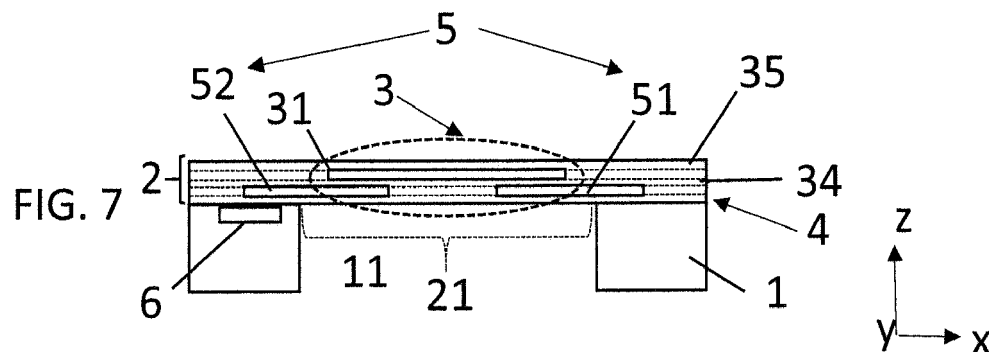
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(54) INFRARED DEVICE

(57) An infrared device comprises a substrate (1). A configuration (3) for one of absorbing and emitting infrared radiation is supported by the substrate (1). The configuration (3) comprises an electrically conducting layer arrangement (31) of less than 50 nm thickness between

dielectric layers (34,35). In addition, one or more of a thermal sensor (5) arranged for sensing the infrared radiation absorbed by the configuration (3), and a heater (7) arranged for heating the configuration (3) to emit the infrared radiation is supported by the substrate (1)



Description

Technical Field

[0001] The present invention relates to an infrared device, and to a method for manufacturing an infrared device.

Background Art

[0002] Conventional gas sensors based on infrared radiation are big in size and hence not suited for integration into mobile electronics, for example. Hence, it is desired to provide a small-scale infrared device that can inter alia be used in gas sensing applications.

Disclosure of the Invention

[0003] According to an aspect of the present invention, an infrared device is provided comprising a substrate. A configuration is supported by the substrate, i.e. arranged on or in the substrate. The configuration is adapted to absorb or to emit infrared radiation.

[0004] For this purpose, the configuration includes an electrically conducting layer arrangement of less than 50 nm thickness. The electrically conducting layer arrangement is arranged between dielectric layers.

[0005] The electrically conducting layer arrangement may include one or more electrically conducting layers, while a thickness of the entire arrangement is limited to 50 nm or less. In a preferred embodiment, the thickness of the electrically conducting layer arrangement is less than 40 nm, in a different embodiment it is less than 30 nm, and in a further embodiment, it is less than 20 nm.

[0006] The formation of the electrically conducting layer arrangement between dielectric layers preferably is such that the electrically conducting layer arrangement is sandwiched between the dielectric layers, i.e. is in direct contact with the dielectric layers. Accordingly, it is preferred that on top of an upper layer of the electrically conducting layer arrangement a dielectric layer is provided and is in contact with, while underneath a bottom layer of the electrically conducting layer arrangement another dielectric layer is provided and is in contact with. In case the electrically conducting layer arrangement consists only of a single layer, the dielectric layers are in touch with a top surface and a bottom surface thereof.

[0007] In case of the infrared device representing an infrared detector, incident infrared radiation is absorbed by the configuration including the electrically conducting layer arrangement, which preferably contributes significantly to the absorption. A temperature increase resulting from the absorbed infrared radiation is sensed by a thermal sensor of the device.

[0008] In case of the infrared device representing an infrared emitter, heat generated by a heater of the device evokes the configuration including the electrically conducting layer arrangement to emit infrared radiation.

[0009] It is assumed, that, in case of an infrared detector, incident infrared radiation leads to a standing wave in the configuration, and in particular to a standing wave between outer surfaces of the configuration. The electrically conducting layer arrangement is of a thickness that enhances absorption given that for layer arrangements with a larger thickness, reflection can be assumed rather than absorption. While the material of the electrically conducting layer arrangement can be considered as a broadband infrared absorber, the thickness of the layer arrangement, its vertical arrangement in the configuration, and preferably a thickness of the configuration may have impact on a dedicated wavelength range / band the detector is more sensitive to than to other wavelength ranges: Accordingly, while the configuration may be exposed to broad band infrared radiation, preferably only the infrared radiation in the defined band may be absorbed and converted into heat measured by the thermal sensor. In case the configuration is heated by a heater, the configuration preferably only emits infrared radiation in the defined band.

[0010] In a preferred application, it may be desired to detect and quantify infrared radiation of a given wavelength band only, which is supported by the configuration promoting selective absorption of infrared radiation, i.e. mainly in the defined wavelength band but close to zero absorption outside the defined wavelength band, at least outside the band in the infrared spectrum. Such band limited infrared absorption may serve as a basis for e.g. determining the presence of a gas compound in the environment of the device which gas compound e.g. may specifically absorb infrared radiation in the subject band. The band may be as narrow as to contain a single wavelength only, but in practice may rather encompass a wavelength range, preferably a wavelength range around a center frequency of interest, preferably representing a phase of a periodic modulation.. The defined wavelength band may be smaller than broadband, and preferably is less than 1 micrometer, and preferably less than 0.5 micrometer. The center wavelength in one embodiment may be 4.3 micrometers. In this respect, and in particular in case of a detector, the configuration may act as a filter for filtering the infrared frequencies of the subject band out of a broader band. In case of an emitter, the configuration preferably generates and emits infrared frequencies only in the subject band. As a result, infrared radiation only of the filtered band is preferably emitted from or absorbed by the configuration for further processing. Hence, in case of an emitter, a device is suggested providing infrared emission preferably in a narrow band which in turn may be beneficial in powering the device and in enhancing the spectral flux in the subject band per power unit supplied. In case of the device being designed as a detector, background noise from frequencies outside the band can be reduced or eliminated by preferred selective absorption in the band only. Hence, by means of the present embodiment, an emissive or receptive spectrum of infrared radiation can be shaped to a desired

band. The device as suggested in a preferred embodiment may be considered as wavelength selective in a range of wavelengths corresponding to the desired band, and hence either as a wavelength selective emitter or a wavelength selective detector.

[0011] The present device preferably can be used in gas sensing, spectroscopy, infrared imaging and / or signaling applications without limitation.

[0012] Hence, a broadband absorption layer in form of the electrically conducting layer arrangement is provided in / on the substrate, and preferably is integrated in a membrane spanning a recess manufactured into the substrate, as will be explained below. The electrically conducting layer arrangement preferably is taken from a standard CMOS layer stack deposited on the substrate, as will be explained further below. Hence, the electrically conducting layer arrangement can be derived from materials and structures already present in the CMOS back-end stack, which makes integration of the layer arrangement straightforward on an industrial scale.

[0013] Preferably, the substrate is a semiconductor substrate such as a silicon substrate, but in different embodiments the substrate may be a ceramic substrate or a substrate of a different material. An arrangement of the configuration on the substrate includes an arrangement directly on a surface of the substrate, or indirectly on any intermediate layer deposited on the substrate. Hence, it suffices that the substrate supports the configuration.

[0014] By means of the substrate supporting the thermal sensor or the heater as well as the configuration, a small-scale device can be manufactured. Preferably, all of the elements heater if any, thermal sensor if any, and configuration are arranged and / or integrated on or in the substrate, directly or indirectly, in a non-removable fashion. Such close arrangement may decrease electrical power required to operate the infrared emitter and / or lower optical power required to generate a signal of sufficient magnitude in the thermal sensor which in turn may reduce size of the device itself or the thermal sensor included in such a device. It is noted that the configuration may or may not include the thermal sensor and / or the heater.

[0015] In a preferred embodiment a recess is provided in the substrate, and a membrane spans at least a portion of the recess in the substrate. In such embodiment, it is preferred that the configuration is arranged on or in the membrane, or represents the membrane. The recess can be manufactured into the substrate by means of etching or otherwise removing material. The recess may go through the entire substrate and as such open the substrate from a backside thereof, while at a front side of the substrate opposite the backside a membrane is arranged spanning at least a portion of the recess. In a different embodiment, the recess does not lead through the entire substrate but forms a cavity in the front side of the substrate that at least is partially spanned by the membrane. In one embodiment, the membrane completely covers the recess without an exchange of gas through the mem-

brane from the recess to the outside or vice versa. In a different variant, the membrane may contain holes for allowing such exchange. The membrane may also take the shape of a bridge bridging the recess and allowing gas to be exchanged between the recess and a volume outside the membrane. A bridge-shaped membrane may be applied to an emitter device, and / or to a detector device. The membrane may be formed from a material applied to the front side of the substrate. Such material may include a layer stack which may contain dielectric layers and metal layers, preferably alternating, and preferably such as used in CMOS processing (Complementary Metal Oxide Semiconductor). Once substrate material is removed, e.g. from the backside of the substrate, a membrane may remain e.g. made from all or at least some layers of the stack, or made from all the layers of the stack and additionally from a portion of the substrate.

[0016] A thermal sensor, if any, may be arranged on or in the membrane, too, e.g. in case the thermal sensor includes one or more thermocouples that may be placed such that hot junctions thereof are arranged on or in the membrane, and cold junctions thereof are arranged outside the membrane on the or in close thermal contact with the substrate for allowing to detect a difference in temperature. In a different embodiment, a temperature sensor is provided based on measuring a resistance change. An example for such a resistive temperature sensor is a bolometer that preferably comprises a resistive temperature sensor made from e.g. metal wires arranged in the stack, and preferably in or on the membrane if any. A thermal mass of the bolometer is represented by the configuration.

[0017] The heater, if any, preferably is arranged on or in the membrane, if any, too, and as such may heat the configuration. High temperatures can be achieved in the membrane by low power owed to the small dimension of the membrane. At the same time, a thermal conduction along the thin membrane is sufficiently small not to induce high temperatures in the rest of the semiconductor chip, which otherwise would impact any electronic circuitry which in one embodiment may be integrated in the substrate, e.g. by CMOS processing. The vast difference of thermal masses of membrane and substrate in addition ensure that the substrate may to a large extent remain at room temperature. Such electronic circuitry may be integrated for one or more of controlling the heater and / or for processing signals from the thermal sensor in form of a determination unit as will be explained later on.

[0018] A good thermal isolation is achieved, in case the configuration and the thermocouples or the resistive temperature sensor are arranged on or in a membrane. In such embodiment, an additional temperature sensor in form of a resistive wire or a thermocouple may be provided and arranged on or in the membrane for monitoring a temperature thereof. Preferably, the measured temperature is used for controlling a temperature of the membrane e.g. by a heater. By such means, it could be compensated for drifts induced by degradation of the heater

if any during operation.

[0019] The configuration preferably comprises layers / material left over from a stack of layers deposited on the substrate e.g. within CMOS processing the substrate, wherein the stack of layers preferably is a stack of CMOS layers deposited on the substrate. Such CMOS layer stack typically includes dielectric and electrically conductive layers arranged in alternating fashion. A dielectric layer may be made from one of SiO₂, or SiN, for example. A conductive layer may e.g. be a metal layer, e.g. made from one of Al, Cu. The stack may additionally include semiconducting layers. In case of a membrane being formed by the layer stack, the configuration may be formed by the respective layers in the portion of the stack spanning the recess, which is the membrane.

[0020] It is preferred that the electrically conducting layer arrangement represents a layer arrangement available in the CMOS layer stack arranged on the substrate. Hence, a structure already existing in the CMOS layer stack is used for infrared detection or emission purposes, however, with the stack experiencing treatment prior to making use of the subject layer arrangement for infrared purposes. Preferably, the electrically conducting layer arrangement is one of an adhesion layer for adhering the inter metal dielectric to a metal layer of the CMOS layer stack, and / or a diffusion barrier for preventing diffusion between the inter metal dielectric and a metal layer. Accordingly, it is assumed that a metal element in the CMOS layer stack not only comprises the metal layer - such as Al or Cu -, but underneath and above provides for a thin electrically conductive layer arrangement - be it a single layer, a double layer or a multi-layer - that either serves for adhering the metal layer to the adjacent inter metal dielectric or that serves as diffusion barrier for protecting the metal layer. Such electrically conductive layer arrangement has a considerably lower thickness than the metal layer itself to which it is attached to. While the metal layer may have a thickness of typically more than 100 nm, the electrically conducting layer arrangement attached to it on both sides preferably has a thickness of less than 50 nm.

[0021] However, in contrast to its original arrangement in the CMOS layer stack, the electrically conducting layer arrangement in the present invention is no longer arranged between the metal layer on the one hand and the inter metal dielectric on the other hand, but is arranged between dielectric layers on both sides.

[0022] Preferably, when using a metal element of a CMOS layer stack the electrically conducting layer arrangement used for infrared purposes preferably is the lower one, i.e. the electrically conducting layer arrangement in a vertical direction towards the substrate. Hence, the dielectric layer underneath the electrically conducting layer arrangement is an inter metal dielectric of the CMOS layer stack. Instead, the dielectric layer on top of the electrically conducting layer arrangement is a dielectric layer explicitly applied to the electrically conducting layer arrangement, such as a passivation layer, and in

particular a SiN layer, in particular after having removed the metal layer and the electrically conducting layer arrangement on top of the metal layer.

[0023] Preferably, the electrically conducting layer arrangement comprises or consists of an interstitial compound comprising one of the metals of group VI to VIII, and preferably of nitride embedded into a metal structure. Accordingly, in one embodiment, the electrically conducting layer arrangement comprises or consists of a Ti layer and a TiN layer. In a different embodiment, the electrically conducting layer arrangement comprises or consists of a Ta layer and a TaN layer. In a further embodiment, the electrically conducting layer arrangement comprises or consists of a layer of one of Al, Cu, Pt, W.

[0024] The dielectric layer on top of the electrically conducting layer arrangement preferably comprises a dielectric tuning layer between the passivation layer and the electrically conducting layer, for tuning the configuration to the desired thickness.

[0025] In addition to the electrically conducting layer arrangement, the configuration may comprise an electrically conducting layer stack, representing e.g. a metal element of the CMOS layer stack. As is explained above, such electrically conducting layer stack preferably is arranged between dielectric layers, preferably has a thickness of more than 100 nm, and preferably is arranged between the electrically conducting layer arrangement and a bottom layer of the configuration. It is preferred that the electrically conducting layer stack comprises or consists of a metal layer arranged between two further electrically conducting layer arrangements. Accordingly, in this embodiment the electrically conducting layer arrangement serving for infrared detection / emission is not built from the bottom most level of metal elements - referred to as M1 metal layer in the CMOS layer stack - but is built from a metal element in at least the next level - referred to as M2 metal layer in the CMOS layer stack. The purpose of the integration of such electrically conducting layer stack also referred to as metal element may be two-fold: On the one hand, and in one embodiment of the present invention, the metal layer of this electrically conducting layer stack may together with another electrically conducting layer of a different material be electrically connected to form one or more thermocouples serving as thermal sensor, or may possibly contribute to implement a heater. On the other hand, the integration of such electrically conducting layer stack may serve as a mirror for reflecting incident infrared radiation, and hence support an infrared detector that only can sense infrared radiation from one side, e.g. from above given that the electrically conducting layer stack is arranged between the electrically conducting layer arrangement and the thermal sensor: Infrared radiation incident from the side of the thermal sensor may only slightly be absorbed owed to a lack of an absorbing element on this side while the electrically conducting layer stack reflects the incident infrared radiation to a large extent owed to its thickness. However, infrared radiation incident from the side of the

electrically conducting layer arrangement may largely be absorbed by the electrically conducting layer arrangement on this side, and non-absorbed infrared radiation travelling through to the electrically conducting layer stack may be reflected there owed to its thickness and again pass the electrically conducting layer arrangement and be absorbed there. Accordingly, this embodiment also improves the sensitivity of the infrared detector.

[0026] According to another aspect of the invention, an infrared device according to any of the above embodiments is used and / or arranged as an infrared detector, wherein the thermal sensor is included rather than the heater. The infrared detector, however, may be exposed to broadband infrared radiation e.g. being received from a measuring volume that is in turn irradiated by an infrared heater, and preferably by an infrared heater of one of the previous embodiments. It is preferred in such scenario, that the configuration of the infrared emitter and the configuration of the infrared detector are identical such that the emitter selectively emits infrared radiation in the defined band into the measurement volume, and the detector selectively absorbs infrared radiation in the defined band, which is the portion of the selectively emitted radiation that is not absorbed by the gas compound to be detected. The signal supplied by the thermal sensor of the infrared detector may be evaluated by a determination unit and may indicate a concentration of the gas compound within the gas in the measuring volume.

[0027] In one embodiment, the infrared device comprises an encapsulation for sealing a volume at one or both sides of the membrane or the substrate. The sealed volume may reduce the effect of heat conduction or convection to / from ambient air. The sealed volume may be evacuated or filled by a protective gas. Such encapsulation preferably includes a window for allowing the configuration to be exposed to the infrared radiation. The encapsulation can also be applied to a device including one or more thermocouples as thermal sensor, and to an infrared emitter.

[0028] The infrared based sensor preferably comprises a volume between the infrared emitter and the infrared detector for accepting a gas to be investigated as to the presence or absence and / or the concentration of a specific gas compound in that gas. Given that the concept of infrared based sensing includes the gas compound to absorb radiation of the band / wavelength the emitter and the detector are tuned to selectively emit / absorb, and specifically to build a relation between the radiant flux at this wavelength at the emitter and the radiant flux at this wavelength at the detector after travelling the volume, an amount of radiation absorbed by the gas compound present in the volume can be derived which is proportional to a concentration of this gas compound in the volume. Emitter and detector can be arranged in a common plane, e.g. on a common carrier, and may be arranged at different ends of the common carrier. A reflector may be provided in the infrared based sensor for deflecting the emitted radiation towards the detector.

[0029] It is preferred that the detector includes an encapsulation for sealing a volume at one or both sides of each of the substrate / membranes. In such embodiment, a window is provided in the encapsulation for allowing the configurations of the detector to be exposed to the infrared radiation, which window is coupled to the volume between the emitter and the detector. A window may also be provided in an encapsulation of an emitter which may prevent convection from ambient air to impact a temperature distribution on a membrane of the emitter.

[0030] For example, a gas compound to be detected is CO₂. Such gas sensor can be realized at chip scale, hence requiring a chip area of few mm², wherein commercial CO₂ sensors, for example, require a footprint on the order of several cm², which prohibits their deployment in applications where small sensor dimensions are important such as in mobile applications including mobile phones, tablets, etc.

[0031] It is preferred to integrate circuitry in the detector which circuitry is configured to filter the signals of the thermal sensor/s, amplify, and calibrate onchip, thus limiting noise pick-up from the environment to a minimum. Such circuitry preferably is integrated into the substrate of the detector.

[0032] According to another aspect of the present invention, a method is provided for manufacturing an infrared device. A wafer is provided including a substrate and a CMOS layer stack arranged on the substrate, which CMOS layer stack includes at least one metal layer arranged between two electrically conducting layer arrangements of less than 50 nm thickness each serving as one or more of an adhesion layer and a diffusion barrier between the metal layer and inter metal dielectrics next to each of the electrically conducting layer arrangements. In a first step the inter metal dielectric arranged on top of an upper of the electrically conducting layer arrangements as well as the upper electrically conducting layer arrangement is removed. Next the metal layer is removed. Finally, a dielectric layer is deposited on the lower of the electrically conducting layer arrangements released by the removal of the metal layer. Accordingly, the CMOS layer stack is modified such as to release the bottom electrically conducting layer arrangement of an electrically conducting layer stack, which electrically conducting layer arrangement originally promotes adhesion or prevents diffusion into the removed metal layer.

[0033] Preferably, the top inter metal dielectric and the upper electrically conducting layer arrangement are removed in a common etching step. The metal layer preferably is removed in a separate etching step.

[0034] In a specific embodiment, a Ti / TiN layer sandwich with corresponding thicknesses in the order of 8nm and 20 nm in a CMOS thermopile membrane is used as electrically conducting layer arrangement for infrared sensing or emitting. The layer sandwich preferably is derived from the adhesion / diffusion barrier layers on the bottom of the aluminum metallization layers used in the CMOS process.

[0035] For structuring the CMOS thermopile membrane, it is preferred to apply an etch stop layer integrated in the form of a plate-like structure patterned on one of the metallization layers of the CMOS backend stack that allows for controlling the thickness of the CMOS thermopile membrane. The etch stop layer preferably is removed in a wet etching process. The Ti/TiN arrangement under the aluminum normally is removed in an extra etching step. However, by skipping this step, the Ti/TiN bi-layer can be kept in the membrane, as the aluminum etch is highly selective with respect to Ti and TiN. The remaining bi-layer arrangement has been experimentally shown to significantly increase infrared absorption in the wavelength band of ~4 μm , relevant for CO₂ detection.

[0036] The subject gas sensor preferably can be manufactured compatible to CMOS processing and hence is compatible with wafer-scale fabrication schemes.

Brief Description the Drawings

[0037] Embodiments of the present invention, aspects and advantages will become apparent from the following detailed description thereof. Such description makes reference to the annexed drawings, wherein the figures show:

Figs. 1 a cut through a CMOS layer stack as used in a method for manufacturing an infrared device, according to an embodiment of the present invention;

Fig. 2 a method for manufacturing an infrared device, according to an embodiment of the present invention;

Figs. 3 to 6 configurations in cut view as used in infrared devices according to embodiments of the present invention; and

Figs. 7 to 11 infrared devices according to embodiments of the present invention.

Detailed Description the Drawings

[0038] Same elements are referred to by same reference numerals across all figures.

[0039] Figure 1 illustrates a cut through a CMOS layer stack 2 such as used in a method for manufacturing an infrared device according to an embodiment of the present invention. The CMOS layer stack comprises various metal elements 9 and inter metal dielectrics collectively referred to as inter metal dielectrics 4. Such CMOS layer stack 2 is generated by depositing metal and dielectric material on a substrate, such as a semiconductor and in particular a silicon substrate, and by structuring the material. Presently, the CMOS layer stack 2 comprises six metal elements 9 arranged on six different levels in vertical direction z originally separated by the various inter metal dielectrics referred to by "IMDxy". Presently, electrically conducting vias 91 are already manufactured between neighboring metal elements 9 in order to allow

electrically conducting paths throughout the entire CMOS layer stack 2 in vertical direction z.

[0040] The metal element 9 on the second level from the bottom is zoomed in and is shown in more detail below: Such metal element 9 includes a stack of layers, wherein a core layer is referred to as metal layer 32 presently made from aluminum Al. In the CMOS layer stack 2, this metal layer 32 is provided as electrically conducting path for interconnecting elements. The metal layer 32 is sandwiched between two electrically conducting layer arrangements, the upper of which in z-direction is referred to by 33, and the lower of which in z-direction is referred to by 31. Each of the electrically conducting layer arrangements 31 and 33 comprises a first layer 311, and 331, respectively, presently made from titanium Ti, and a second layer 31, and 332, respectively, made from titanium nitride TiN. Presently, each electrically conducting layer arrangement 31 and 33 serves the purpose of one or more of an adhesion layer for adhering the inter metal dielectric 4 to the metal layer 32, and a diffusion barrier for preventing diffusion between the inter metal dielectric 4 and the metal layer 32.

[0041] Figure 2 illustrates in diagrams a) to d) steps for manufacturing an infrared device according an embodiment of the present invention. In diagram 2a) a wafer is provided including a substrate 1 and a CMOS layer stack 2 arranged on the substrate 1. The substrate 1 does not scale with respect to the CMOS layer stack 2 but is shown much thinner than in real life compared to the CMOS layer stack 2. The substrate preferably is a semiconductor substrate 1. A photo resist 8 is arranged on top of the wafer.

[0042] The CMOS layer stack 2 comprises metal elements 9 on various levels of the CMOS layer stack 2, and already structured in the horizontal plane x,y. Between the metal elements 9, inter metal dielectric 4 is provided for electrically disconnecting the metal elements 9 from each other. Each metal element 9 includes an electrically conducting layer stack such as is shown for the metal elements 9 in Figure 1, for example. In particular, it is assumed that each metal element 9, and hence, each electrically conducting layer stack comprises a metal layer, such as the metal layer 32 of Figure 1 made from Al, arranged between two electrically conducting layer arrangements, such as the arrangements 31 and 33 comprising a layer 311, 331 of Ti, and a layer 312, 332 of TiN, see Figure 1, again serving for one or more of adhesion or diffusion barrier purposes. Some of the metal elements 9 shown in the wafer of diagram 2a), especially those on the left hand side of the wafer, may be structured and arranged for providing electrical conducting paths within the inter metal dielectric for later on connecting electronic elements integrated into the substrate 1.

[0043] On the right hand side of the wafer of diagram 2a), any upper metal elements are either completely removed or were not deposited from the beginning, such that only a bottom most metal element 92 extends hori-

zontally while no further metal levels are provided on levels above this bottom most metal element 92. In addition, to the left of the bottom most metal element 92, metal element is provided to allow for structuring a step.

[0044] The infrared device as shown in diagram 2a) may further extend to the right as is indicated. The state as shown in diagram 2a) is an intermediate state during the manufacturing of an infrared device, which manufacturing makes use of the layers typically present in a CMOS layer stack 2.

[0045] According to diagram 2b), in a next manufacturing step any inter metal dielectric 4 on top of the bottom most metal element 92 is removed, preferably by way of wet etching. In such etching step, which preferably is a dry etching step, the upper electrically conducting layer arrangement 33 is removed together with the inter metal dielectric 4. The metal layers 32 of each metal element 92 and 93 serve as an etch stop in this manufacturing step, such that the metal layers 32 of each metal element 92 and 93 are exposed as is shown in diagram 2b).

[0046] According to diagram 2c), the metal layers 32 of the metal elements 92 and 93 as exposed in response to the manufacturing step of diagram 2b) are now removed in a separate etching step, preferably by means of wet etching. The result is shown in diagram 2c): The lower electrically conducting layer arrangement 31 of each metal element 92 and 93 serves as etch stop and now is released. Preferably, the now released electrically conducting layer arrangements 31 each comprise a metal layer and a metal nitride layer such as is shown in Figure 1.

[0047] In the following step illustrated in diagram 2d), the photo resist 8 is removed, and in particular the released electrically conducting layer arrangements 31 are now covered with a dielectric layer 35, preferably in form of a passivation layer made from SiN. In addition, a recess 11 is etched into the substrate 1 which makes the remaining layers form a thin membrane 21 thermally insulating the membrane 21 from the substrate 1 to a large extent.

[0048] In particular, the leftovers of metal element 92 which completely are arranged in the membrane 21, in combination with the leftover inter metal dielectric 4 and the dielectric layer 35, and possibly any other layer comprised in the membrane 21, forms a configuration 3 with the electrically conducting layer arrangement 31 absorbing or emitting infrared radiation, but previously serving as lower adhesion layer or diffusion barrier for the metal layer 32 removed in the meantime. Accordingly, layer/s of the CMOS layer stack, which previously were serving the protection of the metal layer 32 now are used for the complete different purpose of infrared sensing / emitting.

[0049] Figure 3 illustrates a configuration 3 as used in an infrared device according to an embodiment of the present invention. So do each of Figures 4 to 6. It is understood, that each configuration 3 may be arranged on a substrate, or, in an alternate embodiment, may form a membrane arranged on and preferably spanning a re-

cess manufactured in the substrate.

[0050] While these embodiments are described by referring to the layers contributing to the configurations, individual materials and thicknesses of the individual layers are suggested in each of the Figures 3 to 6. These materials as well as the thicknesses are only considered as preferred embodiments. Other materials may be applied according to the constraints presented earlier in the application. For each layer thickness provided, it is assumed that an alternative thickness may be found in the range of the given layer thickness +/- 20 per cent.

[0051] According to the cut view of Figure 3, the configuration 3 includes an electrically conducting layer arrangement 31, presently comprising a TiN layer 311 and a Ti layer 312. A dielectric 35 is arranged on top of the electrically conducting layer arrangement 31, such as a passivation layer 351, e.g. made from SiN. Underneath the electrically conducting layer arrangement 31, in -z-direction, another dielectric 34 is provided, e.g. in form of an inter metal dielectric, such as made from SiO₂. A bottom layer 30 of the configuration 3 may be another dielectric layer, such as a SiO₂ layer. Between layers 30 and 34, a polysilicon layer 39 is arranged. Accordingly, the present configuration 3, when e.g. representing a membrane, may in vertical direction z be confined by the top most dielectric 35 and the bottom layer 30.

[0052] The frequency of infrared radiation absorbed or emitted by the configuration 3 of an infrared device may also depend on the overall thickness of the configuration 3. The overall thickness of the configuration of the embodiment of Figure 3 may be given by an accumulation of the thicknesses of the individual layers contributing to the configuration 3.

[0053] However, in case the overall thickness is desired to be tuned in order to manipulate the frequency sensitivity of the configuration 3, the top most dielectric 35 may not only comprise the passivation layer 351, but also an additional dielectric layer 352, e.g. in form of an SiO₂ layer deposited on the electrically conducting layer arrangement 31. The corresponding configuration is shown in Figure 4. By such means, the overall thickness of the configuration is tuned, and may be adjusted so as to optimize the sensitivity of infrared frequencies in a desired range.

[0054] The configuration of Figure 5 differs from the configuration of Figure 3 in that between the electrically conducting layer arrangement 31 and the bottom most layer 30 an electrically conducting layer stack 36, 37, 38 is included, which preferably represents a metal element 9 as introduced in Figure 1. Such electrically conducting layer stack 36, 37, 38 comprises a metal layer 38, and associate electrically conducting layer arrangements 36 and 37, again originally serving as adhesion layer and / or diffusion barrier. However, in contrast to the embodiment of Figure 3, the present metal element remains in the CMOS layer stack 2 and is not partially removed. Accordingly, in the embodiment of Figure 5, the electrically conducting layer stack 36, 37, 38 may represent a

full metal element 9 according to Figure 1, e.g. of metal layer M1 in a conventional CMOS layer stack. As such, the electrically conducting layer stack 36, 37, 38 preferably shows a thickness of 100 nm and more, wherein the metal layer 38, such as made from Al, requires a majority of the stack thickness, while the adjacent electrically conducting layer arrangements 36 and 37 are of minor contribution to the overall thickness. The adjacent electrically conducting layer arrangements 36 and 37 preferably are made from the same materials as the electrically conducting layer arrangement 31.

[0055] Accordingly, another inter metal dielectric is introduced, referred to as layer 301, e.g. made from SiO₂. In this context, the polysilicon layer may be considered as electrically conducting layer 39 that is arranged between the other electrically conducting layer stack 36, 37, 38 and the bottom most layer 30. The electrically conducting layer stack 36, 37, 38 and the electrically conducting layer 39 preferably contribute to one or more thermocouples, and as such are at least connected once, e.g. by means of a via through layer 301. Such one or more thermocouples, e.g. contributing to thermopiles, preferably serve as thermal sensor for receiving the thermal energy absorbed by the configuration. Accordingly, the present configuration also includes means for measuring the absorbed infrared radiation.

[0056] In all Figure 3 to 6, layer 39 is optional, but preferred if contributing to a thermocouple, for example.

[0057] Figure 6 shows another embodiment of a configuration, representing a combination of the embodiments shown in Figures 4 and 5. Accordingly, the present configuration includes the electrically conducting layer stack 36, 37, 38 and the electrically conducting layer 39 for possibly contributing to a thermocouple or thermopile, and at the same time a thickness tuning element in form of layer 352.

[0058] Figure 7 illustrates a cut through an infrared device according to an embodiment of the present invention. It is assumed that this infrared device is exposed to infrared radiation incident from outside the device. The device comprises a substrate 1 and a stack of layers 2 arranged on the substrate 1. The substrate 1, which preferably is a semiconductor substrate, has a recess 11 through an entire thickness of the substrate 1, the recess 11 being made e.g. from etching or otherwise removing material from the substrate 1. The recess 11 generates a membrane 21 made from the layer stack 2 spanning the recess 11 in the substrate 1. The layer stack 2 comprises multiple layers, one of which is an electrically conducting layer arrangement 31 such as introduced in the previous Figures. The infrared device according to Figure 7 may also be referred to as semiconductor chip comprising the bulk substrate 1, such as silicon bulk material, which is covered a CMOS layer stack 2 as defined in CMOS processing, but which is processed afterwards in order to enable infrared detection. The layer stack 2 preferably is used for building a configuration 3 - referred to by a dotted ellipse - designed for absorbing infrared ra-

diation.

[0059] Presently, the electrically conducting layer arrangement 31 extends only across or within the membrane 21 in the x-y plane of the device. Otherwise a thermal short may be achieved to the substrate 1 thereby reducing the responsivity and / or sensitivity.

[0060] The infrared device of Figure 7 comprises a thermal sensor 5 in form of two thermopiles indicated by reference numerals 51 and 52. The thermopiles 51 and 52 are preferably made from a metal and / or a polysilicon layer of the layer stack 2, such as is introduced in the embodiments of Figures 5 and 6. Each thermopile 51, 52 includes a multitude of thermocouples connected to each other at junctions. The junctions reside either on the membrane 21 or outside the membrane 21 on the substrate 1 such that a thermal difference can be detected, wherein the hot junctions of the thermopiles reside on the membrane 21 and are arranged to sense a temperature difference of the membrane 21 at these hot junctions with respect to the temperature of the substrate 1 which temperature is proportional to the radiation emitted by the configuration 3. Hence, the infrared radiation applied to and absorbed by the configuration 3 is converted into heat which heat is sensed by the thermal sensor 5. A circuitry 6 may be integrated into the substrate 1, e.g. a silicon substrate, serving as determination unit for evaluating signals provided by the thermal sensor 5.

[0061] Figure 8 illustrates a cut through an infrared device according to another embodiment of the present invention. Many elements are identical to the embodiment of Figure 7 and are therefore not labelled again in view of enhancing illustration. The infrared device of Figure 8 differs from the device of Figure 7 in that it is an infrared emitter instead of an infrared detector.

[0062] A heater 7 is arranged in a metal layer of the stack of layers 2, e.g. in form of a resistive heater a few meandering lines of which are indicated in Figure 8. The heater 7 is arranged for heating the configuration 3. Preferably, electronic circuitry 6 is integrated into the infrared device which circuitry may be connected to the heater 7 and be configured to control the heater 7, e.g. by switching a power switch on or off. Hence, the configuration 3 and the heater 7 are arranged in the membrane 21 above the recess 11. This arrangement is owed to reducing a heat transfer from the membrane 21 to the rest of the substrate 1.

[0063] By switching on the heater 7 and applying heat to the configuration 3, the configuration 3 is triggered to emit infrared radiation.

[0064] Figure 9 illustrates another cut through an infrared device according to a further embodiment of the present invention. The infrared device of Figure 9 again is an infrared detector and differs from the detector of Figure 7 in that instead of thermopiles 51, 52 a bolometer 53 is used as thermal sensor. The bolometer 53 presently comprises a resistive temperature sensor 53 made from conductive structures, such as metal wires, arranged in the membrane 21, and preferably from one of the con-

ductive layers of the stack 2, preferably a layer underneath the layers contributing to the electrically conducting layer arrangement 31. In combination with the configuration 3, and supported by a good thermal isolation provided by the membrane 21, the resistive temperature sensor 53 builds the bolometer.

[0065] The infrared detector of Figure 10 differs from the infrared detector of Figure 9 in that a volume on both sides of the membrane 21 is limited by an encapsulation. The encapsulation is made from two substrates 12 and 13, e.g. silicon substrates, bonded to the stack of layers 2 or to the substrate 1 by suitable means, e.g. by an adhesive 15. The volume in the encapsulation may be evacuated or may be filled with a protection gas in order to enhance infrared transmission.

[0066] A different variant of encapsulation is shown in Figure 11. A single cap 14 is used as encapsulation, which cap preferably is attached to the layer stack 2, e.g. by bonding. In the present example, the substrate 11 does not have a recess 11 such that there is no backside of a membrane to be evacuated.

[0067] In both embodiments of Figure 10 and Figure 11, infrared radiation from a measurement volume outside the device is desired to meet the configuration 3 of the device such that a window 121 and 141 respectively is arranged in the encapsulation 12 or 14, respectively, which window 121, 141 preferably is transmissive in the infrared spectrum. The window 121, 141 is integrated in the encapsulation 12 and 14 respectively and preferably faces the configuration 3.

Claims

1. Infrared device, comprising a substrate (1), and supported by the substrate (1):

- a configuration (3) for one of absorbing and emitting infrared radiation, the configuration (3) comprising an electrically conducting layer arrangement (31) of a thickness of 50 nm or less arranged between dielectric layers (34,35),
- one or more of a thermal sensor (5) arranged for sensing the infrared radiation absorbed by the configuration (3), and a heater (7) arranged for heating the configuration (3) to emit the infrared radiation.

2. The infrared device of claim 1, comprising a recess (11) in the substrate (1), a membrane (21) spanning at least a portion of the recess (11), wherein the configuration (3) is arranged on or in the membrane (21), or wherein the membrane (21) represents the configuration (3), and wherein the thermal sensor (5) if available and / or the heater (7) if available is arranged on or in the

membrane (21).

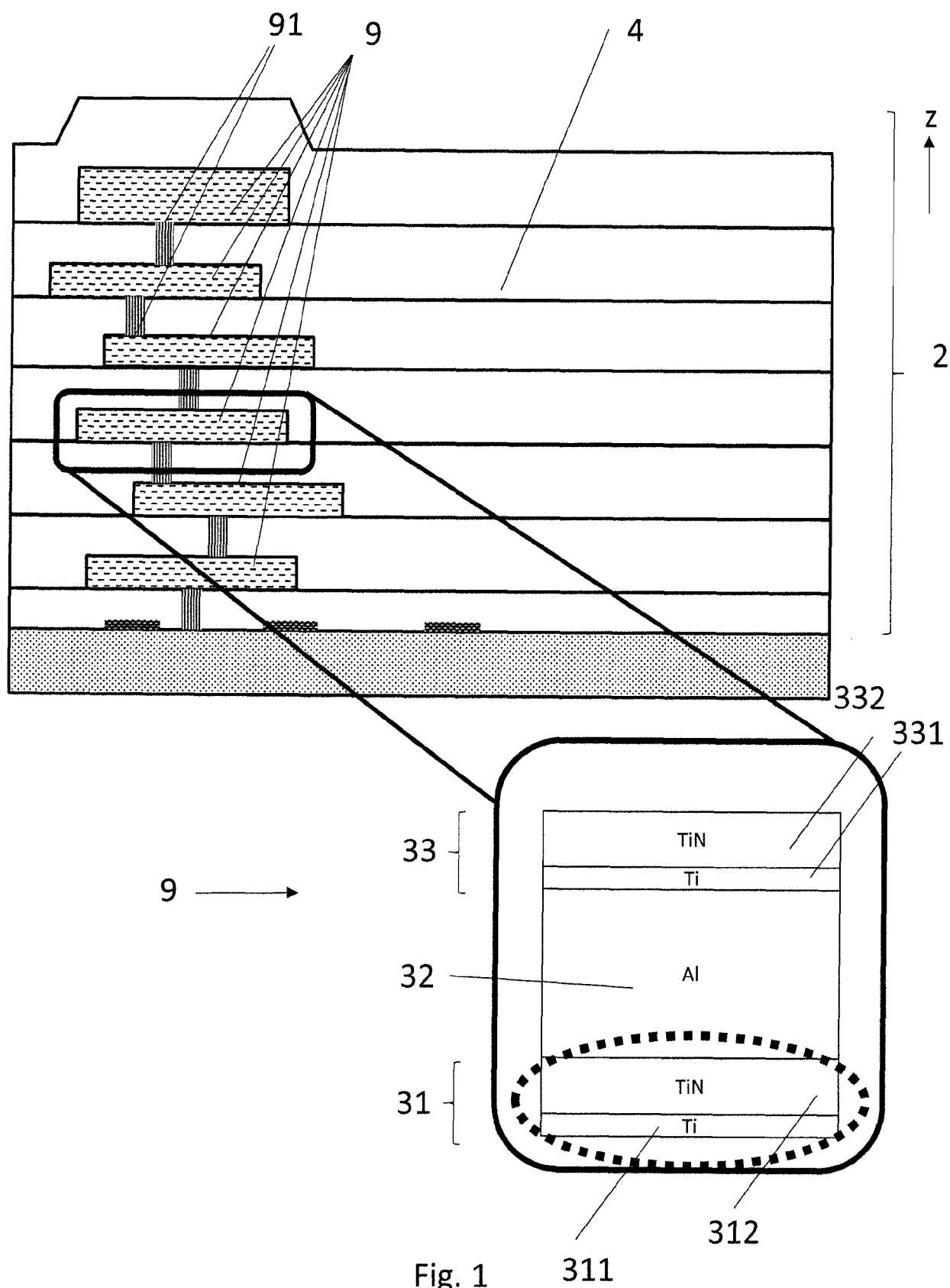
3. The infrared device of claim 1 or claim 2, wherein the electrically conducting layer arrangement (31) is a layer arrangement available in a CMOS layer stack (2) arranged on the substrate (1), wherein, in a vertical direction towards the substrate (1), the dielectric layer (34) underneath the electrically conducting layer arrangement (31) is an inter metal dielectric (4) of the CMOS layer stack (2), and wherein the electrically conducting layer arrangement (31) is one or more of an adhesion layer for adhering the inter metal dielectric (4) to a metal layer (32) of the CMOS layer stack (2) previously removed, and a diffusion barrier for preventing diffusion between the inter metal dielectric (4) and a metal layer (32) previously removed.
4. The infrared device of any of the preceding claims, wherein the electrically conducting layer arrangement (31) comprises or consists of an interstitial compound comprising one of the metals of group VI to VIII.
5. The infrared device of any of the preceding claims, wherein the electrically conducting layer arrangement (31) comprises or consists of a Ti layer and a TiN layer.
6. The infrared device of any of the preceding claims 1 to 4, wherein the electrically conducting layer arrangement (31) comprises or consists of a Ta layer and a TaN layer.
7. The infrared device of any of the preceding claims 1 to 4, wherein the electrically conducting layer arrangement (31) comprises or consists a layer of one of Al, Cu, Pt, W.
8. The infrared device of any of the preceding claims, wherein, in a vertical direction away from the substrate (1), the dielectric layer (35) on top of the electrically conducting layer arrangement (31) comprises or consists of a passivation layer (351), and in particular wherein the passivation layer (351) is a SiN layer.
9. The infrared device of claim 8, wherein the dielectric layer (35) on top of the electrically conducting layer arrangement (31) comprises a dielectric tuning layer (352) between the passivation layer (351) and the electrically conducting layer (31), for tuning a thickness of the configuration (3).
10. The infrared device of any of the preceding claims, wherein the configuration (3) comprises an electri-

cally conducting layer stack (36, 37, 38) arranged between dielectric layers (30, 34), wherein the electrically conducting layer stack (36, 37, 38) has a thickness of more than 100 nm, wherein the electrically conducting layer stack (36, 37, 38) is arranged between the electrically conducting layer arrangement (31) and a bottom layer (30) of the configuration (3), and in particular wherein the electrically conducting layer stack (36, 37, 38) comprises or consists of a metal layer (38) arranged between two further electrically conducting layer arrangements (36, 37).

11. The infrared device of claim 10, wherein the configuration (3) comprises an electrically conducting layer (39) arranged between dielectric layers (30, 301) and of a material different than a material of the metal layer (38) of the electrically conducting layer stack (36, 37, 38), wherein the metal layer (38) of the electrically conducting layer stack (36, 37, 38) and the electrically conducting layer (39) are electrically connected to form one or more thermocouples serving as thermal sensor (5), in particular wherein the metal layer (38) is made from Al and the electrically conducting layer (29) is made from polysilicon.
12. Method for manufacturing an infrared device, comprising providing a wafer including a substrate (1) and a CMOS layer stack (2) arranged on the substrate (1), which CMOS layer stack (2) includes at least one metal layer (32) sandwiched between two electrically conducting layer arrangements (31, 33) of less than 50 nm thickness each serving as one or more of an adhesion layer and a diffusion barrier between the metal layer (32) and inter metal dielectrics (4) next to each of the electrically conducting layer arrangements (31, 33), removing the inter metal dielectric (4) arranged on top of an upper (33) of the electrically conducting layer arrangements (31, 33) as well as the upper electrically conducting layer arrangement (33), removing the metal layer (32), and depositing a dielectric layer (35) on the lower (31) of the electrically conducting layer arrangements (31, 33) released by the removal of the metal layer (32).
13. Method of claim 12, wherein the top inter metal dielectric (4) and the upper electrically conducting layer arrangement (33) are removed in a common etching step, and wherein the metal layer (32) is removed in a separate etching step.
14. Method of claim 12 or claim 13, comprising etching a recess (11) in the substrate (1) for gener-

ating a membrane (21) including the configuration (3) including the electrically conducting layer arrangement (31) serving for one of absorbing and emitting infrared radiation.

15. Method of any one of the preceding claims 12 to 14, comprising providing the wafer including one or more of a thermal sensor (5) arranged for sensing the infrared radiation absorbed by the configuration (3), and a heater (7) arranged for heating the configuration (3) to emit the infrared radiation.



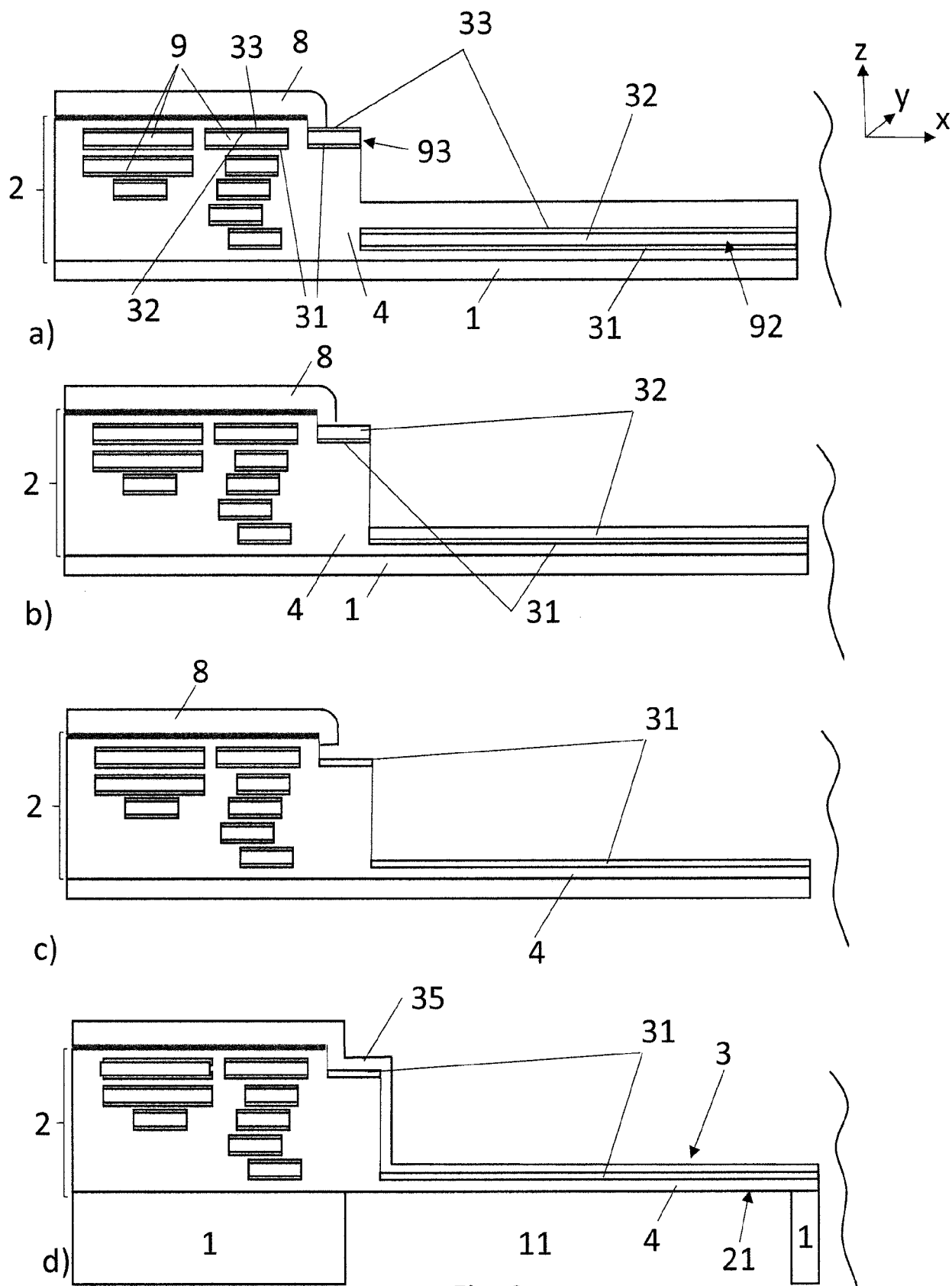


Fig. 2

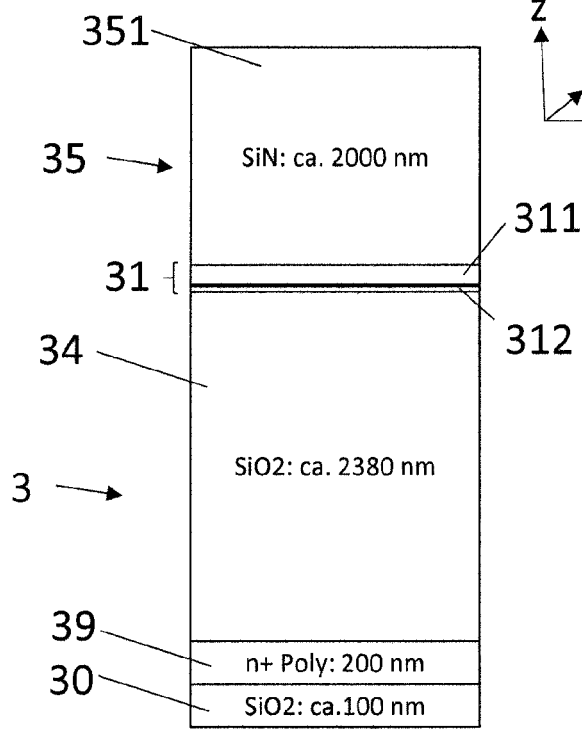


Fig. 3

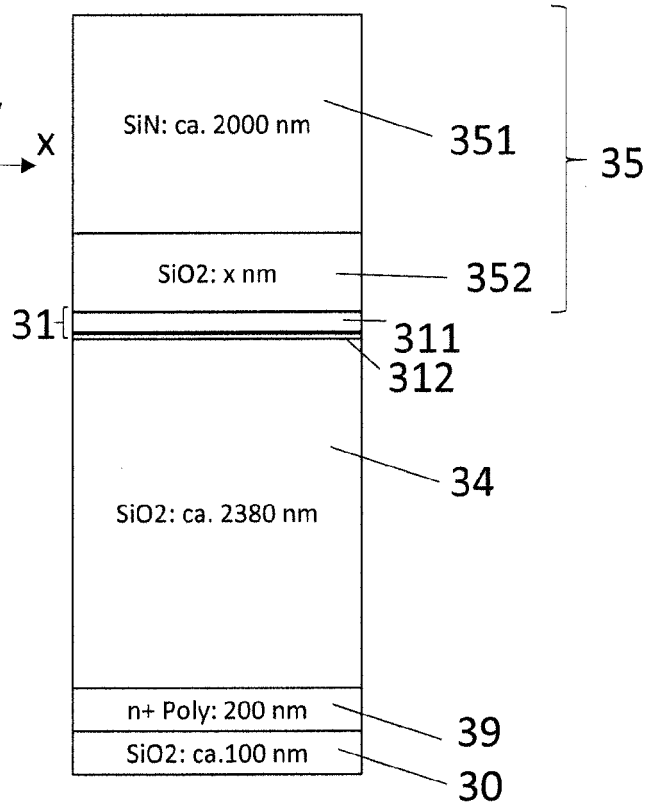


Fig. 4

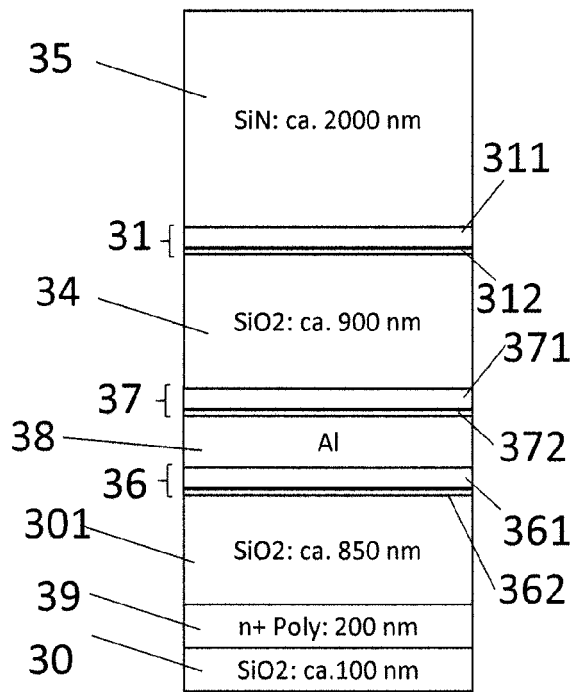


Fig. 5

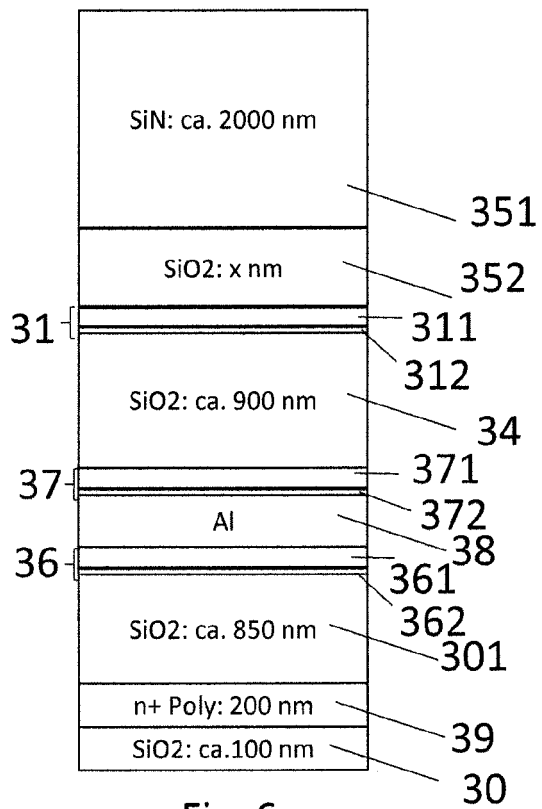
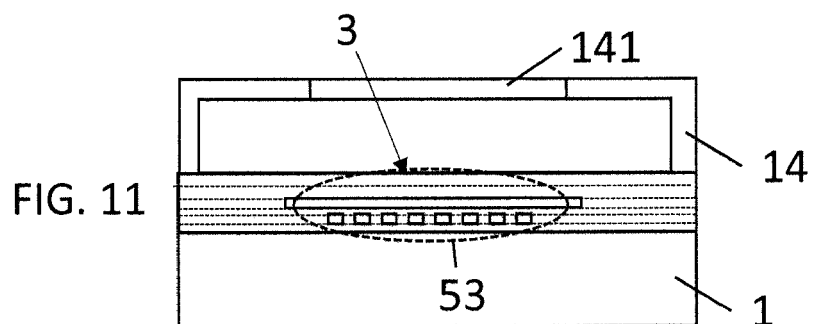
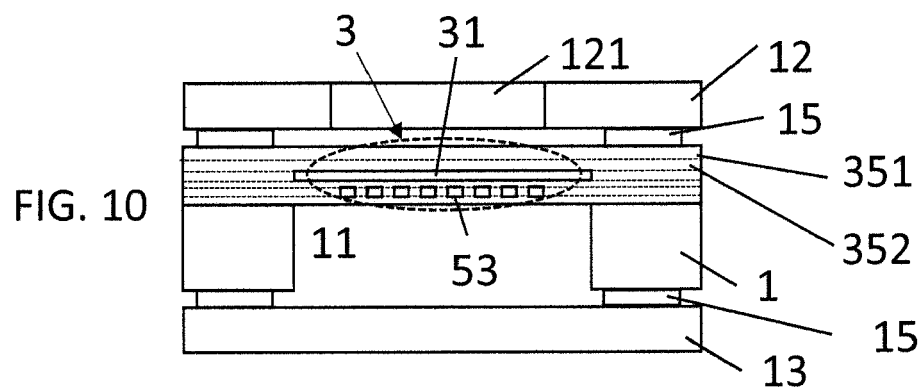
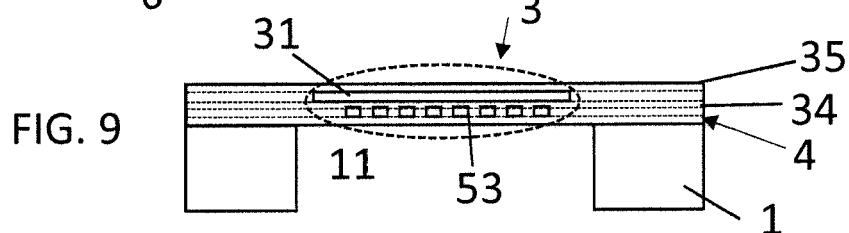
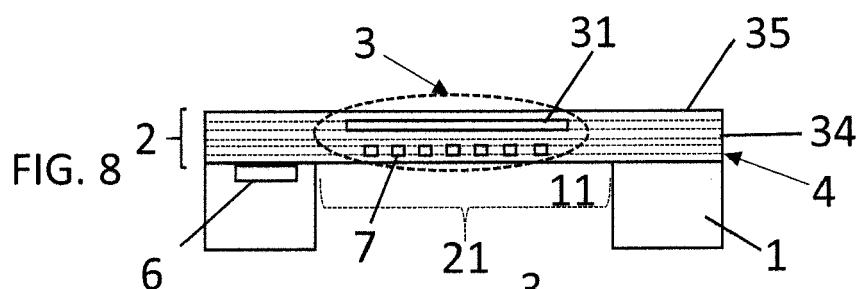
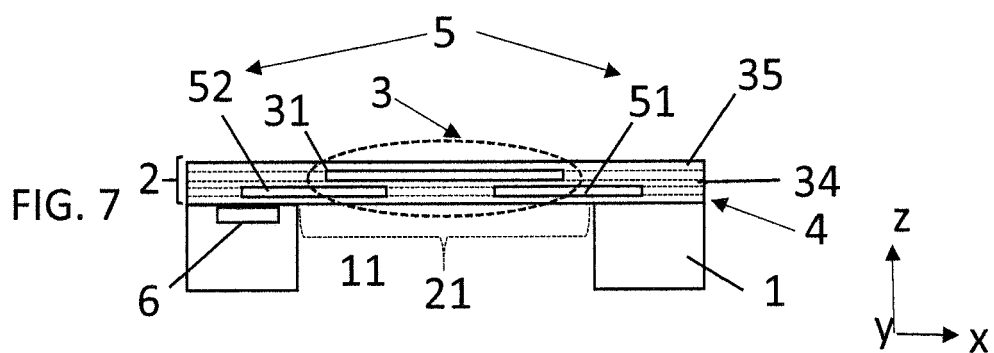


Fig. 6





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