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(54) SEMICONDUCTOR PACKAGING STRUCTURE AND MANUFACTURING METHOD THEREFOR

(57) Embodiments of the present invention provide a semiconductor package structure. The structure includes: a semiconductor component; a connection pad, disposed on the semiconductor component; a protective layer, including a first non-conductive material, a first part, and a second part, where the first part covers the semiconductor component except the connection pad, a surface of the first part is at a first height, the second part covers a periphery of the connection pad, a surface of the second part is at a second height, the first height is less than the second height, a middle part of the connection pad is exposed, and the first part and the second part are connected at an edge of the connection pad; a flat layer, including a second non-conductive material and covering the first part, where a surface of the flat layer is at the second height; an under bump metallization layer, including a first metallic material and covering the flat layer, the second part, and the middle part; and a rewiring layer, including a second metallic material and covering the under bump metallization layer.

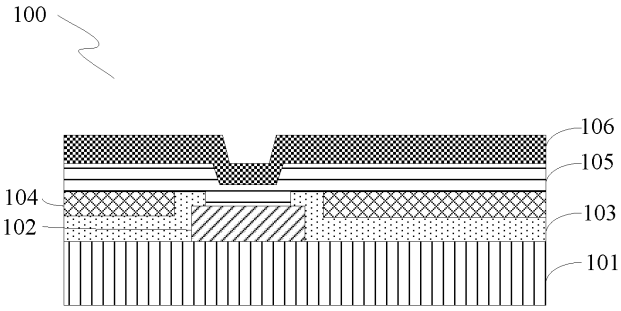

FIG. 1

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Description

TECHNICAL FIELD

[0001] The present invention relates to the semiconductor field, and in particular, to a semiconductor package structure and a semiconductor package structure fabricating method.

BACKGROUND

[0002] In semiconductor chip fabricating technologies, wafer level packaging means that all or most packaging test procedures are directly performed on a wafer before a wafer component is cut to fabricate individual components. Compared with a conventional procedure in which a wafer is first cut and then a packaging test is performed on an individual bare die obtained after the cutting, the wafer level packaging does not need any intermediate layer, filler, or lead frame and omits fabricating processes such as die bonding and wire bonding, so that material and labor costs can be greatly reduced. In addition, in the wafer level packaging, redistribution and bumping technologies are usually used as a wire-winding means for input/output (Input/Output, I/O) ports. Therefore, the wafer level packaging has advantages of a smaller package size and better electrical performance. However, in a wafer level packaging technology, a conducting wire is prone to break off, and a yield rate and reliability of a fabricated chip need to be improved.

SUMMARY

[0003] Embodiments of the present invention provide a semiconductor package structure and a semiconductor package structure fabricating method. The semiconductor package structure has a higher yield rate and better reliability, and signals transmitted by using the semiconductor package structure are also more consistent.

[0004] According to a first aspect, an embodiment of the present invention provides a semiconductor package structure, including: a semiconductor component; a connection pad, disposed on the semiconductor component; a protective layer, including a first non-conductive material, a first part, and a second part, where the first part covers the semiconductor component except the connection pad, a surface of the first part is at a first height, the second part covers a periphery of the connection pad, a surface of the second part is at a second height, the first height is less than the second height, a middle part of the connection pad is exposed, the middle part includes a part on the connection pad except the periphery, and the first part and the second part are connected at an edge of the connection pad; a flat layer, including a second non-conductive material and covering the first part, where a surface of the flat layer is at the second height; an under bump metallization layer, including a first metallic material and covering the flat layer, the second part, and the middle part; and a rewiring layer, including a second metallic material and covering the under bump metallization layer.

[0005] The surface of the flat layer is flush with the surface of the second part. The flat layer makes up a height difference between the first part and the second part of the protective layer, so that the under bump metallization layer can cover a smoother surface, and a risk that the under bump metallization layer and the rewiring layer covering the under bump metallization layer distort, fracture, and peel off at an unsmooth part is reduced.

[0006] In a first possible implementation of the first aspect, the second non-conductive material includes silicon oxide. Compared with an organic material such as polyimide (Polyimide), using the silicon oxide to fabricate the flat layer can lead to higher smoothness precision, so as to further reduce a risk that the under bump metallization layer and the rewiring layer covering the under bump metallization layer distort, fracture, and peel off. This helps improve a yield rate and reliability of a plurality of rewiring layers. In addition, the rewiring layer becomes more even because of improvement in flatness, and signals transmitted by using the rewiring layer are also more consistent.

[0007] With reference to the first aspect or the first possible implementation of the first aspect, in a second possible implementation, the silicon oxide includes silicon dioxide.

[0008] With reference to any one of the first aspect, or the first and the second possible implementations of the first aspect, in a third possible implementation, the first non-conductive material includes silicon nitride.

[0009] With reference to any one of the first aspect, or the first to the third possible implementations of the first aspect, in a fourth possible implementation, the first metallic material includes at least one of copper, nickel, silver, or tin.

[0010] With reference to any one of the first aspect, or the first to the fourth possible implementations of the first aspect, in a fifth possible implementation, the second metallic material includes at least one of copper or aluminum.

[0011] According to a second aspect, an embodiment of the present invention provides a semiconductor package structure fabricating method, including: fabricating a semiconductor component; disposing a connection pad on the semiconductor component; fabricating a protective layer by using a first non-conductive material, where the protective layer includes a first part and a second part, and the fabricating a protective layer includes: covering the semiconductor component except the connection pad with the first part, so that a surface of the first part is at a first height; covering a periphery of the connection pad with the second part, so that a surface of the second part is at a second height, where the first height is less than the second height; and exposing a middle part of the connection pad, where the middle part includes a part on the connection pad except the periphery, and

the first part and the second part are connected at an edge of the connection pad; fabricating a flat layer by using a second non-conductive material, where the fabricating a flat layer includes: covering the first part with the flat layer, so that a surface of the flat layer is at the second height; fabricating an under bump metallization layer by using a first metallic material, and covering the flat layer, the second part, and the middle part with the under bump metallization layer; and fabricating a rewiring layer by using a second metallic material, and covering the under bump metallization layer with the rewiring layer.

[0012] The flat layer makes up a height difference between the first part and the second part of the protective layer, so that the under bump metallization layer can cover a smoother surface, and a risk that the under bump metallization layer and the rewiring layer covering the under bump metallization layer distort, fracture, and peel off at an unsmooth part is reduced.

[0013] In a first possible implementation of the second aspect, the covering the first part with the flat layer, so that a surface of the flat layer is at the second height includes: covering the protective layer and the middle part with a second conductive material by using a chemical vapor deposition (CVD) process; polishing the second conductive material to the second height by using a chemical mechanical polishing (CMP) process; and removing, by using a photo lithography process and an etching process, the second conductive material covering the middle part.

[0014] With reference to the second aspect, or the first possible implementation of the second aspect, in a second possible implementation, the second non-conductive material includes silicon oxide. Compared with an organic material such as polyimide (Polyimide), using the silicon oxide to fabricate the flat layer can lead to higher smoothness precision, so as to further reduce a risk that the under bump metallization layer and the rewiring layer covering the under bump metallization layer distort, fracture, and peel off. This helps improve a yield rate and reliability of a plurality of rewiring layers. In addition, the rewiring layer becomes more even because of improvement in flatness, and signals transmitted by using the rewiring layer are also more consistent.

[0015] With reference to any one of the second aspect, or the first and the second possible implementations of the second aspect, in a third possible implementation, the silicon oxide includes silicon dioxide.

[0016] With reference to any one of the second aspect, or the first to the third possible implementations of the second aspect, in a fourth possible implementation, the first non-conductive material includes silicon nitride.

[0017] With reference to any one of the second aspect, or the first to the fourth possible implementations of the second aspect, in a fifth possible implementation, the first metallic material includes at least one of copper, nickel, silver, or tin.

[0018] With reference to any one of the second aspect, or the first to the fifth possible implementations of the second aspect, in a sixth possible implementation, the second metallic material includes at least one of copper or aluminum.

BRIEF DESCRIPTION OF DRAWINGS

[0019] To describe the technical solutions in embodiments of the present invention or in the prior art more clearly, the following briefly describes the accompanying drawings required for describing the embodiments or the prior art. Apparently, the accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

FIG. 1 is a sectional schematic diagram of a package structure according to a first embodiment of the present invention;

FIG. 2 is a sectional schematic diagram of a semiconductor component, a connection pad, and a protective layer that are in FIG. 1;

FIG. 3 is a flowchart of a package structure fabricating method according to a second embodiment of the present invention;

FIG. 4 is a sectional schematic diagram of a structure in a fabricating process in FIG. 3;

FIG. 5 is another sectional schematic diagram of a structure in a fabricating process in FIG. 3; and

FIG. 6 is still another sectional schematic diagram of a structure in a fabricating process in FIG. 3.

DESCRIPTION OF EMBODIMENTS

[0020] The following clearly and completely describes the technical solutions in embodiments of the present invention with reference to the accompanying drawings in the embodiments of the present invention. Apparently, the described embodiments are merely some but not all of the embodiments of the present invention. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

[0021] FIG. 1 is a sectional schematic diagram of a package structure 100 according to a first embodiment of the present invention. The package structure 100 includes a semiconductor component 101, a connection pad 102, a protective layer 103, a flat layer 104, an under bump metallization layer 105, and a rewiring layer 106.

[0022] In an embodiment, the semiconductor component 101 includes a wafer (Wafer). The connection pad 102 is disposed on the semiconductor component 101. The protective layer 103 includes a first non-conductive material. As shown by 200 in FIG. 2, the protective layer 103 includes a first part 1031 and a second part 1032. The first part 1031 covers the semiconductor component 101. A surface of the first part 1031 is at a first height.

The second part 1032 covers a periphery of the connection pad 102 and is configured to ensure that the protective layer 103 covers all parts of the semiconductor component 101 except an area on which the connection pad is disposed. In an embodiment, from a top view, a surface of the connection pad is in a circular shape. The periphery is an outermost ring of the circular shape. In a process of fabricating a 28-nm semiconductor, a diameter of the connection pad is about 100 um, an outer diameter of the ring is the same as the diameter of the connection pad, and an inner diameter of the ring is about 80 um. A surface of the second part 1032 is at a second height. The first height is less than the second height. A middle part of the connection pad 102 is exposed. The middle part includes a part on the connection pad 102 except the periphery. In the process of fabricating a 28-nm semiconductor, from a top view, a diameter of the middle part is the same as the inner diameter of the ring. The first part 1031 and the second part 1032 are connected at an edge 1033 of the connection pad 102. In an embodiment, the first non-conductive material includes silicon nitride.

[0023] The flat layer 104 includes a second non-conductive material and covers the first part 1031. A surface of the flat layer 104 is at the second height, so that the surface of the flat layer 104 is flush with the surface of the second part 1032. The flat layer 104 makes up a height difference between the first part 1031 and the second part 1032 of the protective layer 103, so that the under bump metallization layer 105 can cover a smoother surface, and a risk that the under bump metallization layer 105 and the rewiring layer 106 covering the under bump metallization layer 105 distort, fracture, and peel off at an unsmooth part is reduced. In an embodiment, the second non-conductive material includes silicon oxide. For example, the silicon oxide is silicon dioxide. Compared with an organic material such as polyimide (Polyimide), using the silicon oxide to fabricate the flat layer 104 can lead to higher smoothness precision, so as to further reduce a risk that the under bump metallization layer 105 and the rewiring layer 106 covering the under bump metallization layer 105 distort, fracture, and peel off. This helps improve a yield rate and reliability of a plurality of rewiring layers. In addition, the rewiring layer 106 becomes more even because of improvement in flatness, and signals transmitted by using the rewiring layer 106 are also more consistent.

[0024] The under bump metallization layer 105 includes a first metallic material and covers the flat layer 104, the second part 1032, and the middle part of the connection pad 102. The first metallic material includes at least one of copper, nickel, silver, or tin. The rewiring layer 106 includes a second metallic material and covers the under bump metallization layer 105. In an embodiment, the second metallic material includes at least one of copper or aluminum.

[0025] The connection pad 102 is configured to connect to the rewiring layer 106 by using the under bump metallization layer 105, and the rewiring layer 106 is connected to an electrical conducting wire, so that the connection pad 102 is electrically connected to another electrical component. The under bump metallization layer 105 is configured to keep a value of resistance generated between the connection pad 102 and the rewiring layer 106 steady in different conditions (such as different voltage conditions).

[0026] In an embodiment, the package structure 100 includes a plurality of structures shown in FIG. 1. A plurality of semiconductor components 101, protective layers 103, flat layers 104, under bump metallization layers 105, and rewiring layers 106 in the structures shown in FIG. 1 are separately connected together. For example, the package structure 100 includes a structure A and a structure B that are shown in FIG. 1. The semiconductor component 101 in the structure A and the semiconductor component 101 in the structure B are connected together, the protective layer 103 in the structure A and the protective layer 103 in the structure B are connected together, and so on.

[0027] FIG. 3 is a flowchart 300 of a package structure fabricating method according to a second embodiment of the present invention. As shown in the figure, in step 302, a semiconductor component 101 is fabricated. In an embodiment, the semiconductor component 101 includes a wafer (Wafer). In step 304, a connection pad 102 is disposed on the semiconductor component. In step 306, a protective layer is fabricated by using a first non-conductive material. The protective layer includes a first part 1031 and a second part 1032. The semiconductor component 101 is covered with the first part 1031, so that a surface of the first part 1031 is at a first height. A periphery of the connection pad is covered with a second part 1302, so that a surface of the second part 1032 is at a second height. The first height is less than the second height, so that a middle part of the connection pad 102 is exposed. The middle part includes a part on the connection pad 102 except the periphery. The first part 1031 and the second part 1032 are connected at an edge 1033 of the connection pad 102. In an embodiment, the first non-conductive material includes silicon nitride.

[0028] In step 308, a flat layer 104 is fabricated by using a second non-conductive material. Specifically, the first part 1031 is covered with the flat layer 104, so that a surface of the flat layer 104 is at the second height. The flat layer 104 makes up a height difference between the first part 1031 and the second part 1032 of the protective layer, so that an under bump metallization layer 105 in a subsequent process can cover a smoother surface, and a risk that the under bump metallization layer 105 and a rewiring layer 106 covering the under bump metallization layer 105 distort, fracture, and peel off at an unsmooth part is reduced.

[0029] In an embodiment, that the first part 1031 is covered with the flat layer 104, so that a surface of the flat layer 104 is at the second height includes: as shown in FIG. 4, the protective layer 103 and the middle part of the connection pad 102 are covered with a second con-

ductive material by using a chemical vapor deposition (CVD) process; as shown in FIG. 5, the second conductive material is polished to the second height by using a chemical mechanical polishing (CMP) process; and as shown in FIG. 6, the second conductive material covering the middle part of the connection pad 102 is removed by using a photo lithography process and an etching process. In an embodiment, the second non-conductive material includes silicon oxide. For example, the silicon oxide includes silicon dioxide. Compared with an organic material such as polyimide (Polyimide), using the silicon oxide to fabricate the flat layer can lead to higher smoothness precision, so as to further reduce a risk that the under bump metallization layer 105 and the rewiring layer 106 covering the under bump metallization layer 105 distort, fracture, and peel off. This helps improve a yield rate and reliability of a plurality of rewiring layers. In addition, the rewiring layer 106 becomes more even because of improvement in flatness, and signals transmitted by using the rewiring layer 106 are also more consistent.

[0030] In step 310, the under bump metallization layer 105 is fabricated by using a first metallic material, so that the flat layer 104, the second part 1032, and the middle part of the connection pad 102 are covered with the under bump metallization layer 105. In an embodiment, the first metallic material includes at least one of copper, nickel, silver, or tin. In step 312, the rewiring layer 106 is fabricated by using a second metallic material, so that the under bump metallization layer 105 is covered with the rewiring layer 106. The second metallic material includes at least one of copper or aluminum.

[0031] What is disclosed above is merely examples of the embodiments of the present invention, and certainly is not intended to limit the protection scope of the present invention. Therefore, equivalent variations made in accordance with the claims of the present invention shall fall within the scope of the present invention.

Claims

1. A semiconductor package structure, comprising:

a semiconductor component;
a connection pad, disposed on the semiconductor component;
a protective layer, comprising a first non-conductive material, a first part, and a second part, wherein the first part covers the semiconductor component except the connection pad, a surface of the first part is at a first height, the second part covers a periphery of the connection pad, a surface of the second part is at a second height, the first height is less than the second height, a middle part of the connection pad is exposed, the middle part comprises a part on the connection pad except the periphery, and the first part and the second part are connected at an edge of the connection pad;
a flat layer, comprising a second non-conductive material and covering the first part, wherein a surface of the flat layer is at the second height;
an under bump metallization layer, comprising a first metallic material and covering the flat layer, the second part, and the middle part; and
a rewiring layer, comprising a second metallic material and covering the under bump metallization layer.

2. The package structure according to claim 1, wherein the second non-conductive material comprises silicon oxide.

3. The package structure according to claim 1 or 2, wherein the silicon oxide comprises silicon dioxide.

4. The package structure according to any one of claims 1 to 3, wherein the first non-conductive material comprises silicon nitride.

5. The package structure according to any one of claims 1 to 4, wherein the first metallic material comprises at least one of copper, nickel, silver, or tin.

6. The package structure according to any one of claims 1 to 5, wherein the second metallic material comprises at least one of copper or aluminum.

7. A semiconductor package structure fabricating method, comprising:

Fabricating a semiconductor component;
Disposing a connection pad on the semiconductor component;
Fabricating a protective layer by using a first non-conductive material, wherein the protective layer comprises a first part and a second part, and the fabricating a protective layer comprises: covering the semiconductor component except the connection pad with the first part, so that a surface of the first part is at a first height; covering a periphery of the connection pad with the second part, so that a surface of the second part is at a second height, wherein the first height is less than the second height; and exposing a middle part of the connection pad, wherein the middle part comprises a part on the connection pad except the periphery, and the first part and the second part are connected at an edge of the connection pad;
Fabricating a flat layer by using a second non-conductive material, wherein the fabricating a flat layer comprises: covering the first part with the flat layer, so that a surface of the flat layer is at the second height;
fabricating an under bump metallization layer by

using a first metallic material, and covering the flat layer, the second part, and the middle part with the under bump metallization layer; and
fabricating a rewiring layer by using a second metallic material, and covering the under bump metallization layer with the rewiring layer.

8. The method according to claim 7, wherein the covering the first part with the flat layer, so that a surface of the flat layer is at the second height comprises:

covering the protective layer and the middle part with a second conductive material by using a chemical vapor deposition (CVD) process;
polishing the second conductive material to the second height by using a chemical mechanical polishing (CMP) process; and
removing, by using a photo lithography process and an etching process, the second conductive material covering the middle part.

9. The method according to claim 7 or 8, wherein the second non-conductive material comprises silicon oxide.

10. The method according to any one of claims 7 to 9, wherein the silicon oxide comprises silicon dioxide.

11. The method according to any one of claims 7 to 10, wherein the first non-conductive material comprises silicon nitride.

12. The package structure according to any one of claims 7 to 11, wherein the first metallic material comprises at least one of copper, nickel, silver, or tin.

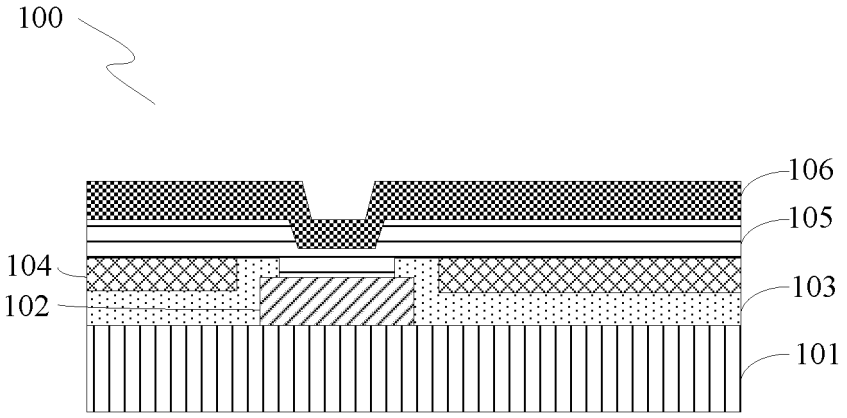
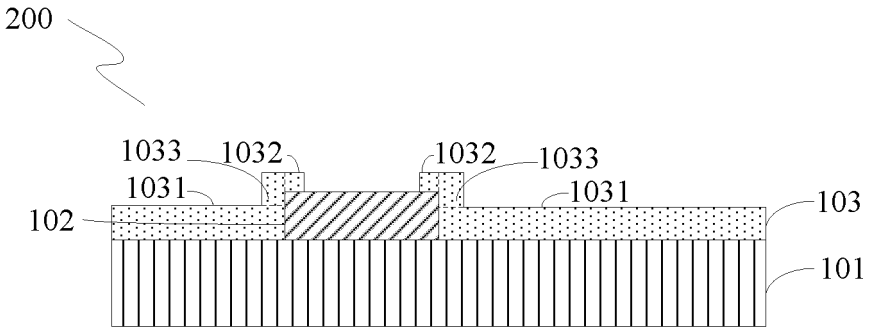

100
106
105
104
103
102
101

FIG. 1


200
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1031
103
102
101

FIG. 2

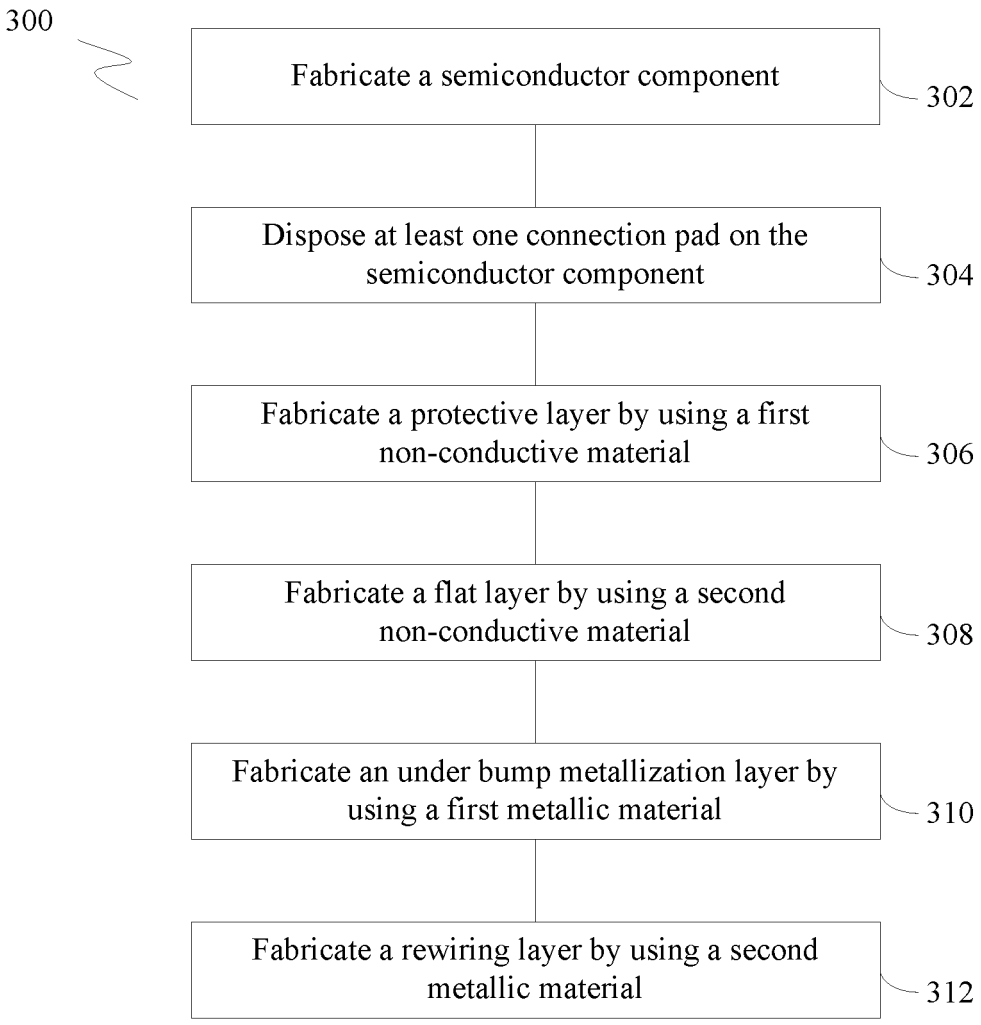
300
Fabricate a semiconductor component
302
Dispose at least one connection pad on the semiconductor component
304
Fabricate a protective layer by using a first non-conductive material
306
Fabricate a flat layer by using a second non-conductive material
308
Fabricate an under bump metallization layer by using a first metallic material
310
Fabricate a rewiring layer by using a second metallic material
312

FIG. 3

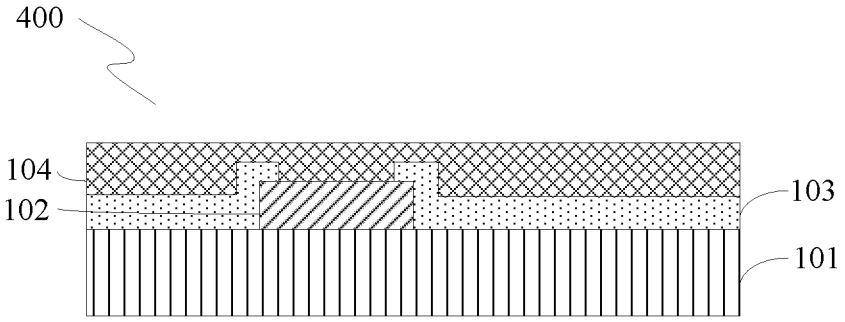

FIG. 4

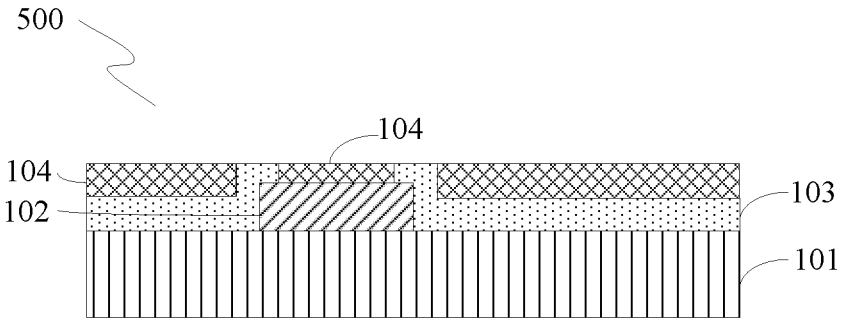

FIG. 5

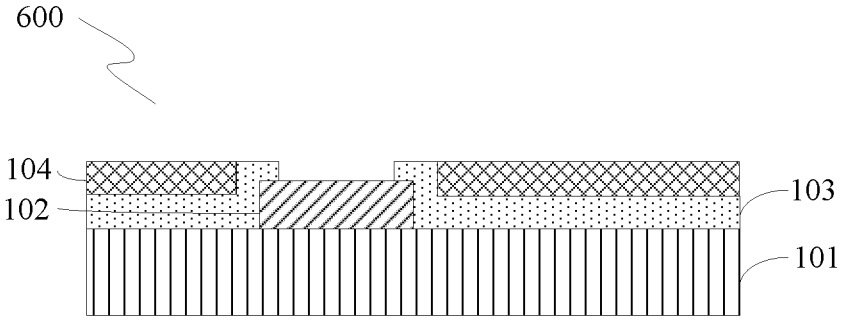

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/098290

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/29 (2006.01) i; H01L 23/31 (2006.01) i; H01L 21/56 (2006.01) i
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI, CNTXT, CNABS: 封装, 晶圆, 焊盘, 焊垫, 接垫, 平坦, 保护, 凸点下金属, 重分布, 重布线, packag+, wafer, pad, flat, planar+, protect+, UBM, bump, RDL, rewir+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 106206472 A (HUAWEI TECHNOLOGIES CO., LTD.) 07 December 2016 (07.12.2016), claims 1-12	1-12
Y	US 2009/0236741 A1 (HUANG et al.) 24 September 2009 (24.09.2009), description, paragraphs [0006]-[0009], and figures 1A-1G	1-12
Y	US 8035226 B1 (WILCOXEN et al.) 11 October 2011 (11.10.2011), description, column 6, line 25 to column 7, line 18, and figure 4	1-12
A	CN 103187394 A (TAIWAN SEMICONDUCTOR MFG CO., LTD.) 03 July 2013 (03.07.2013), entire document	1-12
A	US 2013/0140691 A1 (BAO et al.) 06 June 2013 (06.06.2013), entire document	1-12

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 October 2017	10 November 2017

Name and mailing address of the ISA	Authorized officer
State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No. (86-10) 62019451	ZHAO, Duan Telephone No. (86-10) 62411328

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/098290

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
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US 20090236741 A1	24 September 2009	TW 200941666 A	01 October 2009
US 8035226 B1	11 October 2011	None	
CN 103187394 A	03 July 2013	US 2014073091 A1	13 March 2014
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		US 8963326 B2	24 February 2015

Form PCT/ISA /210 (patent family annex) (July 2009)