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(54) **IMAGE INTENSIFIER WITH STRAY PARTICLE SHIELD**

(57) A light intensifier includes a semiconductor structure to multiply electrons and block stray particles (e.g., photons and/or ions). The semiconductor structure includes an electron multiplier region that is doped to generate a plurality of electrons for each electron that impinges a reception surface of the semiconductor structure, blocking regions that are doped to direct the plurality of electrons towards emissions areas of an emission surface of the semiconductor structure, and shielding regions that are doped to absorb stray particles that impinge the emission surface of the semiconductor structure.

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Description

BACKGROUND

[0001] Image intensifiers are used in low light (e.g., night vision) applications to amplify ambient light into a more visible image.

[0002] An image intensifier may be degraded by internal stray light or ion feedback, which may originate from an anode device such as a phosphor screen or other sensor device.

SUMMARY

[0003] A light intensifier includes a semiconductor structure to multiply electrons and block stray photons or ions (collectively referred to herein as "stray particles"). The semiconductor structure includes an electron multiplier region that is doped to generate a plurality of electrons for each electron that impinges a reception surface of the semiconductor structure, blocking regions that are doped to direct the plurality of electrons towards emissions areas of an emission surface of the semiconductor structure, and shielding regions that are doped to absorb stray particles that impinge the emission surface of the semiconductor structure and stop emission of the resulting electrons.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004]

FIG. 1 is a cross-sectional view of an image-intensifier that includes a semiconductor structure configured as an electron multiplier and shield to absorb stray particles.

FIG. 2 is cross-sectional view of another semiconductor structure configured as an electron multiplier and shield, which may represent an example embodiment of the semiconductor structure of FIG. 1.

FIG. 3 is 3-dimensional cross-sectional perspective view of an example embodiment of the semiconductor structure of FIG. 2, in which the semiconductor structure includes multiple rows of parallel and perpendicular blocking structures to form an array of emission areas.

FIG. 4 is a 2-dimensional view an example embodiment of the semiconductor structure of FIG. 2 directed toward an emission surface of the semiconductor structure, in which shields are omitted for illustrative purposes.

FIG. 5 is another view of the example embodiment of FIG. 4, in which shields are illustrated.

FIG. 6 depicts an expanded view of an electron bombarded cell of an electron multiplier of FIG. 4.

FIG. 7 is a flowchart of a method of intensifying an image and limiting effects of stray particles.

DETAILED DESCRIPTION

[0005] Disclosed herein are techniques to limiting effects of stray particles in semiconductor-based gain layer of an image intensifier.

[0006] FIG. 1 is a cross-sectional view of an image-intensifier 100. Image-intensifier 100 may be configured as a night vision apparatus. Image-intensifier 100 is not, however, limited to a night vision apparatus.

[0007] Image intensifier 100 includes a photo-cathode 102 to convert photons 104 to electrons 106. Each photon 104 that impinges an input surface 102a has a probability to create a free electron 106. Free electrons 106 are emitted from an output surface 102b. Output surface 102b may be activated to a negative electron affinity state to facilitate the flow of electrons 106 from output surface 102b.

[0008] Photo-cathode 102 may be fabricated from a semiconductor material that exhibits a photo emissive effect, such as gallium arsenide (GaAs), GaP, GaInAsP, InAsP, InGaAs, and/or other semiconductor material. Alternatively, photo-cathode 102 may be a known Bi-alkali.

[0009] In an embodiment, a photo-emissive semiconductor material of photo-cathode 102 absorbs photons, which increases a carrier density of the semiconductor material, which causes the semiconductor material to generate a photo-current of electrons 106, which are emitted from output surface 102b.

[0010] Image intensifier 100 further includes a semiconductor structure 110 configured as an electron multiplier and shield to generate a plurality of free electrons 112 for each electron 106 that impinges a surface 110a of semi-conductor structure 110, and to absorb stray particles 114.

[0011] Semiconductor structure 110 may also be referred to herein as an electron multiplier, an electron amplifier, and/or an electron bombarded device (EBD). Semiconductor structure 110 may be configured to generate, for example and without limitation, several hundred free electrons 112 for each free electron 106 that impinges surface 110a.

[0012] Image intensifier 100 further includes an anode 118 to receive electrons 112 from semiconductor structure 110. Anode 118 may include a sensor to sense electrons 112 that impinge a surface 118a of anode 118. Anode 118 may include a phosphor screen to convert electrons 112 to photons. Anode 118 may include an integrated circuit having a CMOS substrate and a plurality of collection wells. In this example, electrons collected in the collection wells may be processed with a signal processor to produce an image, which may be provided to a resistive anode and/or an image display device.

[0013] Image intensifier 100 further includes a vacuum region 108 to facilitate electrons flow between photo cathode 102 and semiconductor structure 110.

[0014] Image intensifier 100 further includes a vacuum region 116 to facilitate electron flow between semiconductor structure 110 and anode 118.

[0015] Image intensifier 100 and/or portions thereof, may be configured as described in one or more examples below. Image intensifier 100 is not, however, limited to the examples below.

[0016] Image intensifier 100 further includes a bias circuit 150. In the example of FIG. 1, bias circuit 150 is configured to apply a first bias voltage between photo-cathode 106 and semiconductor structure 110, a second bias voltage between input surface 110a and an output surface 110b of semiconductor structure 110, and a third bias voltage between semiconductor structure 110 and anode 118 (e.g., to draw electrons 112 through semiconductor structure 110 towards a surface 118a of anode 118.

[0017] A peripheral surface of photo-cathode 102 may be coated with a conductive material, such as chrome, to provide an electrical contact to photo-cathode 102.

[0018] A peripheral surface of semiconductor structure 110 may be coated with a conducting material, such as chrome, to provide an electrical contact to one or more surfaces of semiconductor structure 110.

[0019] A peripheral surface of anode 118 may be coated with a conductive material, such as chrome, to provide an electrical contact to anode 118.

[0020] Image intensifier 100 may include a vacuum housing 130 to house photo-cathode 102, semiconductor structure 110, and anode 118.

[0021] Photo-cathode 102 and semiconductor structure 110 may be positioned such that output surface 102b of photo-cathode 102 is in relatively close proximity to input surface 110a of semiconductor structure 110 (e.g., less than approximately 10 millimeters, or within a range of approximately 100 to 254 microns).

[0022] Semiconductor structure 110 and anode 118 may be positioned such that emission surface 110b is in relatively close proximity to anode surface 118a. For example, if anode 118 includes an integrated circuit, the distance between emission surface 110b and anode surface 118a may be, without limitation, within a range of approximately 10 to 15 millimeters, or within a range of approximately 250 to 381 microns. If anode 118a includes a phosphor screen, the distance between emission surface 110b and sensor surface 118a may be, without limitation, approximately 10 millimeters.

[0023] Image intensifier 100, or portions thereof, may be configured as described in one or more examples below. Image intensifier 100 is not, however, limited to the examples below.

[0024] FIG. 2 is cross-sectional view of a semiconductor structure 200, configured as an electron multiplier and shield. Semiconductor structure 200 may represent an example embodiment of semiconductor structure 110 in FIG. 1.

[0025] Semiconductor structure 200 is doped to generate a plurality of free electrons 204 for each free electron 201 that impinges a surface 200a of semiconductor structure 200.

[0026] Semiconductor structure 200 includes first and second regions 202 and 208, which are doped to direct the flow of electrons 204 to emission areas 210 of emission surface 202b. Emission areas 210 may be activated to a negative electron affinity state to facilitate electron flow from emission regions 210. Second region 208 may also be referred to herein as a background region.

[0027] First region 202 is doped to force electrons 204 away from input surface 200a into semiconductor structure 200, thus inhibiting recombination of electron-hole pairs at input surface 200a. Inhibiting recombination of electron-hole pairs at input surface 200a ensures that more electrons flow through semiconductor structure 200 to emission surface 200b, thereby increasing efficiency.

[0028] Region 208 (alone and/or in combination with region 202), may also be referred to herein as an electron multiplier region.

[0029] Semiconductor structure 200 further includes regions 212, which are doped to repel free electrons 204. Regions 212 may also be referred to herein as blocking structures 212. Blocking structures 212 define blocking areas 214 of emission surface 200b, where electron flow into and out of semiconductor structure 200 is inhibited. Blocking regions 212 may help to maintain spatial fidelity. Blocking structures 212 may provide other benefits and/or perform other functions. Semiconductor structure 200 may provide suitable electron multiplication without blocking structures 212. Thus, in an embodiment, blocking structures 212 are omitted.

[0030] Stray particles 222 that impinge emission surface 200b of semiconductor structure 200 may convert to free electrons and corresponding holes. Thereafter, the free electrons may be emitted from emission surface 200b to contact anode 118 (FIG. 1). This may negatively impact recording and/or presentation of an image (e.g., as noise).

[0031] In FIG. 2, semiconductor structure 200 thus further includes regions 220, which are doped to reduce and/or minimize effects of stray particles 222. Regions 220 may also be referred to herein as shields 220. In an embodiment, shields 220 are doped to encourage recombination of free electrons and holes. Shields 220 may be said to absorb stray particles 222.

[0032] Semiconductor structure 200 may further include a dielectric film 224 disposed over blocking areas 214, or a portion thereof.

[0033] Semiconductor structure 200 may include silicon and/or other semi conductive material such as, without limitation, gallium arsenide (GaAs).

[0034] In an embodiment, semiconductor structure 200 includes silicon and is relatively doped with a P-type dopant to generate a plurality of free electrons 204 for each free electron 201 that impinges a surface 200a of semiconductor structure 200. First doped region 202 may be doped with a P-type dopant such as boron or aluminum. First doped region 202 may be relatively heavily doped (e.g., 10^{19} parts per cubic centimeter). Second doped region 108 may be relatively moderately doped with a P-type dopant. Blocking structures 212 may be

relatively heavily doped with a P-type dopant such as boron or aluminum (e.g., 10^{19} parts per cubic centimeter). Shields 220 may be doped with an N-type dopant, such as by diffusion or implanting.

[0035] Semiconductor structure 200 may have a thickness of, without limitation, approximately 20-30 microns). First doped region 128 may have a thickness T of approximately 10-15 nanometers. Blocking structures 212 may have a height H of approximately 24 microns.

[0036] A gap 240 may be provided between first doped region 202 and blocking structures 212. Gap 240 may be sized or dimensioned such that second doped region 212 does not interfere with the generation of electrons 204 at input surface 200a. This may provide semiconductor structure 200 with an effective electron multiplication area that equals or approaches 100% of an area of input surface 200a. Gap 240 may be, without limitation, approximately one micron.

[0037] Other suitable dopants, concentrations, dimensions, and/or semiconductor materials, such as GaAs, may be used, as will be readily apparent to one skilled in the relevant art(s).

[0038] In FIG. 2, regions between adjacent blocking structures 212 may be view as channels that extend from input surface 200a to emission areas 210. The channels have relatively wide cross-sectional areas near input surface 200a, and relatively narrow cross-sectional areas towards emission areas 210. The channels may act as funnels to direct electrons 204 to emission areas 210. The channels may also be referred to herein as an electron bombarded cells (EBCs). Semiconductor structure 200 may be configured with an array of EBCs, such as described below with reference to FIGS. 3 through 6. Semiconductor structure 200 is not, however, limited to the examples of any of FIGS. 3 through 6.

[0039] FIG. 3 is cross-sectional perspective view of an example embodiment of semiconductor structure 200, in which semiconductor structure 200 includes multiple rows of parallel and perpendicular blocking structures 212, to form an array of emission areas 210.

[0040] FIG. 4 is view an example embodiment of semiconductor structure 200 directed toward emission surface 200b (View A in FIG. 3), in which shields 220 are omitted for illustrative purposes. In this embodiment, semiconductor structure 200 includes a first set of multiple rows of blocking structures 212-1, and a second set of multiple rows of blocking structures 212-2. Blocking structures 212-1 are perpendicular to blocking structures 212-2, to define emission areas 210, and EBCs 402.

[0041] Semiconductor structure 200 may be configured to generate, for example, several hundred electrons in each EBC 402 that receives an electron. The number of electrons emitted from emission areas 210 may thus be significantly greater than the number of electrons that impinge input surface 200a.

[0042] FIG. 5 is another view of the example embodiment of FIG. 4, in which shields 220 are illustrated. In an embodiment, a width W_1 of a base portion of blocking structures 212 is approximately 10-20 microns, and a width W_2 of emission areas 210 is approximately 0.5 to 2.0 microns. In this example, blocking areas 210 encompass more than 80% of an area of emission surface 200b of semiconductor structure 200. Semiconductor structure 200 is not, however, limited to these examples.

[0043] FIG. 6 depicts an expanded view of an EBC 402. In an embodiment, emission area 210 has a width W_2 of is approximately 1 micron. An exposed portion (e.g., ring) of blocking structure 212 extends a distance D of approximately 0.5 micron beyond emission area 210.

[0044] In the examples of FIGS. 3, 4, and 5, semiconductor structure 200 is illustrated as a square array of EBCs 402. Semiconductor structure 200 may be configured with other geometric (e.g., circular, rectangular, or other polygonal shape), which may depend upon an application (e.g., circular for lens compatibility, or square/rectangular for integrated circuit compatibility). In an embodiment, to replicate a conventional micro-channel plate used in an image intensifier tube, a square array 1000×3000 EBCs 402, or more, may be used. This may be useful, for example, to replicate a micro-channel plate of a conventional image intensifier tube.

[0045] In the examples of FIGS. 4 and 5, semiconductor structure 200 is depicted as a 6x6 array of EBCs 402. Semiconductor structure 200 is not, however, limited to this example. The number of EBCs 402 employed in an array may be more or less than in the foregoing example, and may depend on the size of the individual EBCs 402 and/or a desired resolution of an image intensifier.

[0046] In the examples of FIGS. 3 through 6, emission areas 210 are depicted as having square shapes. Emission areas 210 are not, however, limited to square shapes. Emission areas 210 may, for example, be configured as circles and/or other geometric shape(s).

[0047] Each EBC 402 and associated emission area 210 corresponds to a region of input surface 200a (FIG. 2), such that the array of EBCs 402 pixelate electrons received at input surface 200a.

[0048] FIG. 7 is a flowchart of a method 700 of intensifying an image and limiting effects of stray particles. Method 700 may be performed with an apparatus disclosed herein. Method 700 is not, however, limited to example apparatus disclosed herein.

[0049] At 702, a plurality of electrons is generated within a semiconductor structure, for each electron that impinges a reception surface of a semiconductor structure, such as described in one or more examples herein.

[0050] At 704, the plurality of electrons is repelled from blocking regions of the semiconductor structure that are doped to repel electrons, towards emissions areas of an emission surface of the semiconductor structure, such as described in one or more examples herein.

[0051] At 706, stray particles that impinge the emission surface of the semiconductor structure are absorbed within shielding regions of the semiconductor structure, such as described in one or more examples herein.

[0052] Techniques disclosed herein may be implemented with/as passive devices (*i.e.,* with little or no active circuitry or additional electrical connections).

[0053] Techniques disclosed herein are compatible with conventional high temperature semiconductor processes and wafer scale processing, including conventional CMOS and wafer bonding processes.

[0054] Methods and systems are disclosed herein with the aid of functional building blocks illustrating functions, features, and relationships thereof. At least some of the boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries may be defined so long as the specified functions and relationships thereof are appropriately performed. While various embodiments are disclosed herein, it should be understood that they are presented as examples. The scope of the claims should not be limited by any of the example embodiments disclosed herein. While a particular embodiment of the present invention has been shown and described in detail, adaptations and modifications will be apparent to one skilled in the art. Such adaptations and modifications of the invention may be made without departing from the scope thereof, as set forth in the following claims.

Claims

1. A method, comprising:

generating a plurality of electrons for each electron that impinges a reception surface of a semiconductor structure, within an electron multiplier region of a semiconductor structure;
repelling the plurality of electrons from blocking regions of the semiconductor structure that are doped to repel electrons, towards emissions areas of an emission surface of the semiconductor structure; and
absorbing stray particles that impinge the emission surface of the semiconductor structure within shielding regions of the semiconductor structure that are doped to absorb photons, wherein the stray particles include one or more of stray photons and stray ions.

2. The method of claim 1, wherein the absorbing includes:

converting the stray particles to respective pairs of stray electrons and stray holes within the shielding regions; and
recombining the stray electrons with the stray holes within the shielding regions.

3. The method of claim 1, wherein:

the blocking region and the electron multiplier region are doped with a P-type dopant; and
the shielding region is doped with an N-type dopant.

4. The method of claim 1, wherein:

the blocking region extends from the emission surface of the semiconductor structure towards the reception surface of the semiconductor structure; and
the shielding region is within the blocking region.

5. The method of claim 1, wherein:

the blocking region includes a plurality of blocking regions, each doped to repel the plurality of electrons towards respective adjacent emissions areas of the emission surface of the semiconductor structure; and
the shielding region includes a plurality of shielding regions, each doped to absorb stray particles that impinge respective regions of the emission surface of the semiconductor structure.

6. The method of claim 5, wherein:

the plurality of blocking regions include multiple rows of blocking channels that extend from the emission surface of the semiconductor structure toward the reception surface of the semiconductor structure; and
the plurality of shielding regions include multiple shielding channels, each positioned within a respective one of the blocking channels.

7. The method of claim 6, wherein:

the multiple rows of blocking channels includes a first and second rows of blocking channels; and
the first row of blocking channels is perpendicular to the second row of blocking channels.

8. The method of claim 1, wherein:

the semiconductor substrate is configured as an array of similarly configured cells; and
a first one of the cells includes the shielding region, the blocking region within the shielding region, and the emission area within the blocking region.

9. The method of claim 1, wherein:

the blocking region includes a 2-dimensional array of blocking areas on the emission surface of the semiconductor structure;
the emission area includes a 2-dimensional ar-

ray of emission areas, each within a respective one of the blocking areas; and
the shielding region encompasses a remaining portion of the emission surface of the semiconductor structure.

10. An apparatus comprising means for performing the method of any one of claims 1-9

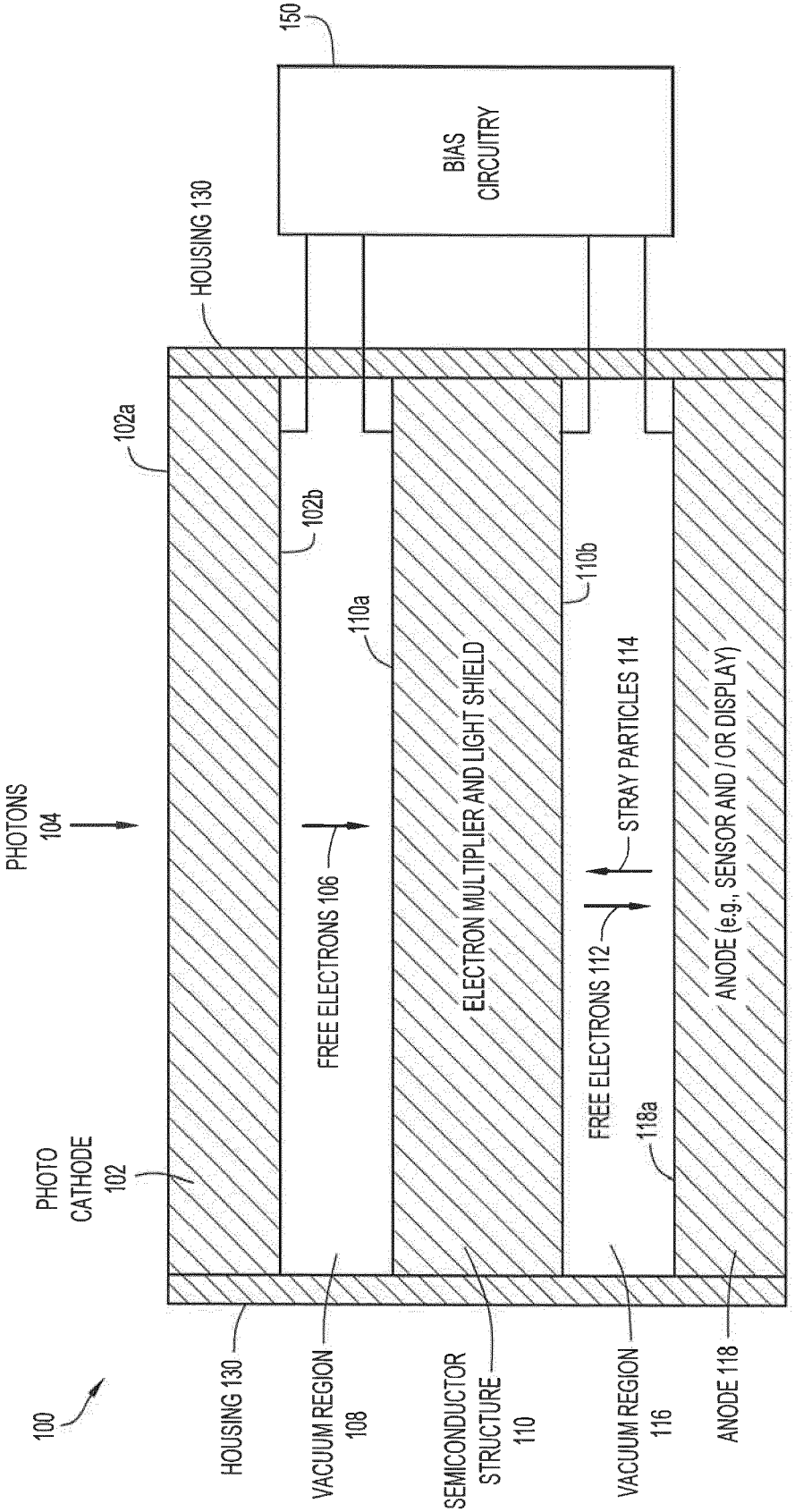

150
BIAS CIRCUITRY
HOUSING 130
102a
102b
110a
110b
PHOTONS 104
FREE ELECTRONS 106
ELECTRON MULTIPLIER AND LIGHT SHIELD
STRAY PARTICLES 114
FREE ELECTRONS 112
118a
ANODE (e.g., SENSOR AND / OR DISPLAY)
PHOTO CATHODE 102
100
HOUSING 130
VACUUM REGION 108
SEMICONDUCTOR STRUCTURE 110
VACUUM REGION 116
ANODE 118

FIG.1

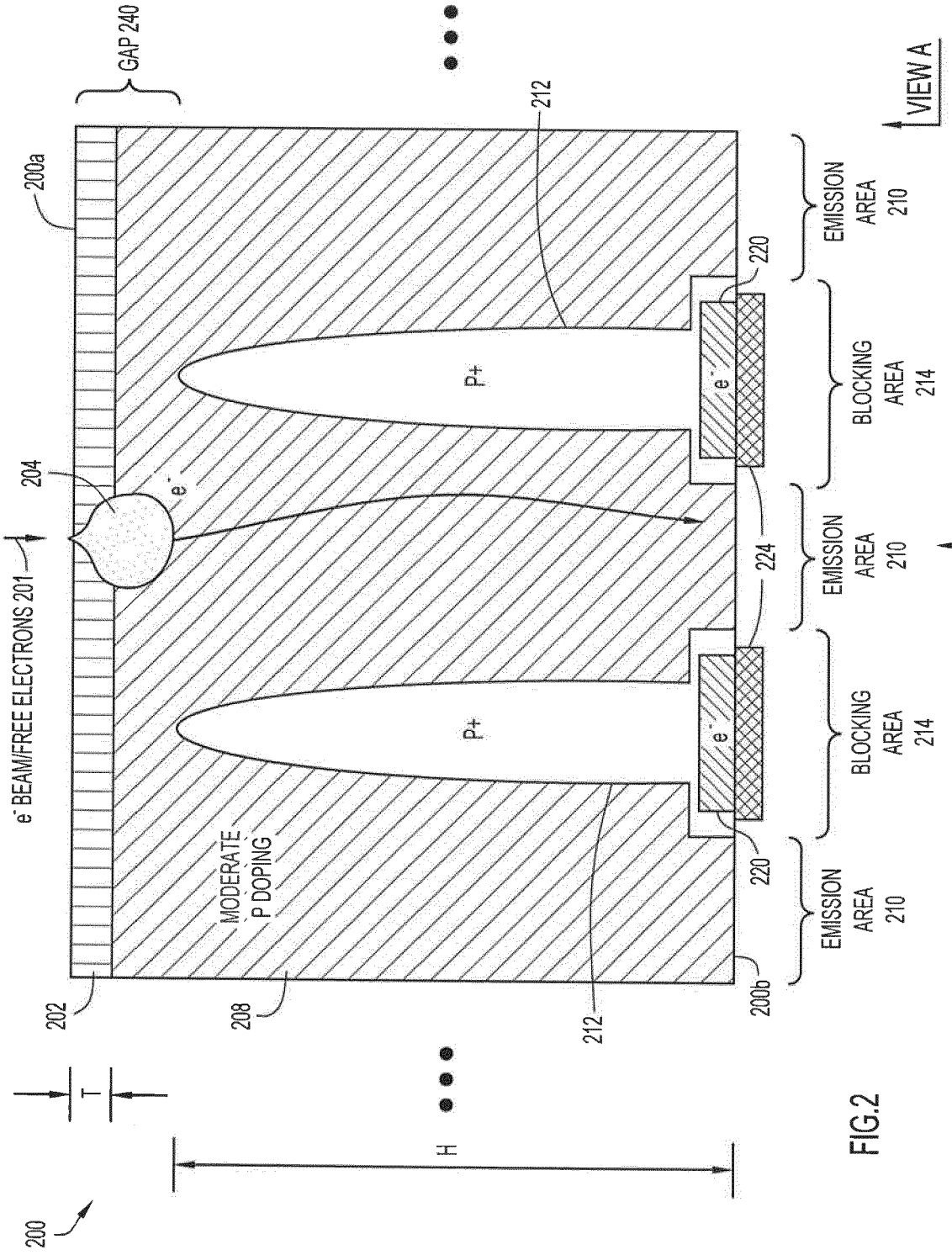
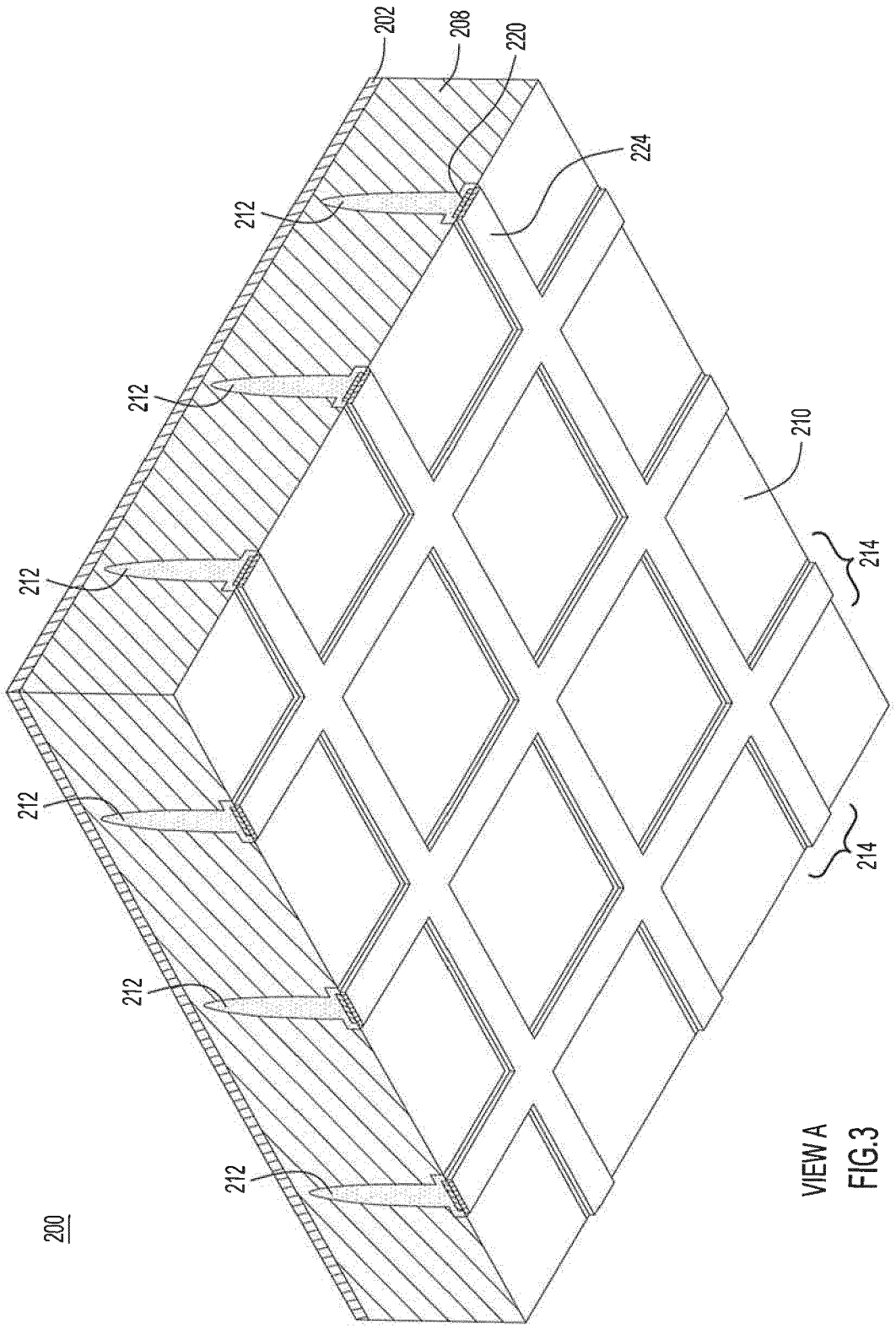
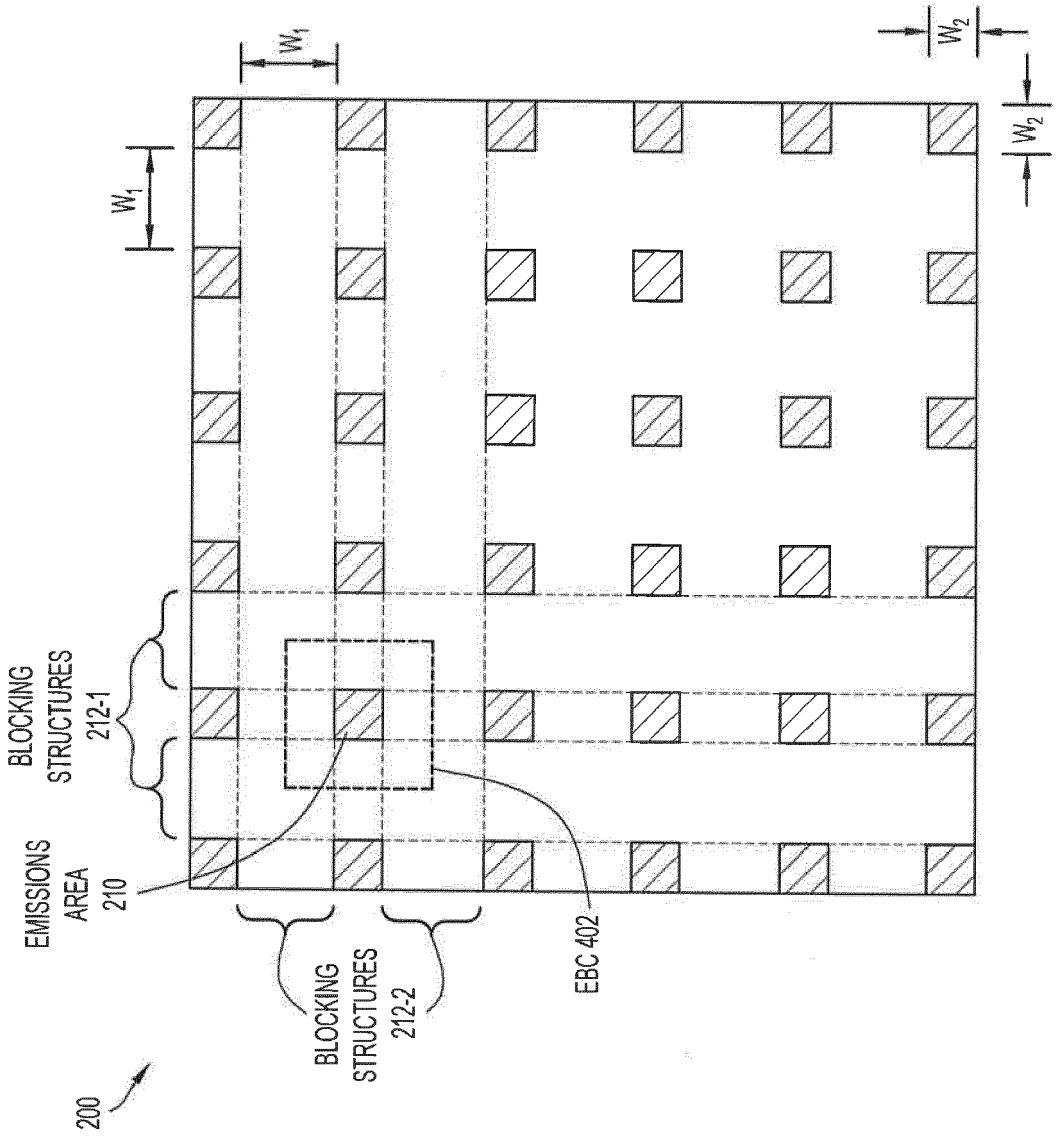

GAP 240
200a
212
VIEW A
EMISSION AREA 210
BLOCKING AREA 214
220
e⁻
P+
204
e⁻ BEAM/FREE ELECTRONS 201
224
STRAY PHOTONS/ELECTRONS 222
MODERATE P DOPING
202
208
212
200b
T
H
200

FIG.2



VIEW A
FIG.3


W1
W2
W2
W1
BLOCKING STRUCTURES 212-1
EMISSIONS AREA 210
BLOCKING STRUCTURES 212-2
EBC 402
200

VIEW A

FIG.4

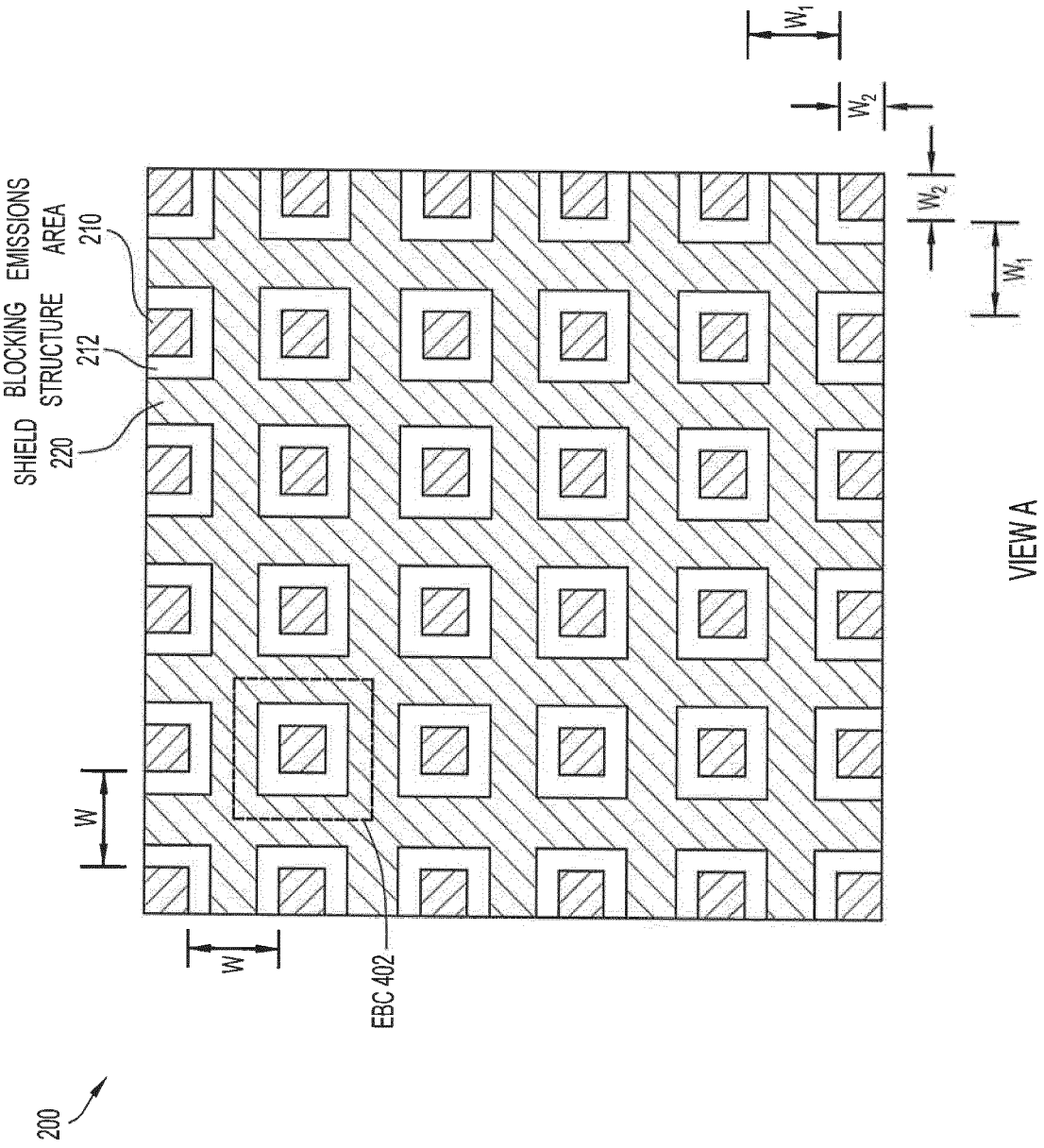
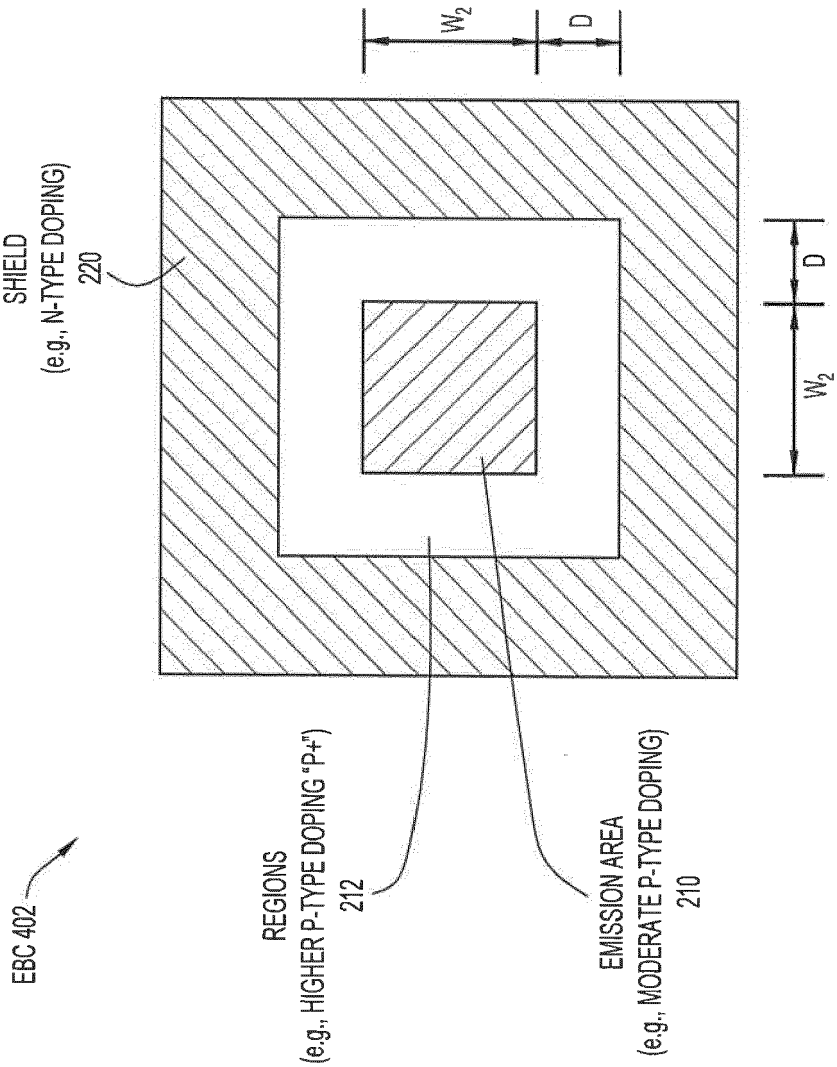

200
SHIELD 220
BLOCKING STRUCTURE 212
EMISSIONS AREA 210
W
W
EBC 402
W1
W2
W2
W1
VIEW A

FIG.5


SHIELD
(e.g., N-TYPE DOPING)
220
EBC 402
REGIONS
(e.g., HIGHER P-TYPE DOPING "P+")
212
EMISSION AREA
(e.g., MODERATE P-TYPE DOPING)
210
W_2
D
D
W_2

VIEW A

FIG.6

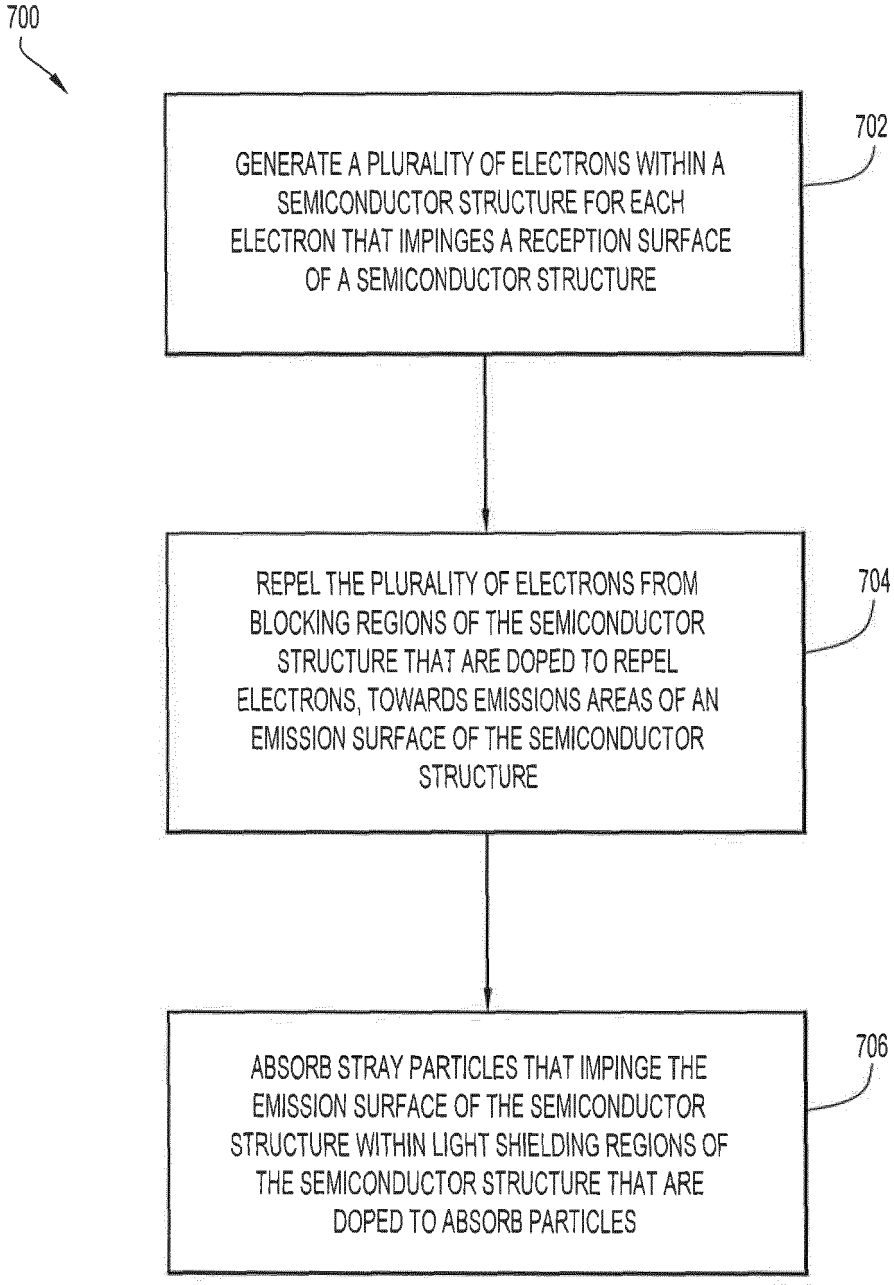

700
GENERATE A PLURALITY OF ELECTRONS WITHIN A SEMICONDUCTOR STRUCTURE FOR EACH ELECTRON THAT IMPINGES A RECEPTION SURFACE OF A SEMICONDUCTOR STRUCTURE
702
REPEL THE PLURALITY OF ELECTRONS FROM BLOCKING REGIONS OF THE SEMICONDUCTOR STRUCTURE THAT ARE DOPED TO REPEL ELECTRONS, TOWARDS EMISSIONS AREAS OF AN EMISSION SURFACE OF THE SEMICONDUCTOR STRUCTURE
704
ABSORB STRAY PARTICLES THAT IMPINGE THE EMISSION SURFACE OF THE SEMICONDUCTOR STRUCTURE WITHIN LIGHT SHIELDING REGIONS OF THE SEMICONDUCTOR STRUCTURE THAT ARE DOPED TO ABSORB PARTICLES
706

FIG.7

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EUROPEAN SEARCH REPORT

Application Number
EP 19 17 5825

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2004/189166 A1 (SMITH ARLYNN WALTER [US]) 30 September 2004 (2004-09-30) * paragraph [0013] - paragraph [0027] * * figures 3, 3a, 4 * -----	1-10	INV. H01J31/50 H01J43/04 H01J1/32
A	Paul M Amirtharaj ET AL: "OPTICAL PROPERTIES OF SEMICONDUCTORS" In: "Handbook of Optics, Volume II, Devices, Measurements, and Properties", 1 January 1995 (1995-01-01), McGraw-Hill, New York, NY 021278, XP055631083, ISBN: 978-0-07-047974-6 pages 36.1-36.96, * first 9 lines of section "Overview"; page 36.12 * -----	1-10	

TECHNICAL FIELDS SEARCHED (IPC)
H01J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	11 October 2019	Cornelussen, Ronald

CATEGORY OF CITED DOCUMENTS

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& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 19 17 5825

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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11-10-2019

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82