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(54) **DIGITAL DRIVING IMPLEMENTATION AT MULTIPLE REFERENCE LIGHT INTENSITIES**

(57) A driver system for driving pixels of an active matrix display and a method related thereto are disclosed. The driver system comprises at least one power supply line pair having first and second power supply lines (311, 312). Each power supply line pair comprises an ordered sequence of contact point pairs (306, 307) distributed over its length. Circuit elements (300, 400) are connected to a data line (313) and to the contact point pairs. During use, the circuit elements are driven at pre-determined current levels through its corresponding contact points, there being at least three such pre-determined current levels selectable via a received data signal. Also provided is a voltage drop calculation unit (30) for calculating voltage drops at the level of each circuit element. A voltage drop causing a deviation of the current levels from their pre-determined values, at least one voltage drop compensation unit (109, 119) is provided for compensating the calculated voltage drops at each circuit element by way of providing a data compensation signal on a data line. A method of calibrating voltage drop compensation signals is also described.

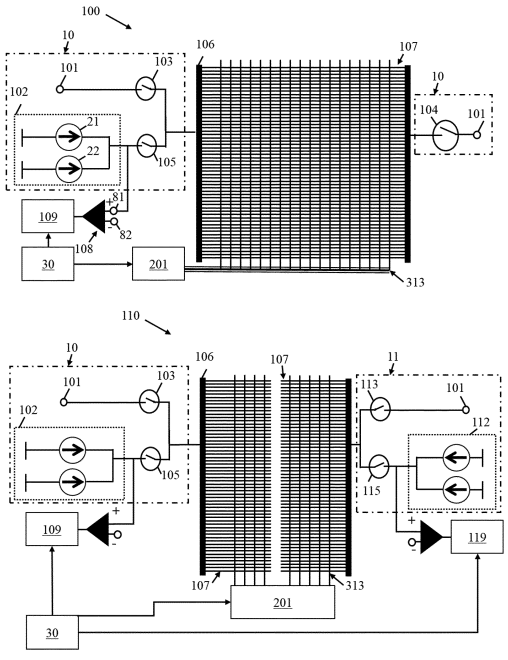

FIG. 1

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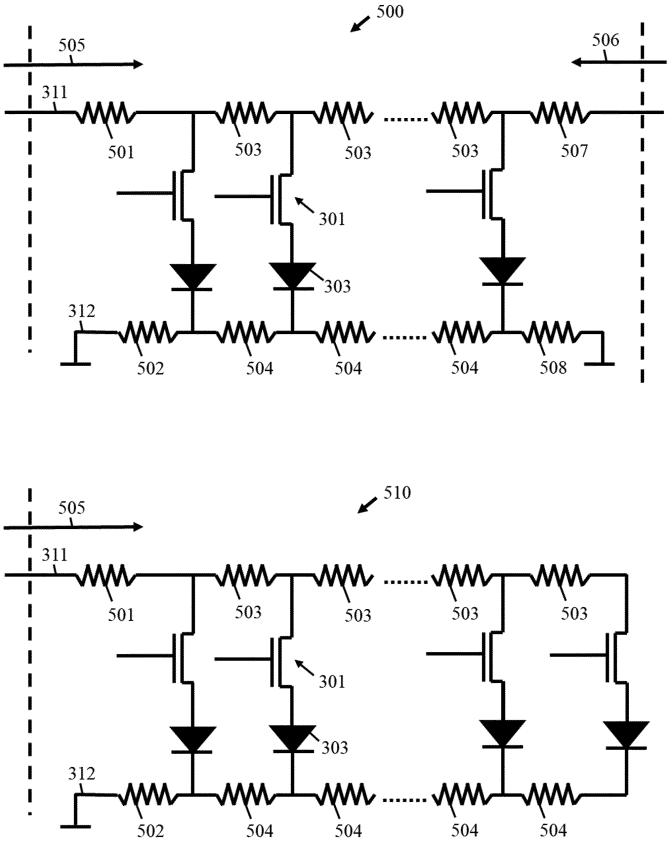
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FIG. 5

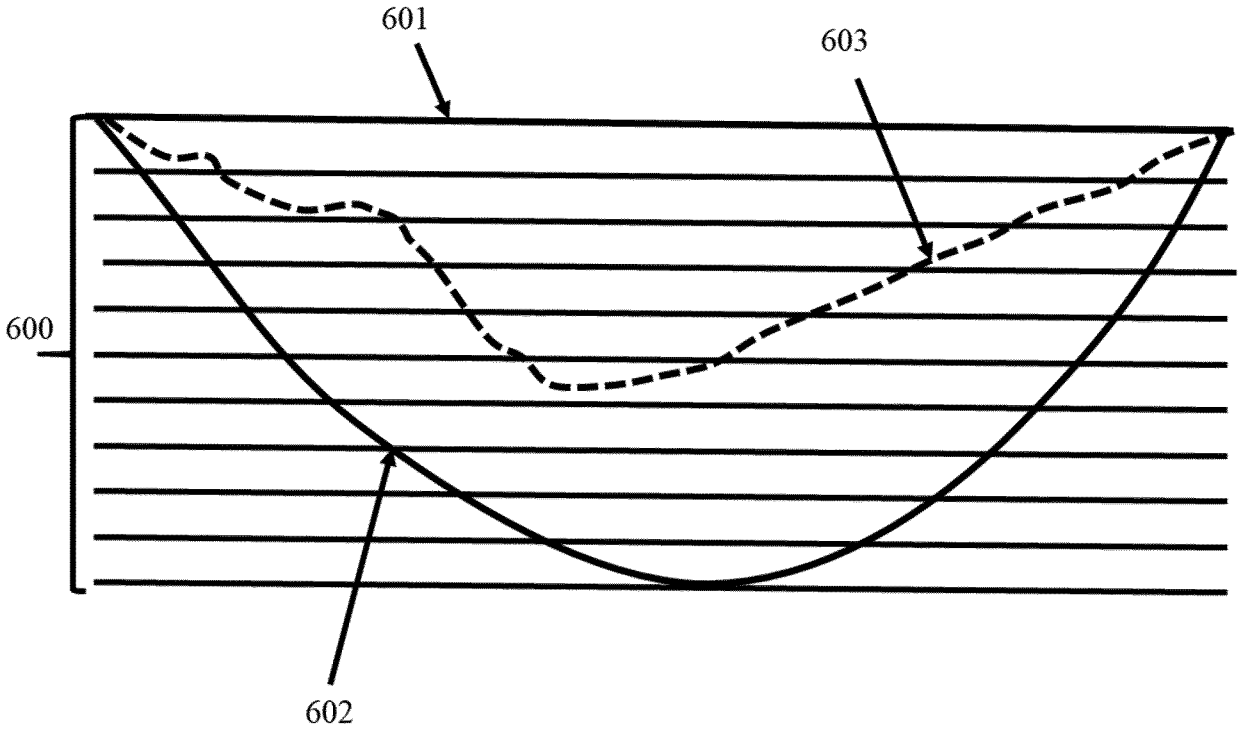
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FIG. 6

Description

Field of the invention

[0001] The present invention relates to the field of digital driving methods and circuitry for active matrix displays, for instance active matrix light emitting diode displays (AMLEDs) or active matrix organic light emitting diode displays (AMOLEDs).

Background of the invention

[0002] In active matrix displays each pixel has an associated pixel driving circuit adapted for controlling its light output, e.g. luminance or brightness, by driving a current through a light emitter, for instance an OLED or LED, in a controlled fashion. This is typically achieved by a driving transistor for which a gate voltage signal is controlling the drained current injected into the light emitter. An analogue driving method ensures a continuous control of the driving current levels and hence of the pixel brightness. A driving current level is held constant during the full frame period and driving transistors are usually operated in the saturation regime. The longer active time of the pixel when it is emitting light can lead to a faster degradation of the light emitters, in particular when being OLEDs, reducing the display's lifecycle. Operating the driving transistors in their saturation regions also requires larger supply voltages, which increases the power dissipation in the backplane of the display panel and also contributes to temperature stress and aging of the active matrix display.

[0003] Digital driving methods commonly implement pulse width modulation (PWM) for encoding the grey scales of the pixel, e.g. its brightness levels. This method uses the driving transistor as a switch which is switched on and off many times during a full frame period by binary voltage signals applied to the transistor gate. A resulting averaged light output over a full frame period corresponds to the desired grey level of the pixel. Digital driving methods using PWM work best if every pixel driving circuit has identical driving currents during operation. However, many causes may contribute to deviations of the driving currents leading to a loss of image quality. Among these causes appear non-uniform fabrication processes (e.g. non-uniform thickness of dielectric layers, doping concentration variations, grain boundaries in low temperature polysilicon, etc.), but also aging, temperature induced changes, and voltage drops on the power supply lines during display operation are adversely affecting uniformity across the flat panel display.

[0004] Patent application EP 16197152.8 discloses a calibration and compensation method for digitally driven active matrix displays which addresses the problem of display non-uniformity caused by resistive voltage drops on the power supply lines. However, this method works only for restricted colour depths/number of grey scales, as the duration of the shortest PWM pulse is limited by the RC time constants of the pixel driving circuits or the rising time (speed) of the PWM driver circuit, whichever is largest. There is still a need for improved active matrix display drivers and compensation methods providing uniform operation characteristics across the display and providing large image contrast for better viewing experience.

Summary of the invention

[0005] It is an object of embodiments of the present invention to provide good devices and methods for driving active matrix displays at high colour accuracy, such as for instance, but not limited thereto, AMLED or AMOLED display.

[0006] The above objective is accomplished by a device and a method in accordance with embodiments of the present invention.

[0007] In a first aspect the present invention relates to a driver system for driving pixels of a display. The driver system comprises at least one power supply line pair of first and second power supply lines. An ordered sequence of contact point pairs is distributed over the length of the at least one power supply line pair; and each one of a plurality of circuit elements is connected to a couple of contact points from the sequence of contact point pairs such that an electrical connection between the first and the second power supply lines is established. Each circuit element is adapted for being driven at pre-determined current levels through its corresponding couple of contact points. At least three such pre-determined current levels are selectable via a data signal which each circuit element is receiving on a data line. A voltage drop calculation unit is calculating the voltage drops over the power supply lines at the level of each connected circuit element, when this is driven so as to deliver a pre-determined current level. A voltage drop causes a deviation of the actually delivered current levels from their pre-determined values. At least one voltage drop compensation unit is compensating the calculated voltage drops at each connected circuit element by providing a data compensation signal to the at least one data line.

[0008] According to some embodiments of the present invention, the at least three pre-determined current levels may comprise exactly two pre-determined non-zero current levels and a third, substantially zero current level.

[0009] Particular embodiments of the present invention may further comprise at least one power supply unit operably connected to the at least one power supply line pair for powering each of the connected circuit elements. The at least

one power supply unit is a switchable power supply unit adapted for switching between a driving mode and a calibration mode.

[0010] The at least one power supply unit may comprises a current generation unit including at least two current sources. A ratio of currents generated by the at least two current sources may be fixed. Alternatively, the at least one power supply unit may comprise a current generation unit including a single programmable current source.

[0011] According to some embodiments of the present invention, at least one power supply unit is operably connected to only one end of the at least one power supply line pair.

[0012] According to other embodiments of the present invention, at least one power supply unit is operably connected to both ends of the at least one powers supply line pair.

[0013] Embodiments of the present invention may comprise at least two power supply line pairs and at least two power supply units and each of the at least two power supply units is operably connected to a different power supply line pair.

[0014] Embodiments of the present invention may further comprise at least one readout unit which is electrically coupled to the at least one switchable power supply unit for detecting a power supply signal in the calibration mode and comparing it to a reference. The reference may be a set of pre-determined voltage drop levels.

[0015] Embodiments of the present invention may further comprise a memory block for storing representative calibration values as a result of comparison with a reference in calibration mode. Stored representative calibration values may be retrieved from the memory block in the driving mode.

[0016] Embodiments of the present invention may further comprise an interpolation unit for interpolating, in the driving mode, between at least two retrieved representative calibration values which were previously stored in the memory block.

[0017] Embodiments of the present invention may further comprise a ground drop multiplication unit for compensating an offset in ground for data signals received at each of the connected circuit elements.

[0018] Particular embodiments of the invention may comprise a plurality of data lines and at least one data line driver for providing data signals on the plurality of data lines. Each circuit element may include a driving transistor, a control terminal of which is connectable to one of the plurality of data lines.

[0019] The driving transistors may be operated in the linear region.

[0020] In particular embodiments of the present invention, the at least one data line driver is suitable for providing pulse width modulated data signals on the plurality of data lines.

[0021] In a second aspect, the present invention relates to an active matrix display for displaying images. The active matrix display comprises a driver system according to any of the embodiments of the first aspect. The plurality of circuit elements are formed by a plurality of pixel driving circuits and each pixel driving circuit comprises at least one light emitting element.

[0022] The at least one light emitting element of each pixel driving circuit may be an OLED or LED. The luminance of each light emitting element may be controllable at up to 16 bit colour resolution.

[0023] For some embodiments of the present invention, pixel driving circuits are implemented as 2T1C driving circuits.

[0024] In a third aspect, the present invention relates to a method of compensating voltage drops on a power supply line pair. In one step of the method voltage drops for contact point pairs placed along a power supply line pair are calculated under the assumption that a current of a pre-determined current level is flowing between each contact point pair. A pre-determined current level is selected from a set of at least three distinct values, one of which is substantially zero. In another step of the method voltage drop compensation signals are determined which, when they are applied to control terminals of circuit elements, cause a deviation of current levels from said pre-determined current levels to be reduced. Each circuit element is connected to a contact point pair and voltage drop compensation signals are determined using the calculated voltage drops as inputs.

[0025] According to some embodiments of the present invention, voltage drop compensation signals may be determined by further using calibrated response curves of connected circuits elements as inputs. A calibration of each response curve may comprise the step of providing a current at one of said pre-determined but non-zero current levels to the single connected circuit element whose response curve is under calibration. The current is injected into a power supply line of the power supply line pair and a pre-determined substantially zero current level is applied to all of the remaining connected circuit elements. In another step a voltage signal may be detected at one end of the power supply line pair and compared to a reference. In another step, a voltage drop compensation value applied to a control terminal of the circuit element under calibration is increased, if comparing the detected voltage signal to a reference yields a first outcome, or memorizing a representative calibration value of the voltage drop compensation value applied to a control terminals of the circuit element under calibration, if comparing the detected voltage signal to a reference yields a second outcome.

[0026] According to some embodiments of the present invention, at least two memorized representative calibration values may be used as inputs for the determination of voltage drop compensation signals. The at least two memorized representative calibration values may be addressed by a calculated voltage drop for the circuit element which is compensated.

[0027] Some embodiments of the present invention, may further comprise the step of interpolating between the at

least two addressed memorized representative calibration values, taking into account the calculated voltage drop for the circuit element which is compensated.

[0028] Some embodiments of the present invention, may further comprise the step of performing a ground voltage multiplication step. This step may be correcting differences in a ground potential in respect of which voltage drop compensation signals at the currently compensated circuit element and a potential across its corresponding contact points are defined.

[0029] It is an advantage of embodiments of the invention that a driving current of the light emitting element is controlled on the power supply lines, rather than a driving voltage. This allows an accurate control of the light output, as a driving current is typically proportional to the light output.

[0030] It is an advantage of embodiments of the invention that accurate light output is obtained, allowing 16 bit colour depth or more for each colour channel.

[0031] Embodiments of the present invention benefit from the fact that non-uniformity of circuit element due to the manufacturing process may be compensated for, for instance compensation of non-uniformity linked to the light emitting elements and/or the driving transistors may be compensated as well as their degradation during the product lifetime.

[0032] It is an advantage of embodiments of the invention that calibration scans calibrating the deviation of a calculated and a measured voltage drop may be performed sporadically, not affecting the correct functioning of the display or its image quality.

[0033] It is an advantage of embodiments of the invention that the compensation of calculated voltage drops may be performed inside an integrated chip, which allows for simple and compact pixel driving circuit layouts. This saves design space and also enables high resolution displays.

[0034] It is an advantage of embodiments of the invention that the driving transistors may be operated in a linear regime, whereby power losses of the display are substantially reduced.

[0035] It is an advantage of embodiments of the invention that voltage drops can be determined in a recursive fashion, as this strongly minimizes the underlying logic circuitry of the driver system. Furthermore, voltage drops can be calculated in real-time for each pixel of the display, which reduces storage capacity and energy.

[0036] It is an advantage of embodiments of the invention that a power supply unit may provide at least two first current sources, which yields a more accurate control of the current levels for calibration over the entire colour depth range. Therefore, also the accuracy of the calibration method itself is improved.

[0037] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims.

[0038] For purposes of summarizing the invention and the advantages achieved over the prior art, certain objects and advantages of the invention have been described herein above. Of course, it is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the invention. Thus, for example, those skilled in the art will recognize that the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other objects or advantages as may be taught or suggested herein.

[0039] The above and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

Brief description of the drawings

[0040] The invention will now be described further, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 illustrates two driver systems adapted to perform voltage drop compensation on power supply lines of an active matrix display, according to embodiments of the present invention.

FIG. 2 is a backside view of a flat panel active matrix display and hardware comprising a driver system adapted to perform voltage drop compensation.

FIG. 3 shows an example of a pixel driving circuit in an active matrix display.

FIG. 4 shows another example of a pixel driving circuit in an active matrix display.

FIG. 5 illustrates two circuit models used to explain the calculation of voltage drops on the power supply lines.

FIG. 6 gives example voltage drop curves for one row of pixels.

FIG. 7 shows details of the voltage drop compensation unit used to obtain voltage drop compensation.

[0041] The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not necessarily correspond to actual reductions to practice of the invention.

[0042] Any reference signs in the claims shall not be construed as limiting the scope.

[0043] In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of illustrative embodiments

[0044] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims.

[0045] The terms first, second and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

[0046] Moreover, directional terminology such as top, bottom, front, back, leading, trailing, under, over and the like in the description and the claims is used for descriptive purposes with reference to the orientation of the drawings being described, and not necessarily for describing relative positions. Because components of embodiments of the present invention can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration only, and is in no way intended to be limiting, unless otherwise indicated. It is, hence, to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

[0047] It is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0048] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0049] Similarly it should be appreciated that in the description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

[0050] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art.

[0051] It should be noted that the use of particular terminology when describing certain features or aspects of the invention should not be taken to imply that the terminology is being re-defined herein to be restricted to include any specific characteristics of the features or aspects of the invention with which that terminology is associated.

[0052] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

DEFINITIONS

[0053] In the detailed description of the present invention, a driver system for pixels of an active matrix display and method of driving related thereto are described. However, it is apparent from the description that the driver system and related method are not restricted to pixels of an active matrix display, but are more generally applicable to other driver system applications for which voltage drops occur on power supply line pairs, influencing fixed level driving currents of connected circuits or circuit elements. An array of pulse width modulation controlled motors sharing a common power supply line or a matrix comprising acoustic membranes vibrating at a specific frequency (e.g. for directed sound) may be other non-limiting examples. Therefore, pixels and pixel driving circuits in the context of the present invention are interpreted in a broader scope as circuit elements, if not referring to pixel displays in particular but more generally to

driver systems suitable for such displays.

[0054] For convenience, pixels of a display are arranged into rows and columns. However, this organization of pixels is interpreted in broader sense to include pixel arrangements in which rows or columns correspond to ordered subsets of the ensemble of pixels of a display, each subset being distinguished by an identifying index or label. Therefore, rows and columns of pixels are not limited to straight horizontal or vertical lines of pixels, but rows and columns may also correspond to ordered sets of circles, squares, diamond shapes, etc., wherein the respective shapes are scaled versions of one another, and wherein an ordering relation between the members of the set may, for example, be given as the length of the respective shape-bounding line/shape perimeter.

[0055] The terms brightness and luminance are used interchangeably hereinafter. Hence, when referring to the brightness of a pixel what is meant is the measure luminance (e.g. in cd/m^2 or nit) attributed to this pixel. Similarly, the detailed description will make a distinction between the light output of a pixel and a luminance value attributed to that pixel.

[0056] FIG. 1 shows schematically driver systems 100, 110 for active matrix flat panel displays. The driver systems 100, 110 are typically arranged at the backplane of the display panel, whereas the light emitting elements are located at the front plane. Each pixel of the active matrix display has associated with it a light emitting element at the front plane of the display panel and additional corresponding pixel driving circuitry at the backplane of the display panel. The pixel driving circuitry is addressed by and controlled through the driver system 100, 110. Each driver system 100, 110 comprises at least one switchable power source 10, 11 electrically connectable to power supply lines 107 via at least one first switching element 103, 104, 113. The switchable power source 10, 11 may be a voltage source 101 in one switching mode, e.g. in a 'driving mode', providing a supply voltage, e.g. a fixed potential VDD, to the power supply lines 107. In a different switching mode, e.g. in a 'calibration mode', the switchable power source 10, 11 may be a current generation unit 102, 112, providing a supply current e.g. a fixed current level out of a set of at three different fixed current levels (e.g. high light current, low-light current, and zero current level), to the power supply lines 107. The state of the at least one first switching element 103, 104 is controlled by a 'driving mode select' signal which may be provided to the driver system 100, 110 by means of a controller (e.g. an image interface unit), which may or may not be part of the driver system 100, 110. Alternatively, the 'driving mode select' signal may be provided externally by a user, e.g. via input connectors of the active matrix display. There is a plurality of power supply lines 107 arranged in a stripe-like pattern across the active matrix display, wherein the plurality of power supply lines 107 are typically arranged in pairs comprising a first and second a power supply line (e.g. a first power supply line connected to VDD and a second power supply line connected to GND). The stripe-like patterns may be wire connections provided, for example, in the backplane of the active matrix display. They serve the purpose of providing a power supply to each of the pixel driving circuits of the active matrix, and in particular, they serve the purpose of powering the light emitting elements of each pixel driving circuit associated with each pixel of the display. The power supplied by the at least one switchable power source 10, 11 may be distributed to a particular pair of first and second power supply line corresponding to a particular row of pixels, for instance, to a pair of first and second power supply line corresponding to a row of pixels selected for writing data signals and/or for actively driving a driving current through the light emitting elements (e.g. LEDs or OLEDs) of the associated pixel driving circuits. This may be achieved by a power distributing unit 106 (e.g. hard-wired) to which the ends of the power supply lines 107 are coupled. Rows of pixels of the display, and therefore also the associated power supply line pairs, are typically selected sequentially for writing data signals and/or for actively driving them in an emission cycle, wherein a sequence is completed if a data frame or sub-frame (e.g. a data sub-frame of one colour for data frames supporting multiple colours, e.g. RGB) has been loaded and displayed by the active matrix display. The at least one current generation unit 102, 112 of each driver system 100, 110 are electrically connectable to the plurality of power supply lines 107 through at least one second switching element 105, 115, a state of which is controlled by a 'calibration mode select' signal. This signal may be provided to the driver system 100, 110 by means of a controller (e.g. an image interface unit), which may or may not be part of the driver system 100, 110, or may be provided externally via input connectors to the display. Each current generation unit 102, 112 may comprise at least two current sources 21, 22 suitable for accurately generating currents of different magnitudes, e.g. a second current source 22 accurately generates currents the magnitudes of which yield a single pixel light output that is larger by a factor 16 as compared to the single pixel light output caused by the current magnitudes accurately generated by a first current source 21. Each readout unit 108 has one of its inputs 81 coupled to the output of one current generation unit 102, 112. A second input 82 of the readout unit 108 may serve as a reference input with respect to the first input 81. An output of the readout unit 108 is connected to a voltage drop compensation unit 109, 119. It is the role of the voltage drop compensation unit(s) 109, 119 to determine the amount of voltage drop compensation necessary to provide uniform driving currents in each pixel driving circuit, based on the calculated voltage drops provided by the voltage drop calculation unit 30 as inputs. To apply the determined voltage drop compensation to the pixel driving circuits of a row of pixels, a voltage drop compensation unit 109, 119 is typically communicating the determined amount of voltage drop compensation to the data line driver 201 and select line driver (not show in FIG. 1) corresponding to this row of pixels, for instance via a control unit or suitable image interface unit 207. Both data line driver 201 and select line driver are included in the driver system 100, 110. Data signals, which can be compensated data signals, are first generated by the data line driver 201 and then distributed on

a plurality of data lines 313 to the respective pixel driving circuit.

[0057] Referring to FIG. 2, a digitally driven active matrix display is shown. This exemplary display supports 2160*3840 pixels (e.g. three colours, 423 ppi) at its front plane. The pixel backplane 220 may be 12,7 cm (5 inch) wide (W), 22,9 cm (9 inch) high (H), and have a diagonal D of 261,6 cm (10.3 inch). A first set of data line drivers 201 and a second set of data line drivers 202 are placed next to the pixel backplane 220 at its top and bottom, respectively. In consequence, a plurality of data lines (not shown) traverse the backplane 220 in the direction of its height H. A select line driver 203 is arranged next to the backplane 220 at its left side. Therefore, select lines (not shown) are traversing the backplane 220 in the direction of its width W. A supply power line 107 is also shown to be oriented in a width W direction. Pixel driving circuits (not shown) are located at points at which data lines cross select lines such that each pixel driving circuit can be addressed by a dedicated data line - select line pair. In operation, the active matrix display receives image data (e.g. an entire frame or a part thereof) representative of the image to be displayed on one or more inputs 206 (e.g. wire connections, data bus, etc.). The received image data is handed over to an image interface unit 207, which determines the selection sequence of rows of pixels and the (encoded) data signals to be sent on the data lines. Data signals and row select signals are then transmitted to the data line driver(s) 201, 202 and the select line driver 203. Furthermore, a control signal may be sent by the image interface unit 207 to the power distribution unit(s) 106 for enabling power distribution to a row of pixels during a light emission cycle. The image interface unit 207 may also be in charge of sending 'driving mode select' signals and/or 'calibration mode select' signals to the at least one first switching element 103, 104, 113 and the at least one second switching element 105, 115, respectively.

[0058] In one particular embodiment of the present invention, the driver system 100 comprises a plurality of parallelly running power supply lines 107 which extend from one side of the active matrix to other side thereof, there being a single pair of first and second power supply line assigned to each line of pixels of the active matrix display. In this case, a line of pixels of the active matrix display coincides with the logical organization of pixels in rows. The power source 101 is connectable, via the at least one first switching element 103, 104, to both ends of each power supply line 107. However, only one side of the power supply lines 107 is connectable, via the second switching element 105 to one current generation unit 102, one readout unit 108 and one voltage drop compensation unit 109.

[0059] In another embodiment of the present invention, the driver system 110 comprises a plurality of parallelly running power supply lines 107 which extend from each side of the active matrix to the middle thereof, there being a single pair of first and second power supply line assigned to each half-line of pixels of the active matrix display. For this particular embodiment, the logical organization of pixels in rows leads to half-lines of pixels of the active matrix display being the ordered subsets. The power source 101 is connectable, via the at least one first switching element 103, 113, to only one end of each power supply line 107. As a consequence of having doubled the number of power supply lines 107 by providing half-lines, each of the left-sided and the right-sided set of power supply lines is provided with a separate current generation unit 102, 112 to which it can be connected by closing the second switching elements 105, 115. Also the number of readout units 108 and voltage drop compensation units 109, 119 is doubled in comparison with the driver system100. Although more circuit components are present in the driver system110, the number of pixel driving circuits per (logical organized) row of pixels that require voltage drop determination and compensation has decreased. This is of benefit for speeding up the voltage drop compensation method.

[0060] All of above switching elements 103, 104, 105, 113, 115, power source 101, power distributing unit 106, current generation unit(s) 102, 112, readout unit(s) 108, and voltage drop compensation unit(s) 109, 119 may be provided as one or more integrated circuits or may be cointegrated with the active matrix.

[0061] A pixel driving circuit 300 is illustrated in FIG. 3. The driving transistors and the wiring (e.g. comprising the power supply lines, data signal lines, and select lines) are typically arranged on a backplane of the display, whereas the light emitting elements of the active pixel matrix (e.g. LEDs or OLEDs) are generally located on a front plane. The circuit 300 shown comprises a driving transistor 301, e.g. a MOSFET, the terminals of which are coupled to a first power supply line 311 (e.g. VDD) and a second power supply line 312 (e.g. GND) via a light emitting element 303, e.g. a LED or an OLED. A control terminal 302 of the driving transistor, e.g. the gate of a MOSFET, is connected to a data line 313 by a data select switch 304 for receiving a data signal which is controlling the driving current 310 through the light emitting element 303. A data select signal is applied to a select line 314, to which the data select switch 304 is connected, for switching on or off one or more data select switches of the active matrix display, e.g. the data select switches of one pixel row of the display. This enables or disables signalling of data, on the data signal line 313, to the driving transistor 301. The driving transistor 301 and/or the data select switch 304 may be implemented in thin-film transistor technology (TFT), p-type or n-type. Non-limiting examples of TFT material platforms may comprise indium gallium zinc oxide (IGZO), amorphous IGZO, polycrystalline silicon (e.g. low-temperature polycrystalline silicone), or amorphous silicon. The circuit further includes a capacitor 305 (e.g. a storage capacitor) one side of which is coupled to the control terminal 302 of the driving transistor 301 and the other side of which is coupled to a contact of the light emitting element 303. A circuit 300 as described with respect to FIG. 3 is an example of a 2T1C (2 transistors, 1 capacitor) pixel driving circuit and may form a building block in an array of pixel driving circuits so as to provide an active matrix display. It is appreciated by the person skilled in the art that such pixel driving circuit may be more complex than in the given example, and may comprise

additional or other electronic elements and/or arrangements of electronic elements. Non-limiting examples of such pixel driving circuits are 6T2C, 5T2C, 4T1C, 4T2C, 3T1C, etc.

[0062] FIG. 4 shows an alternative (inverted) arrangement of a 2T1C pixel driving circuit 400, which differs from the one above in that the light emitting element 303 is arranged such that the driving transistor 301 is coupled to a first power supply line 311 (e.g. VDD) through the light emitting element 303, e.g. the LED or OLED, and is also coupled to the second power supply line 312 (e.g. GND). Moreover, the capacitor 305 has one of its sides coupled to the second power supply line 312 (e.g. GND) instead of being coupled to a contact of the light emitting element 303.

[0063] If the driving transistor 301 is considered as a voltage controlled current source, it is clear from above pixel driving circuits that the output current of the transistor 301 coincides with the driving current 310 injected into the light emitting element 303, whereby the brightness of this pixel is effectively controlled. This provides an analogue driving method for the light output or pixel brightness for which a continuous driving current of the light emitting element 303 is generated by a precise control of the data signal applied to the control terminal 302 of the driving transistor 301. The capacitor 305 may function as a storage capacitor for storing an applied data signal level even after the data select switch 304 is disabled. Then the stored data signal level is still present at the control terminal 302 of the driving transistor 301 and a slowly discharging or floating control terminal 302 is avoided. Therefore, the current driving phase may be decoupled from a phase during which the (storage) capacitor 305 is charged, which may be beneficial for achieving a faster response time of the light emitting element 303.

[0064] As an alternative, a digital driving method may be conceived, wherein a data signal is provided as a pulse width modulated (PWM) signal which, if the data line 313 is selected, is turning the driving transistor 301 on and off. That is, the driving transistor 301 is in this case operated as a switch. According to this digital driving method, the brightness of a pixel is determined by the fraction of time (duty cycle) relative to the time of a full PWM period, for which the driving transistor 301 is in its "on" state, as well as by the driving current 310 injected into the light emitting element 303. In the "off" state, the driving transistor 301 is not conducting and no driving current 310 is flowing through the light emitting element 303. Therefore, embodiments of the present invention obtain both bright pixels and completely dark pixels yielding a high contrast ratio and not suffering from dark glow. Furthermore, a data frame may be divided into several sub-frames, each sub-frame comprising a number of PWM slots. Within a given sub-frame at least one row of pixels is selected twice for the writing of image data to the pixel driving circuits. This approach has been described in patent application US9905159 (B2).

[0065] The shortest time slot allocated in a PWM driving method is generally assigned to the least significant bit (LSB) of a n-bit colour depth (n-bit grey scale with 2^n grey levels) PWM scheme. For a good quality image without flicker, image frame rates of about 60 Hz are required and set an upper bound for the duration of a full PWM period. For instance, an active matrix display comprising 128 lines and operating at a 60 Hz frame rate and 12 bit colour depth (for each colour channel), a PWM driving scheme, which further divides each frame into 16 subframes, may allocate a time slot as small as 4 microseconds to the LSB. The colour depth is then determined by the shortest PWM slot which is still physically possible in the sense that it is not shorter than the characteristic RC constant of the combined data line driver, data lines, and pixel driving circuit (e.g. gate capacitance, storage capacitor, etc.). In practice, state of the art PWM schemes for AMLED or AMOLED displays are restricted to 12 bits of colour depth. The present invention provides a way to extend the range of achievable colour depths without having to introduce more information carrying data bits and without having to further reduce the duration of PWM slots corresponding to the LSB. For instance, particular embodiments of the invention cover a total 16 bit colour depth but use only 12 data bits which effectively carry the image information (e.g. grey tone or brightness level of a pixel). Therefore, the LSB time slot duration remains the one of a conventional 12 bit PWM driving scheme. This is achieved by implementing a high light / low light approach. In fact, at least two different colour scales are used, e.g. a high light scale and a low light scale, both scales occupying only 12 bits. A full 16 bit colour depth may be represented by bit numbers B0, B1, ..., B15. The low light scale uses only 12 out of the 16 bits, wherein bits with numbers B0, B1 , ..., B11 are relevant. Therefore, it makes sense to select the low light scale if all four leading bits, i.e. the four most significant bits B12 to B15, are zero. In the opposite case of detecting one or more non-zero bits among the four most significant bits B12 to B15, the high light scale is chosen. Similar to the low light scale, the high light scale also occupies 12 information carrying bits out of the total 16 bits. However, the high light scale uses the bits with numbers B4, B5, ..., B15. In consequence, the four least significant bits are discarded by the high light scale. This behaviour is supported by the fact that the user's eyes are more sensitive to contrast and grey nuances at low luminance levels as compared to at high luminance levels. It is also supported by the fact that the least significant bits are more relevant for a correct colour representation at lower brightness levels (in the dark) than at higher brightness levels. For instance, if a correct colour representation mixes green and blue with a ratio 20:1 (e.g. blue value at 5 % of green value) then a green light output at 1100 entails a blue light output at 55, which is a correctly representable colour depth value for blue. If the brightness of this colour mixture drops to 1 %, the green light output would be at 11 and still well represented but a blue light output would be either 0 or 1 (depending on truncation/rounding) instead at the required 0.55. Therefore, if a dynamic range is not changed, as proposed by the use of the two colour depth scales (high light and low light), a correct representation of the colour mixture in the dark is not achieved any longer and the perceived colour is different

as it would be at higher display brightness. A practical consequence of the high light / low light approach is that a digital PWM driving method now faces two different colour scales with two different luminance ranges. Depending on whether a pixel is to emit within the high range or the low range, the PWM driving hardware selects either a high reference current level $HL*I_{ref}$ or a low reference current level $LL*I_{ref}$ for driving the light emitting elements 303 of that pixel, e.g. by adjusting the data signals sent on the data lines 313 to the control gate 302 of the driving transistor 301 of the addressed pixel driving circuit.

[0066] The first and second power supply line 311, 312 may provide a supply voltage to the pixel, or alternatively, may provide a supply current to the pixel. Furthermore, the first and second power supply line 311, 312 typically deliver a supply voltage to more than just a single pixel of the display, e.g., they may deliver a supply voltage to a subset of pixels (e.g. a row of pixels). In view of the fact that pixel driving circuits 300, 400 are connected in parallel to form rows of pixels, each row sharing a common the first and second power supply line 311, 312, it is more convenient to connect a voltage source to the first and second power supply line 311, 312 rather than a current generating unit. A supply voltage to the pixel may be defined as the potential difference between first and second power supply line 311, 312 at the points 360, 307 the pixel driving circuit is contacting them with its supply terminals. A supply current to the pixel may be defined as the driving current 310 flowing through the light emitting element 303, which may be proportional to the brightness of the pixel in the operation region. However, a driving current 310 may be compensated for non-linear effects in the light output (e.g. reduced light output due to Auger recombination at higher current levels or non-radiative losses at low current levels), which advantageously widens an operating region of possible pixel brightness levels of a display. Pre-determined values of current levels therefore also allow for a good linearity in the light output of a pixel. Furthermore, it will be appreciated that a variation in light output-driving current response curves of light emitting elements due to fabrication imperfections may be overcome even for a set of pre-determined driving currents common to all the light emitting elements and controlled by a same PWM data signal. To this end, one may compensate the PWM data signal on a pixel driving circuit basis such that additional or less pulses/time slots are allocated for driving the light emitting elements at one of the pre-determined current levels. In consequence, a measurable average light output of different light emitting elements is uniformized for identical (originally uncompensated) PWM data signals, despite the variations in their light output-driving current response curves.

[0067] It is apparent from the above pixel driving circuits 300, 400 in FIG. 3 and FIG. 4 that the supply voltage to the pixel is distributed over the driving transistor 301, the light emitting element 303, and over ohmic contact losses, which may be negligible in comparison to resistive voltage drops of at least one of the light emitting element 303 or the driving transistor 301. The voltage drop across the light emitting element 303 may vary from pixel to pixel of the active matrix display as a consequence of non-uniform fabrication resulting in a statistical distribution of threshold voltages of the light emitting elements 303 (e.g. 0.1 V standard deviation of threshold voltages). Degradation due to aging effects, temperature stress, etc., may also lead to threshold voltages and related voltage drops across the light emitting elements 303 which are not all equal. Therefore, a voltage drop across the driving transistor 301 fluctuates in a pixel dependent fashion. As explained below, also resistive voltage drops along the first and second power supply line 311, 312 introduce a variation of voltage drops across the driving transistors 301 for each pixel driving circuit connected to these lines.

[0068] As the light emitting element 303 is a current-driven element and the driving current 310 directly affects the amount of light it emits, e.g. the associated pixel brightness, a precise control of the driving current 310 is generally required. One way of circumventing the problem of the variability in the voltage drops across the driving transistor 301 causing fluctuations and unstable driving currents 310 across the display, thus leading to non-uniform brightness levels over the display, is to operate the driving transistor 301 in its saturation regime for which the output current is substantially independent on the applied voltage. In this case, the precise transistor output current, and hence the driving current 310, is determined by the signal applied to the control terminal 302 of the driving transistor 301 and by the threshold voltage of the driving transistor 301. This approach, however, requires the high voltage levels typical for the saturation regime (e.g. more than 10 V), which increases the power dissipation of the active matrix display and may cause a shortening of the display lifetime. A transistor threshold voltage compensation circuit may also be necessary (e.g. 0.1 V standard deviation of transistor threshold voltages obtained during fabrication), increasing the number of transistors in the pixel driving circuit and thus limiting display resolution. In the present invention, the driving transistor 301 is preferably operated in the linear or triode regime with the advantage of operating at decreased voltage levels across the driving transistor 301 (e.g. drain source voltages less than 6 V, preferably less than IV) generating less heat and increasing the display's lifetime. If required, the voltage signal at the control terminal 302 (e.g. the gate voltage) of the driving transistor 301 can be reduced.

[0069] A driving current 310 for each light emitting element 303 of the display, may be below 1 microampere, e.g. may be smaller than 0.5 microampere, e.g. about 0.15 microampere, depending on the pixel size and the expected light output. A voltage across the light emitting element 303 is generally higher than the threshold voltage of the light emitting element 303 such that the driving current 310 is indeed flowing and generating light. This voltage may be below 5 V, e.g. about 3.5 V, but may in some cases depend on the emission wavelength (colour) of the light emitting element. For light emitting elements in the red region of the spectrum, it may, for example, range between 2.1 V and 3.1 V, whereas

voltage ranges between 3 V and 4V and in some cases even beyond 5V may be appropriate for light emitting elements working in the blue region of the spectrum.

[0070] Both first and second power supply line 311, 312 may be implemented as metal traces (e.g. copper) in the backplane of the display panel and may be several centimetres long for providing a suitable power supply to the pixel driving circuits of one row of pixels of the display. As a consequence, a small amount of voltage is repeatedly dropped across the distributed resistances of first and second power supply line 311, 312.

[0071] FIG. 5 schematically depicts a portion of one row of pixels 500, 510 (pixel driving circuits are only indicated by their driving transistor 301 and their light emitting element 303, other parts not shown). The first and second power supply line 311, 312 are connected to power source(s) at one side of the row of pixels 510 or on both sides of the row of pixels 500. For instance, the first power supply line 311 may be connected to a positive potential VDD of a voltage source and the second power supply line 312 may be connected to ground potential GND. A supply current 505 is injected into the row of pixels 510 at one side, or two supply currents 505, 506 are injected into the row of pixels 500 on both sides. A small amount of voltage is repeatedly dropped at distributed resistances 503 and 504 if at least a fraction of the provided supply current is flowing through them. Resistances 503 and 504 may correspond to a lumped resistance value (e.g. 0.4 Ohm) for the interconnection wiring between successive pixel driving circuits in a row 500, 510 and the ohmic losses occurring at the contact point pairs 306, 307, respectively. Additionally, there is typically a higher wiring resistance attributed to the wire connections between the row of pixels 500, 510 and the power source(s). These extra resistances 501, 502 or 507, 508, respectively, are only located at the end(s) of the row of pixels 500, 510.As a consequence of the existence of resistances 501, 502, 503, 504, 507, 508, a voltage potential VDD provided by a power source at one end of the first power supply line 311 of a row of pixels 500, 510 is not constant over the whole first power supply line 311. This has the effect that pixel driving circuits arranged farther away from the power source(s) experience a lower pixel supply voltage across their supply terminals, e.g. across their contact point pairs 306, 307, due to the accumulated voltage drops. The same is true for the potential GND provided at an end of the second power supply line 312. Moreover, the voltage drops at resistances 501, 502, 503, 504, 507, 508 also depend on the magnitude of the supply current(s) 505, 506, which is the larger the more pixel driving circuits are actively emitting, e.g. their driving transistors 301 are "on". Therefore, the voltage drops along the first and second power supply lines 311, 312, and hence the supply voltages for each pixel driving circuit of a row of pixels 500, 510, depend on location and on activity. Compensating changes in the supply voltage of a pixel driving circuit is a data-specific process and preferably performed in real-time to not negatively affect the image quality or viewing experience. In particular driving transistors 301 operating in the linear regime for reduced power dissipation are adversely affected by a voltage drop at the pixel driving circuits. Therefore, very accurate determination of voltage drops at each pixel driving circuit in the 'driving mode' is desirable and an accurate calibration process ensures that the correct voltage drop compensation signals are provided to reduce or cancel the voltage drops.

[0072] The difference in potential at the n-th pixel driving circuit in a row of pixels 500, 510 (cumulative voltage drop), determining the supply voltage for this n-th pixel, is expressed as a sum over previous voltage drops

$$\begin{aligned} \Delta V[n] &\equiv V_{DD} - V_n = \sum_{j=0}^{n-1} \partial V_j \\ \Delta V[n] &= \left(R_{SL} + (n-1)R_{ref}\right) I_0 - R_{ref} I_{ref} \sum_{j=1}^{n-1} (n-j) b_j s_j \end{aligned} \qquad (1)$$

[0073] Herein I_0 represents the supply current generated by one of the connected power source(s), R_{SL} the combined resistances 501, 502 of power source wire connections at one end of the row of pixels 500, 510, I_{ref} the reference level for the driving current 310, and R_{ref} the combined resistances 503, 504 of the interconnection wires between consecutive pixel driving circuits in a row of pixels 500, 510. The set of b_i is a sequence of binary values, b in $\{0,1\}^N$, reflecting the "on" or "off" state of each driving resistor 301, that is the "on" or "off" state of each associated pixel. This sequence is determined by the PWM encoding scheme for the data signals and changes dynamically for each data frame to be loaded. A PWM encoded binary sequence b_i may be provided by the image interface unit 207 in response to a received input stream representing an image (or portion thereof) to be loaded. The set of s_i is a sequence of scale factors for the driving current reference level I_{ref} and is a consequence of the high light/low light approach to increased PWM depth (e.g. 16 bit wide instead of 12 bit wide PWM scheme). Therefore, each s_i takes one of the two values 'HL' (high light scale factor) or 'LL' (low light scale factor): s in $\{HL, LL\}^N$. Introducing a constant M representing the ratio of source resistances R_{SL} to R_{ref}, the cumulative voltage drop as a function of pixel position n on the row of pixels 500, 510 is given in Eq. 2.

$$\Delta V[n] = \sum_{j=0}^{n-1} \partial V_j = (M + n - 1) R_{ref} I_0 - R_{ref} I_{ref} \sum_{j=1}^{n-1} \sum_{i=1}^{j} b_i s_i \qquad (2)$$

[0074] If a power source is connected to both ends of the first and second power supply line 311, 312 of a row of pixels 500, the cumulative drop of Eq. 2 may be re-arranged into Eq. 5, using the following boundary condition given in Eq. 3 and the intermediate result of Eq. 4. For convenience it is assumed that the power source(s) on either side of the row of pixels 500 is at a same potential, but it is straightforward to generalize the equations to also include the case of an offset between the two potentials. The first case of a common potential may be obtained by using a single power source and connecting it to either side of the row of pixels 500, which is advantageous, as it avoids additional electronic circuit for implementing another power source.

$$\partial V_N = \Delta V[N] = I_N R_{SR} = I_N P R_{ref} \tag{3}$$

$$I_0 = I_{ref} \frac{\sum_{j=1}^{N} (N+P-j) s_j b_j}{M-1+N+P} \tag{4}$$

$$\Delta V[n] = I_{ref} R_{ref} \left[\frac{M+n-1}{M-1+N+P} \sum_{j=1}^{N} (N+P-j) b_j s_j - \sum_{j=1}^{n-1} (n-j) b_j s_j \right] \tag{5}$$

$$\begin{gathered} \Delta V[n] = \frac{I_{ref} R_{ref}}{M-1+N+P} B_n \\ B_n = (M+n-1) A_N - (M-1+N+P) \sum_{j=1}^{n} (n-j) b_j s_j \\ A_N = \sum_{j=1}^{N} (N+P-j) b_j s_j \end{gathered} \tag{6}$$

[0075] Herein I_N represents the supply current generated by another power source connected to the opposite end of the first and second power supply line 311, 312 of a row of N pixels 500, R_{SR} is the combined resistances 507, 508 of power source wire connections at that opposite end of the row of pixels 500, and P is the ratio of source resistances R_{SR} to R_{ref}. The values of the resistances R_{SR}, R_{SL}, and R_{ref} may be estimated based on design geometries and material selection in a controlled wafer process or may be characterized through measurements on test structures. They are thus known constants and the constants M, P are deduced therefrom. In Eq. 6, the constants A_N and B_n are defined to replace the sums. Constant A_N may be evaluated one row ahead. That is A_N may be evaluated for row x+1 of N pixels (e.g. row of pixels 500) while row x of pixels is actively driven. Once the constant A_N has been determined, the N constants B_n (n=1, ..., N) can be calculated in real-time, e.g. each B_n is determined within one clock cycle after a data signal (e.g. a signal encoding a brightness level of a pixel) addressing the n-th pixel of a row has been received (e.g. by an image interface unit 207) and the so determined value is sent to a suitable data driver, e.g. to the data line driver 201.

[0076] The calculation of each B_n and of A_N may be performed recursively, e.g. with initial conditions $A_0=B_0=C_{0=}0$ and a step stated in Eq. 7. A recursive implementation is of advantage, as it strongly minimizes the underlying logic circuitry of the driver system enabling this calculation and therefore, a calculation of the B_n's is also enabled. A real-time calculation of each B_n is highly desirable since an upfront calculation thereof would require too much storage capacity and energy.

$$\begin{gathered} A_n = \sum_{j=1}^{n} (N+P-j) b_j s_j = A_{n-1} + (N+P-n) s_n b_n \\ B_n = B_{n-1} + A_N - (M-1+N+P) C_{n-1} \\ C_n = \sum_{j=1}^{n} b_j s_j = C_{n-1} + s_n b_n \end{gathered} \tag{7}$$

However, it generally is advantageous to only perform one addition per iteration, for instance one addition per clock cycle in a hardware implemented method, and to avoid the more complex multiplications with two changing multiplicands. This speeds up a hardware implementation for the voltage drop calculation, e.g. in the voltage drop calculation unit 30. Eq. 8 provides an alternative recursion for the B_n and of A_n and uses the fact that the sums of Eq. 6 can be written as double sums. It is observed that all A_n are now recursive sums involving the addition of only two summands in one step of the recursion, e.g. one addition per clock cycle in a hardware implementation. This is achieved by introducing and updating three "helper" partial sums $C_n^{(bn,sn)}$ which only differ by their initial value $C_0^{(bn,sn)}$. The block of equations Eq. 8 may serve as a building block in a hardware description language, e.g. as a VHDL block, for emulating or implementing the voltage calculation method in hardware, e.g. in a voltage drop calculation unit 30. It may also serve as a building

block for implementing the voltage drop calculation in the image interface unit 207 of a display, for example in an arithmetic unit included therein which then is an example of the voltage drop calculation unit 30.

$$\begin{gathered} A_n = P\sum_{j=1}^{n} b_j s_j + \sum_{i=1}^{n-1}\sum_{j=1}^{i} b_j s_j = A_{n-1} + C_{n-1}^{(bn,sn)} \\ A_0 = 0 \\ C_m^{(bn,sn)} = \sum_{j=1}^{m} b_j s_j = C_{m-1}^{(bn,sn)} + s_m b_m \\ C_0^{(bn,sn)} = P s_n b_n \\ B_n = B_{n-1} + D_{n-1} \\ B_0 = (M-1)A_N \\ D_n = A_N - (M-1+N+P)C_n \\ D_n = D_{n-1} - (M-1+N+P)s_n b_n \\ D_0 = A_N \end{gathered} \tag{8}$$

[0077] From Eq. 6, the required size (bit width) for representing A_N at a given resolution (e.g step size of 'one') may be estimated by determining the maximum value A_N takes if all pixel circuits for that row of pixels are active and driven at a high light brightness scale (b_i=1 and s_i=HL, for all i). This results in $Amax_N$ =HL*N*(2P+N-1)/2. Similarly the maximum value of each B_n can take is calculated as $Bmax_n$ =HL*[N(M-1+n)(2P+N-1)-n(M-1+N+P)(n-1)]/2. The largest $Bmax_n$ is estimated by treating n as a continuous variable and determining the local maximum of Bmax(n) as a function of n. One finds n_{max}=[N(2P+N)+(M-1+P)]/[2(M-1+N+P)]. Therefore, the required size/bit width (and related full range) for representing all the B_n's at a given resolution (e.g. single bit steps of size 'one') may be determined from design or measured constants alone as indicated in Eq. 9.

$$\begin{gathered} B_{Nmax} \equiv \max_n B_n = Bmax(n_{max}) \\ B_{Nmax} = HL\,\frac{M^2(4\mathrm{N}(2\mathrm{P}+\mathrm{N}-1)+1)+2\mathrm{M}\left(N^2(2\mathrm{N}+6\mathrm{P}-5)+4\mathrm{N}(\mathrm{P}-1)^2+(\mathrm{P}-1)\right)+\left((\mathrm{N}-1)^2+\mathrm{P}(2\mathrm{N}-1)\right)^2}{8(\mathrm{M}-1+\mathrm{N}+\mathrm{P})} \end{gathered} \tag{9}$$

[0078] To not lose any available resolution at a given bit width, it may be advantageous to rescale the set of B_n's according to their full range, e.g. $B_n \rightarrow B_r$*FullRange/B_{Nmax}. A scaling factor common to all the pixel driving circuits of one row of pixels may be stored in a table, along with all the other scaling factors of different rows of pixels. The recursively defined sums in Eq. 8 are rescaled accordingly and listed in Eq. 10. It is observed that the updates are advantageously computed as sums of two summands, wherein the second summand takes the value of a constant. This may be implemented in hardware, an emulator, or test software, e.g. as a VHDL block in a voltage drop calculation unit 30, for testing or running the implemented method.

$$\begin{gathered} B_n = B_{n-1} + D_{n-1} \\ B_0 = (M-1)\frac{FullRange}{B_{Nmax}}A_N = Scaling_M A_N \\ D_n = D_{n-1} - (M-1+N+P)\frac{FullRange}{B_{Nmax}}s_n b_n \\ D_n = D_{n-1} - \begin{cases} 0, & b_n = 0 \\ Scaling_{MNPLL}, & b_n = 1, s_n = 0 \\ Scaling_{MNPHL}, & b_n = 1, s_n = 1 \end{cases} \\ D_0 = \frac{FullRange}{B_{Nmax}}A_N = A_N Scaling \end{gathered} \tag{10}$$

[0079] FIG. 6 shows an exemplary diagram of calculated voltage drops for the N pixel driving circuits along the first and second power supply line of a typical row of pixels. A power source of equal potential is connected at both ends of the first and second power supply line. A horizontal axis corresponds to the pixel driving circuit count (e.g. n with n=1,...,N) and the vertical axis describes the voltage level present at the respective pixel driving circuit. Therefore, voltage drops are shown in FIG. 6 as deviations from a reference potential, e.g. the potential of the connected power source(s). The line 601 indicates the reference potential, e.g. VDD. The curve 602 represents the case of a maximum voltage drop for the N pixel driving circuits along the first and second power supply line, e.g. all the B_n's in Eq. 6 used for the calculation

of the n-th voltage drops $\Delta V[n]$ are equal to their maximum value $Bmax_n$. Due to the constants M, P not being exactly equal, the curve 602 may not be symmetric, e.g. the largest voltage drop may not occur at the pixel driving circuit located in the middle of the row of pixels. Another curve 603 represents a typical voltage drop behaviour for the N pixel driving circuits of a row of pixels. It is typical in the sense that the voltage levels at the pixel driving circuits are found somewhere in between the reference potential and the minimum possible potential (corresponding to the determined maximal voltage drop), and that the voltage levels at the pixel driving circuits near the centre of the row of pixels are lower (higher accumulated voltage drop) as compared to the voltage levels at the pixel driving circuits near an end (one side connected to a power source) or near the ends (both ends connected to a power source). The collection of lines 600 indicates possible discrete voltage drop reference levels, e.g. a one dimensional grid, to which the readout voltage levels of a single pixel driving circuit are compared during a calibration process. These voltage drop reference levels are typically providing a coarser resolution of the full range of voltage drops on a first and second power supply line than the finely resolved B_n's during driving, e.g. the calculated voltage drops for voltage drop compensation in a selected 'driving mode'. This has the benefit of accelerating the calibration process and also leads to more compact hardware implementations, as less voltage drop reference levels require calibration and less calibration values have to be stored in a memory block, e.g. a look-up table. In particular embodiments of the present invention, the three most significant bits (MSBs) of a binary representation of the B_n's may be selected to define the grid of voltage drop reference levels, resulting in eight discrete voltage drop reference levels for the calibration process. Other voltage drops reference levels may be defined for other embodiments of the present invention, for example voltage drops reference levels which are not equidistant. Furthermore, different rows of pixels may have different voltage drop reference levels, e.g. one row of pixels defines eight such levels and another row of pixels sixteen such levels, or the absolute positions of the voltage drop reference levels may vary from row to row.

[0080] Knowledge of either the supplied voltage (different from the source voltage of the power source 101) or the associated voltage drops at each individual pixel driving circuit of a selected row of pixels thus enables compensation of such (resistive) voltage drops on the corresponding first and second power supply line during use of the display, e.g. in the 'driving mode'. This may be achieved by applying a data compensation signal to the data signal for controlling the driving transistors, via the signal present at the control terminal, of each pixel driving circuit of the selected row of pixels. The driving transistors functioning as voltage controlled current sources, driving current levels through the light emitting elements may be adjusted so as to take into account a voltage drop on the first and second power supply line, e.g. the reduced supply voltage at the pixel driving circuits may be compensated by precisely adjusting the data signals present at the control terminal of the driving transistors. The adjusted data signals or data compensation signals may be obtained from a calibration table, a interpolation table, or a combination thereof as explained hereinafter. As the amount of voltage drop compensation depends dynamically on the number of active pixels/pixel driving circuits of each selected row of pixels and the colour scale under which they are currently operated (high light or low light), it is useful to have a calibration table available so as to quickly determine the required voltage drop compensation signals, which are typically applied as compensated data signals during use, corresponding to the calculated voltage drop of each active pixel/pixel driving circuit. As a consequence of non-uniform fabrication and/or degradation and aging, also voltage drop compensation signals may be different even if equal voltage drops have been calculated for two or more pixel driving circuits, e.g. due to different threshold voltages V_{TH} of their respective driving transistors 301. Another factor which may affect the voltage drop compensation values is the difference in ground "seen" by each circuit element, e.g. the ground defined at the control terminals 302 of each pixel driving circuit. A difference in ground may be caused by voltage drops on the corresponding ground line, e.g. the second power supply line 312. Therefore, a voltage drop compensation unit 109, 119 is regularly calibrated for each circuit element, e.g. each pixel driving circuit, individually, or a calibration table is filled at regular time intervals taking into account the updated calibration values obtained during the calibration process explained hereinafter.

[0081] A 'calibration mode select signal' is sent to the driver system 100, 110 for calibration. In response to this signal, the voltage source(s) 101 are disconnected from the first and second power supply line 107, e.g. by opening the at least one first switching element 103, 104, 113, and the current source(s) 21, 22 of the current generation unit 102, 112 are connected to only one side thereof, e.g. by closing the at least one second switching element 105, 115. All but one pixel driving circuit, x, per row of pixels are then turned off (e.g. by first selecting this row and then writing data signals $< V_{TH}$ to the control terminal 302 of each pixel driving circuit of this row, except for the x-th one) and an injected reference current s_x*I_{ref} is flowing through the first and second power supply line via the x-th pixel driving circuit only. The current generation unit may comprise and use at least two current sources 21, 22 to inject the injected reference current s_x*I_{ref}. For instance, a first current source 21 may accurately generate current levels $LL*I_{ref}$ corresponding to the low light colour scale of pixel x, and a second current source 22 is suitable for accurately generating higher current levels $HL*I_{ref}$ (e.g. current levels that result in a 16 times brighter light output of pixel x) corresponding to the high light colour scale of that pixel x. Providing a first current source 21 and a second current source 22 yields a more accurate control of the current levels for both the low light and the high light colour scale regime. The accuracy with which a pre-determined current level is injected into the each pixel driving circuit being directly proportional to the obtainable accuracy during calibration

of this pixel driving circuit, a more accurate control of the current sources 201, 202 and the related pre-determined current levels is of advantage. Alternatively, a single programmable current source may be used for generating the pre-determined current levels/reference currents, which may result in a more compact current generation unit. For a single-side connection of a power source (e.g. the current source(s) 21, 22 of a current generation unit 102 connected to the left side), a different boundary condition Eq. 11 is used to determine voltage drops, yielding the following expression provided by Eq. 12 for the voltage drop at the n-th pixel driving circuit of a row of pixels if all but the x-th pixel driving circuit of that row of pixels are inactive ("off").

$$I_0 = I_{ref} \sum_{j=1}^{N} b_j s_j \qquad (11)$$

$$\Delta V_{cal}[n] = I_{ref} R_{ref} s_x (M - 1 + \min(x, n)) \qquad (12)$$

$$V_x = V_{cal} - \Delta V_{cal}[x] = V_{cal} - I_{ref} R_{ref} s_x (M - 1 + x) \qquad (13)$$

[0082] In consequence, the voltage V_x applied at the active pixel driving circuit x may be determined according to Eq. 13, provided that a value for the potential 81 (voltage V_{cal}), at which the current generating unit 102 is delivering the current $s_x * I_{ref}$ to the x-th pixel driving circuit, is known. This value may be detected by a readout unit 108, e.g. a voltage sensing device such as, but not limited thereto, one or more voltage comparators electrically connected to an output of the current generation unit 102.

[0083] Referring to FIG. 7, it is explained how the calibration process may be performed in the 'calibration mode' and how a calibrated driver system 100, 110 may proceed to achieve good voltage drop compensation in the 'driving mode'. For each pixel driving circuit x of a row of pixels selected for calibration, the voltage V_x supplied to this x-th pixel driving circuit may be inferred from a voltage value 81 (V_{cal}) detected at the readout unit 108, as demonstrated above. For the purpose of calibration, the detected voltage value 81 is compared to each of the voltage drop reference levels 600 defined for the row of pixels currently undergoing calibration and shifted by an amount $\Delta V_{cal}[x]$, starting for instance with the largest one (e.g. VDD). The shifted voltage drop reference levels may be sequentially applied to the second input 82 of the readout unit 108, e.g. a voltage comparator. The shift $\Delta V_{cal}[x]$ may be neglected in some embodiments, but for more accurate embodiments this shift is taken into account, as it correctly calculates a voltage drop on the first and second power supply line also present during the calibration process. This is of advantage if the pixel count per row is large, causing larger voltage drops. For each (shifted) voltage drop reference level applied to the second input 82 of the readout unit 108, the data signal at the control terminal 302 of the driving transistor 301 of the x-th pixel driving circuit is varied. This variation explores at least locally a response curve of the connected circuit element, e.g. the pixel driving circuit being calibrated, the response of a change in the data signal present at the control terminal 302 being a deterministic change in the potential (voltage) across the same circuit element at a fixed current level. A variation of the data signal may start just above the transistor threshold level (V_{TH}) and then increase gradually to a defined maximum, or vice versa. For a fixed current flowing through the x-th driving transistor and a given data signal at its control terminal, the transistor transfer characteristics define a unique value for the voltage across the transistor (e.g. the drain-source voltage V_{DS} of a TFT). This voltage across the transistor is in general a decreasing function of the data signal at a fixed current flow. The voltage V_x supplied to the x-th pixel driving circuit being the sum of a light emitter voltage and a voltage across the driving transistor, and the light emitter voltage being a known and constant value for a fixed reference current $s_x I_{ref}$, an increasing data signal at the x-th control terminal generates a decreasing supply voltage V_x. Therefore, a variation of the x-th data signal alone (the other driving transistors are "off") is sufficient to cause a variation of the detected voltage value 81. In particular embodiments of the present invention, the detected voltage 81 is decreased in a sweep, until it crosses the currently applied (shifted) voltage drop reference level.

[0084] During the calibration process, the readout unit 108 sends a 'calibration store signal' 72 to an input of a memory block 702, e.g. a calibration look-up table. Non-limiting examples of a 'calibration store signal' 72 are a logic state (e.g. logic low or high), a transition in a logic state, e.g. a rising or falling edge, etc. Taking the exemplary case of a 'calibration store signal' 72 which toggles from high to low at the crossing point, e.g. voltage signal 81 equals (shifted) reference signal 82, the memory block 702, when detecting the 'calibration store signal' going low at one of its inputs, will store a value representative of the x-th data signal at the crossing point at a location addressed by an address signal 71. In general, the address signal 71 is given as the reference level count, but a more detailed address signal 71 may also include the pixel count x and/or the colour scale index s_x ('HL' or 'LL'). The representative value of the x-th data signal may be provided by a dedicated counter 701 which is also connected to an input of the memory block 702 and which counts, for instance, the number of discrete steps by which the x-th data signal has been increased so far in a stepped

sweep. Writing of the counter value into the memory block 702 may be enabled as long as the 'calibration store signal' is high and may be disabled if the 'calibration store signal' is going low. This has the effect of storing the representative value, in this case the counter value, in the memory block 702. Thereafter, the counter 701 may be reset, the following (shifted) voltage drop reference level may be applied to the second input 82 of the readout unit 108, and an address signal 71 for pointing to a storage location in the memory block 702 is updated, e.g. to the next reference level count.

[0085] The memory block 702 outputs at least two stored representative values 73, 74 when receiving a read query, which may be the address signal 71 presented to one of its input ports. If the address signal 71 includes the voltage drop reference level count 'n' (reference level index n), the first of the at least two stored representative values 73 may be the representative value of the x-th data signal (e.g. the counter value) obtained for the voltage drop reference level count 'n' and the second of the at least two stored representative values 74 may be the representative value of the x-th data signal (e.g. the counter value) obtained for the voltage drop reference level count 'n+1'. The at least two stored representative values 73, 74 are transmitted to an interpolation unit 703. During calibration, the interpolation unit 703 just passes the first of the at least two stored representative values 73 to a sum unit 704. This may be obtained by setting an additional 'interpolation point input' 75 of the interpolation unit 703 to zero. The sum unit 704 adds an output received from a ground voltage drop multiplication unit 705 to the output received from the interpolation unit 703 and passes the result to a first input (with address code '1') of a multiplexer 706. A constant '1' is applied as a multiplex address signal 76 to the multiplexer 706 during the entire calibration process. Therefore, the result of the sum unit 704 is directed to the data line driver 201. As long as the 'calibration store signal' 72 does not transition to low in this particular embodiment, the counter values of the counter 701 are repeatedly updated in and output by the memory block 702. During calibration, the interpolation unit 703 is just passing the updated counter values read from the memory block 702 and so does the multiplexer 706. Ignoring the contribution of the ground drop multiplication unit 705, this has the effect that the data line driver 201 repeatedly receives an increasing counter value, which the data line driver 201 converts into a stepwise increasing data signal for the x-th pixel driving circuit undergoing calibration. This closes the loop of events described above. Once the detected voltage signal 81 falls below the (shifted) voltage drop reference level applied to the second input 82 of the readout unit 108, the updating of the counter values in the memory block 702 stops. Thus, an exit point from the loop exists. The ground voltage drop multiplication unit 705 takes into account and compensates for the differences in ground which may exist between the potential at the x-th control terminal 302 determined by the x-th data signals provided via data lines and the potentials at the x-th driving transistor 301 terminals (terminals through which the driving or reference current is flowing) determined by the voltage drops on the second power supply line (e.g. the power supply line connecting to a common GND of the power source 101). In other words, a data signal applied at the control terminal 302, which may be a data compensation signal, e.g. a compensated data signal, is only relevant with respect to its local ground, which for each pixel driving circuit is the contact point 307 on the second power supply line 312. During calibration, this correction may be neglected. Alternatively, it may be included and determined as a fixed fraction of the total voltage drop $\Delta V_{cal}[x]$ during calibration. Said fixed fraction of the total voltage drop may be inferred by direct measurements on the (circuit) mask. For particular embodiments of the present invention it may be substantially equal to one half (e.g. $B_n/2$), assuming that the first and the second power line 311, 312 have substantially identical material properties and geometrical dimensions, e.g. the same width. Therefore, $\Delta V_{cal}[x]$ may be used as an input 77 to the ground drop multiplication unit 705.

[0086] When the calibration process is finished, the 'calibration mode select mode' signal may be disabled and the 'driving mode select' signal applied for toggling the display back into the driving mode. As a result of the calibration process, the memory block 702 has been filled or updated with new representative (calibration) values for the data signals. The voltage drop compensated data signals for driving the data lines during use of the display are obtained as described hereinafter.

[0087] A binary string representing the calculated B_n's for each pixel driving circuit of a selected row of pixels is split into a MSBs section and a LSBs section, e.g. the three most significant bits of the B_n's are kept in the MSBs section and the rest is assigned to the LSBs section. This split may be performed by the voltage drop calculation unit 30. The bits of the MSBs section are used together with the pixel count and the colour scale indicator to form a query address signal 71 for the memory block 702. In response to this query, the memory block 702 reads and outputs the at least two stored representative (calibration) values 73, 74 at this address, which may correspond to the stored counter values for the voltage drop reference level with index equal to the MSBs string section and to the voltage drop reference level with index equal to the MSBs string section increased by one. These at least two stored representative (calibration) values 73, 74 are passed to the interpolation unit 703 for which they serve as lower and upper known calibration data point in the interval for which interpolation is sought. As a matter of fact, if the LSBs string section applied to the 'interpolation point input' 75 of the interpolation unit 703 is zero, the lower known calibration data point is passed to the sum unit 704. If the applied LSBs string section is non-zero instead, a more accurate representative (calibration) value is interpolated at the point inside the interpolation interval requested by the signal applied to the 'interpolation point input' 75, e.g. the LSBS string section. Fast linear interpolation or more accurate higher order interpolation (with more than two stored representative values as input) may be used. The interpolated representative (calibration) value is passed to the sum

unit 704 which applies an offset depending on the voltage drop fraction of the second power supply line and pixel to be compensated. The voltage drop fraction is inferred from the B_n's applied to the input 77 of the ground drop multiplication unit 705. The interpolated representative (calibration) value with ground voltage drop offset applied is passed to the multiplexer 706 and is directed to the data line driver 201 if the binary data bit b_i associated with the compensated pixel driving circuit is '1', e.g. the associated pixel driving circuit is "on". The sequence of binary data bits b_i is typically generated by the image interface unit 207, or may be passed forward by the image interface unit 207 if the binary data bit sequence has been generated by other dedicated hardware modules, and represent frames or sub-frames (e.g. grey scale PWM contributions/slots). In contrast, if the binary data bit b_i associated with the compensated pixel driving circuit is '0', e.g. the associated pixel driving circuit is "off", the multiplexer address signal 76 is also '0' and a zero is selected at the other multiplexer input and directed to the data line driver 201. Thus, the data line driver 201 ensures that the associated pixel driving circuit is "off" by applying a data signal below a threshold value (V_{TH}) of its driving transistor.

[0088] The voltage drop compensation unit 109 may form a compact hardware block which may be part of the image interface unit 207 in some embodiments of the present invention.

[0089] This calibration process is typically performed for each pixel driving circuit of the row of pixels selected for calibration and for each of the at least two colour scales 'HL' and 'LL'. Rows of pixels may be sequentially selected for calibration.

[0090] The calibration process may be performed in real-time. This may be achieved by determining the representative values of the data signals and storing them in the memory block 702 during empty PWM slots. PWM slots may be empty if an even number of time slots is allocated for driving the data line(s) but the duty cycle of the PWM encoded data signals is composed of dyadic fractions of a unit time interval (e.g. the full PWM period). Alternatively, the calibration process may be performed at the time the display is turned on and/or at regular time intervals during use.

[0091] Although the methods for calculating and compensating voltage drops and for calibration have been described for a single pair of power supply lines, e.g. the first and second power supply line of a row of pixels, they also apply to other pairs of power supply lines supplying power to other rows of pixels of an active matrix display. The methods for calculating and compensating voltage drops and for calibration may be implemented in hardware such that they are performed for a single row of pixels of an active matrix display at a time. Alternatively, the methods for calculating and compensating voltage drops and for calibration may be implemented in hardware such that they are performed for multiple rows of pixels of an active matrix display concurrently. For the latter case, dedicated power sources, current generating unit as well as at least one first and second switching element are provided for each of the concurrently active rows of pixels.

EXAMPLE

[0092] The method has been implemented on a hardware platform for testing and verification, in the present example on a Xilinx FPGA. The FPGA board allowed real-time computation of resistive voltage drops for two distinct brightness scales (increased colour depth), here the high-light and low-light signals, realized through two distinct driving current levels. A 12-bit wide PWM scheme was used to encode the grey values of both the high-light and the low-light signal, yielding a combined 16-bit dynamic range of light output on a display the intrinsic RC delays of which only support a 12-bit PWM driving signal. Driving current levels of the light emitting elements, e.g. OLEDS, have been fixed relatively to each other such that the light output or brightness of the associated display pixel is larger by a factor 16 for the high light driving current level as compared to the low light driving current level.

[0093] Only one clock cycle (e.g. 5 ns for a 200 MHz clock rate) is needed to accurately determine the (resistive) voltage drops on the first and second power supply line for the row of pixels which is next to drive. From Eq. 10 it is seen that a recursively calculated resistive voltage drop B_n is obtained by performing a single multiply and accumulate operation, which can be done very efficiently within one clock cycle by a suitable hardware block. After only seven clock cycles the data line driver is ready to communicate data signals on the data lines to the pixel driving circuits of the selected row of pixels, e.g. by writing data signals to the control terminal of the driving transistors (e.g. gates) and/or storing them on the (storage) capacitors. Therefore, a real-time determination of the voltage drops on the first and second power supply line and a corresponding voltage drop compensation is obtained. This example demonstrates that good brightness control and uniformity are achieved in real-time, via compensation and calibration techniques, for an active matrix pixel display even for increased colour depths.

[0094] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. The foregoing description details certain embodiments of the invention. It will be appreciated, however, that no matter how detailed the foregoing appears in text, the invention may be practiced in many ways. The invention is not limited to the disclosed embodiments, but by the claims.

Claims

1. A driver system (100, 110) for driving pixels of a display, the driver system comprising:

   - at least one power supply line pair comprising first and second power supply lines (311, 312), each power supply line pair comprising an ordered sequence of contact point pairs (306, 307) distributed over its length;
   - a plurality of circuit elements (300, 400), each circuit element being connected to a couple of contact points (306, 307) for making an electrical connection between the first and the second power supply lines (311, 312), and to a data line (313) for receiving data signals, and each circuit element being adapted for being driven at pre-determined current levels through its corresponding couple of contact points (306, 307), there being at least three such pre-determined current levels selectable via a received data signal;
   - a voltage drop calculation unit (30) for calculating voltage drops over the power supply lines at the level of each connected circuit element, when driven so as to deliver a pre-determined current level, a voltage drop causing a deviation of the actually delivered current levels from their pre-determined values;
   - at least one voltage drop compensation unit (109, 119) for compensating the calculated voltage drops at each connected circuit element by providing a data compensation signal to the at least one data line (313).

2. A driver system according to claim 1, wherein the at least three pre-determined current levels comprise exactly two pre-determined non-zero current levels and a third, substantially zero current level.

3. A driver system according to any of the previous claims, further comprising at least one power supply unit (10, 11) operably connected to the at least one power supply line pair for powering each of the connected circuit elements, wherein the at least one power supply unit is a switchable power supply unit adapted for switching between a driving mode and a calibration mode.

4. A driver system according to claim 3, further comprising at least one readout unit (108) electrically coupled to the at least one switchable power supply unit for detecting a power supply signal (81) in the calibration mode and comparing it to a reference (82).

5. A driver system according to claim 4, wherein the reference is a set of pre-determined voltage drop levels (600).

6. A driver system according to any of claims 4 or 5, further comprising a memory block (702) for storing representative calibration values as a result of comparison with a reference in calibration mode and for retrieving stored representative calibration values in driving mode.

7. A driver system according to claim 6, further comprising an interpolation unit (703) for interpolating between at least two retrieved stored representative calibration values (73, 74) in driving mode.

8. A driver system according to any of claims 3 to 7, wherein the at least one power supply unit comprises a current generation unit (102, 112) including at least two current sources (21, 22).

9. A driver system according to claim 8, wherein a ratio of currents generated by the at least two current sources is fixed.

10. A driver system according to any of the previous claims, furthermore comprising a plurality of data lines and at least one data line driver (201) for providing data signals on the plurality of data lines, wherein each circuit element comprises a driving transistor (301), a control terminal (302) of which is connectable to one of the plurality of data lines.

11. A driver system according to claim 10, wherein the driving transistors are operated in the linear region.

12. A driver system according to any of claims 10 or 11, wherein the at least one data line driver is suitable for providing pulse width modulated data signals on the plurality of data lines.

13. An active matrix display for displaying images, the active matrix display comprising a driver system according to any of the previous claims, wherein the plurality of circuit elements (300, 400) are formed by a plurality of pixel driving circuits, each pixel driving circuit comprising at least one light emitting element (303).

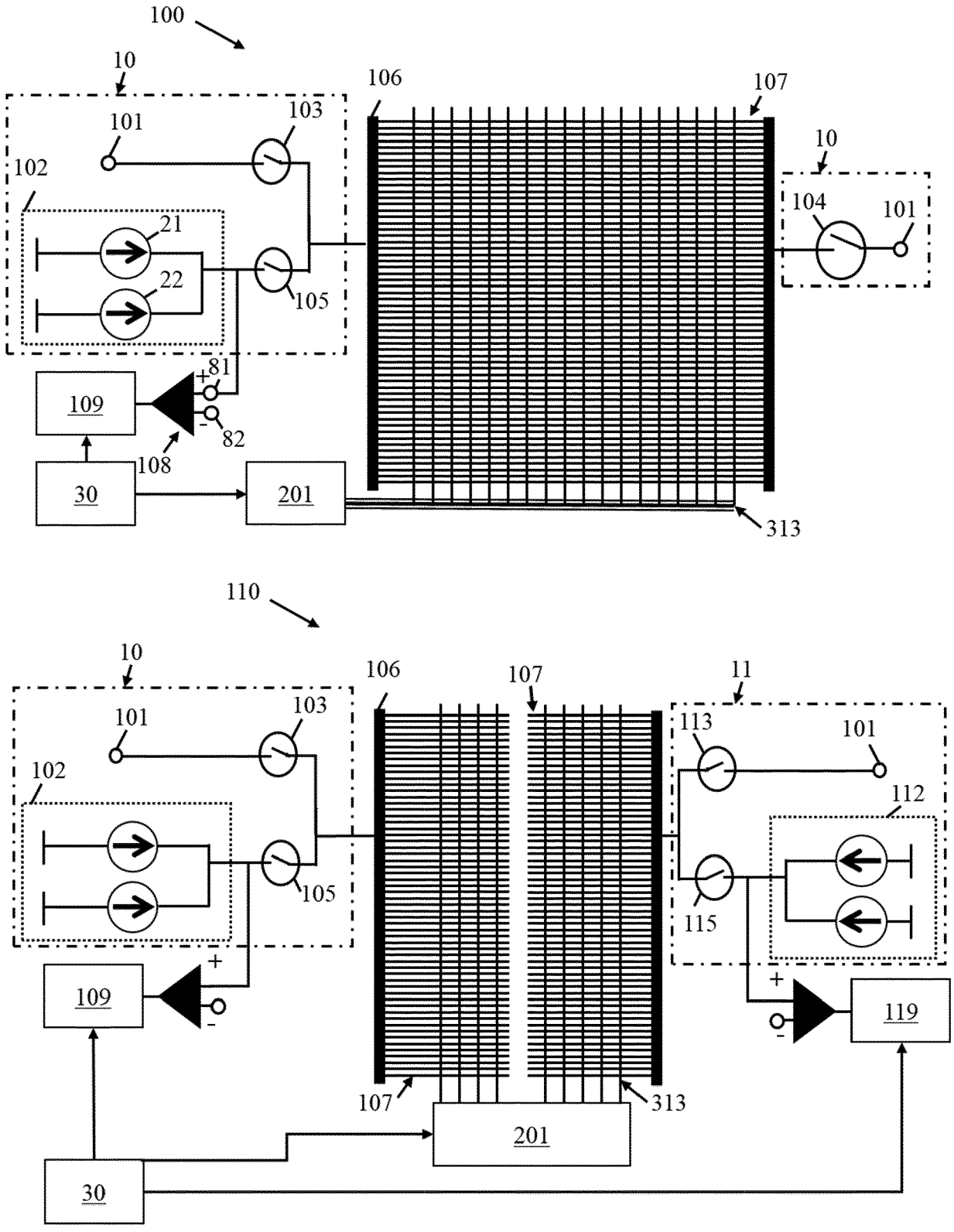
14. A method of compensating voltage drops on a power supply line pair comprising:

- calculating voltage drops for contact point pairs (306, 307) placed along a power supply line pair (311, 312) assuming a pre-determined current level flowing between each contact point pair, a pre-determined current level being selected from a set of at least three distinct values, one of which is substantially zero;
- determining voltage drop compensation signals which, when applied to control terminals (302) of circuit elements, each connected to a contact point pair, cause a deviation of current levels from said pre-determined current levels to be reduced;

wherein voltage drop compensation signals are determined using the calculated voltage drops as inputs.

15. A method according to claim 14, wherein voltage drop compensation signals are determined further using calibrated response curves of connected circuits elements as inputs, a calibration of each response curve comprising the steps of:

- providing a current at one of said pre-determined but non-zero current levels to the single connected circuit element whose response curve is being calibrated by injecting it into a power supply line of the power supply line pair;
- applying a pre-determined substantially zero current level to all of the remaining connected circuit elements;
- detecting a voltage signal (81) at one end of the power supply line pair;
- comparing the detected voltage signal to a reference (82);
- increasing a voltage drop compensation value applied to a control terminal (302) of the circuit element being calibrated if comparing the detected voltage signal to a reference yields a first outcome, or
- memorizing a representative calibration value of the voltage drop compensation value applied to a control terminals (302) of the circuit element being calibrated if comparing the detected voltage signal to a reference yields a second outcome.


100
10
101
103
102
21
22
105
106
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104
101
81
+
-
82
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201
313
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101
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+
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109
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201
30

FIG. 1

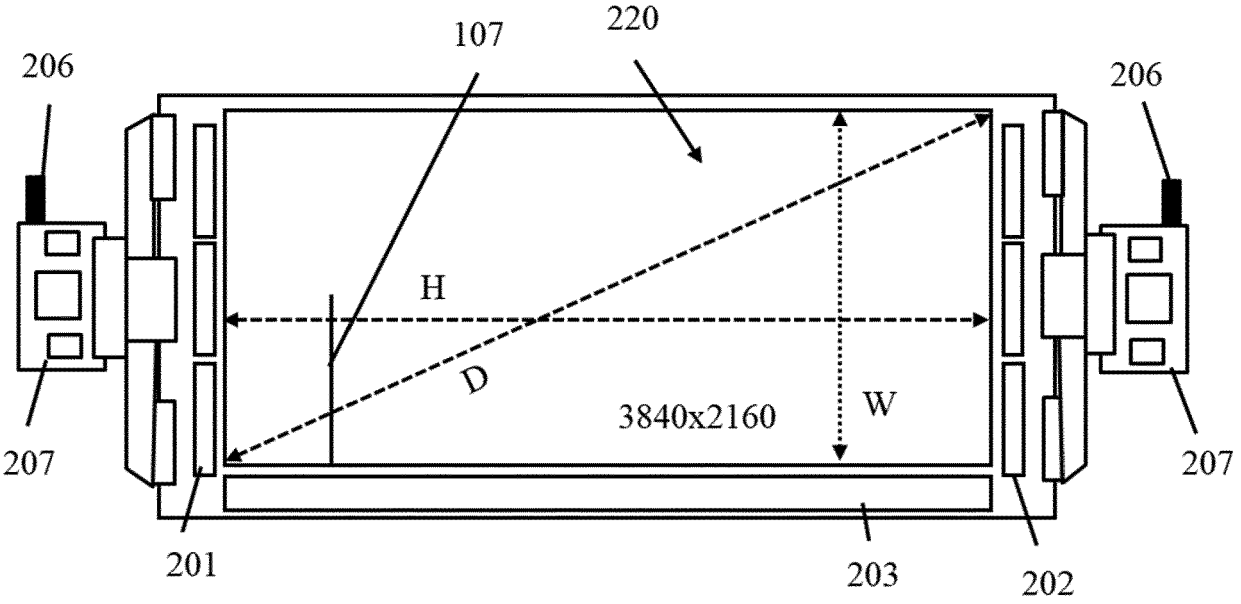
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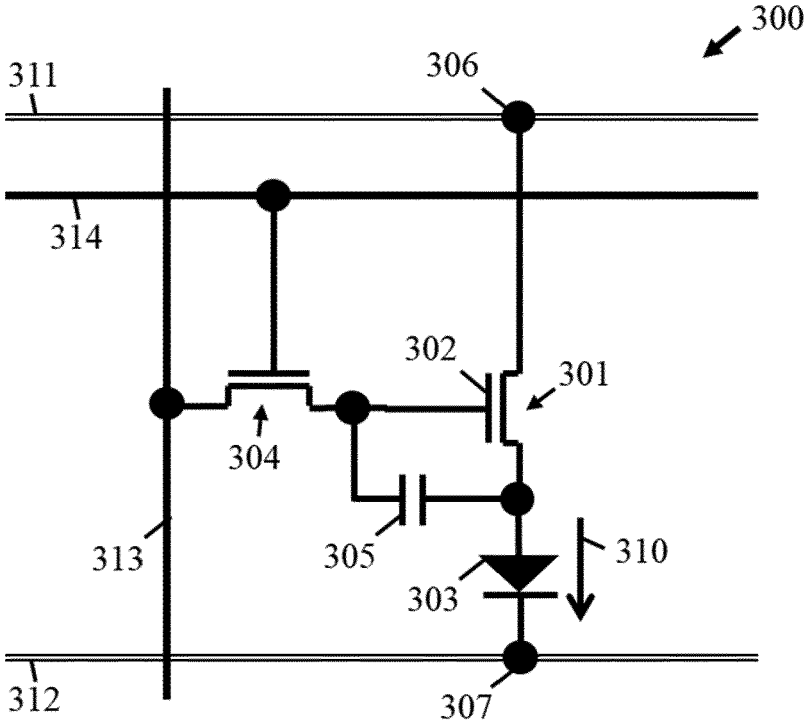
FIG. 2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313
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310
303
312
307

FIG. 3

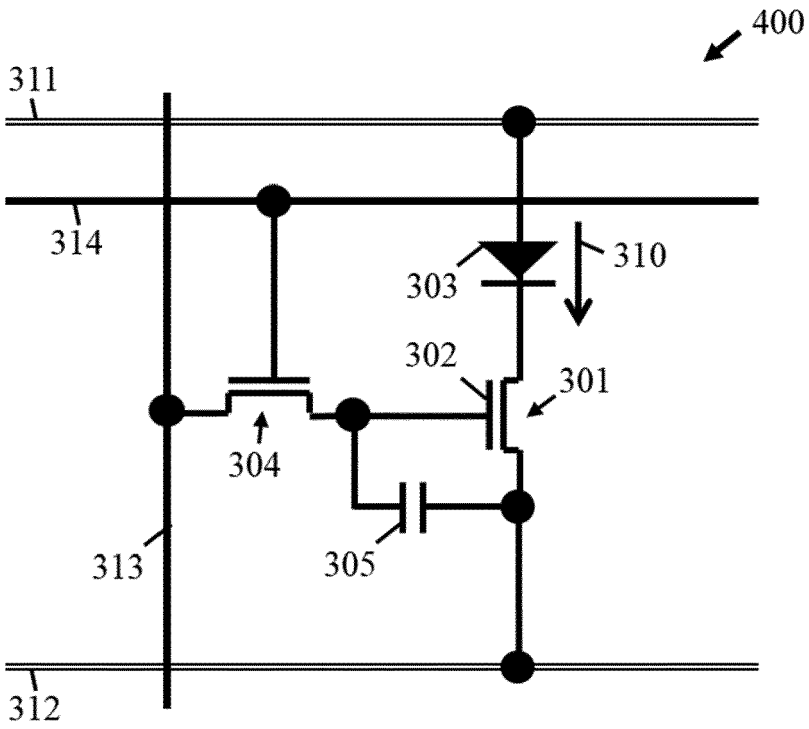
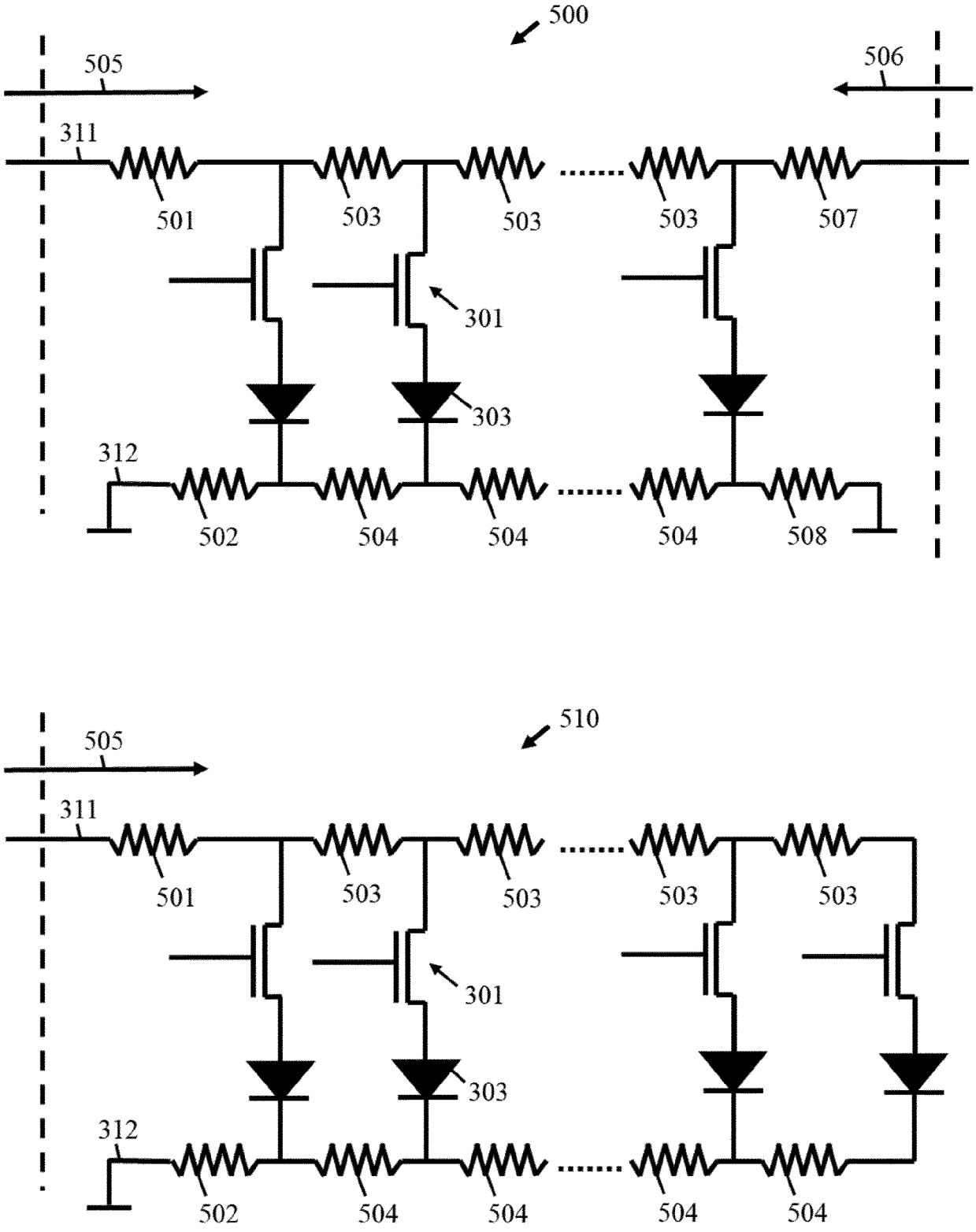


FIG. 4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504
504

FIG. 5

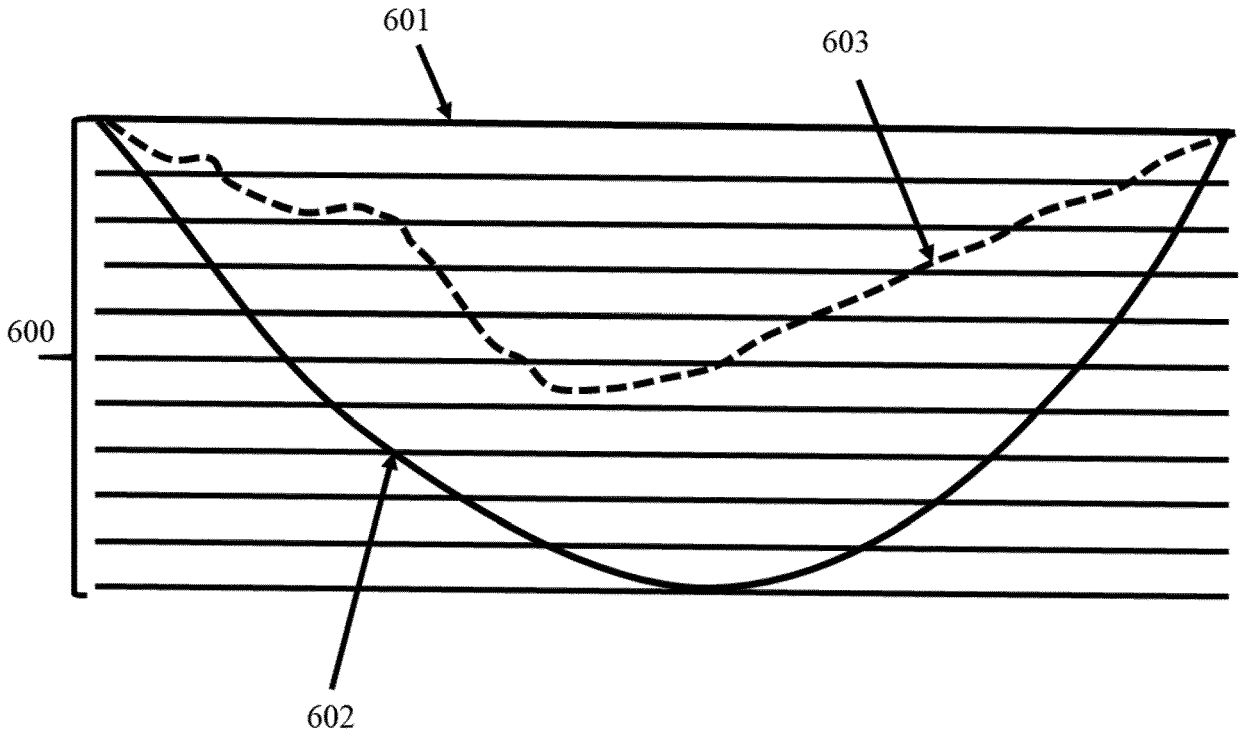
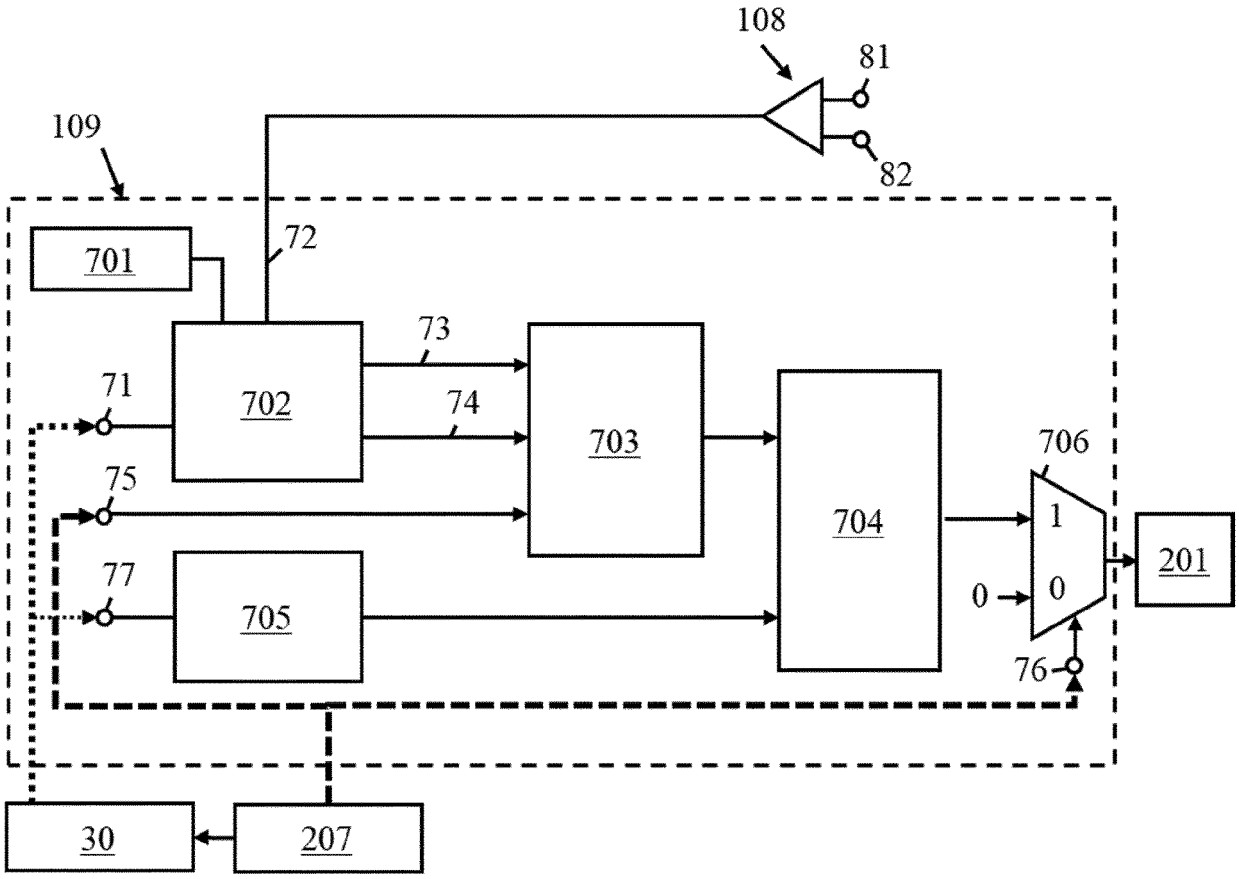


FIG. 6


108
81
82
109
701
72
73
71
702
74
703
706
75
704
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201
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705
0
0
76
30
207

FIG. 7

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European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 18 18 0080

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	EP 3 319 075 A1 (IMEC VZW [BE]; UNIV LEUVEN KATH [BE]) 9 May 2018 (2018-05-09) * figures 1,6,9 * -----	1-15	INV. G09G3/3208

TECHNICAL FIELDS SEARCHED (IPC)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	27 September 2018	Gundlach, Harald

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