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Amended claims in accordance with Rule 137(2) EPC.

(54) **VOLTAGE REGULATION CIRCUIT**

(57) A voltage regulator (10) configured to regulate an input voltage (V_{DD}) to a predetermined regulated output voltage (V_{OUT}) is described. The regulator comprises a voltage reference (20), a controlling and regulating element (70, 80) connected to the voltage reference (20) and a programmable array (50) of output elements (55a-c) for generating a load current (Ii) on an output. The input of the programmable array (50) is connected to an output (44) of the controlling and regulating element (70, 80) and the output of the programmable array (50) is connected to an input of the controlling and regulating element (70, 80).

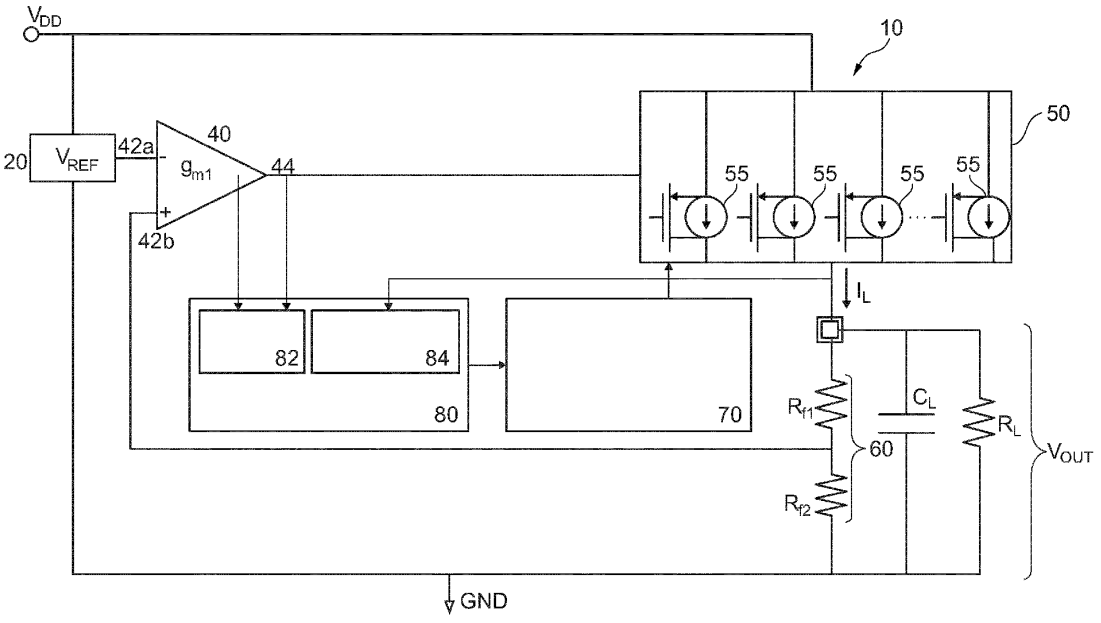


Fig. 1

EP 3 594 773 A1

Description

Cross-Reference to Related Applications

[0001] None

Field of the Invention

[0002] The invention relates to a voltage regulation circuit which is configured to regulate an output voltage.

Background to the Invention

[0003] A voltage regulator is an electronic circuit that provides a stable output DC voltage which is independent of load current (I_L). A low-dropout (LDO) regulator is an example of the voltage regulator that regulates the output voltage, even when the supply voltage (V_{DD}) is very close to the output voltage (V_{OUT}). One of the issues related to the use of the voltage regulators is that the voltage regulator needs to dissipate power and thus heat across the voltage regulator in order to regulate the output voltage. This dissipation of power and heat can lead to problems with the stability of the voltage regulator. The LDO regulator, due to its reduced voltage dropout, limits its internal power dissipation and has therefore an overall better power efficiency.

[0004] Examples of prior art voltage regulation techniques include a circuit shown in US Patent Application 2017/0063231 which shows an analog-to-digital converter receiving a reference voltage and an output voltage of the voltage regulator. The analog-to-digital converter provides a digital error signal which is used to provide a digital control signal that is in turn used to control a power stage.

[0005] Other examples of voltage regulators are taught in the publications by C.K.Chava, J.Silva-Martinez, "A Frequency Compensation Scheme for LDO Voltage Regulators", IEEE Transactions on Circuits and Systems, Vol. 51, No. 6, June 2004, pp. 1041-1050, and R.J.Milliken, J.Silva-Martinez, E.Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator", IEEE Transactions on Circuits and Systems, Vol. 54, No. 9, Sept. 2007, pp. 1879-1890.

[0006] The accuracy of the voltage regulators known in the art is currently limited by several factors. These include the overall limited open loop DC gain of the voltage regulator when its error amplifier is cascaded with a pass element output stage. This is illustrated in Fig. 3 which illustrates a simplified model of voltage regulator having an output voltage $V_{OUT} = V_L = Vin-$ and input voltage V_{REF}. It is known that $V_{OUT} = Vin- = A(Vin+-Vin-)$, where A is the gain of the amplifier. For an insufficient DC gain, for example 50dB gain, A=250 and $V_{out} = 0.996\ V_{in}+$. As a result, for a nominal reference voltage V_{REF} of 5 V, the output voltage V_{OUT} will be 4.98V. In other words, this prior art voltage regulator has a 20mV error.

[0007] The overall limited, insufficient DC gain can occur, for instance, when the output stage pass element transistor transitions from a saturation region (i.e. the region in which the gate-source voltage minus the threshold voltage is lower than the drain-source voltage) into a triode region (in which the gate-source voltage minus threshold voltage $V_{t,p}$ is higher than the drain-source voltage) due to high current drawing, thus causing a reduction of the transconductance gain of the output stage pass element transistor.

[0008] Another factor limiting accuracy is shown in Fig. 4 which illustrates the existence of systematic offsets due to "perturbations" in the operating point. At low output currents, the PMOS pass element 400 due to its large size is almost off. Then the gate-source voltage Vgs of the pass element 400 nearly equals its threshold voltage $V_{t,p}$, which is forced to the output of the right branch 410r of the PMOS cascode 410. The effect is to "squeeze" the right branch 410r of the PMOS cascode 410 and thus create an imbalance of the cascode 140 and results in an offset current I_c-ΔI_c which is equivalent to an input offset voltage $V_{off}=\Delta I/gm$ = 20 mV drop. Moreover, the cascode 410 does not operate properly, resulting again in a reduction of the DC gain due the lowered output impedance.

[0009] Another example of a prior art circuit is shown in Fig. 5 which illustrates the stability of the prior art voltage regulator versus the output load current (I_L). The second stage (output stage) is the dominant pole ($\omega p2$) and the first stage is the non-dominant pole ($\omega p1$). The value of $\omega p1$ is given by

$$\omega p1 \approx \frac{1}{R1(C1 + gm, pass(rds \,||\, (Rf1 + Rf2) \,||\, RL)Cgd, pass)}$$

and the value of $\omega p2$ by

$$\omega p2 \quad \frac{1}{(rds \,||\, (Rf1 + Rf2) \,||\, RL)CL}$$

[0010] The value of the second-stage dominant pole $\omega p2$ moves to a higher frequency for higher loads I_L, because the output resistance rds of the pass transistor decreases at higher currents due to channel modulation effect.

[0011] At higher load current I_L, $\omega p2$ moves to a higher frequency and as $\omega p2$ approaches the value of $\omega p1$, the voltage regulator shown in Fig. 5 becomes unstable.

[0012] In order to overcome these issues, here is therefore a need to provide an improved voltage regulator.

Summary of the Invention

[0013] This document describes a voltage regulator which is configured to provide a regulated output voltage from a supply voltage. The voltage regulator of this disclosure has an internal sensor for sensing the load current and output voltage and is able to adjust automatically and dynamically the size of a pass element, to provide an accurate, stable, regulated output voltage, by ensuring high internal DC loop gain and regulator stability. More particularly, the voltage regulator comprises a voltage reference V_{REF} and a regulator monitor with a voltage monitor and a current sensor. A programmable array is used as the pass element and comprises a plurality of output elements for generating a load current. The programmable array is connected to the output of the regulator and controlled by the regulator itself. The output of the programmable array is connected to an input of the regulator for feedback. The regulator monitor monitors both the voltage and the output load current on the output of the voltage regulator.

[0014] The use of a plurality of output elements as the pass element enables the regulator monitor to switch different ones of the pass elements on and off in order to change the output current to maintain the regulated output voltage. This provides a versatile voltage regulator that is accurate and can provide a wide range of load currents. It requires no compensation circuits.

[0015] The regulator monitor comprises a first comparator and a second comparator, an up-down counter connected to the outputs of the first comparator and the second comparator, and a decoder. An output of the up-down counter is connected to an input of the decoder and a plurality of decoder outputs are connected to a plurality of switches of the programmable array.

[0016] In one aspect, the programmable array comprises a plurality of field effect transistors (pass elements) that are connected to ones of the plurality of the switches in order to activate or deactivate one or more of the plurality of field effect transistors. The field effect transistors may have differing channel lengths and widths so that they could provide different current contributions to the load current.

[0017] A method for regulating an output voltage is also taught in this document. The method comprises sensing at least one of the load current or the output voltage using a regulator monitor and comparing the sensed one of the load current or the output voltage with a reference value. An output value based on the comparing is passed to a controller and the controller via the switches activates one or more of a plurality of output elements in the pass element (programmable array) to control the internal operating points for regulating the output current. The number of activated transistors of the plurality of output elements is dependent on the output value of the current monitor.

[0018] The output value of the current monitor is in one aspect a digital value and is passed to an up-down counter, wherein the value of the up-down counter is changeable depend on the comparison result.

[0019] The voltage regulator of this document has numerous applications, such as power-battery management circuits, microcontrollers, RF transceivers, and other applications.

Description of the drawings

[0020]

Fig. 1 shows an architectural overview of a circuit for the voltage regulation circuit of this document.
Fig. 2 shows an example of a topology for the voltage regulations circuit.
Fig. 3 shows a simplified prior art example of an amplifier.
Fig. 4 shows an example of a circuit with perturbations of its operating point.
Fig. 5 shows an example of a circuit illustrating in general the stability problem of a prior art regulator.
Fig. 6 shows an outline of the method for changing the load current depending on the current change.
Fig. 7 shows an outline of the method for changing the load current depending on the change in the output voltage.

Detailed description of the invention

[0021] The invention will now be described on the basis of the drawings Fig. 1 to Fig. 7. It will be understood that the embodiments and aspects of the invention described herein are only examples and do not limit the protective scope of the claims in any way. The invention is defined by the claims and their equivalents. It will be understood that features of one aspect or embodiment of the invention can be combined with a feature of a different aspect or aspects and/or

embodiments of the invention.

[0022] Fig.1 shows an overview of a voltage regulation circuit 10, which is configured to supply from an input supply voltage V_{DD} a predetermined regulated output voltage V_{OUT} across a resistor R_L. The voltage regulation circuit 10 comprises a voltage reference V_{REF} 20, which is connected between ground and the input voltage V_{DD}. The output of the voltage reference V_{REF} 20 is connected to an inverting input 42a of an error amplifier 40. It will be appreciated that the voltage reference V_{REF} 20 is shown only schematically in this Fig. 1 as a block. The source of the voltage reference V_{REF} 20 could be an externally generated value or an internal circuit and the exact implementation is not limiting of the invention.

[0023] The output 44 of the error amplifier 40 is connected to a programmable array 50 of voltage controlled current sources 55, which form commonly a pass element. The output of the programmable array 50 is a current I_L which is passed to a first voltage divider 60 (formed by the resistors R_{f1} and R_{f2}), as well as to a load capacitor C_L and load resistor R_L.

[0024] The programmable array 50 is controlled by a controller 70. The controller 70 is connected to a regulator monitor 80 which has a voltage monitor 82 and a load current sensor 84. The voltage monitor 82 receives an output signal from the error amplifier 40 and the load current sensor receives the value of the load current I_L from the output of the programmable array 50. The controller and the regulator monitor collectively form a controlling and regulating element.

[0025] An exemplary topology of the voltage regulator 10 is given in Fig. 2. It will be appreciated that identical elements in Fig. 1 are given identical reference numerals in Fig. 2.

[0026] It will be seen that the load current sensor 84 shown in Fig. 1 comprises a sensing FET 100 (through which a sensing current I_{sense} passes) as well as a pass FET 105 (through which a reference current I_{REF} passes). The sensing FET 100 and the pass FET 105 are substantially identical, and the gate of the sensing FET 100 and the gate of the pass FET 105 are both connected to each other and to the output 44 of the error amplifier 40. The reference current I_{REF} passes through the pass FET 105 to the first voltage divider 60. The channel of the sensing FET 100 is connected to a second voltage divider 62 and so the current from the channel of the sensing FET 100 passes to the voltage divider 62 when the voltage on the gate of the sensing FET 100 is off, i.e. there is no output from the error amplifier 40. It will be noted that the values of the resistors in the first voltage divider 60 and the second voltage divider 62 are substantially identically such that the output of the first voltage divider 60 and the second voltage divider 62 is designed to be equivalent to the reference voltage V_{REF}. The output of the second voltage divider 62 is connected to two comparators 110a and 110b, as well be explained later

[0027] The output of the second voltage divider 62 is connected to the non-inverting input of the first comparator 110a and to the inverting input of the second comparator 110b. The inverting input of the first comparator 110a is connected to a voltage which is equivalent to the reference voltage V_{REF} with a small offset ΔV. This has the effect that whenever the output voltage of the second voltage divider 62 exceeds the value of ΔV then an output UP pulse is output from the first comparator 110a and passed to an up-down counter 120. The function of the up-down counter 120 will be explained later.

[0028] Similarly, the output of the second voltage divider 62 is passed to the inverting input of the second comparator 110b. The input on the non-inverting input of the second comparator 110b is equal to the reference voltage less a small offset ΔV. This means that whenever the voltage at the output of the second voltage divider 62 falls below the value of the offset ΔV, then an output DOWN pulse is output from the second comparator 110b and passed to the up-down counter 120.

[0029] The up-down counter 120 receives the UP pulse from the first comparator 110a and the DOWN pulse from the second comparator 110b and outputs a value to a k-bit decoder 130. The k-bit decoder 130 has as an input a digital value that it converts to a binary output. The output of the k-bit decoder 130 is provided to a plurality of lines 135 which have signals on them dependent on the binary value of the digital value in the k-bit decoder 130. It will be seen that the plurality of lines 135 are connected to a plurality of switches 53a-53c in the programmable array 50. The switches 53a-53c are connected to gates of a plurality of field effect transistors 57a-57c forming the current sources 55 of the programmable array 50.

[0030] The field effect transistors 57a-57c in the programmable array 50 are shown implemented as PMOS transistors in this Fig. 2. It will be seen in this illustrated aspect that the different ones of the pMOSFET transistors 57a-57c in the programmable array 50 each have a different channel width and length, which differ by a factor of 2, but this difference is not limiting of the invention. It would be possible for the different ones of the pMOSFET transistors 57a-57c to have different channel widths and lengths that do not differ by a factor of 2. In practice, the individual pMOSFET transistors 57a-57c will be formed from one or more cells in order to achieve the different current passages.

[0031] It will be appreciated that when the differences in size of the channels in the pMOSFET transistors 57a-57c differ by a factor of two, then the programmable array 50 forms a current steering digital to analog converter.

[0032] The size of the single unit transistor (W/L) in the cell(s) is chosen such that the gate-source voltage V_{gs} is equal to the bias voltage of the output state when the voltage regulator 10 is in a quiescent mode, i.e. there is no load current. In this quiescent mode, the current passing through the single unit transistor will be equal to the reference current I_{REF}

in the voltage divider 60.

[0033] In operation, therefore, the k-bit decoder 130 sends the signals over the plurality of lines 135 to the gates of the field effect transistors 57a-57d, which then switches in the current sources 57a-c to increase the load current I_L across the resistor R_L.

[0034] The operation of the voltage regulator 10 will now be described with respect to Figs. 6 and 7. Fig. 6 shows the operation to sense the change in the load current I_L and Fig. 7 shows the operation to sense the change in the output voltage V_{OUT}.

[0035] In a first step, the load current I_L will be sensed in step 600 and a change will be determined in step 610. Should the load current increase, then the gate source voltage V_{gs} on the pass FET 105 will increase and the sensing current I_{sense} will also increase. this increase will be determined in step 620 in the first comparator 110a and an UP pulse passed to the up-down counter in step 625. The value in the k-bit decoder 130 will increase by one in step 630 and this will be reflected by a change in signals on the plurality of lines 135 in step 645. One of more of the switches 53a-53c in the programmable array 50 will be switched on or off in step 650 to change which ones of the current sources 55a-55c will continue to supply current to the output current I_L in step 655 and enable additional ones of the current sources 55a-55c to be switched in.

[0036] If on the other hand, the load current I_L decreases then the opposite happens. In step 635 the second comparator 110b will output a DOWN pulse due to the decrease in the sensing current I_{sense} and pass this DOWN pulse to the up-down counter 120 in step 640. The value in the k-bit decoder 130 will be decreased by one in step 642 and this will be reflected by a change in the signals on the plurality of lines 135 in step 645. As above, one or more of the switches 53a-53c in the programmable array 50 will be switched on or off in step 650 to change which ones of the current sources 57a-57c will continue to supply current to the output current I_L in step 655.

[0037] It is also possible to use regulation circuit 10 to monitor the output voltage V_{OUT}. In this aspect of the invention, the output voltage V_{OUT} is sensed in a first step 700 and a change will be determined in step 710 in voltage monitor 82. If it is found in 710 that the voltage V_{OUT} has increased 720, then an UP pulse is generated in step 725 and passed to the up-down counter in step 725. The value in the k-bit decoder 130 will increase by one in step 730 and this will be reflected by a change in signals on the plurality of lines 135 in step 745. One of more of the switches 53a-53c in the programmable array 50 will be switched on or off in step 750 to change which ones of the current sources 55a-55c will continue to supply current across the load resistor R_L to change the output voltage V_{OUT} in step 755.

[0038] If on the other hand, the output voltage V_{OUT} decreases then the opposite happens. In step 735 the second comparator 110b will output a DOWN pulse due to the decrease in the output voltage V_{OUT} and pass this DOWN pulse to the up-down counter 120 in step 740. The value in the k-bit decoder 130 will be decreased by one in step 742 and this will be reflected by a change in the signals on the plurality of lines 135 in step 745. As above, one or more of the switches 53a-53c in the programmable array 50 will be switched on or off in step 750 to change which ones of the current sources 57a-57c will continue to supply current across the load resistor R_L in step 755.

[0039] In the aspect shown in Fig. 2, the voltage monitor 82 is also implemented using the sensing FET 100 and the pass FET 105 as will now be explained. Suppose that the output voltage V_{OUT} across the load resistor RL increases. This will be due to an increase in the output current I_L The gate-source voltage of the pass FET 105 will then increase and, as this pass FET 105 is identical with the sensing FET 100 and the gate of the pass FET 105 is commonly connected to the gate of the sensing FET 100 and the output node 44 of the error amplifier 40, then the gate-source voltage of the sensing FET 100 will also increase, which will lead to an increase in the current through the second voltage divider 62 and thus an increase in the voltage across the resistor Rfl. As a result, the voltage at the input of the first comparator 110a increases above the threshold voltage $V_{REF} + \Delta V$ that leads to an Up pulse being generated and passed to the up-down counter 120. As explained above, this leads to a change in the value in the k-bit decoder 130 which leads to different ones of the plurality of the FET transistors 57a-57c being switched on or off to adjust the load current I_L and thus stabilise the output voltage V_{OUT}. Similarly, should the output voltage V_{OUT} be decreased then using the same mechanism a down pulse will be generated in the second comparator 110b leading to a decrease of the value in the up-down-counter 120 and thus in the k-bit decode 130. The load current I_L will be increased by switching one or more of the pass FETs 57a-57c.

[0040] This mechanism means that the gate source voltage V_{gs} on the pass FET 105 is controlled in a limited range over a wide range of currents and this enables a stable DC output voltage. The field effect transistors 57a-57c remain in saturation and the load current (W/L) ratio remains substantially constant which results in improved frequency stability of the voltage regulator 10.

Reference Numerals

[0041]

10 Voltage regulator

20	Voltage reference
30	Output voltage sensing circuit
40	Error amplifier
42a, 42b	Inputs
44	Output
49a-	Decoder outputs
50	Programmable array
53a-53c	Switches
55a-55c	Current source
57a-57c	field effect transistors
60	First voltage divider
62	Second voltage divider
70	Controller
80	Regulator monitor
82	Voltage monitor
84	Load current sensor
100	Sensing FET
105	Pass FET
110a, 110b	Comparator
120	Up-down counter
130	K-Bit decoder
135	Lines
400	Pass transistor
410	Cascode
V_{DD}	Input voltage
V_{OUT}	Output voltage
I_{sense}	Sensing current
I_{REF}	Reference current

Claims

1. A voltage regulator (10) configured to regulate an input voltage (V_{DD}) to a predetermined regulated output voltage (V_{OUT}) and comprising:

   - a voltage reference (20);
   - a controlling and regulating element (70, 80) connected to the voltage reference (20) ; and
   - a programmable array (50) of output elements (55a-c) for generating a load current (I_l) on an output, the input of the programmable array (50) being connected to an output (44) of the controlling and regulating element (70, 80) and the output of the programmable array (50) being connected to an input of the controlling and regulating element (70, 80).

2. The voltage regulator (10) of claim 1, further comprising an error amplifier (40) with inputs (42a, 42b) connected to the voltage reference (20) and to the output voltage sensing circuit (30).

3. The voltage regulator (10) of claim 1 or 2, further comprising a current sensor (84) connected to the controlling and regulating element (70, 80).

4. The voltage regulator (10) of claim 3, wherein the current sensor (84) comprises a first FET (105) and a first voltage divider (60) connected in series with each other and a second FET (100) and a second voltage divider (62) connected in series with each other, and wherein the gate of the first FET (100) and the gate of the second FET (105) are connected together.

5. The voltage regulator (10) of any of the above claims, wherein the controlling and regulating element (70, 80) comprises a controller (70) for controlling the programmable array (50) and a regulator monitor (80) for receiving inputs from the output of the programmable array (50).

6. The voltage regulator (10) of claim 5, wherein the regulator monitor (80) comprises a first comparator (110a) and a

second comparator (110b), an up-down counter (120) connected to outputs of the first comparator (110a) and the second comparator (110b), and a decoder (130), wherein
an output of the up-down counter (120) is connected to an input of the decoder (130) and a plurality of decoder outputs (135) are connected to a plurality of switches (53a-53c) of the programmable array (50).

7. The voltage regulator of claim 6, wherein the output of the second voltage divider (62) is connected to the first comparator (110a) and the second comparator (110b).

8. The voltage regulator (10) of any of the above claims, wherein the programmable array (50) comprises a plurality of field effect transistors (57a-c).

9. The voltage regulator (10) of claim 8, wherein gates of the plurality of field effect transistors (57a-c) are connected to ones of the plurality of the switches (53a-53c).

10. The voltage regulator (10) of claim 8 or 9, wherein differing ones of the plurality of field effect transistors (52) have differing channel lengths and widths.

11. The voltage regulator (10) of any of the above claims, wherein the programmable array (50) comprises a plurality of FET transistors.

12. A method for regulating an output voltage comprising:

sensing at least one of the load current (I_L) or the output voltage (V_{OUT}) using a regulator monitor (80);
comparing the sensed one of the at least one of the load current (I_L) or the output voltage (V_{OUT}) with a reference value;
outputting an output value based on the comparing and passing the output value to a controller (70); and
switching on one or more of a plurality of output elements (55a-55c) for changing the output current I_L, wherein the number of switched on ones of the plurality of output elements (55a-55c) is dependent on the output current I_L.

13. The method of claim 12, wherein the output value is a digital value and is passed to an up-down counter (120), wherein the value of the up-down counter (120) is changeable depend on the comparing.

14. The method of claim 12, wherein the up-down counter passes a numerical value to a decoder (130) for the switching on of one or more of the plurality of output elements (55).

Amended claims in accordance with Rule 137(2) EPC.

1. A voltage regulator (10) configured to regulate an input voltage (V_{DD}) to a predetermined regulated output voltage (V_{OUT}) and comprising:

- a voltage reference (20);
- a controlling and regulating element (70, 80) connected to the voltage reference (20);
- a programmable array (50) of output elements (55a-c) for generating a load current (I_1) on an output, the input of the programmable array (50) being connected to an output (44) of the controlling and regulating element (70, 80) and the output of the programmable array (50) being connected to an input of the controlling and regulating element (70, 80);
- a first FET (105) passing a reference current (I_{REF}) to a first voltage divider (60), wherein the first FET (105) and the first voltage divider (60) are connected in series with each other; and
- a load current sensor (84) connected to the controlling and regulating element (70, 80), wherein the load current sensor (84) comprises a second FET (100) and a second voltage divider (62) connected in series with each other, wherein the second FET (100) passing a sensing current (I_{sense}) to the second voltage divider (62), and wherein the values of the resistors in the first voltage divider (60) and in the second voltage divider (62) are identically.

2. The voltage regulator (10) of claim 1, further comprising an error amplifier (40) with inputs (42a, 42b) connected to the voltage reference (20).

3. The voltage regulator (10) of any of the above claims, wherein the controlling and regulating element (70, 80) comprises a controller (70) for controlling the programmable array (50) and a regulator monitor (80) for receiving inputs from the output of the programmable array (50).

4. The voltage regulator (10) of claim 3, wherein the regulator monitor (80) comprises a first comparator (110a) and a second comparator (110b), an up-down counter (120) connected to outputs of the first comparator (110a) and the second comparator (110b), and a decoder (130), wherein
an output of the up-down counter (120) is connected to an input of the decoder (130) and a plurality of decoder outputs (135) are connected to a plurality of switches (53a-53c) of the programmable array (50).

5. The voltage regulator of claim 4, wherein the output of the second voltage divider (62) is connected to the first comparator (110a) and the second comparator (110b).

6. The voltage regulator (10) of any of the above claims, wherein the programmable array (50) comprises a plurality of field effect transistors (57a-c).

7. The voltage regulator (10) of claim 6, wherein gates of the plurality of field effect transistors (57a-c) are connected to ones of the plurality of the switches (53a-53c).

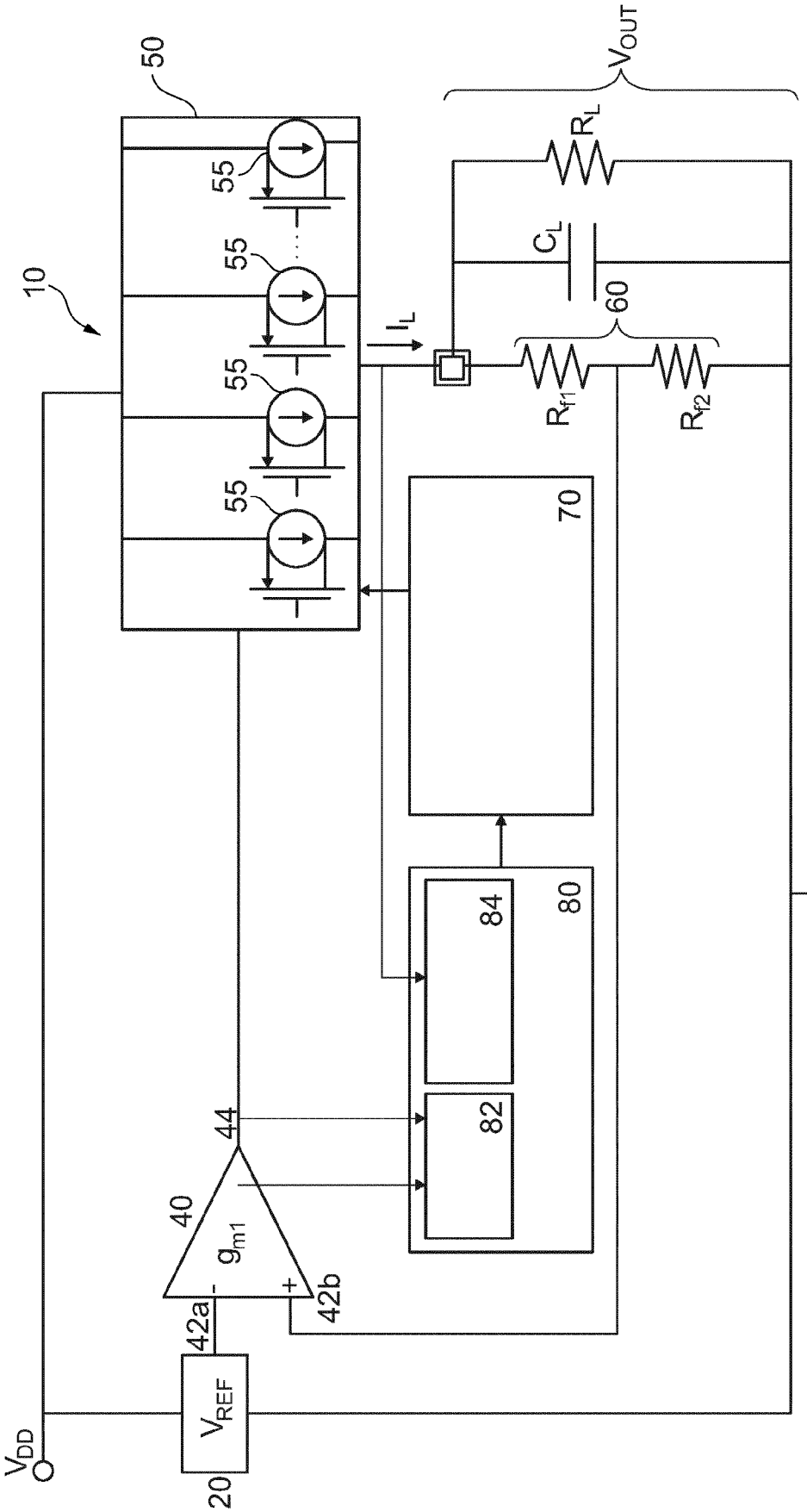
8. The voltage regulator (10) of claim 6 or 7, wherein differing ones of the plurality of field effect transistors (52) have differing channel lengths and widths.

9. A method for regulating an output voltage comprising:

sensing at least one of the load current (I_L) or the output voltage (V_{OUT}) using a regulator monitor (80);
comparing the sensed one of the at least one of the load current (I_L) or the output voltage (V_{OUT}) with a reference value;
outputting an output value based on the comparing and passing the output value to a controller (70); and
switching on one or more of a plurality of output elements (55a-55c) for changing the output current I_L, wherein the number of switched on ones of the plurality of output elements (55a-55c) is dependent on the output current I_L.

10. The method of claim 9, wherein the output value is a digital value and is passed to an up-down counter (120), wherein the value of the up-down counter (120) is changeable depend on the comparing.

11. The method of claim 9, wherein the up-down counter passes a numerical value to a decoder (130) for the switching on of one or more of the plurality of output elements (55).


50
55
55
55
55
10
I_L
V_{OUT}
R_L
C_L
60
R_{f1}
R_{f2}
70
80
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82
44
40
g_{m1}
42a
42b
V_{REF}
20
V_{DD}
GND

Fig. 1

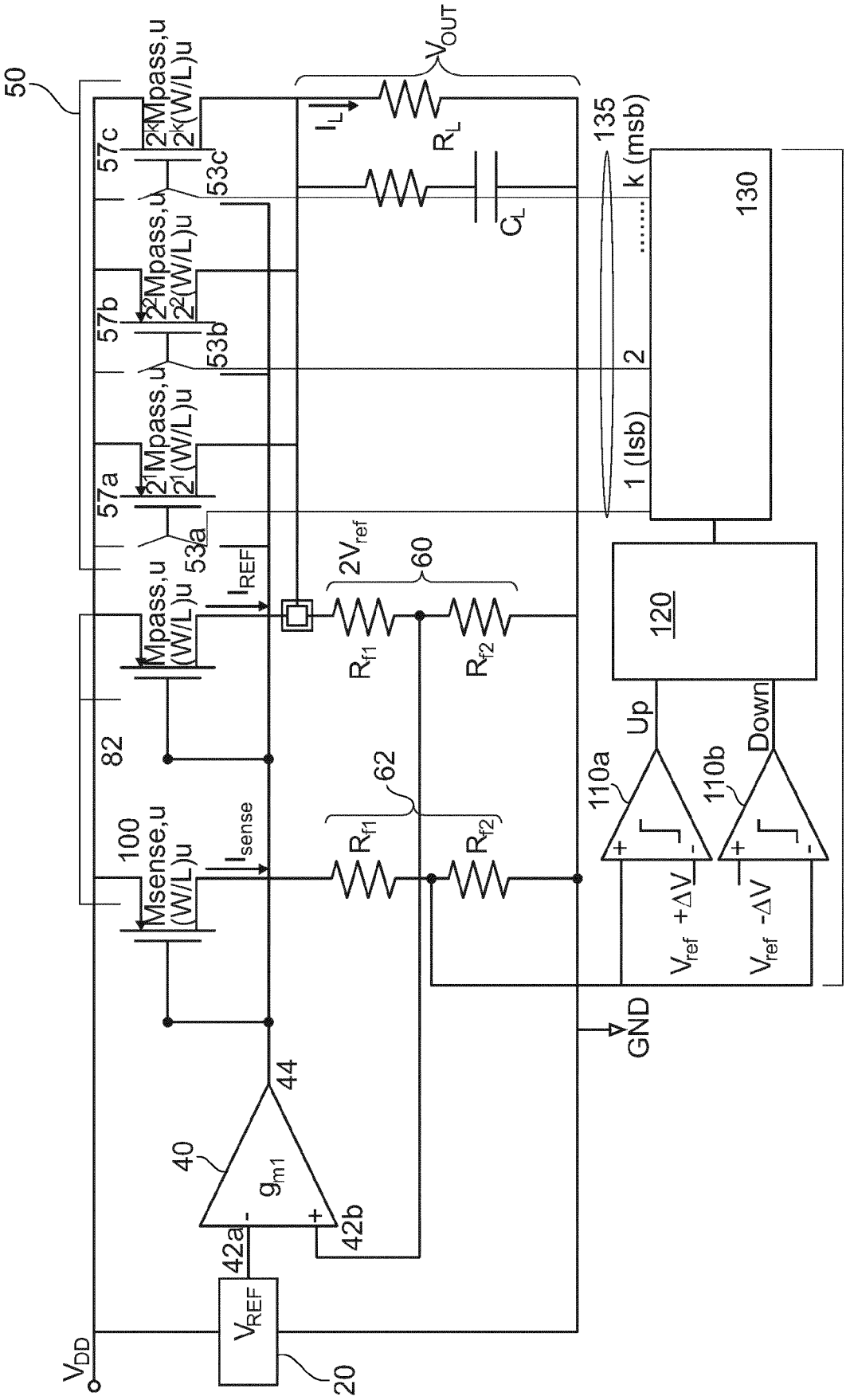
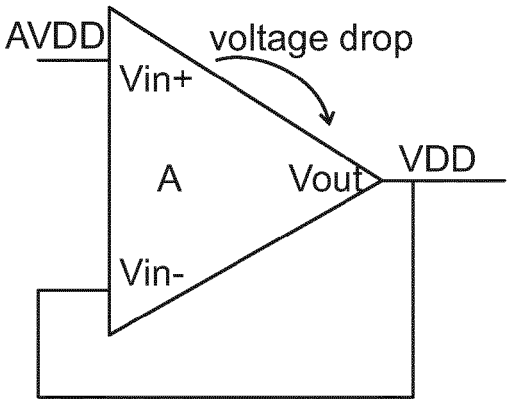
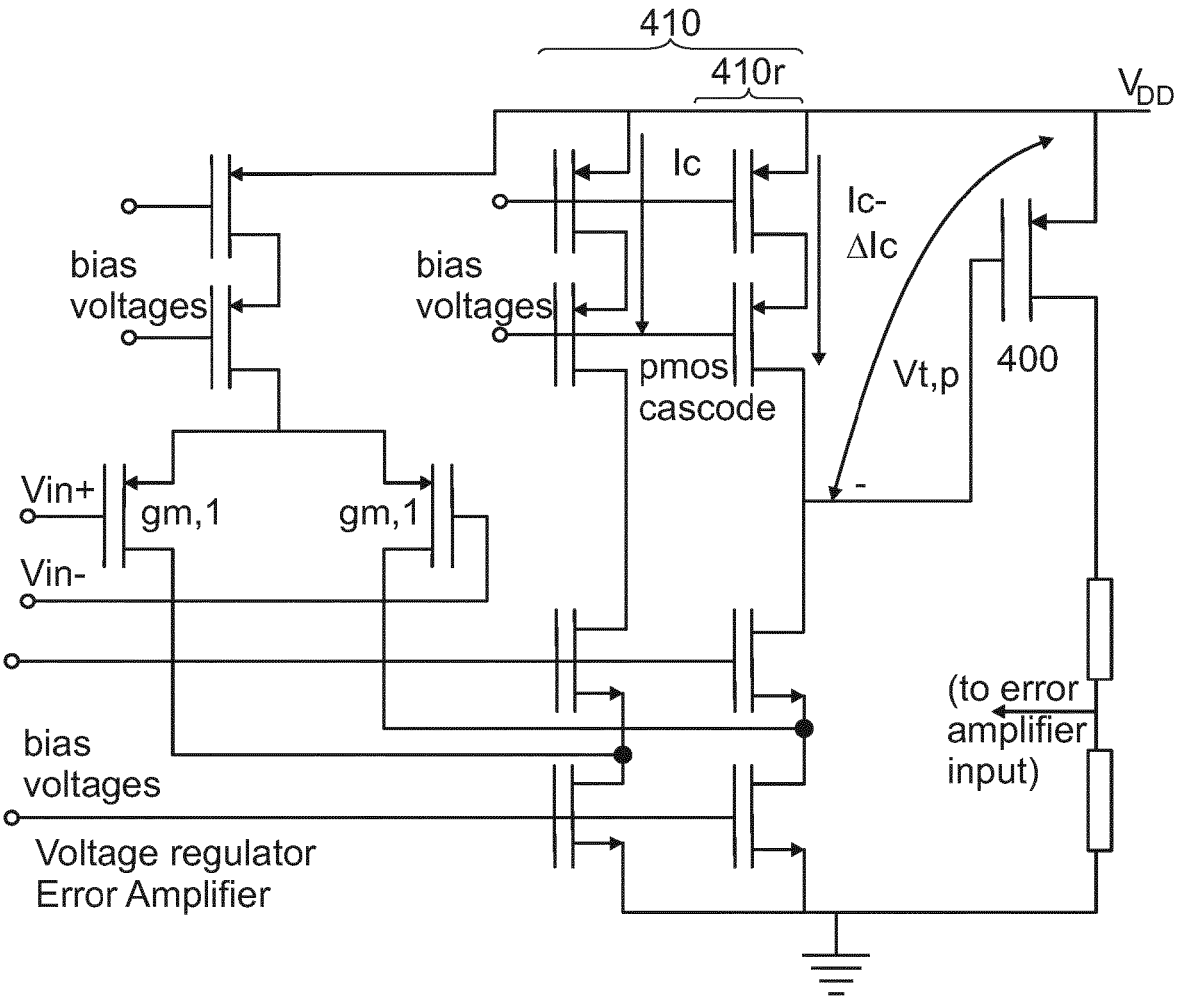

50
57c
57b
57a
82
100
53c
53b
53a
2^kMpass,u 2^k(W/L)u
2^2Mpass,u 2^2(W/L)u
2^1Mpass,u 2^1(W/L)u
Mpass,u (W/L)u
Msense,u (W/L)u
I_{REF}
I_{sense}
I_L
V_{OUT}
R_L
C_L
135
k (msb)
2
1 (lsb)
130
120
$2V_{ref}$
60
R_{f1}
R_{f2}
62
Up
Down
110a
110b
V_{ref} +ΔV
V_{ref} -ΔV
GND
44
40
g_{m1}
42a
42b
V_{REF}
20
V_{DD}

Fig. 2



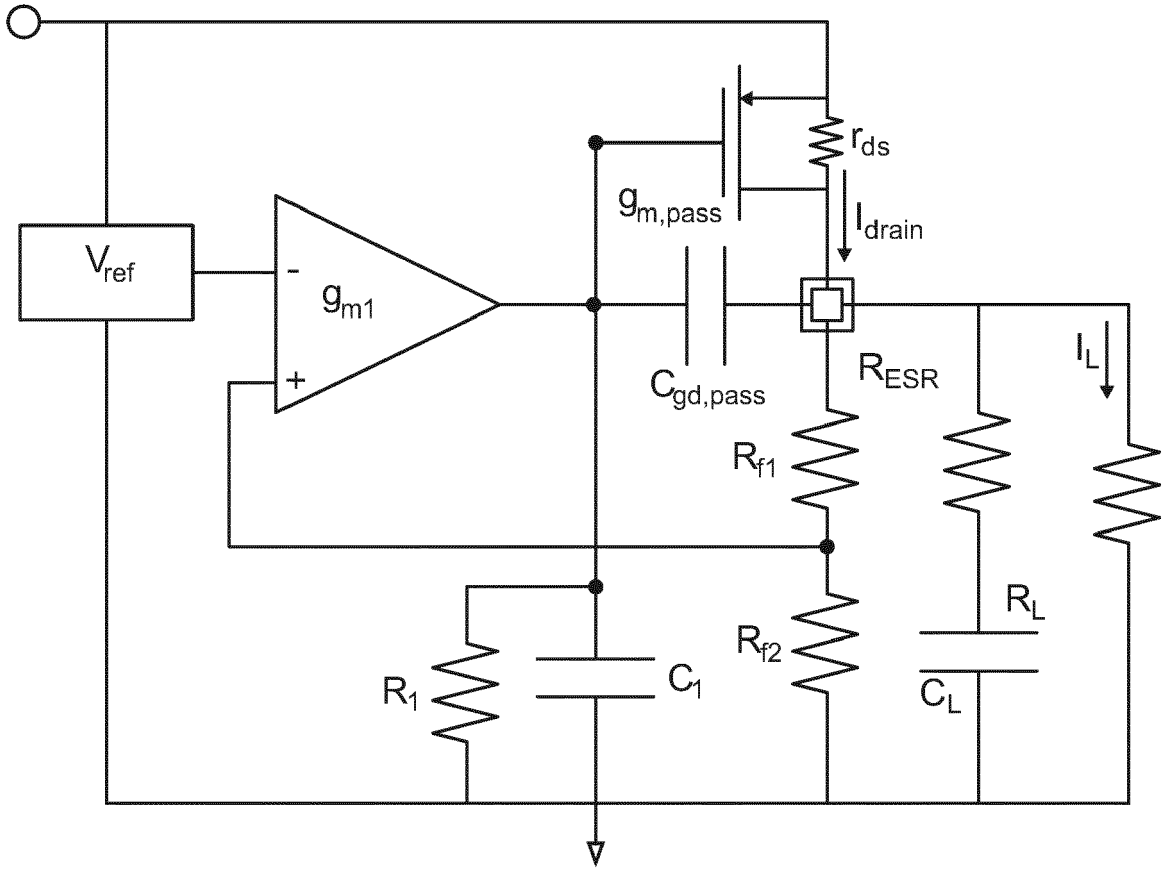
Prior Art

Fig. 3



Prior Art

Fig. 4



Prior Art

Fig. 5

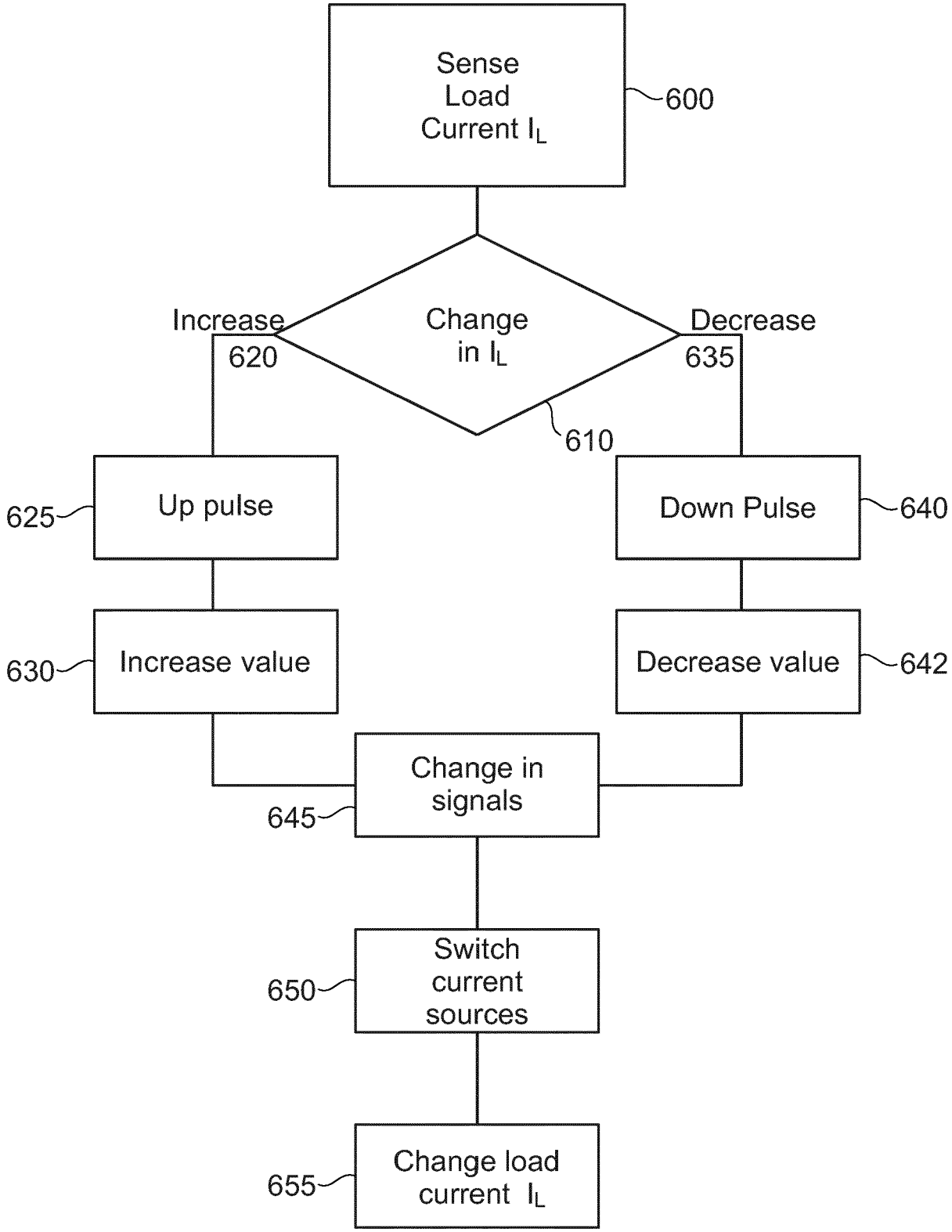

Sense Load Current I_L
600
Change in I_L
Increase
620
Decrease
635
610
Up pulse
625
Down Pulse
640
Increase value
630
Decrease value
642
Change in signals
645
Switch current sources
650
Change load current I_L
655

Fig. 6

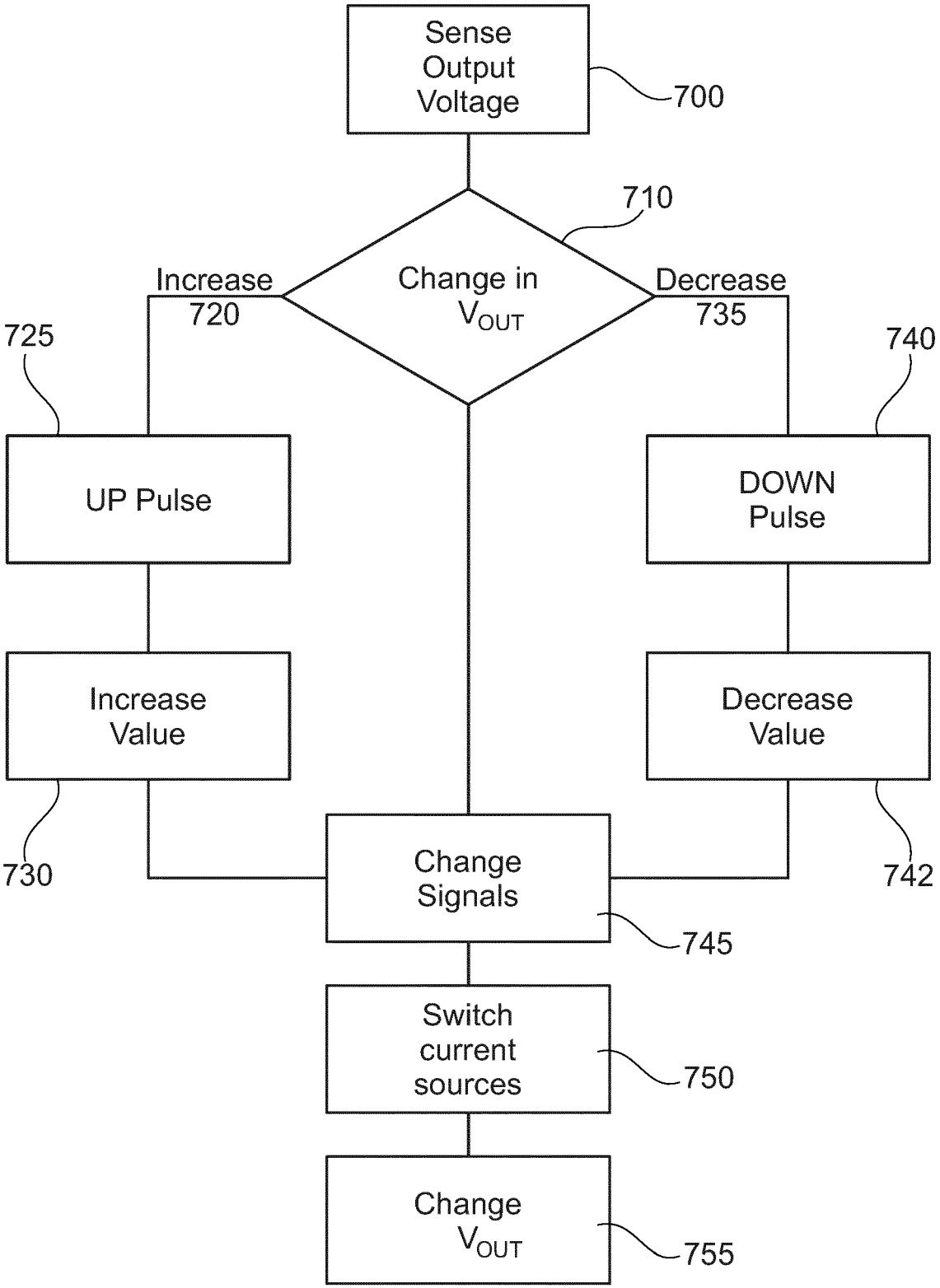

Sense Output Voltage
700
710
Change in V_{OUT}
Increase
720
Decrease
735
725
740
UP Pulse
DOWN Pulse
Increase Value
Decrease Value
730
742
Change Signals
745
Switch current sources
750
Change V_{OUT}
755

Fig. 7

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EUROPEAN SEARCH REPORT

Application Number
EP 18 18 3138

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2009/189577 A1 (LIN YING-HSIN [TW] ET AL) 30 July 2009 (2009-07-30) * abstract; figures 2-5 * -----	1-4,8-12	INV. G05F1/573 G05F1/575 G05F1/59
X	US 2014/167813 A1 (RAYCHOWDHURY ARIJIT [US] ET AL) 19 June 2014 (2014-06-19) * abstract; figure 2A * -----	1,5-8, 10-14	
X	US 2006/170401 A1 (CHEN TIEN-TZU [TW] ET AL) 3 August 2006 (2006-08-03) * abstract; figure 2 * -----	1,12	
X	US 2009/033298 A1 (KLEVELAND BENDIK [US]) 5 February 2009 (2009-02-05) * abstract; figure 4 * -----	1,12	

TECHNICAL FIELDS SEARCHED (IPC)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	21 January 2019	Arias Pérez, Jagoba

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009189577 A1	30-07-2009	TW 200933333 A	01-08-2009
		US 2009189577 A1	30-07-2009
US 2014167813 A1	19-06-2014	US 2014167813 A1	19-06-2014
		US 2017041001 A1	09-02-2017
US 2006170401 A1	03-08-2006	NONE	
US 2009033298 A1	05-02-2009	NONE	

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Patent documents cited in the description

- US 20170063231 A **[0004]**

Non-patent literature cited in the description

- **C.K.CHAVA ; J.SILVA-MARTINEZ.** A Frequency Compensation Scheme for LDO Voltage Regulators. *IEEE Transactions on Circuits and Systems,* June 2004, vol. 51 (6), 1041-1050 **[0005]**
- **R.J.MILLIKEN ; J.SILVA-MARTINEZ ; E.SANCHEZ-SINENCIO.** Full On-Chip CMOS Low-Dropout Voltage Regulator. *IEEE Transactions on Circuits and Systems,* September 2007, vol. 54 (9), 1879-1890 **[0005]**