(19)





## (11) **EP 3 599 640 A8**

(12)

## CORRECTED EUROPEAN PATENT APPLICATION

- (15) Correction information: Corrected version no 1 (W1 A1) Corrections, see Bibliography INID code(s) 71
- (48) Corrigendum issued on: 15.04.2020 Bulletin 2020/16
- (43) Date of publication: 29.01.2020 Bulletin 2020/05
- (21) Application number: 19188125.9
- (22) Date of filing: 24.07.2019

(51) Int Cl.: H01L 27/02 <sup>(2006.01)</sup> H01L 29/778 <sup>(2006.01)</sup>

H01L 29/66 (2006.01)

(84) Designated Contracting States: (72) Inventors: AL AT BE BG CH CY CZ DE DK EE ES FI FR GB Shibib, Muhammad Ayman GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO San Jose, CA California 95118 (US) PL PT RO RS SE SI SK SM TR · Liao, Chungchi Gina **Designated Extension States:** Los Altos, CA California 94028 (US) BA ME **Designated Validation States:** (74) Representative: Dilg, Haeusler, Schindelmann Patentanwaltsgesellschaft mbH KH MA MD TN Leonrodstraße 58 (30) Priority: 25.07.2018 US 201816044835 80636 München (DE) (71) Applicant: Vishay-Siliconix San Jose, California 95134 (US)

## (54) HIGH ELECTRON MOBILITY TRANSISTOR ESD PROTECTION STRUCTURES

A multi-gate High Electron Mobility Transistor (57) (HEMT) can include a Two-Dimension Electron Gas (2DEG) channel between the drain and the source. A first gate can be disposed proximate the 2DEG channel between the drain and source. The first gate can be configured to deplete majority carriers in the 2DEG channel proximate the first gate when a potential applied between the first gate and the source is less than a threshold voltage associated with the first gate. A second gate can be disposed proximate the 2DEC channel, between the drain and the first gate. The second gate can be electrically coupled to the drain. The second gate can be configured to deplete majority carriers in the 2DEG channel proximate the second gate when a potential applied between the second gate and the 2DEG channel between the second gate and the first gate is less than a threshold voltage associated with the second gate. The threshold voltage associated with the second gate can be equal to or greater than the threshold voltage associated with the first gate.

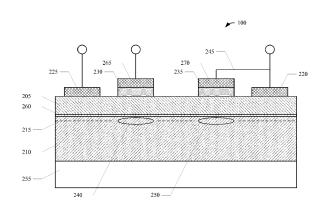


FIG. 2