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(54) **A METHOD FOR PRODUCING A GATE CUT STRUCTURE ON AN ARRAY OF SEMICONDUCTOR FINS**

(57) The method of the invention is performed on a substrate (2) comprising on its surface an array of dual stack semiconductor fins, each fin comprising a monocrystalline base portion (1), a polycrystalline portion (4) and a mask portion (5). The trenches between the fins are filled with STI oxide (10) and with polycrystalline material (12), after which the surface is planarized. Then a second mask (13) is produced on the planarized surface, the second mask defining at least on one opening (15), each opening extending across an exposed fin, and a thermal oxidation is performed of the polycrystalline material on either side of the exposed fin in each of the openings (15), thereby obtaining two oxide strips (16) in the openings. Using the second mask (13) and the strips (16) as a mask for self-aligned etching, the material of the exposed dual stack fins is removed, and subsequently replaced by an electrically isolating material, thereby creating gate cut structures (21).

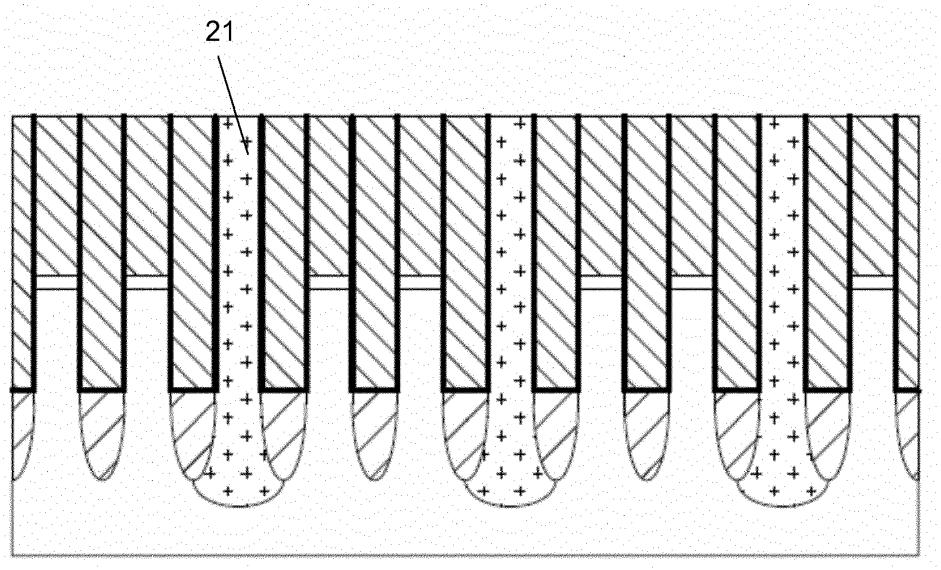


FIG. 1n

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Description

Field of the Invention

[0001] The present invention is related to semiconductor processing, in particular to finFET processing and the aspect of isolating neighbouring gate electrodes on a dense array of fin structures.

State of the art.

[0002] The design rules for scaling fin-based semiconductor devices continue to evolve towards smaller dimensions. This evolution poses important challenges on the processing of these devices. One aspect that has demanded particular attention is the isolation of adjacent gate electrodes extending transversally across an array of semiconductor fins. The realization of so-called gate cut isolating structures has become more critical as the dimensions of the fins decreases, to the point where classic lithographic techniques are no longer suitable, due to overlay-related inaccuracies in terms of the position of the isolating structures.

[0003] In order to meet these strict constraints, efforts have been made to realize the gate cut structures without the need for lithographic patterning. Document US2016/0233298 describes a method for producing self-aligned gate cut and local interconnect structures. The method involves the production of dummy spacers on both sides of the fins of an array of parallel fins, followed by the deposition of an isolation structure in the space between two dummy spacers. This method requires the step of removing fins from an array of fins, prior to the formation of the spacers. The method furthermore requires careful attention to controlling the thickness of the spacers, in order to obtain given dimensions of the isolation structures. This approach is therefore complex in terms of process steps and control.

[0004] Another document, US9960077, describes a method wherein a self-aligned lithographic process is used for at least partially removing one fin from an array of fins, followed by the replacement of said fin by an isolating structure. The method is applied to an array of silicon fins of standard height. The method however involves a number of planarization steps which are incompatible with this standard fin height. In other words, the method is difficult to realize in practice without reducing the fin height.

Summary of the invention

[0005] The invention aims to provide a method that remedies the above-described deficiencies. This aim is achieved by the method according to the appended claims. The method of the invention is performed on a substrate comprising on its surface an array of dual stack semiconductor fins, each fin comprising a monocrystalline base portion, a polycrystalline portion and a mask portion. The trenches between the fins are filled with STI oxide and with polycrystalline material, after which the surface is planarized. Then a second mask is produced on the planarized surface, the second mask defining at least one opening, each opening being located across an exposed fin, and a thermal oxidation is performed of the polycrystalline material on either side of the exposed fin in each of the openings, thereby obtaining two oxide strips adjacent the exposed fin. Using the second mask and the strips as a mask for self-aligned etching, the material of the exposed dual stack fins is removed, and subsequently replaced by an electrically isolating material, thereby creating isolating gate cut structures.

[0006] The invention is in particular related to a method for producing a gate cut structure on an array of semiconductor fins, the method comprising the steps of :

- Providing a substrate comprising an array of dual stack fins, each fin comprising : a base portion consisting of monocrystalline semiconductor material, a portion consisting of a polycrystalline semiconductor material on the monocrystalline portion, a portion of a first mask on the polycrystalline portion,
- Depositing a shallow trench isolation dielectric material in between and on top of the dual stack fins, and planarizing said STI material, stopping on the first mask portions of the dual stack fins,
- Etching back said STI material beyond the top surface of the monocrystalline portions of the dual stack fins, to thereby form trenches between the dual stack fins, the trenches having said STI material on the bottom thereof,
- Depositing a conformal dielectric layer on the dual stack fins and on the bottom of said trenches, followed by :
- Depositing said polycrystalline semiconductor material in said trenches and on top of the dual stack fins to form a layer of the polycrystalline material, and planarizing said layer, stopping on the first mask portions of the dual stack fins, followed by :
- Producing a second mask on the planarized surface, said second mask defining at least one opening that exposes a dual stack fin and that extends parallel to said exposed dual stack fin, said opening having a width (w) that exceeds the width (w_f) of the exposed dual stack fin, and that fully overlaps said width of the exposed dual stack fin,
- Heating the substrate thereby forming two oxide strips formed of thermally oxidized polycrystalline semiconductor material at the bottom of said at least one opening, the strips being positioned on either side of the first mask portion of the exposed dual stack fin, followed by:
- Removing the first mask portion, the polycrystalline portion and at least part of the monocrystalline portion of the exposed dual stack fin, by a self-aligned etching process in said opening, thereby creating a trench,

- Filling the trench with an electrically isolating material, thereby forming the gate cut structure.

[0007] The dual stack fins may furthermore comprise a dielectric portion in between the monocrystalline portion and the polycrystalline portion, wherein said dielectric portion is equally removed when creating the trench.

[0008] According to an embodiment, the semiconductor material is silicon and the polycrystalline semiconductor material is polycrystalline silicon.

[0009] The first mask portion on top of the polycrystalline portion of the dual stack fins may be formed of Si_3N_4. The second mask may be formed of an oxide material.

[0010] According to an embodiment, the semiconductor material is silicon, the polycrystalline material is polysilicon, and the second mask is formed of silicon oxide.

[0011] The invention is furhermore related to a semiconductor substrate comprising on its surface :

- an array of dual stack fins, each fin comprising : a base portion consisting of monocrystalline semiconductor material, a portion consisting of a polycrystalline semiconductor material on the monocrystalline portion, a portion of a first mask on the polycrystalline portion,
- trenches in between the dual stack fins, said trenches having a shallow trench isolation material at the bottom of the trenches, a conformal dielectric layer on the sidewalls and on the STI material at the bottom of the trenches, and a polycrystalline semiconductor material inside the trenches, and wherein the substrate is planarized at the level of the first mask portions,
- a second mask on the planarized surface, said second mask defining at least one opening that exposes a dual stack fin and that extends parallel to said dual stack fin, said opening having a width (w) that exceeds the width (w_f) of the dual stack fin, and that fully overlaps said width of the dual stack fin,
- two strips formed of an oxide of the polycrystalline semiconductor material at the bottom of said at least one opening, the strips being positioned on either side of the first mask portion of the exposed dual stack fin.

[0012] According to an embodiment of the substrate according to the invention, the dual stack fins furthermore comprise a dielectric portion in between the monocrystalline portion and the polycrystalline portion, and wherein said dielectric portion is equally removed when creating the trench.

[0013] According to an embodiment of the substrate according to the invention, the semiconductor material is silicon and the polycrystalline semiconductor material is polycrystalline silicon.

[0014] According to an embodiment of the substrate according to the invention, the first mask portion on top of the polycrystalline portion of the dual stack fins is formed of Si_3N_4.

[0015] According to an embodiment of the substrate according to the invention, the second mask is formed of an oxide material.

[0016] According to an embodiment of the substrate according to the invention, the semiconductor material is silicon, the polycrystalline material is polysilicon, and the second mask is formed of silicon oxide.

Brief description of the figures

[0017] Figures 1a to 1o illustrate the method of the invention according to a preferred embodiment.

Detailed description of the invention

[0018] The method of the invention is applied to an array of so-called dual-stack fins, as illustrated in Figure 1a. This structure is known per se. The dual stack fins are produced by known lithography and etch techniques applied to a monocrystalline semiconductor substrate 2. In this detailed description, substrate 2 is a monocrystalline silicon substrate but other semiconductor materials may be used in the method of the invention. Substrate 2 could be a monocrystalline layer on top of another substrate. On top of each monocrystalline semiconductor portion 1 of the dual stack fins is a portion 3 of a dielectric material, which may be a layer of silicon nitrate (Si_3N_4). On top of the dielectric layer 3 is a portion 4 of polycrystalline silicon. The thickness of the polycrystalline Si portion 4 is of the same order as the height of the monocrystalline fin portions 1. On top of the polySi portion 4 is a mask portion 5 which may be formed of Si_3N_4. The mask portion 5 is originally a patterned layer produced on a blanket Si wafer comprising the layers 3 and 4, and patterned in order to be able to create the trenches 6 between the fins, by etching the material in between the strips of the mask 5. If both portions 3 and 5 are Si_3Ni_4, mask portion 5 may be protected during etching of layer 3. The thickness of dielectric portion 3 is in any case considerably smaller than the thickness of the mask portion 5, for example 3-4nm for portion 3 and 40nm for mask portion 5.

[0019] Layer 3 may also be a silicon oxide layer. According to an embodiment, the polysilicon portions 4 are directly on the upper surface of the monocrystalline fin portions 1, without any intermittent layer between the fin portions 1 and the respective polySi portions 4.

[0020] First, as illustrated in Figure 1b, a shallow trench isolation (STI) oxide 10 is deposited in between and on top of the dual stack fins. The STI 10 may be deposited by Chemical Vapour Deposition (CVD). The parameters of such a deposition are known to the skilled person and therefore not described here in detail. The STI oxide 10 is planarized (Fig. 1c) by grinding and/or CMP (chemical mechanical polishing), stopping on the mask 5, and the STI oxide is etched back until the oxide 10 remains in an area at the bottom of the trenches (Fig. 1d), thereby sep-

arating the monocrystalline fin portions 1. Then a dummy silicon oxide layer 11 is deposited conformally on the dual stack fins (Fig. 1e). The layer 11 may be deposited by Atomic Layer Deposition, applying ALD parameters known as such by the person skilled in the art. Layer 11 covers the side walls of the fins, the top of the fins, and the bottom of the trenches, now formed by the STI oxide 10. Polysilicon is then deposited, preferably by low pressure CVD (LPCVD), filling the trenches and forming a layer 12 on top of the dual stack fins (Fig. 1f). The polySi layer 12 is planarized (Fig. 1g), stopping on the mask 5. Then a silicon oxide (SiO_2) layer 13 is deposited preferably by CVD, on the planarized surface (Fig. 1h), followed by the production of a patterned hardmask 14 on the SiO_2 layer (Fig. 1i). The hardmask 14 may be a photoresist layer for example. According to preferred embodiments, the hardmask is a tri-layer stack, for example a PR/SoG/SoC stack formed of photoresist, spin-on glass and spin-on carbon. The SiO_2 layer 13 is then etched, stopping on the planarized surface, and the hardmask 14 is stripped (Fig. 1j). The hardmask pattern is such that openings 15 are formed above a number of exposed fins, the width w of the openings 15 being superior to the width of the fins w_f, and positioned relative to the fins such that the width w of the openings fully overlaps the respective fins. The length of the opening (in the direction perpendicular to the drawings) can be chosen in accordance with a particular design. The use of silicon oxide for the mask 13 is advantageous in particular when the mask 5 is formed of Si_3N_4, given that Si_3N_4 can be removed selectively relative to silicon oxide and to silicon by wet etching with H_3PO_4.

[0021] By a heating step, thermal oxidation of the polysilicon on either side of the exposed mask portion 5 in the openings 15 is then obtained, see Fig. 1k. This forms an oxide layer in the shape of two elongate strips 16 of oxide on either side of the exposed fins in each of the openings 15. The thickness of the oxide layer is preferably between 2 and 10 nm.

[0022] The patterned oxide 13 and the oxide strips 16 are now used as a mask for selectively removing the material of the dual stack fins in the openings (Fig. 1l). The removal of the fin material occurs in a self-aligned manner, because of the overlapping width w of the opening 15 relative to the width w_f of the fins. Preferably, the etch continues into the silicon substrate 2, as shown in Figure 1l, creating trenches 17. The trenches could also stop higher up in the monocrystalline fin portion 1. Generally, it can be said that said monocrystalline portion 1 is at least partially removed. Possibly it is completely removed, and possibly the etching continues into the substrate 2, creating trenches 17 with the appearance shown in the drawings.

[0023] A series of different etch processes may be used to remove consecutively the mask portion 5, the polysilicon portion 4, the thin dielectric portion 3, and the monocrystalline portion 1 of the dual stack fins, as well as a portion of the substrate 2. For example, when the mask 5 and the thin dielectric portion 3 are formed of Si_3Ni_4, these portions may be removed by a wet etch process using H_3PO_4. The polysilicon 4 and the monocrystalline silicon material 1 and 2 may be removed by tetramethylammoniumhydroxide (TMAH). The trenches 17 formed as a result of the etch processes are then filled with an electrically isolating material 20, see Figure 1m. This may be Si_3N_4. A sequence of planarization steps may then be applied, until the mask 5 is removed from the remaining fins, thereby creating self-aligned gate cut structures 21 (Fig. 1n). Finally, a polySi layer 22 is applied (Fig. 1o).

[0024] The resulting structure can be further used in a known replacement gate process flow for producing transistor devices on the monocrystalline fins 1. The isolating gate cut structures 21 are significantly higher than the monocrystalline fins 1. Therefore the replacement gate process can be applied without loss of height of the fins. A particular advantage of the method according to the invention is that the mask 5 used for creating the fins can remain on the fins until the end of the method.

[0025] The invention is related also to intermediate products obtained at particular stages of the method, as shown in Figures 1k, 1l and 1m. This is the substrate comprising the mask 13 and the oxide strips 16 formed on the areas of polySi on either side of the fins in the openings 15.

[0026] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

[0027] Unless specifically specified, the description of a layer being present, deposited or produced 'on' another layer or substrate, includes the options of

- said layer being present, produced or deposited directly on, i.e. in physical contact with, said other layer or substrate, and
- said layer being present, produced or deposited on one or a stack of intermediate layers between said layer and said other layer or substrate.

Claims

1. A method for producing a gate cut structure (21) on an array of semiconductor fins (1), the method com-

prising the steps of :

- Providing a substrate (2) comprising an array of dual stack fins, each fin comprising : a base portion (1) consisting of monocrystalline semiconductor material, a portion (4) consisting of a polycrystalline semiconductor material on the monocrystalline portion, a portion of a first mask (5) on the polycrystalline portion (4),
- Depositing a shallow trench isolation dielectric material (10) in between and on top of the dual stack fins, and planarizing said STI material, stopping on the first mask portions (5) of the dual stack fins,
- Etching back said STI material (10) beyond the top surface of the monocrystalline portions (1) of the dual stack fins, to thereby form trenches (6) between the dual stack fins, the trenches having said STI material (10) on the bottom thereof,
- Depositing a conformal dielectric layer (11) on the dual stack fins and on the bottom of said trenches (6), followed by :
- Depositing said polycrystalline semiconductor material in said trenches and on top of the dual stack fins to form a layer (12) of the polycrystalline material, and planarizing said layer (12), stopping on the first mask portions (5) of the dual stack fins, followed by :
- Producing a second mask (13) on the planarized surface, said second mask defining at least one opening (15) that exposes a dual stack fin and that extends parallel to said exposed dual stack fin, said opening having a width (w) that exceeds the width (w_f) of the exposed dual stack fin, and that fully overlaps said width of the exposed dual stack fin,
- Heating the substrate (2) thereby forming two oxide strips (16) formed of thermally oxidized polycrystalline semiconductor material at the bottom of said at least one opening (15), the strips (16) being positioned on either side of the first mask portion (5) of the exposed dual stack fin, followed by
- Removing the first mask portion (5), the polycrystalline portion (4) and at least part of the monocrystalline portion (1) of the exposed dual stack fin, by a self-aligned etching process in said opening (15), thereby creating a trench (17),
- Filling the trench (17) with an electrically isolating material, thereby forming the gate cut structure (21).

2. The method according to claim 1, wherein the dual stack fins furthermore comprise a dielectric portion (3) in between the monocrystalline portion (1) and the polycrystalline portion (4), and wherein said dielectric portion (3) is equally removed when creating the trench (17).

3. The method according to claim 1 or 2, wherein the semiconductor material is silicon and the polycrystalline semiconductor material is polycrystalline silicon.

4. The method according to any one of claims 1 to 3, wherein the first mask portion (5) on top of the polycrystalline portion (4) of the dual stack fins is formed of Si_3N_4.

5. The method according to any one of the preceding claims, wherein the second mask (13) is formed of an oxide material.

6. The method according to claim 5, wherein the semiconductor material is silicon, the polycrystalline material is polysilicon, and the second mask (13) is formed of silicon oxide.

7. A semiconductor substrate (2) comprising on its surface :

- an array of dual stack fins, each fin comprising : a base portion (1) consisting of monocrystalline semiconductor material, a portion (4) consisting of a polycrystalline semiconductor material on the monocrystalline portion, a portion of a first mask (5) on the polycrystalline portion (4),
- trenches in between the dual stack fins, said trenches having a shallow trench isolation material (10) at the bottom of the trenches, a conformal dielectric layer (11) on the sidewalls and on the STI material (10) at the bottom of the trenches, and a polycrystalline semiconductor material (12) inside the trenches, and wherein the substrate is planarized at the level of the first mask portions (5),
- a second mask (13) on the planarized surface, said second mask defining at least one opening (15) that exposes a dual stack fin and that extends parallel to said dual stack fin, said opening having a width (w) that exceeds the width (w_f) of the dual stack fin, and that fully overlaps said width of the dual stack fin,
- two strips (16) formed of an oxide of the polycrystalline semiconductor material at the bottom of said at least one opening (15), the strips (16) being positioned on either side of the first mask portion (5) of the exposed dual stack fin.

8. The substrate according to claim 7, wherein the dual stack fins furthermore comprise a dielectric portion (3) in between the monocrystalline portion (1) and the polycrystalline portion (4), and wherein said dielectric portion (3) is equally removed when creating

the trench (17).

9. The substrate according to claim 7 or 8, wherein the semiconductor material is silicon and the polycrystalline semiconductor material is polycrystalline silicon.

10. The substrate according to any one of claims 7 to 9, wherein the first mask portion (5) on top of the polycrystalline portion (4) of the dual stack fins is formed of Si_3N_4.

11. The substrate according to any one of claims 7 to 10, wherein the second mask (13) is formed of an oxide material.

12. The substrate according to claim 11, wherein the semiconductor material is silicon, the polycrystalline material is polysilicon, and the second mask (13) is formed of silicon oxide.

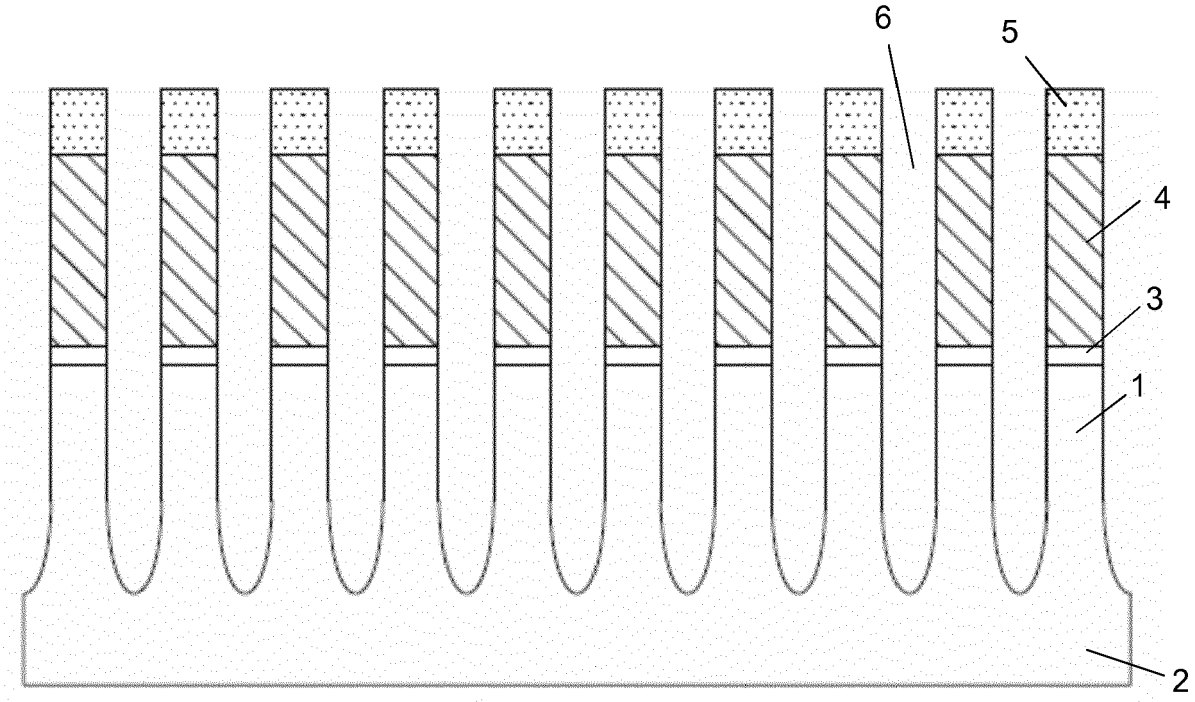


FIG. 1a

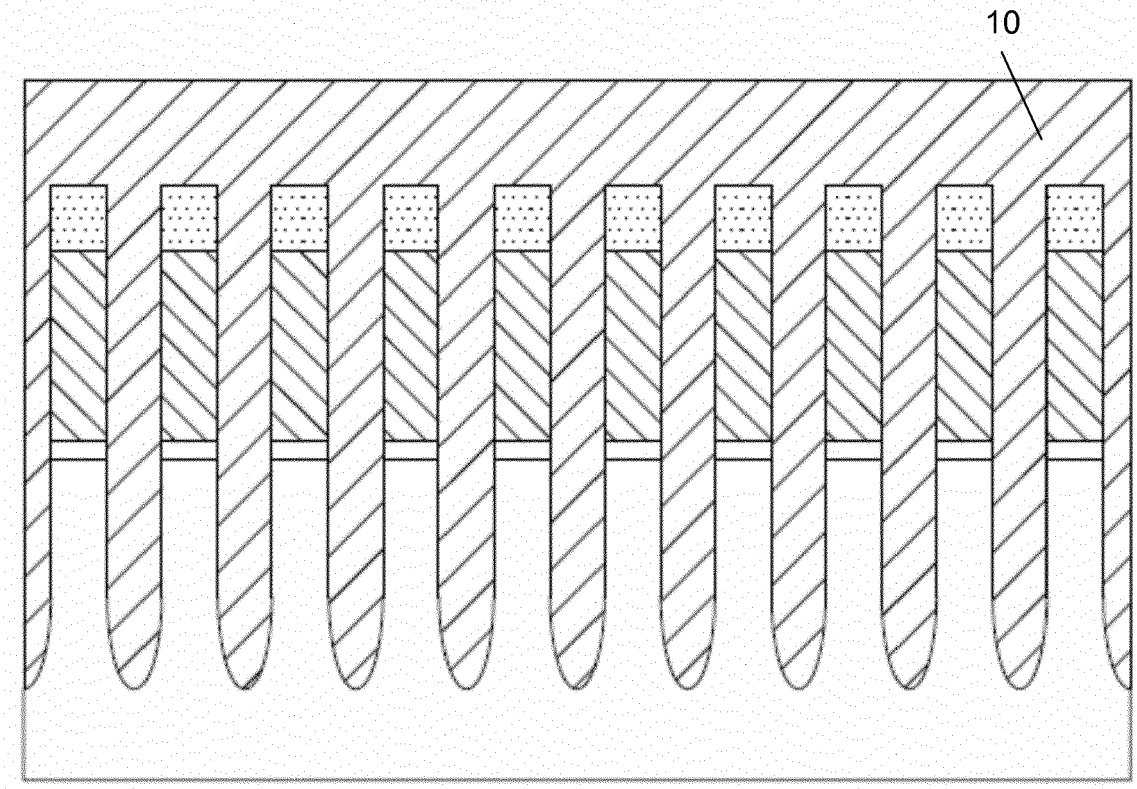


FIG. 1b

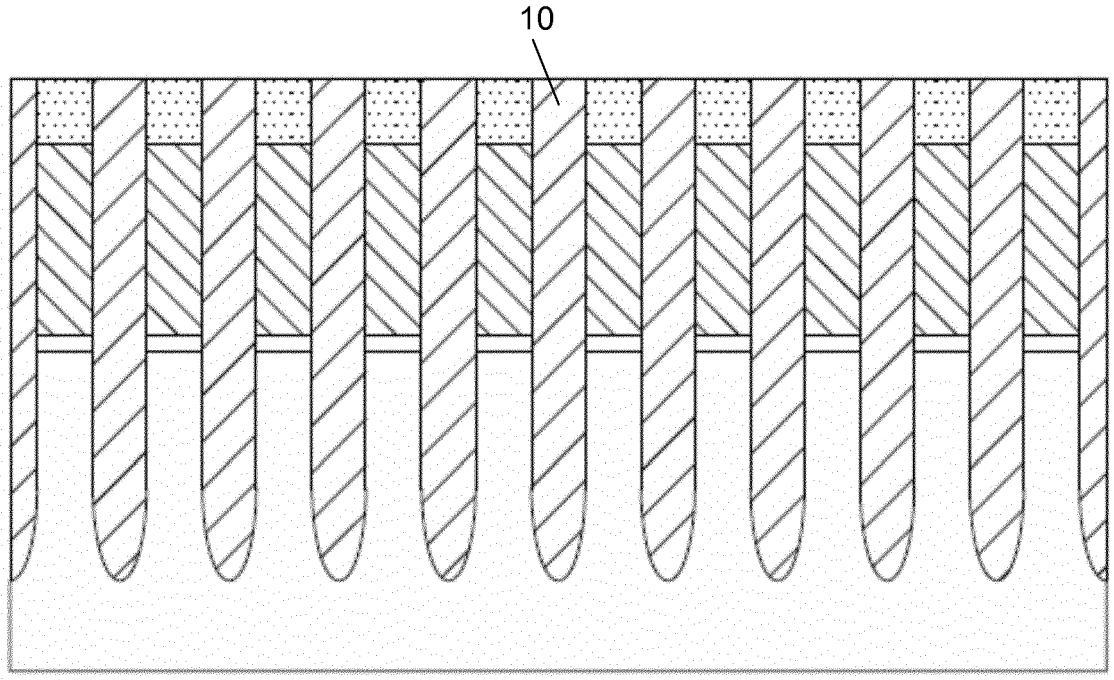


FIG. 1c

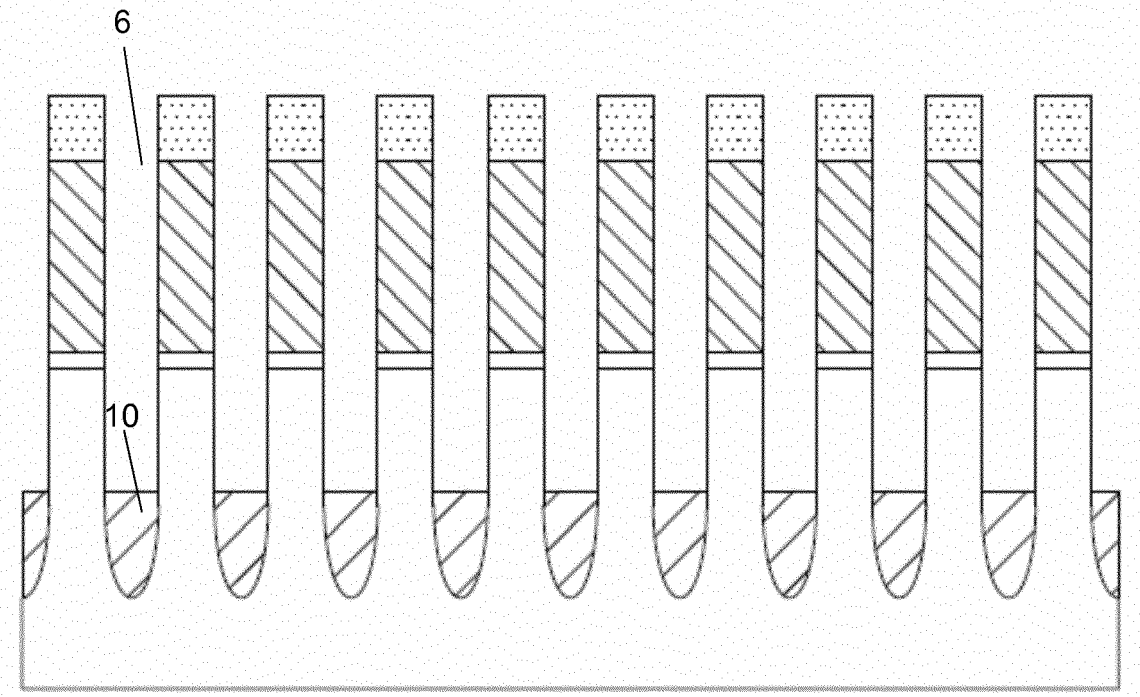


FIG. 1d

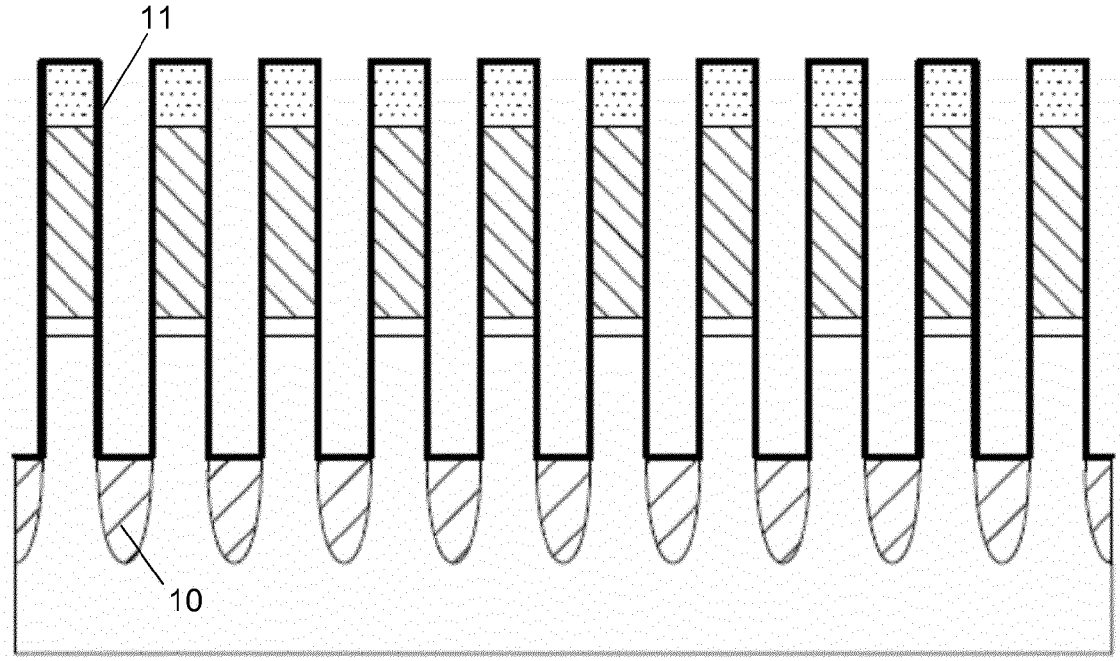


FIG. 1e

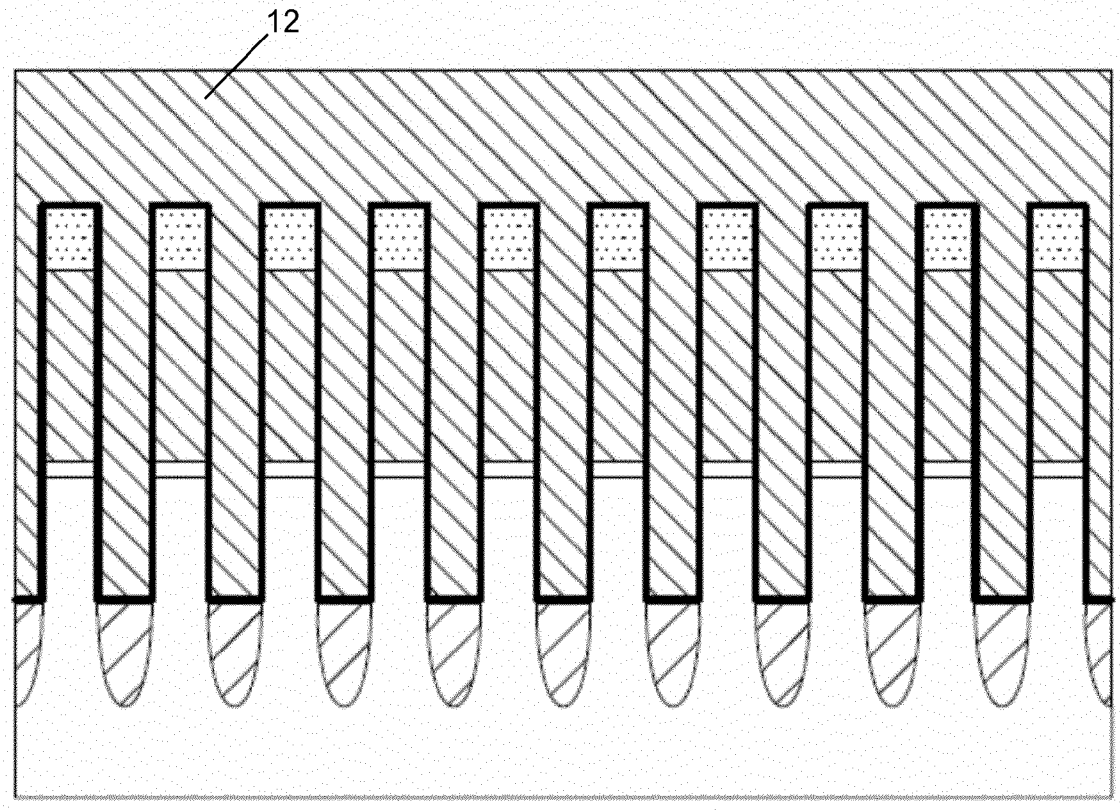


FIG. 1f

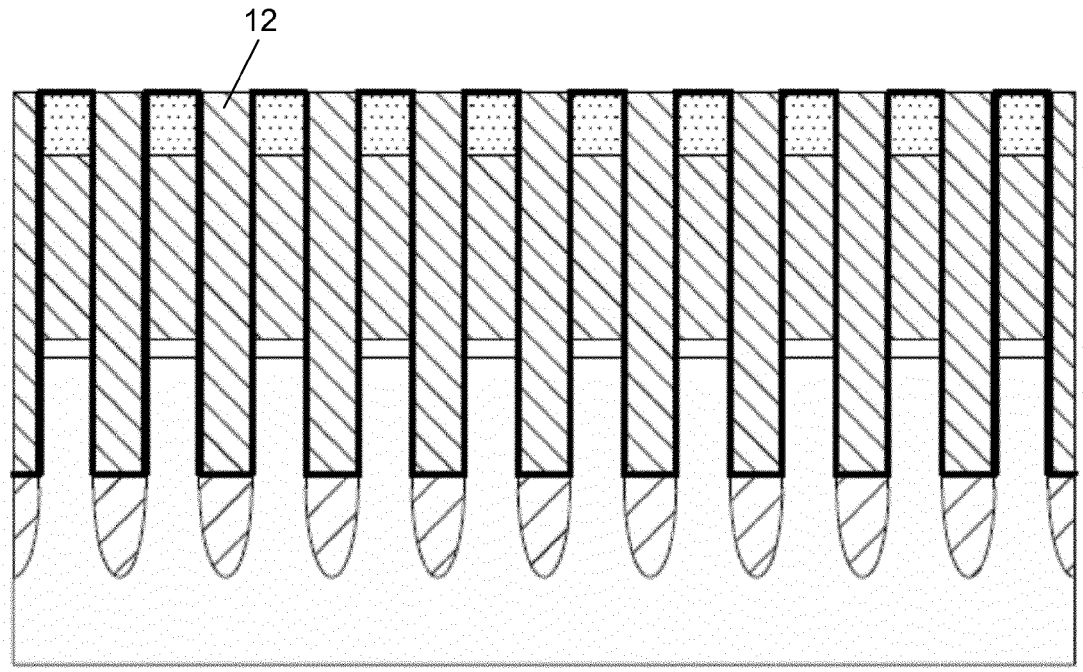


FIG. 1g

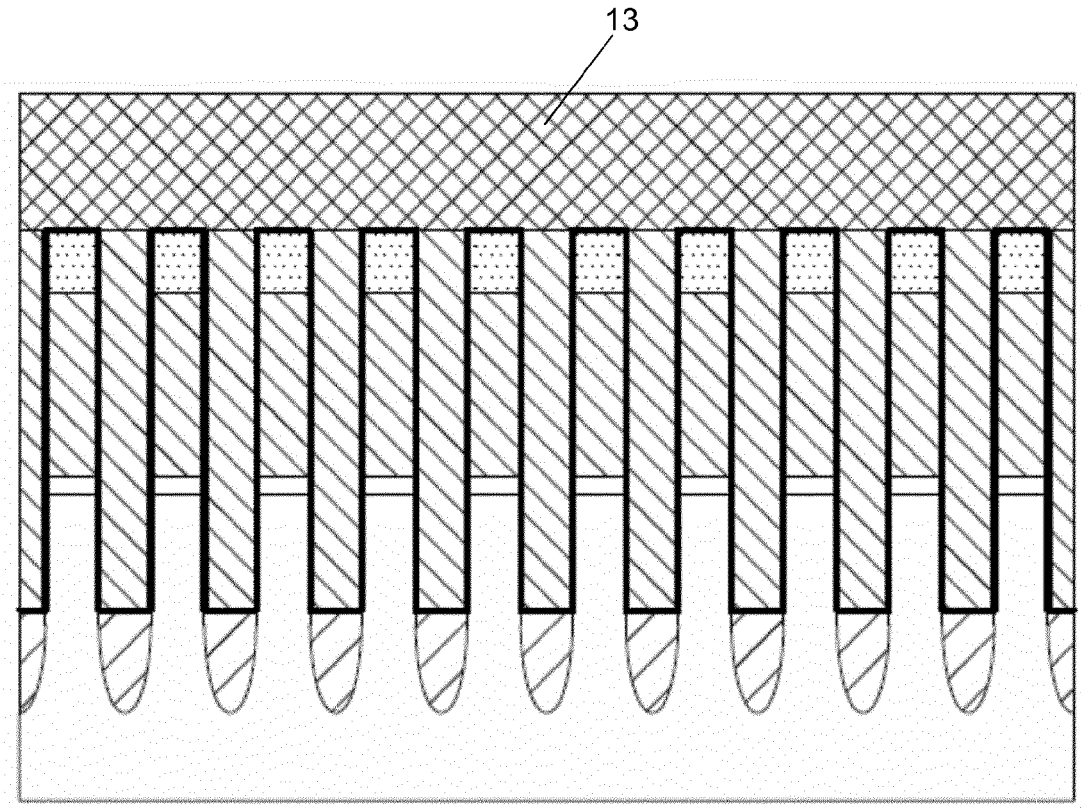


FIG. 1h

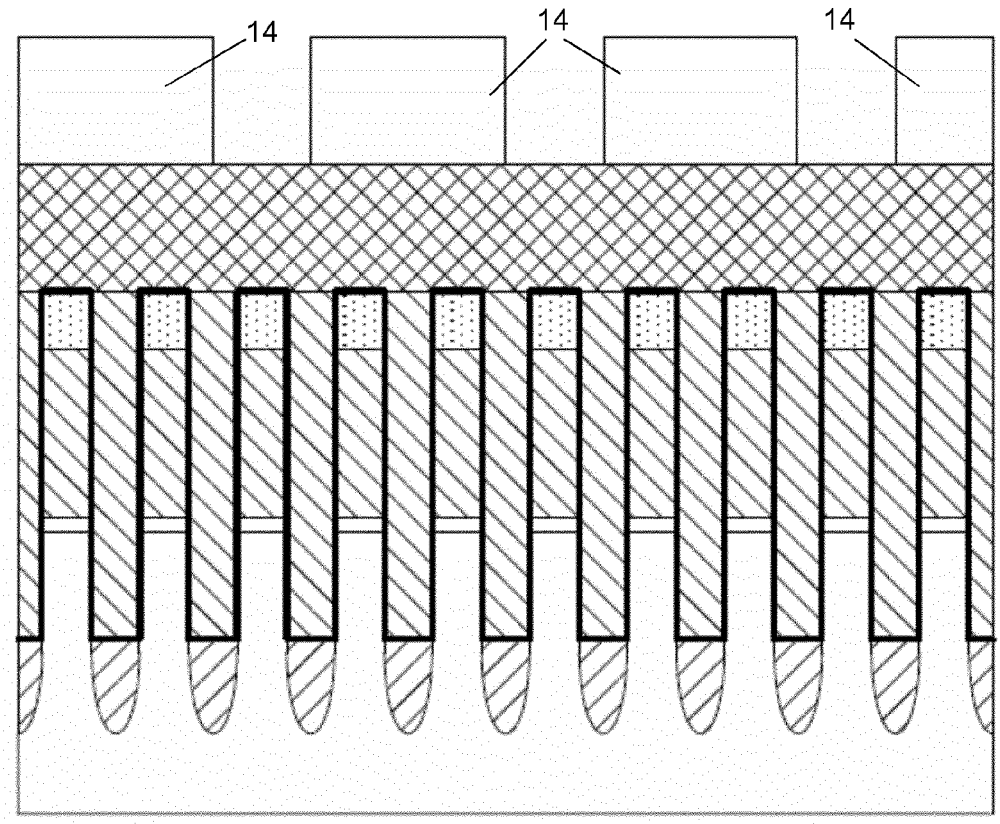


FIG. 1i

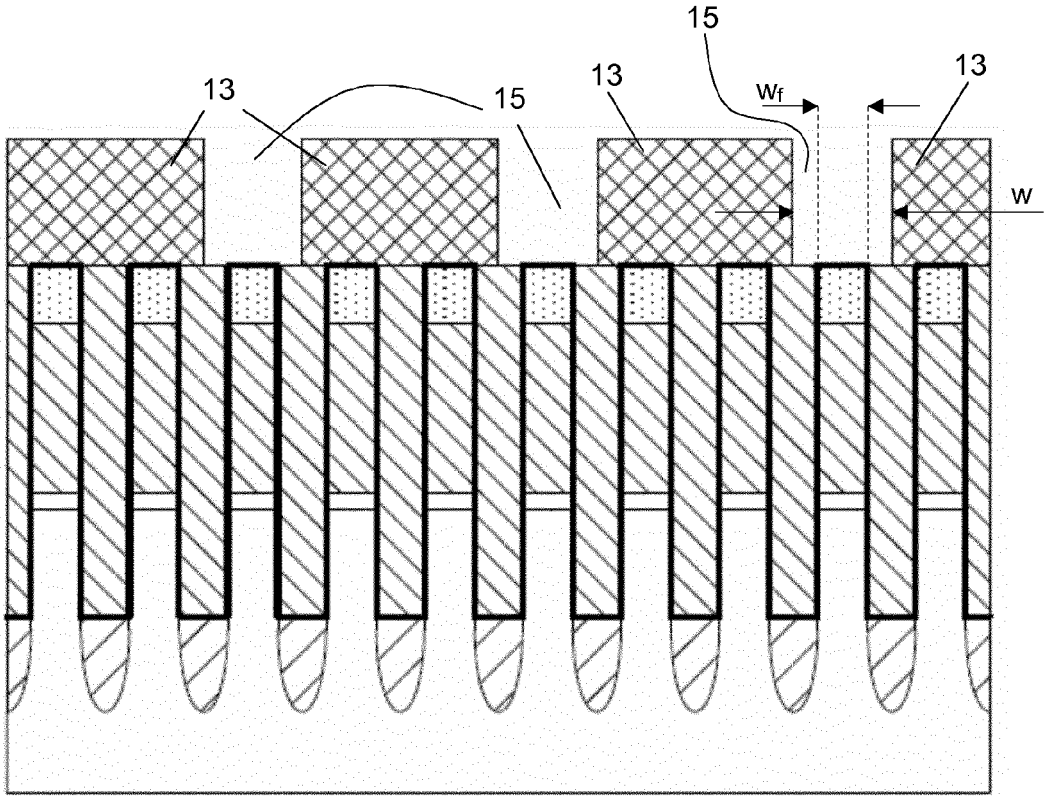


FIG. 1j

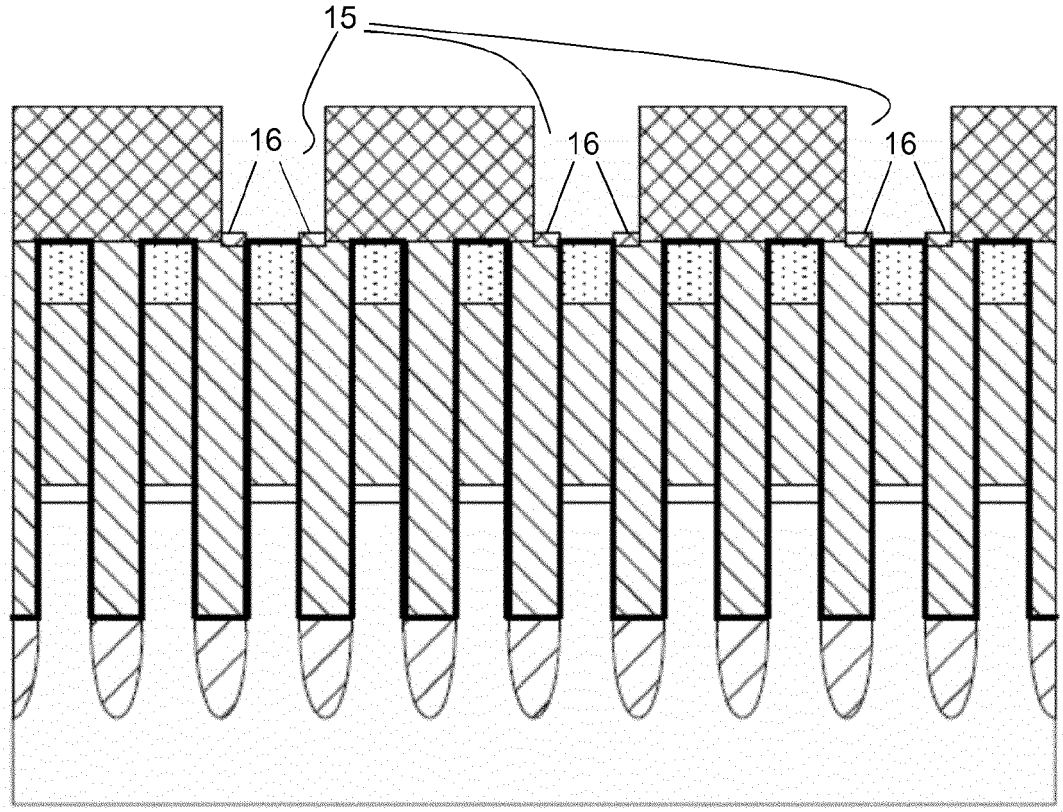


FIG. 1k

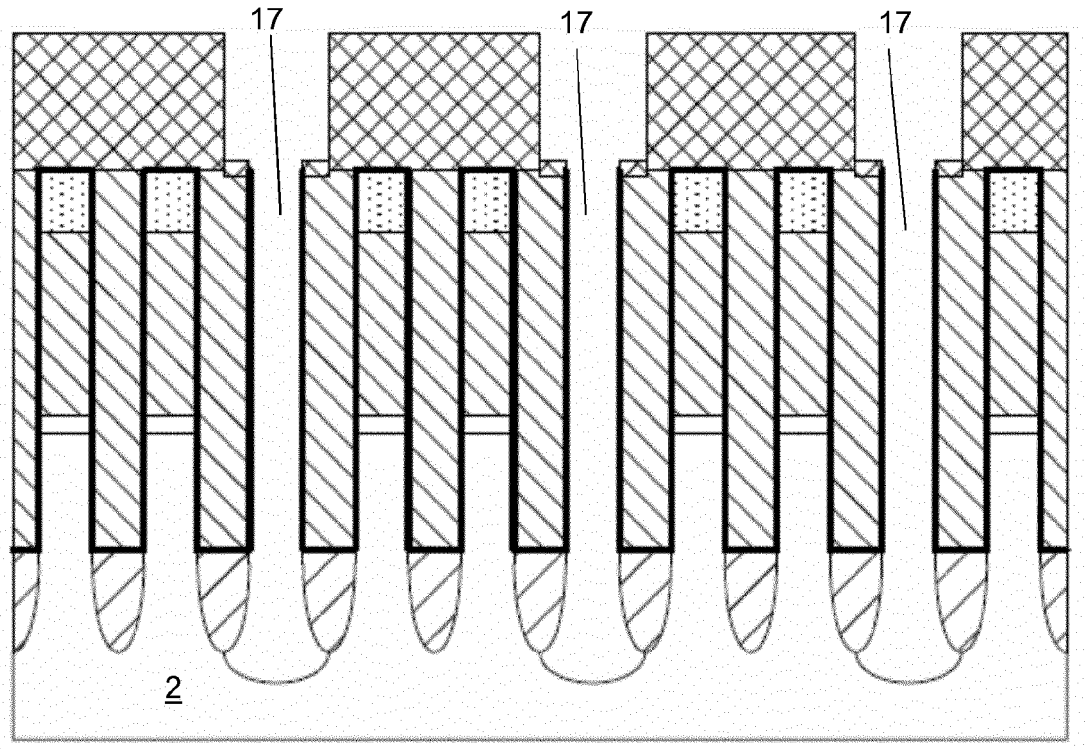


FIG. 1l

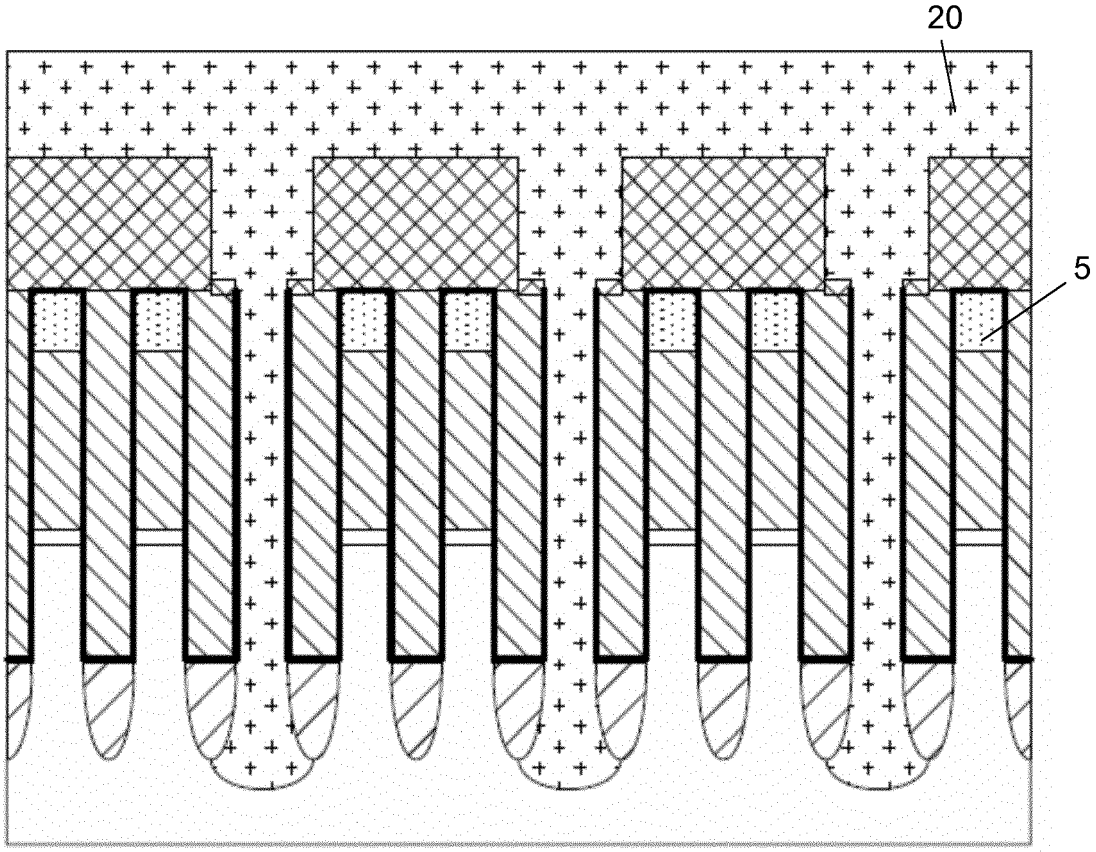


FIG. 1m

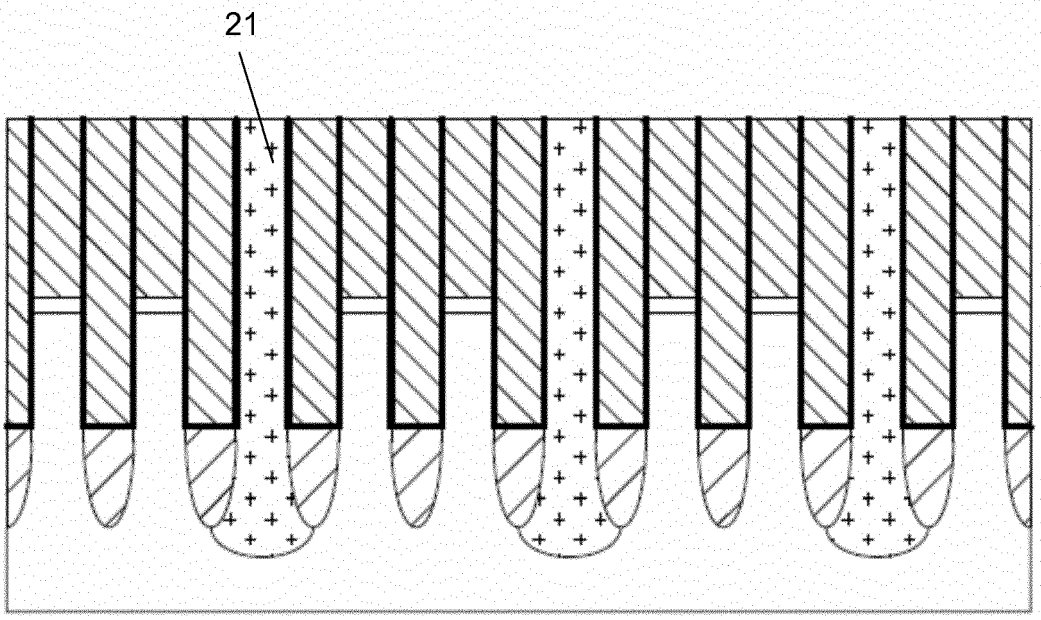


FIG. 1n

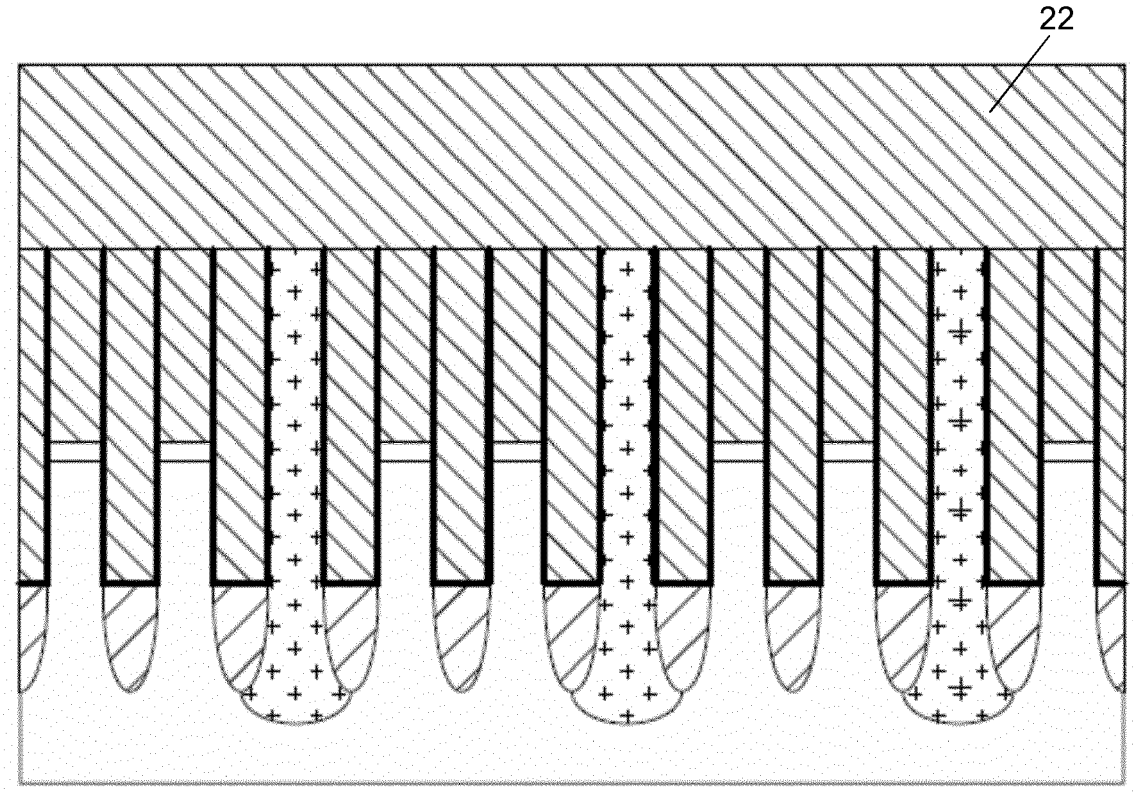


FIG. 1o

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European Patent Office
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EUROPEAN SEARCH REPORT

Application Number
EP 18 19 3273

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A,D	US 9 960 077 B1 (ZANG HUI [US] ET AL) 1 May 2018 (2018-05-01) * figures 2-9 *	1-12	INV. H01L29/66 H01L21/8234 H01L27/088
A,D	US 2016/233298 A1 (WEBB MILTON C [US] ET AL) 11 August 2016 (2016-08-11) * paragraph [0043]; figures 6,7 *	1-12	
A	US 2014/315371 A1 (CAI XIUYU [US] ET AL) 23 October 2014 (2014-10-23) * figures 2A-2H *	1-12	
A	US 2016/056181 A1 (ANDERSON BRENT A [US] ET AL) 25 February 2016 (2016-02-25) * figures 9A-11A *	1-12	

TECHNICAL FIELDS SEARCHED (IPC)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Berlin	20 February 2019	Juhl, Andreas

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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20-02-2019

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 9960077 B1	01-05-2018	NONE	
US 2016233298 A1	11-08-2016	CN 106415800 A	15-02-2017
		EP 3084815 A1	26-10-2016
		JP 6325669 B2	16-05-2018
		JP 2016541114 A	28-12-2016
		KR 20160098195 A	18-08-2016
		TW 201533902 A	01-09-2015
		TW 201719896 A	01-06-2017
		TW 201735362 A	01-10-2017
		TW 201830703 A	16-08-2018
		US 2016233298 A1	11-08-2016
		US 2018047808 A1	15-02-2018
		WO 2015094305 A1	25-06-2015
US 2014315371 A1	23-10-2014	NONE	
US 2016056181 A1	25-02-2016	US 2016056181 A1	25-02-2016
		US 2016233094 A1	11-08-2016

EPO FORM P0459

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20160233298 A **[0003]**
- US 9960077 B **[0004]**