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# (54) OPERATION OF A DIRECT CURRENT CIRCUIT BREAKING DEVICE

BETRIEB EINES GLEICHSTROMSCHUTZSCHALTERS

FONCTIONNEMENT D'UN DISPOSITIF DE COUPURE DE CIRCUIT À COURANT CONTINU

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(73) Proprietor: **ABB Power Grids Switzerland AG**
**5400 Baden (CH)**

(72) Inventors:
- **ERIKSSON, Thomas R.**
  **743 86 Bälinge (SE)**
- **ACHARYA, Anirudh**
  **9000 Aalborg (DK)**

(74) Representative: **AWA Sweden AB**
**P.O. Box 45086**
**104 30 Stockholm (SE)**

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## Description

### TECHNICAL FIELD

**[0001]** The invention generally related to the interruption of currents in direct current power transmission systems. More particularly, the invention relates to a direct current circuit breaking device to be connected in series with a power line as well as to a method and computer program product for controlling the direct current circuit breaking device.

### BACKGROUND

**[0002]** High Voltage Direct Current (HVDC) systems are known to be used in different power transmission situations, such as for transmitting power over long distances using power lines that may be over-headlines or cables.

**[0003]** In these systems there is often also needed a circuit breaker in order to disconnect the power line or cable during pole faults, such as pole-to-ground faults. A direct current circuit breaker may then comprise a number of parallel branches, where one branch comprises a mechanical disconnector in series with a load commutation switch, another branch comprises a main breaker made up of a number of series-connected power semiconductor switches and a further branch comprises at least one non-linear resistor often in the form of a surge arrester or varistor.

**[0004]** This type of DC circuit breaker is for instance described in WO 2011/ 057675. Variations of the above-described circuit breaker are known.

**[0005]** US 2012/234796 discloses a high voltage DC breaker comprising at least two individually controllable HVDC breaker sections connected in series.

**[0006]** In case of a fault in the transmission line, the DC breaker is operated to clear the fault. This operation involves opening or blocking the main breaker in order to force the fault current to flow through the surge arrester branch. The arrester branch dissipates energy and gradually brings the fault current to zero.

**[0007]** Transition of the fault current from the main breaker to the surge arrester branch is carried out in the order of few microseconds through the blocking of the main breaker. Due to high value of the fault current and small transition time, the rate of change of current (di/dt) through the surge arrester branch is high. The stray parameters, due to connection wires, current sensors, arrester mechanical arrangement and the physical property of the arrester, lead to a voltage above the designed arrester protective voltage due to high di/dt.

**[0008]** The circuit breaker may because of this be exposed to an exceedingly high transient voltage.

**[0009]** It would therefore be of interest to mitigate the overvoltage experienced by a direct current circuit breaker during blocking of a main breaker and to decrease the rate of rise of the overvoltage.

**[0010]** The present invention is concerned with this problem.

**[0011]** There is in view of what has been described above a need for improvement in the mitigating of overvoltages experienced by a direct current circuit breaker.

### SUMMARY

**[0012]** One object of the invention is therefore to provide an improvement in the mitigating of overvoltages experienced by a direct current circuit breaking device.

**[0013]** This object is according to a first aspect achieved by a direct current circuit breaking device according to claim 1.

**[0014]** This object is according to a second aspect also achieved by a method of controlling a direct current circuit breaking device according to claim 9.

**[0015]** This object is according to a third aspect also achieved by a computer program product for controlling a direct current circuit breaking device according to claim 12.

**[0016]** The invention according to the above-mentioned aspects has a number of advantages. It reduces overvoltages experienced in the circuit breaking device when currents are diverted to the non-linear resistors. Thereby elements with lower ratings may also be used. This is furthermore obtained without any additional components. It may be implemented only using some modified control software.

**[0017]** It should be emphasized that the term "comprises/comprising" when used in this specification is taken to specify the presence of stated features, integers, steps or components, but does not preclude the presence or addition of one or more other features, integers, steps, components or groups thereof.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0018]** The present invention will in the following be described with reference being made to the accompanying drawings, where

fig. 1 schematically shows a simple HVDC system comprising a power transmission medium in the form of a power line or cable connected to a DC circuit breaking device,

fig. 2 schematically shows a multi-terminal HVDC system comprising a number of power transmission lines or cables, each connected to a DC circuit breaking device,

fig. 3 schematically shows the structure of a DC circuit breaking device,

fig. 4 schematically shows the voltage across a disconnector of the DC circuit breaking device during conventional circuit breaking activity,

fig. 5 schematically shows a flow chart of a number of method steps performed by a control unit of the DC circuit breaking device when performing a mod-

ified circuit breaking activity according to the invention,

fig. 6 schematically shows the voltage across the disconnector of the DC circuit breaking device when the modified circuit breaking activity is performed, and

fig. 7 schematically shows a computer program product computer program medium comprising computer program code for implementing the adjusted circuit breaking activity.

## DETAILED DESCRIPTION

**[0019]** In the following, a detailed description of preferred embodiments of the invention will be given.

**[0020]** Fig. 1 shows one variation of a high voltage direct current (HVDC) power transmission system.

**[0021]** The system in fig. 1 is a point-to-point system for connection between two Alternating Current (AC) power transmission systems. For this reason the HVDC system includes a first and a second converter station 10 and 12, where the first converter station 10 includes a first transformer T1. The first converter station 10 also comprises a first converter 14 for conversion between AC and DC, which converter therefore comprises an AC side connected to the transformer T1 and a DC side connected to a first reactor L1. The first transformer T1 thus connects the first converter 14 to the first AC power transmission system (not shown). The first converter 14 is connected to a second converter 16 of a second converter station 12 via a DC transmission medium 18, which DC transmission medium maybe a power line 18 such as an overhead line or a cable. As described earlier, the first converter 10 may here be connected to a first end of the transmission medium via a first reactor L1 and the second converter may be connected to a second end of the transmission medium 18 via a second reactor L2.

**[0022]** The second converter 16 also converts between AC and DC and may be an inverter. The second converter station 12 may also include a second transformer T2, which connects the second converter 16 to the second AC power transmission system (not shown).

**[0023]** The converters 14 and 16 may be any type of converters, such as line-commutated Current Source Converters (CSC) or forced commutated Voltage Source Converters (VSC). The converters may more particularly comprise a number of converter valves. A voltage source converter maybe a two-level voltage source converter or a multi-level voltage source converter employing submodules. In series with the transmission medium there is finally also a Direct Current (DC) circuit breaking device 20. Although only one is shown, it should be realized that there may be one such device in the proximity of a converter, for instance in proximity of each converter. There may thus be a device on opposite sides of the transmission medium 18.

**[0024]** The HVDC system in fig. 1 is a monopole system. It should however be realized that the system may also be a bipole system.

**[0025]** Fig. 2 shows another type of HVDC system. The system is here a multi-terminal HVDC system, such as an HVDC system comprising a number of converters converting between AC and DC. Each converter comprises an AC side and a DC side, where the DC side of a third converter 24 is connected to the DC side of a fourth converter 26 via a power transmission medium in the form of a power line that may be a second overhead line or cable 32, the DC side of a fifth converter 28 is connected to the DC side of a sixth converter 30 via a third DC line or cable 34. There is also a fourth DC line or cable 36 interconnecting the DC sides of the third and the fifth converters 24 and 28 as well as a fifth DC line or cable 38 interconnecting the DC sides of the fourth and sixth converters 26 and 30.

**[0026]** As can also be seen there is a corresponding DC circuit breaking device 20 connected in series with all the power lines 32, 34, 36 and 38.

**[0027]** Fig. 3 shows a first embodiment of the DC circuit breaking device 20. The DC circuit breaking device 20 may comprise two parallel branches. There is a first branch comprising a mechanical disconnector, which maybe a so-called ultrafast disconnector UFD, in series with a load commutation switch LCS that is a fast electronic switch. There is also a second branch with a number of series-connected current diverting modules, where each current diverting module comprises a non-linear resistor in parallel with a corresponding electronic power switch. The totality of power switches may together form a main breaker MB, while the totality of non-linear resistors may be seen as forming a surge arrester branch. There is in the example in fig. 3 a first current diverting module comprising a first surge arrester SA1 in parallel with a first power switch S1, a second current diverting module comprising a second surge arrester SA2 in parallel with a second power switch S2, a third current diverting module comprising a third surge arrester SA3 in parallel with a third power switch S3 and finally a fourth current diverting module comprising a fourth surge arrester SA4 in parallel with a fourth power switch S4. Although only four current diverting modules are shown in the figure, it should be known that more or fewer may be included. As an example the number of current diverting modules may range between two and twenty. As another example they may range between six and eight. The main breaker MB is furthermore operable to be opened for diverting a current through the main breaker MB to the non-linear resistors, i.e. to the surge arrester branch.

**[0028]** Each power switch S1, S2, S3 or S4 may be realized in the form of a switching element together with an anti-parallel freewheeling unidirectional conduction element, which may be a diode. In this example the power switches are each realized with switching elements that are controllable to be turned on and off via control terminals, such as gates or bases. In the switches shown here the switching elements are realized as IGBTs (Insulated Gate Bipolar Transistor) and the unidirectional conduc-

tion elements as diodes.

**[0029]** It may also be mentioned that it is possible with other types of switching elements such as for instance BIGTs (Bi-mode Insulated Gate Transistors) or IGCTs (Integrated Gate-Commutated Thyristors). The main breaker MB shown in fig. 3 is only an example of one type of circuit breaker device only capable of performing blocking in one current direction. However, it should be realized that it is possible to modify the main breaker MB so that it can block current in two directions. The same is of course also true for the load commutation switch LCS.

**[0030]** There is also a control unit 40 which is shown as controlling the ultra fast disconnector UFD, the load commutation switch LCS as well as gates of the individual power electronic switches S1, S2, S3 and S4. The control unit 40 may be realized in the form of as computer or processing circuitry, such as a Field-Programmable Gate Array (FPGA).

**[0031]** The purpose of the circuit breaking device 20 being connected in series with a power line is to interrupt the current in the power line and to possibly also obtain a mechanical separation from the power line.

**[0032]** Therefore in case of fault in the HVDC line, such as pole to ground fault or a pole to pole fault, the DC circuit breaking device 20 is operated to interrupt the fault current through the power line and to clear the fault. The operation involves forcing a fault current running through the main breaker MB to be diverted to the surge arrester branch, which typically involves blocking of the main breaker MB. Once the main breaker MB has been blocked, the fault current is forced to flow through the surge arrester branch. This operation is typically performed after the load commutation switch LCS has been blocked and the mechanical disconnector UFD has been opened.

**[0033]** Transition of the fault current from the main breaker MB to the surge arrester branch may take place quickly, such as in the order of a few microseconds. Due to the value of the fault current and small transition time, the rate of change of current (di/dt) through the surge arrester branch is high. The stray parameters of the direct current circuit breaking device, due to connection wires, current sensors, arrester mechanical arrangement and the physical property of the arrester, may lead to a voltage above the designed arrester protective voltage due to high di/dt.

**[0034]** This high voltage developed across the surge arrester branch is seen by the other elements of the DC circuit breaking device 20, i.e. by the mechanical disconnector UFD, the load commutation switch LCS and the main breaker MB. These elements thus have to withstand the additional voltage over and above the arrester protection voltage.

**[0035]** The voltage distribution across each element in the first branch, i.e. the branch comprising the mechanical disconnector UFD and the load commutation switch LCS, during initial transient, mainly depends on the capacitance across it. The net capacitance across the LCS switch in blocked condition is significantly higher than the net capacitance across the UFD in open position. Therefore, the initial peak voltage developed by the arrester branch, along with the stray parameters in other branches, is seen by the UFD during the initial transient and the voltage across the LCS is negligible or is limited to a voltage magnitude by the arrester across it. The voltage across the first branch over time is shown in fig. 4 for a conventionally operated circuit breaking device. There is here a nominal or steady-state operational voltage Vss and an overvoltage or arrestor protection voltage Vp. The main breaker MB, i.e. the totality of power switches maybe set to take the system overrating for which the surge arresters have been designed, i.e. the arrestor protection voltage. The power switches may as an example be designed for an overrating of 40 %. They may thus as an example be designed for a voltage that is 1.4 times the operational steady-state voltage Vss. It can here be seen that the first branch and therefore also the mechanical disconnector UFD may experience a voltage well above the protection voltage Vp.

**[0036]** The various elements, such as the UFD, are designed to withstand the arrester protection voltage Vp with a certain margin. It is not desirable, in practice, to exceed the arrester protection voltage Vp. Exceeding the voltage above the designed maximum blocking voltage may result in failure of one or more of the elements such as of the UFD. Another factor that is critical is the rate of rise of blocking voltage across an open or blocked element, such as an open UFD. Since the arrester conducts almost immediately, the rate of rise of voltage across the element may be high.

**[0037]** It may therefore be necessary to adopt techniques to mitigate the overvoltage seen by elements in parallel with the surge arrester branch, for instance as seen across the UFD, during blocking of the main breaker MB and decrease the rate of rise of voltage across the elements. These parameters are critical in design and dimensioning of elements such as the UFD.

**[0038]** One way to mitigate the voltage overshoot is proposed here. The method, which is a modified circuit breaking activity, is possible to perform due to the modular structure of the used main breaker MB.

**[0039]** The operation will now be described with reference being made also to fig. 5, which shows a flow chart of a method of controlling the DC circuit breaking device 20 and being performed by the control unit 40.

**[0040]** A current is initially, in steady state fault free operation of the system, running through the first branch comprising the mechanical disconnector UFD and load commutation switch LCS. The first branch is thereby the normal current path. Both the mechanical disconnector UFD and the load commutation switch LCS are thereby closed. Also the main breaker MB is closed.

**[0041]** As a fault is detected in the system, the control unit 40 first opens the load commutation switch LCS, step 42, in order to commutate the current over to the main

breaker MB. Once the current has been commutated over to the main breaker MB, the control unit 40 then opens the mechanical disconnector UFD, step 44. Thereby the main current path has been disconnected and the fault current instead runs through the main breaker MB.

**[0042]** Thereafter the main breaker MB is to be opened in order to commutate the fault current over to the surge arrester branch.

**[0043]** This is done through the control unit 40 turning off or blocking the power switches S1, S2, S3 and S4 of the main breaker MB according to a sequential blocking scheme, step 46. The power switches are thus blocked according to a blocking sequence. The sequential blocking scheme defines a sequence of blocking instances at which the power switches are blocked. Thereby at least some of the power switches are being blocked at different points in time.

**[0044]** One example of such a scheme can be understood from fig. 6. Fig. 6 shows the voltage across the first branch and thus also the voltage experienced by the disconnector UFD, during the operation of the main breaker MB according to the sequential blocking scheme. The voltage levels are here the same as those shown in fig. 4.

**[0045]** In the example in fig. 6 the operation of seven power switches is shown. Fig. 6 thus exemplifies the operation of a circuit breaking device comprising seven current diverting modules. The power switches may be set to be blocked sequentially, i.e. in a sequence of blocking instances. In the example in fig. 6, only one power switch is blocked at each blocking instance and the blocking instances are separated by the same blocking instance separation time or time delay..

**[0046]** It can be seen that the overvoltage experienced by the circuit breaking device 20, here exemplified by the mechanical disconnector UFD, is significantly reduced as compared with the case when all power switches were blocked simultaneously, see fig. 4. It is thereby possible to use elements with lower ratings or perhaps increase the period between scheduled maintenance. This is especially advantageous with respect of the ultrafast disconnector UFD, which may be the most sensitive element of the circuit breaking device 20.

**[0047]** The power switches of the main breaker MB may thus be blocked successively, one, two or more at a time, perhaps with a delay, so that the power switches of the current diverting blocks conduct in groups of one, two or more after each other. One power switch may thus be controlled to be blocked at each blocking instance. In case more than one power switch is controlled to be blocked at a blocking instance, then the voltage withstand levels of these power switches may need to be comparable with each other. The voltage developed by each of the current diverting blocks are a fraction of the protection voltage Vp. Therefore, the voltage across the UFD builds to the protection voltage in steps- with a finite delay between each step.

**[0048]** In the present configuration, when the DC breaker operates, the fault current is limited by blocking the main breaker MB and diverting it through the arrester. Since all of the arresters are forced to conduct an arrester protection voltage develops across each module. Therefore, across the UFD the voltage seen will be the superposition of the arrester protection voltage and ringing voltage due to parasitics.

**[0049]** It is observed that the voltage ringing settles after a while. The proposed scheme takes advantage of this fact. As a modular main breaker is used, that is, the main breaker is made up of a series connection of power switches in current diverting blocks, the block structure provides the flexibility to connect several such blocks in series to develop a main breaker with desired voltage level. Each block then receives a separate control command to block or de-block the corresponding power switch. The proposed method takes advantage of this fact. Therefore, when the main breaker MB as a unit has to be blocked, a separate control command is sent to all the power semiconductor switches of the main breaker MB connected in series.

**[0050]** In the disclosed method, the rate of rise of voltage (dv/dt) and the peak voltage across the UFD is controlled by sequentially blocking the main breaker semiconductor switches. The blocking instance separation time or delay between blocking of each main breaker power switch may be so chosen to avoid a large overshoot and to achieve the desired rate of rise of voltage across the element, such as the UFD. The delay may be set such that the amplitude of the ringing experienced by the element is damped to an acceptable level,. The delay may more particularly be set to allow a sufficient degree of the ringing caused by the parasitics of the circuit breaking device to be damped. It may for instance be set so that the amplitude of the ringing is damped to a suitable level where it settles across the element, like 50, 40, 30, 20 or 10 % of the initial ringing amplitude before a following blocking instance takes place.

**[0051]** There are a number of different variations that are possible to make of the above described blocking sequence.

**[0052]** The duration of the sequence is not really time critical as long as it can be completed within a maximum allowed time for completion of the circuit breaking operation after the detection of a fault, which as an example may be 5 ms. The maximum allowed time may then also have to include the opening times of the mechanical disconnector UFD and the load commutation switch LCS as well as the time for receiving a fault indication from a fault detecting device.

**[0053]** Moreover, in the blocking scheme it is possible that more than one power switch is being blocked at the same time. It is thus possible that more than one power switch is blocked at a blocking instance. It is as an example possible that two or even more power switches are blocked at a blocking instance. It is more particularly possible that power switches of current diverting modules that together make up a voltage corresponding to the operational voltage Vss are being blocked at the same

blocking instance. This may in turn be followed by singly blocked power switches. The delay between blocking instances may also depend on the number of power switches being blocked. The delay following a blocking instance may as an example generally be set as n times the delay of a single blocked power switch, where n is the number of simultaneously blocked power switches. Thereby it is clear that the delays between the blocking instances do not have to be equally sized.

**[0054]** It is also possible that one or more of the blocking instances at the end of the sequence, each only involves the blocking of a single power switch. It is for instance possible that the last blocking instance in the sequence only blocks one power switch.

**[0055]** The advantage of this can be clearly seen in fig. 6. The ringing at the last blocking of the sequence will, if the ringing of previous blocking instances have been sufficiently damped, have a low amplitude and thereby the circuit breaking device will essentially only have to be dimensioned for a voltage comprising the rated overvoltage Vp together with the amplitude of the ringing of a singly blocked power switch.

**[0056]** The actual power switch selected for being blocked at a certain blocking instance is not important. The power switches all perform the same function. It may therefore be wise if the order in which the power switches are selected to be blocked in a blocking sequence is changed from time to time. The power switches may thus be controlled to be blocked in a first sequence for a first interrupting of a current through the power line and in a second sequence for a second interrupting of a current through the power line, where the second sequence is different from the first sequence. The order in which power switches are selected in the first sequence may thus be different than the order in which the same power switches are selected in the second following blocking sequence.

**[0057]** The invention has a number of advantages. It mitigates the overvoltages experienced in the circuit breaking device when currents are diverted to the non-linear resistors. This is furthermore obtained without any additional components. It may be implemented only using some modified control software.

**[0058]** As was mentioned above, a control unit may be realized in the form of discrete components, such as one or more FPGAs. However, it may also be implemented in the form of one or more processors with accompanying program memories comprising computer program code that performs the desired control functionality when being run on a processor. A computer program product carrying such code can be provided as a data carrier such as one or more CD ROM discs or one or more memory sticks carrying the computer program code, which performs the above-described control functionality. One such data carrier in the form of a CD ROM disk 48 carrying computer program code 50 is shown in fig. 7.

**[0059]** While the invention has been described in connection with what is presently considered to be most practical and preferred embodiments, it is to be understood that the invention is not to be limited to the disclosed embodiments, but on the contrary, is intended to cover various modifications and equivalent arrangements which fall within the scope of the following claims.

**[0060]** It should for instance be understood that the circuit breaking device may be provided without the first branch. The first branch with mechanical disconnector and optional load commutation switch may thus be omitted. In this case the main breaker is used for conducting current in steady state fault free operation. Therefore the invention is only to be limited by the following claims.

## Claims

1. A direct current circuit breaking device (20) to be connected in series with a power line (18; 32, 34, 36, 38) and comprising:

   a branch comprising a number of series-connected current diverting modules, each current diverting module comprising a non-linear resistor (SA1, SA2, SA3, SA4) in parallel with a corresponding power switch (S1, S2, S3, S4), where the power switches together form a main breaker (MB) operable to be opened for diverting a current through the main breaker to the non-linear resistors (SA1, SA2, SA3, SA4),
   said power switches (S1, S2, S3, S4) being controllable, upon the circuit breaking device being set to interrupt a current through the power line caused by a fault in the power line,
   **characterized in that**,
   said power switches are to be blocked according to a sequential blocking scheme that defines a sequence of blocking instances at which power switches are to be blocked in order to commutate the fault current over to the non-linear resistors,
   wherein the blocking instances are separated by a blocking instance separation time set to allow a ringing amplitude of a ringing voltage to be damped to an acceptable level, where a voltage seen across the non-linear resistors is a superposition of a protection voltage of the non-linear resistors and the ringing voltage.

2. The direct current circuit breaking device (20) according to claim 1, wherein the number of power switches to be blocked at the last blocking instance of the sequence is one.

3. The direct current circuit breaking device (20) according to claim 1 or 2, wherein more than one power switch is controllable to be blocked at one blocking instance, where the voltage withstand levels of these power switches are comparable.

4. The direct current circuit breaking device (20) according to any previous claim, wherein the power switches of a number of current diverting modules together set to hold a voltage corresponding to the nominal operating voltage (Vss) are controllable to be blocked at the same blocking instance.

5. The direct current circuit breaking device (20) according to claim 1 or 2, wherein one power switch is controllable to be blocked at each blocking instance.

6. The direct current circuit breaking device according to any previous claim, wherein said power switches are controllable to be blocked in a first sequence for a first interrupting of a current through the power line (18; 32, 34, 36, 38) and in a second sequence for a second interrupting of a current through the power line (18; 32, 34, 36, 38), where the second sequence is different form the first sequence.

7. The direct current circuit breaking device (20) according to any previous claim, comprising a further branch in parallel with the branch of series-connected current diverting modules, said further branch comprising a mechanical disconnector (UFD) operable to obtain a mechanical separation from the power line.

8. The direct current circuit breaking device (20) according to any previous claim, further comprising a control unit (40) configured to control the blocking of the power switches (S1, S2, S3, S4) according to the sequential blocking scheme.

9. A method of controlling a direct current circuit breaking device (20) when interrupting a current in a power line (18; 22, 24, 26, 28) connected in series with the circuit breaking device, where the circuit breaking device comprises a branch comprising a number of series-connected current diverting blocks, where each current diverting block comprises a non-linear resistor (SA1, SA2, SA3, SA4) in parallel with a corresponding power switch (S1, S2, S3, S4) and the power switches (S1, S2, S3, S4) together form a main breaker (MB), the method being performed in the direct current circuit breaking device (20) during the opening of the main breaker (MB) for diverting a current caused by a fault in the power line to the non-linear resistors (SA1, SA2, SA3, SA4), **characterized in that** the method comprises controlling (46) the power switches (S1, S2, S3, S4) to be blocked according to a sequential blocking scheme that defines a sequence of blocking instances at which power switches are to be blocked in order to commutate the fault current over to the non-linear resistors, wherein the blocking instances are separated by a blocking instance separation time set to allow a ringing amplitude of a ringing voltage to be damped to an acceptable level, where a voltage seen across the non-linear resistors is a superposition of a protection voltage of the non-linear resistors and the ringing voltage.

10. The method according to claim 9, wherein the number of power switches being blocked at the last blocking instance of the sequence is one.

11. The method according to claim 9 or 10, wherein there is a further branch connected in parallel with the branch that comprises a number of series-connected current diverting modules, said further branch comprising a mechanical disconnector (UFD) operable to obtain a mechanical separation from the power line and a load commutation switch (LCS), the method further comprising opening (42) the load commutation switch (LCS) for commutating the current to the main breaker (MB) and opening (44) the mechanical disconnector (UFD) for separating the circuit breaking device from the power line and opening (46) the main breaker (MB) for diverting the current to the non-linear resistors.

12. A computer program product for controlling a direct current circuit breaking device (20) when interrupting currents in a power line (18; 32, 34, 36, 38) connected in series with the circuit breaking device, where the circuit breaking device (20) comprises a branch comprising a number of series-connected current diverting blocks, where each current diverting block comprises a non-linear resistor (SA1, SA2, SA3, SA4) in parallel with a corresponding power switch (S1, S2, S3, S4) and the power switches together form a main breaker (MB), the computer program product comprising a data carrier (48) with computer program code (50) configured to:

control, in the opening of the main breaker (MB) for diverting a current caused by a fault in the power line to the non-linear resistors (SA1, SA2, SA3, SA4), the power switches (S1, S2, S3, S4), **characterized in that**,

the power switches are to be blocked according to a sequential blocking scheme that defines a sequence of blocking instances at which power switches are to be blocked in order to commutate the fault current over to the non-linear resistors,

wherein the blocking instances are separated by a blocking instance separation time set to allow a ringing amplitude of a ringing voltage to be damped to an acceptable level, where a voltage seen across the non-linear resistors is a superposition of a protection voltage of the non-linear resistors and the ringing voltage.

**Patentansprüche**

1. Gleichstrom-Unterbrechungsvorrichtung (20), die mit einer Stromleitung (18; 32, 34, 36, 38) in Reihe zu schalten ist und Folgendes umfasst:

   einen Zweig, der eine Anzahl in Reihe geschalteter Stromumleitungsmodule umfasst, wobei jedes Stromumleitungsmodul einen nichtlinearen Widerstand (SA1, SA2, SA3, SA4) parallel zu einem entsprechenden Leistungsschalter (S1, S2, S3, S4) umfasst, wobei die Leistungsschalter zusammen einen Hauptunterbrecher (MB) bilden, der betreibbar ist, zum Umleiten eines Stroms durch den Hauptunterbrecher zu den nichtlinearen Widerständen (SA1, SA2, SA3, SA4) geöffnet zu werden,
   wobei die Leistungsschalter (S1, S2, S3, S4) aufgrund dessen, dass die Unterbrechungsvorrichtung derart eingestellt ist, dass ein Strom durch die Stromleitung unterbrochen wird, der durch einen Fehler in der Stromleitung bewirkt wird, steuerbar sind,
   **dadurch gekennzeichnet, dass** die Leistungsschalter gemäß einem sequentiellen Sperrschema gesperrt werden sollen, das eine Abfolge von Sperrzeitpunkten definiert, zu denen Leistungsschalter gesperrt werden sollen, um den Fehlerstrom über die nichtlinearen Widerstände umzuschalten,
   wobei die Sperrzeitpunkte durch eine Sperrzeitpunkt-Trennungszeit getrennt sind, die derart eingestellt ist, dass ermöglicht wird, dass eine Überschwingamplitude einer Überschwingspannung auf einen annehmbaren Pegel gedämpft wird, wobei eine Spannung, die über den nichtlinearen Widerständen anliegt, eine Überlagerung einer Schutzspannung der nichtlinearen Widerstände und der Überschwingspannung ist.

2. Gleichstrom-Unterbrechungsvorrichtung (20) nach Anspruch 1, wobei die Anzahl der Leistungsschalter, die zum letzten Sperrzeitpunkt der Abfolge gesperrt werden sollen, eins ist.

3. Gleichstrom-Unterbrechungsvorrichtung (20) nach Anspruch 1 oder 2, wobei mehr als ein Leistungsschalter derart steuerbar ist, dass er zu einem Sperrzeitpunkt gesperrt wird, zu dem die Stehspannungspegel dieser Leistungsschalter vergleichbar sind.

4. Gleichstrom-Unterbrechungsvorrichtung (20) nach einem der vorhergehenden Ansprüche, wobei die Leistungsschalter einer Anzahl von Stromumleitungsmodulen, die zusammen derart eingestellt sind, dass sie eine Spannung halten, die der Nennbetriebsspannung (Vss) entspricht, derart steuerbar sind, dass sie zu demselben Sperrzeitpunkt gesperrt werden.

5. Gleichstrom-Unterbrechungsvorrichtung (20) nach Anspruch 1 oder 2, wobei ein Leistungsschalter derart steuerbar ist, dass er zu jedem Sperrzeitpunkt gesperrt wird.

6. Gleichstrom-Unterbrechungsvorrichtung nach einem der vorhergehenden Ansprüche, wobei die Leistungsschalter derart steuerbar sind, dass sie in einer ersten Abfolge für eine erste Unterbrechung eines Stroms durch die Stromleitung (18; 32, 34, 36, 38) und in einer zweiten Abfolge für eine zweite Unterbrechung eines Stroms durch die Stromleitung (18; 32, 34, 36, 38) gesperrt werden, wobei die zweite Abfolge von der ersten Abfolge verschieden ist.

7. Gleichstrom-Unterbrechungsvorrichtung (20) nach einem der vorhergehenden Ansprüche, die einen weiteren Zweig parallel zu dem Zweig mit in Reihe geschalteten Stromumleitungsmodulen umfasst, wobei der weitere Zweig einen mechanischen Trennschalter (UFD) umfasst, der betreibbar ist, eine mechanische Trennung von der Stromleitung zu erhalten.

8. Gleichstrom-Unterbrechungsvorrichtung (20) nach einem der vorhergehenden Ansprüche, die ferner eine Steuereinheit (40) umfasst, die konfiguriert ist, das Sperren der Leistungsschalter (S1, S2, S3, S4) gemäß dem sequentiellen Sperrschema zu steuern.

9. Verfahren zum Steuern einer Gleichstrom-Unterbrechungsvorrichtung (20), wenn ein Strom in einer Stromleitung (18; 22, 24, 26, 28) unterbrochen wird, die mit der Unterbrechungsvorrichtung in Reihe geschaltet ist, wobei die Unterbrechungsvorrichtung einen Zweig umfasst, der eine Anzahl in Reihe geschalteter Stromumleitungsblöcke umfasst, wobei jeder Stromumleitungsblock einen nichtlinearen Widerstand (SA1, SA2, SA3, SA4) parallel zu einem entsprechenden Leistungsschalter (S1, S2, S3, S4) umfasst und die Leistungsschalter (S1, S2, S3, S4) zusammen einen Hauptunterbrecher (MB) bilden, wobei das Verfahren in der Gleichstrom-Unterbrechungsvorrichtung (20) während des Öffnens des Hauptunterbrechers (MB) zum Umleiten eines Stroms, der durch einen Fehler in der Stromleitung bewirkt wird, zu den nichtlinearen Widerständen (SA1, SA2, SA3, SA4) durchgeführt wird,

   **dadurch gekennzeichnet, dass** das Verfahren das Steuern (46) der Leistungsschalter (S1, S2, S3, S4), derart, dass sie gemäß einem sequentiellen Sperrschema gesperrt werden, das eine Abfolge von Sperrzeitpunkten definiert, zu denen Leistungsschalter gesperrt werden sollen,

um den Fehlerstrom über die nichtlinearen Widerstände umzuschalten, umfasst,
wobei die Sperrzeitpunkte durch eine Sperrzeitpunkt-Trennungszeit getrennt sind, die derart eingestellt ist, dass ermöglicht wird, dass eine Überschwingamplitude einer Überschwingspannung auf einen annehmbaren Pegel gedämpft wird, wobei eine Spannung, die über den nichtlinearen Widerständen anliegt, eine Überlagerung einer Schutzspannung der nichtlinearen Widerstände und der Überschwingspannung ist.

**10.** Verfahren nach Anspruch 9, wobei die Anzahl der Leistungsschalter, die zum letzten Sperrzeitpunkt der Abfolge gesperrt werden sollen, eins ist.

**11.** Verfahren nach Anspruch 9 oder 10, wobei es einen weiteren Zweig gibt, der zu dem Zweig, der eine Anzahl in Reihe geschalteter Stromumleitungsmodule umfasst, parallel geschaltet ist, wobei der weitere Zweig einen mechanischen Trennschalter (UFD), der betreibbar ist, eine mechanische Trennung von der Stromleitung zu erhalten, und einen Lastumschaltungsschalter (LCS) umfasst, wobei das Verfahren ferner das Öffnen (42) des Lastumschaltungsschalters (LCS) zum Umschalten des Stroms zum Hauptunterbrecher (MB) und das Öffnen (44) des mechanischen Trennschalters (UFD) zum Trennen der Unterbrechungsvorrichtung von der Stromleitung und das Öffnen (46) des Hauptunterbrechers (MB) zum Umleiten des Stroms zu den nichtlinearen Widerständen umfasst.

**12.** Computerprogrammprodukt zum Steuern einer Gleichstrom-Unterbrechungsvorrichtung (20), wenn Ströme in einer Stromleitung (18; 32, 34, 36, 38) unterbrochen werden, die mit der Unterbrechungsvorrichtung in Reihe geschaltet ist, wobei die Unterbrechungsvorrichtung (20) einen Zweig umfasst, der eine Anzahl in Reihe geschalteter Stromumleitungsblöcke umfasst, wobei jeder Stromumleitungsblock einen nichtlinearen Widerstand (SA1, SA2, SA3, SA4) parallel zu einem entsprechenden Leistungsschalter (S1, S2, S3, S4) umfasst und die Leistungsschalter zusammen einen Hauptunterbrecher (MB) bilden, wobei das Computerprogrammprodukt einen Datenträger (48) mit Computerprogrammcode (50) umfasst, der konfiguriert ist zum:

Steuern der Leistungsschalter (S1, S2, S3, S4) beim Öffnen des Hauptunterbrechers (MB) zum Umleiten eines Stroms, der durch einen Fehler in der Stromleitung bewirkt wird, zu den nichtlinearen Widerständen (SA1, SA2, SA3, SA4),
**dadurch gekennzeichnet, dass** die Leistungsschalter gemäß einem sequentiellen Sperrschema gesperrt werden sollen, das eine Abfolge von Sperrzeitpunkten definiert, zu denen Leistungsschalter gesperrt werden sollen, um den Fehlerstrom über die nichtlinearen Widerstände umzuschalten,
wobei die Sperrzeitpunkte durch eine Sperrzeitpunkt-Trennungszeit getrennt sind, die derart eingestellt ist, dass ermöglicht wird, dass eine Überschwingamplitude einer Überschwingspannung auf einen annehmbaren Pegel gedämpft wird, wobei eine Spannung, die über den nichtlinearen Widerständen anliegt, eine Überlagerung einer Schutzspannung der nichtlinearen Widerstände und der Überschwingspannung ist.

**Revendications**

**1.** Dispositif de coupure de circuit à courant continu (20) destiné à être connecté en série à une ligne d'alimentation électrique (18 ; 32, 34, 36, 38) et comprenant :

une branche comprenant un certain nombre de modules de déviation de courant connectés en série, chaque module de déviation de courant comprenant une résistance non linéaire (SA1, SA2, SA3, SA4) en parallèle avec un interrupteur de puissance correspondant (S1, S2, S3, S4), où les interrupteurs de puissance forment ensemble un disjoncteur principal (MB) pouvant être ouvert pour dévier un courant à travers le disjoncteur principal vers les résistances non linéaires (SA1, SA2, SA3, SA4),
lesdits interrupteurs de puissance (S1, S2, S3, S4) pouvant être commandés, lorsque le dispositif de coupure de circuit est réglé, pour interrompre un courant à travers la ligne d'alimentation électrique causé par un défaut dans la ligne d'alimentation électrique,
**caractérisé en ce que** :

lesdits interrupteurs de puissance doivent être bloqués selon un schéma de blocage séquentiel qui définit une séquence d'instances de blocage auxquelles les interrupteurs de puissance doivent être bloqués afin de commuter le courant de défaut sur les résistances non linéaires,
où les instances de blocage sont séparées par un temps de séparation d'instance de blocage défini pour permettre à une amplitude de sonnerie d'une tension de sonnerie d'être amortie à un niveau acceptable, où une tension observée aux bornes des résistances non linéaires est une superposition d'une tension de protection des résistances non linéaires et de la tension de son-

nerie.

**2.** Dispositif de coupure de circuit à courant continu (20) selon la revendication 1, dans lequel le nombre d'interrupteurs de puissance à bloquer à la dernière instance de blocage de la séquence est de un.

**3.** Dispositif de coupure de circuit à courant continu (20) selon la revendication 1 ou la revendication 2, dans lequel plus d'un interrupteur de puissance peut être commandé pour être bloqué à une instance de blocage, où les niveaux de résistance à la tension de ces interrupteurs de puissance sont comparables.

**4.** Dispositif de coupure de circuit à courant continu (20) selon l'une quelconque des revendications précédentes, dans lequel les interrupteurs de puissance d'un certain nombre de modules de dérivation de courant réglés ensemble pour maintenir une tension correspondant à la tension de fonctionnement nominale (Vss) peuvent être commandés pour être bloqués à la même instance de blocage.

**5.** Dispositif de coupure de circuit à courant continu (20) selon la revendication 1 ou la revendication 2, dans lequel un interrupteur de puissance peut être commandé pour être bloqué à chaque instance de blocage.

**6.** Dispositif de coupure de circuit à courant continu selon l'une quelconque des revendications précédentes, dans lequel lesdits interrupteurs de puissance peuvent être commandés pour être bloqués dans une première séquence pour une première interruption d'un courant à travers la ligne d'alimentation électrique (18 ; 32, 34, 36, 38) et dans une seconde séquence pour une seconde interruption d'un courant à travers la ligne d'alimentation électrique (18 ; 32, 34, 36, 38), où la seconde séquence est différente de la première séquence.

**7.** Dispositif de coupure de circuit à courant continu (20) selon l'une quelconque des revendications précédentes, comprenant une autre branche en parallèle avec la branche des modules de déviation de courant connectés en série, ladite autre branche comprenant un dispositif de déconnexion mécanique (UFD) pouvant fonctionner pour obtenir une séparation mécanique de la ligne d'alimentation électrique.

**8.** Dispositif de coupure de circuit à courant continu (20) selon l'une quelconque des revendications précédentes, comprenant en outre une unité de commande (40) configurée pour commander le blocage des interrupteurs de puissance (S1, S2, S3, S4) selon le schéma de blocage séquentiel.

**9.** Procédé de commande d'un dispositif de coupure de circuit à courant continu (20) lors de l'interruption d'un courant dans une ligne d'alimentation électrique (18 ; 22, 24, 26, 28) connectée en série au dispositif de coupure de circuit, où le dispositif de coupure de circuit comprend une branche comprenant un certain nombre de blocs de dérivation de courant connectés en série, où chaque bloc de déviation de courant comprend une résistance non linéaire (SA1, SA2, SA3, SA4) en parallèle avec un interrupteur de puissance correspondant (S1, S2, S3, S4) et les interrupteurs de puissance (S1, S2, S3, S4) forment ensemble un disjoncteur principal (MB), le procédé étant exécuté dans le dispositif de coupure de circuit à courant continu (20) pendant l'ouverture du disjoncteur principal (MB) pour dévier un courant provoqué par un défaut dans la ligne d'alimentation électrique vers les résistances non linéaires (SA1, SA2, SA3, SA4), **caractérisé en ce que** le procédé comprend de commander (46) les interrupteurs de puissance (S1, S2, S3, S4) à bloquer selon un schéma de blocage séquentiel qui définit une séquence d'instances de blocage auxquelles les interrupteurs de puissance doivent être bloqués afin de commuter le courant de défaut sur les résistances non linéaires, où les instances de blocage sont séparées par un temps de séparation d'instance de blocage défini pour permettre à une amplitude de sonnerie d'une tension de sonnerie d'être amortie à un niveau acceptable, où une tension observée aux bornes des résistances non linéaires est une superposition d'une tension de protection des résistances non linéaires et de la tension de sonnerie.

**10.** Procédé selon la revendication 9, dans lequel le nombre d'interrupteurs de puissance étant bloqués à la dernière instance de blocage de la séquence est de un.

**11.** Procédé selon la revendication 9 ou la revendication 10, dans lequel il existe une autre branche connectée en parallèle avec la branche qui comprend un certain nombre de modules de dérivation de courant connectés en série, ladite autre branche comprenant un dispositif de déconnexion mécanique (UFD) pouvant fonctionner pour obtenir une séparation mécanique de la ligne d'alimentation électrique et un interrupteur de commutation de charge (LCS), le procédé comprenant en outre d'ouvrir (42) l'interrupteur de commutation de charge (LCS) pour commuter le courant vers le disjoncteur principal (MB) et d'ouvrir (44) le dispositif de déconnexion mécanique (UFD) pour séparer le dispositif de coupure de circuit de la ligne d'alimentation électrique et ouvrir (46) le disjoncteur principal (MB) pour dévier le courant vers les résistances non linéaires.

**12.** Produit programme informatique pour commander

un dispositif de coupure de circuit à courant continu (20) lors de l'interruption des courants dans une ligne d'alimentation électrique (18 ; 32, 34, 36, 38) connectée en série au dispositif de coupure de circuit, où le dispositif de coupure de circuit (20) comprend une branche comprenant un certain nombre de blocs de déviation de courant connectés en série, où chaque bloc de déviation de courant comprend une résistance non linéaire (SA1, SA2, SA3, SA4) en parallèle avec un interrupteur de puissance correspondant (S1, S2, S3, S4) et les interrupteurs de puissance forment ensemble un disjoncteur principal (MB), le produit programme informatique comprenant un support de données (48) avec un code de programme informatique (50) configuré pour :

commander, lors de l'ouverture du disjoncteur principal (MB) pour dévier un courant provoqué par un défaut dans la ligne d'alimentation électrique vers les résistances non linéaires (SA1, SA2, SA3, SA4), les interrupteurs de puissance (S1, S2, S3, S4), **caractérisé en ce que** les interrupteurs de puissance doivent être bloqués selon un schéma de blocage séquentiel qui définit une séquence d'instances de blocage auxquelles les interrupteurs de puissance doivent être bloqués afin de commuter le courant de défaut sur les résistances non linéaires,
où les instances de blocage sont séparées par un temps de séparation d'instance de blocage défini pour permettre à une amplitude de sonnerie d'une tension de sonnerie d'être amortie à un niveau acceptable, où une tension observée aux bornes des résistances non linéaires est une superposition d'une tension de protection des résistances non linéaires et de la tension de sonnerie.

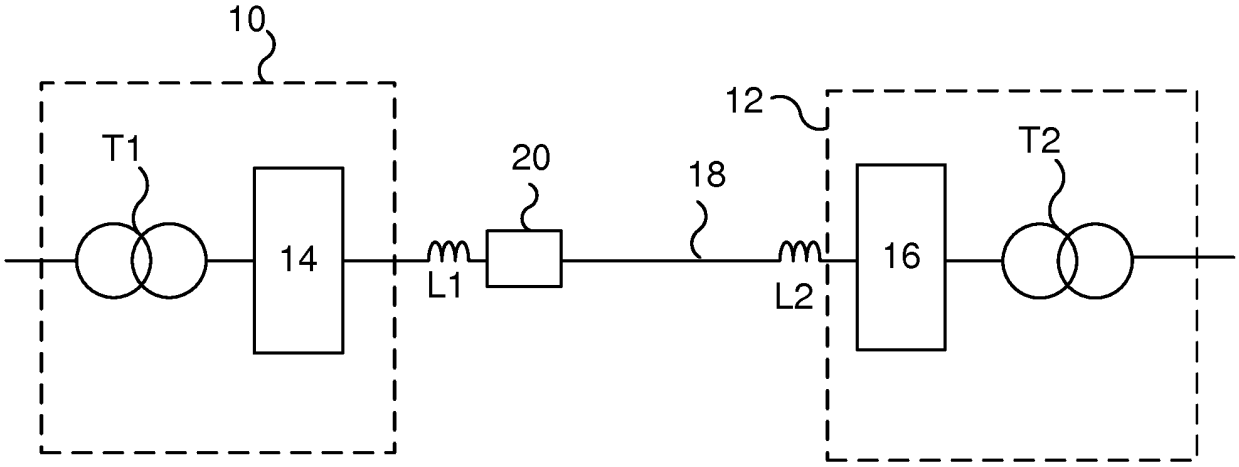


Fig. 1

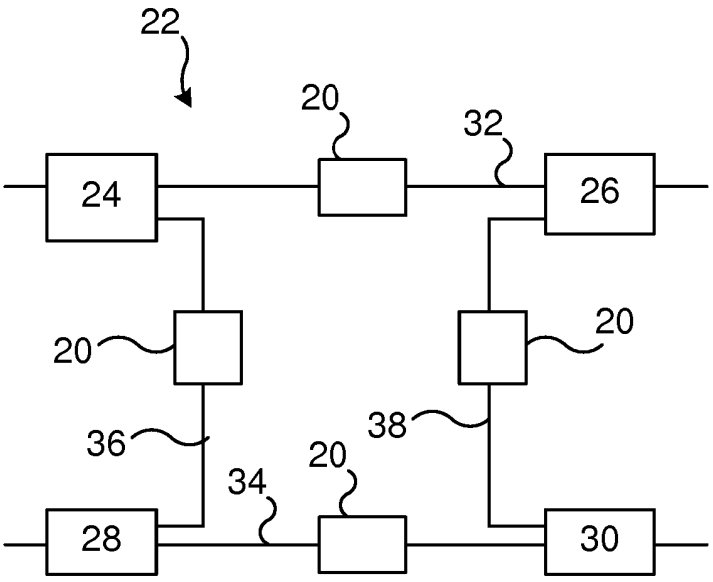


Fig. 2

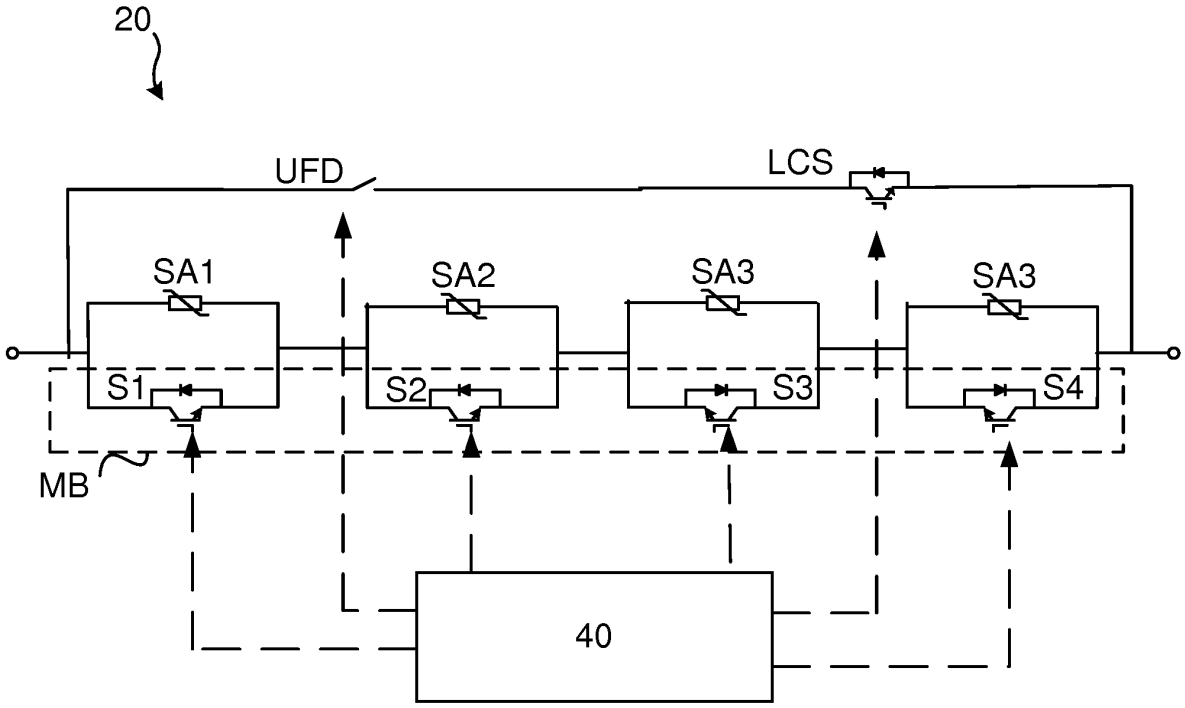


Fig. 3

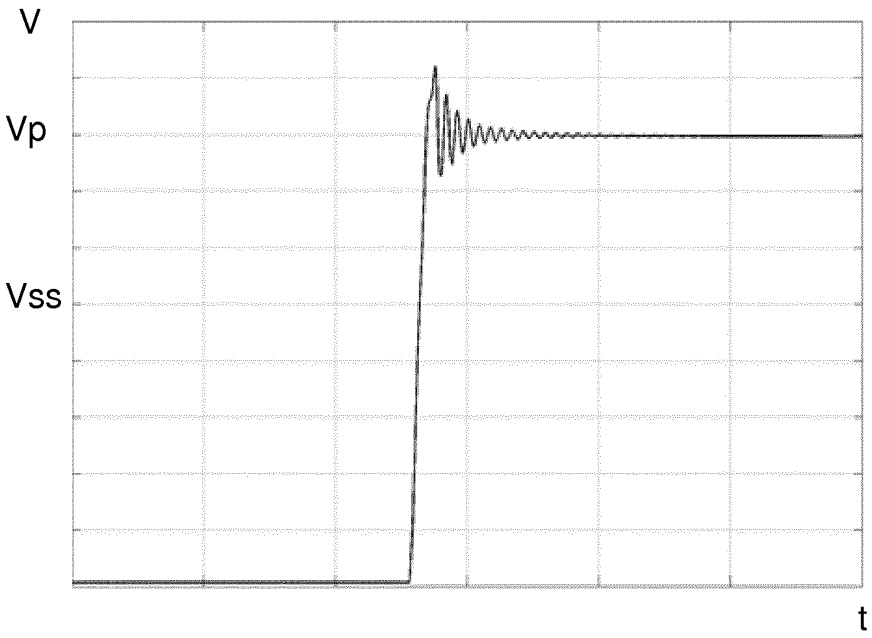


Fig. 4

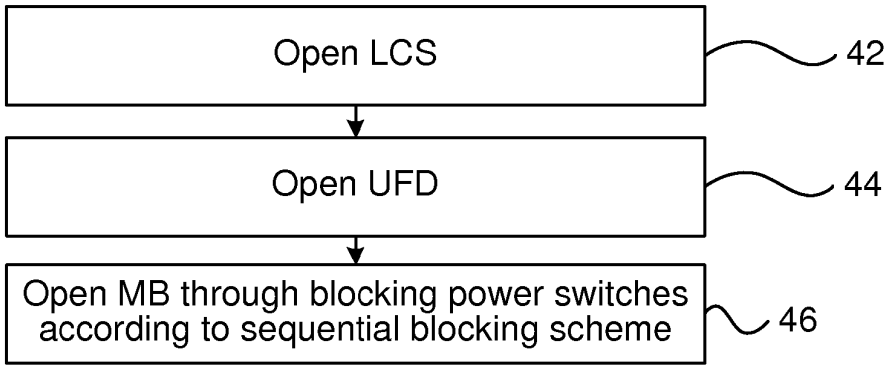


Fig. 5

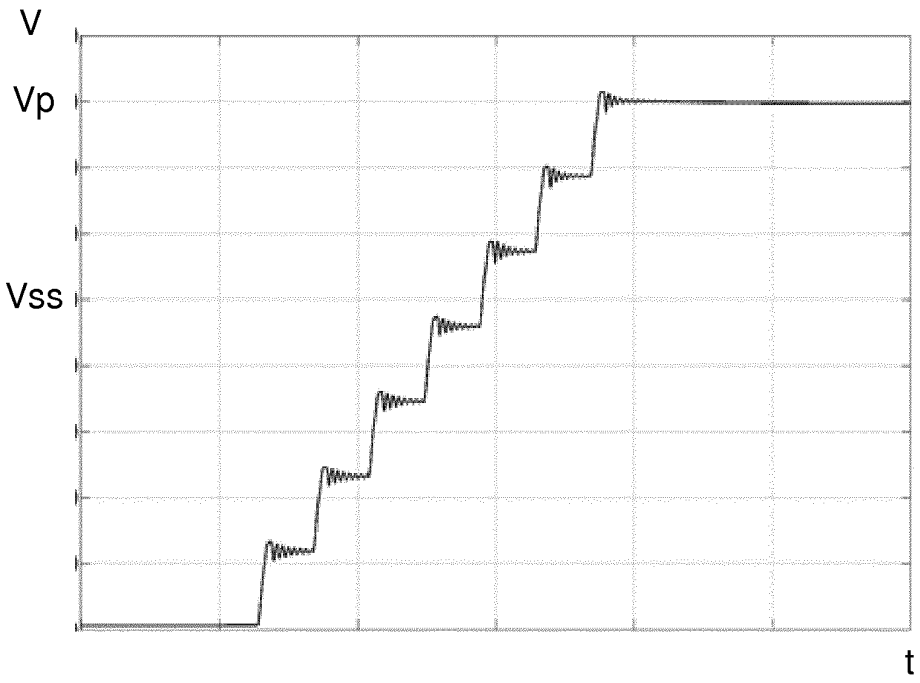


Fig. 6

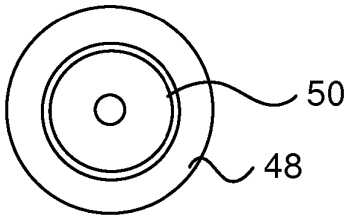


Fig. 7

## REFERENCES CITED IN THE DESCRIPTION

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