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(54) METHOD FOR FABRICATING DIELECTRIC MICRO-SPACERS ON DIFFERENT SUBSTRATES

(57) Method for fabricating dielectric micro-spacers, DMSs, comprising the following steps:
A. performing a photoresist deposition of a thin photoresist film on a surface of a substrate, the substrate being a metal, or a semiconductor or an insulator;
B. patterning the photoresist film for obtaining a photoresist patter;
C. performing a dielectric deposition of a dielectric layer by additive deposition techniques, the dielectric layer comprising a first dielectric pattern conformal to the photoresist pattern and a second dielectric pattern corresponding to areas of the first surface that are not occupied by the photoresist pattern, the dielectric layer being highly electrical resistive and poorly thermal conductive, having an electrical resistivity ranging from 10^2 Ω cm to 10^{18} Ω cm and a thermal conductivity ranging from 10^{-3} W/(cm K) to 10 W/(cm K).
D. removing the photoresist pattern, whereby the first dielectric pattern deposited on the photoresist pattern is removed and the second dielectric pattern remaining unaltered and forming an array of DMSs.

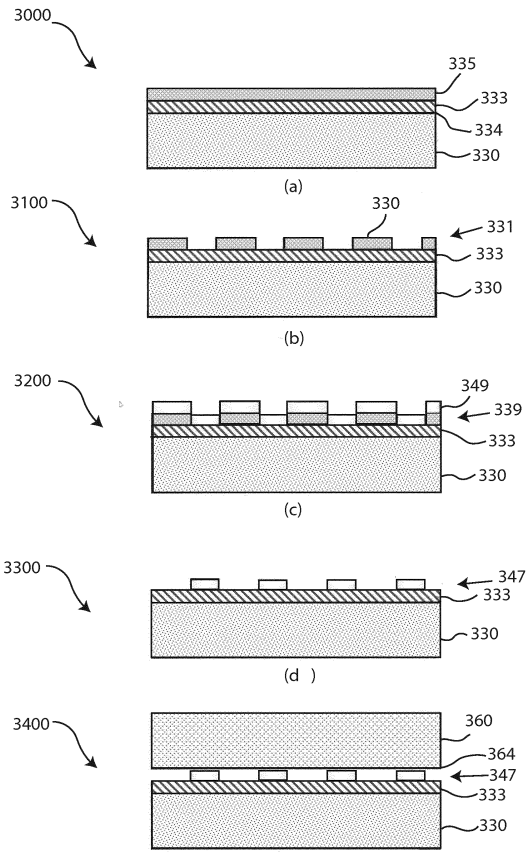

Fig. 3

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Description

[0001] The project leading to this application, that has been maintained confidential and has not been publicly disclosed so far, has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 754568.

[0002] The present invention relates to a method for fabricating dielectric micro-spacers, DMSs, able to physically separate two surfaces at the micrometre scale and to ensure both a thermal and electrical separation between such surfaces maintaining their mechanical and functional properties at high temperature and in harsh environment. The method of the present invention is able to operate in a controlled, versatile, efficient, reliable, simple, and cost-effective way.

[0003] A lot of devices belonging to a wide range of technological fields need to establish a fixed distance between two surfaces while ensuring thermal and/or electric insulation between them, as described hereinafter.

[0004] For example, thermionic devices for energy conversion, TECs, operate as thermal vacuum diodes, and require very high operating temperatures (> 600 °C), whereas in case of photon-enhanced TECs the operating temperatures are lower (> 80 °C). In many cases, TECs are suitable for operation in extremely hot environments, such as nuclear reactors, propulsion systems in spacecrafts, solar concentrating systems, combustion chambers in petrol and/or air engines, or industrial furnaces, where they can be successfully employed as thermal energy recovery systems. The development of a spacer able to maintain a gap between the electrodes of few micrometres is a primary condition for the efficiency of a vacuum diode. The optimal gap value mainly depends on the TEC hot cathode operating temperature, but gaps larger than few micrometres induce a strong reduction of the established current between the electrodes, and consequently of the overall efficiency of the conversion module. Conversely, a gap between cathode and anode narrower than the optimal one is not desirable since it may cause anode overheating owing to near-field effects, resulting anyway in a conversion efficiency drop-off. Up to now, a widespread application of TECs was severely limited exactly because of the absence of a similar technology, substituted in a palliative way by the use of caesium vapours, which are toxic and lead to a significant reduction of efficiency, and magnetic fields, usually associated to the use of large magnets hampering downscalable systems.

[0005] In the field of microelectronics, lumped elements for RF and microwave circuits technology make large use of air-bridges and dielectric crossovers. The primary purpose of air-bridges and dielectric crossovers is to provide a cross-connection for two non-connecting printed transmission-line sections as shown in Figure 1. They are also commonly employed in transistors (e.g. to create a non-connecting crossover between a multiple source and gate, or emitter and base), electrodes, spiral inductors, transformers, metal-insulator-metal capacitors (to improve the breakdown voltage), and other RF and microwave circuits. Air-bridges and dielectric crossovers are also used to reduce the parasitic capacitance between the conductors and the ground plane in MMICs (i.e. Monolithic Microwave Integrated Circuits), thus increasing the maximum operating frequency of the devices. Air-bridges use air as the dielectric between the two conductors, whereas dielectric crossovers employ a layer of low dielectric constant material, such as polyimide or benzocyclobutene (BCB). Both air-bridges and dielectric crossovers have their own advantages and drawbacks:

- Air-bridges. Being the primary function of air-bridges and dielectric crossovers to provide a perfect electrical insulation between two transmission lines (Line 1 and Line 2 in Figure 1a), air-bridges are undoubtedly preferable to dielectric crossovers, obviously because air has the lowest dielectric constant (approximatively equal to the vacuum one). On the other hand, air-bridges require very complex technological steps for their fabrication (e.g. prolonged chemical etching to "empty" the volume between Line 1 and Line 2 of Figure 1a), which result in a non-optimal process yield. Furthermore, the mechanical stability of the structure poses a constraint on the maximum length of the bridge: air-bridge collapse is observed rather frequently, further affecting the process yield.
- Dielectric crossovers. The advantages of crossovers if compared to air-bridges are a simpler fabrication technology (mostly because there's no need to "empty" the inter-line space) and, obviously, a significantly better mechanical stability, acting the dielectric film also as a mechanical support for the overhead part of Line 1 of Figure 1b. However, low dielectric constant materials (such as polyimides and BCB) are only partially suitable to work in harsh environments: indeed, whilst the high operating temperature is not an issue (polyimides work well up to 250 - 300°C), radiation hardness is very poor. For example, electric conductivity of polyimide has been recently found to increase dramatically (several orders of magnitude) with increased electron exposure (Cooper et al., "Effects of Radiation Damage on Polyimide Resistivity", Journal of Spacecraft and Rockets, Vol. 54, No. 2 (2017), pp. 343-348).

[0006] Thermo-tunnel diodes are innovative devices for thermal energy recovery, and can be efficiently exploited in every field of application in which intermediate operating temperatures (<300 °C) are concerned, i.e. not high enough to ensure an efficient performance of pure thermionic devices. This is the case, for example, of all the automotive systems excluding the components of the exhaust system (e.g. engine compartment and transmission, wheel-ABS sensors, etc.), where temperatures as

high as 800 °C can be reached. By coating the radiator with thermo-tunnel diodes it would be possible to double the engine's efficiency, because it's possible to eliminate the pumping, friction and incomplete fuel combustion loss. In its simplest form, a thermo-tunnel diode consists of two electrodes with a spacing of only a few nanometers, such that electrons are able to tunnel from one electrode to the other. However, because of the extremely narrow inter-electrode space, the two electrodes will get very likely into contact due to thermal expansion of metals at even moderate temperatures, causing a short-circuit and consequently a device failure. This is the reason why thermo-tunnel diodes, despite their very high potential, are still at a prototype level, and have not yet been developed on a large scale.

[0007] Most of the above mentioned drawbacks and disadvantages are overcome by an array of dielectric solid microspacers that keeps two surfaces well separated but very close to each other avoiding any point of contact, and ensuring that the volume of space between the surfaces (namely the inter-surface gap) is occupied by a solid material as few as possible, which means that the inter-surface gap should be almost entirely an empty space (i.e. a vacuum or a gas-filled space). Such array of DMSs has to be mechanically, chemically, and physically stable in a broad range of high temperatures, from room temperature to values even >500 °C, and in harsh environments such as for example space and nuclear reactors, for maintaining the fixed distance between the two surfaces to be separated and ensuring the thermal and electric insulation between them.

[0008] In fact, the exploitation of DMSs in thermionic devices for energy conversion improves their efficiency and avoids using caesium vapours and magnetic fields, thus improving environmental sustainability and scalability of devices. In the automotive field, among the different powertrain components, those related to the combustion chamber and the exhaust systems may reach significantly high temperatures (500 °C - 800 °C), enabling the possibility of applying thermionic devices exploiting DMSs. The integration of arrays of thermionic energy converters equipped with DMSs, able to convert the exhaust heat into electric power, can be successfully used to create an additional energy source (for example supporting the car battery or supplying low-power devices, such as LEDs, actuators, or even the MEMS sensors themselves). In fact, it is possible to compensate the energy losses of a thermal engine deriving from pumping, friction and incomplete fuel combustion by thermionic diodes that generate an equivalent power amount. Coating the radiator and the exhaust system with them could allow for doubling the engine efficiency.

[0009] Moreover, DMSs may represent the optimal solution for lumped elements for RF and microwave circuits, because they represent the perfect trade-off between air-bridges and dielectric crossovers, retaining all the advantages of the two technologies and removing their drawbacks:

- DMSs ensure approximatively the same dielectric behaviour of air-bridges (being the inter-line space only minimally occupied by the micro-spacers), but constraints on the maximum length of the bridge are removed, because DMSs act as bridge piers, allowing for a practically unlimited length without risk of collapse. Also, the fabrication process is slightly more simple and reliable than air-bridges, resulting in a better process yield.
- DMSs can be made up of are radiation-hard materials, such as for example alumina and zirconia. This overcomes the limitations of conventional dielectric crossovers in harsh environments, where a significant amount of ionizing radiation may be present.

[0010] Also, DMSs may represent a turning point for thermo-tunnel diode technology, avoiding any kind of short circuit, and allowing at the same time an efficient electron tunnelling by maximizing the cathode free surface. An inter-electrode space of a few nanometres, which is a distance about two orders of magnitude smaller than the case of a thermionic energy converter, represents a challenge for DMS technology itself. However, the technological improvements disclosed in the present invention below, may overcome in the short term this limitation, mostly through the employment of planarization techniques such as CMP (Chemical Mechanical Planarization).

[0011] Several documents of prior art disclose methods for realizing micrometre-scale spacers whose aim is either thermally or electrically insulate two surfaces kept at fixed distance. However such methods are not suitable to obtain spacers for more than one purpose per time.

[0012] Even more critical is the fact that most of these methods have a top-down approach performed by a subtractive manufacturing, by first depositing a continuous film of the spacing material onto the surface of a substrate, and then fabricating the desired pattern, i.e the array of microspacers, by selective removal of the deposited material. The selective removal usually involves wet or dry etching performed by acids or aggressive ionized plasmas (e.g. using techniques as semi-isotropic dry plasma etching, reactive ion etching, or sputter etching), thus damaging some kind of substrates such as metallic ones. Therefore only substrates that do not undergo deterioration during the removal steps of the method can be used. In particular, prior art documents only disclose methods for fabricating micro-spacers onto semiconductor substrates.

[0013] It is an object of this invention to overcome the disadvantages described above, allowing for the fabrication of solid dielectric micro-spacers on different types of substrates, such as metals, semiconductors, or insulators, ensuring a mechanical separation and a thermal and electrical insulation between the substrate surface and another surface facing it at a distance of few micrometres.

[0014] It is specific subject-matter of the present inven-

tion a method for fabricating an array of DMSs as described in the independent claim 1.

[0015] Further embodiments of the method according to the invention are described in the dependent claims.

[0016] It is antoher specific subject-matter of the present invention a device as described in the independent claim 10.

[0017] Further embodiment of the device according to the invention is described in the dependent claim 11.

[0018] It is antoher specific subject-matter of the present invention a device as described in the independent claim 12.

[0019] Further embodiment of the device according to the invention is described in the dependent claim 13.

[0020] The advantages offered by the method according to the invention with respect to the prior art solutions are numerous and significant.

[0021] First, the method is based on a bottom-up approach performed by an addictive manufacturing, i.e. DMSs arrays are fabricated by depositing a conformal film of the dielectric material onto the patterned substrate, then lifting-off the masking layer. This, advantageously, allows for the use of a wider selection of substrates (e.g metallic substrates) with respect to the state-of-the-art methods. Another advantage is that the method of the present invention allows obtaining thermal and electrical barriers between two surfaces kept at a fixed distance that can be used in devices in a wide range of different technological applications. Furthermore, the method fabricates thermal and electrical dielectric (e.g. alumina, zirconia) barriers that are mechanically and chemically-physically stable at high temperature and in harsh environments. Finally, it's worth recalling that the method for fabricating DMSs is scalable, cost-effective, can be implemented by limited-size deposition systems, and allows for an accurate and real-time control of all the fabrication parameters.

[0022] The present invention will be described, by way of illustration, but not by way of limitation, according to its preferred embodiments, with particular reference to the Figures of the accompanying drawings, in which:

Figure 1 shows air-bridges (a) and dielectric cross-overs (b) currently employed in the technology of lumped elements for RF and microwave integrated circuits;

Figure 2 shows a block diagram of a first preferred embodiment of the method for fabricating an array of DMSs according to the invention;

Figures 3(a)-3(e) schematically illustrate cross-section views of sequential stages of the method for fabricating an array of DMSs of Figure 2 using of a positive photoresist film;

Figure 4 shows a block diagram of a second preferred embodiment of the method for fabricating an array of DMSs according to the invention;

Figures 5(a)-5(g) schematically illustrate cross-section views of sequential stages of the method for fabricating an array of DMSs of Figure 4;

Figure 6 shows a sketch of a preferred embodiment of a sputtering apparatus for carrying out the method for fabricating an array of DMSs of Figures 3;

Figures 7(a)-7(b) show scanning electron micrographs (SEM) of an array of DMSs obtained by carrying out a second embodiment of the invention.

[0023] In the Figures, identical reference numerals will be used for alike elements.

[0024] With reference to Figures 2 and 3, a first preferred embodiment of the method according to the present invention is described. It comprises a preliminary deposition 205 of a coating film 333 on a first surface 334 of a substrate 330. This coating thin film 333 induces specific optical and electronic properties to the substrate 330. For example, alkali metals reduce the work function of a substrate and noble metals increase the optical reflectance of a substrate. Moreover, the coating thin film may reduce the surface roughness of the substrate. Then a photoresist deposition 210 of a thin positive photoresist film 335 on the coating film 333 is performed. In other embodiments of the method according to the invention, a deposition step of a thin negative photoresist film is performed. The photoresist deposition 210 allows obtaining a substrate/coating film/photoresist film system 3000 shown in the cross-section of Figure 3(a). In other embodiments of the method according to this invention, the method includes the deposition 210 of the thin photoresist film 335 directly onto a first surface 334 of a substrate 330 without the preliminary deposition 205 of a coating film, thus obtaining a substrate/photoresist film system. The techniques of both preliminary deposition 205 of a coating film and photoresist deposition 210 are selected from the group consisting of spin coating, dip coating, roller coating, curtain coating, extrusion coating, meniscus coating, spray casting, silk screen printing, sputtering, thermal evaporation, electron-beam evaporation, pulsed-laser deposition, galvanic growth, electrophoresis, chemical vapour deposition. Substrate 330 comprises metallic materials, selected from the group consisting of refractory metals, noble metals, aluminium, nickel, chromium, or alternatively semiconductor or insulator materials, selected from the group consisting of silicon, germanium, gallium arsenide, gallium nitride, aluminium nitride, boron nitride, III-V in general and their ternary or quaternary compounds, diamond. Photoresist thickness has to be larger than the height of the DMSs to be obtained. The photoresist film 335 is then patterned 220 by optical lithography resulting in a photoresist pattern 339 corresponding to the pattern of the exposed areas 336 of photoresist film 335 (or to the pattern of unexposed areas in case of deposition of a negative photoresist film). Therefore, a substrate/coating film/photoresist pattern system 3100 is obtained and it is schematically shown in the cross-section of Figure 3(b). In order to transfer selected geometries on the photoresist, opaque material master films (e.g. chromium) developed on transparent

(e.g. quartz) freestanding photomasks, not shown in the Figures, were specifically designed and fabricated. The geometry is then transferred by using a lithographic contact, proximity or projection procedure, performed by illuminating the mask with optical radiation (e.g. UV), or direct writing such as in the case of laser writing or electron beam lithography or scanning probe lithography. The optical lithographic procedure involves the use of a mask aligner in soft-contact, proximity or projection mode. The sample coated with the photoresist film 335 (on which the photomask is positioned) is exposed to optical radiation. The exposure duration time has to ensure the complete photoreaction of the exposed areas 336 of photoresist film 335. Photoresist is finally dipped in a dedicated chemical solution (developer), which removes unexposed areas of photoresist in case of a positive photoresist (or exposed areas in case of a negative photoresist). In other embodiments of the method according to this invention, the photoresist film 335 is directly patterned by different pattering techniques selected from the group consisting of direct imprinting, direct laser writing, electron beam lithography, scanning probe lithography for higher resolution in the nanometre range.

[0025] Optionally, after the photoresist deposition 210, the substrate/coating film/photoresist film system 3000 is soft baked at temperatures ranging from 30 to 200 °C, preferably at 100 °C, for a time ranging from 1 to 3600 s, preferably 60s, in order to facilitate the evaporation of residual solvents present in the photoresist film 335. Such solvents may indeed contaminate the transparent photomask, or cause adhesions between the mask and the substrate surface on which the photoresist was deposited.

The next step of the first preferred embodiment of method is a dielectric deposition 230 of a layer of dielectric material on the photoresist pattern 339 by sputtering technique. In other embodiments of the method according to this invention, the dielectric deposition is performed by different additive deposition techniques such as thermal evaporation, electron-beam evaporation, pulsed-laser deposition, galvanic growth, electrophoresis, chemical vapour deposition. The dielectric film is selected among highly electrical resistive and poorly thermal conductive, thermally resistant materials at high temperatures, such as (but not limited to) aluminium oxide (alumina, Al_2O_3), zirconium oxide (zirconia, ZrO_2), silicon oxide (SiO_2), boron nitride. In the first preferred embodiments of the invention, the RF plasma produced by a magnetron sputtering deposits dielectric materials by a reactive deposition procedure using metal targets and oxygen. Alternatively, the dielectric deposition 230 of a layer of dielectric material can also be carried out by a direct procedure, therefore using dielectric oxide targets and inert gases (e.g. Argon), but, in this case, there is a drastic reduction in the deposition rate. The yield of dielectric deposition 230 is a dielectric layer 349 that is conformal to the underneath substrate/coating film/photoresist pattern. The dielectric layer 349 comprises a first dielectric pattern corresponding to the exposed areas 336 of photoresist (or unexposed areas in case of a negative photoresist), i.e. the photoresist pattern 339, and a second dielectric pattern 347 corresponding to the unexposed areas of photoresist (or exposed areas in case of a negative photoresist). In other words, the second dielectric pattern 347 is on the areas of the substrate 350 that are not occupied by (i.e. that are free of) the photoresist. Therefore, the second dielectric pattern 347 has been directly deposited on the coated first surface 334 of the substrate 330. A substrate/coating film/photoresist pattern/dielectric layer system 3200 is then obtained and it is schematically shown in the cross-section of Figure 3(c). The next step of the method is a removal step 240 of the photoresist pattern 339 and consequently of the first dielectric pattern deposited on it. In this way, the array of DMSs is obtained according to the geometry defined during the photoresist patterning 220. The photoresist is removed by rinsing the substrate/photoresist pattern/dielectric layer system 3200 in removers specific for the used photoresist. In other embodiments of the invention, common solvents such as acetone or dimethylsulfoxide can be used. Dielectric material deposited on the patterned resist (i.e. the first dielectric pattern) is washed away, whereas the dielectric material deposited on the substrate (i.e. the second dielectric pattern 347) remains unaltered, forming the array of DMSs. In other words, each single structure of the unaltered second dielectric pattern 347 correspond to a single DMS forming the array of DMS. A substrate/coating film/DMS array system 3300 is obtained and it is schematically shown in the cross-section of Figure 3(d). A second surface 364 of a body 360 is then positioned 250 upon the array of DMSs, establishing a fixed distance from the substrate first surface 334 that is equal to the thickness of the array of DMSs. The final substrate/coating film/DMS array/body system 3400 is obtained and it is schematically shown in the cross-section of Figure 3(e). The second surface 364 has a roughness that is lower than the height of the DMSs.

[0026] The height of the DMS structures can range from few nanometres to 50 μm, optionally from few nanometres to 1 μm for thermo-tunnel diodes and from 0.5 μm to 50 μm for the thermionic energy converters. Typical lateral size of a single DMS structure ranges from few nanometres to 100 μm. An array or any geometrical arrangement of DMS structures can be as large as the substrate size. The shape of the single DMS structure is not limited to a single type, but the preferred embodiment is a cone or pyramid with the base in contact with the substrate, or truncated cone or prism or cylinder optionally hollowed to reduce contact area with the hot component, thus to reduce the thermal conduction mechanism, more preferably with features smaller than 10 nm in order to significantly reduce the thermal conductivity as described in "Ultralow thermal conductivity and mechanical resilience of architected nanolattices" by Rob Jagt, University of Groningen, May 2017.

[0027] With reference to Figure 4 and 5, a second pre-

ferred embodiment of the method according to the present invention is described. This second preferred embodiment is similar to the first one, but comprises an additional deposition step 421 of a sacrificial layer on the photoresist pattern 539 of the substrate/coating film/photoresist pattern system 5100 (shown in Figure 5(b)) and then an additional lift-off step 422 of the photoresist pattern 539. The additional steps 421 and 422 are performed after the photoresist patterning 420 and before the dielectric deposition 430 of the dielectric layer. The sacrificial layer 559 comprises materials such as metals, semiconductors, insulators or other polymers and it is conformal to the underneath photoresist pattern 539. The sacrificial layer comprises a first sacrificial pattern 556 corresponding to the exposed areas 536 of photoresist (or unexposed areas in case of a negative photoresist), i.e. the photoresist pattern 539, and a second sacrificial pattern 557 corresponding to the unexposed areas of photoresist in case of a positive photoresist (or exposed areas in case of a negative photoresist). Therefore, a substrate/coating film/photoresist pattern/sacrificial layer system 5101 is obtained and it is schematically shown in the cross-section of Figure 5(b1). After that, the lift-off step 422 is applied to the photoresist pattern 539, resulting in the removal of the first sacrificial pattern 556. Therefore, a substrate/coating film/second sacrificial pattern system 5102 is obtained and it is schematically shown in the cross-section of Figure 5(b2). These additional steps 421 and 422 are performed to allow a larger versatility in the DMS fabrication: the sacrificial layer can be more resistant to the DMS deposition temperature or inert to the deposition atmosphere. A requirement is that the sacrificial layer material can be etched selectively with respect to the DMS material. In the first preferred embodiment, photoresist patterning 420 is made by using a mask reporting an inverted pattern with respect to the mask used for photoresist patterning 220. Alternatively, photoresist patterning 420 can be made by using the same mask used for photoresist patterning 220, but making sure to use an inverted photoresist. The additional deposition technique is selected form the group consisting of spin coating, dip coating, roller coating, curtain coating, extrusion coating, meniscus coating, spray casting, silk screen printing, sputtering, thermal evaporation, electron-beam evaporation, pulsed-laser deposition, galvanic growth, electrophoresis, chemical vapour deposition. The subsequent steps of this second preferred embodiment are those already described above, i.e. dielectric material is deposited 430 on the second sacrificial pattern 557 obtaining a substrate/second sacrificial pattern/dielectric layer system 5200 (Figure 5(c)). Then the second sacrificial pattern 557 is removed by rinsing the substrate/second sacrificial pattern/dielectric layer system 5200 in removers, obtaining a substrate/coating film/DMS array system 5300 (Figure 5(d)). Finally, a second surface 564 of a body 560 is positioned 450 upon the array of DMSs, obtaining a final substrate/coating film/DMS array/body system 5400 schematically shown in the cross-section of Figure 5(e). The second surface 564 has a roughness that is lower than the height of the DMSs.

[0028] In a preferred embodiment of the method, the dielectric deposition 230, 430 of a dielectric material layer 349, 549 is carried out by a sputtering apparatus 100 sketched in Figure 6, as described hereafter.

[0029] The sputtering apparatus 100 comprises a chamber 1 equipped with a pumping system (not shown in Figure 6) that guarantees a vacuum level lower than 10^{-1} mbar, preferably lower than 10^{-6} mbar, a magnetron source system 3, a first gas inlet 2 for a reactive gas flow close to a target 4, and a second gas inlet 5 for an oxygen flow close to a sample holder 10 housing a substrate 11 (i.e. the substrate/photoresist pattern system 310) on which the dielectric material has to be deposited. Two gas flow meters (not shown) are mounted on the gas inlets, allowing for a control of the reactive gas and oxygen flows. The sputtering apparatus 100 comprises a bias voltage control system (not shown), and a shutter 12 positioned over the target 4. The sputtering apparatus further comprises a thermocouple 6, for example but not limited to a type K, aimed at monitoring the process temperature *T* of the substrate 11 and, optionally, a high precision quartz microbalance 9 for measuring the deposition rate *R* and providing at the same time information on the oxidation process (when oxygen reacts with aluminium, the deposition rate reaches a steady state condition). A control unit 7 allows for a real-time monitoring and adjusting of the deposition parameters of the dielectric layer 50 on the substrate 11.

[0030] The use of sputtering technique guarantees the deposition of dielectric material on surfaces at relatively low temperatures (even <100 °C) making possible to treat substrates that could be subject to damage if subjected to higher temperatures. In another embodiment of the present invention, different deposition techniques can be exploited, such as electron-beam (e-beam) evaporation, working at even lower temperatures, as well as thermal evaporation, pulsed-laser deposition, galvanic growth, electrophoresis, chemical vapour deposition.

[0031] In the preferred embodiment of the present invention, the deposition 230 of the dielectric layer by the sputtering system 100 is carried out according to the following steps:

- The substrate 11 is first subjected to acid cleaning (e.g., with a buffered solution HF: H_2O = 1: 100 to remove the native oxides).
- Deposition chamber is evacuated until reaching the appropriate base pressure (1-2x10^{-6} mbar or less).
- The argon flow necessary to sputter the metal particles from the solid target is set to a value ranging from 1 to 1000 sccm (preferably 30 sccm).
- The power value on the magnetron source is set to a value high enough for an efficient sputtering yield, but not too high to avoid temperatures higher than 100 °C;

- Pre-sputtering is performed to remove possible native oxide layers from the target (maintaining the shutter closed in order to avoid deposition of sputtered atoms on the substrate);
- The flow of O_2 (or other reactive gases, including air) is set to enable a the desired deposition rate, preferably in the range 1 - 10 Å/s. The operating pressure is set by a vacuum gate or valve that can be partially opened with a manual or electronic control.
- The stability of the deposition parameters, as well as of the operating temperature and pressure, is monitored for a few minutes to ensure a stable and deposition rate. The parameters that mostly influence the stoichiometric characteristics of the DMSs are the oxygen flow and the power supplied to the source. The experimental conditions are therefore varied by mainly acting on these two parameters.
- If necessary, the deposition parameters are adjusted to keep the deposition rate stable during the process; the rate can be controlled by reading the measured value from the quartz microbalance.
- Deposition on the substrate starts by opening the optional shutter.
- Optional shutter is closed when the deposited film has reached the desired thickness.

[0032] Inventors implemented the first preferred embodiment of this invention in several experiments. A detailed description of the resist deposition step 210, 410, the dielectric layer deposition step 230, 430, and the photoresist removal step 240, 440 of such experiments are reported hereafter.

Example of photoresist patterning

[0033] AZ 4533 (Microchemicals GmbH) is a positive near-UV photoresist for thin (up to 3 μm) surface coatings. After spin-coating, the sample is soft baked at 100 °C for 60 minutes, then the customized quartz photomask is positioned on the spin-coated samples. Then the sample+mask system is exposed to an UV radiation (i-line, 365 nm wavelength) using a 350 W mercury UV lamp (Osram HBO 350 W/S9). Time of exposure is 90 s. Finally, the sample is developed by using the developer AZ 826 MIF (Microchemicals GmbH) undiluted for 60 s. AZ 4533 has a maximum development rate of about 2 μm/min after exposition to a i-line intensity of 8.5 mW/cm^2, typical of 350 W lamps.

Example of Alumina layer deposition

[0034] The deposition of alumina layer by a RF sputtering is carried out by means of an aluminium target and using oxygen as reactive gas. The process is strictly dependent on the base pressure, the partial pressures of the gases, the concentrations of aluminium and oxygen, as well as the ratio between them. The substrate is positioned inside the chamber, where it is expected that a pressure of $5x10^{-6}$ mbar or less has been reached. The argon flow is set to a fixed value of 30 sccm and, keeping the shutter closed, a cleaning procedure of the target is carried out by pre-sputtering at 250 W power. After 15 minutes, the shutter is opened and the oxygen flow is set to values in the range 2.0-3.6 sccm. Note that the increase of oxygen flow causes a drastic reduction in the deposition rate (below 0.4 Å/s). Then, the magnetron source is powered at 180 - 230 W, high enough to guarantee a good sputtering yield of the aluminum target at a temperature lower than 100 °C. The process begins at an operating pressure in the range of $2.2 - 2.4x10^{-3}$ mbar, the temperature is kept between 80 and 90 °C and the deposition rate is kept in the range 0.8-1 Å/s.

Example of Zirconia layer deposition

[0035] The deposition of a good quality stoichiometric zirconia layer is the same as the one described for alumina layer with the following differences:

- use of a zirconium target;
- higher Ar flow (40 sccm);
- wider range of operating pressures ($2.0 - 3.0x10^{-3}$ mbar);
- wider range of deposition temperatures (65 - 100 °C);
- lower deposition rate (0.4 - 0.9 Å/s).

Example of photoresist removal

[0036] The lift-off process is carried out by dipping the sample in undiluted AZ100 Remover at 60 °C for 5 minutes. Figure 7 shows SEM images of an array of 5 μm diameter cup-shaped DMSs fabricated by the first preferred embodiment of the invention. This geometrical structure offers the advantage of further reducing the contact area between the two surfaces to be separated.

[0037] The preferred embodiments of this invention have been described, but it should be understood that those skilled in the art can make other variations and changes, without so departing from the scope of protection thereof, as defined by the attached claims.

Claims

1. Method for fabricating dielectric micro-spacers, DMSs, comprising the following steps:

   A. performing a photoresist deposition (210; 410) of a thin photoresist film (335; 535) on a surface (334; 534) of a substrate (330; 530), the substrate (330; 530) being a metal, or a semiconductor or an insulator;

   B. patterning (220; 420) the photoresist film (335; 535) for obtaining a photoresist patter (339; 539);

   C. performing a dielectric deposition (230; 430)

of a dielectric layer (349; 549) by additive deposition techniques, the dielectric layer (349; 549) comprising a first dielectric pattern (346; 546) conformal to the photoresist pattern (349; 549) and a second dielectric pattern (347; 547) corresponding to areas of the first surface (334; 534) that are not occupied by the photoresist pattern (339; 539), the dielectric layer (349; 549) being highly electrical resistive and poorly thermal conductive, having an electrical resistivity ranging from 10^2 Ω cm to 10^{18} Ω cm and a thermal conductivity ranging from 10^{-3} W/(cm K) to 10 W/(cm K).

D. removing (240; 440) the photoresist pattern (339; 539), whereby the first dielectric pattern (346; 546) deposited on the photoresist pattern (339; 539) is removed and the second dielectric pattern (347; 547) remaining unaltered and forming an array of DMSs.

2. Method according to claim 1, wherein the substrate (330; 530) comprises metallic material selected from the group consisting of refractory metals, noble metals, aluminium, nickel, chromium, or alternatively semiconductor or insulator materials selected from the group consisting of silicon, germanium, gallium arsenide, gallium nitride, aluminium nitride, boron nitride, III-V in general and their ternary or quaternary compounds, diamond.

3. Method according to claim 1 or 2, wherein the photoresist film (335; 535) has a thickness larger than a thickness of the dielectric layer (349; 549).

4. Method according to any one of the preceding claims, comprising before step A the following step:

A0. preliminary deposition (205; 405) of a coating film (333; 533) on the first surface (334; 534) configured to induce specific optical and electronic properties to the substrate (330; 530), wherein optionally the preliminary deposition is performed by a technique selected from the group consisting of spin coating, dip coating, roller coating, curtain coating, extrusion coating, meniscus coating, spray casting, silk screen printing, sputtering, thermal evaporation, electron-beam evaporation, pulsed-laser deposition, galvanic growth, electrophoresis, chemical vapour deposition.

5. Method according to any one of the preceding claims, wherein step A is performed by a technique selected from the group consisting of spin coating, dip coating, roller coating, curtain coating, extrusion coating, meniscus coating, spray casting, silk screen printing, sputtering, thermal evaporation, electron-beam evaporation, pulsed-laser deposition, galvanic growth, electrophoresis, chemical vapour deposition.

6. Method according to any one of the preceding claims, wherein step C is performed by means of a RF plasma produced by a magnetron sputtering depositing dielectric materials by a reactive deposition procedure using metal targets and oxygen or dielectric oxide targets and inert gases.

7. Method according to any one of the preceding claims, wherein the thickness of the dielectric layer (349; 549) ranges from few nanometres to 50 μm and a lateral size of a structure of the second dielectric pattern (347; 547) ranges from few nanometres to 100 μm.

8. Method according to any one of the preceding claims, wherein a shape of the single structure of the second dielectric pattern (347; 547) is selected form the group consisting of cone, truncated cone, pyramid, prism, cylinder, hollowed cylinder, with a base in contact with the substrate (330;530).

9. Method according to any one of the preceding claims, comprising after step A the following step:

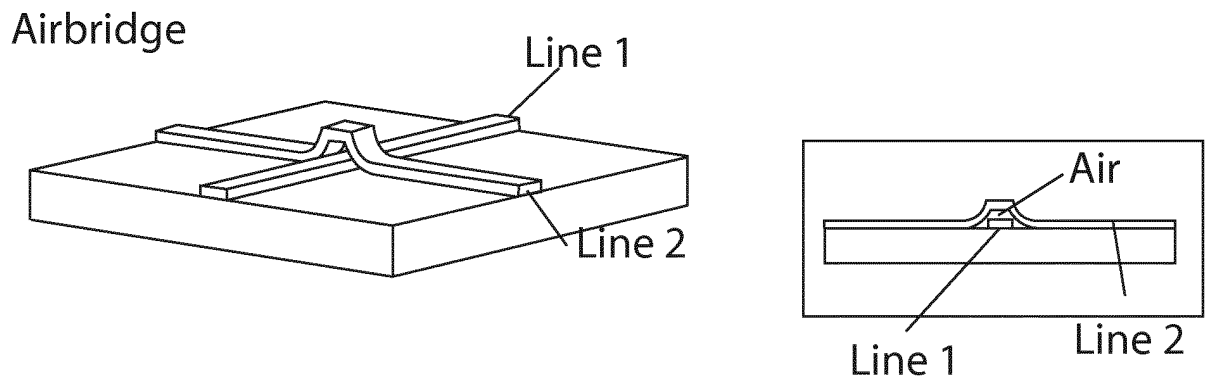
E. positioning (250; 450) upon the array of DMSs a second surface 364 of a body 360, establishing a fixed distance from the first surface (334; 534).

10. Device manufactured by the method of claim 9, configured to be used as thermo-tunnel diodes.

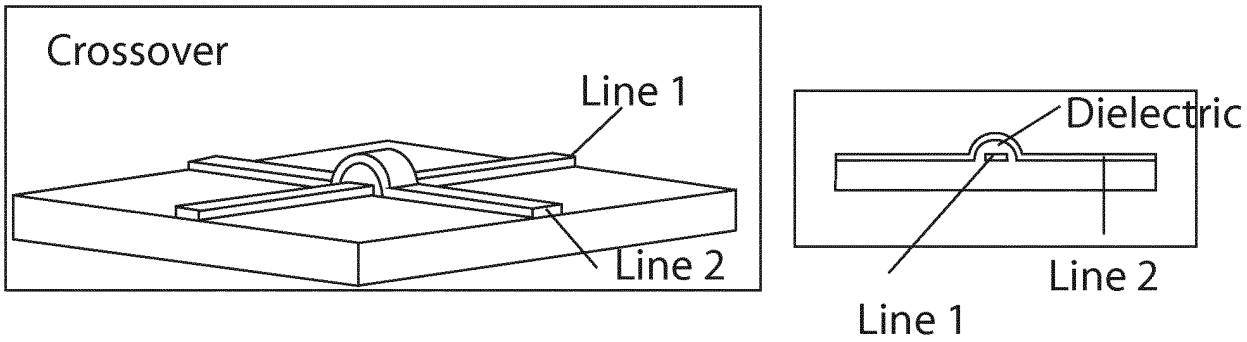
11. Device according to claim 10, wherein each DMS has a height ranging from few nanometres to 1 μm.

12. Device manufactured by the method of claim 9, configured to be used as thermionic energy converters.

13. Device according to claim 12, wherein each DMS has a height ranging from 0.5 μm to 50 μm.



(a)



(b)

STATE OF THE ART

Fig. 1

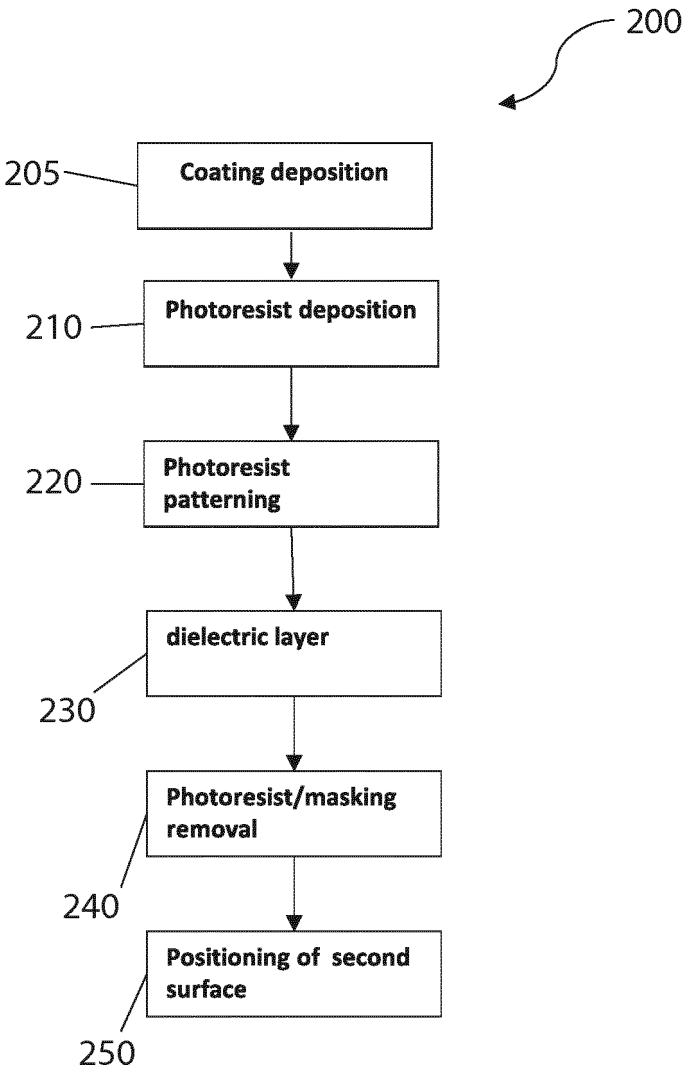

200
205
Coating deposition
210
Photoresist deposition
220
Photoresist patterning
dielectric layer
230
Photoresist/masking removal
240
Positioning of second surface
250

Fig. 2

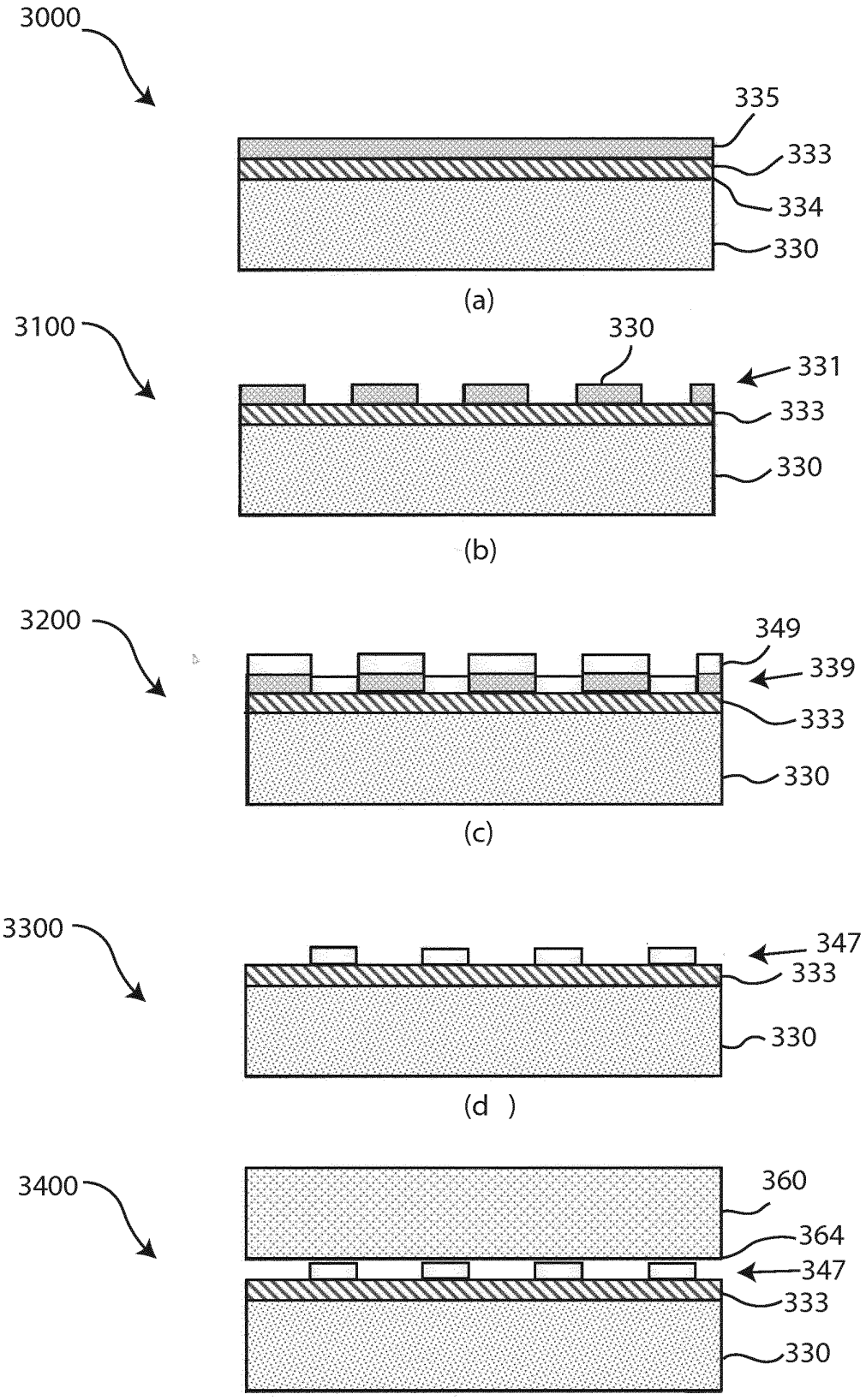

3000
335
333
334
330
(a)
3100
330
331
333
330
(b)
3200
349
339
333
330
(c)
3300
347
333
330
(d)
3400
360
364
347
333
330

Fig. 3

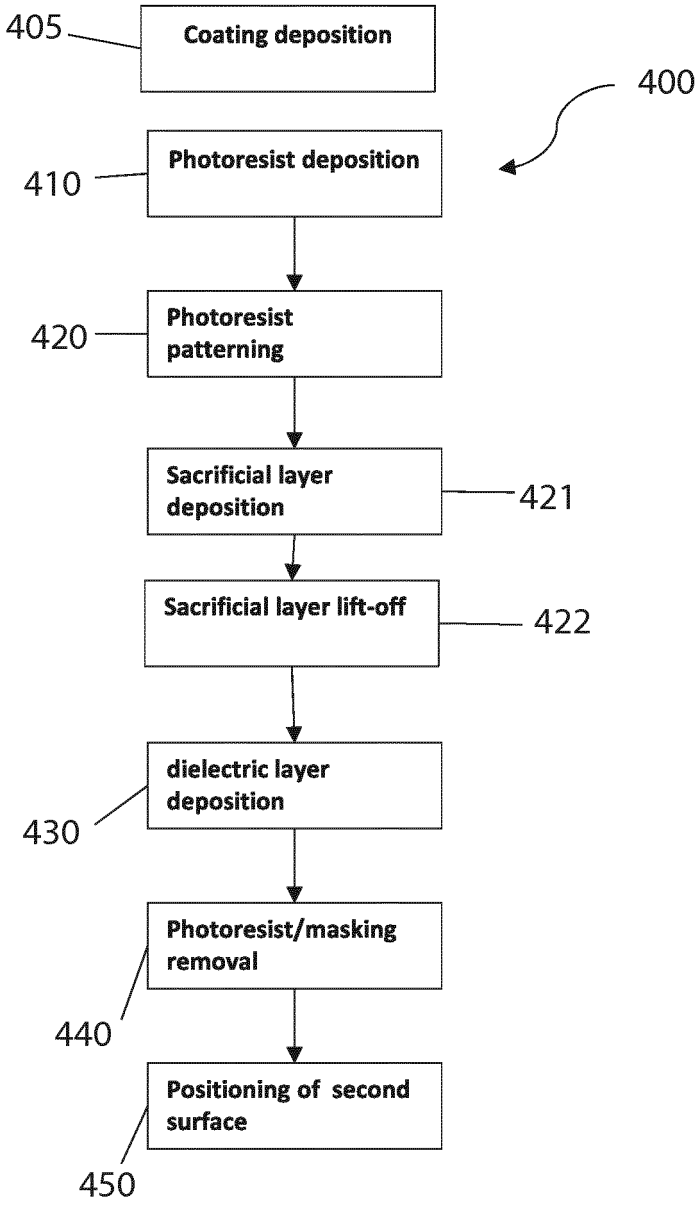

405
Coating deposition
400
410
Photoresist deposition
420
Photoresist patterning
Sacrificial layer deposition
421
Sacrificial layer lift-off
422
dielectric layer deposition
430
Photoresist/masking removal
440
Positioning of second surface
450

Fig. 4

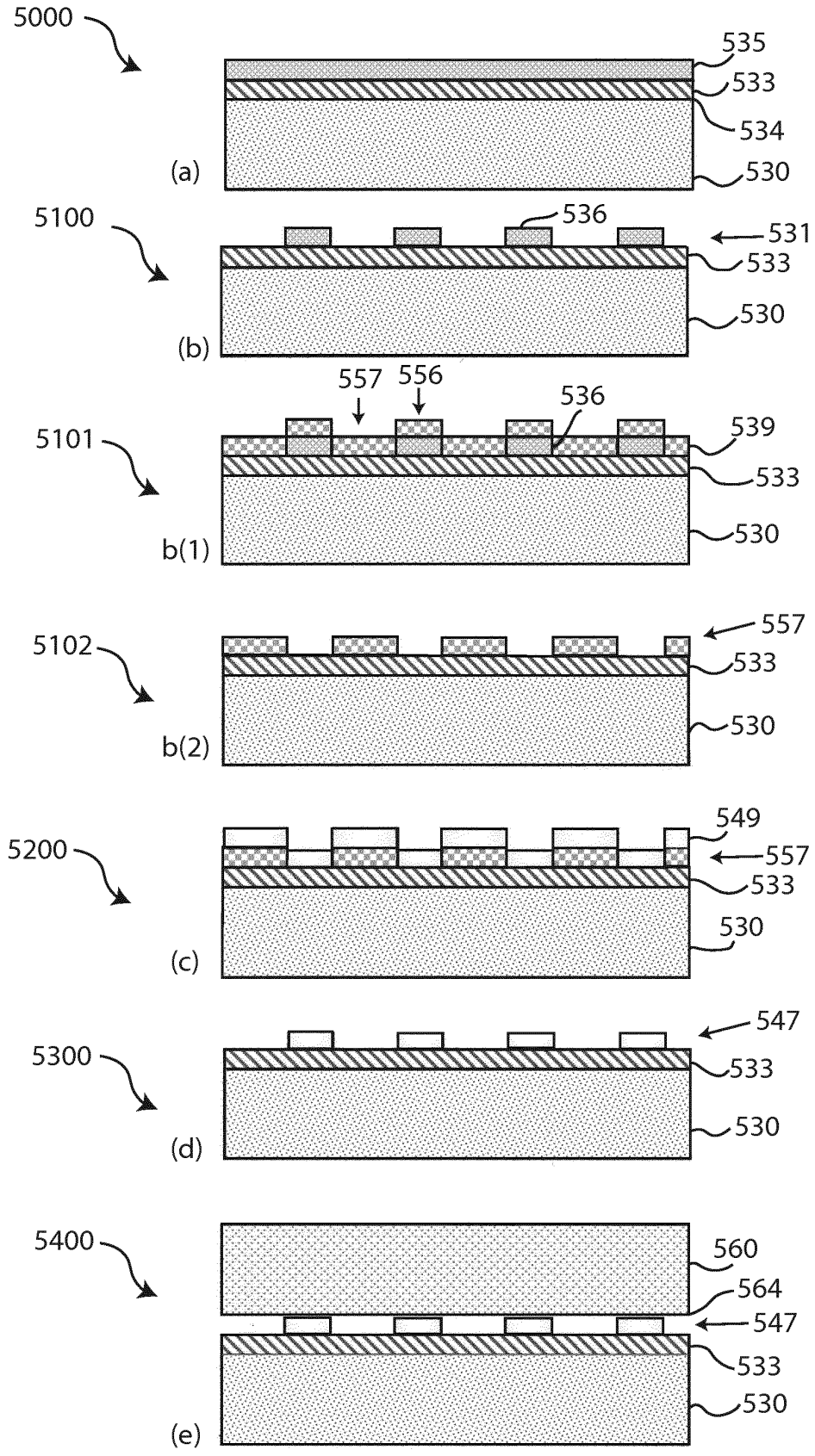

5000
535
533
534
530
(a)
5100
536
531
533
530
(b)
557
556
536
5101
539
533
530
b(1)
5102
557
533
530
b(2)
5200
549
557
533
530
(c)
5300
547
533
530
(d)
5400
560
564
547
533
530
(e)

Fig. 5

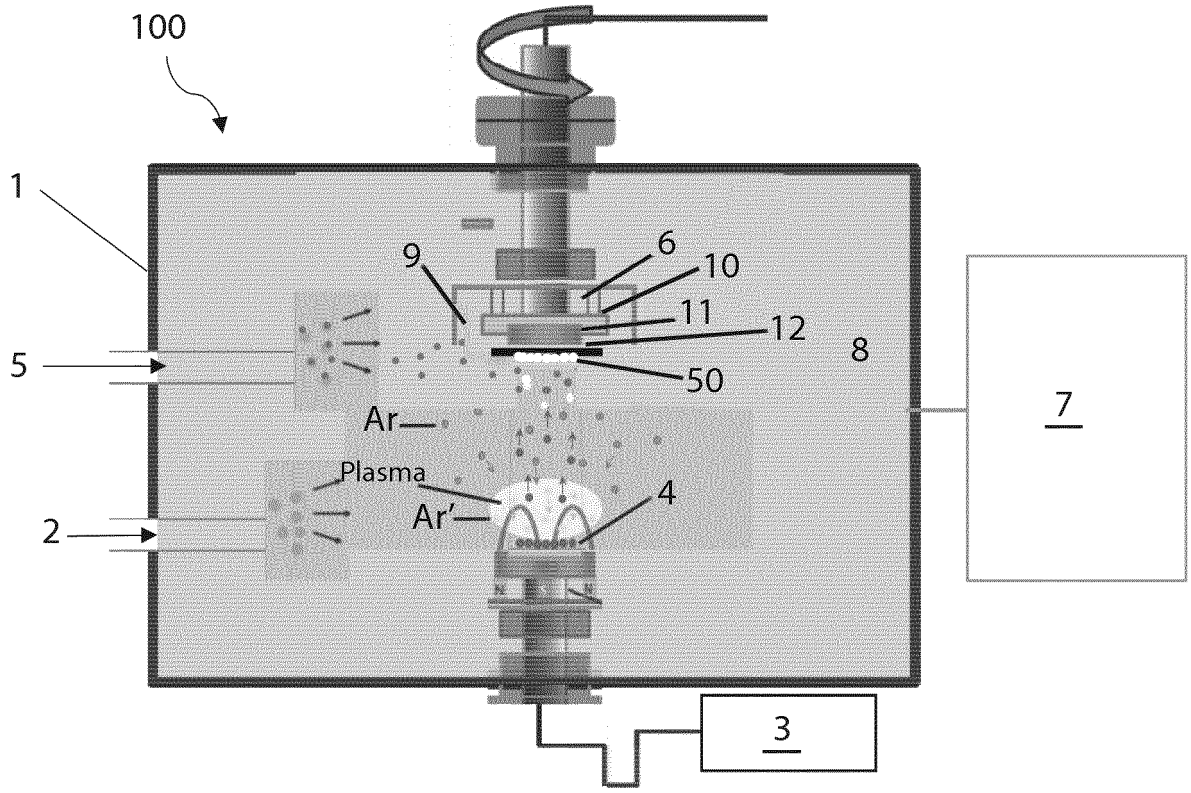
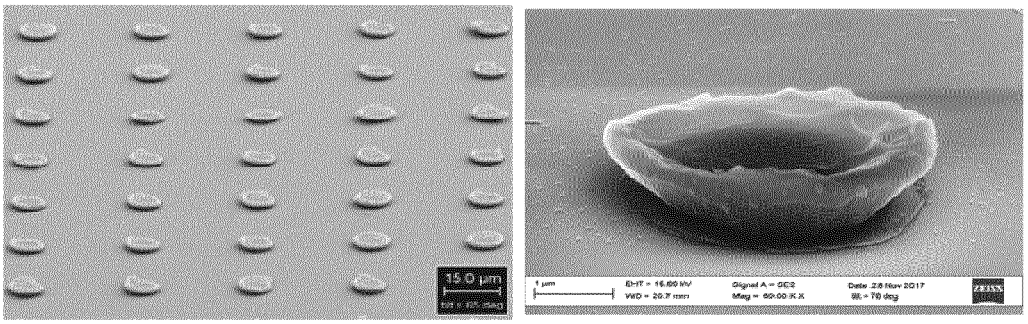


Fig. 6



(a) (b)

Fig. 7

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EUROPEAN SEARCH REPORT

Application Number
EP 18 20 9581

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	EP 3 206 060 A1 (VIAVI SOLUTIONS INC [US]) 16 August 2017 (2017-08-16) * paragraphs [0004], [0017], [0026], [0038], [0041], [0043]; figures 1a,4 *	1-7,9	INV. H01J45/00
X	US 2018/202903 A1 (CHOU STEPHEN Y [US] ET AL) 19 July 2018 (2018-07-19) * paragraphs [0380] - [0381]; figures 1,4 * * paragraphs [0292], [0294] *	1,2,4,5, 7-9	
X	WO 2007/044517 A1 (BOREALIS TECH LTD [US]; WALITZKI HANS JUERGEN [US] ET AL.) 19 April 2007 (2007-04-19) * page 12, lines 3-10; figures 3,8 * * page 13, lines 6-12 *	10-13	
			TECHNICAL FIELDS SEARCHED (IPC) H01J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	15 May 2019	Pérennès, Frédéric

CATEGORY OF CITED DOCUMENTS

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15-05-2019

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REFERENCES CITED IN THE DESCRIPTION

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- **COOPER et al.** Effects of Radiation Damage on Polyimide Resistivity. *Journal of Spacecraft and Rockets,* 2017, vol. 54 (2), 343-348 **[0005]**
- **ROB JAGT.** Ultralow thermal conductivity and mechanical resilience of architected nanolattices. University of Groningen, May 2017 **[0026]**