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(54) **CHIP AND INK CARTRIDGE**

(57) The present invention provides a chip and an ink cartridge. The chip is used for being installed on the ink cartridge, and the ink cartridge is used for being installed in an installation portion of a printer along an installation direction. The chip includes a memory, first contact portions used for installation detection, and second contact portions. At least one second contact portion is electrically connected to the memory. The first contact portions and the second contact portions are respectively in contact with a stylus in the printer. The first contact portions are arranged in a plurality of lines in the installation direction. In the installation direction, one or more lines formed by the second contact portions are disposed between the plurality of lines formed by the first contact portions, or the plurality of lines formed by the first contact portions are disposed between a plurality of lines formed by the second contact portions. Such a structure in which the first contact portions and the second contact portions are arranged in different lines helps reduce burr waves generated due to non-contact electromagnetic interference caused by a voltage difference between the first contact portions and the second contact portions, and free the terminals of an erroneous data signal, thereby ensuring that the chip works normally.

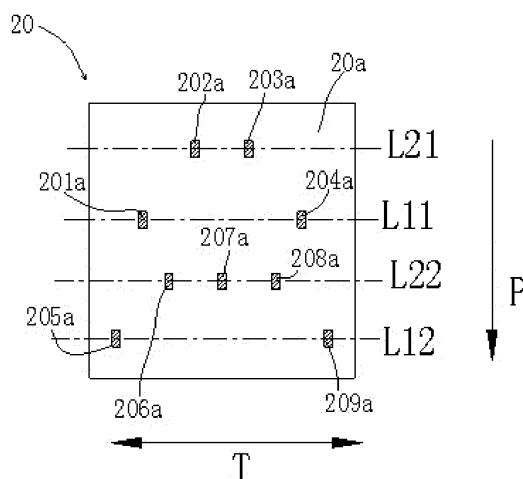


FIG. 4

Description

TECHNICAL FIELD

[0001] The present invention relates to the field of ink-jet printer technologies, and in particular, to a chip and an ink cartridge.

RELATED ART

[0002] With continuous improvement of science and technologies, the printer industry develops rapidly, and ink-jet printers are more widely applied. As a consumable component of the ink-jet printer, an ink cartridge is provided with a chip for storing manufacturer information, ink volume information, ink cartridge type information, ink color information, and the like. The chip for the ink cartridge plays a decisive role in normal operation of the ink-jet printer.

[0003] FIG. 1 is a schematic diagram before an ink cartridge 10 is installed in an installation portion 90. FIG. 2 is a schematic diagram of a chip 20 in the prior art. As shown in FIG. 1 and FIG. 2, the installation portion 90 is a component of a printer, used for receiving one or more ink cartridges 10. The ink cartridge 10 is detachably installed in the installation portion 90 along an installation direction P. The ink cartridge 10 includes the chip 20, a handle 30, an ink outlet 40, and a cartridge body 50. The installation portion 90 has a stylus portion 91 and an ink supply portion 92. Ink is stored in the cartridge body 50, and flows through the ink outlet 40 to the ink supply portion 92, so that the ink supply portion 92 may supply the ink to a print head, and the ink can be used for performing printing actions. The chip 20 has a terminal group 200. The terminal group 200 may be in contact with and electrically connected to a stylus 91a of the stylus portion 91 for mutual transmission of electrical signals. The handle 30 is used for fastening the ink cartridge 10 to the installation portion 90, to prevent the ink cartridge 10 from getting out of the installation portion 90.

[0004] The chip 20 in the prior art has a substrate 20a, the terminal group 200 disposed on the substrate 20a, and a memory (not shown in the figure). The terminal group 200 includes nine terminals 201 to 209. The nine terminals are classified into first terminals 201, 204, 205, and 209, and second terminals 202, 203, and 206 to 208. The first terminals are terminals used for installation detection when the ink cartridge 10 is installed in the installation portion 90. The second terminals are terminals other than the first terminals. At least some of the second terminals are used for connecting to the memory of the chip 20. The nine terminals 201 to 209 respectively include contact portions 201a to 209a in contact with the stylus 91a. The nine contact portions 201a to 209a are arranged in two lines (a first line L1 and a second line L2) in the installation direction P, and in a width direction T perpendicular to the installation direction P, the nine contact portions 201a to 209a are arranged staggered.

Contact portions 201a and 204a of the terminals 201 and 204 in the first terminals and second contact portions 202a and 203a of the terminals 202 and 203 in the second terminals are disposed in the first line L1, and the contact portions 201a and 204a are located at two ends in the width direction T of the first line L1 respectively. Contact portions 205a and 209a of the terminals 205 and 209 in the first terminals and second contact portions 206a to 208a of the terminals 206 to 208 in the second terminals are disposed in the second line L2, and the contact portions 205a and 209a are located at two ends in the width direction T of the second line L2 respectively.

[0005] In the prior art, for better installation detection, generally, input voltages of the first terminals 201, 204, 205, and 209 are different from those of the second terminals 202, 203, and 206 to 208. Electrical signals on all the terminals need to be within a certain range, so that the chip 20 may normally perform installation detection and signal transmission. A voltage difference exists between the first terminals and the second terminals (for example, a high voltage of 42 V is input to the first terminals for installation detection and a low voltage of 3.3 V is input to the second terminals connected to the memory). However, as shown in FIG. 2, the first terminals used for installation detection are disposed excessively close to the second terminals. Consequently, signal interference is caused between an installation detection signal on the first terminals and a signal on the second terminals, and an interfered-with terminal may mistake the interference for a data signal (for example, the high voltage of 42 V at the first terminals may generate a burr wave on a neighboring terminal and thus the terminal may mistake the burr wave for a data signal). Due to the signal interference between the first terminals and the second terminals, the terminals may be subject to an erroneous data signal, and the terminal group 200 of the chip 20 cannot work normally.

SUMMARY

[0006] The present invention provides a chip and an ink cartridge, to resolve a technical problem of mutual signal interference between terminals in the prior art.

[0007] A first aspect of embodiments of the present invention provides a chip. The chip is used for being installed on an ink cartridge, and the ink cartridge is used for being installed in an installation portion of a printer along an installation direction. The chip includes a memory, first contact portions used for installation detection, and second contact portions. At least one second contact portion is electrically connected to the memory. The first contact portions and the second contact portions are respectively in contact with a stylus in the printer.

[0008] The first contact portions are arranged in a plurality of lines in the installation direction.

[0009] In the installation direction, one or more lines formed by the second contact portions are disposed between the plurality of lines formed by the first contact

portions, or the plurality of lines formed by the first contact portions are disposed between a plurality of lines formed by the second contact portions.

[0010] Optionally, the first contact portions include a first group of installation detection contact portions connected to each other and a second group of installation detection contact portions connected to each other. The first group of installation detection contact portions and the second group of installation detection contact portions are arranged in a plurality of lines in the installation direction.

[0011] Optionally, the first group of installation detection contact portions forms a first line in the installation direction. The second group of installation detection contact portions forms a second line in the installation direction. The one or more lines formed by the second contact portions are disposed between the first line and the second line.

[0012] Optionally, the first group of installation detection contact portions are connected by a wire, and the second group of installation detection contact portions are connected by a resistor. A voltage applied to the second group of installation detection contact portions is greater than a voltage of the first group of installation detection contact portions.

[0013] Optionally, the second contact portions include a ground contact portion not connected to the memory, and further include a power supply contact portion, a data contact portion and a reset contact portion that are connected to the memory.

[0014] Optionally, the chip includes a plurality of first terminals and a plurality of second terminals. The plurality of first contact portions are disposed on the plurality of first terminals, and the plurality of second contact portions are disposed on the plurality of second terminals.

[0015] Optionally, the chip includes the plurality of first terminals and the plurality of second terminals. In the installation direction, one or more lines formed by the second terminals are disposed between a plurality of lines formed by the first terminals.

[0016] Optionally, the plurality of lines formed by the first contact portions are spaced from the one or more lines of the second contact portions.

[0017] Optionally, in the installation direction, the plurality of lines of the first contact portions are each spaced from the plurality of lines of the second contact portions.

[0018] Optionally, in the installation direction, the first contact portions form the first line and the second line. The second contact portions form a third line and a fourth line. The first line and the second line are each spaced from the third line and the fourth line.

[0019] Optionally, the second line is closer to a front end side of the installation direction than the third line and the fourth line.

[0020] Optionally, the fourth line is closer to a front end side of the installation direction than the first line and the second line.

[0021] Optionally, the chip includes a first part and a

second part. The first part and the second part are made of two circuit substrates.

[0022] Optionally, the first part and the second part are made of the substrates of different materials. The second part is made of conductive silicon or a conductive metal material.

[0023] Optionally, the second contact portions are disposed on the first part, and the first contact portions are disposed on the second part.

[0024] Optionally, the chip further includes a through portion. The through portion penetrates the chip in a thickness direction of the chip.

[0025] Optionally, the chip further includes a substrate. The first contact portions are more protruded relative to the substrate than the second contact portions.

[0026] Optionally, the first part is provided with terminal-holes for terminals provided with contact portions on the second part to penetrate and the terminals are protruded relative to the first part.

[0027] Optionally, in the installation direction, the first contact portions form the first line and the second line. The second contact portions form the third line and the fourth line. The first line and the second line are disposed between the third line and the fourth line.

[0028] Optionally, in a perpendicular direction of the installation direction, the second group of installation detection contact portions are located on an outermost side of all contact portions, and the first group of installation detection contact portions are located on a second outermost side of all the contact portions.

[0029] Optionally, the first contact portions are located closer to a front end of the installation direction than the second contact portions, and the front end is a downstream side of the installation direction.

[0030] Optionally, a distance between each two first contact portions, a distance between each two second contact portions, and a distance between each first contact portion and each second contact portion are greater than or equal to a preset distance threshold.

[0031] A second aspect of the embodiments of the present invention provides an ink cartridge, including the chip according to any of the above. The technical solutions achieve beneficial effects as follows: In the installation direction, the one or more lines formed by the second contact portions are disposed between the plurality of lines formed by the first contact portions, and the plurality of lines formed by the first contact portions are disposed between the plurality of lines formed by the second contact portions. That is, the first contact portions and the second contact portions are arranged in different lines. This structure helps reduce burr waves generated due to non-contact electromagnetic interference caused by a voltage difference between the first contact portions and the second contact portions, and free the terminals of an erroneous data signal, thereby ensuring that the chip works normally.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] To describe the technical solutions in the embodiments of the present invention more clearly, the following briefly describes the accompanying drawings required for describing the embodiments. Apparently, the accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

FIG. 1 is a schematic diagram before an ink cartridge is installed in an installation portion;

FIG. 2 is a schematic diagram of a chip in the prior art;

FIG. 3 is a schematic diagram of a chip according to Embodiment 1;

FIG. 4 is a schematic diagram of contact portions of a chip according to Embodiment 2;

FIG. 5 is a schematic diagram of a first chip according to Embodiment 2;

FIG. 6 is a schematic diagram of a first chip according to Embodiment 2;

FIG. 7a and FIG. 7b are structural diagrams of a chip according to a first implementation of Embodiment 2;

FIG. 8 is a structural diagram of a chip according to a second implementation of Embodiment 2;

FIG. 9 is a schematic diagram of contact portions of a chip according to Embodiment 3;

FIG. 10 is a structural diagram of a chip according to a first implementation of Embodiment 3;

FIG. 11 is a structural diagram of a chip according to a second implementation of Embodiment 3;

FIG. 12 is a structural diagram of a chip according to a third implementation of Embodiment 3;

FIG. 13a and FIG. 13b are structural diagrams of a chip according to a fourth implementation of Embodiment 3;

FIG. 14a and FIG. 14b are structural diagrams of a chip according to a fifth implementation of Embodiment 3;

FIG. 15 is a schematic diagram of a chip according to Embodiment 4;

FIG. 16 is a structural diagram of a chip according to a first implementation of Embodiment 4; and

FIG. 17 is a structural diagram of a chip according to a second implementation of Embodiment 4.

DETAILED DESCRIPTION

[0033] To make the technical solutions in the present invention more comprehensible, the following describes the embodiments of the present invention in detail with reference to the accompanying drawings.

[0034] It should be clear that the described embodiments are merely some but not all of the embodiments of the present invention. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

Embodiment 1

[0035] FIG. 1 is a schematic diagram before an ink cartridge 10 is installed in an installation portion 90. As shown in FIG. 1, the installation portion 90 is a component of a printer, used for receiving one or more ink cartridges 10. The ink cartridge 10 is detachably installed in the installation portion 90 along an installation direction P. A chip 20 is installed on the ink cartridge 10. The ink cartridge 10 includes the chip 20, a handle 30, an ink outlet 40, and a cartridge body 50. The installation portion 90 has a stylus portion 91 and an ink supply portion 92. Ink is stored in the cartridge body 50, and flows through the ink outlet 40 to the ink supply portion 92, so that the ink supply portion 92 may supply the ink to a print head, and the ink can be used for performing printing actions. The chip 20 has a terminal group 200. The terminal group 200 may be electrically connected to a stylus 91a of the stylus portion 91 for mutual transmission of electrical signals. The handle 30 is used for fastening the ink cartridge 10 to the installation portion 90, to prevent the ink cartridge 10 from getting out of the installation portion 90.

[0036] FIG. 3 is a schematic diagram of a chip according to Embodiment 1. As shown in FIG. 1 and FIG. 3, the chip 20 has a substrate 20a, the terminal group 200 disposed on the substrate 20a, and a memory (not shown in the figure). Optionally, the chip may include the terminal group 200, including nine terminals 201 to 209. The nine terminals are classified into first terminals 201, 204, 205, and 209, and second terminals 202, 203, and 206 to 208. The first terminals are terminals used for installation detection when the ink cartridge 10 is installed in the installation portion 90. The second terminals are terminals other than the first terminals. At least some of the second terminals are used for connecting to the memory of the chip 20. The nine terminals 201 to 209 respectively include contact portions 201a to 209a in contact with the stylus 91a. First contact portions 201a, 204a, 205a, and

209a are disposed on the first terminals 201, 204, 205, and 209. Second contact portions (reference numerals of the contact portions are not shown in the figure) are disposed on the second terminals 202, 203, and 206 to 208. The first contact portions are arranged in a plurality of lines in the installation direction P. That is, the first contact portions 201a, 204a, 205a, and 209a form a line L11 and a line L12. The second contact portions on the second terminals 202, 203, and 206 to 208 are arranged in a line in the installation direction P, and form a line L21. The second contact portions on the second terminals 202, 203, and 206 to 208 may alternatively be arranged in a plurality of lines. FIG. 3 is merely used to describe an example that the second contact portions are arranged in the line L21. The line L21, the line L11, and the line L12 are spaced in the installation direction P. That is, the line L21, the line L11, and the line L12 are arranged in different lines in the installation direction P, and the line L21 is located between the line L11 and the line L12. In the installation direction P, as shown in FIG. 3, the line L21 of the second contact portions may be located between the line L11 and the line L12 that are formed by the first contact portions. Alternatively, as shown in FIG. 15, the line L11 and the line L12 of the first contact portions may be located between a line L21 and a line L22 that are formed by the second contact portions. For both of the arrangement structures in FIG. 3 and FIG. 15, in the installation direction, the one or more lines formed by the second contact portions are disposed between the plurality of lines formed by the first contact portions. Alternatively, the plurality of lines formed by the first contact portions are disposed between the plurality of lines formed by the second contact portions. This structure helps reduce burr waves generated due to non-contact electromagnetic interference caused by a voltage difference between the first contact portions and the second contact portions, and free the terminals of an erroneous data signal, thereby ensuring that the chip works normally.

[0037] Optionally, the first contact portions 201a, 204a, 205a, and 209a may include a first group 200a of installation detection contact portions (201a and 204a) connected to each other and a second group 200b of installation detection contact portions (205a and 209a) connected to each other. The first group 200a of installation detection contact portions (201a and 204a) and the second group 200b of installation detection contact portions (205a and 209a) are arranged in a plurality of lines in the installation direction P. Specifically, as shown in FIG. 3, the first group 200a of installation detection contact portions (201a and 204a) forms a first line L11 in the installation direction. The second group 200b of installation detection contact portions (205a and 209a) forms a second line L12 in the installation direction P. The one line (L21) or the plurality of lines formed by the second contact portions (contact portions shown on the second terminals 202, 203, and 206 to 208) is disposed between the first line L11 and the second line L12. In the foregoing struc-

ture, the first group of installation detection contact portions 201a and 204a forms the line L11, and the second group of installation detection contact portions 205a and 209a forms the line L12. In this way, the first contact portions are divided into groups and arranged in lines, so that the terminal group 200 may have a larger design space, and a layout is better performed on the substrate 20a.

[0038] Optionally, the first group 200a of installation detection contact portions (201a and 204a) are connected by a wire, and the second group 200b of installation detection contact portions (205a and 209a) are connected by a resistor. A voltage applied to the second group 200b of installation detection contact portions (205a and 209a) is greater than a voltage of the first group 200a of installation detection contact portions (201a and 204a).

[0039] Different working voltages are input to contact portions of different groups, and installation detection contact portions of different groups are arranged in different lines. A layout of such spaced arrangement manner further reduces burr waves generated due to non-contact electromagnetic interference caused by a voltage difference between installation detection contact portions of different groups, and frees the terminals of an erroneous data signal, thereby ensuring that the chip works normally. In the example of FIG. 3, the first terminals 201, 204, 205, and 209 are divided into two groups during installation detection. A first installation detection terminal 201 and a second installation detection terminal 204 form a first group of installation detection terminals. The first contact portions 201a and 204a on the first group of installation detection terminals are connected to each other to form the first group 200a of installation detection contact portions. A third installation detection terminal 205 and a fourth installation detection terminal 209 form a second group of installation detection terminals. The first contact portions 205a and 209a on the second group of installation detection terminals are connected to each other to form the second group 200b of installation detection contact portions. The printer inputs a voltage of 2.4 V to the first group of installation detection terminals 201 and 204, and inputs a voltage of 42 V to the second group of installation detection terminals 205 and 209. The printer inputs a voltage of 3.3 V to terminals connected to the memory in the second terminals 202, 203, and 206 to 208, to maintain signal transmission between the chip 20 and the printer. The first contact portions and the second contact portions form the line L11, the line L12, and the line L21. The line L11, the line L12, and the line L21 are spaced in the installation direction P, that is, are in different lines, and are separated and independent. This structure helps reduce burr waves generated due to non-contact electromagnetic interference caused by a voltage difference between the first group 200a of installation detection contact portions, the second group 200b of installation detection contact portions, and the second contact portions with different input voltages, and free the terminals of an erroneous data signal, thereby ensuring

that the chip works normally.

[0040] Optionally, the second contact portions (for example, the contact portions shown on the second terminals 202, 203, and 206 to 208) include a ground contact portion (a contact portion on the terminal 207) not connected to the memory (not shown in the figure), and further include a power supply contact portion (a contact portion on the terminal 206), a data contact portion (a contact portion on the terminal 208), and a reset contact portion (a contact portion on the terminal 202) that are connected to the memory.

[0041] Specifically, purposes and functions of the terminals in the terminal group 200 are as follows:

the terminal 201 belongs to the first group of installation detection terminals;

the terminal 202 is a reset terminal;

the terminal 203 is a clock terminal;

the terminal 204 belongs to the first group of installation detection terminals;

the terminal 205 belongs to the second group of installation detection terminals;

the terminal 206 is a power supply terminal;

the terminal 207 is a ground terminal;

the terminal 208 is a data terminal; and

the terminal 209 belongs to the second group of installation detection terminals.

[0042] In the second terminals 202, 203, and 206 to 208, the terminals 202, 203, 207 and 208 are connected to the memory for exchanging electrical signals with the printer, and work at the voltage of 3.3 V. The terminal 207 is a ground terminal, and has a voltage of 0 V. The terminal 207 is not connected to the memory. A person skill in the art may understand that the terminal group 200 may alternatively not include the terminal 207.

[0043] Optionally, a larger voltage difference between terminals makes it easier for the terminals to affect each other. Signal interference easily occurs, the terminals are easily subject to an erroneous signal, and normal operation cannot be performed. A voltage difference between the second group of installation detection terminals 205 and 209 (with the voltage of 42 V input) and the second terminals (with 3.3 V input) is larger. Therefore, the line L12 may be disposed on a front end side of the installation direction P, namely, an outermost side of the terminal group 200. The first group of installation detection terminals 201 and 204 (with 2.4 V input) having a smaller voltage difference from the second terminals is disposed in the line L11. As viewed from the installation direction P,

an input voltage of the line L11 is 2.4 V, an input voltage of the line L21 is 3.3 V, an input voltage of the line L12 is 42 V, and the voltages are arranged from low to high. That is, the plurality of lines of the first contact portions and/or the second contact portions are sequentially arranged according to the input voltages of the portions, so that a voltage difference between each two lines is as low as possible. This reduces burr waves generated due to non-contact electromagnetic interference caused by a voltage difference, and further helps free the terminals of an erroneous data signal, thereby ensuring that the chip works normally.

[0044] Further, the first contact portions 201a, 204a, 205a, and 209a in FIG. 3 are laid out and form a quadrangle, and the second terminals or the second contact portions on the second terminals are disposed within the quadrangle surrounded by the first contact portions 201a, 204a, 205a, and 209a, thereby ensuring that the second terminals are in good contact with the stylus. Because the first contact portions used for installation detection are on the outermost side of the terminal group 200, in the process of installing the ink cartridge 10, if the chip 20 and the stylus 91a of the printer finish the installation detection, it indicates that all the installation detection terminals (the first terminals) are in good connection, and it can be ensured that all positions within the polygon formed by the first contact portions are in good contact. Further, a quantity of the first contact portions may be any of more than three, and the beneficial effects can be achieved as long as the second contact portions are located within the polygon formed by the first contact portions.

[0045] Optionally, as shown in FIG. 3, the line L12 formed by the first contact portions 205a and 209a of the first terminals 205 and 209 is located closer to a front end of the installation direction P than the line L21 in which the second contact portions are located. The front end is a downstream side of the installation direction P. With this structure, in the process of installing the ink cartridge 10 in the installation portion 90, the terminals of the line L12 can be first in contact with the stylus 91a and perform installation detection, and then the second terminals of the line L21 are in contact with the stylus 91a. Therefore, in the installation process, the stylus 91a is first in contact with the terminals that perform installation detection, and then in contact with the terminals connected to the memory, to avoid a case that the chip 20 is erroneously installed or the terminals connected to the memory are erroneously connected. Further, in a direction T perpendicular to the installation direction P, the second group 200b of installation detection contact portions are located on an outermost side of all the contact portions, and the first group 200a of installation detection contact portions are located on a second outermost side of all the contact portions. As shown in FIG. 3, the first contact portions 205a and 209a of the second group 200b of installation detection contact portions are located on the outermost side in the perpendicular direction T, the first contact por-

tions 201a and 204a of the first group 200a of installation detection contact portions are located on the second outermost side, and the second terminals 202, 203, and 206 to 208 on which the remaining second contact portions are located are on an innermost side. This layout can also implement that the terminals to which a highest voltage is input (the terminals 205 and 209 have a voltage of 42 V input) are located on the outermost side, the terminals to which a second highest voltage is input (the terminals 201 and 204 have a voltage of 2.4 V input) are located on the second outermost side, and the terminals to which a lower voltage is input (the second terminals have a voltage of 3.3 V input) are located on the innermost side, so that the voltage difference between neighboring terminals is as low as possible. This reduces burr waves generated due to non-contact electromagnetic interference caused by the voltage difference, and further helps free the terminals of an erroneous data signal, thereby ensuring that the chip works normally.

Embodiment 2

[0046] FIG. 4 is a schematic diagram of contact portions of a chip according to Embodiment 2. FIG. 5 is a schematic diagram of a first chip according to Embodiment 2. FIG. 6 is a schematic diagram of a first chip according to Embodiment 2. FIG. 4 omits terminals on the chip, which is a schematic diagram showing only the contact portions. FIG. 5 and FIG. 6 are schematic diagrams of two chips respectively. FIG. 7a and FIG. 7b are structural diagrams of a chip according to a first implementation of Embodiment 2. FIG. 8 is a structural diagram of a chip according to a second implementation of Embodiment 2. As shown in FIG. 4 to FIG. 6, first contact portions 201a, 204a, 205a, and 209a of first terminals 201, 204, 205, and 209 form a line L11 and a line L12. Second contact portions 202a, 203a, and 206a to 208a of second terminals 202, 203, and 206 to 208 form a line L21 and a line L22 in an installation direction P. One line or the plurality of lines (the line L21 and the line L22) formed by the second contact portions is disposed between the plurality of lines (the line L11 and the line L12) formed by the first contact portions. Alternatively, the plurality of lines (the line L11 and the line L12) formed by the first contact portions are disposed between the plurality of lines (the line L21 and the line L22) formed by the second contact portions, which can still achieve beneficial effects of the present application.

[0047] Further, the plurality of lines (the line L11 and the line L12) formed by the first contact portions are each spaced from the plurality of lines (the line L21 and the line L22) of the second contact portions. That is, in the installation direction P, the first contact portions form a first line L11 and a second line L12, and the second contact portions form a third line L21 and a fourth line L22. The first line L11 and the second line L12 are each spaced from the third line L21 and the fourth line L22. In this way, the first contact portions and the second contact portions

sequentially form the line L21, the line L11, the line L22, and the line L12. With this structure, the first terminals and the second terminals, namely, the first contact portions and the second contact portions are spaced from each other, so that the terminals have a larger design space, which helps increase the space between the terminals, and reduce electromagnetic mutual interference between the terminals.

[0048] Optionally, as shown in FIG. 4, the second line (the line L12) (the line L12 formed by the first contact portions 205a and 209a) is closer to a front end side of the installation direction P than the third line L21 and the fourth line L22. That is, the line L12 is located on a most front end side of the installation direction P. In a process of installing an ink cartridge 10 in an installation portion 90, the terminals of the line L12 are first in contact with a stylus 91a and perform installation detection, and then the second terminals of the line L22 are in contact with the stylus 91a. Therefore, in the installation process, the terminals may first perform installation detection, and then the terminals connected to a memory are in contact with the stylus 91a, to avoid a case that the chip 20 is erroneously installed or the terminals connected to the memory are erroneously connected.

[0049] FIG. 5 and FIG. 6 show two specific arrangement manners of terminal arrangements, either of which may be used as long as it is ensured that the contact portions are distributed as shown in FIG. 4. Further, arrangement manners of the terminals of the chip 20 are not limited to the arrangement manners of FIG. 5 or FIG. 6. There may be various arrangement manners. Different arrangement manners of the terminals based on FIG. 4 shall all fall within the protection scope of the present application.

[0050] As described in Embodiment 1, the terminal 202 may be a reset terminal, the terminal 203 may be a clock terminal, the terminal 206 may be a power supply terminal, the terminal 207 may be a ground terminal, and the terminal 208 may be a data terminal. The terminals 206 to 208 in the second terminals of a terminal group 200 are more important than the terminal 202 and the terminal 203. Optionally, as shown in FIG. 5, the first contact portions 201a, 204a, 205a, and 209a are laid out and form a virtual quadrangle, and the terminals 206 to 208 in the second terminals are disposed within a range of the quadrangle. More important terminals (the terminals 206 to 208 in this embodiment) in the second terminals are disposed within the quadrangle surrounded by the first terminals (in other words, important communications terminals that are more easily affected by a signal are disposed in an area away from the four first terminals), which may ensure good contact of these terminals. In the process of installing the ink cartridge 10, if the chip 20 and the stylus 91a of the printer finish installation detection, it indicates that all the installation detection terminals (the first terminals) are in good connection, and it can be ensured that all positions within the polygon formed by the first contact portions are in good contact. Therefore, it

can be ensured that the more important terminals (the terminals 206 to 208 in this embodiment) in the second terminals are in good contact. Further, a quantity of the first contact portions may be any of more than three, and the beneficial effects can be achieved as long as the second contact portions are located within the polygon formed by the first contact portions.

[0051] Further, when the ink cartridge 10 is installed in the installation portion 90, the ink cartridge has a certain movement range in the width direction T. The following case may occur: The chip 20 has been installed, but the first terminals (installation detection terminals) are not in contact with the stylus 91a. The chip in this embodiment may avoid this case. The lines formed by the first terminals and the lines formed by the second terminals are different lines, so that the width of each terminal can be increased, and this case is avoided as the width increases.

[0052] Further, the first terminals are far from the second terminals, which may avoid a fact that short circuits are caused between the first terminals and the second terminals because foreign matters (such as ink) dropped accidentally cover the first terminals and the second terminals, and result in damage of the chip or a printer. That is, a distance between each two first contact portions, a distance between each two second contact portions, and a distance between each first contact portion and each second contact portion are greater than or equal to a preset distance threshold. The distance threshold may be preset to a plurality of different values by a person skilled in the art according to values of voltages applied to the terminals, to achieve the technical effects and further reduce mutual interference of signals between the terminals.

[0053] The rest is the same as that in Embodiment 1

[0054] The following is two implementations of this embodiment.

First implementation:

[0055] FIG. 7a and FIG. 7b are structural diagrams of a chip according to the first implementation of Embodiment 2. As shown in FIG. 7a and FIG. 7b, the chip 20 includes a first part 21 and a second part 22. The second terminals 202, 203, and 206 to 208 are disposed on the first part 21. The first terminals 201, 204, 205, and 209 are disposed on the second part 22.

[0056] The first part 21 and the second part 22 are made of two circuit substrates 21a and 22a. Then, the first part 21 and the second part 22 are fastened together by soldering, adhesive, snaps, or the like to finally form the chip 20.

[0057] The chip 20 is made of the two circuit substrates 21a and 22a, so that the terminals on the first part 21 and the terminals on the second part 22 are located at different heights, and are respectively in contact with different positions of the stylus 91a when being in contact with the stylus 91a, to implement the layout shown in FIG. 4 of

the first contact portions and the second contact portions.

[0058] The chip 20 further includes additional terminals 210 and 211 and fastening portions 251, 252, and 253. The additional terminals 210 and 211 are not in contact with the stylus 91a in the installation portion 90. The additional terminals may prevent short circuits between the terminals of the terminal group 200, or scrape the stylus 91a when being in contact with the stylus 91a, to clean the stylus 91a. The fastening portions 251, 252, and 253 may fasten the chip 20 to the ink cartridge 10, to prevent the chip 20 from getting out of the ink cartridge 10.

Second implementation:

[0059] FIG. 8 is a structural diagram of a chip according to the second implementation of Embodiment 2. As shown in FIG. 8, the chip 20 includes only one substrate 20a. The chip 20 further includes additional terminals 210 and 211 and fastening portions 251 and 252, and further includes a through portion 255. The through portion 255 penetrates the chip in a thickness direction of the chip. The additional terminals 210 and 211 and the fastening portions 251 and 252 are the same as those in the first implementation of this embodiment, and are not described again. The through portion 255 is used for accommodating the stylus 91a, so that the first terminals and the second terminals are respectively in contact with different positions of the stylus 91a, to implement the layout shown in FIG. 4 of the first contact portions and the second contact portions. The thickness direction is a direction perpendicular to both the installation direction P and the width direction T. In this implementation, the thickness direction of the chip is also a direction parallel to a shortest side direction of the chip. The thickness direction of the chip is perpendicular to a surface on which the terminals are located.

Embodiment 3

[0060] FIG. 9 is a schematic diagram of contact portions of a chip according to Embodiment 3. FIG. 10 is a structural diagram of a chip according to a first implementation of Embodiment 3. FIG. 11 is a structural diagram of a chip according to a second implementation of Embodiment 3. FIG. 12 is a structural diagram of a chip according to a third implementation of Embodiment 3. FIG. 13a and FIG. 13b are structural diagrams of a chip according to a fourth implementation of Embodiment 3. FIG. 14a and FIG. 14b are structural diagrams of a chip according to a fifth implementation of Embodiment 3. FIG. 9 omits terminals on the chip, which is a schematic diagram showing only the contact portions. FIG. 10 to FIG. 14b are structural diagrams of five chips respectively. As shown in FIG. 9, first contact portions 201a, 204a, 205a, and 209a of first terminals 201, 204, 205, and 209 form a line L11 and a line L12. Second contact portions 202a, 203a, and 206a to 208a of second terminals 202, 203, and 206 to 208 form a line L21 and a line L22 in an

installation direction P. One line or the plurality of lines (the line L21 and the line L22) formed by the second contact portions is disposed between the plurality of lines (the line L11 and the line L12) formed by the first contact portions. Alternatively, the plurality of lines (the line L11 and the line L12) formed by the first contact portions are disposed between the plurality of lines (the line L21 and the line L22) formed by the second contact portions, which can still achieve beneficial effects of the present application.

[0061] Further, the line L11 and the line L12 are each spaced from the line L21 and the line L22. That is, in the installation direction P, the first contact portions form a first line L11 and a second line L12. The second contact portions form a third line L21 and a fourth line L22. The first line L11 and the second line L12 are each spaced from the third line L21 and the fourth line L22. In this way, along the installation direction P, the first contact portions and the second contact portions sequentially form the line L11, the line L21, the line L12, and the line L22. With this structure, the first terminals and the second terminals, namely, the first contact portions and the second contact portions are spaced from each other, so that the terminals have a larger a design space of the terminals.

[0062] Optionally, as shown in FIG. 9, the fourth line L22 is closer to a front end side of the installation direction than the first line L11 and the second line L12. That is, the line L22 is located on a most front end side of the installation direction P.

[0063] Functions of the terminals of a terminal group 200 are not limited to the terminal functions described in Embodiment 3. The terminal 202 and the terminal 203 in the second terminals are more important than the terminals 206 to 208. As shown in FIG. 9, the first contact portions 201a, 204a, 205a, and 209a are laid out and form a virtual quadrangle, and the terminal 202 and the terminal 203 in the second terminals are disposed within a range of the quadrangle. More important terminals (the terminal 202 and the terminal 203 in this embodiment) in the second terminals are disposed within the quadrangle surrounded by the first terminals (in other words, important communications terminals that are more easily affected by a signal are disposed in an area away from the four first terminals), which may ensure good contact. In a process of installing an ink cartridge 10, if the chip 20 and the stylus 91a of the printer finish installation detection, it indicates that all the installation detection terminals (the first terminals) are in good connection, and it can be ensured that all positions within the polygon formed by the first contact portions 201a, 204a, 205a, and 209a are in good contact. Therefore, it can be ensured that the more important terminals (the terminals 202 and the terminal 203 in this embodiment) in the second terminals are in good contact.

[0064] The rest is the same as that in Embodiment 2.

[0065] The following is four implementations of this embodiment.

First implementation:

[0066] FIG. 10 is a structural diagram of a chip according to the first implementation of Embodiment 3. As shown in FIG. 10, the chip 20 includes a first part 21 and a second part 22. The first terminals 201, 204, 205 and 209 are disposed on the first part 21. The second terminals 202, 203, and 206 to 208 are disposed on the second part 22.

[0067] The first part 21 and the second part 22 are made of two different circuit substrates 21a and 22a. Then, the first part 21 and the second part 22 are fastened together by soldering, adhesive, snaps, or the like to finally form the chip 20.

[0068] The chip 20 is made of the two circuit substrates 21a and 22a, so that the terminals on the first part 21 and the terminals on the second part 22 are located at different heights, and are respectively in contact with different positions of the stylus 91a when being in contact with the stylus 91a, to implement the layout shown in FIG. 9 of the first contact portions and the second contact portions.

[0069] The chip 20 further includes fastening portions 251, 252, and 253. The fastening portions 251, 252, and 253 may fasten the chip 20 to the ink cartridge 10, to prevent the chip 20 from getting out of the ink cartridge 10.

[0070] The chip 20 may further include additional terminals (not shown in the figure, and reference may be made to a disposition manner of the additional terminals 210 and 211 in FIG. 8). The additional terminals are not in contact with the stylus 91a in the installation portion 90. The additional terminals may prevent short circuits between the terminals of the terminal group 200, or scrape the stylus 91a when being in contact with the stylus 91a, to clean the stylus 91a.

Second implementation:

[0071] FIG. 11 is a structural diagram of a chip according to the second implementation of Embodiment 3. As shown in FIG. 11, the chip 20 includes only one substrate 20a. The chip 20 may further include additional terminals 210 and 211, fastening portions 251 and 252, and through portions 255. The additional terminals 210 and 211 and the fastening portions 251 and 252 are the same as those in the first implementation of this embodiment, and are not described again. The through portions 255 are used for accommodating the stylus 91a, so that the first terminals and the second terminals are respectively in contact with different positions of the stylus 91a, to implement the layout shown in FIG. 9 of the first contact portions and the second contact portions.

[0072] The through portions 255 penetrating the chip 20 in this implementation are located at two sides in a width direction T of the second terminals 202, 203, and 206 to 208 respectively. With this structure, the first terminals 201, 204, 205, and 209 are separated from the second terminals 202, 203, and 206 to 208 in space by the through portions 255 penetrating the chip 20, which

further avoids a fact that short circuits are caused between the first terminals and the second terminals because foreign matters (such as ink) dropped accidentally cover the first terminals and the second terminals, and result in damage of the chip or a printer. For example, when the ink is dropped between the first terminals and the second terminals, the through portions 255 penetrating the chip 20 enable the ink to flow from the through portions 255 to a lower portion of the chip 20 without remaining on an upper surface (a surface on which the terminals are provided) of the chip 20.

Third implementation:

[0073] FIG. 12 is a structural diagram of a chip according to the third implementation of Embodiment 3. As shown in FIG. 12, the first terminals 201, 204, 205, and 209 are protruded relative to the substrate 20a. The first terminals 201, 204, 205, and 209 may be connected to the substrate 20a by soldering or the like. That is, the first contact portions (not shown in FIG. 12) located on the first terminals 201, 204, 205, and 209 are more protruded relative to the substrate 20a than the second contact portions (not shown in FIG. 12) located on the second terminals 202, 203, and 206 to 208.

[0074] Further, the first terminals 201, 204, 205, and 209 are protruded relative to the substrate 20a. The second terminals 202, 203, and 206 to 208 are disposed on the substrate 20a. The first terminals 201, 204, 205, and 209 and the second terminals 202, 203, and 206 to 208 have a height difference, so that the first terminals and the second terminals are respectively in contact with different positions of the stylus 91a, to implement the layout shown in FIG. 9 of the first contact portions and the second contact portions.

[0075] With this structure in which the first terminals 201, 204, 205, and 209 are protruded relative to the substrate 20a, the first terminals 201, 204, 205, and 209 are separated from the second terminals 202, 203, and 206 to 208 in space, which further avoids a fact that short circuits are caused between the first terminals and the second terminals because foreign matters (such as ink) dropped accidentally cover the first terminals and the second terminals, and result in damage of the chip or a printer.

Fourth implementation:

[0076] FIG. 13a and FIG. 13b are structural diagrams of a chip according to the fourth implementation of Embodiment 3. As shown in FIG. 13a and FIG. 13b, the first terminals 201, 204, 205, and 209 are disposed on the second part 22, and the second terminals 202, 203, and 206 to 208 are disposed on the substrate 21a of the first part 21. The first part 21 is provided with terminal-holes 201b, 204b, 205b, and 209b for terminals (the first terminals 201, 204, 205, and 209) provided with contact portions on the second part 22 to penetrate and the ter-

minals are protruded relative to the first part 21. That is, the first terminals 201, 204, 205, and 209 on the second part 22 penetrate the terminal-holes 201b, 204b, 205b, and 209b and are protruded relative to the first part 21.

The first terminals 201, 204, 205, and 209 and the second terminals 202, 203, and 206 to 208 have a height difference, so that the first terminals and the second terminals are respectively in contact with different positions of the stylus 91a, to implement the layout shown in FIG. 9 of the first contact portions and the second contact portions. The second part 22 may be made of conductive silicon or a conductive metal material, or the substrate 22a of the second part 22 is made of non-conductive substrate materials. The first terminals 201, 204, 205, and 209 are made of conductive materials.

[0077] The rest is the same as that in the third implementation of this embodiment.

Fifth implementation:

[0078] FIG. 14a and FIG. 14b are structural diagrams of a chip according to the fifth implementation of Embodiment 3. As shown in FIG. 14a and FIG. 14b, the chip 20 includes a first part 21 and a second part 22. The second part 22 is used for receiving the chip and may be fastened to a chip rack on an ink cartridge body. A first group of installation detection terminals 201 and 204 in the first terminals are disposed on the second part 22. A first group of installation detection terminals 205 and 209 in the first terminals are disposed on the substrate 21a of the first part 21. The second terminals 202, 203, and 206 to 208 (not shown in the figure) are disposed on the substrate 21a of the first part 21. The first part 21 is provided with terminal-holes 201b and 204b. The first terminals 201 and 204 on the second part 22 penetrate the terminal-holes 201b and 204b and are protruded relative to the substrate 21a of the first part 21. The first terminals 205 and 209 are protruded relative to the substrate 21a of the first part 21. The first terminals 205 and 209 may be formed of pads or bumps that are disposed on the substrate 21a and then plated with copper. The first terminals 201, 204, 205, and 209 and the second terminals 202, 203, and 206 to 208 have a height difference, so that the first terminals and the second terminals are respectively in contact with different positions of the stylus 91a, to implement the layout shown in FIG. 9 of the first contact portions and the second contact portions. The second part 22 further functions as a chip rack (receiving the chip and fastening the chip to the cartridge body of the ink cartridge) while receiving the first terminals 201 and 204. This structure reduces a quantity of components of the ink cartridge, and reduces costs. The second part 22 may be made of conductive silicon or a conductive metal material, or the substrate 22a of the second part 22 is made of non-conductive substrate materials. The first terminals 201, 204, 205, and 209 are made of conductive materials. The second part 22 may be made of conductive silicon. In this way, when the chip 20 is in

contact with the stylus 91a, the second part 22 may be deformed to a certain extent, to avoid wear or scratches of the terminals caused by hard contact between the terminals on the chip 20 and the stylus 91a.

[0079] The rest is the same as that in the third implementation of this embodiment.

Embodiment 4

[0080] FIG. 15 is a schematic diagram of a chip according to Embodiment 4. FIG. 16 is a structural diagram of a chip according to a first implementation of Embodiment 4. FIG. 17 is a structural diagram of a chip according to a second implementation of Embodiment 4. FIG. 16 and FIG. 17 are structural diagrams of two chips respectively. As shown in FIG. 15, first contact portions 201a, 204a, 205a, and 209a (the reference numerals are not shown in the figure) of first terminals 201, 204, 205, and 209 form a first line (a line L11) and a second line (a line L12). Second contact portions 202a, 203a, and 206a to 208a (the reference numerals are not shown in the figure) of second terminals 202, 203, and 206 to 208 form a third line (a line L21) and a fourth line (a line L22) in an installation direction P. One line or the plurality of lines (the line L21 and the line L22) formed by the second contact portions is disposed between the plurality of lines (the line L11 and the line L12) formed by the first contact portions. Alternatively, the plurality of lines (the line L11 and the line L12) formed by the first contact portions are disposed between the plurality of lines (the line L21 and the line L22) formed by the second contact portions, which can still achieve beneficial effects of the present application.

[0081] Further, the first contact portions form the first line (the line L11) and the second line (the line L12). The second contact portions form the third line (the line L21) and the fourth line (the line L22). The first line (the line L11) and the second line (the line L12) are disposed between the third line (the line L21) and the fourth line (the line L22). That is, along the installation direction P, the first contact portions and the second contact portions sequentially form the line L21, the line L11, the line L12, and the line L22. With this structure, the third line (the line L21) and the fourth line (the line L22) formed by the second contact portions are located on a peripheral side of the first line (the line L11) and the second line (the line L12) that are formed by the first contact portions. The second contact portions 202a, 203a, and 206a to 208a are entirely located on the periphery of the first contact portions 201a, 204a, 205a, and 209a. The second contact portions 202a, 203a, and 206a to 208a are located outside an area of a polygon (a quadrangle in this embodiment) formed by the plurality of first contact portions 201a, 204a, 205a, and 209a, which further prevents interference of an electrical signal between the first terminals and the second terminals.

[0082] The rest is the same as that in Embodiment 3.

[0083] The following is two implementations of this em-

bodiment.

First implementation:

[0084] FIG. 16 is a structural diagram of a chip according to the first implementation of Embodiment 5. As shown in FIG. 16, the chip 20 includes a first part 21 and a second part 22. The terminals 202 and 203 and the terminals 205 and 209 are disposed on the first part 21. The terminals 201, 204, and 206 to 208 are disposed on the second part 22.

[0085] The first part 21 and the second part 22 are made of two different circuit substrates 21a and 22b. Then, the first part 21 and the second part 22 are fastened together by soldering, adhesive, snaps, or the like to finally form the chip 20.

[0086] The chip 20 is made of the two circuit substrates 21a and 22b, so that the terminals on the first part 21 and the terminals on the second part 22 are located at different heights, and are respectively in contact with the stylus 91a when being in contact with the stylus 91a, to achieve the layout shown in FIG. 15.

[0087] The chip 20 further includes additional terminals 210 and 211. The additional terminals 210 and 211 are not in contact with the stylus 91a in the installation portion 90. The additional terminals may prevent short circuits between the terminals of a terminal group 200 or scrape the stylus 91a when being in contact with the stylus 91a, to clean the stylus 91a.

Second implementation:

[0088] FIG. 17 is a structural diagram of a chip according to the second implementation of Embodiment 5. As shown in FIG. 17, the terminals 202, 203, 205, and 209 are disposed on the second part 22. The terminals 201, 204, and 206 to 208 are disposed on the substrate 21a of the first part 21. The first part 21 is provided with terminal-holes 202b, 203b, 205b, and 209b, and the terminals 202, 203, 205, and 209 on the second part 22 penetrate the terminal-holes 202b, 203b, 205b, and 209b and are protruded relative to the first part 21. The terminals 202, 203, 205, and 209 and the terminals 201, 204, and 206 to 208 have a height difference, so that the terminals are respectively in contact with different positions of the stylus 91a, to implement the layout shown in FIG. 15 of the first contact portions and the second contact portions. The second part 22 may be made of conductive silicon or a conductive metal material, or the substrate 22a of the second part 22 is made of non-conductive substrate materials. The first terminals 201, 204, 205, and 209 are made of conductive materials.

[0089] The rest is the same as that in the first implementation of this embodiment.

[0090] The present invention further provides an ink cartridge, including any of the chips described in the foregoing embodiments.

[0091] The foregoing descriptions are merely exem-

plary embodiments of the present invention, but are not intended to limit the present invention. Any modification, equivalent replacement, or improvement made within the spirit and principle of the present invention shall fall within the protection scope of the present invention.

[0092] Finally, it should be noted that the foregoing embodiments are merely used for describing the technical solutions of the present invention, but are not intended to limit the present invention. Although the present invention is described in detail with reference to the foregoing embodiments, a person of ordinary skill in the art should understand that, modifications may still be made to the technical solutions in the foregoing embodiments, or equivalent replacements may be made to some technical features, without causing the essence of corresponding technical solutions to depart from the scope of the technical solutions in the embodiments of the present invention.

Claims

1. A chip, wherein the chip is used for being installed on an ink cartridge, and the ink cartridge is used for being installed in an installation portion of a printer along an installation direction; the chip comprises a memory, first contact portions used for installation detection, and second contact portions; at least one second contact portion is electrically connected to the memory; and the first contact portions and the second contact portions are respectively in contact with a stylus in the printer, **characterized in that:**

the first contact portions are arranged in a plurality of lines in the installation direction; and in the installation direction, one or more lines formed by the second contact portions are disposed between the plurality of lines formed by the first contact portions, or the plurality of lines formed by the first contact portions are disposed between a plurality of lines formed by the second contact portions.

2. The chip according to claim 1, wherein the first contact portions comprise a first group of installation detection contact portions connected to each other and a second group of installation detection contact portions connected to each other, wherein the first group of installation detection contact portions and the second group of installation detection contact portions are arranged in a plurality of lines in the installation direction.
3. The chip according to claim 2, wherein the first group of installation detection contact portions forms a first line in the installation direction; the second group of installation detection contact portions forms a second line in the installation direction; and the one or

more lines formed by the second contact portions are disposed between the first line and the second line.

4. The chip according to claim 3, wherein the first group of installation detection contact portions are connected by a wire, and the second group of installation detection contact portions are connected by a resistor, wherein a voltage applied to the second group of installation detection contact portions is greater than a voltage of the first group of installation detection contact portions.
5. The chip according to claim 3, wherein the second contact portions comprise a ground contact portion not connected to the memory, and further comprise a power supply contact portion, a data contact portion and a reset contact portion that are connected to the memory.
6. The chip according to claim 1, wherein the chip comprises a plurality of first terminals and a plurality of second terminals, wherein the plurality of first contact portions are disposed on the plurality of first terminals, and the plurality of second contact portions are disposed on the plurality of second terminals.
7. The chip according to claim 6, wherein the chip comprises the plurality of first terminals and the plurality of second terminals, and in the installation direction, one or more lines formed by the second terminals are disposed between a plurality of lines formed by the first terminals.
8. The chip according to claim 1, wherein the plurality of lines formed by the first contact portions are spaced from the one or more lines of the second contact portions.
9. The chip according to any of claims 1 to 8, wherein in the installation direction, the plurality of lines of the first contact portions are each spaced from the plurality of lines of the second contact portions.
10. The chip according to claim 9, wherein in the installation direction, the first contact portions form the first line and the second line, the second contact portions form a third line and a fourth line, and the first line and the second line are each spaced from the third line and the fourth line.
11. The chip according to claim 10, wherein the second line is closer to a front end side of the installation direction than the third line and the fourth line.
12. The chip according to claim 10, wherein the fourth line is closer to a front end side of the installation direction than the first line and the second

line.

13. The chip according to claim 9, wherein the chip comprises a first part and a second part, and the first part and the second part are made of two circuit substrates. 5
14. The chip according to claim 13, wherein the first part and the second part are made of the substrates of different materials, and the second part is made of conductive silicon or a conductive metal material. 10
15. The chip according to claim 13, wherein the second contact portions are disposed on the first part, and the first contact portions are disposed on the second part. 15
16. The chip according to claim 9, wherein the chip further comprises a through portion, and the through portion penetrates the chip in a thickness direction of the chip. 20
17. The chip according to claim 9, wherein the chip further comprises a substrate, and the first contact portions are more protruded relative to the substrate than the second contact portions. 25
18. The chip according to claim 13, wherein the first part is provided with terminal-holes for terminals provided with contact portions on the second part to penetrate and the terminals are protruded relative to the first part. 30
19. The chip according to claim 9, wherein in the installation direction, the first contact portions form the first line and the second line, the second contact portions form the third line and the fourth line, and the first line and the second line are disposed between the third line and the fourth line. 35
40
20. The chip according to claim 1, wherein in a perpendicular direction of the installation direction, the second group of installation detection contact portions are located on an outermost side of all the contact portions, and the first group of installation detection contact portions are located on a second outermost side of all the contact portions. 45
21. The chip according to claim 1, wherein the first contact portions are located closer to a front end of the installation direction than the second contact portions, and the front end is a downstream side of the installation direction. 50
22. The chip according to claim 1, wherein a distance between each two first contact portions, a distance between each two second contact portions, and a distance between each first contact portion and each 55

second contact portion are greater than or equal to a preset distance threshold.

23. An ink cartridge, comprising the chip according to any of claims 1 to 22.

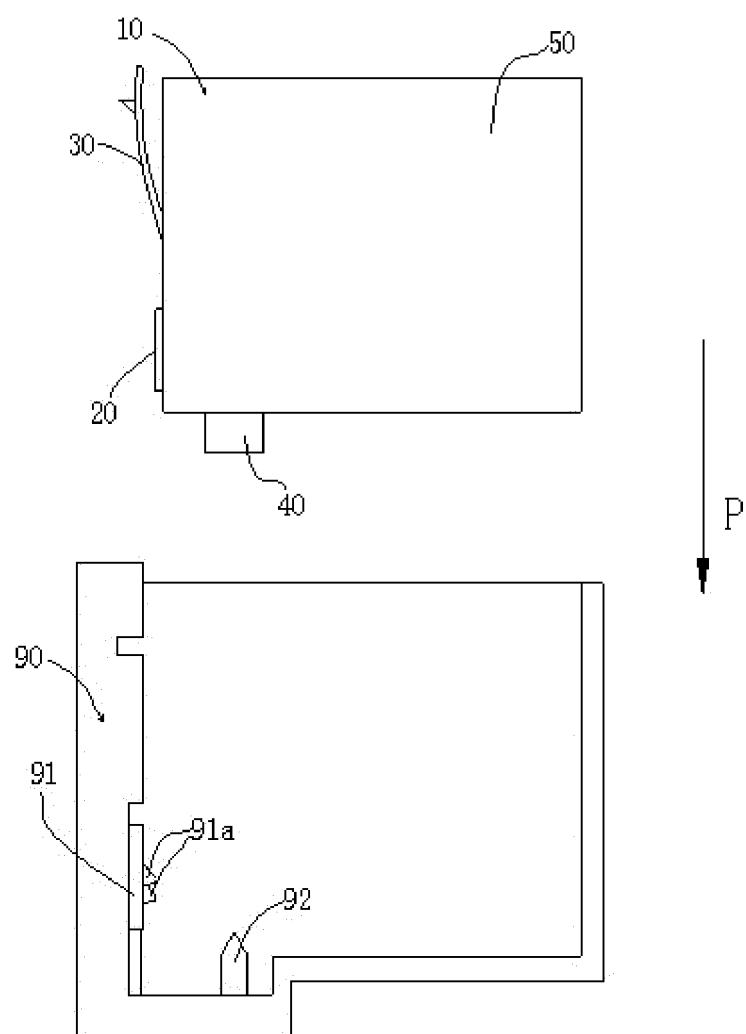


FIG. 1

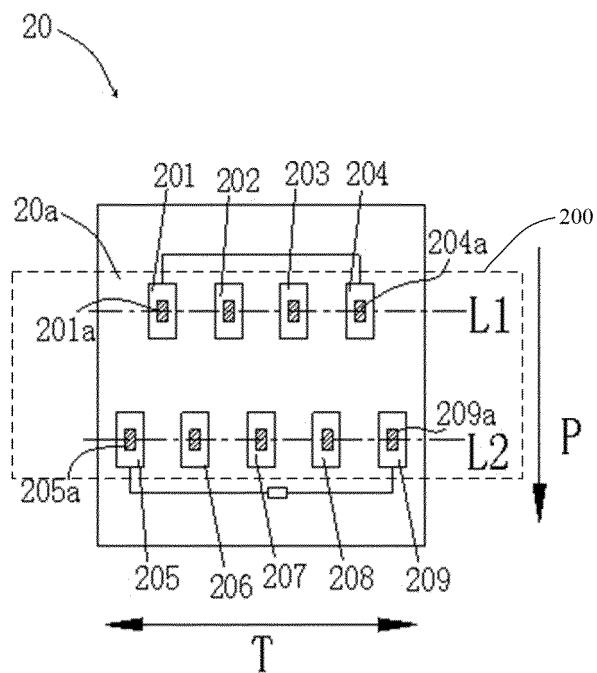


FIG. 2

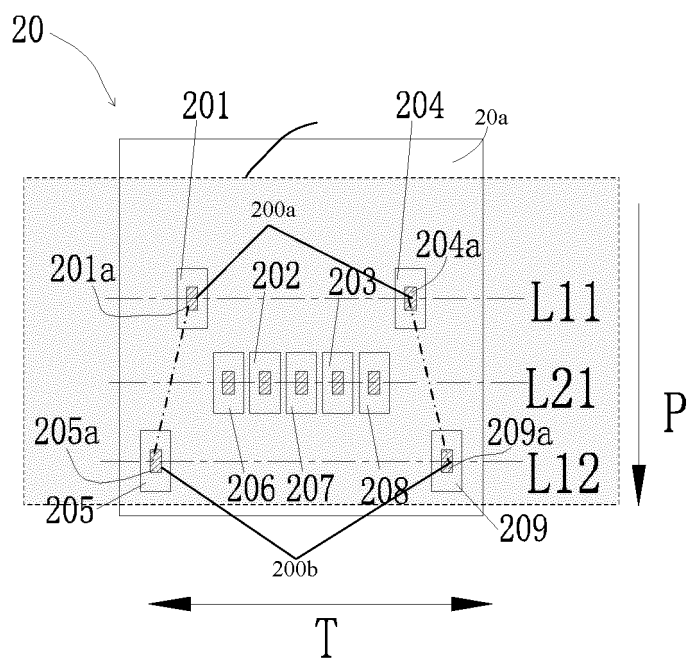


FIG. 3

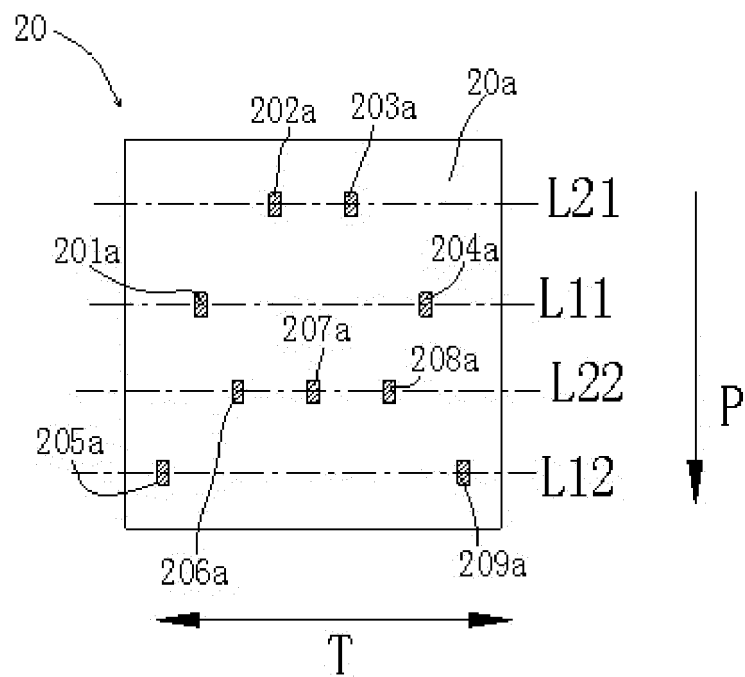


FIG. 4

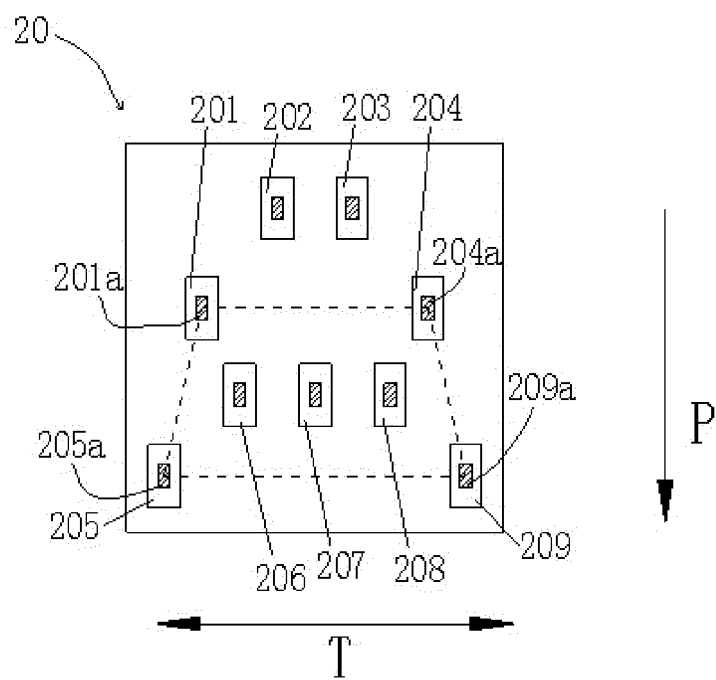


FIG. 5

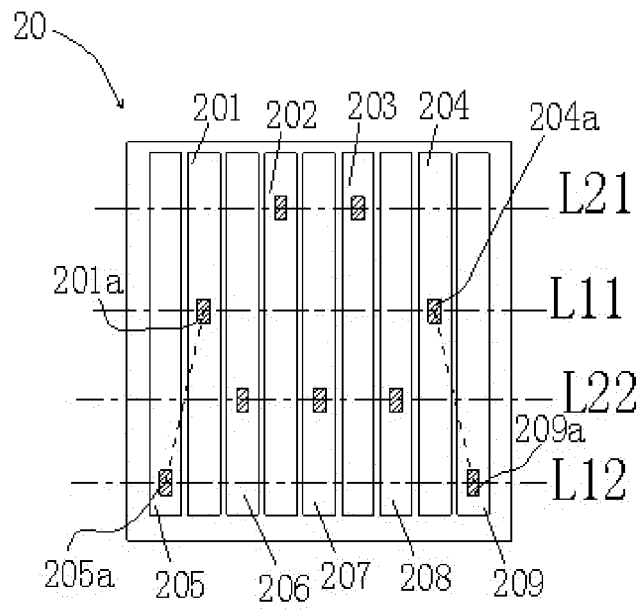


FIG. 6

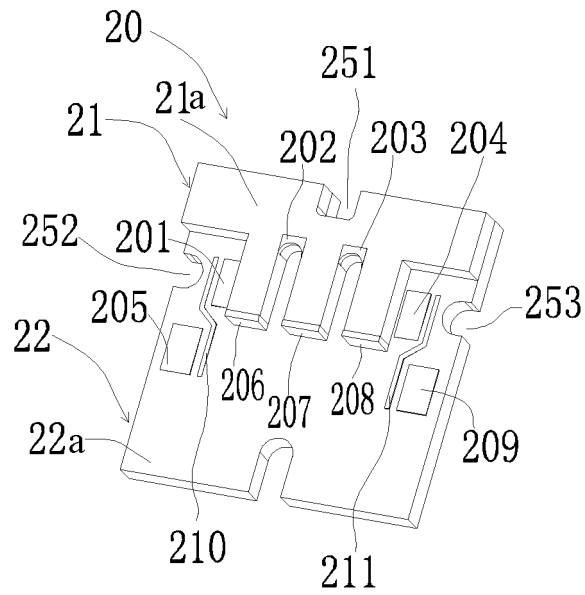


FIG. 7a

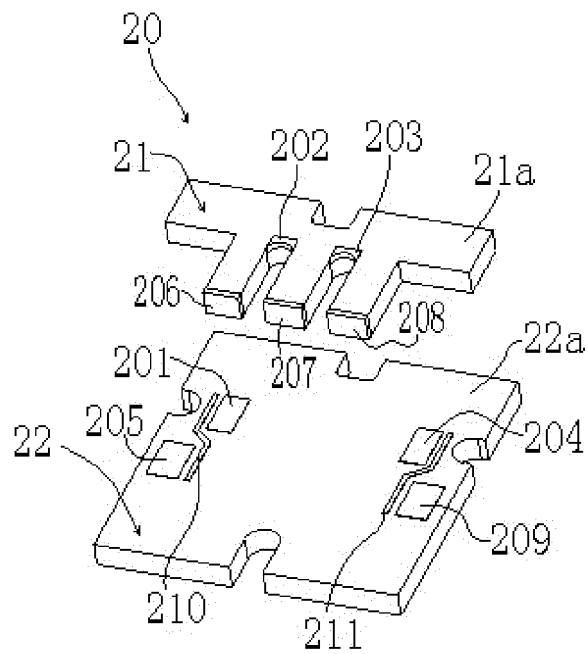


FIG. 7b

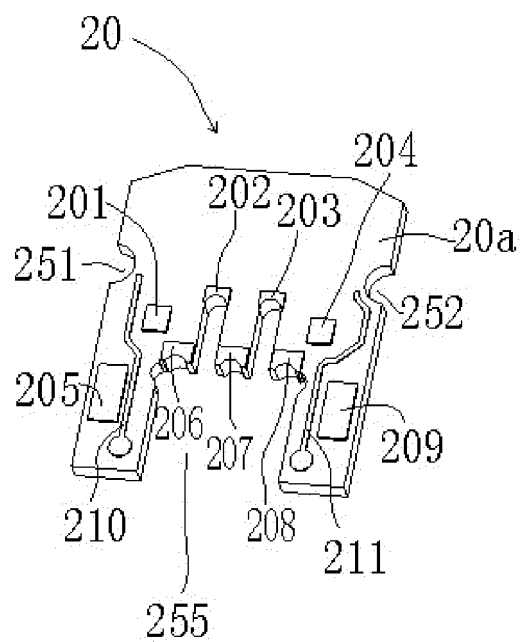


FIG. 8

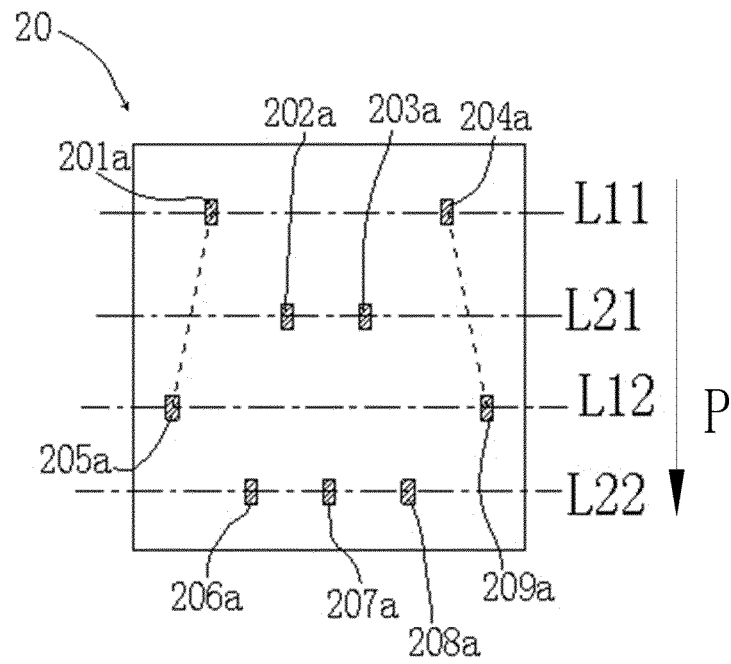


FIG. 9

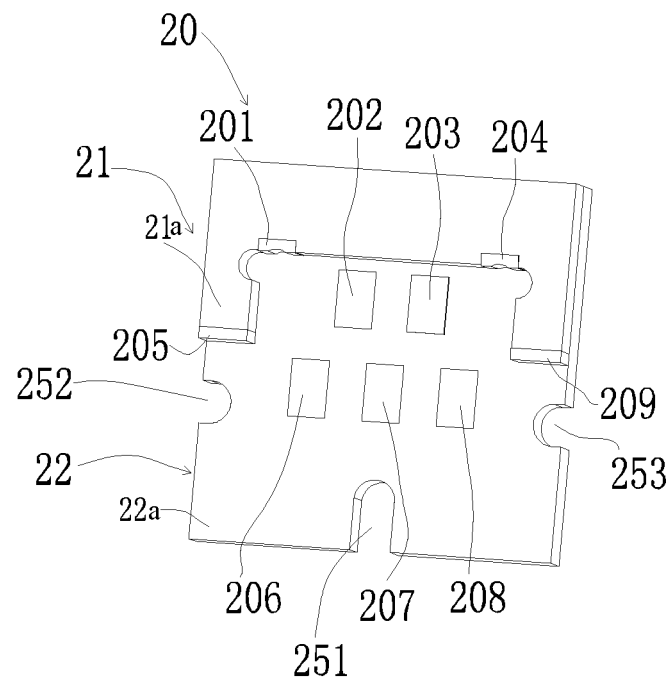


FIG. 10

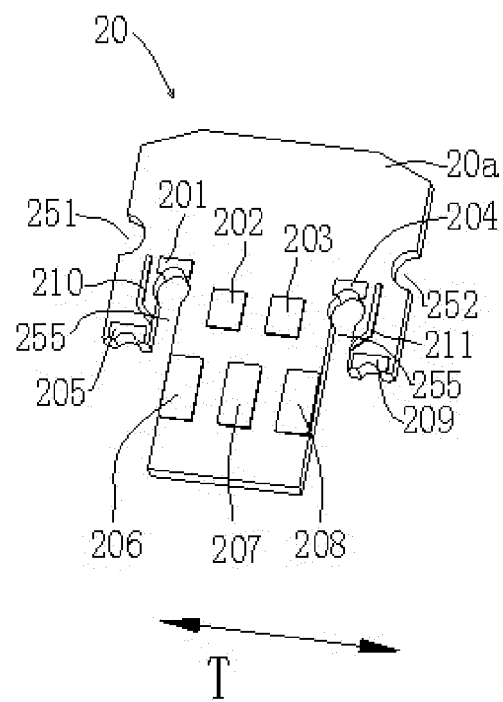


FIG. 11

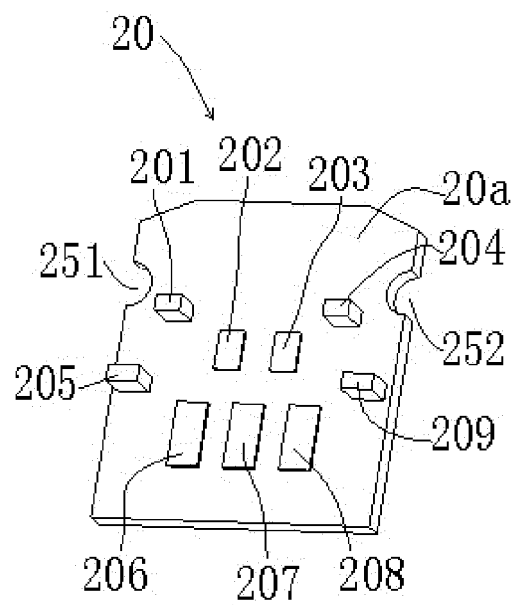


FIG. 12

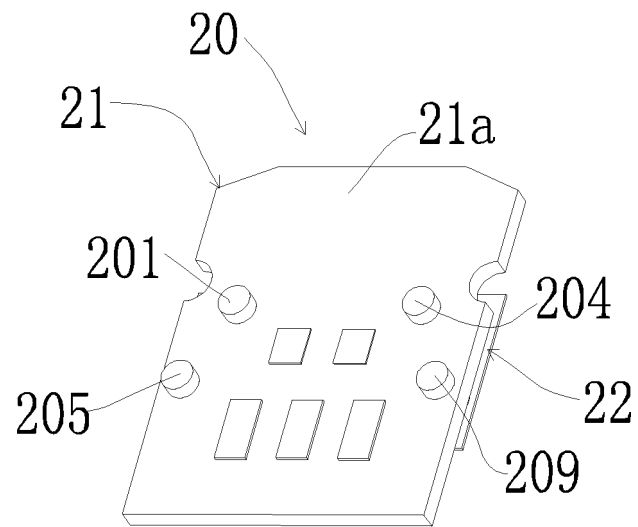


FIG. 13a

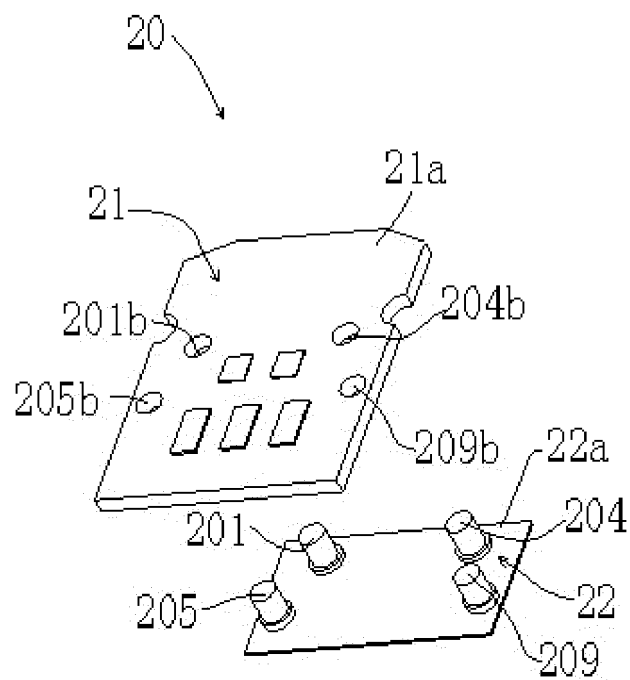


FIG. 13b

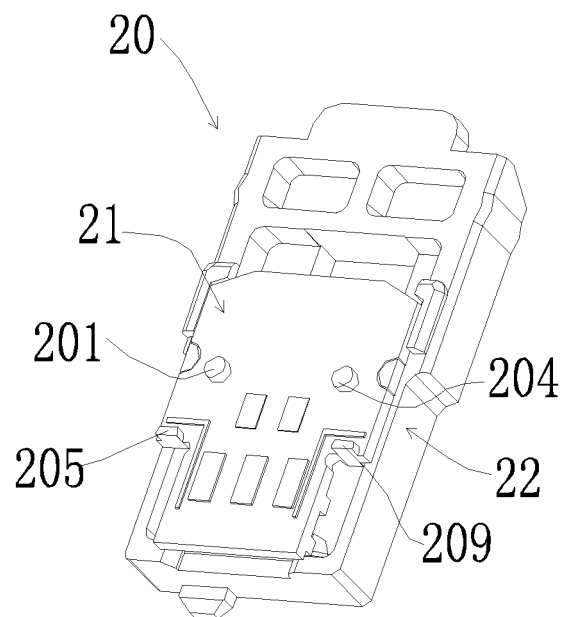


FIG. 14a

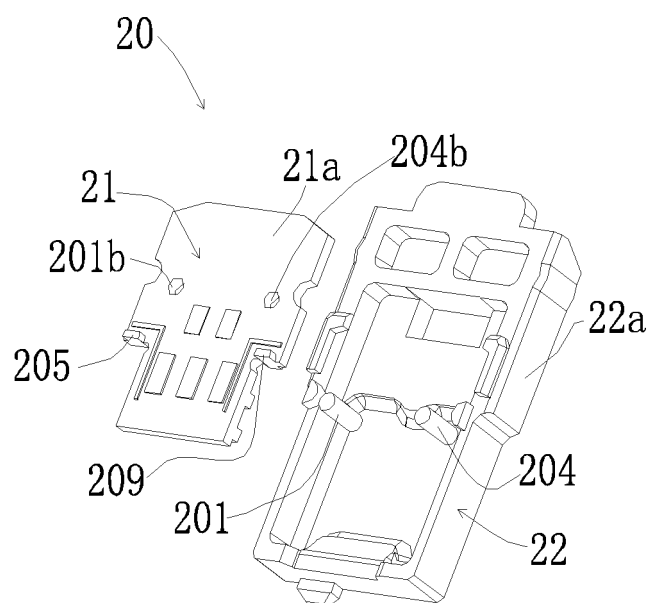


FIG. 14b

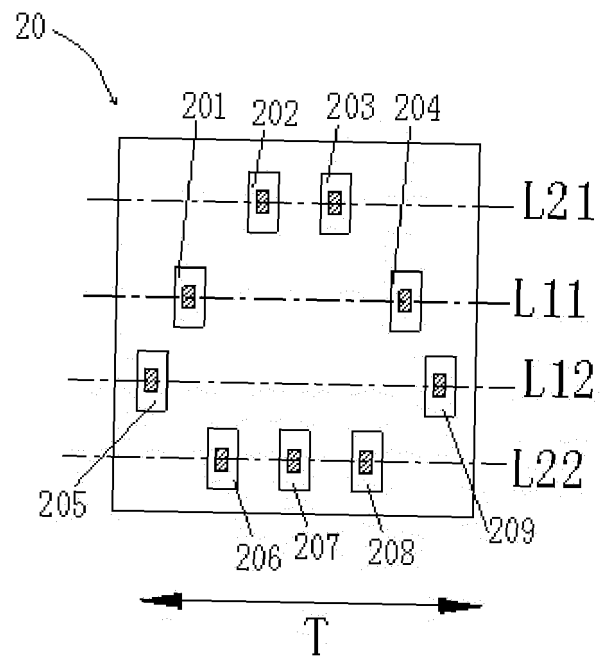


FIG. 15

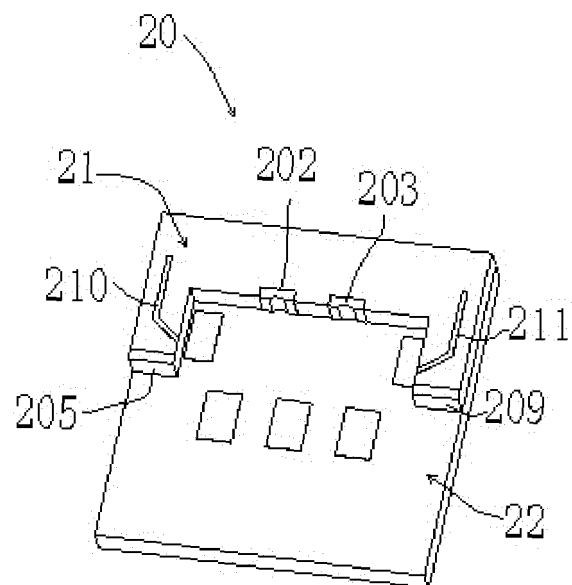


FIG. 16

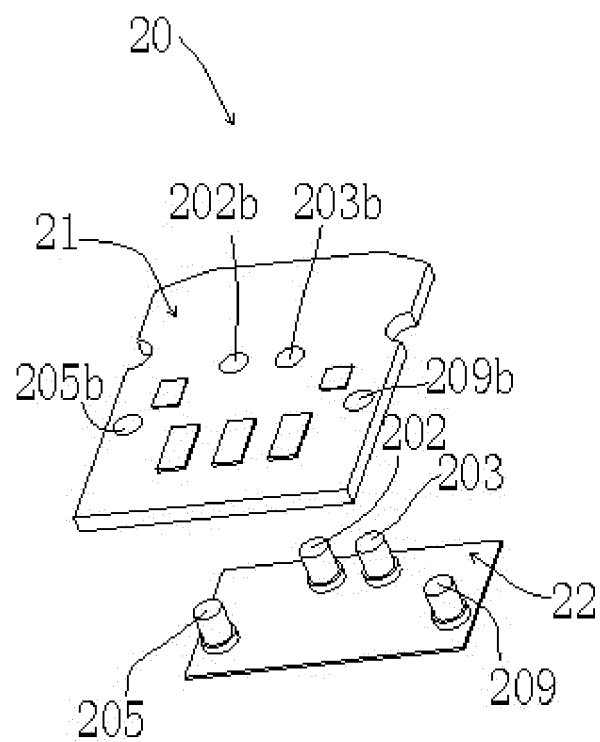


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/099628

A. CLASSIFICATION OF SUBJECT MATTER

B41J 2/175(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B41J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS; CNTXT; SIPOABS; DWPI; CNKI; WOTXT; EPTXT; USTXT: 墨盒, 芯片, 端子, 终端, 存储器, 接触, 电连接, 电压, 触针, 多排, 信号, ink cartridge, box, chip, memory, contact, electric+, detect+, terminal?, pin?, row

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 107901611 A (ZHUHAI NASIDA ENTERPRISE MANAGEMENT CO., LTD.) 13 April 2018 (2018-04-13) claims 1-23	1-23
A	CN 201109241 Y (PRINT-RITE TECHNOLOGY DEVELOPMENT CO., LTD. OF ZHUHAI) 03 September 2008 (2008-09-03) description, pages 3-4, and figures 1 and 2	1-23
A	CN 106864040 A (ZHUHAI NASIDA ENTERPRISE MANAGEMENT CO., LTD.) 20 June 2017 (2017-06-20) entire document	1-23
A	JP H04128049 A (CANON KK) 28 April 1992 (1992-04-28) entire document	1-23
A	CN 204914914 U (APEX MICROELECTRONICS CO., LTD.) 30 December 2015 (2015-12-30) entire document	1-23

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10 September 2018

Date of mailing of the international search report

24 October 2018

Name and mailing address of the ISA/CN

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Facsimile No. (86-10)62019451

Authorized officer

Telephone No.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/099628

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
CN 107901611 A	13 April 2018	None	
CN 201109241 Y	03 September 2008	None	
CN 106864040 A	20 June 2017	CN 106864040 B	25 May 2018
		WO 2017101249 A1	22 June 2017
JP H04128049 A	28 April 1992	None	
CN 204914914 U	30 December 2015	None	

Form PCT/ISA/210 (patent family annex) (January 2015)