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(54) **INTEGRATED CIRCUIT COMPRISING A BALUN**

(57) An integrated circuit and a method of making the same. The integrated circuit includes a semiconductor substrate. The integrated circuit also includes a balun. The balun includes a primary inductor coil having a first end and a second end. The first end of the primary inductor coil is coupled to a reference voltage. A second end of the primary inductor coil forms a single ended input of the balun. The balun also includes a secondary inductor coil having a first end and a second end. The first end and the second end form a differential output of the balun. The secondary inductor coil has a center tap coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

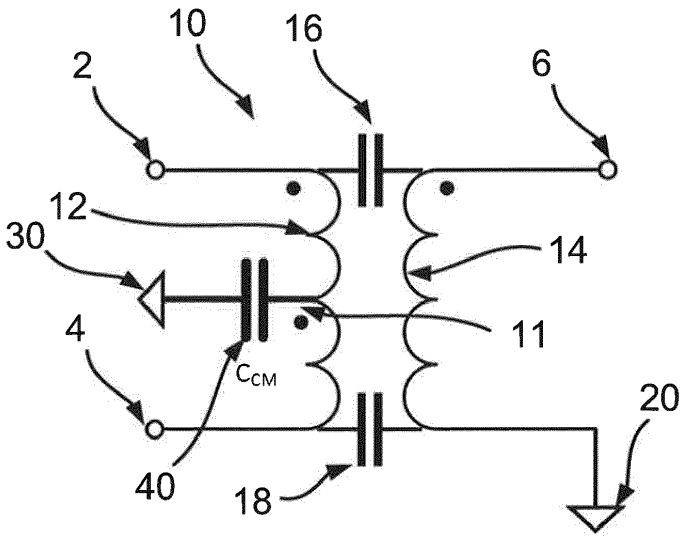

Fig. 1

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Description

BACKGROUND

[0001] The present specification relates to an integrated circuit comprising a semiconductor substrate and a balun. The present specification also relates to method of making such an integrated circuit.

[0002] At RF and mmWave frequencies, a balun (balanced to unbalanced converter) is used to transform a single-ended signal to a differential signal. A monolithically integrated balun is usually implemented with symmetrically coupled inductors. At high frequencies the parasitic capacitive coupling can cause an imbalance, resulting in a finite common-mode rejection ratio (CMRR). Imperfect balance could give rise to undesired common-mode signal injection (noise, etc.) and common- or mixed-mode instability.

SUMMARY

[0003] Aspects of the present disclosure are set out in the accompanying independent and dependent claims. Combinations of features from the dependent claims may be combined with features of the independent claims as appropriate and not merely as explicitly set out in the claims.

[0004] According to an aspect of the present disclosure, there is provided an integrated circuit comprising:

a semiconductor substrate; and
a balun comprising:

a primary inductor coil having a first end and a second end, wherein the first end of the primary inductor coil is coupled to a reference voltage, and wherein the second end of the primary inductor coil forms a single ended input of the balun; and
a secondary inductor coil having a first end and a second end, wherein the first end and the second end form a differential output of the balun, and wherein the secondary inductor coil has a center tap coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

[0005] According to another aspect of the present disclosure, there is provided a method of making an integrated circuit, the method comprising:

providing a semiconductor substrate; and
forming a balun on a major surface of the substrate by:

forming a primary inductor coil having a first end and a second end, wherein the first end of the primary inductor coil is coupled to a reference voltage, and wherein the second end of the primary inductor coil forms a single ended input of the balun; and
forming a secondary inductor coil having a first end and a second end, wherein the first end and the second end form a differential output of the balun, and wherein the secondary inductor coil has a center tap coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

[0006] The coupling of a center tap of the secondary inductor coil coupled to a reference voltage via a capacitance can allow a common mode rejection ratio (CMRR) of the balun to be tuned (e.g. by selecting the value of the capacitance). This may improve the performance of the device.

[0007] Conveniently, the capacitance (coupled to the center tap) for tuning a common mode rejection ratio of the balun may comprise a capacitor component having first and second capacitor plates.

[0008] The capacitance (coupled to the center tap) for tuning a common mode rejection ratio of the balun may comprise a ground shield located on or in the semiconductor substrate. The use of a ground shield in this way can simultaneously provide shielding for the balun and tuning of the CMRR by configuring (e.g. the shape and size of) the ground shield to select the capacitance that it provides. It is envisaged that the capacitance (coupled to the center tap) for tuning a common mode rejection ratio of the balun may comprise a combination of a ground shield and a separate capacitor component having first and second capacitor plates as noted above.

[0009] For effective shielding of the inductor coils, the ground shield may be located adjacent (e.g. underneath) the primary and secondary inductor coils.

[0010] The ground shield may be coupled to the center tap of the secondary inductor coil. This can provide optimal tuning of the CMRR.

[0011] The first end of the primary inductor coil may be coupled to said reference voltage via a capacitance for tuning

a common mode rejection ratio of the balun. This can allow for further tuning of the CMRR by choosing the value of the capacitance.

[0012] Conveniently, the primary inductor coil and the secondary inductor coil may comprise patterned metal features located in a metallization stack on a major surface of the semiconductor substrate.

[0013] Conveniently, the ground shield may comprise a patterned metal feature located in a metal layer of the metallization stack.

[0014] The center tap may form a virtual ground node of the secondary inductor coil.

[0015] The reference voltage to which the center tap of the secondary inductor coil may be coupled via said capacitance may be ground.

[0016] The reference voltage to which the first end of the primary inductor coil is coupled may be ground.

[0017] According to a further aspect of the present disclosure, there is provided a differential transceiver comprising the integrated circuit of any of claims 1 to 11.

[0018] According to another aspect of the present disclosure, there is provided a power amplifier comprising the integrated circuit of any of claims 1 to 11.

[0019] According to a further aspect of the present disclosure, there is provided a low noise amplifier comprising the integrated circuit of any of claims 1 to 11.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Embodiments of this disclosure will be described hereinafter, by way of example only, with reference to the accompanying drawings in which like reference signs relate to like elements and in which:

Figure 1 shows a balun according to an embodiment of this disclosure;
Figure 2 shows a balun according to another embodiment of this disclosure;
Figures 3-5 show the various metal layers of a balun according to an embodiment of this disclosure;
Figure 6 shows some of the metal layers of a balun according to another embodiment of this disclosure;
Figure 7 shows a balun;
Figure 8 models the phase imbalance, amplitude imbalance and CMRR of the balun of Figure 7;
Figure 9-10 show a network analysis of a balun according to an embodiment of this disclosure;
Figure 11 models the phase imbalance, amplitude imbalance and CMRR of a balun of the kind shown in Figure 1;
Figure 12 models the phase imbalance, amplitude imbalance and CMRR of a balun of the kind shown in Figure 2;
Figure 13 models the phase imbalance, amplitude imbalance and CMRR of a balun of the kind shown in Figure 1, which is provided also with a patterned ground shield; and
Figure 14 models the phase imbalance, amplitude imbalance and CMRR of a balun of the kind shown in Figure 2, which is provided also with a patterned ground shield.

DETAILED DESCRIPTION

[0021] Embodiments of this disclosure are described in the following with reference to the accompanying drawings.

[0022] Figure 1 shows a balun 10 according to an embodiment of this disclosure. The balun 10 is provided on an integrated circuit. The integrated circuit comprises a semiconductor substrate, which may for instance comprise silicon. Further details of the construction and manufacture of a balun 10 of the kind disclosed herein will be set out below in relation to Figures 3 to 6.

[0023] The balun 10 in Figure 1 includes a primary inductor coil 14 and a secondary inductor coil 12. The primary inductor coil 14 has a first end and a second end, with a number of windings located in-between. The first end of the primary inductor coil 14 is coupled to a reference voltage 20. Typically, the reference voltage 20 may be ground. The second end of the primary inductor coil 14 forms a single ended input 6 of the balun. The secondary inductor coil 12 has a first end and a second end, which form a differential output 2, 4 of the balun 10. The capacitance between the ends of the primary inductor coil 14 and the secondary inductor coil 12 are represented in Figure 1 by the capacitances 16, 18.

[0024] In accordance with embodiments of this disclosure, the secondary inductor coil 12 is provided with a center tap 11. The center tap 11 is typically provided at a point located midway along the turn(s) between the first end and the second end of the secondary inductor coil 12. The center tap 11 may thus form a virtual ground node of the secondary inductor coil 12. The center tap 11 is coupled to a reference voltage 30. Typically, the reference voltage 30 may be ground. In particular, and as shown in Figure 1, the center tap 11 is coupled to the reference voltage 30 via a capacitance 40. The coupling of a center tap 11 of the secondary inductor coil 12 to a reference voltage via the capacitance 40 in this way can allow a common mode rejection ratio (CMRR) of the balun 10 to be tuned. This may be achieved by, for instance, selecting the value of the capacitance. Accordingly, the performance of the device may be improved.

[0025] In some embodiments, the capacitance 40 may be implemented as a separate capacitor component having

first and second capacitor plates, coupled between the center tap 11 and the reference voltage 30. In such embodiments, tuning the CMRR may be achieved conveniently by choosing the capacitance value of the separate capacitor component.

[0026] In some embodiments, the capacitance 40 may be implemented using a ground shield of the balun 10. The ground shield is typically located on or in the semiconductor substrate (e.g. adjacent to (e.g. beneath) the primary inductor coil 14 and the secondary inductor coil 12). The ground shield in such embodiments is connected to the virtual ground node provided by the center tap 11. The use of a ground shield in this way can simultaneously provide electromagnetic (EM) shielding for the balun 10 and tuning of the CMRR by configuring (e.g. the shape and size of) the ground shield to select the capacitance that it provides. The provision of a ground shield of this kind will be described in more detail below in relation to Figure 6.

[0027] It is envisaged that the capacitance 40 may be implemented using a combination of a ground shield and a separate capacitor component as noted above.

[0028] Figure 2 shows a balun 10 according to another embodiment of this disclosure. The balun 10 in Figure 2 is similar to the balun 10 shown in Figure 1, and only the differences will be described below.

[0029] The balun 10 in Figure 2 is provided with a capacitance 42. In this embodiment, the first end of the primary inductor coil 14 is coupled to the reference voltage 20 via the capacitance 42. The capacitance 42 may be implemented as a separate capacitor component having first and second capacitor plates, coupled between the first end of the primary inductor coil 14 and the reference voltage 20. In such embodiments, further tuning of the CMRR may be achieved conveniently by choosing the capacitance value of the separate capacitor component. The CMRR tuning in the embodiment of Figure 2 may thus be provided by a combination of the capacitance 40 and the capacitance 42. As noted above, the capacitance 40 may be implemented as a separate capacitor component and/or by a ground shield.

[0030] Figures 3-5 show the various metal layers of a balun 10 according to an embodiment of this disclosure. The primary inductor coil 14 and the secondary inductor coil 12 described above may be implemented as patterned metal features located in a metallization stack 100 on a major surface of the semiconductor substrate of the integrated circuit. As is known in the art of semiconductor manufacturing, metallization stacks typically include a plurality of metal layers including lithographically patterned metal features. The stack 100 typically also includes via layers, which are sandwiched between the metal layers. The via layers include electrically conductive vias, for interconnecting the patterned metal features located in the neighbouring metal layers.

[0031] In the example of Figures 3 to 5, the metallization stack 100 includes at least six metal layers (M1, M2, M3, M4, M5, M6) and intervening via layers (VI, V2, V3, V4, V5). The primary inductor coil 14 and the secondary inductor coil 12 are implemented in metal layers M4, M5 and M6. Figure 3 shows the patterned metal features located in metal layer M4, plus the features located in the via layer (V4) between M4 and M5. Figure 4 shows the patterned metal features located in metal layer M5, plus the features located in the via layer (V5) between M5 and M6. Figure 5 shows the patterned metal features located in metal layer M6, plus (again) the features located in the via layer (V5) between M5 and M6.

[0032] In Figure 3, the metal feature 52 forms the part of the secondary inductor coil 12 located in M4 and V4. The metal features 54 form the differential output of the balun. The metal features 56 is located in via layer V4 and connect the features 54 to corresponding features in metal layer M5.

[0033] In Figure 4, metal feature 62 forms the part of the secondary inductor coil 12 located in M5. Metal feature 64 forms the part of the primary inductor coil 14 located in M5. Metal feature 69A forms a first end of the primary inductor coil 14, which may be coupled to a reference voltage. Metal feature 69B forms a second end of the primary inductor coil 14, which forms the single ended input of the balun. Metal features 67, which are located in via layer V5, connect the features of the primary inductor coil 14 in M5 to the features of the primary inductor coil 14 in M6. Metal features 66, which are located in via layer V5, connect the features of the secondary inductor coil 12 in M5 to the features in metal layer M6. Metal features 68 form the differential output of the balun (along with the features 54 shown in Figure 3).

[0034] In Figure 5, the metal feature 70 forms the part of the secondary inductor coil 12 located in M6. The metal feature 72 forms the part of the primary inductor coil 14 located in M6. Metal features 66 located in via layer V5 (described above in relation to Figure 4) are also visible in Figure 5. Metal feature 74 forms a ground reference ring around the structure, which have the purpose of defining the input and output common-mode ground potential both at the primary and secondary inductor coil positions.

[0035] Figure 6 shows, in addition to the features of Figure 5, the optional provision of a patterned ground shield formed by metal feature 110. The metal feature 110 forming the ground shield may be provided adjacent the primary inductor coil 14 and the secondary inductor coil 12. For instance, as shown in Figure 6, the metal feature 110 forming the ground shield is provided beneath the primary inductor coil 14 and the secondary inductor coil 12.

[0036] As noted above, in some embodiments, the capacitance 40 of the balun 10 may be implemented at least in part by a ground shield. Figure 6 shows some of the metal layers of a balun according to another embodiment of this disclosure, in which such a ground shield 110 is included. Note that the features of the primary inductor coil 14, the secondary inductor coil 12, the center tap 11 and so on in this embodiment may be substantially as already described above in relation to Figure 3 to 5.

[0037] The ground shield 110 may be provided in a metal layer of a via layer of the metallization stack 100. As can be appreciated from Figure 6, for effective shielding of the features of the balun 10, the ground shield in this embodiment is located beneath the primary 14 and secondary 12 inductor coils. For instance, when viewed from above the major surface of the substrate upon which the metallization stack 100 is provided, the turns of the primary 14 and secondary 12 inductor coils may be located within an outer peripheral edge of the ground shield 110.

[0038] According to an embodiment of the present disclosure, a method of making integrated circuit may include the following steps. The method includes providing a semiconductor substrate. As noted above, the substrate may, for instance, be a silicon substrate. It is envisaged that the substrate may comprise part of a larger wafer, which may subsequently be singulated (diced), for manufacturing a plurality of like integrated circuits, each including a balun according to the present disclosure.

[0039] The substrate may, as part of the back end of line (BEOL) manufacturing process, be provided with a metallization stack 100. The stack 100 may include features for interconnecting components of the integrated circuit located in the substrate and for providing input/output terminals to the substrate. As described herein, the metallization stack 100 may also include patterned metal features implementing the balun 10.

[0040] Accordingly, the method may also include forming a balun on a major surface of the substrate. This may be done by using BEOL metallization techniques to form the primary inductor coil 14 and the secondary inductor coil 12, the center tap 11 and optional ground shield 110. As noted above, the primary inductor coil 14 has a first end and a second end. The first end of the primary inductor coil 14 is coupled to a reference voltage, which may be ground. For instance, the first end of the primary inductor coil 14 may be coupled to a ground terminal of the substrate. The second end of the primary inductor coil 14 forms a single ended input of the balun. As also noted above, the secondary inductor coil 12 has a first end and a second end, which form the differential output of the balun 10. The secondary inductor coil also has a center tap 11 coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun 10. Again, the reference voltage may be ground (e.g. the capacitance may be coupled to a ground terminal of the substrate).

[0041] Where the capacitances 40 and 42 comprise separate capacitor components, these may also be implemented in the metallization stack, for instance by providing patterned metal features forming the capacitor plates thereof.

[0042] Figure 7 shows a balun, and Figure 8 models the phase imbalance, amplitude imbalance and CMRR of the balun of Figure 7.

[0043] In Figure 7, the second end of the primary inductor coil (i.e. the end that forms the single ended input) of the balun is labelled as terminal 1, the first end of the secondary inductor coil of the balun is labelled as terminal 2, and the second end of the secondary inductor coil of the balun is labelled as terminal 3. The inductance of the primary inductor coil may be denoted as L_p, and the inductance of the secondary inductor coil may be denoted as L_s. L_s includes two contributions $L_{s/2}$, each from a respective part of the secondary inductor coil that is located on either side of the center tap. The capacitance between the primary inductor coil and the secondary inductor coil of the balun is represented by the capacitances C_p.

[0044] The single ended to differential mode transfer, the single ended to common mode transfer, the CMRR and the imbalance of the balun shown in Figure 7 may be expressed as follows: $S_{d1} = \frac{1}{\sqrt{2}}\left(S_{21} - S_{31}\right)$: single-ended to differential-mode transfer $S_{c1} = \frac{1}{\sqrt{2}}\left(S_{21} + S_{31}\right)$: single-ended to common-mode transfer

$$CMRR = 20 \cdot \log\left|\frac{S_{21} - S_{31}}{S_{21} + S_{31}}\right|$$: common-mode rejection ratio

$$\text{Imbalance} = -\frac{S_{21}}{S_{31}}$$

[0045] Turning to Figure 8, the upper graph models the phase imbalance 80 and the amplitude imbalance 81 of the balun of Figure 7, while the lower graph models the CMRR 82. As may be appreciated from Figure 8, the balun of Figure 7 exhibits imperfect imbalance and limited CMRR.

[0046] Figure 9-10 show a network analysis of a balun according to an embodiment of this disclosure.

[0047] The CMRR of the balun may be converted from s- to z-parameters (see S. Aloui, et al., "High-Gain and Linear 60-GHz Power Amplifier With a Thin Digital 65-nm CMOS Technology," IEEE Trans. on MTT, vol. 61, no. 6, pp. 2425-2437, June 2013):

$$CMRR\_Z = \frac{Z_{31}\cdot\left(Z_0 + Z_{22} + Z_{32}\right) - Z_{21}\cdot\left(Z_0 + Z_{33} + Z_{32}\right)}{Z_{31}\cdot\left(Z_0 + Z_{22} - Z_{32}\right) + Z_{21}\cdot\left(Z_0 + Z_{33} - Z_{32}\right)}$$

[0048] Assuming $Z_{22} \approx Z_{33}$ (symmetry) and $Z_{32} << Z_0 + Z_{22(33)}$, then:

$$Z_{22} = Z_{33} \rightarrow CMRR\_Z = \left(\frac{Z_0 + Z_{22} + Z_{32}}{Z_0 + Z_{22} - Z_{32}}\right)\cdot\left(\frac{Z_{31} - Z_{21}}{Z_{31} + Z_{21}}\right)$$

$$Z_{32} = \left(Z_{22} + Z_0\right) \rightarrow CMRR\_Z \approx \left(\frac{Z_{31} - Z_{21}}{Z_{31} + Z_{21}}\right)$$

[0049] To reach high CMRR_Z, the condition $Z_{31} + Z_{21}$ may be satisfied.

[0050] In the ideal model, this goal may be reached by adding a compensation capacitor (CCM) for the common-mode signals (note that in Figure 10 the balun is modeled by two mutually coupled inductors L_1 and L_2).

[0051] Resulting from the network analysis shown in Figures 9 and 10 and set out above:

$$Z_{21} = \left.\frac{v_2}{i_1}\right|_{i_2 = i_3 = 0} = j\omega M\left[1 + \frac{L_1 - M}{M\cdot X}\left(L_2 - M - \frac{1}{\omega^2 C_{CM}}\right)\right]$$

$$Z_{31} = \left.\frac{v_3}{i_1}\right|_{i_2 = i_3 = 0} = -j\omega M\left[1 - \frac{L_1 - M}{X}\left(1 + \frac{1}{\omega^2 M\cdot C_{CM}}\right)\right]$$

$$X = L_1 + L_2 - 2M - \frac{C_P + C_{CM}}{\omega^2 C_P C_{CM}}$$

[0052] Now, solving for

$$Z_{31} + Z_{21} = 0 \Rightarrow C_{CM} = \frac{1}{\omega^2 L_2 / 2} \Rightarrow Z_{22} = Z_{33} = \frac{L_2}{2X}\left(L_1 - \frac{1}{\omega^2 C_p}\right) - \frac{M^2}{X}$$

[0053] This solution has been checked by simulations in which it has been found that the solution is also valid for the non-simplified model (i.e. it is valid for both the right hand side circuit and the left hand side circuit shown in Figure 9).

[0054] Turning to Figure 11, the upper graph models the phase imbalance 83 and the amplitude imbalance 84 of a balun of the kind shown in Figure 1, which includes a center tap 11 provided at a point located midway along the turn(s) between the first end and the second end of the secondary inductor coil 12, and in which the center tap 11 is coupled to ground via a capacitance 40. The lower graph in Figure 11 models CMRR Z 85 and CMRR 86 of the balun 10. The capacitance 40 of the balun 10 modelled in Figure 11 comprises a separate capacitor component as noted above. As may be appreciated from Figure 11, a balun according to an embodiment of this invention has an improved balance and an improved CMRR (>34dB and the bandwidth of the device). In accordance with an embodiment of this disclosure, a particular bandwidth of interest is in the range 26-30 GHz.

[0055] Turning to Figure 12, the upper graph models the phase imbalance 87 and the amplitude imbalance 88 of a balun of the kind shown in Figure 2, which includes a center tap 11 provided at a point located midway along the turn(s) between the first end and the second end of the secondary inductor coil 12, in which the center tap 11 is coupled to ground via a capacitance 40, and in which the first end of the primary inductor coil 14 is coupled to a reference voltage 20 via the capacitance 42. The lower graph in Figure 12 models CMRR_Z 89 and CMRR 90 of the balun 10. The capacitances 40 and 42 of the balun 10 modelled in Figure 12 each comprise a separate capacitor component as noted above. As may be appreciated from Figure 12, a balun according to an embodiment of this invention has a further improved balance and a further improved CMRR (>42dB and the bandwidth of the device). Again, in accordance with an embodiment of this disclosure, a particular bandwidth of interest is in the range 26-30 GHz.

[0056] Turning to Figure 13, the upper graph models the phase imbalance 91 and the amplitude imbalance 92 of a balun of the kind shown in Figure 1, which includes a center tap 11 provided at a point located midway along the turn(s) between the first end and the second end of the secondary inductor coil 12, and in which the center tap 11 is coupled to ground via a capacitance 40. The lower graph in Figure 13 models CMRR_Z 93 and CMRR 94 of the balun 10. The capacitance 40 of the balun 10 modelled in Figure 13 comprises a combination of separate capacitor component and a ground shield 110 of the kind described above in relation to Figure 6. As may be appreciated from Figure 13, a balun according to an embodiment of this invention has a yet further improved balance and a yet further improved CMRR (>40dB and the bandwidth of the device). Again, in accordance with an embodiment of this disclosure, a particular bandwidth of interest is in the range 26-30 GHz.

[0057] Turning to Figure 14, the upper graph models the phase imbalance 95 and the amplitude imbalance 96 of a balun of the kind shown in Figure 2, which includes a center tap 11 provided at a point located midway along the turn(s) between the first end and the second end of the secondary inductor coil 12, in which the center tap 11 is coupled to ground via a capacitance 40, and in which the first end of the primary inductor coil 14 is coupled to a reference voltage 20 via the capacitance 42. The lower graph in Figure 14 models CMRR_Z 97 and CMRR 98 of the balun 10. The capacitance 40 of the balun 10 modelled in Figure 14 comprises a combination of separate capacitor component and a ground shield 110 of the kind described above in relation to Figure 6. The capacitance 42 of the balun 10 modelled in Figure 14 comprises a separate capacitor component as noted above. As may be appreciated from Figure 14, a balun according to an embodiment of this invention also has a yet further improved balance and a yet further improved CMRR (>50dB and the bandwidth of the device). Again, in accordance with an embodiment of this disclosure, a particular bandwidth of interest is in the range 26-30 GHz.

[0058] In integrated circuit including a balun 10 of the kind described above may have a number of applications. For instance, in some embodiments there may be provided a differential transceiver (e.g. for operation at RF and mmWave frequencies) including an integrated circuit having a balun 10 of the kind described above. Such a differential transceiver may be provided in mobile or fixed network systems. In another embodiment, there may be provided a power amplifier (PA) including an integrated circuit having a balun 10 of the kind described above, in which the balun 10 operates as an output balun of the power amplifier. In a further embodiment, there may be provided a low noise amplifier (LNA) including an integrated circuit having a balun 10 of the kind described above, in which the balun operates as an input balun of the low noise amplifier.

[0059] Accordingly, there has been described an integrated circuit and a method of making the same. The integrated circuit includes a semiconductor substrate. The integrated circuit also includes a balun. The balun includes a primary inductor coil having a first end and a second end. The first end of the primary inductor coil is coupled to a reference voltage. A second end of the primary inductor coil forms a single ended input of the balun. The balun also includes a secondary inductor coil having a first end and a second end. The first end and the second end form a differential output

of the balun. The secondary inductor coil has a center tap coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

[0060] Although particular embodiments of this disclosure have been described, it will be appreciated that many modifications/additions and/or substitutions may be made within the scope of the claims.

Claims

1. An integrated circuit comprising:

a semiconductor substrate; and
a balun comprising:

a primary inductor coil having a first end and a second end, wherein the first end of the primary inductor coil is coupled to a reference voltage, and wherein the second end of the primary inductor coil forms a single ended input of the balun; and
a secondary inductor coil having a first end and a second end, wherein the first end and the second end form a differential output of the balun, and wherein the secondary inductor coil has a center tap coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

2. The integrated circuit of claim 1, wherein the capacitance for tuning a common mode rejection ratio of the balun comprises a capacitor component having first and second capacitor plates.

3. The integrated circuit of claim 1 or claim 2, wherein the capacitance for tuning a common mode rejection ratio of the balun comprises a ground shield located on or in the semiconductor substrate.

4. The integrated circuit of claim 3, wherein the ground shield is located adjacent the primary and secondary inductor coils.

5. The integrated circuit of claim 3 or claim 4, wherein the ground shield is coupled to the center tap of the secondary inductor coil.

6. The integrated circuit of any preceding claim, wherein the first end of the primary inductor coil is coupled to said reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

7. The integrated circuit of any preceding claim, wherein the primary inductor coil and the secondary inductor coil comprise patterned metal features located in a metallization stack on a major surface of the semiconductor substrate.

8. The integrated circuit of claim 7, when dependent upon any of claims 3 to 5, wherein the ground shield comprises a patterned metal feature located in a metal layer of the metallization stack.

9. The integrated circuit of any preceding claim, wherein the center tap forms a virtual ground node of the secondary inductor coil.

10. The integrated circuit of any preceding claim, wherein the reference voltage to which the center tap of the secondary inductor coil is coupled via said capacitance is ground.

11. The integrated circuit of any preceding claim, wherein the reference voltage to which the first end of the primary inductor coil is coupled is ground.

12. A differential transceiver comprising the integrated circuit of any preceding claim.

13. A power amplifier comprising the integrated circuit of any of claims 1 to 11.

14. A low noise amplifier comprising the integrated circuit of any of claims 1 to 11.

15. A method of making an integrated circuit, the method comprising:

providing a semiconductor substrate; and
forming a balun on a major surface of the substrate by:

forming a primary inductor coil having a first end and a second end, wherein the first end of the primary inductor coil is coupled to a reference voltage, and wherein the second end of the primary inductor coil forms a single ended input of the balun; and
forming a secondary inductor coil having a first end and a second end, wherein the first end and the second end form a differential output of the balun, and wherein the secondary inductor coil has a center tap coupled to a reference voltage via a capacitance for tuning a common mode rejection ratio of the balun.

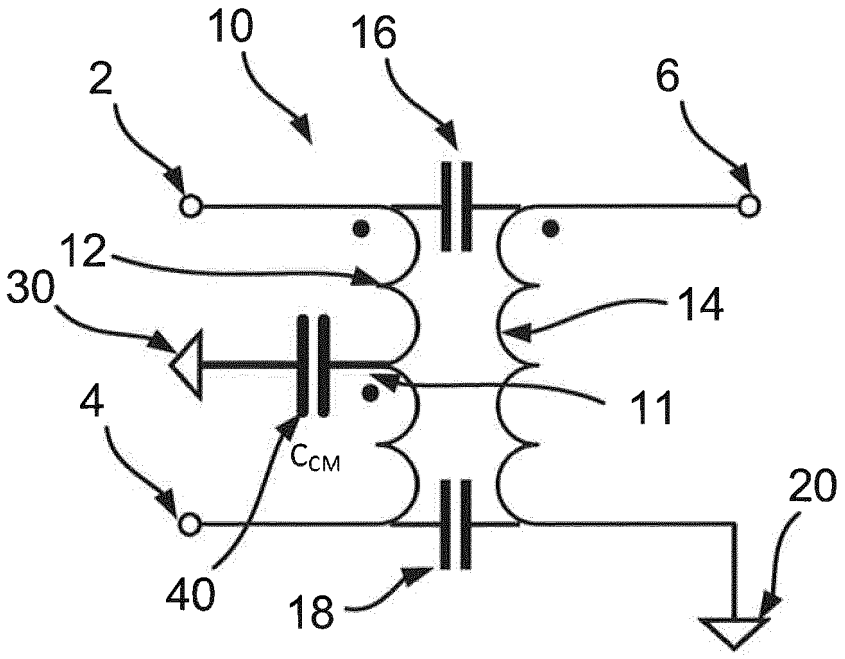
10
16
2
6
12
30
14
11
4
C_{CM}
20
40
18

Fig. 1

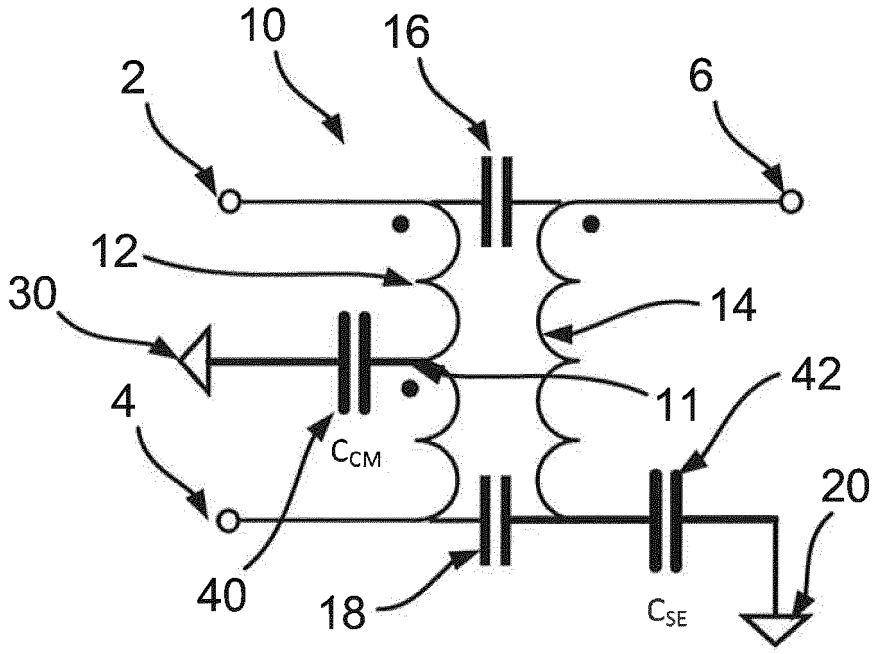
10
16
2
6
12
30
14
11
42
4
C_{CM}
20
40
18
C_{SE}

Fig. 2

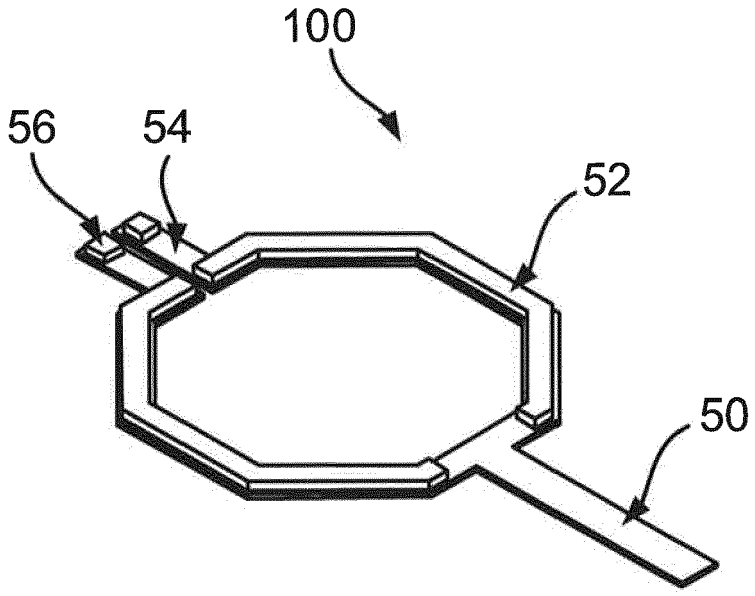

Fig. 3

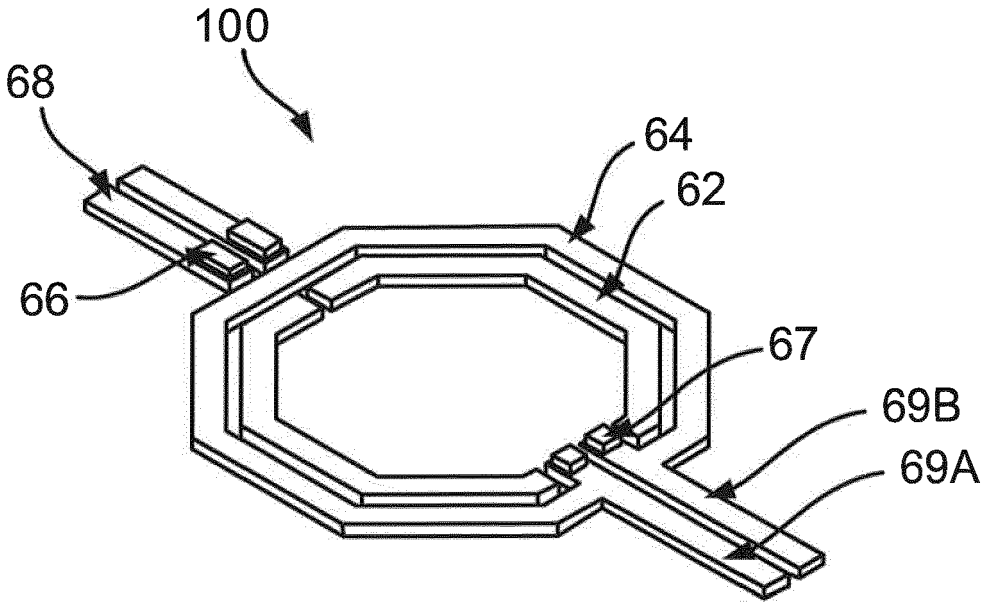

Fig. 4

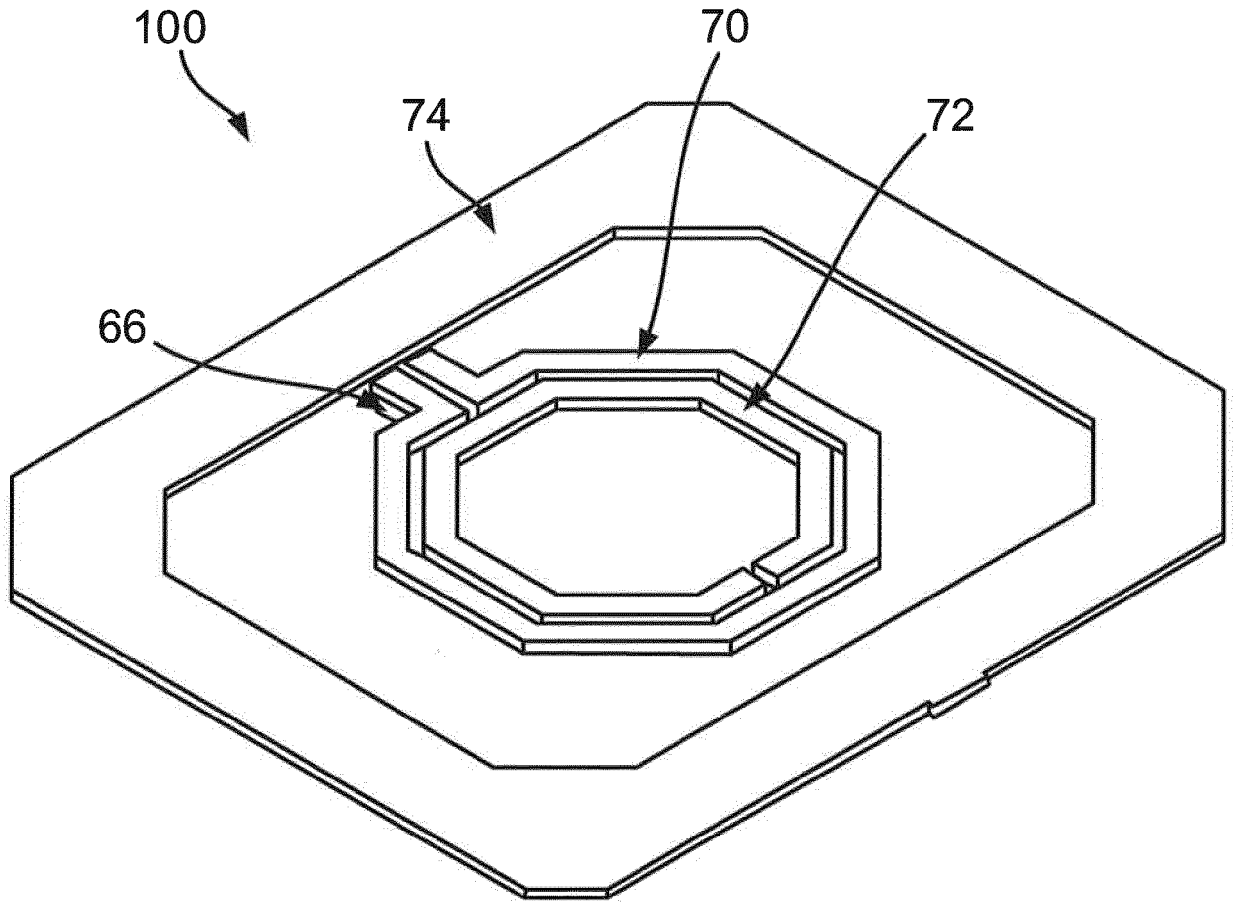

Fig. 5

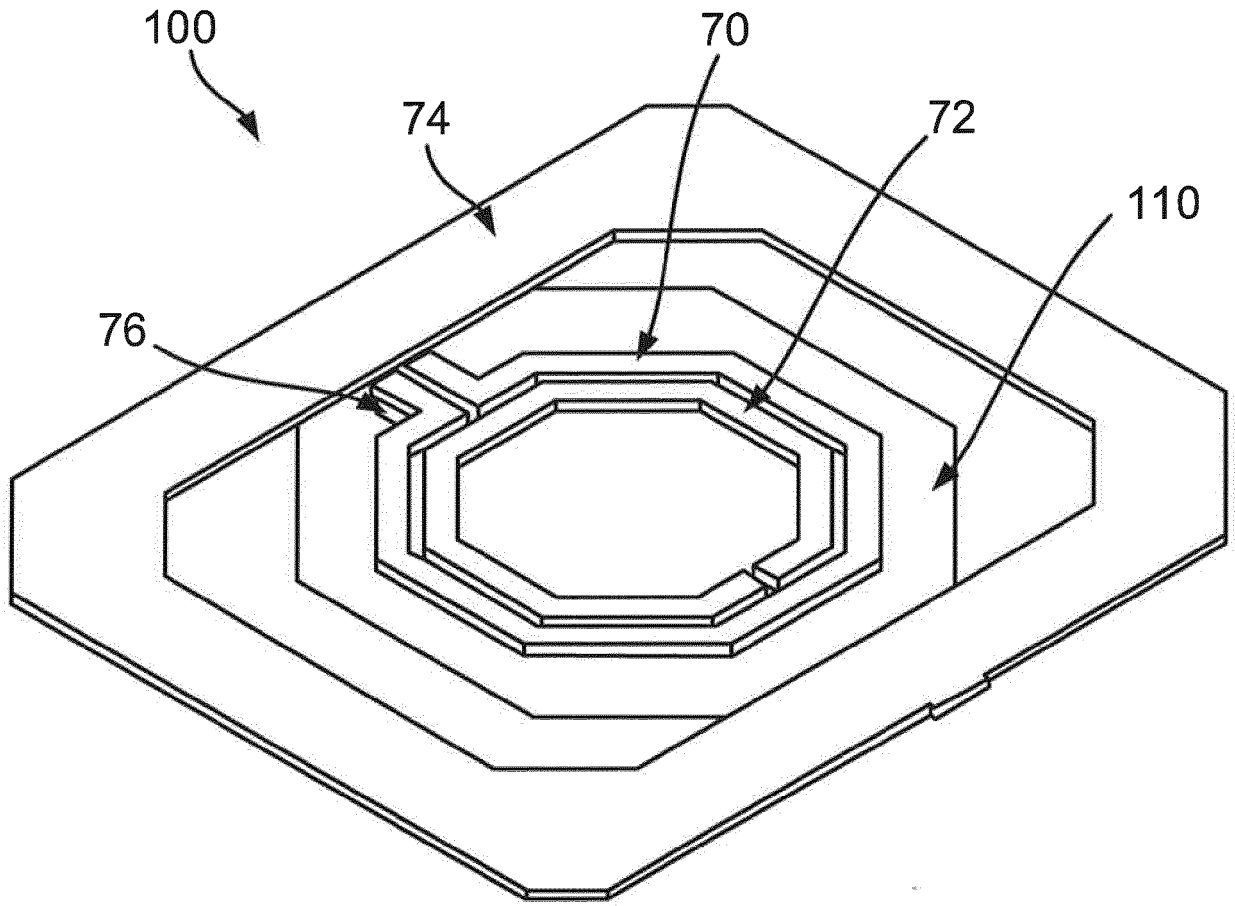

Fig. 6

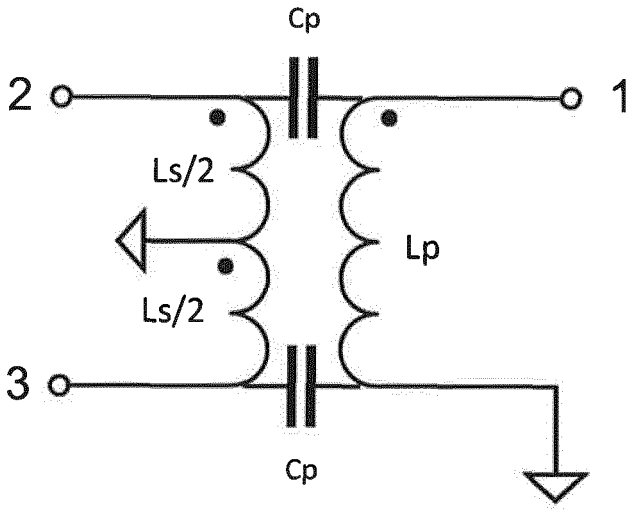
Cp
2
1
Ls/2
Lp
Ls/2
3
Cp

Fig. 7

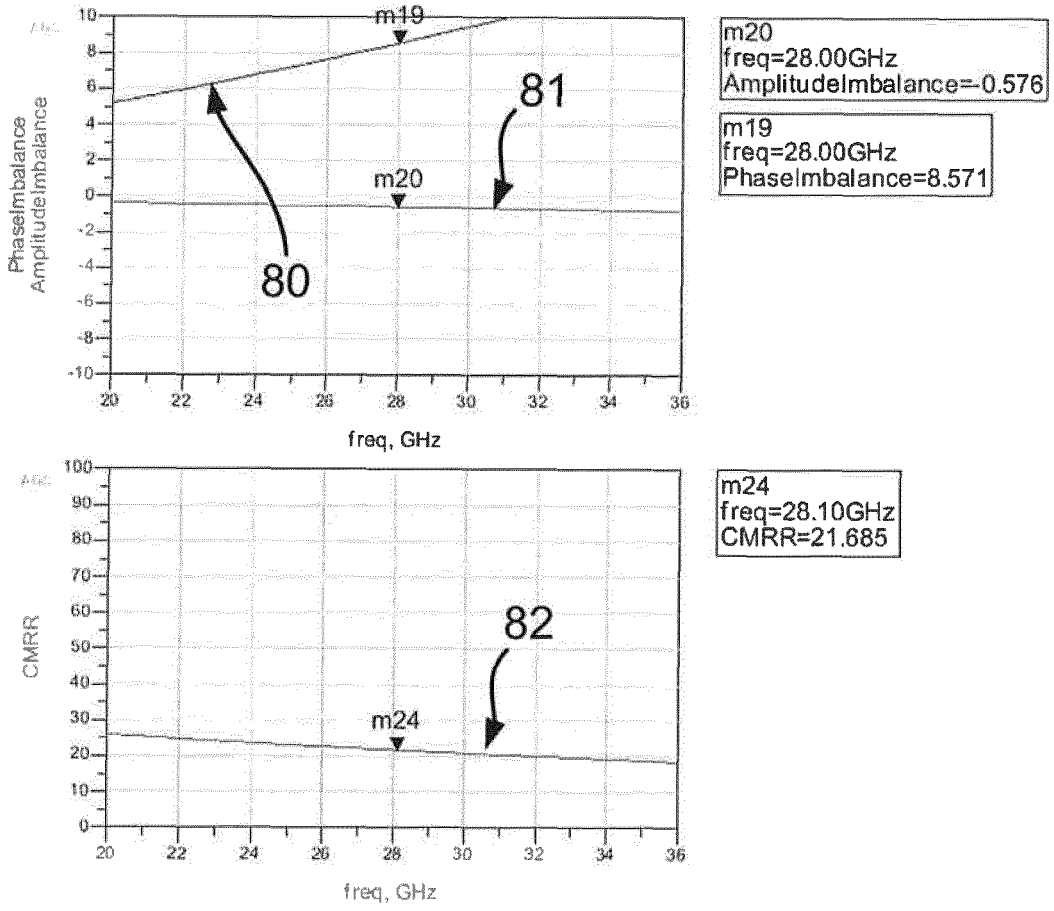
m19
81
m20
80
PhaseImbalance
AmplitudeImbalance
freq, GHz
m20
freq=28.00GHz
AmplitudeImbalance=-0.576
m19
freq=28.00GHz
PhaseImbalance=8.571
82
m24
CMRR
freq, GHz
m24
freq=28.10GHz
CMRR=21.685

Fig. 8

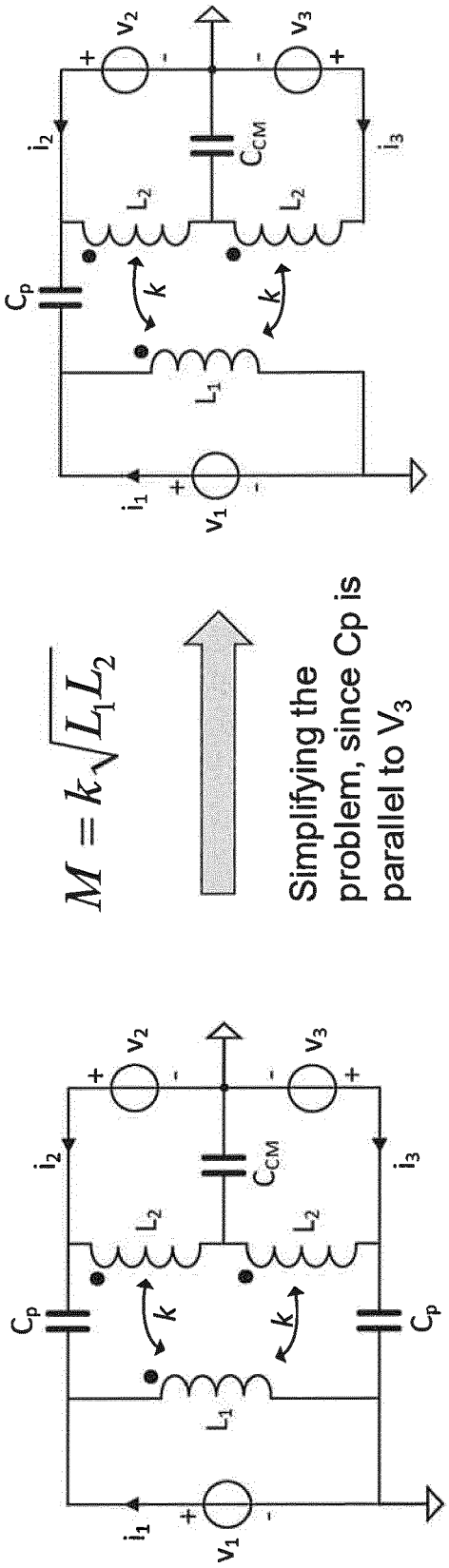
v2
v3
i2
i3
CCM
L2
L2
Cp
k
k
L1
i1
v1
$M = k\sqrt{L_1 L_2}$
Simplifying the problem, since Cp is parallel to V3
Cp

Fig. 9

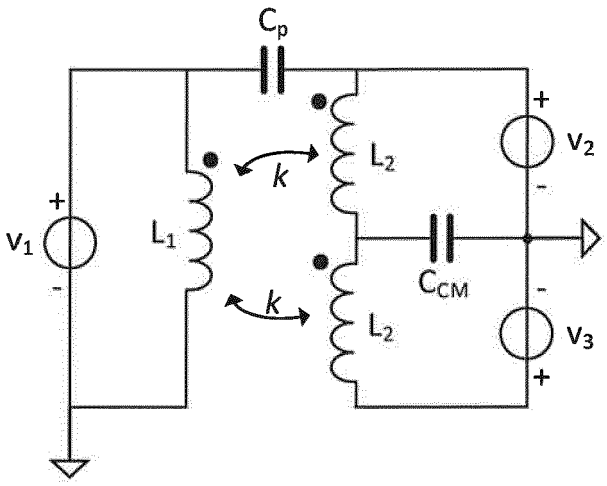
Cp
L1
L2
L2
k
k
CCM
V1
V2
V3
+
-

Fig. 10

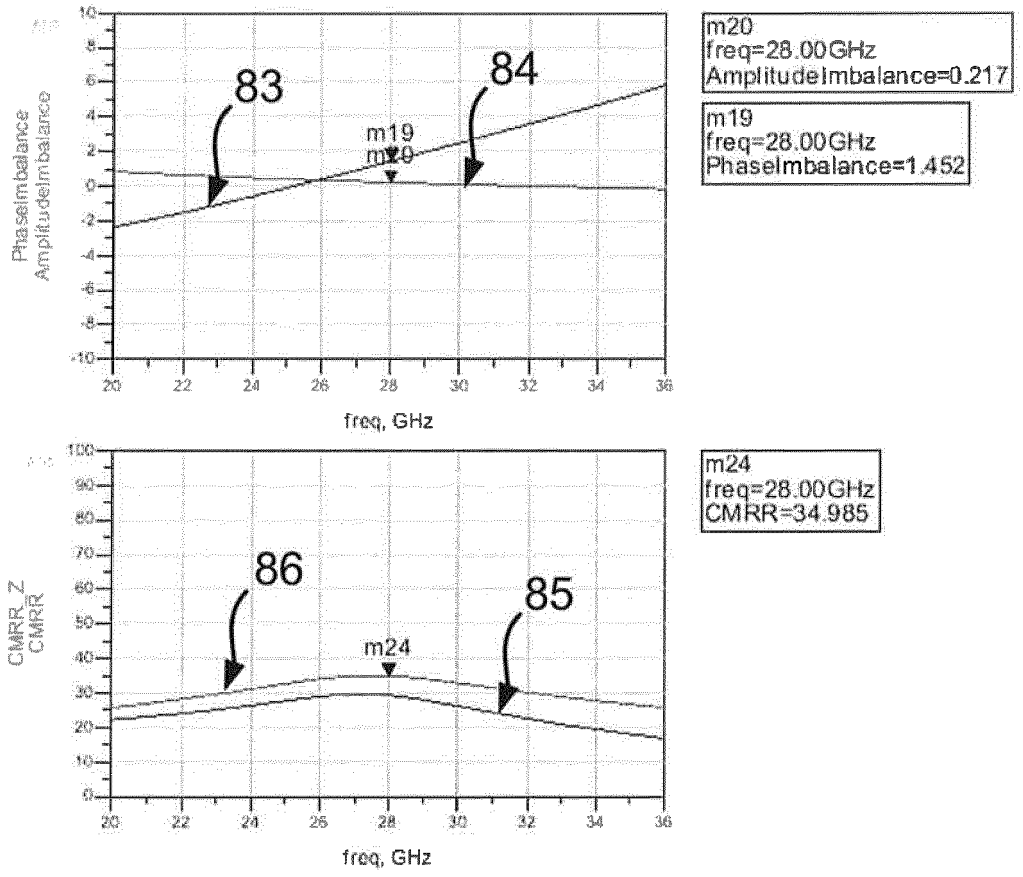
PhaseImbalance
AmplitudeImbalance
freq, GHz
83
84
m19
m20
m20
freq=28.00GHz
AmplitudeImbalance=0.217
m19
freq=28.00GHz
PhaseImbalance=1.452
CMRR_Z
CMRR
freq, GHz
86
85
m24
m24
freq=28.00GHz
CMRR=34.985

Fig. 11

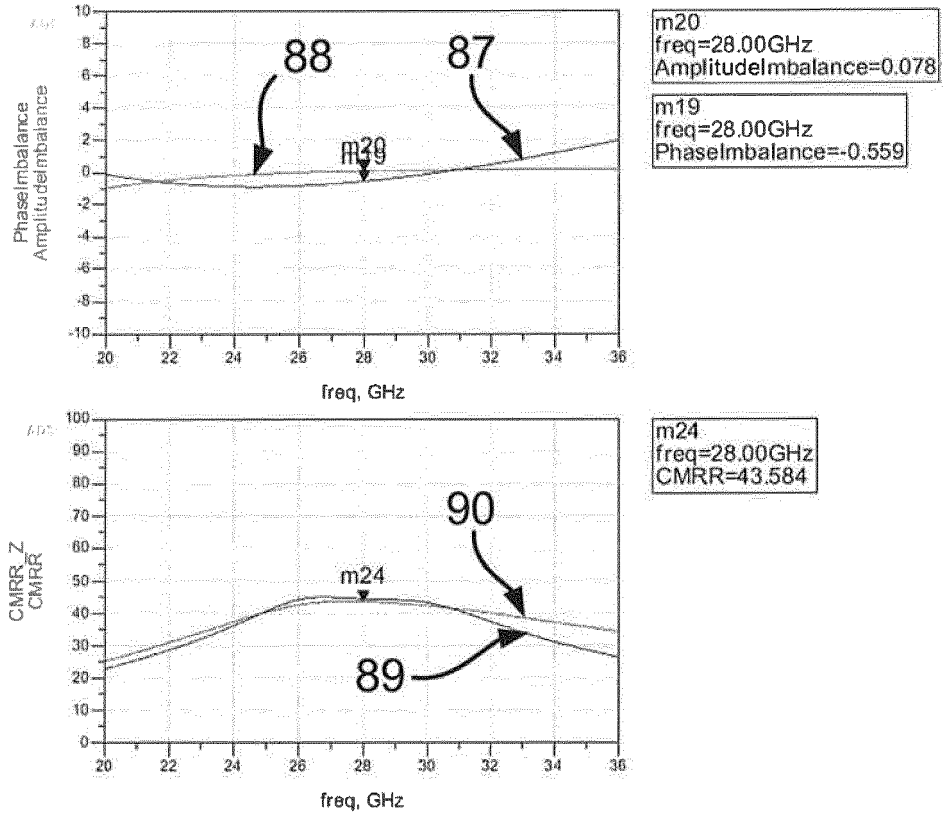
m20
freq=28.00GHz
AmplitudeImbalance=0.078
m19
freq=28.00GHz
PhaseImbalance=-0.559
88
87
m20
m19
PhaseImbalance
AmplitudeImbalance
freq, GHz
m24
freq=28.00GHz
CMRR=43.584
90
m24
89
CMRR_Z
CMRR
freq, GHz

Fig. 12

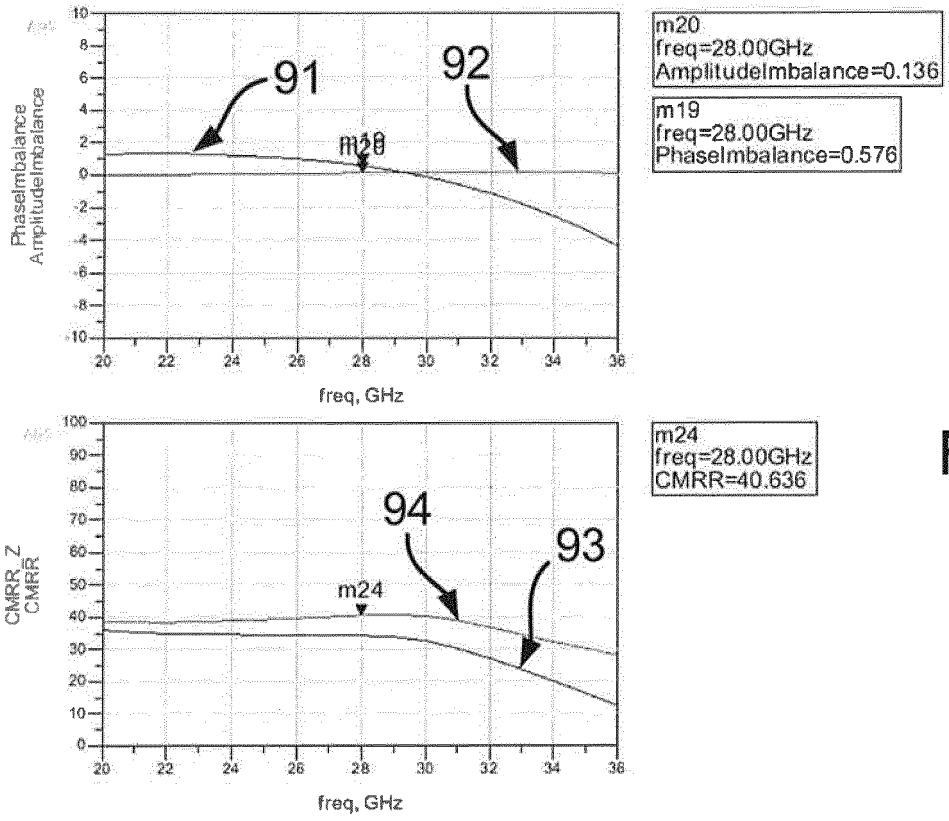
m20
freq=28.00GHz
AmplitudeImbalance=0.136
m19
freq=28.00GHz
PhaseImbalance=0.576
91
92
m20
PhaseImbalance
AmplitudeImbalance
freq, GHz
m24
freq=28.00GHz
CMRR=40.636
94
93
m24
CMRR_Z
CMRR
freq, GHz

Fig. 13

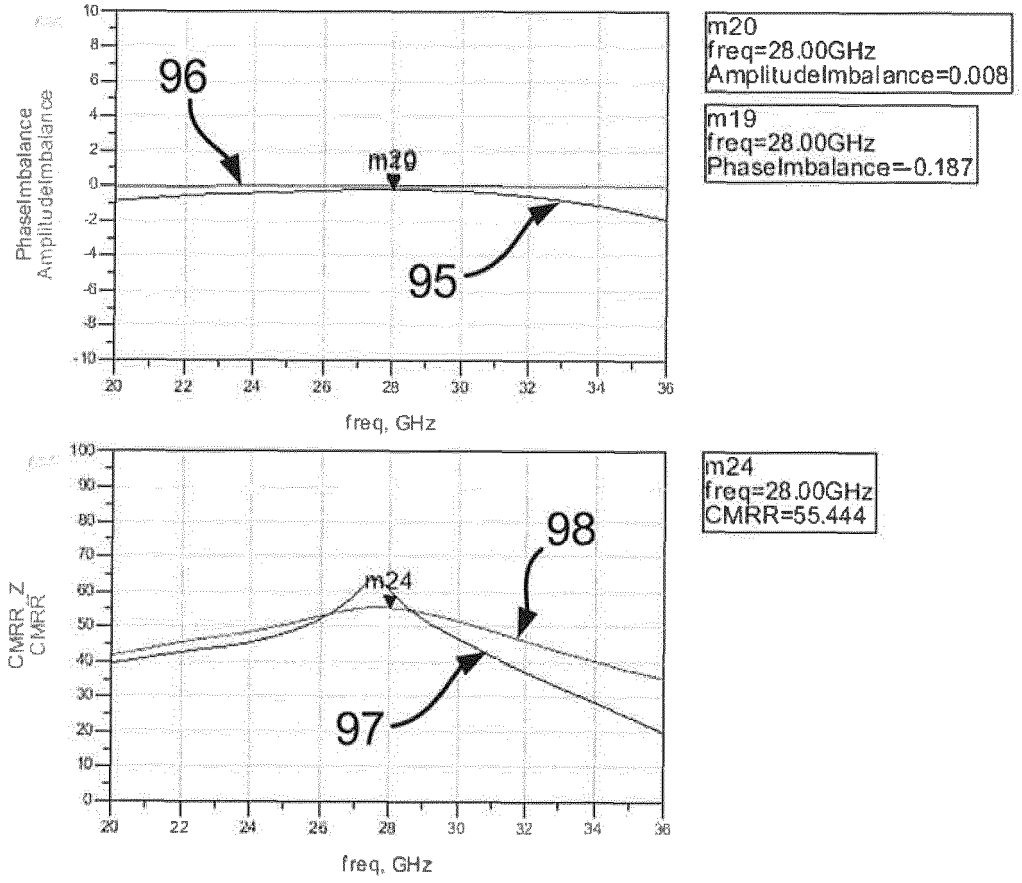
PhaseImbalance
AmplitudeImbalance
freq, GHz
96
95
m20
freq=28.00GHz
AmplitudeImbalance=0.008
m19
freq=28.00GHz
PhaseImbalance=-0.187
CMRR_Z
CMRR
freq, GHz
98
97
m24
freq=28.00GHz
CMRR=55.444

Fig. 14

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EUROPEAN SEARCH REPORT

Application Number
EP 18 21 2964

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	24 June 2019	Rouzier, Brice

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