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(54) **SEMICONDUCTOR DEVICE**

(57) A semiconductor device includes: a vertical Hall element provided in a first region of a semiconductor substrate, and having the first to the third electrodes arranged side by side in order along a first straight line; a circuit provided in a second region of the semiconductor substrate different from the first region, and having a heat source; and a second straight line intersecting orthogonally a current path for a Hall element drive current which flows between the first electrode and the third electrode. The second line passes a center of the vertical Hall element, and a center point of a region which reaches the highest temperature in the circuit during an operation of the vertical Hall element lies on the second straight line.

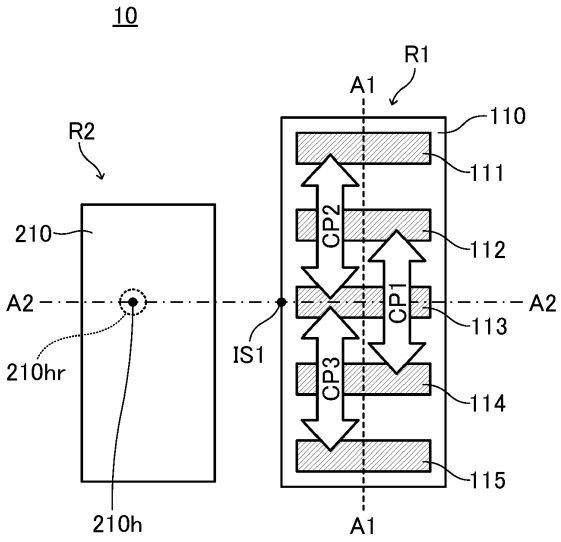

FIG. 1

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor device, and more particularly, to a semiconductor device including a vertical Hall element and a heat source.

2. Description of the Related Art

[0002] A Hall element is capable of detecting position or angle without contact as a magnetic sensor, and accordingly has various uses. While magnetic sensors that use a horizontal Hall element configured to detect magnetic field component perpendicular to a semiconductor substrate surface are particularly well known, there have been proposed various magnetic sensors that use a vertical Hall element configured to detect magnetic field component parallel to the substrate surface. Further, there has been proposed a magnetic sensor configured to detect a magnetic field two-dimensionally or three-dimensionally with use of a combination of a horizontal Hall element and a vertical Hall element.

[0003] Since it is difficult for a vertical Hall element to have a structure with high geometrical-symmetry, the vertical Hall element is more likely to generate a so-called offset voltage than the horizontal Hall element even though no magnetic field is applied. In a vertical Hall element which is used as a magnetic sensor, removal of the offset voltage is necessary. The spinning current method has been known as one of the methods.

[0004] For removal of the offset voltage through use of the spinning current method in a vertical Hall element which has five electrodes linearly arranged at some intervals on a surface of a semiconductor substrate, a method is known in which direction of the flow of the drive current is switched among four directions while the magnetic field is applied in a direction parallel to the semiconductor substrate (see, for example, FIGS. 1 of WO 03/036733).

[0005] With this method, the offset voltage is removed by adding or subtracting the following first to fourth output signals. The first output signal corresponds to a potential difference caused between a center electrode and each of two electrodes on opposite ends by a drive current flowing in a direction (referred to as "first direction") from one of two electrodes on both sides of the center electrode to the other, the second output signal corresponds to a potential difference caused between the center electrode and each of the two electrodes on opposite ends by the drive current flowing in a direction (referred to as "second direction") opposite to the first direction, the third output signal corresponds to a potential difference caused between the two electrodes on both sides of the center electrode by the drive current flowing in a direction (referred to as "third direction") from the center electrode to each of the two electrodes on opposite ends, and the fourth output signal corresponds to a potential difference caused between the two electrodes on both sides of the center electrode by the drive current flowing in a direction (referred to as "fourth direction") opposite to the third direction.

[0006] In the conventional vertical Hall element as described in WO 03/036733, the temperature inside the vertical Hall element is not uniform and a temperature distribution occurs in the vertical Hall element, then a thermoelectric current constantly flows from a high-temperature portion to a low-temperature portion in the vertical Hall element. Such a state is made, for example, when a circuit for driving the vertical Hall element which includes an element acting as a heat source is provided around the vertical Hall element.

[0007] In the removal of the offset voltage through use of the spinning current method in the above-mentioned state, the current flows differently in the first to fourth directions due to the influence of the thermoelectric current, with the result that the offset voltage cannot be removed with sufficiently high accuracy.

SUMMARY OF THE INVENTION

[0008] In view of the above, it is an object of the present invention to provide a semiconductor device including a circuit having a heat source, and including a vertical Hall element in which an offset voltage can be removed with high accuracy through use of a spinning current method.

[0009] According to at least one embodiment of the present invention, a semiconductor device includes: a first vertical Hall element provided in a first region of a semiconductor substrate, and having a first electrode, a second electrode, and a third electrode that are arranged side by side in order along a first straight line; a first circuit provided in a second region of the semiconductor substrate different from the first region, and having a heat source; and a second straight line intersecting orthogonally a first current path for a Hall element drive current which flows between the first electrode and the third electrode, the second straight line passing a center of the first vertical Hall element, wherein a center point of a region that reaches the highest temperature in the first circuit during an operation of the first vertical Hall element lies on the second straight line.

[0010] According to at least one embodiment of the present invention, heat generated from the heat source is transferred symmetrically in plan view with respect to the second straight line passing the center of the vertical Hall element, into the vertical Hall element from a portion at which the second straight line crosses an end portion of the vertical Hall element on the heat source side. Even though the vertical Hall element has a temperature distribution due to the influence of the heat generated from the heat source, upon switching the direction of the current flowing through the current path in accordance with the spinning current method, manner of flowing of the

currents becomes substantially the same in every direction, and thus the offset voltage can be removed with high accuracy.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Embodiments of the invention will now be described by way of example only with reference to the accompanying drawings, in which:

FIG. 1 is a plan view of a semiconductor device according to a first embodiment of the present invention.
FIG. 2 is a sectional view taken along the line A1-A1 of FIG. 1.
FIG. 3 is a plan view of a semiconductor device according to a second embodiment of the present invention.
FIG. 4 is a plan view of a semiconductor device according to a third embodiment of the present invention.
FIG. 5 is a plan view of a semiconductor device according to a fourth embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0012] In the following, embodiments of the present invention are described in detail with reference to the drawings.

[First Embodiment]

[0013] FIG. 1 is a plan view of a semiconductor device 10 including a vertical Hall element and a heat source according to the first embodiment of the present invention. FIG. 2 is a sectional view taken along the line A1-A1 of FIG. 1. The line A1-A1 is supposed to equally divide the vertical Hall element 110 along the longitudinal direction.

[0014] As illustrated in FIG. 1, the semiconductor device 10 of the first embodiment includes a vertical Hall element 110 provided in a region R1 of a semiconductor substrate 101 (see FIG. 2), and a circuit 210 having a heat source which is provided in a region R2 different from the region R1.

[0015] As illustrated in FIG. 2, the vertical Hall element 110 includes an N-type (second conductivity type) semiconductor layer 102 formed as a magnetic sensing portion on the P-type (first conductivity type) semiconductor substrate 101, and electrodes 111 to 115 formed from N-type impurity regions and arranged in the surface of the semiconductor layer 102 as electrodes for supplying a drive current and for producing a Hall voltage. As illustrated in FIG. 1, the electrodes 111 to 115 are arranged side by side in order along the straight line A1-A1.

[0016] As illustrated in FIG. 2, a P-type element isolation diffusion layer 103 is formed around the vertical Hall element 110 so as to surround the vertical Hall element 110. The vertical Hall element 110 and the circuit 210 having the heat source are electrically isolated from each other by the element isolation diffusion layer 103.

[0017] The circuit 210 having the heat source is, for example, a circuit for driving the vertical Hall element 110 or a circuit for processing an output signal from the vertical Hall element 110. Such circuit has a transistor or the like acting as a heat source in many cases. Examples of the heat source include a resistive element through which large current flows and an output transistor of a voltage regulator which is used for obtaining an internal power supply voltage as a power supply voltage for driving the vertical Hall element 110, generated by stepping down an external power supply voltage through the voltage regulator, instead of using the external power supply voltage.

[0018] Next, a positional relationship between the vertical Hall element 110 and the circuit 210 having the heat source is described.

[0019] In the vertical Hall element 110 of FIG. 1, removal of an offset voltage through use of the spinning current method requires flow of the drive current in four directions, that is, a direction (first direction) from the electrode 112 to the electrode 114, a direction (second direction) from the electrode 114 to the electrode 112, a direction (third direction) from the electrode 113 to each of the electrode 111 and the electrode 115, and a direction (fourth direction) from each of the electrode 111 and the electrode 115 to the electrode 113. In FIG. 1, a current path CP1 for a Hall element drive current flowing between the electrode 112 and the electrode 114, a current path CP2 for a Hall element drive current flowing between the electrode 113 and the electrode 111, and a current path CP3 for a Hall element drive current flowing between the electrode 113 and the electrode 115 are illustrated. Specifically, the current path CP1 corresponds to a path for the drive current in the first direction and the second direction, and the current paths CP2 and CP3 correspond to paths for the drive current in the third direction and the fourth direction.

[0020] In the first embodiment, the vertical Hall element 110 and the circuit 210 having the heat source are arranged so that a center point 210h of a region 210hr that reaches the highest temperature in the circuit 210 during the operation of the vertical Hall element 110 (during execution of the spinning current method), lies on the straight line A2-A2 intersecting orthogonally the current path CP1 and passing the center of the vertical Hall element 110.

[0021] With this arrangement, heat generated from the heat source in the circuit 210 is transferred symmetrically in plan view with respect to the straight line A2-A2, into the vertical Hall element 110 from a portion IS1 at which the straight line A2-A2 crosses an end portion of the vertical Hall element 110 on the circuit 210 side. Even though the vertical Hall element 110 has a temperature distribution due to the influence of the heat generated from the heat source in the circuit 210, upon switching a direction

in which a current flows through the current path CP1 between the first direction and the second directions in accordance with the spinning current method, manner of flowing of the two currents hence becomes substantially the same in those two directions.

[0022] Upon switching the direction of the current supplied to flow through each of the current paths CP2 and CP3 between the third direction and the fourth direction as well, the current path CP2 and the current path CP3 are arranged symmetrically in plan view with respect to the straight line A2-A2, and hence the vertical Hall element 110 has a temperature distribution symmetric in plan view with respect to the straight line A2-A2, with the result that the current path CP2 and the current path CP3 exhibit substantially the same and symmetric temperature distribution. Manner of flowing of the two currents hence becomes substantially the same in the third direction and the fourth direction.

[0023] Consequently, according to the first embodiment, even though the heat generated from the heat source in the circuit 210 reaches the vertical Hall element 110 and the vertical Hall element 110 has a temperature distribution, the offset voltage can be removed with high accuracy through use of the spinning current method.

[0024] Here, the electrodes 111 to 115 of the vertical Hall element 110 preferably have substantially the same size and shape and are arranged at substantially equal intervals. With this configuration, the vertical Hall element 110 becomes line-symmetric with respect to its center line, that is, the straight line A2-A2, and manner of flowing of the currents becomes substantially the same in every direction in any of the current paths CP1, CP2, and CP3. This configuration allows highly accurate removal of the offset voltage through use of the spinning current method.

[Second Embodiment]

[0025] In the first embodiment described above, the number of circuits having a heat source is one, but the number of circuits having a heat source in the circuits provided around the vertical Hall element is not limited to one. In the second embodiment of the present invention, description is given of a case in which a plurality of circuits having a heat source are provided around a vertical Hall element. FIG. 3 is a plan view of a semiconductor device 20 including a vertical Hall element and circuits having a heat source according to the second embodiment of the present invention.

[0026] As illustrated in FIG. 3, the semiconductor device 20 of the second embodiment further includes a circuit 220 having a heat source which is provided in a region R3 different from the regions R1 and R2 in addition to the components of the semiconductor device 10 of the first embodiment. The same components as those of the semiconductor device 10 of the first embodiment as illustrated in FIG. 1 are denoted by the same reference symbols, and redundant description thereof is omitted as appropriate.

[0027] In the semiconductor device 20 of the second embodiment, the circuit 220 having the heat source is provided so that a center point 220h of a region 220hr that reaches the highest temperature in the circuit 220 during the operation of the vertical Hall element 110 (during execution of the spinning current method), lies on the straight line A2-A2.

[0028] With this arrangement, heat generated from the heat source in the circuit 220 is transferred symmetrically in plan view with respect to the straight line A2-A2, into the vertical Hall element 110 from a portion IS2 at which the straight line A2-A2 crosses an end portion of the vertical Hall element 110 on the circuit 220 side. Accordingly, even though the vertical Hall element 110 has a temperature distribution due to an influence of the heat generated from the heat source in the circuit 220 similarly to the heat generated from the heat source in the circuit 210, upon switching the direction in which the current flows through the current path CP1 between the first direction and the second direction in accordance with the spinning current method, manner of flowing of the currents becomes substantially the same in those two directions. Further, the temperature distributions along the current path CP2 and the current path CP3 are also symmetric and substantially the same. Manner of flowing of the currents thus becomes substantially the same in the third direction and the fourth direction.

[0029] Consequently, according to the second embodiment, even though the heat generated from the heat source in the circuit 210 and the heat generated from the heat source in the circuit 220 reach the vertical Hall element 110, and generate a temperature distribution in the vertical Hall element 110, the offset voltage can be removed with high accuracy through use of the spinning current method.

[0030] As described above, even though a plurality of circuits having a heat source are provided, the offset voltage can be removed with high accuracy through use of the spinning current method.

[0031] In the first and second embodiments description was made for the one vertical Hall element. In the following, as third and fourth embodiments of the present invention, description is given of a plurality of vertical Hall elements provided on the same semiconductor substrate.

[Third Embodiment]

[0032] In the third embodiment, description is given of two vertical Hall elements provided in parallel to each other on the same semiconductor substrate. FIG. 4 is a plan view of a semiconductor device 30 including vertical Hall elements and a heat source according to the third embodiment of the present invention.

[0033] As illustrated in FIG. 4, the semiconductor device 30 of the third embodiment further includes a vertical Hall element 120 provided in parallel to the vertical Hall

element 110, in the region R3 different from the regions R1 and R2, in addition to the components of the semiconductor device 10 of the first embodiment. The same components as those of the semiconductor device 10 of the first embodiment as illustrated in FIG. 1 are denoted by the same reference symbols, and redundant description thereof is omitted as appropriate.

[0034] The vertical Hall element 120 includes the N-type semiconductor layer 102 (see FIG. 2) formed as the magnetic sensing portion on the P-type semiconductor substrate 101, and electrodes 121 to 125 formed from N-type impurity regions in the surface of the semiconductor layer 102 as electrodes for supplying a drive current and for outputting a Hall voltage. As illustrated in FIG. 4, the electrodes 121 to 125 are arranged side by side in order along the straight line A3-A3. The line A3-A3 is supposed to equally divide the vertical Hall element 120 along the longitudinal direction.

[0035] The P-type element isolation diffusion layer 103 (see FIG. 2) is formed to surround the vertical Hall element 120, and the circuit 210 having the heat source, the vertical Hall element 110, and the vertical Hall element 120 are electrically and mutually isolated by the element isolation diffusion layer 103.

[0036] Next, a positional relationship among the circuit 210 having the heat source, the vertical Hall element 110, and the vertical Hall element 120 is described.

[0037] In the vertical Hall element 120 of FIG. 4, removal of the offset voltage through use of the spinning current method requires flow of the drive current in four directions, that is, a direction (first direction) from the electrode 122 to the electrode 124, a direction (second direction) from the electrode 124 to the electrode 122, a direction (third direction) from the electrode 123 to each of the electrode 121 and the electrode 125, and a direction (fourth direction) from each of the electrode 121 and the electrode 125 to the electrode 123. In FIG. 4, a current path CP4 for a Hall element drive current flowing between the electrode 122 and the electrode 124, a current path CP5 for a Hall element drive current flowing between the electrode 123 and the electrode 121, and a current path CP6 for a Hall element drive current flowing between the electrode 123 and the electrode 125 are illustrated. Specifically, the current path CP4 corresponds to a path for a drive current in the first direction and the second direction in the vertical Hall element 120, and the current paths CP5 and CP6 correspond to paths for a drive current in the third direction and the fourth direction in the vertical Hall element 120.

[0038] In the third embodiment, the vertical Hall element 120 is provided, in addition to the semiconductor device 10 of the first embodiment as illustrated in FIG. 1 in which the vertical Hall element 110 and the circuit 210, having the heat source are arranged so that the straight line intersecting orthogonally the current path CP4 in the vertical Hall element 120 and passing the center of the vertical Hall element 120 coincides with the straight line A2-A2. As in semiconductor device 10 of the first embodiment, the center point 210h of the region 210hr that reaches the highest temperature in the circuit 210 during the operation of the vertical Hall element 110 (during execution of the spinning current method), lies on the straight line A2-A2 intersecting orthogonally the current path CP1 in the vertical Hall element 110 and passing the center of the vertical Hall element 110.

[0039] With this arrangement, during the operation of the vertical Hall element 120 (during execution of the spinning current method), heat generated from the heat source in the circuit 210 is transferred symmetrically in plan view with respect to the straight line A2-A2, into the vertical Hall element 120 from the portion IS2 at which the straight line A2-A2 crosses an end portion of the vertical Hall element 120 on the circuit 210 side. Even though the vertical Hall element 120 has a temperature distribution due to the influence of the heat generated from the heat source in the circuit 210, upon switching a direction in which a current flows through the current path CP4 between the first direction and the second direction in accordance with the spinning current method, manner of flowing of the two currents hence becomes substantially the same in those two directions. Further, the current path CP5 and the current path CP6 also exhibit substantially the same and symmetric temperature distribution. Manner of flowing of the two currents hence becomes substantially the same in the third direction and the fourth direction.

[0040] Consequently, according to the third embodiment, even though the heat generated from the heat source in the circuit 210 reaches the vertical Hall element 120 and the vertical Hall element 120 has a temperature distribution, the offset voltage can be removed with high accuracy through use of the spinning current method.

[0041] As described above, even though a plurality of vertical Hall elements is provided in parallel mutually on the same semiconductor substrate, the offset voltage can be removed with high accuracy through use of the spinning current method.

[Fourth Embodiment]

[0042] In the fourth embodiment, description is given of a case in which two vertical Hall elements are arranged perpendicular to each other on the same semiconductor substrate. FIG. 5 is a plan view of a semiconductor device 40 including vertical Hall elements and a heat source according to the fourth embodiment of the present invention.

[0043] As illustrated in FIG. 5, the semiconductor device 40 of the fourth embodiment further includes the vertical Hall element 120 provided perpendicular to the vertical Hall element 110, in the region R3 different from the regions R1 and R2, in addition to the components of the semiconductor device 10 of the first embodiment. The same components as those of the semiconductor device 10 of the first embodiment as illustrated in FIG. 1 are denoted by the same reference symbols, and redundant

description thereof is omitted as appropriate.

[0044] The vertical Hall element 120 includes the N-type semiconductor layer 102 (see FIG. 2) formed as the magnetic sensing portion on the P-type semiconductor substrate 101, and the electrodes 121 to 125 formed from N-type impurity regions in the surface of the semiconductor layer 102 as electrodes for supplying a drive current and for outputting a Hall voltage. As illustrated in FIG. 5, the electrodes 121 to 125 are arranged side by side in order along the straight line A3-A3 orthogonal to the straight line A1-A1. The line A3-A3 is supposed to equally divide the vertical Hall element 120 along the lateral direction.

[0045] The P-type element isolation diffusion layer 103 (see FIG. 2) is formed to surround the vertical Hall element 120, and the circuit 210 having the heat source, the vertical Hall element 110, and the vertical Hall element 120 are electrically and mutually isolated by the element isolation diffusion layer 103.

[0046] Next, a positional relationship among the circuit 210 having the heat source, the vertical Hall element 110, and the vertical Hall element 120 is described.

[0047] In the vertical Hall element 120 of FIG. 5, removal of the offset voltage through use of the spinning current method requires flow of the drive current in four directions, that is, a direction (first direction) from the electrode 122 to the electrode 124, a direction (second direction) from the electrode 124 to the electrode 122, a direction (third direction) from the electrode 123 to each of the electrode 121 and the electrode 125, and a direction (fourth direction) from each of the electrode 121 and the electrode 125 to the electrode 123. In FIG. 5, the current path CP4 for a Hall element drive current flowing between the electrode 122 and the electrode 124, the current path CP5 for a Hall element drive current flowing between the electrode 123 the electrode 121, and the current path CP6 for a Hall element drive current flowing between the electrode 123 and the electrode 125 are illustrated. Specifically, the current path CP4 corresponds to a path for a drive current in the first direction and the second direction in the vertical Hall element 120, and the current paths CP5 and CP6 correspond to paths for a drive current in the third direction and the fourth direction in the vertical Hall element 120.

[0048] In the fourth embodiment, the vertical Hall element 120 is provided, in addition to the semiconductor device 10 of the first embodiment as illustrated in FIG. 1 in which the vertical Hall element 110 and the circuit 210 having the heat source are arranged so that the center point 210h of the region 210hr lies on the straight line A4-A4 intersecting orthogonally the current path CP4 in the vertical Hall element 120 and passing the center of the vertical Hall element 120. As in the semiconductor device 10 of the first embodiment, the center point 210h of the region 210hr that reaches the highest temperature in the circuit 210 during the operation of the vertical Hall element 110 (during execution of the spinning current method), lies on the straight line A2-A2 intersecting orthogonally the current path CP1 in the vertical Hall element 110 and passing the center of the vertical Hall element 110.

[0049] With this arrangement, during the operation of the vertical Hall element 120 (during execution of the spinning current method), heat generated from the heat source in the circuit 210 is transferred symmetrically in plan view with respect to the straight line A4-A4, into the vertical Hall element 120 from the portion IS2 in the vertical Hall element 120 at which the straight line A4-A4 crosses an end portion of the vertical Hall element 120 on the circuit 210 side. Even though the vertical Hall element 120 has a temperature distribution due to the influence of the heat generated from the heat source in the circuit 210, upon switching a direction in which a current flows through the current path CP4 between the first direction and the second direction in accordance with the spinning current method, manner of flowing of the two currents hence becomes substantially the same in those two directions. Further, the current path CP5 and the current path CP6 also exhibit substantially the same and symmetric temperature distribution. Manner of flowing of the two currents hence becomes substantially the same in the third direction and the fourth direction.

[0050] Consequently, according to the fourth embodiment, even though the heat generated from the heat source in the circuit 210 reaches the vertical Hall element 120, and the vertical Hall element 120 has a temperature distribution, the offset voltage can be removed with high accuracy through use of the spinning current method.

[0051] As described above, even though the two vertical Hall elements are arranged perpendicular to each other on the same semiconductor substrate, the offset voltage can be removed in each vertical Hall element with high accuracy through use of the spinning current method.

[0052] As described above, according to the embodiments of the present invention, even if any circuit having a heat source is provided around the vertical Hall element, it is possible to substantially eliminate an influence of heat generated from the heat source during execution of the spinning current method in the vertical Hall element. This eliminates the need to, for example, provide the circuit having the heat source away from the vertical Hall element, and thus enables reduction in circuit size.

[0053] The embodiments of the present invention have been described above, but the present invention is not limited to the above-mentioned embodiments, and it is to be understood that various modifications can be made thereto without departing from the scope of the present invention.

[0054] For example, in the example described in the above-mentioned embodiments, the vertical Hall element includes five electrodes. However, three or more electrodes in total, specifically, two electrodes for drive current supply and one electrode for Hall voltage output, suffice for the purpose.

[0055] Further, in the example described in the above-

mentioned embodiments, the first conductivity type is the P type, and the second conductivity type is the N type. However, the opposite case is allowed, that is, the first conductivity type is the N type and the second conductivity type is the P type.

[0056] The electrodes 121 to 125 of the vertical Hall element 120 in the third and fourth embodiments preferably have substantially the same size and shape and are arranged at substantially equal intervals. With this configuration, the vertical Hall element 120 becomes line-symmetric with respect to its center line, that is, the straight line A3-A3, and manner of flowing of the currents becomes substantially the same in every direction in any of the current paths CP4, CP5, and CP6. This configuration allows highly accurate removal of the offset voltage through use of the spinning current method.

The invention being thus described, it will be obvious that it may be varied in many ways. Such variations are not to be regarded as a departure from the scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A semiconductor device (10), comprising:

a first vertical Hall element (110) provided in a first region (R1) of a semiconductor substrate, and having a first electrode (112), a second electrode (113), and a third electrode (114) which are arranged side by side in order along a first straight line (A1-A1);
a first circuit (210) provided in a second region (R2) of the semiconductor substrate different from the first region, and having a heat source; and
a second straight line (A2-A2) intersecting orthogonally a first current path (CP1) for a Hall element drive current which flows between the first electrode (112) and the third electrode (114), the second straight line passing a center of the first vertical Hall element,
wherein a center point (210h) of a region (210hr) which reaches the highest temperature in the first circuit during an operation of the first vertical Hall element lies on the second straight line.

2. The semiconductor device (20) according to claim 1, further comprising a second circuit (220) provided in a third region (R3) of the semiconductor substrate different from the first region and the second region, and having a heat source,
wherein a center point (220h) of a region (220hr) which reaches the highest temperature in the second circuit during the operation of the first vertical Hall element lies on the second straight line (A2-A2).

3. The semiconductor device (30) according to claim 1 or claim 2, further comprising a second vertical Hall element (120) provided in a third region (R3) of the semiconductor substrate different from the first region and the second region, and having a fourth electrode (122), a fifth electrode (123), and a sixth electrode (124) which are arranged side by side in order along a third straight line (A3-A3),
wherein a straight line intersecting orthogonally a second current path (CP4) for a Hall element drive current which flows between the fourth electrode (122) and the sixth electrode (124), and passing a center of the second vertical Hall element, coincides with the second straight line (A2-A2).

4. The semiconductor device (40) according to any one of the preceding claims, further comprising:

a second or further vertical Hall element (120) provided in a third region of (R3) the semiconductor substrate different from the first region and the second region, and having a fourth electrode (122), a fifth electrode (123), and a sixth electrode (124) which are arranged side by side in order along a third straight line (A3-A3) orthogonal to the first straight line (A1-A1); and
a fourth straight line (A4-A4) intersecting orthogonally a second current path (CP4) as a path for a Hall element drive current which flows between the fourth electrode (122) and the sixth electrode (124), and passing a center of the second vertical Hall element, and
wherein the center point (210h) of the region (210hr) that reaches the highest temperature in the first circuit during the operation of the first vertical Hall element lies on the fourth straight line.

5. The semiconductor device according to any one of the preceding claims, wherein the first vertical Hall element (110) further includes a seventh electrode (111) and an eighth electrode (115) provided side by side with respect to the first electrode, the second electrode, and the third electrode along the first straight line so as to sandwich the first electrode, the second electrode, and the third electrode.

6. The semiconductor device according to any one of the preceding claims, wherein the first vertical Hall element is line-symmetric with respect to the second straight line.

7. The semiconductor device according to any one of claims 3 to 6, wherein the second or further vertical Hall element further comprises a ninth electrode (121) and a tenth electrode (125) provided side by side with respect to the fourth electrode, the fifth electrode, and the sixth electrode along the third straight

line (A3-A3) so as to sandwich the fourth electrode, the fifth electrode, and the sixth electrode.

8. The semiconductor device according to any one of claims 3 to 7, wherein the second or further vertical Hall element is line-symmetric with respect to the second straight line.

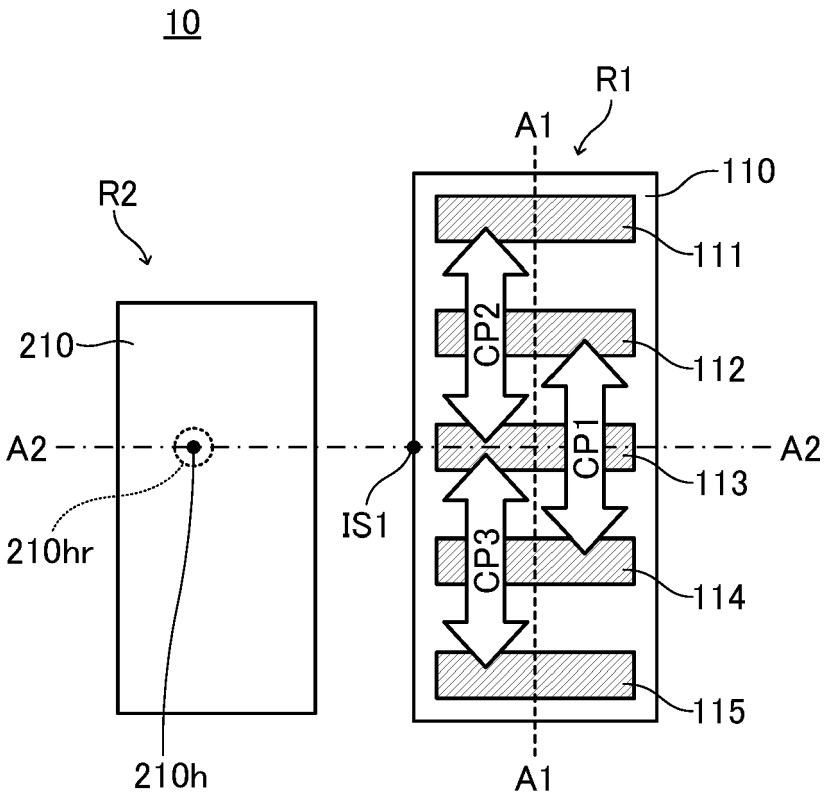
10
R1
A1
110
R2
111
210
CP2
112
A2
CP1
A2
113
IS1
210hr
CP3
114
115
210h
A1

FIG. 1

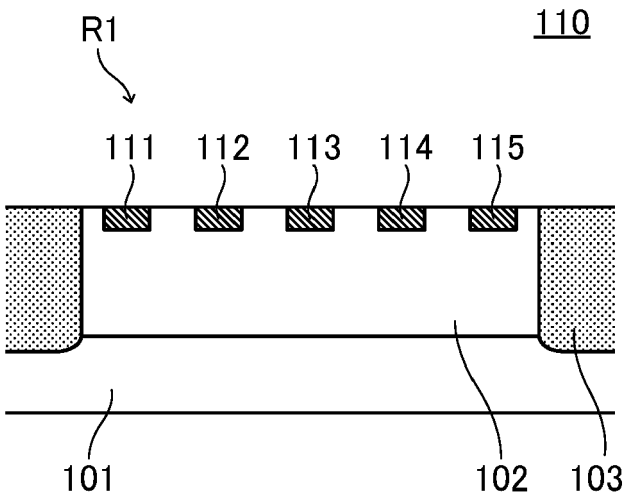

FIG. 2

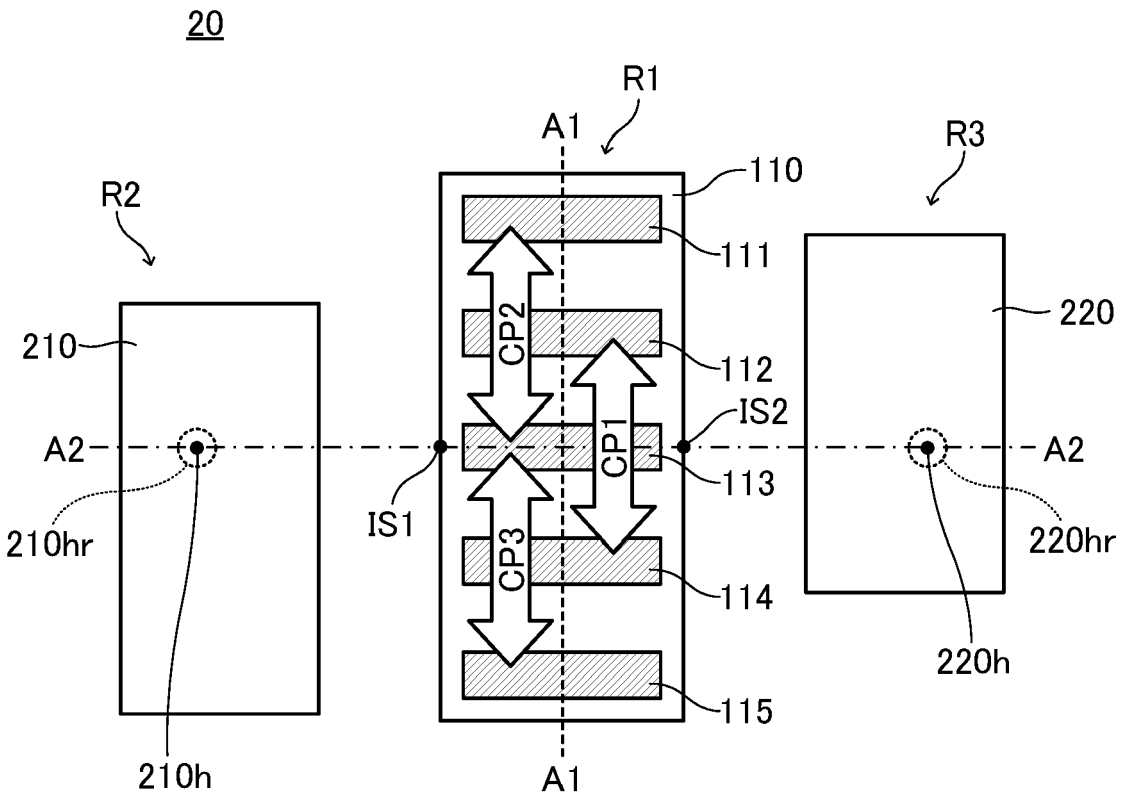
20
R1
A1
R3
110
R2
111
220
210
CP2
112
IS2
A2
CP1
113
A2
IS1
220hr
210hr
CP3
114
220h
115
210h
A1

FIG. 3

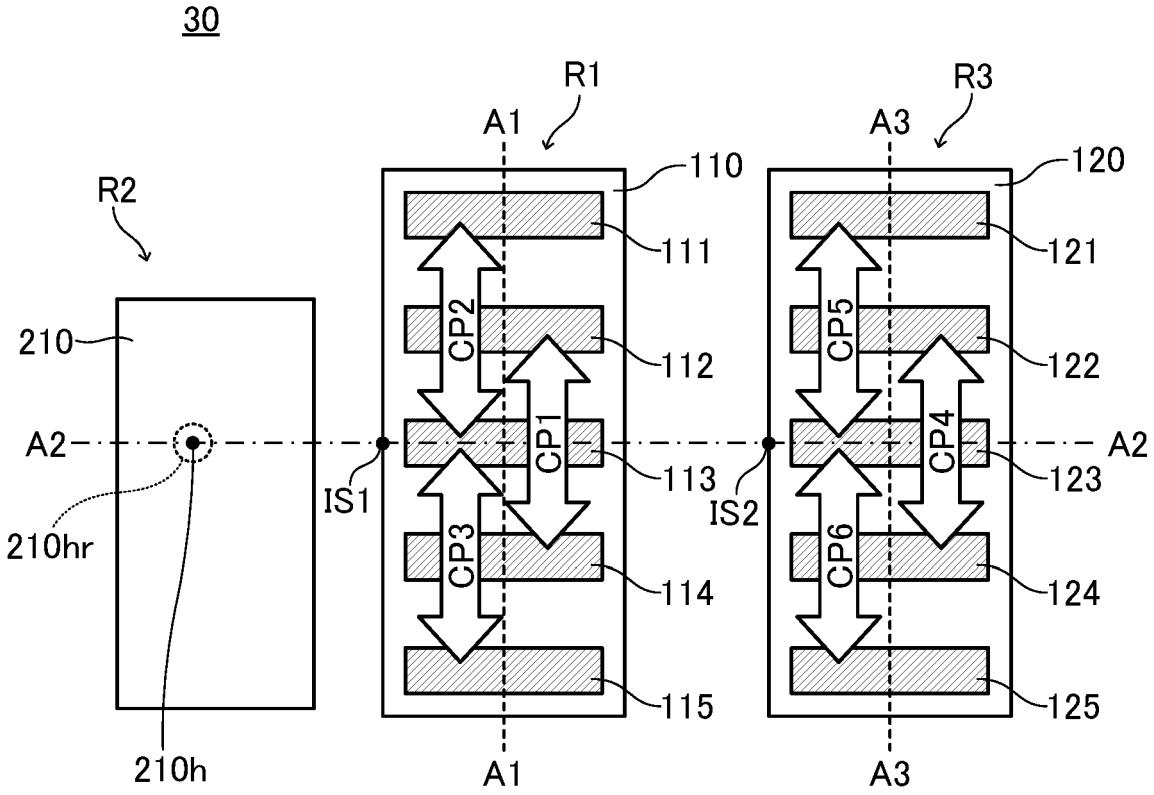
30
R1
A1
R3
A3
110
120
R2
111
121
210
CP2
CP5
112
122
A2
CP1
CP4
A2
113
123
IS1
IS2
210hr
CP3
CP6
114
124
115
125
210h
A1
A3

FIG. 4

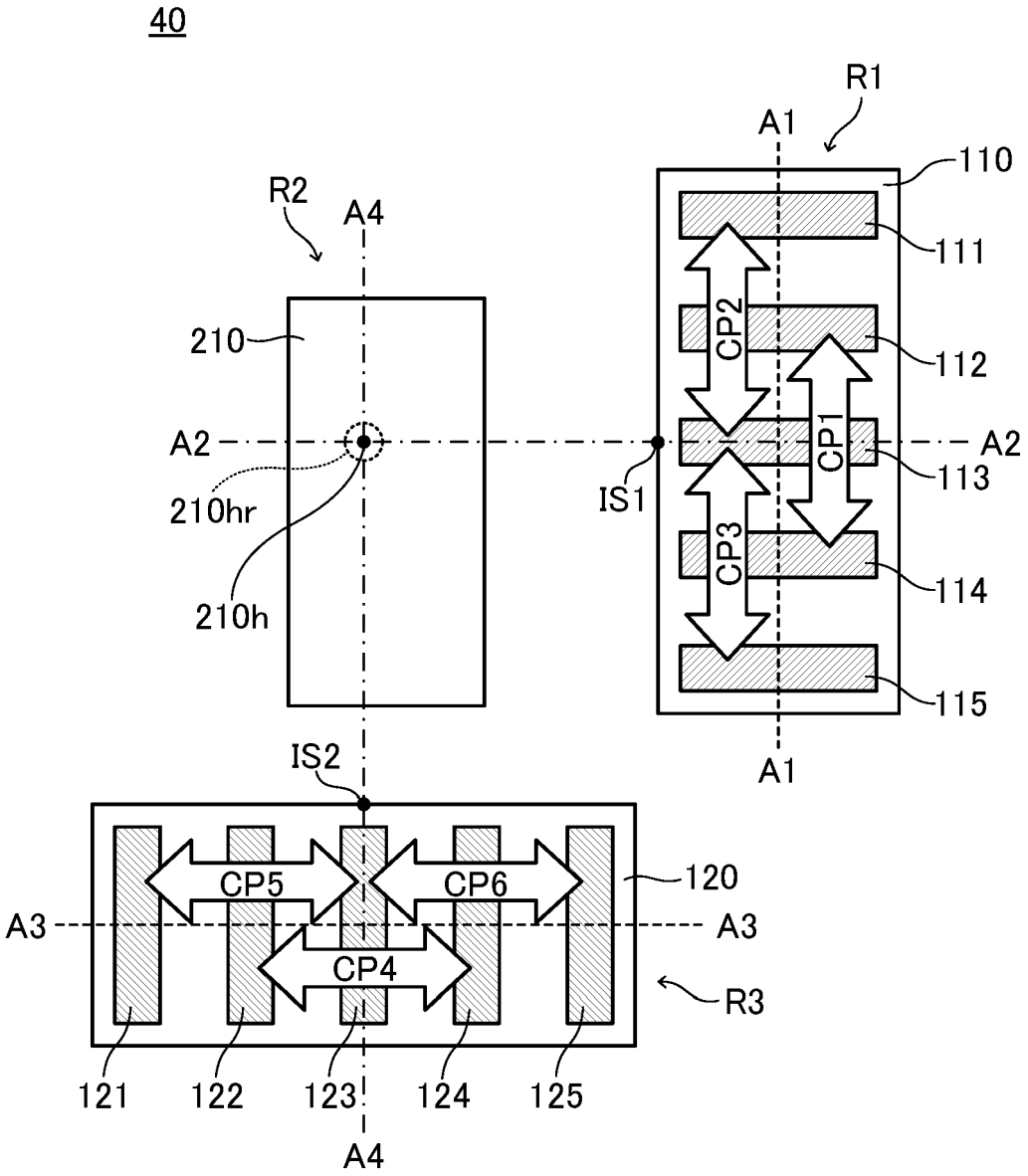
40
R1
A1
110
111
112
113
114
115
CP1
CP2
CP3
A2
IS1
R2
A4
210
210hr
210h
IS2
CP4
CP5
CP6
120
A3
R3
121
122
123
124
125

FIG. 5

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EUROPEAN SEARCH REPORT

Application Number
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	15 June 2020	Philipp, Peter

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