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(54) **DEVICE AND METHOD OF HANDLING A TIME DE-INTERLEAVER BLOCK**

(57) A time de-interleaver (TDI) comprises at least one buffer; a double data rate (DDR) storage device; a buffer writing circuit, coupled to the at least one buffer, for writing a plurality of data cells in a TDI block to the at least one buffer; a control circuit, coupled to the buffer writing circuit, for generating a plurality of DDR addresses

of the plurality of data cells according to a plurality of TDI addresses of the plurality of data cells; and a DDR writing circuit, coupled to the control circuit and the DDR storage device, for writing the plurality of data cells in the at least one buffer to the DDR storage device according to the plurality of DDR addresses.

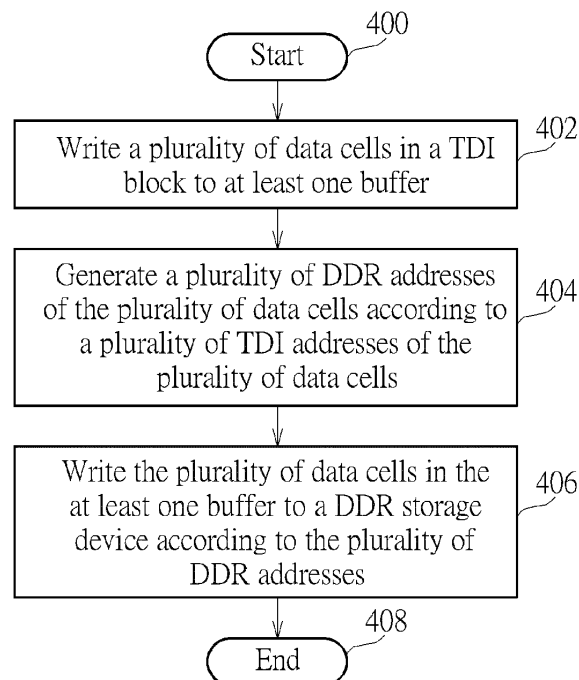


FIG. 4

Description

Field of the Invention

5 **[0001]** The present invention relates to a communication device and a method of handling a time de-interleaver block in a wireless communication system.

Background of the Invention

10 **[0002]** In a wireless communication system, a receiver (e.g., a user equipment (UE)) may obtain information in a time de-interleaver (TDI) block by using a double data rate (DDR) reading/writing (R/W) with the TDI. However, when using the TDI R/W, the TDI repeatedly reads information. The receiver unnecessarily consumes in a large amount of resources. Thus, how to reduce the resource consumption is an important problem to be solved.

Summary of the Invention

[0003] The present invention therefore provides a method and related communication device for handling a time de-interleaver (TDI) block to solve the abovementioned problem.

20 **[0004]** This is achieved by a TDI for handling a TDI block according to the independent claims here below. The dependent claims pertain to corresponding further developments and improvements.

[0005] As will be seen more clearly from the detailed description following below, a claimed TDI comprises at least one buffer; a double data rate (DDR) storage device; a buffer writing circuit, coupled to the at least one buffer, for writing a plurality of data cells in a TDI block to the at least one buffer; a control circuit, coupled to the buffer writing circuit, for generating a plurality of DDR addresses of the plurality of data cells according to a plurality of TDI addresses of the plurality of data cells; and a DDR writing circuit, coupled to the control circuit and the DDR storage device, for writing the plurality of data cells in the at least one buffer to the DDR storage device according to the plurality of DDR addresses.

Brief Description of the Drawings

30 **[0006]**

Fig. 1 is a schematic diagram of a communication system according to an example of the present invention.

Fig. 2 is a schematic diagram of a time de-interleaver according to an example of the present invention.

35 Fig. 3 is a schematic diagram of a time de-interleaver block and a double data rate storage device according to an example of the present invention.

Fig. 4 is a flowchart of a process according to an example of the present invention.

Fig. 5 is a schematic diagram of a time de-interleaver according to an example of the present invention.

Fig. 6 is a flowchart of a process according to an example of the present invention.

Detailed Description

40 **[0007]** Fig. 1 is a schematic diagram of a communication system 10 according to an example of the present invention. The communication system 10 may be any communication system using an orthogonal frequency-division multiplexing (OFDM) technique (or termed as discrete multi-tone modulation (DMT) technique), and is briefly composed of a transmitter TX and a receiver RX. In Fig. 1, the transmitter TX and the receiver RX are simply utilized for illustrating the structure of the communication system 10. For example, the communication system 10 may be any wired communication system such as an asymmetric digital subscriber line (ADSL) system, a power line communication (PLC) system or an Ethernet over coax (EOC), or may be any wireless communication system such as a wireless local area network (WLAN), a Digital Video Broadcasting (DVB) system, a Long Term Evolution (LTE) system, a Long Term Evolution-advanced (LTE-A) system or a fifth generation (5G) system. In addition, the transmitter TX and the receiver RX may be installed in a mobile phone, a laptop, etc., but is not limited herein.

50 **[0008]** Fig. 2 is a schematic diagram of a time de-interleaver (TDI) 20 according to an example of the present invention. The TDI 20 may be utilized in the receiver RX of Fig. 1, for handling a TDI block transmitted by the transmitter TX. The TDI 20 includes at least one buffer 200, a double data rate (DDR) storage device 202, a buffer writing circuit 204, a control circuit 206 and a DDR writing circuit 208. In detail, the buffer writing circuit 204 is coupled to the at least one buffer 200, and writes (e.g., stores) data cells in the TDI block to the at least one buffer 200. The control circuit 206 is coupled to the buffer writing circuit 204, and generates DDR addresses of the data cells according to TDI addresses of the data cells. The DDR writing circuit 208 is coupled to the control circuit 206 and the DDR storage device 202, and

writes (e.g., stores) the data cells in the at least one buffer 200 to the DDR storage device 202 according to DDR addresses.

[0009] Fig. 3 is a schematic diagram of a TDI block 300 and a DDR storage device 302 according to an example of the present invention. The DDR storage device 302 may be utilized for realizing the DDR storage device 202 of Fig. 2. The TDI block 300 has N_r rows and N_c columns. There are $N_r \times N_c$ data cells in the TDI block 300, and each data cell has a cell number. In Fig. 3, there are 16384 data cells in the TDI block 300 with $N_r=16$ and $N_c=1024$, but is not limited herein.

[0010] In the prior art, the DDR writing circuit 208 writes the data cells in the TDI block 300 to the DDR storage device 202 sequentially. For example, the TDI 20 writes data cells in a first row of the TDI block 300 to the DDR storage device 202, and then writes data cells in a second row of the TDI block 300 to the DDR storage device 202, and so on. According to the prior art, writing data cells in a TDI block to a DDR storage device sequentially causes the resource consumption when reading the data cells in the DDR storage device. The detail may be mentioned later.

[0011] In the present invention, the buffer writing circuit 204 writes the data cells in the TDI block 300 to the at least one buffer 200 in a more efficient way. An example is illustrated according to Figs 2 and 3 as follows. There are 16 buffers with buffer indices 0-15 in the TDI 20. A data cell with a cell number 0 is written to a buffer with a buffer index 0 (i.e., $0 \bmod 16 = 0$). A data cell with a cell number 18 is written to a buffer with a buffer index 2 (i.e., $18 \bmod 16 = 2$). When the at least one buffer 200 (e.g., the 16 buffers) is full, the DDR writing circuit 208 writes the data cells in the at least one buffer 200 to the DDR storage device 302.

[0012] In one example, the control circuit 206 generates the DDR addresses according to the TDI addresses. A TDI address (R, C) represents that a data cell is located in the R-th row and the C-th column of the TDI block 300, wherein R and C are positive integers. In one example, the control circuit 206 generates the DDR addresses according to the following equation:

$$DDR\ address = N_c \times (R - 1) + \left\lfloor \frac{C}{(N_b \times BUF)} \right\rfloor \times (N_b \times BUF) + (C \bmod N_b) \times N_b \times \frac{BUF}{8} + \left(\left\lfloor \frac{C}{N_b} \right\rfloor \bmod (N_b \times BUF) \right), \quad (Eq. 1)$$

wherein N_c is the number of columns of the TDI block, (R, C) is one of the TDI addresses, N_b is the number of the at least one buffer 200, and BUF is a parameter. BUF is related to a ratio of a capacity of a DDR reading/writing (R/W) and a size of a data cell. Thus, the DDR writing circuit 208 may write the data cells in the at least one buffer 200 to the DDR storage device 302 according to the DDR addresses.

[0013] The following example is used for illustrating how the TDI 20 handles the TDI block 300. The TDI block 300 with $N_r=16$ and $N_c=1024$ and the at least one buffer 200 with $N_b=16$ are assumed. A size of a data cell is 32 bits, and the capacity of the DDR R/W is 256 bits. That is, BUF is $256/32=8$. First, the buffer writing circuit 204 writes the data cells to the at least one buffer 200, which can be referred to the previous description and is not narrated herein. After the buffer writing circuit 204 writes the data cells to the at least one buffer 200 (e.g., the 16 buffers), the DDR addresses of the data cells can be obtained according to the equation (Eq. 1). Setting $N_b=16$, $N_c=1024$ and $BUF=8$, the Equation (Eq. 1) can be rewritten as follows:

$$DDR\ address = 1024 \times (R - 1) + \left\lfloor \frac{C}{(16 \times 8)} \right\rfloor \times (16 \times 8) + (C \bmod 16) \times 16 + \left\lfloor \frac{C}{16} \right\rfloor. \quad (Eq. 2)$$

[0014] Thus, the data cells are written from the at least one buffer 200 to the DDR storage device 302 according to (Eq. 2). For example, a data cell with a TDI address (1, 8) is written to the DDR storage device 302 with a DDR address 128. A data cell with a TDI address (1, 24) is written to the DDR storage device 302 with a DDR address 129. The detail can be referred to the DDR storage device 302 in Fig. 3.

[0015] Operations of the TDI 20 in the above examples can be summarized into a process 40 shown in Fig. 4. The process 40 is utilized in the TDI 20, and includes the following steps:

Step 400: Start.

Step 402: Write a plurality of data cells in a TDI block to at least one buffer.

(continued)

- Step 404: Generate a plurality of DDR addresses of the plurality of data cells according to a plurality of TDI addresses of the plurality of data cells.
- 5 Step 406: Write the plurality of data cells in the at least one buffer to a DDR storage device according to the plurality of DDR addresses.
- Step 408: End.

10 **[0016]** The process 40 is used for illustrating the operations of the TDI 20. Detailed description and variations of the process 40 can be referred to the previous description, and is not narrated herein.

[0017] Fig. 5 is a schematic diagram of a time de-interleaver (TDI) 50 according to an example of the present invention. The TDI 50 may be utilized in the receiver RX of Fig. 1, for handling data cells in a DDR storage device. The TDI 50 includes a DDR storage device 500, a cache 502, a DDR reading circuit 504 and a cache writing circuit 506. In detail, the DDR reading circuit 504 is coupled to the DDR storage device 500, and reads a first part of the data cells in the DDR storage device 500. The cache writing circuit 506 is coupled to the DDR reading circuit 504 and the cache 502, and writes (e.g., stores) the first part of the data cells in the DDR storage device 500 to the cache 502. Thus, the receiver RX may obtain the first part of the data cells from the cache 502 instead of the DDR storage device 500, and may process the first part of the data cells.

20 **[0018]** In one example, the DDR reading circuit 504 reads a second part of the data cells in the DDR storage device 500, e.g., when the first part of the data cells in the cache 502 is not needed for the receiver RX. The cache writing circuit 506 writes (e.g., stores) the second part of the data cells in the DDR storage device 500 to the cache 502. The receiver RX may obtain the second part of the data cells from the cache 502, and may process the second part of the data cells.

25 **[0019]** In one example, the DDR reading circuit 504 reads the first part of the data cells in the DDR storage device 500 by using a DDR R/W. In one example, after the receiver RX obtains (or processes) the first part of the data cells (e.g., the first part of the data cells in the cache 502 is no longer needed for the receiver RX), the DDR reading circuit 504 reads the second part of the data cells in the DDR storage device 500 by using the DDR R/W. Similarly, after the receiver RX obtains (or processes) the second part of the data cells (e.g., the second part of the data cells in the cache 502 is no longer needed for the receiver RX), the DDR reading circuit 504 reads a third part of the data cells in the DDR storage device 500 by using the DDR R/W.

30 **[0020]** In one example, the first part of the data cells and the second part of the data cells are not overlapped in the DDR storage device 500. Similarly, the second part of the data cells and the third part of the data cells are not overlapped in the DDR storage device 500. In one example, a capacity of the cache 502 is not smaller than the capacity of the DDR R/W. That is, the minimum capacity of the cache 502 is equal to the capacity of the DDR R/W.

35 **[0021]** The following example is used for illustrating how the TDI 50 handles the data cells in the DDR storage device 500. A data cell with a size of 32 bits and the DDR R/W with a capacity of 256 bits are assumed. That is, the TDI 50 reads 8 data cells at a time by using the DDR R/W. The minimum capacity of the cache 502 is 256 bits. First, the DDR reading circuit 504 reads 8 data cells of the data cells in the DDR storage device 500 (e.g., the DDR storage device 302 with DDR addresses 128-135) by using the DDR R/W, and the cache writing circuit 506 writes the 8 data cells to the cache 502. That is, the receiver RX may obtain the 8 data cells from the cache 502, and may process the 8 data cells. 40 After the receiver RX processes the 8 data cells, the DDR reading circuit 504 reads other 8 data cells of the data cells in the DDR storage device 500 (e.g., the DDR storage device 302 with DDR addresses 136-143) by using the DDR R/W, and the cache writing circuit 506 writes the other 8 data cells to the cache 502. Thus, the DDR reading circuit 504 needs to read 2048 (i.e., $16 \times 1024 / 8$) times to read all the data cells in the DDR storage device 500.

45 **[0022]** In the prior art, the DDR reading circuit 504 reads the data cells in the DDR storage device 500 according to an order of the cell numbers. For example, the DDR reading circuit 504 first reads a data cell with a cell number 0 (i.e., the data cell with a TDI address (1, 1) in the TDI block 300) by reading 8 data cells with TDI addresses (1, 1), (1, 2), ..., (1, 8). The data cell with the TDI address (1, 1) is useful for the receiver RX, while the other 7 data cells are useless. That is, the receiver RX uses only one cell read by the DDR reading circuit 504. Then, the DDR reading circuit 504 reads a data cell with a cell number 1 (i.e., the data cell with a TDI address (2,2) in the TDI block 300) by reading 8 data cells with TDI addresses (2, 1), (2, 2), ..., (2, 8). Similarly, the data cell with the TDI address (2, 2) is useful for the receiver RX, while the other 7 data cells are useless. Accordingly, in the prior art, the DDR reading circuit 504 needs to read 16384 (i.e., 16×1024) times to read all the data cells in the DDR storage device 500. According to the present invention, the resource consumption (e.g., the number of TDI reading) is reduced.

55 **[0023]** Operations of the TDI 50 in the above examples can be summarized into a process 60 shown in Fig. 6. The process 60 is utilized in the TDI 50, and includes the following steps:

- Step 600: Start.

(continued)

- Step 602: Read a first part of a plurality of data cells in a DDR storage device.
 Step 604: Write the first part of the plurality of data cells in the DDR storage device to a cache.
 Step 606: End.

[0024] The process 60 is used for illustrating the operations of the TDI 50. Detailed description and variations of the process 60 can be referred to the previous description, and is not narrated herein.

[0025] It should be noted that realizations of the TDI 20 (including the at least one buffer 200, the DDR storage device 202, the buffer writing circuit 204, the control circuit 206 and the DDR writing circuit 208) and the TDI 50 (including the DDR storage device 500, the cache 502, the DDR reading circuit 504 and the cache writing circuit 506) are various. For example, the circuits mentioned above may be integrated into one or more circuits. In addition, the TDI 20 and the TDI 50 may be realized by hardware (e.g., circuit), software, firmware (known as a combination of a hardware device, computer instructions and data that reside as read-only software on the hardware device), an electronic system or a combination of the devices mentioned above, but is not limited herein.

[0026] To sum up, the present invention provides a device and a method for handling a TDI block. According to the present invention, a TDI generates DDR addresses, and writes data cells in a TDI block to a DDR storage device according to the DDR addresses, to reduce the resource consumption. Thus, better efficiency is achieved.

Claims

1. A time de-interleaver (TDI) (20), **characterized by** the TDI (20) comprising:

at least one buffer (200);
 a double data rate (DDR) storage device (202);
 a buffer writing circuit (204), coupled to the at least one buffer (200), for writing a plurality of data cells in a TDI block to the at least one buffer (200) (402);
 a control circuit (206), coupled to the buffer writing circuit (204), for generating a plurality of DDR addresses of the plurality of data cells according to a plurality of TDI addresses of the plurality of data cells (404); and
 a DDR writing circuit (208), coupled to the control circuit (206) and the DDR storage device (202), for writing the plurality of data cells in the at least one buffer (200) to the DDR storage device (202) according to the plurality of DDR addresses (406).

2. The TDI (20) of claim 1, **characterized in that** the DDR writing circuit (208) writes the plurality of data cells in the at least one buffer (200) to the DDR storage device (202) according to the plurality of DDR addresses, when the at least one buffer (200) is full.

3. The TDI (20) of any of claims 1-2, **characterized in that** the control circuit (206) generates the plurality of DDR addresses according to the plurality of TDI addresses according to the following equation:

$$N_c \times (R - 1) + \left\lfloor \frac{C}{(N_b \times BUF)} \right\rfloor \times (N_b \times BUF) + (C \bmod N_b) \times N_b \times \frac{BUF}{8} \\ + \left(\left\lfloor \frac{C}{N_b} \right\rfloor \bmod (N_b \times BUF) \right)$$

wherein N_c is a number of columns of the TDI block, (R, C) is one of the plurality of TDI addresses, N_b is a number of the at least one buffer (200), and BUF is a parameter.

4. The TDI (20) of claim 3, **characterized in that** the BUF is related to a ratio of a capacity of a DDR reading/writing (R/W) and a size of one of the plurality of data cells.

5. A time de-interleaver (TDI) (50), **characterized by** the TDI (50) comprising:

a double data rate (DDR) storage device (500);
a cache (502);
a DDR reading circuit (504), coupled to the DDR storage device (500), for reading a first part of a plurality of
data cells in the DDR storage device (500); and
5 a cache writing circuit (506), coupled to the DDR reading circuit (504) and the cache (502), for writing the first
part of the plurality of data cells in the DDR storage device (500) to the cache (502).

6. The TDI (50) of claim 5, **characterized in that** the TDI (50) further comprising:

10 the DDR reading circuit (504), for reading a second part of the plurality of data cells in the DDR storage device
(500); and
the cache writing circuit (506), for writing the second part of the plurality of data cells in the DDR storage device
(500) to the cache (502).

15 7. The TDI (50) of claim 6, **characterized in that** the first part of the plurality of data cells and the second part of the
plurality of data cells are not overlapped in the DDR storage device (500).

8. The TDI of any of claims 5-7, **characterized in that** a capacity of the cache (502) is not smaller than a capacity of
a DDR reading/writing (R/W).

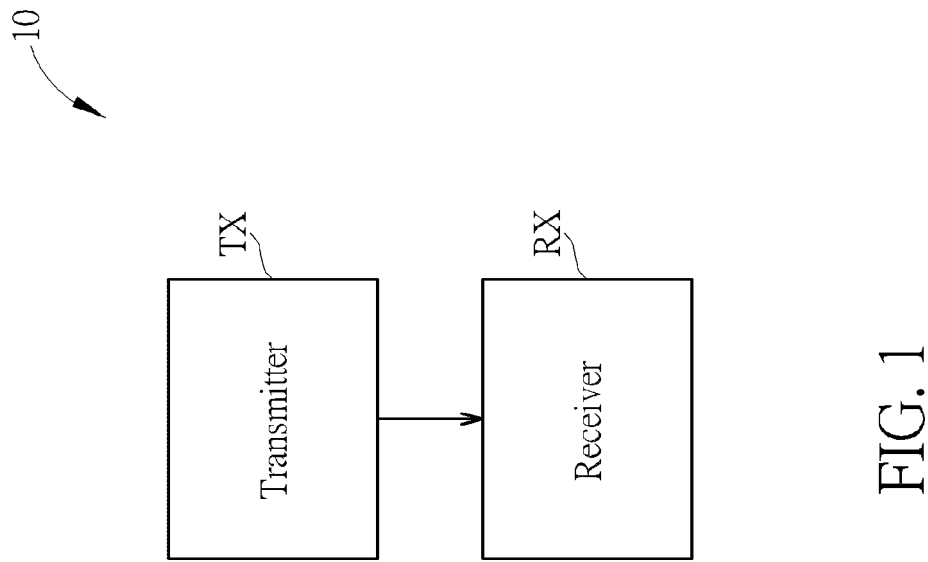


FIG. 1

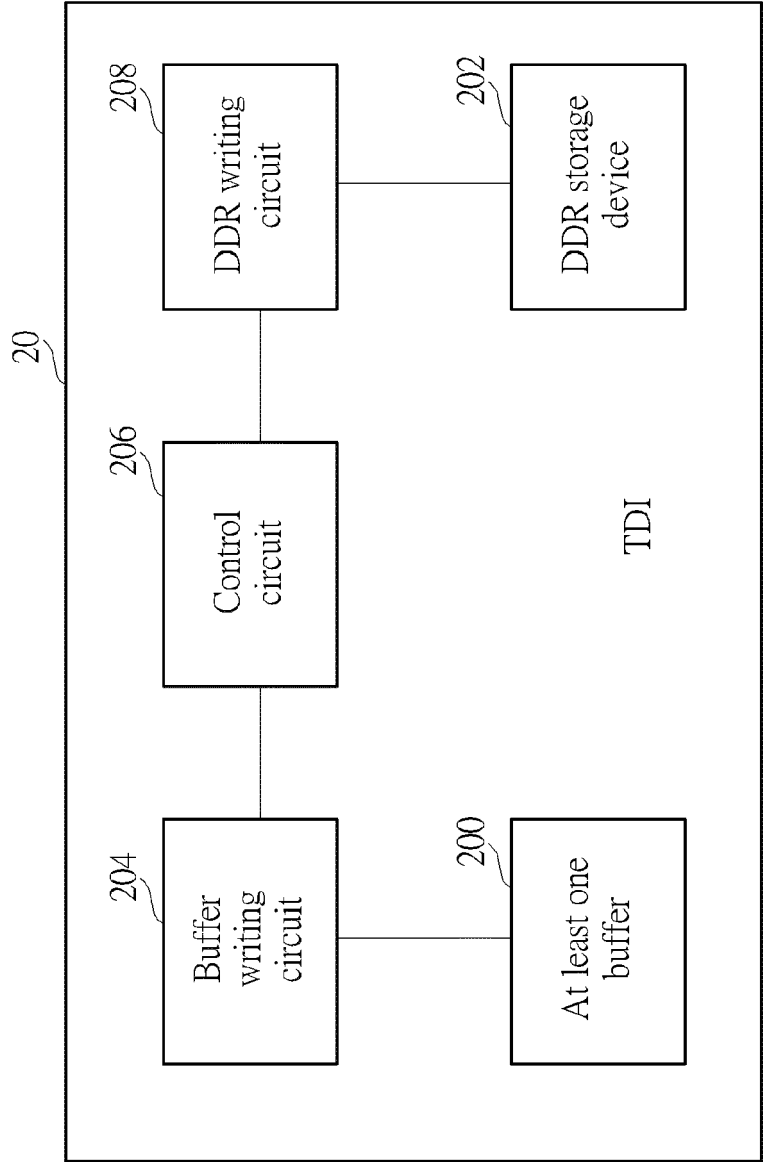


FIG. 2

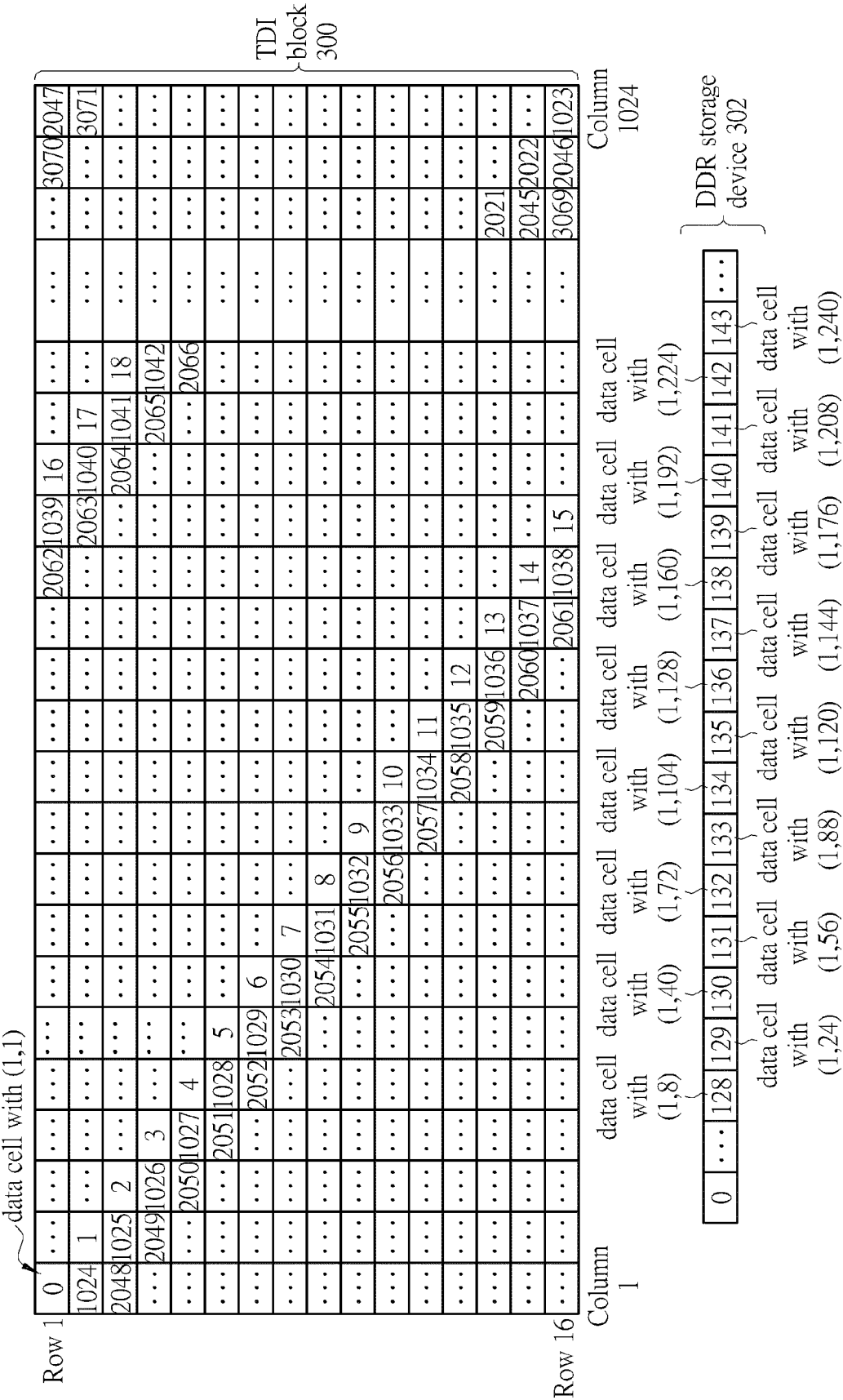


FIG. 3

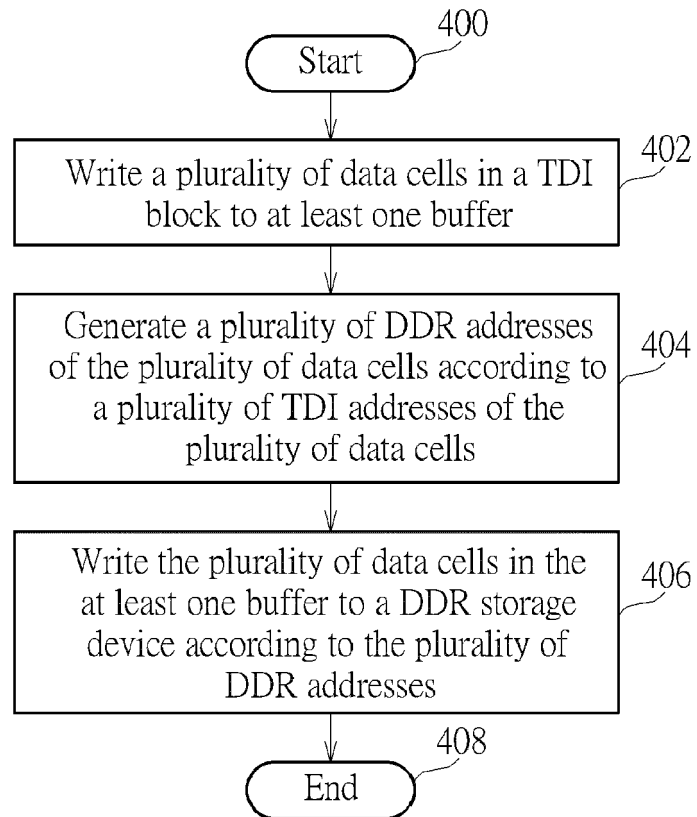


FIG. 4

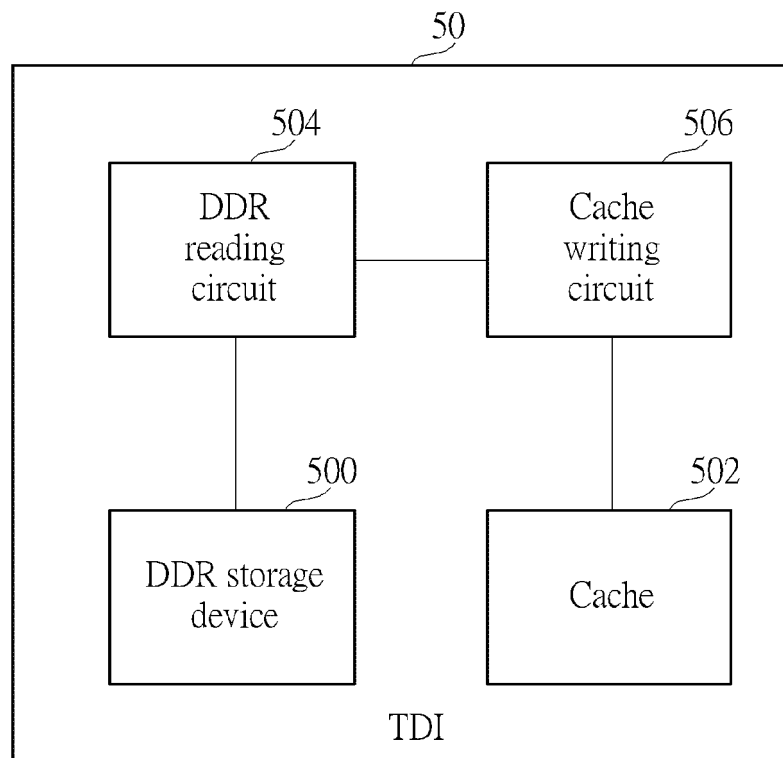


FIG. 5

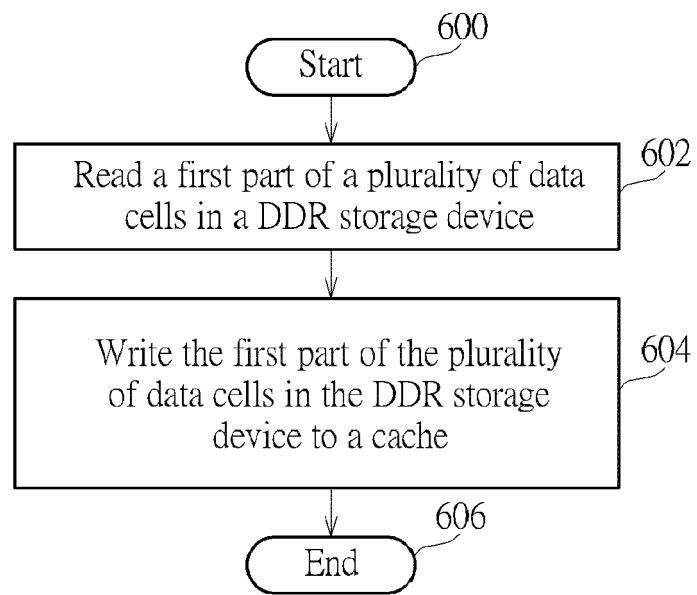


FIG. 6



EUROPEAN SEARCH REPORT

 Application Number
 EP 19 15 8480

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CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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