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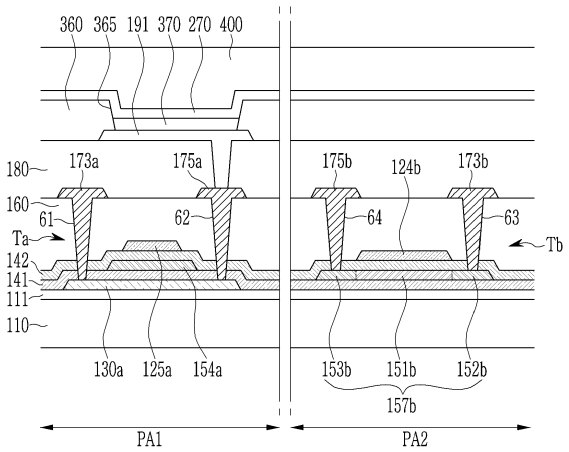
(54) DISPLAY DEVICE

(57) A display device according to an embodiment includes: a substrate; a first transistor and a second transistor disposed on the substrate and spaced apart from each other; a first electrode connected to one of the first transistor and the second transistor; a second electrode overlapping the first electrode; and a light emitting layer between the first electrode and the second electrode, wherein the first transistor may include: a first semiconductor layer on the substrate; a first gate electrode on the first semiconductor layer; and a first source electrode and a first drain electrode connected to the first semiconductor layer, and the second transistor may include: a second semiconductor layer on the substrate; a second gate electrode on the second semiconductor layer; and a second source electrode and a second drain electrode connected to the second semiconductor layer, and the first gate electrode and the second semiconductor layer may be on the same layer.

FIG. 1



EP 3 840 051 A1

Description

BACKGROUND

(a) Field

[0001] The present disclosure relates to a display device.

(b) Description of the Related Art

[0002] Generally, as a display device, a liquid crystal display (LCD), a light emitting diode (LED) display, and the like are used.

[0003] A light emitting diode display includes two electrodes and a light emitting layer disposed therebetween, and an electron injected from a cathode, which is one electrode, and a hole injected from an anode, which is the other electrode, are coupled with each other in the light emitting layer to generate an exciton, and the exciton emits energy to emit light.

[0004] The light emitting diode display includes a plurality of pixels including a light emitting diode including a cathode, an anode, and a light emitting layer, and each pixel includes a plurality of transistors and capacitors for driving the light emitting diode.

[0005] The transistor includes a gate electrode, a source electrode, a drain electrode, and a semiconductor layer. The semiconductor layer is an important element determining characteristics of the transistor. The semiconductor layer is mainly made of silicon (Si). Silicon is classified into amorphous silicon and polycrystalline silicon according to a crystal form. Amorphous silicon has a simple manufacturing process, but has low charge mobility, so it has limitations in manufacturing high-performance transistors, while polycrystalline silicon has high charge mobility, but requires a step of crystallizing silicon, increasing manufacturing cost and making the process complicated. Recently, research has been conducted on transistors using oxide semiconductors having higher electron mobility and a higher ON/OFF ratio than amorphous silicon and having lower cost and higher uniformity than polycrystalline silicon.

SUMMARY OF THE INVENTION

[Technical Problem]

[0006] Embodiments provide a display device that may reduce a time and cost required for a manufacturing process through a simple manufacturing process.

[Technical Solution]

[0007] A display device according to an embodiment includes: a substrate; a first transistor and a second transistor disposed on the substrate and spaced apart from each other; a first electrode connected to one of the first transistor and the second transistor; a second electrode overlapping the first electrode; and a light emitting layer between the first electrode and the second electrode, wherein the first transistor may include: a first semiconductor layer on the substrate; a first gate electrode on the first semiconductor layer; and a first source electrode and a first drain electrode connected to the first semiconductor layer, and the second transistor may include: a second semiconductor layer on the substrate; a second gate electrode on the second semiconductor layer; and a second source electrode and a second drain electrode connected to the second semiconductor layer, and the first gate electrode and the second semiconductor layer may be on the same layer.

[0008] The first gate electrode may include polycrystalline silicon doped with impurities.

[0009] The second semiconductor layer may include polycrystalline silicon.

[0010] The first semiconductor layer may include an oxide semiconductor.

[0011] The first transistor may be connected to the first electrode.

[0012] The display device may include: a buffer layer on the substrate; and a first gate insulating layer on the first semiconductor layer, and the first semiconductor layer may be between the buffer layer and the first gate insulating layer, while the second semiconductor layer and the first gate electrode may be on the first gate insulating layer.

[0013] The display device may further include a second gate insulating layer on the second semiconductor layer and the first gate electrode, and the second gate electrode may be on the second gate insulating layer.

[0014] A display device according to another embodiment includes: a substrate; a first transistor and a second transistor disposed on the substrate and spaced apart from each other; a first electrode connected to one of the first transistor and the second transistor; a second electrode overlapping the first electrode; and a light emitting layer between the first electrode and the second electrode, wherein the first transistor may include: a first semiconductor layer on the substrate; a first gate electrode on the first semiconductor layer; and a first source electrode and a first drain electrode connected to the first semiconductor layer, and the second transistor may include: a second semiconductor layer on the substrate; a second gate electrode on the second semiconductor layer; and a second source electrode and a second drain electrode connected to the second semiconductor layer, and the first semiconductor layer and the second gate electrode may be on the same layer.

[0015] The first semiconductor layer may include polycrystalline silicon, and the second semiconductor layer may include an oxide semiconductor.

[0016] The second gate electrode may include polycrystalline silicon doped with impurities.

[0017] The display device may further include: a buffer layer on the substrate; an insulating layer on the second

semiconductor layer; and a first gate insulating layer on the first semiconductor layer, and the second semiconductor layer may be between the buffer layer and the insulating layer, while the first semiconductor layer may be between the insulating layer and the first gate insulating layer.

[0018] The first gate electrode may be on the first gate insulating layer, and the second gate electrode may be between the insulating layer and the first gate insulating layer.

[0019] A display device according to another embodiment includes: a substrate; a first transistor and a second transistor disposed on the substrate and spaced apart from each other; a first electrode connected to one of the first transistor and the second transistor; a second electrode overlapping the first electrode; and a light emitting layer between the first electrode and the second electrode, wherein the first transistor may include: a first gate electrode on the substrate; a first semiconductor layer on the first gate electrode; and a first source electrode and a first drain electrode connected to the first semiconductor layer, and the second transistor may include: a second semiconductor layer on the substrate; a second gate electrode on the second semiconductor layer; and a second source electrode and a second drain electrode connected to the second semiconductor layer, and the first gate electrode and the second semiconductor layer may be on the same layer.

[0020] The first gate electrode may include polycrystalline silicon doped with impurities.

[0021] The first semiconductor layer may include an oxide semiconductor.

[0022] The second semiconductor layer may include polycrystalline silicon.

[0023] The display device may further include an auxiliary metal layer on the first semiconductor layer, wherein the auxiliary metal layer and the second gate electrode may be on the same layer.

[0024] The auxiliary metal layer may be between the first semiconductor layer and the first source electrode and between the first semiconductor layer and the first drain electrode.

[0025] The auxiliary metal layer may directly contact the first semiconductor layer.

[0026] The display device may further include: a buffer layer on the substrate; and a gate insulating layer on the buffer layer, and the first gate electrode and the second semiconductor layer may be between the buffer layer and the gate insulating layer.

[Advantageous Effects]

[0027] According to the embodiments, it is possible to provide a display device that may reduce a time and cost required for a manufacturing process through a simple manufacturing process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028]

FIG. 1 illustrates a cross-sectional view a partial area of a display device according to an embodiment.
FIG. 2 illustrates a cross-sectional view a partial area of a display device according to an embodiment.
FIG. 3 illustrates a cross-sectional view a partial area of a display device according to an embodiment.
FIG. 4 illustrates a cross-sectional view a partial area of a display device according to an embodiment.
FIG. 5, FIG. 6, FIG. 7, and FIG. 8 respectively illustrate a cross-sectional view of a partial area of a display device according to a manufacturing process.
FIG. 9 illustrates an equivalent circuit diagram of one pixel of a display device according to an embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0029] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

[0030] Parts that are irrelevant to the description will be omitted to clearly describe the present disclosure, and like reference numerals designate like elements throughout the specification.

[0031] Further, in the drawings, the size and thickness of each element are arbitrarily illustrated for ease of description, and the present disclosure is not necessarily limited to those illustrated in the drawings. In the drawings, the thicknesses of layers, films, panels, regions, areas, etc. are exaggerated for clarity. In the drawings, for ease of description, the thicknesses of some layers and areas are exaggerated.

[0032] It will be understood that when an element such as a layer, film, region, area, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Further, in the specification, the word "on" or "above" means positioned (or disposed) on or below the object portion, and does not necessarily mean positioned (or disposed) on the upper side of the object portion based on a gravitational direction.

[0033] In addition, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising" will be understood to imply the inclusion of stated elements but not the exclusion of any other elements.

[0034] Further, throughout the specification, the phrase "in a plan view" or "on a plane" means viewing a

target portion from the top, and the phrase "in a cross-section" or "on a cross-section" means viewing a cross-section formed by vertically cutting a target portion from the side.

Hereinafter, a display device according to an embodiment will be described in detail with reference to the accompanying drawings. Hereinafter, a display device according to an embodiment will be described with reference to FIG. 1. FIG. 1 illustrates a cross-sectional view a partial area of a display device according to an embodiment.

[0035] *Referring to FIG. 1, a substrate 110 includes a first area PA1 in which a first transistor Ta is disposed and a second area PA2 in which a second transistor Tb is disposed. First, the first area PA1 will be described, and then the second area PA2 will be described.*

[0036] *The substrate 110 may include a glass substrate or a substrate in which a polymer layer and a barrier layer are alternately stacked.*

[0037] *A buffer layer 111 is disposed on the substrate 110 corresponding to the first area PA1. The buffer layer 111 may include an inorganic insulating material such as a silicon oxide, a silicon nitride, or the like, or an organic insulating material. The buffer layer 111 may be a single layer or a multilayer. For example, when the buffer layer 111 is a double layer, a lower layer thereof may include a silicon nitride, and an upper layer thereof may include a silicon oxide.*

[0038] *A first semiconductor layer 130a is disposed on the buffer layer 111. The first semiconductor layer 130a according to the embodiment includes an oxide semiconductor.*

[0039] *The oxide semiconductor may include a combination of a metal oxide such as zinc (Zn), indium (In), gallium (Ga), tin (Sn), or titanium (Ti), or a metal such as zinc (Zn), indium (In), gallium (Ga), tin (Sn), or titanium (Ti), and an oxide thereof. More specifically, the oxide semiconductor may include at least one of a zinc oxide (ZnO), a zinc-tin oxide (ZTO), a zinc-indium oxide (ZIO), an indium oxide (InO), a titanium oxide (TiO), an indium-gallium-zinc oxide (IGZO), and an indium-zinc-tin oxide (IZTO).*

[0040] *A first gate insulating layer 141 is disposed on the first semiconductor layer 130a. The first gate insulating layer 141 may include an inorganic insulating material such as a silicon nitride, a silicon oxide, or the like, or an organic insulating material.*

[0041] *A first gate electrode 154a is disposed on the first gate insulating layer 141. The first gate electrode 154a overlaps the first semiconductor layer 130a.*

[0042] *The first gate electrode 154a according to the embodiment includes polycrystalline silicon doped with impurities. The first gate electrode 154a is in a conductive state as impurities are doped into polycrystalline silicon. An impurity doped into the first gate electrode 154a may be a group 5 element, and the first gate electrode 154a may be n+ doped.*

[0043] *A second gate insulating layer 142 is disposed on the first gate electrode 154a and the first gate insulating layer 141. The second gate insulating layer 142 may include an inorganic insulating material such as a silicon nitride, a silicon oxide, or the like, or an organic insulating material.*

[0044] *A storage electrode 125a is disposed on the second gate insulating layer 142. The storage electrode 125a may include at least one of copper, a copper alloy, aluminum, an aluminum alloy, molybdenum, and a molybdenum alloy.*

[0045] *A storage capacitor may be configured by overlapping the first gate electrode 154a and the storage electrode 125a in a plan view with the second gate insulating layer 142 therebetween.*

[0046] *A first insulating layer 160 is disposed on the storage electrode 125a and the second gate insulating layer 142. The first insulating layer 160 may include an inorganic insulating material such as a silicon nitride, a silicon oxide, and an aluminum oxide, or may include an organic insulating material.*

[0047] *A first source electrode 173a connected to the first semiconductor layer 130a including the oxide semiconductor and a first drain electrode 175a connected to the first semiconductor layer 130a are disposed on the first insulating layer 160.*

[0048] *The first source electrode 173a is connected to the first semiconductor layer 130a through a first contact hole 61 formed in the first insulating layer 160, the second gate insulating layer 142, and the first gate insulating layer 141. The first drain electrode 175a is connected to the first semiconductor layer 130a through a second contact hole 62 formed in the first insulating layer 160, the second gate insulating layer 142, and the first gate insulating layer 141.*

[0049] *The first source electrode 173a and the first drain electrode 175a may include a metal film including at least one of copper, a copper alloy, aluminum, an aluminum alloy, molybdenum, and a molybdenum alloy. The first source electrode 173a and the first drain electrode 175a may include a single layer or a multilayer according to embodiments.*

[0050] *A second insulating layer 180 is disposed on the first source electrode 173a and the first drain electrode 175a. The second insulating layer 180 covers and flattens the first source electrode 173a and the first drain electrode 175a. The second insulating layer 180 may include an organic insulating material or an inorganic insulating material.*

[0051] *A pixel electrode 191, which is a first electrode, is disposed on the second insulating layer 180. The pixel electrode 191 may be connected to the first drain electrode 175a through a contact hole formed in the second insulating layer 180.*

[0052] *A partition wall 360 overlapping the second insulating layer 180 and a portion of the pixel electrode 191 is disposed on the pixel electrode 191. The partition wall 360 has an opening 365 exposing the pixel electrode 191.*

[0053] *The partition wall 360 may include an organic*

material such as a polyacrylate resin and a polyimide resin, or a siloxane-based inorganic material.

[0054] A light emitting layer 370, which is a light emitting member, is disposed on the pixel electrode 191 exposed by the opening 365. A common electrode 270 is disposed on the light emitting layer 370 and the partition wall 360. The pixel electrode 191, the light emitting layer 370, and the common electrode 270 may form a light emitting diode.

[0055] Here, the pixel electrode 191 is an anode that is a hole injection electrode, and the common electrode 270 is a cathode that is an electron injection electrode. However, the present embodiment is not limited thereto, and the pixel electrode 191 may be a cathode and the common electrode 270 may be an anode according to a driving method of the display device. Holes and electrons are injected into the light emitting layer 370 from the pixel electrode 191 and the common electrode 270, respectively, and exitons generated by coupling the injected holes and electrons fall from an excited state to a ground state to emit light.

[0056] The light emitting layer 370 may include a low molecular organic material or a polymer organic material such as poly(3,4-ethylenedioxythiophene) (PEDOT). The light emitting layer 370 may be formed as a multilayer including a light emitting layer and at least one of a hole injecting layer, a hole transporting layer, an electron transporting layer, and an electron injecting layer. When all of these are included, the hole injection layer is disposed on the pixel electrode 191, which is an anode, and the hole transport layer, the light emitting layer, the electron transport layer, and an electron injection layer may be sequentially stacked thereon.

[0057] An encapsulation layer 400 for protecting the light emitting diode may be disposed on the common electrode 270. The encapsulation layer 400 may be sealed to the substrate 110 by a sealant. The encapsulation layer 400 may be formed of various materials such as glass, quartz, ceramic, a polymer, and metal. Meanwhile, the encapsulation layer 400 may be formed by depositing an inorganic film and an organic film on the common electrode 270 without using a sealant.

[0058] Hereinafter, the second area PA2 will be described. Detailed description of the constituent elements described in the first area PA1 will be omitted.

[0059] The buffer layer 111 is disposed on the substrate 110 corresponding to the second area PA2. In addition, the first gate insulating layer 141 is disposed on the buffer layer 111.

[0060] A second semiconductor layer 157b is disposed on the first gate insulating layer 141. The second semiconductor layer 157b includes polycrystalline silicon.

[0061] The second semiconductor layer 157b includes a source region 152b connected to a source electrode 173b to be described later, a drain region 153b connected to a drain electrode 175b to be described later, and a channel region 151b disposed between the source region 152b and the drain region 153b. The source region 152b and the drain region 153b are in a conductive state in which impurities are doped into polycrystalline silicon. The impurities doped into the source region 152b and the drain region 153b may be a group 5 element, and may be n+ doped.

[0062] The second gate insulating layer 142 is disposed on the second semiconductor layer 157b and the first gate insulating layer 141.

[0063] A second gate electrode 124b is disposed on the second gate insulating layer 142. The second gate electrode 124b overlaps the channel region 151b of the second semiconductor layer 157b.

[0064] The second gate electrode 124b may include at least one of copper, a copper alloy, aluminum, an aluminum alloy, molybdenum, and a molybdenum alloy.

[0065] The first insulating layer 160 is disposed on the second gate electrode 124b and the second gate insulating layer 142.

[0066] The second source electrode 173b connected to the source region 152b of the second semiconductor layer 157b and the second drain electrode 175b connected to the drain region 153b of the second semiconductor layer 157b are disposed on the first insulating layer 160.

[0067] The second source electrode 173b and the source region 152b are connected through a third contact hole 63 formed in first insulating layer 160 and the second gate insulating layer 142. In addition, the second drain electrode 175b and the drain region 153b are connected through a fourth contact hole 64 formed in the first insulating layer 160 and the second gate insulating layer 142.

[0068] In the second area PA2, the second insulating layer 180, the partition wall 360, the common electrode 270, and the encapsulation layer 400 may be sequentially stacked on the second source electrode 173b and the second drain electrode 175b.

[0069] Hereinafter, a stacking relationship between the first transistor Ta disposed in the first area PA1 and the second transistor Tb disposed in the second area PA2 will be described.

[0070] The first semiconductor layer 130a according to the embodiment is disposed between the buffer layer 111 and the first gate insulating layer 141.

[0071] The first gate electrode 154a and the second semiconductor layer 157b are disposed between the first gate insulating layer 141 and the second gate insulating layer 142. The first gate electrode 154a and the second semiconductor layer 157b are disposed on the same layer. The first gate electrode 154a and the second semiconductor layer 157b may include the same material, and may be formed through the same manufacturing process.

[0072] Since the first gate electrode 154a may be simultaneously formed in the process of forming the second semiconductor layer 157b, a separate gate electrode forming process is not required, and thus the manufacturing process of the display device may be simplified.

[0073] The first gate electrode 154a and the second semiconductor layer 157b include polycrystalline silicon. In addition, the source region 152b and the drain region

153b of the second semiconductor layer 157b and the first gate electrode 154a may include poly crystalline silicon doped with impurities.

[0074] *The storage electrode 125a and the second gate electrode 124b are disposed between the second gate insulating layer 142 and the first insulating layer 160. The storage electrode 125a and the second gate electrode 124b may be formed in the same process, and may include the same material.*

[0075] *The display device according to the embodiment may include the first transistor Ta including an oxide semiconductor and the second transistor Tb including polycrystalline silicon. In this case, since the first gate electrode 154a included in the first transistor Ta and the semiconductor layer 157b included in the second transistor Tb may be formed through the same process, the manufacturing process and the stacked structure may be simplified.*

Hereinafter, a display device according to an embodiment will be described with reference to FIG. 2 and FIG. 4. FIG. 2, FIG. 3, and FIG. 4 illustrate a cross-sectional view of a display device according to an embodiment, respectively. A description of the same or similar constituent elements as those of the embodiments described above will be omitted.

[0076] First, referring to FIG. 2, the substrate 110 includes the first area PA1 in which the first transistor Ta is disposed and the second area PA2 in which the second transistor Tb is disposed. First, the first area PA1 will be described, and then the second area PA2 will be described.

[0077] The buffer layer 111 is disposed on the substrate 110 corresponding to the first area PA1. An insulating layer 131 is disposed on the buffer layer 111. The insulating layer 131 may include an inorganic insulating material or an organic insulating material.

[0078] Next, a first semiconductor layer 157a is disposed on the insulating layer 131. The first semiconductor layer 157a includes polycrystalline silicon.

[0079] The first semiconductor layer 157a includes a source region 152a connected to a source electrode 173a to be described later, a drain region 153a connected to a drain electrode 175a, and a channel region 151a disposed between the source region 152a and the drain region 153a. The source region 152a and the drain region 153a are in a conductive state in which impurities are doped.

[0080] The first gate insulating layer 141 is disposed on the insulating layer 131 and the first semiconductor layer 157a.

[0081] A first gate electrode 124a is disposed on the first gate insulating layer 141. The first gate electrode 124a overlaps the channel region 151a of the first semiconductor layer 157a. The first gate electrode 124a may include at least one of copper, a copper alloy, aluminum, an aluminum alloy, molybdenum, and a molybdenum alloy.

[0082] A second gate insulating layer 142 is disposed on the first gate electrode 124a and the first gate insulating layer 141.

[0083] A storage electrode 125a is disposed on the second gate insulating layer 142. Although not shown in the present specification, the storage electrode 125a may be connected to a separate driving voltage line and the like.

[0084] The storage electrode 125a and the first gate electrode 124a may form a storage capacitor by overlapping each other with the second gate insulating layer 142 therebetween.

[0085] A first insulating layer 160 is disposed on the storage electrode 125a and the second gate insulating layer 142.

[0086] The first source electrode 173a and the source region 152a of the first semiconductor layer 157a are connected through the first contact hole 61 formed in the first insulating layer 160, the second gate insulating layer 142, and the first gate insulating layer 141. The first drain electrode 175a and the drain region 153a of the first semiconductor layer 157a are connected through the second contact hole 62 of the first insulating layer 160, the second gate insulating layer 142, and the first gate insulating layer 141.

[0087] A second insulating layer 180 is disposed on the first source electrode 173a and the first drain electrode 175a.

[0088] A pixel electrode 191, which is a first electrode, is disposed on the second insulating layer 180. The pixel electrode 191 may be connected to the first drain electrode 175a through a contact hole formed in the second insulating layer 180.

[0089] A partition wall 360 overlapping the second insulating layer 180 and a portion of the pixel electrode 191 is disposed on the pixel electrode 191. A light emitting layer 370, which is a light emitting member, is disposed on the pixel electrode 191 exposed by the opening 365 included in the partition wall 360. A common electrode 270 is disposed on the light emitting layer 370 and the partition wall 360. The pixel electrode 191, the light emitting layer 370, and the common electrode 270 may form a light emitting diode. An encapsulation layer 400 for protecting the light emitting diode may be disposed on the common electrode 270.

[0090] Hereinafter, the second transistor Tb disposed in the second area PA2 will be described.

[0091] The buffer layer 111 is disposed on the substrate 110, and a second semiconductor layer 130b is disposed on the buffer layer 111.

[0092] The second semiconductor layer 130b according to the embodiment includes an oxide semiconductor. The oxide semiconductor may include a combination of a metal oxide such as zinc (Zn), indium (In), gallium (Ga), tin (Sn), or titanium (Ti), or a metal such as zinc (Zn), indium (In), gallium (Ga), tin (Sn), or titanium (Ti), and an oxide thereof. More specifically, the oxide semiconductor may include at least one of a zinc oxide (ZnO), a zinc-tin oxide (ZTO), a zinc-indium oxide (ZIO), an indium oxide

(InO), a titanium oxide (TiO), an indium-gallium-zinc oxide (IGZO), and an indium-zinc-tin oxide (IZTO).

[0093] The insulating layer 131 is disposed on the second semiconductor layer 130b and the buffer layer 111. The insulating layer 131 may include an inorganic insulating material or an organic insulating material. A second gate electrode 154b is disposed on the insulating layer 131.

[0094] The second gate electrode 154b may include polycrystalline silicon doped with impurities. The second gate electrode 154b is in a conductive state as impurities are doped into polycrystalline silicon.

[0095] The first gate insulating layer 141, the second gate insulating layer 142, and the first insulating layer 160 are sequentially disposed on the insulating layers 131 and the second gate electrodes 154b.

[0096] A second source electrode 173b connected to the second semiconductor layer 130b and a second drain electrode 175b connected to the second semiconductor layer 130b are disposed on the first insulating layer 160.

[0097] The second source electrode 173b may be connected to the second semiconductor layer 130b through the third contact hole 63, and the second drain electrode 175b may be connected to the second semiconductor layer 130b through the fourth contact hole 64.

[0098] The second insulating layer 180, the partition wall 360, the common electrode 270, and the encapsulation layer 400 are sequentially disposed on the second source electrode 173b and the second drain electrode 175b.

[0099] Hereinafter, a stacking relationship between the first transistor Ta disposed in the first area PA1 and the second transistor Tb disposed in the second area PA2 will be described.

[0100] The second semiconductor layer 130b is disposed between the buffer layer 111 and the insulating layer 131.

[0101] The first semiconductor layer 157a and the second gate electrode 154b are disposed between the insulating layer 131 and the first gate insulating layer 141. The first semiconductor layer 157a and the second gate electrode 154b are disposed on the same layer. The first semiconductor layer 157a and the second gate electrode 154b may include the same material, and may be formed through the same manufacturing process.

[0102] The first semiconductor layer 157a and the second gate electrode 154b include polycrystalline silicon. The source region 152a and the drain region 153a of the first semiconductor layer 157a and the second gate electrode 154b may include polycrystalline silicon doped with impurities.

[0103] Since the second gate electrode 154b may be simultaneously formed in the process of forming the first semiconductor layer 157a, a separate gate electrode forming process is not required, and thus the manufacturing process may be simplified.

[0104] The display device according to the embodiment may include the first transistor Ta including polycrystalline silicon and the second transistor Tb including an oxide semiconductor. In this case, since the semiconductor layer 157a included in the first transistor Ta and the gate electrode 154b included in the second transistor Tb may be formed through the same process, the manufacturing process and the stacked structure may be simplified.

[0105] Hereinafter, it will be described with reference to FIG. 3. In FIG. 3, the first area PA1 in which the first transistor Ta is disposed will be first described.

[0106] Referring to FIG. 3, the first gate electrode 154a is disposed on the buffer layer 111. The first gate electrode 154a may include polycrystalline silicon doped with impurities.

[0107] A gate insulating layer 140 is disposed on the first gate electrode 154a and the buffer layer 111.

[0108] The first semiconductor layer 157a is disposed on the gate insulating layer 140. The first semiconductor layer 157a according to the embodiment may include an oxide semiconductor.

[0109] The first insulating layer 160 is disposed on the first semiconductor layer 157a. A first source electrode 173a connected to a first semiconductor layer 130a including an oxide semiconductor through a first contact hole 61 and a first drain electrode 175a connected to the first semiconductor layer 130a through a second contact hole 62 are disposed on the first insulating layer 160.

[0110] Next, the second area PA2 in which the second transistor Tb is disposed will be described.

[0111] The second semiconductor layer 157b is disposed on the buffer layer 111 disposed on the substrate 110. The second semiconductor layer 157b includes polycrystalline silicon.

[0112] The second semiconductor layer 157b includes a source region 152b connected to a second source electrode 173b, a drain region 153b connected to a second drain electrode 175b, and a channel region 151b disposed between the source region 152b and the drain region 153b. The source region 152b and the drain region 153b are in a conductive state in which impurities are doped.

[0113] The gate insulating layer 140 is disposed on the second semiconductor layer 157b and the buffer layer 111. A second gate electrode 124b is disposed on the gate insulating layer 140. The second gate electrode 124b may overlap the channel region 151b of the second semiconductor layer 157b.

[0114] The second gate electrode 124b may include a metal film including at least one of copper, a copper alloy, aluminum, an aluminum alloy, molybdenum, and a molybdenum alloy. The second gate electrode 124b may include a single film or multi-film according to an embodiment.

[0115] The first insulating layer 160 is disposed on the second gate electrode 124b and the gate insulating layer 140.

[0116] The second source electrode 173b is connected to the source region 152b through the third contact

hole 63 formed in the first insulating layer 160 and the gate insulating layer 140. The second drain electrode 175b is connected to the drain region 153b through the fourth contact hole 64 formed in the first insulating layer 160 and the gate insulating layer 140.

[0117] The first gate electrode 154a and the second semiconductor layer 157b according to the embodiment may be disposed between the buffer layer 111 and the gate insulating layer 140. The first gate electrode 154a and the second semiconductor layer 157b are disposed on the same layer. The first gate electrode 154a and the second semiconductor layer 157b may include the same material, and may be formed through the same manufacturing process.

[0118] The first gate electrode 154a and the second semiconductor layer 157b include polycrystalline silicon. In addition, the source region 152b and the drain region 153b of the second semiconductor layer 157b and the first gate electrode 154a may be doped with impurities in polycrystalline silicon.

[0119] Since the first gate electrode 154a may be simultaneously formed in the process of forming the second semiconductor layer 157b, a separate gate electrode forming process is not required, and thus a process therefor may be simplified.

[0120] Although the present specification shows the configuration in which the light emitting diode is connected to the first transistor Ta in FIG. 3, the present invention is not limited thereto, and the light emitting diode may be connected to the second transistor Tb.

[0121] Hereinafter, it will be described with reference to FIG. 4. Referring to FIG. 4, auxiliary metal layers 126a and 127a are disposed on the first semiconductor layer 157a disposed in the first area PA. The first insulating layer 160 is disposed on the auxiliary metal layers 126a and 127a.

[0122] The first source electrode 173a and the first drain electrode 175a are disposed on the first insulating layer 160. The first source electrode 173a is connected to the auxiliary metal layer 126a through the first contact hole 61 formed in the first insulating layer 160. The first drain electrode 175a may be connected to the auxiliary metal layer 127a through the second contact hole 62 formed in the first insulating layer 160.

[0123] The auxiliary metal layers 126a and 127a may be disposed on the same layer as the second gate electrode 124b. The auxiliary metal layers 126a and 127a and the second gate electrode 124b may be disposed between the gate insulating layer 140 and the first insulating layer 160.

[0124] Hereinafter, a manufacturing method of the display device according to the embodiment will be described with reference to FIG. 5 to FIG. 8. FIG. 5, FIG. 6, FIG. 7, and FIG. 8 respectively illustrate a cross-sectional view of a partial area of a display device according to a manufacturing process.

[0125] First, as shown in FIG. 5, the substrate 110 includes the first area PA1 and the second area PA2. The buffer layer 111 is disposed on the entire surface of the substrate 110 so as to overlap the first area PA1 and the second area PA2. In addition, the first semiconductor layer 130a including an oxide semiconductor is formed in the first area PA1.

[0126] Next, as shown in FIG. 6, the first gate insulating layer 141 overlapping the entire surface of the substrate 110 is formed on the buffer layer 111 and the first semiconductor layer 130a.

[0127] The second semiconductor layer 157b is formed on the first gate insulating layer 141 disposed in the second area PA2, and the first gate electrode 154a is formed on the gate insulating layer 141 disposed in the first area PA1. The first gate electrode 154a and the second semiconductor layer 157b are formed on the same layer.

[0128] The first gate electrode 154a and the second semiconductor layer 157b include polycrystalline silicon. In addition, the source region 152b and the drain region 153b of the second semiconductor layer 157b and the first gate electrode 154a may be doped with impurities in polycrystalline silicon.

[0129] Since the first gate electrode 154a may be simultaneously formed in the process of forming the second semiconductor layer 157b, a separate gate electrode forming process is not required, and thus a process therefor may be simplified.

[0130] As shown in FIG. 7, the second gate insulating layer 142 overlapping the entire surface of the substrate 110 is formed on the first gate electrode 154a, the second semiconductor layer 157b, and the first gate insulating layer 141. Then, the storage electrode 125a and the second gate electrode 124b are formed on the second gate insulating layer 142.

[0131] Next, as shown in FIG. 8, the first insulating layer 160 overlapping the entire surface of the substrate 110 is formed. The first insulating layer 160, the second gate insulating layer 142, and the first gate insulating layer 141 have the first contact hole 61 and the second contact hole 62 exposing a portion of the first semiconductor layer 130a. In addition, the first insulating layer 160 and the second gate insulating layer 142 have the third contact hole 63 exposing a portion of the source region 152b and the fourth contact hole 64 exposing a portion of the drain region 153b.

[0132] Next, the first source electrode 173a, the first drain electrode 175a, the second source electrode 173b, and the second drain electrode 175b are formed on the first insulating layer 160, and then the light emitting diode connected to the first drain electrode 175a is formed, thereby providing the display device as shown in FIG. 1.

[0133] Hereinafter, a display device according to an embodiment will be described with reference to FIG. 9. FIG. 9 illustrates an equivalent circuit diagram of one pixel of a display device according to an embodiment.

[0134] As shown in FIG. 9, one pixel PX of the display device according to the embodiment may include a plurality of transistors T1, T2, T3, T4, T5, T6, and T7 con-

nected to a plurality of signal lines 151, 152, 153, 154, 155, 156, 171, and 172, a storage capacitor Cst, and a light emitting diode LED. Although a structure including seven transistors and one capacitor is shown in the present embodiment, the present embodiment is not necessarily limited thereto, and the number of transistors and the number of capacitors may be variously changed.

[0135] The transistors T1, T2, T3, T4, T5, T6, and T7 may include the first transistor Ta including an oxide semiconductor and the second transistor Tb including polycrystalline silicon. The first transistor Ta may include a driving transistor T1, a switching transistor T2, an operation control transistor T5, and a light emission control transistor T6. The second transistor Tb may include a compensation transistor T3, an initialization transistor T4, and a bypass transistor T7, but is not limited thereto.

[0136] The signal lines 151, 152, 153, 154, 155, 156, 171, and 172 may include a first scan line 151, a second scan line 152, a third scan line 153, an emission control line 154, a bypass control line 155, an initialization voltage line 156, a data line 171, and a driving voltage line 172. The first scan line 151, the second scan line 152, the third scan line 153, the emission control line 154, the bypass control line 155, the initialization voltage line 156, the data line 171, and the driving voltage line 172 may be connected to one pixel PX.

[0137] The first scan line 151 may transmit a first scan signal GW1 to the switching transistor T2, the second scan line 152 may transmit a second scan signal GW2 to the compensation transistor T3, and the third scan line 153 may transmit a third scan signal GI to the initialization transistor T4. In addition, the emission control line 154 may transmit an emission control signal EM to the operation control transistor T5 and the emission control transistor T6, and the bypass control line 155 may transmit a bypass signal GB to the bypass transistor T7. Further, the initialization voltage line 156 may transmit an initialization voltage Vint that initializes the driving transistor T1.

[0138] The data line 171 may transmit a data signal Dm, and the driving voltage line 172 may transmit a driving voltage ELVDD.

[0139] A gate electrode G1 of the driving transistor T1 is connected to one end Cst1 of the storage capacitor Cst, and a source electrode S1 of the driving transistor T1 is connected to the driving voltage line 172 via the operation control transistor T5. A drain electrode D1 of the driving transistor T1 may be electrically connected to an anode of the light emitting diode LED via the light emission control transistor T6. The driving transistor T1 may receive the data signal Dm in accordance with a switching operation of the switching transistor T2 to supply a driving current Id to the light emitting diode LED.

[0140] A gate electrode G2 of the switching transistor T2 may be connected to the first scan line 151, a source electrode S2 of the switching transistor T2 may be connected to the data line 171, and a drain electrode D2 of the switching transistor T2 may be connected to the source electrode S1 of the driving transistor T1 and may be connected to the driving voltage line 172 via the operation control transistor T5. The switching transistor T2 may be turned on in response to the first scan signal GW1 transmitted through the first scan line 151 to perform a switching operation to transmit the data signal Dm transmitted to the data line 171 to the source electrode S1 of the driving transistor T1.

[0141] A gate electrode G3 of the compensation transistor T3 may be connected to the second scan 152, a source electrode S3 of the compensation transistor T3 may be connected to the drain electrode D1 of the driving transistor T1 and may be connected to the anode of the light emitting diode LED via the emission control transistor T6, and a drain electrode D3 of the compensation transistor T3 may be connected to the drain electrode D4 of the initialization transistor T4, one end Cst1 of the storage capacitor Cst, and the gate electrode G1 of the driving transistor T1. The compensation transistor T3 may be turned on depending on the second scan signal GW2 transmitted through the second scan line 152 to connect the gate electrode G1 and the drain electrode D1 of the driving transistor T1 to each other to diode-connect the driving transistor T1. According to an example, the second scan signal GW2 is a signal in which a level of the first scan signal GW1 is inverted, and thus, when the first scan signal GW1 is at a high level, the second scan signal GW2 may be at a low level, while when the first scan signal GW1 is at a low level, the second scan signal GW2 may be at a high level.

[0142] A gate electrode G4 of the initialization transistor T4 may be connected to the third scan line 153, a source electrode S4 of the initialization transistor T4 may be connected to the initialization voltage line 156, and a drain electrode D4 of the initialization transistor T4 may be connected to the one end Cst1 of the storage capacitor Cst and the gate electrode G1 of the driving transistor T1 via the drain electrode D3 of the compensation transistor T3. The initialization transistor T4 may be turned on according to the third scan signal GI transmitted through the third scan 153 to transmit the initialization voltage Vint to the gate electrode G1 of the driving transistor T1 to perform an initializing operation to initialize a gate voltage Vg of the gate electrode G1 of the driving transistor T1.

[0143] A gate electrode G5 of the operation control transistor T5 may be connected to the emission control line 154, a source electrode S5 of the operation control transistor T5 may be connected to the driving voltage line 172, and a drain electrode D5 of the operation control transistor T5 may be connected to the source electrode S1 of the driving transistor T1 and the drain electrode S2 of the switching transistor T2.

[0144] A gate electrode G6 of the emission control transistor T6 may be connected to the emission control line 154, a source electrode S6 of the emission control transistor T6 may be connected to the drain electrode D1 of the driving transistor T1 and the source electrode S3 of

the compensation transistor T3, and a drain electrode D6 of the emission control transistor T6 may be electrically connected to the anode of the light emitting diode LED. The operation control transistor T5 and the emission control transistor T6 may be simultaneously turned on according to an emission control signal EM transmitted through the emission control line 154, thus the driving voltage ELVDD may be compensated through the diode-connected driving transistor T1 and then may be transmitted to the light emitting diode LED.

[0145] A gate electrode G7 of the bypass transistor T7 may be connected to the bypass control line 155, a source electrode S7 of the bypass transistor T7 may be connected together to the drain electrode D6 of the emission control transistor T6 and the anode of the light emitting diode LED, and a drain electrode D7 of the bypass transistor T7 may be connected together to the initialization voltage line 156 and the source electrode S4 of the initialization transistor T4.

[0146] The other end Cst2 of the storage capacitor Cst may be connected to the driving voltage line 172, and the cathode of the light emitting diode LED may be connected to a driving voltage line 741 for transmitting the common voltage ELVSS.

[0147] While this invention has been described in connection with what is presently considered to be practical embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

Claims

1. A display device comprising:

a substrate;
a first transistor and a second transistor disposed on the substrate and spaced apart from each other;
a first electrode electrically connected to one of the first transistor and the second transistor;
a second electrode overlapping the first electrode; and
a light emitting layer between the first electrode and the second electrode,
wherein the first transistor includes:

a first semiconductor layer on the substrate;
a first gate electrode on the first semiconductor layer; and
a first source electrode and a first drain electrode electrically connected to the first semiconductor layer, and

the second transistor includes:

a second semiconductor layer on the substrate;
a second gate electrode on the second semiconductor layer; and
a second source electrode and a second drain electrode electrically connected to the second semiconductor layer, and

the first gate electrode and the second semiconductor layer are on the same layer.

2. The display device of claim 1, wherein
the first gate electrode includes polycrystalline silicon doped with impurities.

3. The display device of claim 1, wherein
the second semiconductor layer includes polycrystalline silicon.

4. The display device of claim 1, wherein
the first semiconductor layer includes an oxide semiconductor.

5. The display device of claim 1, wherein
the first transistor is connected to the first electrode.

6. The display device of claim 1, wherein
the display device further includes:

a buffer layer on the substrate; and
a first gate insulating layer on the first semiconductor layer, and
wherein the first semiconductor layer is between the buffer layer and the first gate insulating layer, while
the second semiconductor layer and the first gate electrode are on the first gate insulating layer.

7. The display device of claim 6, wherein
the display device further includes a second gate insulating layer on the second semiconductor layer and the first gate electrode, and
wherein the second gate electrode is on the second gate insulating layer.

8. A display device comprising:

a substrate;
a first transistor and a second transistor disposed on the substrate and spaced apart from each other;
a first electrode electrically connected to one of the first transistor and the second transistor;
a second electrode overlapping the first electrode; and
a light emitting layer between the first electrode and the second electrode,

wherein the first transistor includes:

a first semiconductor layer on the substrate;
a first gate electrode on the first semiconductor layer; and
a first source electrode and a first drain electrode electrically connected to the first semiconductor layer, and

the second transistor includes:

a second semiconductor layer on the substrate;
a second gate electrode on the second semiconductor layer; and
a second source electrode and a second drain electrode connected to the second semiconductor layer, and

the first semiconductor layer and the second gate electrode are on the same layer.

9. The display device of claim 8, wherein
the first semiconductor layer includes polycrystalline silicon, and the second semiconductor layer includes an oxide semiconductor.

10. The display device of claim 8, wherein
the second gate electrode includes polycrystalline silicon doped with impurities.

11. The display device of claim 8, wherein
the display device further includes:

a buffer layer on the substrate;
an insulating layer on the second semiconductor layer; and
a first gate insulating layer on the first semiconductor layer, and
the second semiconductor layer is between the buffer layer and the insulating layer, and the first semiconductor layer is between the insulating layer and the first gate insulating layer.

12. The display device of claim 11, wherein
the first gate electrode is on the first gate insulating layer, and
the second gate electrode is between the insulating layer and the first gate insulating layer.

13. A display device comprising:

a substrate;
a first transistor and a second transistor disposed on the substrate and spaced apart from each other;
a first electrode electrically connected to one of the first transistor and the second transistor;
a second electrode overlapping the first electrode; and
a light emitting layer between the first electrode and the second electrode,
wherein the first transistor includes:

a first gate electrode on the substrate;
a first semiconductor layer on the first gate electrode; and
a first source electrode and a first drain electrode connected to the first semiconductor layer, and

the second transistor includes:

a second semiconductor layer on the substrate;
a second gate electrode on the second semiconductor layer; and
a second source electrode and a second drain electrode connected to the second semiconductor layer, and

the first gate electrode and the second semiconductor layer are on the same layer.

14. The display device of claim 13, wherein
the first gate electrode includes polycrystalline silicon doped with impurities.

15. The display device of claim 13, wherein
the first semiconductor layer includes an oxide semiconductor.

16. The display device of claim 13, wherein
the second semiconductor layer includes polycrystalline silicon.

17. The display device of claim 13, further comprising
an auxiliary metal layer on the first semiconductor layer,
wherein the auxiliary metal layer and the second gate electrode are on the same layer.

18. The display device of claim 17, wherein
the auxiliary metal layer is between the first semiconductor layer and the first source electrode and between the first semiconductor layer and the first drain electrode.

19. The display device of claim 17, wherein
the auxiliary metal layer directly contacts the first semiconductor layer.

20. The display device of claim 13, wherein
the display device further includes:

a buffer layer on the substrate; and

a gate insulating layer on the buffer layer, and the first gate electrode and the second semiconductor layer are between the buffer layer and the gate insulating layer.

FIG. 1

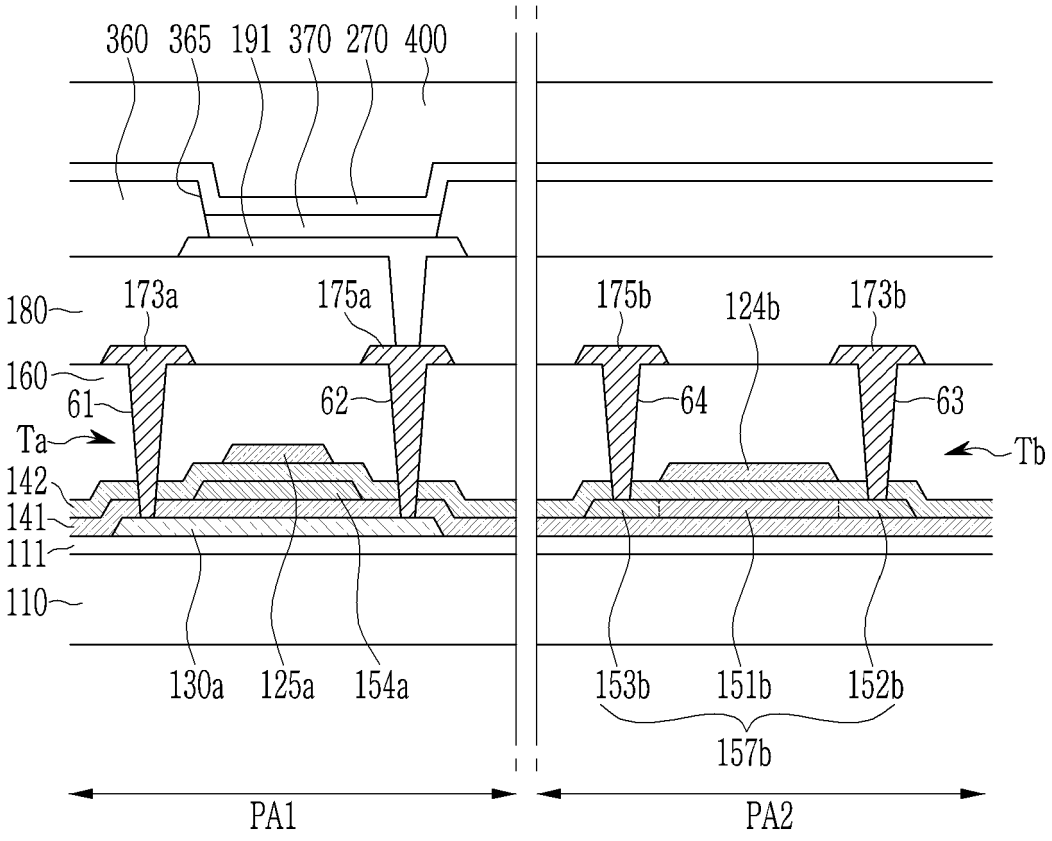

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FIG. 2

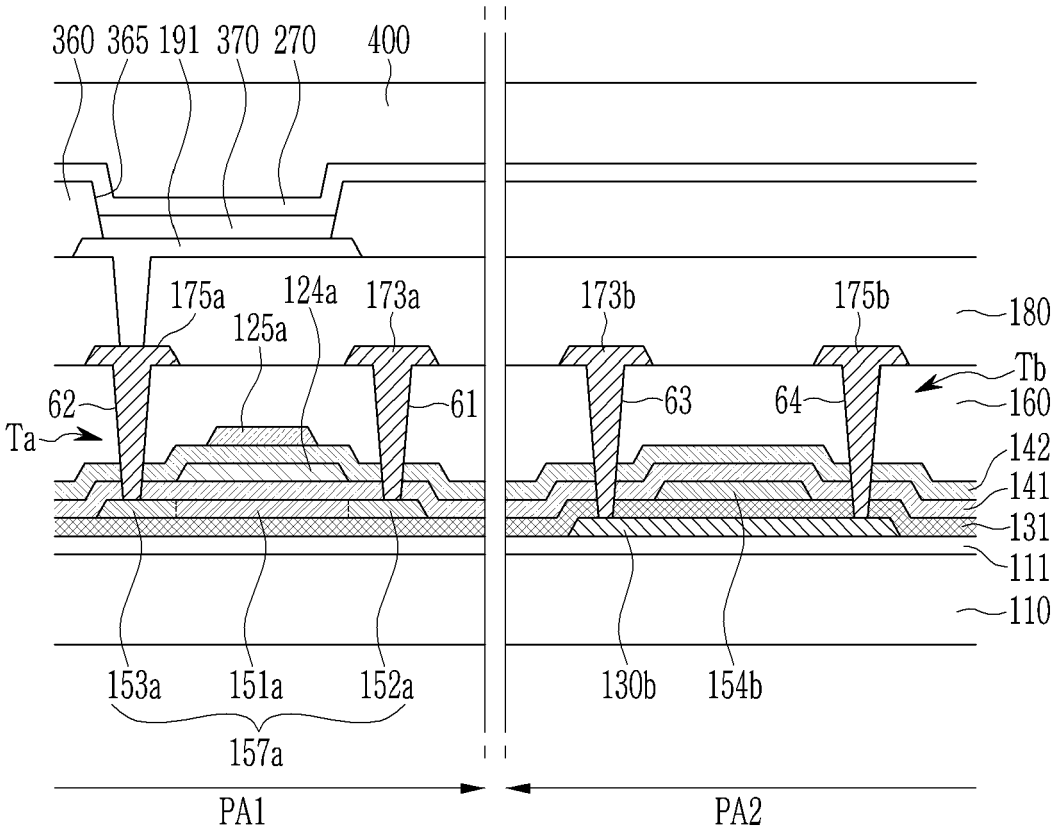
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FIG. 3

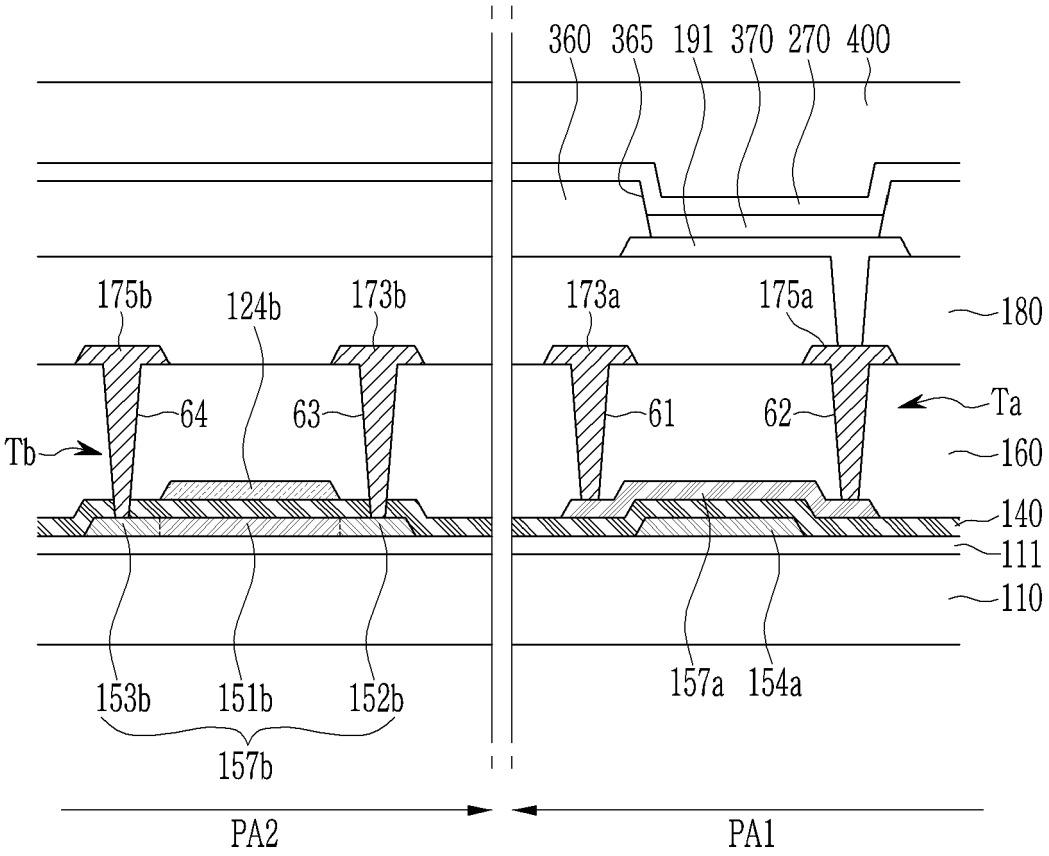
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FIG. 4

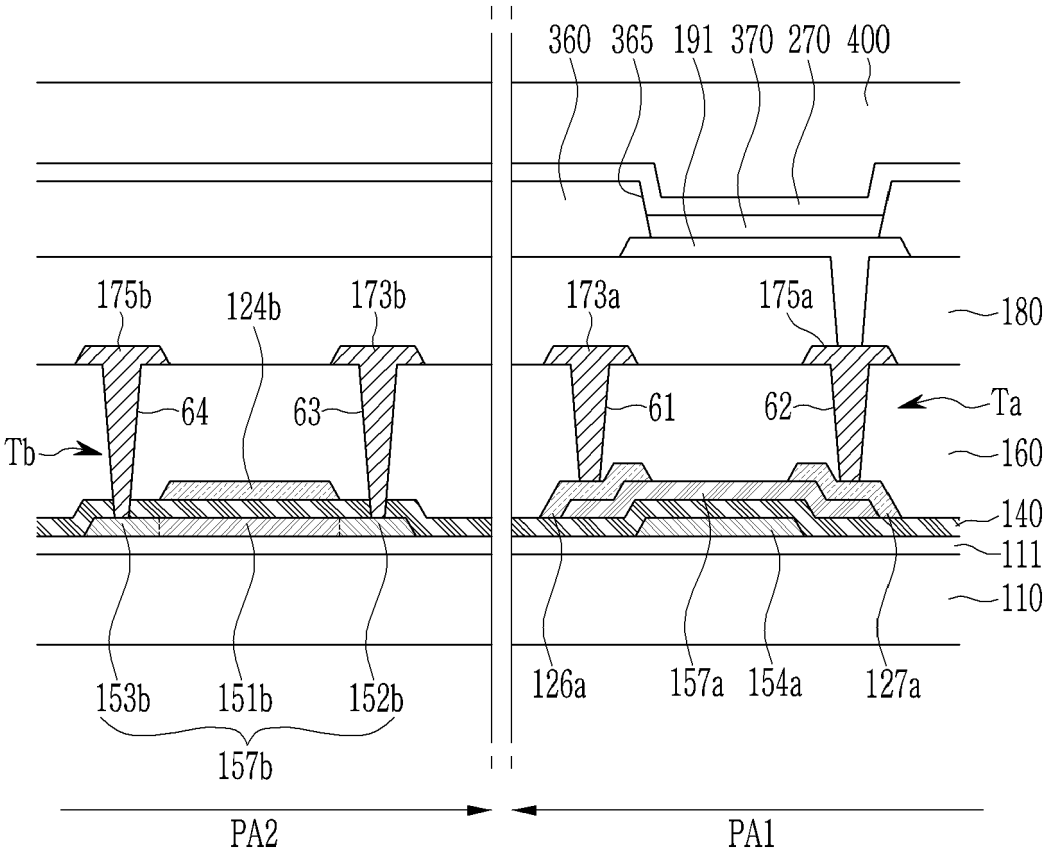
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FIG. 5

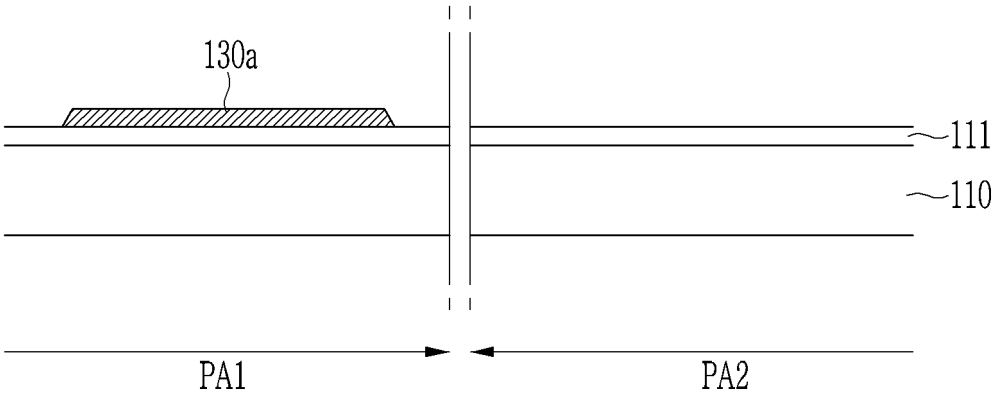


FIG. 6

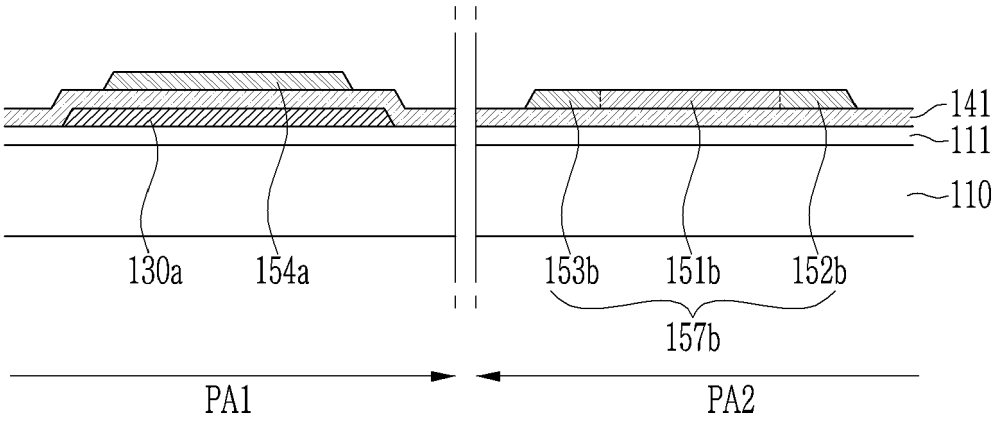
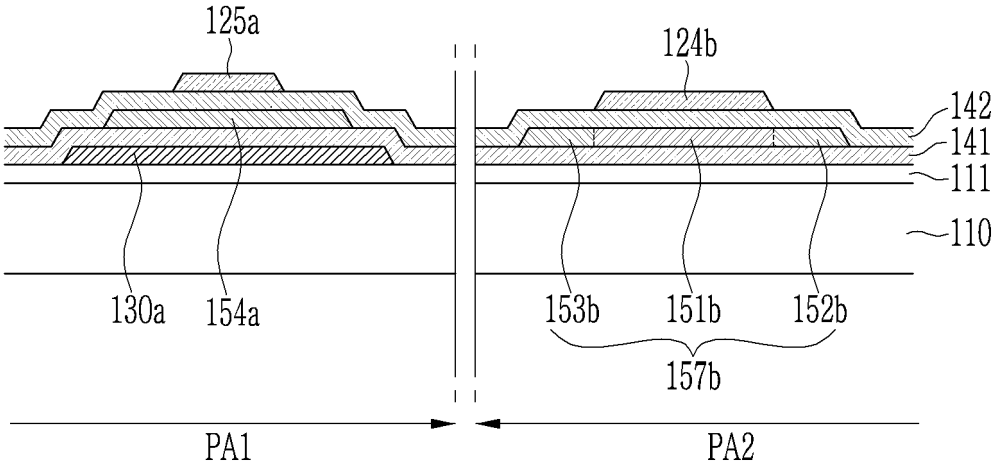


FIG. 7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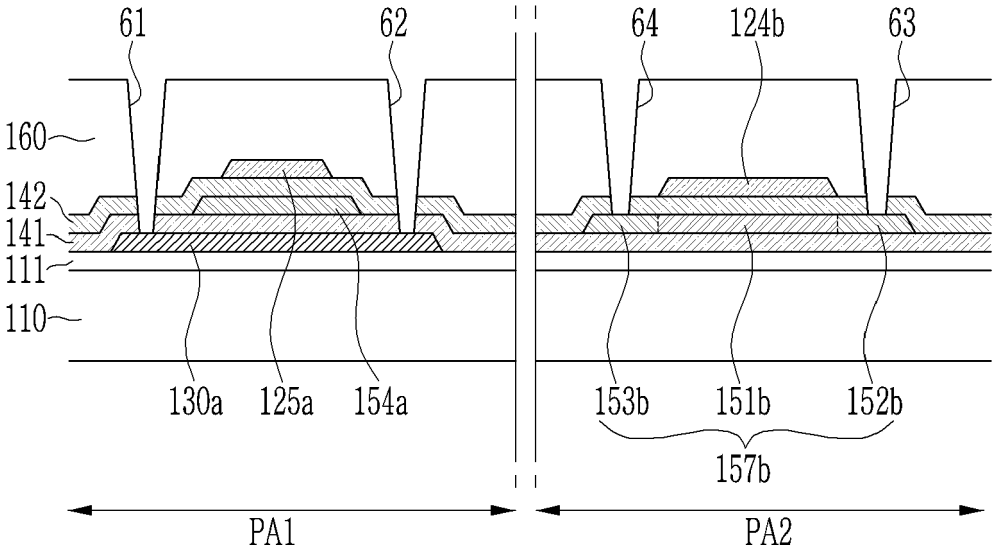
PA2

FIG. 8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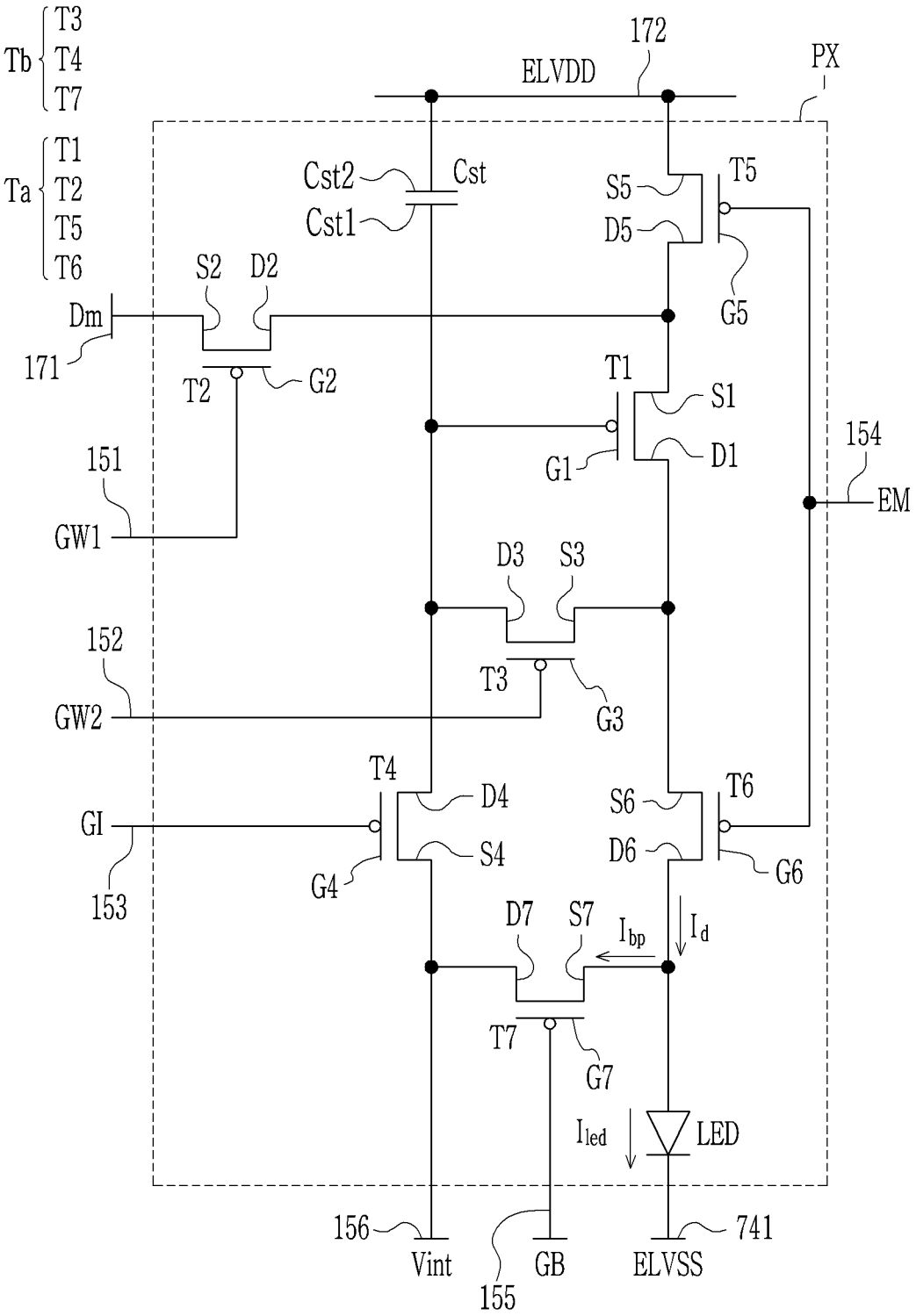
PA1
PA2

FIG. 9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G1
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GW1
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741

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2019/009108

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/32(2006.01)i, H01L 51/50(2006.01)i, H01L 29/786(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/32; G09G 3/3233; H01L 21/336; H01L 27/12; H01L 29/786; H01L 51/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models: IPC as above
Japanese utility models and applications for utility models: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS (KIPO internal) & Keywords: display device, transistor, semiconductor layer, gate electrode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y		2-4,9-10,17-19
A		13-16,20
X	KR 10-2011-0024935 A (SAMSUNG MOBILE DISPLAY CO., LTD.) 09 March 2011 See paragraphs [0032]-[0072] and figures 1-6.	13-16,20
Y		2-4,9-10,17-19
A	KR 10-2017-0101203 A (LG DISPLAY CO., LTD.) 05 September 2017 See paragraphs [0062]-[0077] and figures 6a-6h.	1-20
A	KR 10-2018-0025354 A (SAMSUNG DISPLAY CO., LTD.) 09 March 2018 See paragraphs [0042]-[0067] and figures 3-5.	1-20
A	KR 10-2018-0026610 A (SAMSUNG DISPLAY CO., LTD.) 13 March 2018 See paragraphs [0072]-[0101] and figure 3.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 NOVEMBER 2019 (27.11.2019)	**27 NOVEMBER 2019 (27.11.2019)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex Daejeon Building 4, 189, Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. +82-42-481-8578	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

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Information on patent family members

International application No.
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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