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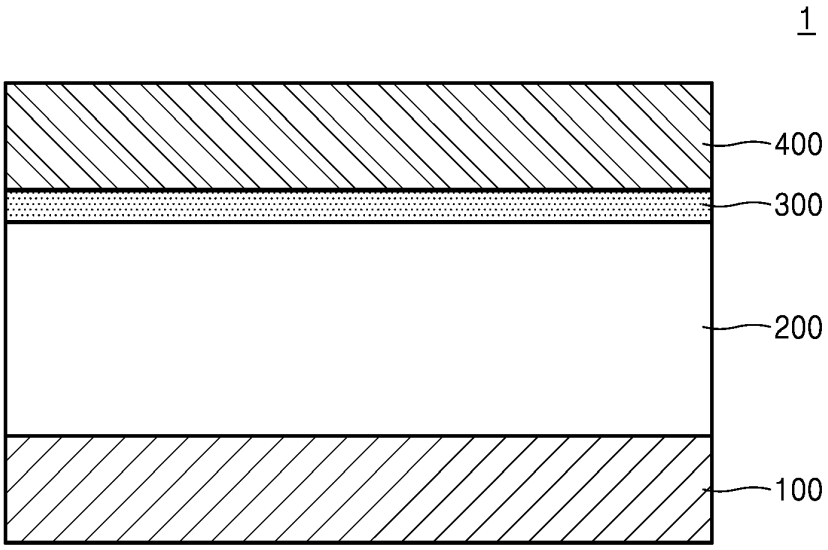
(54) **CAPACITOR COMPRISING DOPED ALUMINUM OXIDE, SEMICONDUCTOR DEVICE INCLUDING THE SAME, AND METHOD OF FABRICATING CAPACITOR**

(57) A capacitor includes: a bottom electrode; a top electrode over the bottom electrode; a dielectric film between the bottom electrode and the top electrode; and a doped Al_2O_3 film between the top electrode and the dielectric film, wherein the doped Al_2O_3 film includes a first dopant, and an oxide including the same element as the first dopant has a higher dielectric constant than a dielectric constant of Al_2O_3.

FIG. 1



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Description

FIELD OF THE INVENTION

[0001] The present disclosure relates to capacitors, semiconductor devices, and methods of fabricating capacitors.

BACKGROUND OF THE INVENTION

[0002] Along with down-scaling of integrated circuit devices, spaces occupied by capacitors have been reduced. Capacitors include top and bottom electrodes and dielectric films between these electrodes and employ dielectric materials having high dielectric constants to exhibit high capacitance. Leakage current may flow through the insides of capacitors. Techniques for reducing and/or minimizing a reduction in capacitance while reducing leakage current flowing through the insides of capacitors may be needed.

SUMMARY OF THE INVENTION

[0003] Provided are capacitors having excellent leakage current blocking properties and having high capacitance.

[0004] Provided are semiconductor devices which include capacitors having excellent leakage current blocking properties and having high capacitance.

[0005] Provided are methods of fabricating capacitors which have excellent leakage current blocking properties and have high capacitance.

[0006] However, the present disclosure is not limited to the aspects set forth above.

[0007] Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of the presented embodiments of the disclosure.

[0008] According to an aspect of an embodiment, a capacitor includes: a bottom electrode; a top electrode over the bottom electrode; a dielectric film between the bottom electrode and the top electrode; and a doped Al_2O_3 film between the top electrode and the dielectric film. The doped Al_2O_3 film includes a first dopant, and an oxide including a same element as the first dopant has a higher dielectric constant than a dielectric constant of Al_2O_3.

[0009] In some embodiments, the first dopant may include one of Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu.

[0010] In some embodiments, the doped Al_2O_3 film may include the first dopant in an amount greater than 0 % and less than 50 at%.

[0011] In some embodiments, the doped Al_2O_3 film may further include a second dopant that is different from the first dopant, and an oxide including a same element as the second dopant may have a higher dielectric constant than the dielectric constant of Al_2O_3.

[0012] In some embodiments, the second dopant may include one of Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu.

[0013] In some embodiments, the first dopant and the second dopant may be present in an amount greater than 0 at % and less than 50 at% in total in the doped Al_2O_3 film.

[0014] In some embodiments, the bottom electrode may directly contact the dielectric film.

[0015] In some embodiments, the capacitor may further include an interfacial film between the bottom electrode and the dielectric film, and the interfacial film may include an oxide including a metal element that is included in the bottom electrode.

[0016] In some embodiments, the bottom electrode may include a metal nitride represented by MM'N, and the interfacial film may include a metal oxynitride represented by MM'ON, wherein M may be a metal element, M' may be an element different from M, N may be nitrogen, and O may be oxygen.

[0017] In some embodiments, the bottom electrode may include carbon impurities in an amount greater than 0 % and less than or equal to 1 %.

[0018] In some embodiments, M may be Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U.

[0019] In some embodiments, M' may be H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U.

[0020] In some embodiments, the metal nitride may be represented by $M_xM'_yN_z$, where $0<x\leq 2$, $0<y\leq 2$, and $0<z\leq 4$ may be satisfied.

[0021] In some embodiments, the dielectric film may have a thickness of greater than 0 nm and less than 5 nanometers (nm), and the doped Al_2O_3 film may have a thickness of greater than 0 nm and less than 2 nm.

[0022] In some embodiments, the top electrode may directly contact a top surface of the doped Al_2O_3 film, and the dielectric film may directly contact a bottom surface of the doped Al_2O_3 film.

[0023] In some embodiments, the top electrode may include TiN, MoN, CoN, TaN, TiAlN, TaAlN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, (Ba,Sr)RuO_3 (BSRO), $CaRuO_3$ (CRO), (La,Sr)CoO_3 (LSCO), or a combination thereof.

[0024] According to an aspect of another embodiment, a semiconductor device includes: a substrate; a gate structure on the substrate; a first source/drain region and a second source/drain region, both arranged in upper portions of the substrate; and a capacitor on the substrate. The capacitor includes a bottom electrode, a top electrode, a dielectric film between the bottom electrode and the top electrode, and a doped Al_2O_3 film between the top electrode and the dielectric film. The bottom electrode is electrically connected to the first source/drain region. The top electrode is over the bottom electrode. The doped Al_2O_3 film includes a first dopant. An oxide including a same element as the first dopant has a higher dielectric constant than a dielectric constant of Al_2O_3.

[0025] In some embodiments, the doped Al_2O_3 film may further include a second dopant that is different from the first dopant. An oxide including a same element as the second dopant may have a higher dielectric constant than the dielectric constant of Al_2O_3.

[0026] In some embodiments, the first dopant and the second dopant may be selected from different elements among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu.

[0027] In some embodiments, the doped Al_2O_3 film may include the first dopant and the second dopant in an amount greater than 0 at % and less than 50 at% in total.

[0028] In some embodiments, the bottom electrode may include a metal nitride represented by MM'N, wherein M may be a metal element, M' may be an element different from M, N may be nitrogen, and O may be oxygen.

[0029] In some embodiments, M may be Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U. M' may be H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U.

[0030] In some embodiments, the metal nitride may be represented by MxM'yNz, where $0<x\leq 2$, $0<y\leq 2$, and $0<z\leq 4$ may be satisfied.

[0031] In some embodiments, the top electrode may directly contact a top surface of the doped Al_2O_3 film, and the dielectric film may directly contact a bottom surface of the doped Al_2O_3 film.

[0032] According to another embodiment, a method of fabricating a capacitor includes: forming a bottom electrode; forming a dielectric film on the bottom electrode; forming a doped Al_2O_3 film on the dielectric film; and forming a top electrode on the doped Al_2O_3 film. The doped Al_2O_3 film includes a first dopant. An oxide including a same element as the first dopant has a higher dielectric constant than a dielectric constant of Al_2O_3.

[0033] In some embodiments, the forming the doped Al_2O_3 film may include forming an Al_2O_3 film on the dielectric film and performing a heat treatment on the dielectric film and the Al_2O_3 film. The dielectric film may include an oxide of an element that is the same as the first dopant. The performing the heat treatment may include diffusing the element that is the same as the first dopant from the dielectric film into the Al_2O_3 film by the heat treatment to provide the doped Al_2O_3 film by the heat treatment to provide the doped Al_2O_3 film. The first dopant may be Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, or Lu.

[0034] In some embodiments, the forming the doped Al_2O_3 film may include: depositing Al, O, and a same element as the first dopant on the dielectric film by an in-situ process, wherein the same element as the first dopant may be Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, or Lu.

[0035] In some embodiments, the doped Al_2O_3 film may further include a second dopant that is different from the first dopant, and an oxide including a same element as the second dopant may have a higher dielectric constant than the dielectric constant of Al_2O_3.

[0036] In some embodiments, the forming the doped Al_2O_3 film may include: forming an additional oxide film on the dielectric film; forming an Al_2O_3 film on the additional oxide film, performing a heat treatment. The heat treatment may be performed on the dielectric film, the additional oxide film, and the Al_2O_3 film. The dielectric film and the additional oxide film may respectively include oxides including two different elements selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu. The two elements, which are selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu and are respectively in the dielectric film and the additional oxide, may be diffused into the Al_2O_3 film by the heat treatment. The first dopant and the second dopant may be respectively the two elements selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu and diffused into the Al_2O_3 film.

[0037] In some embodiments, the doped Al_2O_3 film may include the first dopant and the second dopant in an amount greater than 0 at % and less than 50 at% in total.

[0038] In some embodiments, the forming the bottom electrode may include: arranging a substrate in a reaction

chamber; supplying a first source including a metal organic ligand into the reaction chamber; performing a first purging for removing an organic ligand of the first source that is not adsorbed onto the substrate; supplying a second source including a halogen compound into the reaction chamber; performing second purging for removing the organic ligand that has not reacting with the second source; and supplying a nitridant into the reaction chamber.

[0039] In some embodiments, the metal organic ligand may be represented by MR_x (where M may be a metal element, M, and R may be an organic ligand), wherein x may be in a range of $0 < x \leq 6$.

[0040] In some embodiments, M may be Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U.

[0041] In some embodiments, R may include at least one of a C1-C10 alkyl group, a C2-C10 alkenyl group, a carbonyl group (C=O), a halide, a C6-C10 aryl group, a C6-C10 cycloalkyl group, a C6-C10 cycloalkenyl group, (C=O)R (where R is hydrogen or a C1-C10 alkyl group), a C1-C10 alkoxy group, a C1-C10 amidinate, a C1-C10 alkylamide, a C1-C10 alkylimide, -N(Q)(Q') (where Q and Q' are each independently a C1-C10 alkyl group or hydrogen), Q(C=O)CN (where Q is hydrogen or a C1-C10 alkyl group), and a C1-C10 β-diketonate.

[0042] In some embodiments, halogen compound may be represented by $M'A_y$ (where y is a real number greater than 0 and A may be a halogen element. M' may be H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U.

[0043] In some embodiments, A may include at least one of F, Cl, Br, and I, and y may be in a range of $0<y\leq6$.

[0044] In some embodiments, the supplying the first source, the supplying the second source, and the supplying the nitridant may be performed using an atomic layer deposition (ALD) process.

[0045] In some embodiments, the nitridant may include at least one of NH_3, N_2H_2, N_3H, and N_2H_4.

[0046] In some embodiments, the method set forth above may further include performing a heat treatment for removing the halogen element of the halogen compound, the halogen element remaining as a reaction by-product.

[0047] In some embodiments, the bottom electrode may include carbon impurities in an amount greater than 0 % and less than or equal to 1 %.

[0048] According to an embodiment, a capacitor includes a bottom electrode; a top electrode over the bottom electrode; a dielectric film between the bottom electrode and the top electrode; and a doped Al_2O_3 film between the top electrode and the dielectric film. The doped Al_2O_3 film may include a first dopant. An oxide of first dopant may have a dielectric constant that is higher than a dielectric constant of Al_2O_3.

[0049] In some embodiments, the doped Al_2O_3 film may further include a second dopant that is different from the first dopant. An oxide of second dopant may have a dielectric constant that is higher than a dielectric constant of Al_2O_3, The first dopant and the second dopant may be different elements among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, or Lu. The dielectric film may include an oxide of the first dopant, an oxide of the second dopant, or both the oxide of the first dopant and the oxide of the second dopant.

[0050] In some embodiments, the dielectric film may include a first region and a second region. The first region may include the oxide of the first dopant. The second region may include the oxide of the second dopant. The second region of the dielectric film may be between the first region of the dielectric film and the doped Al_2O_3 film.

[0051] In some embodiments, a semiconductor device may include one of the above-described capacitors.

[0052] In some embodiments, a semiconductor device may include one of the above-described capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0053] The above and other aspects, features, and effects of certain embodiments of the disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a capacitor according to an example embodiment;
FIG. 2 illustrates normalized capacitance change graphs;
FIG. 3 illustrates leakage current change graphs;
FIG. 4 is a cross-sectional view of a capacitor according to an example embodiment;
FIG. 5 is a cross-sectional view of a semiconductor device according to an example embodiment;
FIG. 6 is a cross-sectional view of a semiconductor device according to an example embodiment;
FIG. 7 is a cross-sectional view illustrating a method of fabricating the capacitor of FIG. 1;
FIG. 8 is a cross-sectional view illustrating a method of fabricating the capacitor of FIG. 1;
FIG. 9 is a cross-sectional view illustrating a method of fabricating the capacitor of FIG. 1;
FIG. 10 is a flowchart illustrating a method of manufacturing a bottom electrode that includes a metal nitride represented by MM'N;
FIG. 11A is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;

FIG. 11B is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 11C is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 11D is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 11E is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 11F is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 11G is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 11H is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10;
FIG. 12 is a schematic diagram for an electronic device including a capacitor according to some embodiments; and
FIG. 13 is a schematic diagram of a memory system including a capacitor according to some embodiments.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0054] Reference will now be made in detail to embodiments, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. In this regard, the present embodiments may have different forms and should not be construed as being limited to the descriptions set forth herein. Accordingly, the embodiments are merely described below, by referring to the figures, to explain aspects. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. For example, "at least one of A, B, and C," "at least one of A, B, or C," "one of A, B, C, or a combination thereof," and "one of A, B, C, and a combination thereof," respectively, may be construed as covering any one of the following combinations: A; B; A and B; A and C; B and C; and A, B, and C."

[0055] Hereinafter, embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. Like components will be denoted by like reference numerals throughout the specification, and in the drawings, the size of each component may be exaggerated for clarity and convenience of descriptions. It should be understood that embodiments described below are provided for illustrative purposes only and that various changes and modifications can be made to these embodiments.

[0056] It will be understood that, when an element is referred to as being placed "on" another element, it can be directly placed on the other element, or an intervening layer(s) may also be present.

[0057] As used herein, the singular terms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be understood that the terms such as "comprises", "comprising", "includes", "including", "has", and "having", when used herein, specify the presence of stated components, but do not preclude the presence or addition of other components, unless clearly stated otherwise.

[0058] As used herein, the terms "part," "module," and the like refer to a unit for performing at least one function or operation, and such a unit may be implemented by hardware, software, or a combination of hardware and software.

[0059] FIG. 1 is a cross-sectional view of a capacitor according to an example embodiment.

[0060] Referring to FIG. 1, a capacitor 1 may be provided. The capacitor 1 may include a bottom electrode 100, a dielectric film 200, a doped Al_2O_3 film 300, and a top electrode 400. A material of the bottom electrode 100 may be selected to secure conductivity for use as an electrode and to maintain stable capacitance performance even after a high temperature process during a process of fabricating the capacitor 1.

[0061] In an example, the bottom electrode 100 may include a metal, a metal nitride, a metal oxide, or a combination thereof. For example, the top electrode 400 may include TiN, MoN, CoN, TaN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, $(Ba,Sr)RuO_3$ (BSRO), $CaRuO_3$ (CRO), $(La,Sr)CoO_3$ (LSCO), or a combination thereof.

[0062] For example, the bottom electrode 100 may include a metal nitride represented by MM'N. Here, M is a metal element, M' is an element that is different from M, and N is nitrogen. The metal nitride, that is, MM'N, which constitutes the bottom electrode 100, may also be described as being obtained by doping a metal nitride, MN, with an element, M'. M', which is an element different from M, may be a metal, but is not limited thereto, and may be a material other than a metal.

[0063] M may be one of Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, TI, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, and U.

[0064] M' may be one of H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, TI, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, and U. When a composition ratio of M to M' to N in the metal nitride, MM'N, is x:y:z (e.g., the metal nitride may be $M_xM'_yN_z$), $0<x\leq 2$, $0<y\leq 2$, and $0<z\leq 4$ may be satisfied. Electrical properties as well as electrical conductivity of the capacitor 1 may vary depending upon the composition ratio. The composition ratio is a factor that also influences a material composition of an interfacial film 500 (see FIG. 4), and this is because the interfacial film 500 is a main cause of a change in capacitance according to bias voltages. The composition ratio may vary according to specific selections of M and M'.

[0065] In an atomic layer deposition (ALD) process generally used to manufacture a metal nitride, as a source of a

metal material, a metal organic ligand material is used as a precursor. Here, when an organic ligand is not sufficiently removed after the metal material is applied onto a target surface, carbon impurities are included in a metal nitride film, and this may be a cause of deterioration in performance of a capacitor. In the capacitor 1 according to an embodiment, as described above, the metal nitride, MM'N, is used as a material of the bottom electrode 100, and according to a manufacturing method described below, the metal nitride, MM'N, having almost no carbon impurities is employed for the bottom electrode 100. The bottom electrode 100 may include carbon in an amount of 1 % or less and greater than 0 %.

[0066] The dielectric film 200 may be arranged on the bottom electrode 100. The dielectric film 200 may directly contact the bottom electrode 100. The dielectric film 200 may include a material capable of implementing desired capacitance. Along with increasing degrees of integration of integrated circuit devices including the capacitor 1, a space occupied by the capacitor 1 gradually decreases, and thus, a dielectric having a high dielectric constant may be used. The dielectric film 200 may include a high-dielectric constant (high-k) material. A high dielectric constant denotes a dielectric constant that is higher than the dielectric constant of silicon oxide. The dielectric film 200 may include a metal oxide including at least one metal selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu. For example, the dielectric film 200 may include HfO_2, ZrO_2, CeO_2, La_2O_3, Ta_2O_3, or TiO_2. Although the dielectric film 200 may have a single-layer structure as illustrated, the dielectric film 200 is not limited thereto and may have a multilayer structure. The dielectric film 200 may have a thickness allowing desired capacitance to be implemented. For example, the dielectric film 200 may have a thickness less than 5 nm.

[0067] The doped Al_2O_3 film 300 may be arranged on the dielectric film 200. The doped Al_2O_3 film 300 may block or reduce flow of leakage current between the top electrode 400 and the bottom electrode 100. That is, the doped Al_2O_3 film 300 may be a leakage current reducing layer. In an example, the doped Al_2O_3 film 300 may include a first dopant. The first dopant may be determined such that a dielectric constant of an oxide including the same element as the first dopant is higher than the dielectric constant of Al_2O_3. For example, the first dopant may be one selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu. The doped Al_2O_3 film 300 may include the first dopant in an amount less than 50 at%. In an example, the doped Al_2O_3 film 300 may further include a second dopant that is different from the first dopant. The second dopant may be determined such that a dielectric constant of an oxide including the same element as the second dopant is higher than the dielectric constant of Al_2O_3. For example, the second dopant may be one selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu. In the doped Al_2O_3 film 300, the first dopant and the second dopant may be present in an amount less than 50 at% in total. The doped Al_2O_3 film 300 is not limited to including, as a dopant, only one type of element or two types of elements. In another example, the doped Al_2O_3 film 300 may further include at least one type of dopant that is different from the first and second dopants. For example, the doped Al_2O_3 film 300 may have a thickness less than 2 nm.

[0068] The top electrode 400 may be arranged on the doped Al_2O_3 film 300. The top electrode 400 may include a metal, a metal nitride, a metal oxide, or a combination thereof. For example, the top electrode 400 may include TiN, MoN, CoN, TaN, TiAlN, TaAlN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, (Ba,Sr)RuO_3 (BSRO), $CaRuO_3$ (CRO), (La,Sr)CoO_3 (LSCO), or a combination thereof.

[0069] Unlike the present disclosure, when an undoped Al_2O_3 film is arranged between the top electrode 400 and the dielectric film 200, although leakage current may be reduced, the capacitance of the capacitor may be reduced. The doped Al_2O_3 film 300 of the present disclosure may limit and/or minimize a reduction in capacitance while having a leakage current blocking property that is similar to that of an undoped Al_2O_3 film.

[0070] Unlike the present disclosure, when an undoped Al_2O_3 film or a doped Al_2O_3 film is arranged between the dielectric film 200 and the bottom electrode 100, crystallinity of the dielectric film 200 may be reduced due to deterioration in induction, performed by the bottom electrode 100, of the crystallinity of the dielectric film 200. Accordingly, the capacitance of the capacitor may be reduced. The doped Al_2O_3 film 300 of the present disclosure may be arranged between the dielectric film 200 and the top electrode 400 and thus may not reduce the crystallinity of the dielectric film 200. Accordingly, the capacitance of the capacitor may not be reduced.

[0071] FIG. 2 illustrates normalized capacitance change graphs. FIG. 3 illustrates leakage current change graphs.

[0072] Referring to FIG. 2, a normalized capacitance change graph ① in the case where the doped Al_2O_3 film 300 was removed from the capacitor 1 of FIG. 1, a normalized capacitance change graph ② of the capacitor 1 of FIG. 1, a normalized capacitance change graph ③ in the case where an undoped Al_2O_3 film, instead of the doped Al_2O_3 film 300, was applied to the capacitor 1 of FIG. 1, and a normalized capacitance change graph ④ in the case where, in the capacitor 1 of FIG. 1, the doped Al_2O_3 film 300 was arranged between the bottom electrode 100 and the dielectric film 200 rather than between the top electrode 400 and the dielectric film 200 are provided.

[0073] As compared with the case where the doped Al_2O_3 film 300 was removed from the capacitor 1 of FIG. 1 (graph ①), there was a greatest reduction in capacitance in the case where, in the capacitor 1 of FIG. 1, the doped Al_2O_3 film 300 was arranged between the bottom electrode 100 and the dielectric film 200 rather than between the top electrode 400 and the dielectric film 200 (graph ④).

[0074] In the case where an undoped Al_2O_3 film, instead of the doped Al_2O_3 film 300, was applied to the capacitor 1 of FIG. 1 (graph ③), the reduction in capacitance was smaller than in the case where, in the capacitor 1 of FIG. 1, the

doped Al_2O_3 film 300 was arranged between the bottom electrode 100 and the dielectric film 200 rather than between the top electrode 400 and the dielectric film 200 (graph ④).

[0075] In the case of the capacitor 1 of FIG. 1 (graph ②), the reduction in capacitance was smallest.

[0076] Referring to FIG. 3, a leakage current change graph ⓐ in the case where the doped Al_2O_3 film 300 was removed from the capacitor 1 of FIG. 1, a leakage current change graph ⓑ of the capacitor 1 of FIG. 1, and a leakage current change graph ⓒ in the case where an undoped Al_2O_3 film, instead of the doped Al_2O_3 film 300, was applied to the capacitor 1 of FIG. 1 are provided.

[0077] As compared with the case where the doped Al_2O_3 film 300 was removed from the capacitor 1 of FIG. 1 (graph ⓐ), the reduction in leakage current in the case of the capacitor 1 of FIG. 1 (graph ⓑ) was similar to the reduction in leakage current in the case where an undoped Al_2O_3 film, instead of the doped Al_2O_3 film 300, was applied to the capacitor 1 of FIG (graph ⓒ).

[0078] The doped Al_2O_3 film 300 of the present disclosure may limit and/or minimize the reduction in capacitance of the capacitor 1 while having a leakage current reducing property similar to that of an undoped Al_2O_3 film.

[0079] FIG. 4 is a cross-sectional view of a capacitor according to an example embodiment. For simplicity of descriptions, substantially the same descriptions as those given with reference to FIG. 1 may be omitted.

[0080] Referring to FIG. 4, a capacitor 2 may be provided. The capacitor 2 may include a bottom electrode 100, an interfacial film 500, a dielectric film 200, a doped Al_2O_3 film 300, and a top electrode 400. The bottom electrode 100, the dielectric film 200, the doped Al_2O_3 film 300, and the top electrode 400 may be respectively and substantially the same as the bottom electrode 100, the dielectric film 200, the doped Al_2O_3 film 300, and the top electrode 400, which have been described with reference to FIG. 1.

[0081] The interfacial film 500 may be arranged between the bottom electrode 100 and the dielectric film 200. The interfacial film 500 may include a metal oxide including a metal element that is included in the bottom electrode 100. When the bottom electrode 100 includes a metal nitride represented by MM'N, the interfacial film 500 may include a metal oxynitride represented by MM'ON. Here, M is a metal element included in the bottom electrode 100, M' is an element included in the bottom electrode 100 and different from M, N is nitrogen, and O is oxygen. Example materials of M and M' may be substantially the same as those described with reference with FIG. 1. The thickness of the interfacial film 500 may be less than the thickness of the bottom electrode 100. The interfacial film 500 may include carbon impurities in an amount of 1 % or less.

[0082] FIG. 5 is a cross-sectional view of a semiconductor device according to an example embodiment. For simplicity of descriptions, substantially the same descriptions as those given with reference to FIG. 1 may be omitted.

[0083] Referring to FIG. 5, a semiconductor device 11 including a substrate 1100, a gate structure 1300, an interlayer dielectric 1400, a contact 1500, and a capacitor 1 may be provided. The substrate 1100 may include a semiconductor substrate. For example, the substrate 1100 may include a silicon substrate, a germanium substrate, or a silicon-germanium substrate.

[0084] A first source/drain region 1210 and a second source/drain region 1220 may be arranged in upper portions of the substrate 1100. The first and second source/drain regions 1210 and 1220 may be apart from each other in a first direction DR1 that is parallel to a top surface of the substrate 1100. The first and second source/drain regions 1210 and 1220 may be formed by implanting impurities into the substrate 1100.

[0085] The gate structure 1300 may be arranged on the substrate 1100. The gate structure 1300 may be arranged between the first and second source/drain regions 1210 and 1220. The gate structure 1300 may include a gate electrode 1310 and a gate insulating film 1320. The gate electrode 1310 may include a conductive material. For example, the gate electrode 1310 may include a metal or polysilicon.

[0086] The gate insulating film 1320 may be arranged between the gate electrode 1310 and the substrate 1100. The gate insulating film 1320 may electrically insulate the substrate 1100 from the gate electrode 1310. The gate insulating film 1320 may include a dielectric material. For example, the gate insulating film 1320 may include a Si oxide (for example, SiO_2), an Al oxide (for example, Al_2O_3), or a high-k material (for example, HfO_2).

[0087] The interlayer dielectric 1400 may be arranged on the substrate 1100 to cover the gate structure 1300. The interlayer dielectric 1400 may include an insulating material. For example, the interlayer dielectric 1400 may include a Si oxide (for example, SiO_2), an Al oxide (for example, Al_2O_3), or a high-K material (for example, HfO_2).

[0088] The capacitor 1 may be arranged on the interlayer dielectric 1400. The capacitor 1 may include a bottom electrode 100, a top electrode 400, a dielectric film 200, and a doped Al_2O_3 film 300. The bottom electrode 100, the top electrode 400, the dielectric film 200, and the doped Al_2O_3 film 300 may be respectively and substantially the same as the bottom electrode 100, the top electrode 400, the dielectric film 200, and the doped Al_2O_3 film 300, which have been described with reference to FIG. 1.

[0089] The contact 1500 may be arranged between the bottom electrode 100 and the first source/drain region 1210. The contact 1500 may penetrate the interlayer dielectric 1400. The contact 1500 may electrically connect the bottom electrode 100 to the first source/drain region 1210. The contact 1500 may include a conductive material (for example, a metal).

[0090] The doped Al_2O_3 film 300 may limit and/or minimize a reduction in capacitance of a capacitor while having a leakage current blocking property similar to that of an undoped Al_2O_3 film. The capacitor 1 of the present disclosure may include the doped Al_2O_3 film 300 as a leakage current reducing layer. Accordingly, the stability and reliability of the semiconductor device 11 may be improved.

[0091] FIG. 6 is a cross-sectional view of a semiconductor device according to an example embodiment. For simplicity of descriptions, substantially the same descriptions as those given with reference to FIGS. 1, 4, and 5 may be omitted.

[0092] Referring to FIG. 6, a semiconductor device 12 including a substrate 1100, a gate structure 1300, an interlayer dielectric 1400, a contact 1500, and a capacitor 2 may be provided. The substrate 1100, the gate structure 1300, the interlayer dielectric 1400, and the contact 1500 may be respectively and substantially the same as the substrate 1100, the gate structure 1300, the interlayer dielectric 1400, and the contact 1500, which have been described with reference to FIG. 5.

[0093] The capacitor 2 may be arranged on the interlayer dielectric 1400. The capacitor 2 may include a bottom electrode 100, an interfacial film 500, a top electrode 400, a dielectric film 200, and a doped Al_2O_3 film 300. The bottom electrode 100, the top electrode 400, the dielectric film 200, and the doped Al_2O_3 film 300 may be respectively and substantially the same as the bottom electrode 100, the top electrode 400, the dielectric film 200, and the doped Al_2O_3 film 300, which have been described with reference to FIG. 1. The interfacial film 500 may be substantially the same as the interfacial film 500 described with reference to FIG. 4.

[0094] The doped Al_2O_3 film 300 may limit and/or minimize a reduction in capacitance of a capacitor while having a leakage current blocking property similar to that of an undoped Al_2O_3 film. The capacitor 2 of the present disclosure may include the doped Al_2O_3 film 300 as a leakage current reducing layer. Accordingly, the stability and reliability of the semiconductor device 12 may be improved.

[0095] FIG. 7 is a cross-sectional view illustrating a method of fabricating the capacitor of FIG. 1. FIG. 8 is a cross-sectional view illustrating a method of fabricating the capacitor of FIG. 1.

[0096] Referring to FIG. 7, the bottom electrode 100 and the dielectric film 200 may be sequentially formed on a substrate SU in this stated order. The substrate SU may include a semiconductor material pattern, an insulating material pattern, and a conductive material pattern. For example, the substrate SU may include the substrate 1100, the gate structure 1300, the interlayer dielectric 1400, and the contact 1500 of FIGS. 5 and 6.

[0097] The bottom electrode 100 may be formed on the substrate SU by a deposition process. For example, a process of forming the bottom electrode 100 may include a chemical vapor deposition (CVD) process, a physical vapor deposition (PVD) process, or an atomic layer deposition (ALD) process. The bottom electrode 100 may include a metal, a metal nitride, a metal oxide, or a combination thereof. For example, the bottom electrode 100 may include TiN, MoN, CoN, TaN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, (Ba,Sr)RuO_3 (BSRO), $CaRuO_3$ (CRO), (La,Sr)CoO_3 (LSCO), or a combination thereof. A method of manufacturing the bottom electrode 100 when the bottom electrode 100 includes a metal nitride represented by MM'N will be described below in detail.

[0098] The dielectric film 200 may be deposited on the bottom electrode 100. For example, the dielectric film 200 may be formed by a CVD process, a PVD process, or an ALD process. The dielectric film 200 may include a high-k material. For example, the dielectric film 200 may include a metal oxide including at least one metal selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu. For example, the dielectric film 200 may include HfO_2, ZrO_2, CeO_2, La_2O_3, Ta_2O_3, or TiO_2.

[0099] Referring to FIG. 8, an undoped Al_2O_3 film 302 may be formed on the dielectric film 200. The undoped Al_2O_3 film 302 may be formed by a deposition process. For example, the undoped Al_2O_3 film 302 may be formed by a CVD process, a PVD process, or an ALD process.

[0100] During the process of forming the undoped Al_2O_3 film 302, or after the completion of the process of forming the undoped Al_2O_3 film 302, a heat treatment process H may be performed. By the heat treatment process H, a metal element in the dielectric film 200 may be diffused into the undoped Al_2O_3 film 302. For example, at least one selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu, in the dielectric film 200, may be diffused into the undoped Al_2O_3 film 302. The heat treatment process H allows the undoped Al_2O_3 film 302 to be doped with the diffused metal element, thereby forming the doped Al_2O_3 film 300 described with reference to FIG. 1. In other words, the doped Al_2O_3 film 300 may be doped with the diffused metal element. However, a process of forming the doped Al_2O_3 film 300 is not limited to the example set forth above. In another example, elements (aluminum (Al) and oxygen (O)) constituting an Al_2O_3 film and an element (for example, hafnium (Hf) and/or zirconium (Zr)) required to be doped into the Al_2O_3 film may be deposited in situ by an ALD process, thereby forming the doped Al_2O_3 film 300. The doped Al_2O_3 film 300 may include one type of dopant (for example, the first dopant described with reference to FIG. 1).

[0101] Referring again to FIG. 1, the top electrode 400 may be formed on the doped Al_2O_3 film 300. The top electrode 400 may be formed by a deposition process. For example, the top electrode 400 may be formed by a CVD process, a PVD process, or an ALD process. The top electrode 400 may include a metal, a metal nitride, a metal oxide, or a combination thereof. For example, the top electrode 400 may include TiN, MoN, CoN, TaN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, (Ba,Sr)RuO_3 (BSRO), $CaRuO_3$ (CRO), (La,Sr)CoO_3 (LSCO), or a combination thereof.

[0102] The present disclosure may provide a method of fabricating the capacitor 1 that includes the doped Al_2O_3 film 300 including one type of dopant.

[0103] FIG. 9 is a cross-sectional view illustrating a method of fabricating the capacitor of FIG. 1. For simplicity of descriptions, substantially the same descriptions as those given with reference to FIGS. 7 and 8 may be omitted.

[0104] The bottom electrode 100 and the dielectric film 200 may be formed on the substrate SU by substantially the same process as that described with reference to FIG. 7. Referring to FIG. 9, an additional oxide film 200a may be formed on the dielectric film 200. For example, the additional oxide film 200a may be formed by a CVD process, a PVD process, or an ALD process. The additional oxide film 200a may include a high-k material. For example, the additional oxide film 200a may include a metal oxide including at least one metal, which is selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu while not included in the dielectric film 200. For example, the additional oxide film 200a may include HfO_2, ZrO_2, CeO_2, La_2O_3, Ta_2O_3, or TiO_2. The dielectric film 200 and additional oxide film 200a may provide a dielectric film structure where dielectric film 200 is a first region and the additional oxide film 200a is a second region.

[0105] The undoped Al_2O_3 film 302 may be formed on the additional oxide film 200a. The undoped Al_2O_3 film 302 may be formed by a deposition process. For example, the undoped Al_2O_3 film 302 may be formed by a CVD process, a PVD process, or an ALD process.

[0106] During the process of forming the undoped Al_2O_3 film 302, or after the completion of the process of forming the undoped Al_2O_3 film 302, the heat treatment process H may be performed. By the heat treatment process H, a metal element in the dielectric film 200 and a metal element in the additional oxide film 200a may be diffused into the undoped Al_2O_3 film 302. For example, one selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu, in the dielectric film 200, and one selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu, in the additional oxide film 200a, may be diffused into the undoped Al_2O_3 film 302. The heat treatment process H allows the undoped Al_2O_3 film 302 to be doped with the diffused metal elements, thereby forming the doped Al_2O_3 film 300 described with reference to FIG. 1. However, the process of forming the doped Al_2O_3 film 300 is not limited to the example set forth above. In another example, elements (aluminum (Al) and oxygen (O)) constituting an Al_2O_3 film and an element (for example, hafnium (Hf) and/or zirconium (Zr)) required to be doped into the Al_2O_3 film may be deposited in situ by an ALD process, thereby forming the doped Al_2O_3 film 300. The doped Al_2O_3 film 300 of the present disclosure may include two types of dopants (for example, the first dopant and the second dopant, both described with reference to FIG. 1). However, the doped Al_2O_3 film 300 is not limited to including two types of dopants. In another example, the doped Al_2O_3 film 300 may include three or more types of dopants.

[0107] Referring again to FIG. 1, the top electrode 400 may be formed on the doped Al_2O_3 film 300. The top electrode 400 may be formed by a deposition process. For example, the top electrode 400 may be formed by a CVD process, a PVD process, or an ALD process. The top electrode 400 may include a metal, a metal nitride, a metal oxide, or a combination thereof. For example, the top electrode 400 may include TiN, MoN, CoN, TaN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, (Ba,Sr)RuO_3 (BSRO), $CaRuO_3$ (CRO), (La,Sr)CoO_3 (LSCO), or a combination thereof.

[0108] The present disclosure may provide a method of fabricating the capacitor 1 that includes the doped Al_2O_3 film 300 including two types of dopants.

[0109] FIG. 10 is a flowchart illustrating a method of manufacturing a bottom electrode that includes a metal nitride represented by MM'N. FIG. 11A is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11B is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11C is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11D is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11E is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11F is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11G is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10. FIG. 11H is a conceptual diagram illustrating the method of manufacturing a bottom electrode according to FIG. 10.

[0110] Referring to FIGS. 10, 11A, and 11B, the substrate SU may be prepared (S100).The substrate SU may have a target surface on which a bottom electrode is to be formed. The substrate SU may include a semiconductor material pattern, an insulating material pattern, and a conductive material pattern. For example, the substrate SU may include the substrate 1100, the gate structure 1300, the interlayer dielectric 1400, and the contact 1500 of FIGS. 5 and 6.

[0111] The substrate SU may be arranged in a reaction chamber, and then, a first source including a metal organic ligand may be supplied into the reaction chamber (S110).The metal organic ligand may be represented by MRx including a metal element, M, and an organic ligand, R. Here, x may be in a range of $0<x\leq6$. M may be one of Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, and U. R may include at least one of a C1-C10 alkyl group, a C2-C10 alkenyl group, a carbonyl group (C=O), a halide, a C6-C10 aryl group, a C6-C10 cycloalkyl group, a C6-C10 cycloalkenyl group, (C=O)R (where R is

hydrogen or a C1-C10 alkyl group), a C1-C10 alkoxy group, a C1-C10 amidinate, a C1-C10 alkylamide, a C1-C10 alkylimide, -N(Q)(Q') (where Q and Q' are each independently a C1-C10 alkyl group or hydrogen), Q(C=O)CN (where Q is hydrogen or a C1-C10 alkyl group), and a C1-C10 β-diketonate.

[0112] As a process of supplying the first source, an ALD process may be used. The ALD process may be performed at a temperature of about 100 °C to about 500 °C. The process temperature may be set according to the thermal stability of the metal organic ligand. Because a metal organic ligand having low thermal stability may be decomposed at high temperatures, an ALD process for the metal organic ligand having low thermal stability may be performed at a temperature of about 400 °C or less.

[0113] The organic ligand, which is not adsorbed onto the substrate SU, in the metal organic ligand supplied into the reaction chamber may be removed by purging (S120). The purging is a process of discharging, out of the reaction chamber, the organic ligand not involved in a reaction, or the organic ligand that is a by-product after involved in the reaction. An inert gas such as Ar, He, Ne, or the like, or N_2 gas may be used for the purging.

[0114] As shown in FIG. 11B, the metal organic ligand is adsorbed onto the substrate SU.

[0115] The processes of FIGS. 11A and 11B may be represented by the following Chemical Equations (1) and (2).

$$xMR_4 \rightarrow xMR_{4-a} + x^*aR \quad (1)$$

$$xMR_{4-a} + x^*aR \rightarrow xMR_{4-a} \quad (2)$$

[0116] Chemical Equation (2) indicates that the residual ligand component is removed by the purging.

[0117] Next, it may be determined by a control device (not shown) whether additional supply of the source for MR_x is required (S130), and operations S110 and S120 may be repeated as needed.

[0118] Referring to FIGS. 10, 11C, 11D, and 11E, a second source including a halogen compound may be supplied into the reaction chamber (S140). As a process of supplying the second source, an ALD process may be used. The ALD process may be performed at a temperature of about 100 °C to about 500 °C. The process temperature may be set by taking into account the thermal stability of the metal organic ligand adsorbed onto the substrate SU. Because a metal organic ligand having low thermal stability may be decomposed at high temperatures, an ALD process for the halogen compound may be performed at a temperature of about 400 °C or less.

[0119] The halogen compound may be represented by M'Ay (where y is a real number greater than 0) including a halogen element, A. A may include at least one of F, Cl, Br, and I. y may be in a range of $0<y\leq 6$. M' may be one of H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, and U.

[0120] Next, the organic ligand not reacting with the halogen compound may be removed by purging (S150). An inert gas such as Ar, He, Ne, or the like, or N_2 gas may be used for the purging. In this operation, both the halogen compound not involved in a reaction and a reaction by-product may be removed.

[0121] Operation S140 of supplying the second source including the halogen compound and operation S150 of performing the purging are illustrated in FIGS. 11C to 11E and may be represented by the following Chemical Equations (3) to (5).

$$yM'Cl_4 \rightarrow yM'Cl_{4-b} + y^*bCl \quad (3)$$

$$xMR_{4-a} + yM'Cl_{4-b} + y^*bCl \rightarrow xMCl_{4-a} + y\,M'Cl_{4-b} + x^*(4-a)R + ((y^*b-x^*(4-a))/2)Cl_2 \quad (4)$$

$$xMCl_{4-a} + yM'Cl_{4-b} + x^*(4-a)R + ((y^*b-x^*(4-a))/2)Cl_2 \rightarrow xMCl_{4-a} + yM'Cl_{4-b} \quad (5)$$

[0122] In the above Chemical Equations (3) to (5), Cl is given as an example of the halogen element, A, and Chemical Equation (5) indicates that the residual ligand component and the reaction by-product are removed by the purging.

[0123] As shown in FIG. 11E, M supplied from the first source and M' supplied from the second source are adsorbed onto the substrate SU while bonded to the halogen element, A.

[0124] Next, it may be determined whether additional supply of the source for M'Ay is required (S160), and operations S140 and S150 may be repeated as needed.

[0125] Referring to FIGS. 10, 11F, 11G, and 11H, a nitridant may be supplied into the reaction chamber (S170). An ALD process may be used as a process of supplying the nitridant and may be performed at a temperature of about 100 °C to about 500 °C. The nitridant, which is a reaction gas including nitrogen, may include at least one of NH_3, N_2H_2, N_3H, and N_2H_4. The nitridant reacts with M bonded to the halogen element, A, and reacts with M' bonded to the halogen element, A, and a metal nitride film, that is, MM'N, is formed on the substrate SU. Most of a reaction by-product including the halogen element is vaporized due to the process temperature.

[0126] The supply of the nitridant and the reaction due to the nitridant are illustrated in FIGS. 11F to 11H and may be represented by the following Chemical Equation (6).

$$xMCl_{4-a} + yM'Cl_{4-b} + zNH_c \rightarrow M_xM'_yN_z + (z*c)HCl + ((x*(4-a)+y*(4-b)-z*c)/2)Cl_2 \quad (6)$$

[0127] It may be checked whether a metal nitride film 101 is formed to a desired thickness, and operations S110 to S170 may be repeated as needed (S180). The metal nitride film 101 may be the bottom electrode 100 described above.

[0128] In an example, after operation S170 of supplying the nitridant into the reaction chamber, a heat treatment may be additionally performed to remove the halogen element of the halogen compound, the halogen element remaining as a reaction by-product. A temperature of the heat treatment may range from about 200 °C to about 1000 °C.

[0129] In the metal nitride film 101 formed according to the above-described operations, the amount of impurities except for MM'N is extremely low. Because almost all of the organic ligands included in the source used for the formation of MM'N are removed, there are almost no carbon impurities in the metal nitride film 101. This is as shown in the processes according to Chemical Equations (1) to (6). The carbon impurities may be present in an amount of about 1 % or less in the metal nitride film 101 formed according to those processes. On the other hand, according to existing methods, ligands or reaction by-products have no choice but to remain. A metal nitride film has higher resistivity with an increasing amount of impurities and thus is not suitable to function as an electrode. The value of resistivity of the metal nitride film may vary by up to a factor of several hundreds depending upon the amount of impurities. The metal nitride film, MM'N, which is manufactured by the method according to an embodiment and thus includes almost no impurities, may have a low value of resistivity and may be used as an excellent electrode material. In an example, the metal nitride film 101 may be the bottom electrode 100 shown in FIGS. 1, 4, 5, 6, 7, 8, and 9.

[0130] The method of manufacturing a bottom electrode including a metal nitride, according to the present disclosure, does not include directly reacting a metal organic ligand with a nitridant, and thus, the bottom electrode including the metal nitride having better quality may be formed.

[0131] FIG. 12 is a schematic diagram for an electronic device including a capacitor according to some embodiments.

[0132] Referring to FIG. 12, an electronic device 900 according to example embodiments of inventive concepts may be a personal digital assistant (PDA), a laptop computer, a portable computer, a web tablet, a wireless phone, a mobile phone, a digital music player, a cable/wireless electronic device, etc., but is not limited thereto. The electronic device 900 may include a controller 910, an input/output (I/O) device 920 (e.g., a keypad, a keyboard and/or a display), a memory device 930, and a wireless interface unit 940 which are combined with each other through a data bus 950. The controller 910 may be implemented with processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the processing circuitry more specifically may include, but is not limited to, a central processing unit (CPU), a microprocessor, a digital signal processor, a microcontroller or other logic devices. The other logic devices may have a similar function to any one of the microprocessor, the digital signal processor and the microcontroller. The memory device 930 may store, for example, commands performed by the controller 910. Additionally, the memory device 930 may also be used for storing a user data.

[0133] The memory device 930 includes a plurality of memory cells MC. Each of the memory cells MC may include a capacitor C connected to a transistor TR. A word line WL may be connected to a gate of the transistor TR. A bit line BL may be connected one source/drain region of the transistor TR and the capacitor C may be connected to the other source/drain region of the transistor TR. The other end of the capacitor C may be connected to a power supply voltage Vdd. The capacitor C may include the capacitors 1 and/or 2 described in FIGS. 1, 4, 5, and 6 of the present application.

[0134] The electronic device 900 may use the wireless interface unit 940 in order to transmit data to a wireless communication network communicating with a radio frequency (RF) signal or in order to receive data from the network. For example, the wireless interface unit 940 may include an antenna or a wireless transceiver. The electronic device 900 may be used in a communication interface protocol such as a third generation communication system (e.g., CDMA, GSM, NADC, E-TDMA, WCDAM, and/or CDMA2000).

[0135] FIG. 13 is a schematic diagram of a memory system including a capacitor according to some embodiments.

[0136] FIG. 13 is a schematic block diagram illustrating a memory system. Referring to FIG. 13, a memory system 1000 may include a memory device 1010 for storing data and a memory controller 1020. The memory controller 1020 may read or write data from/into the memory device 1010 in response to read/write request of a host 1030. The memory controller 1020 may make an address mapping table for mapping an address provided from the host 1030 (e.g., a mobile device or a computer system) into a physical address of the memory device 1010. The memory controller 1020 may be implemented with processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the processing circuitry more specifically may include, but is not limited to, a central processing unit (CPU), an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), a System-on-Chip (SoC), a programmable logic unit, a microprocessor, application-specific integrated circuit (ASIC), etc. The memory device 1010 may include a plurality of

memory cells MC. Each of the memory cells MC may include a capacitor C connected to a transistor TR, and may have structure that is the same as the memory cell MC described in FIG. 10. The capacitor C may include the capacitors 1 and/or 2 described in FIGS. 1, 4, 5, and 6 of the present application.

[0137] The present disclosure may provide a capacitor having improved properties of leakage current and capacitance.

[0138] The present disclosure may provide a method of fabricating a capacitor having improved properties of leakage current and capacitance.

[0139] The present disclosure may provide a semiconductor device including a capacitor having improved properties of leakage current and capacitance.

[0140] However, the present disclosure is not limited to the above-described aspects.

[0141] It should be understood that embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each embodiment should typically be considered as available for other similar features or aspects in other embodiments. While one or more embodiments have been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope as defined by the following claims.

Claims

1. A capacitor comprising:

a bottom electrode;
a top electrode over the bottom electrode;
a dielectric film between the bottom electrode and the top electrode; and
a doped Al_2O_3 film between the top electrode and the dielectric film,
the doped Al_2O_3 film including a first dopant, and
an oxide including a same element as the first dopant having a higher dielectric constant than a dielectric constant of Al_2O_3.

2. The capacitor of claim 1, wherein the first dopant comprises one of Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu; and/or
wherein the doped Al_2O_3 film comprises the first dopant in an amount greater than 0 at % and less than 50 at%; and/or
wherein the bottom electrode directly contacts the dielectric film; and/or
wherein the dielectric film has a thickness of greater than 0 nm and less than 5 nm, and the doped Al_2O_3 film has a thickness of greater than 0 nm and less than 2 nm; and/or
wherein the top electrode directly contacts a top surface of the doped Al_2O_3 film, and the dielectric film directly contacts a bottom surface of the doped Al_2O_3 film; and/or
wherein the top electrode comprises TiN, MoN, CoN, TaN, TiAlN, TaAlN, W, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, (Ba,Sr)RuO_3 (BSRO), $CaRuO_3$ (CRO), (La,Sr)CoO_3 (LSCO), or a combination thereof; and/or
wherein
the doped Al_2O_3 film further comprises a second dopant that is different from the first dopant, and an oxide comprising a same element as the second dopant has a higher dielectric constant than the dielectric constant of Al_2O_3, preferably:
wherein the second dopant comprises one of Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu, and/or wherein the first dopant and the second dopant are present in an amount greater than 0 at% and less than 50 at% in total in the doped Al_2O_3 film.

3. The capacitor of claims 1 or 2, further comprising:

an interfacial film between the bottom electrode and the dielectric film,
wherein the interfacial film comprises an oxide comprising a metal element that is included in the bottom electrode;
preferably wherein
the bottom electrode comprises a metal nitride represented by MM'N,
the interfacial film comprises a metal oxynitride represented by MM'ON,
M is a metal element,
M' is an element that is different from M,
N is nitrogen, and
O is oxygen.

4. The capacitor of claim 3, wherein the bottom electrode comprises carbon impurities in an amount of greater than 0 % and less than or equal to 1 %; and/or
wherein M is Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U; and/or
wherein M' is H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U; and/or
wherein
the metal nitride is represented by $M_xM'_yN_z$,
$0<x\leq 2$,
$0<y\leq 2$, and
$0<z\leq 4$.

5. A semiconductor device comprising:

a substrate;
a gate structure on the substrate;
a first source/drain region and a second source/drain region, both arranged in upper portions of the substrate; and
the capacitor of any of claims 1-4 on the substrate,
wherein the bottom electrode is electrically connected to the first source/drain region;
preferably wherein
the bottom electrode comprises a metal nitride represented by MM'N,
M is a metal element,
M' is an element that is different from M, and
N is nitrogen.

6. The semiconductor device of claim 5, wherein
M is Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U, and M' is H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U; and/or
wherein,
the metal nitride is represented by $M_xM'_yN_z$,
$0<x\leq 2$,
$0<y\leq 2$, and
$0<z\leq 4$.

7. A method of fabricating a capacitor, the method comprising:

forming a bottom electrode;
forming a dielectric film on the bottom electrode;
forming a doped Al_2O_3 film on the dielectric film, the doped Al_2O_3 film including a first dopant, and an oxide comprising a same element as the first dopant having a higher dielectric constant than a dielectric constant of Al_2O_3; and
forming a top electrode on the doped Al_2O_3 film.

8. The method of claim 7, wherein
the forming the doped Al_2O_3 film comprises forming an Al_2O_3 film on the dielectric film and performing a heat treatment on the dielectric film and the Al_2O_3 film,
the dielectric film comprises an oxide of an element that is the same as the first dopant,
the performing the heat treatment includes diffusing the element that is the same as the first dopant from the dielectric film into the Al_2O_3 film by the heat treatment to provide the doped Al_2O_3 film, and
the first dopant is Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, or Lu; and/or
wherein
the forming the doped Al_2O_3 film comprises depositing Al, O, and a same element as the first dopant on the dielectric

film by an in-situ process, and
the same element as the first dopant is Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, or Lu.

9. The method of claims 7 or 8, wherein
the doped Al_2O_3 film further comprises a second dopant that is different from the first dopant, and
an oxide comprising a same element as the second dopant has a higher dielectric constant than the dielectric constant of Al_2O_3.

10. The method of claim 9, wherein
the forming of the doped Al_2O_3 film comprises forming an additional oxide film on the dielectric film, forming an Al_2O_3 film on the additional oxide film, and performing a heat treatment,
the heat treatment is performed on the dielectric film, the additional oxide film, and the Al_2O_3 film,
the dielectric film and the additional oxide film respectively comprise oxides comprising two different elements selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu,
the two different elements selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu, respectively in the dielectric film and the additional oxide film, are diffused into the Al_2O_3 film by the heat treatment, and
the first dopant and the second dopant are respectively the two elements selected from among Ca, Sr, Ba, Sc, Y, La, Ti, Hf, Zr, Nb, Ta, Ce, Pr, Nd, Gd, Dy, Yb, and Lu and diffused into the Al_2O_3 film; and/or
wherein the doped Al_2O_3 film comprises the first dopant and the second dopant in an amount greater than 0 at % and less than 50 at% in total.

11. The method of any of claims 7-10, wherein the forming of the bottom electrode comprises:

arranging a substrate in a reaction chamber and supplying a first source comprising a metal organic ligand into the reaction chamber;
performing a first purging for removing an organic ligand of the first source that is not adsorbed onto the substrate;
supplying a second source comprising a halogen compound into the reaction chamber;
performing a second purging for removing the organic ligand that has not reacted with the second source; and
supplying a nitridant into the reaction chamber;
preferably wherein
the metal organic ligand is represented by MR_x (where M is a metal element and R is an organic ligand), and x is in a range of $0 < x \leq 6$.

12. The method of claim 11, wherein M is Be, B, Na, Mg, Al, Si, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U; and/or
wherein
R comprises at least one of a C1-C10 alkyl group, a C2-C10 alkenyl group, a carbonyl group (C=O), a halide, a C6-C10 aryl group, a C6-C10 cycloalkyl group, a C6-C10 cycloalkenyl group, (C=O)R (where R is hydrogen or a C1-C10 alkyl group), a C1-C10 alkoxy group, a C1-C10 amidinate, a C1-C10 alkylamide, a C1-C10 alkylimide, -N(Q)(Q') (where Q and Q' are each independently a C1-C10 alkyl group or hydrogen), Q(C=O)CN (where Q is hydrogen or a C1-C10 alkyl group), and a C1-C10 β-diketonate.

13. The method of claims 11 or 12, wherein
the halogen compound is represented by $M'A_y$ (where y is a real number greater than 0 and A is a halogen element), and
M' is H, Li, Be, B, N, O, Na, Mg, Al, Si, P, S, K, Ca, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, As, Se, Rb, Sr, Y, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Ag, Cd, In, Sn, Sb, Te, Cs, Ba, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Tl, Pb, Bi, Po, Fr, Ra, Ac, Th, Pa, or U, preferably wherein A comprises at least one of F, Cl, Br, and I, and y is in a range of $0<y\leq6$; and/or
wherein the supplying the first source, the supplying the second source, and the supplying the nitridant each are performed using an atomic layer deposition (ALD) process; and/or
wherein the nitridant comprises at least one of NH_3, N_2H_2, N_3H, and N_2H_4; and/or
further comprising performing a heat treatment for removing a halogen element of the halogen compound, the halogen element remaining as a reaction by-product; and/or
wherein the bottom electrode comprises carbon impurities in an amount greater than 0 % and less than or equal to 1 %.

14. A capacitor comprising:

a bottom electrode;
a top electrode over the bottom electrode;
a dielectric film between the bottom electrode and the top electrode; and
a doped Al_2O_3 film between the top electrode and the dielectric film,
the doped Al_2O_3 film including a first dopant, an oxide of the first dopant having a dielectric constant that is higher than a dielectric constant of Al_2O_3.

15. A semiconductor device or electronic device comprising:
the capacitor of claim 14.

FIG. 1

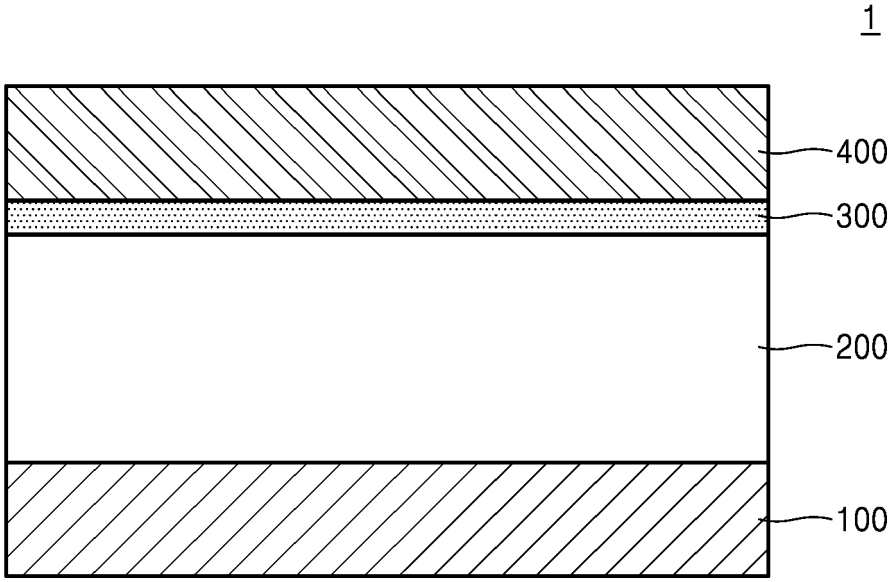


FIG. 2

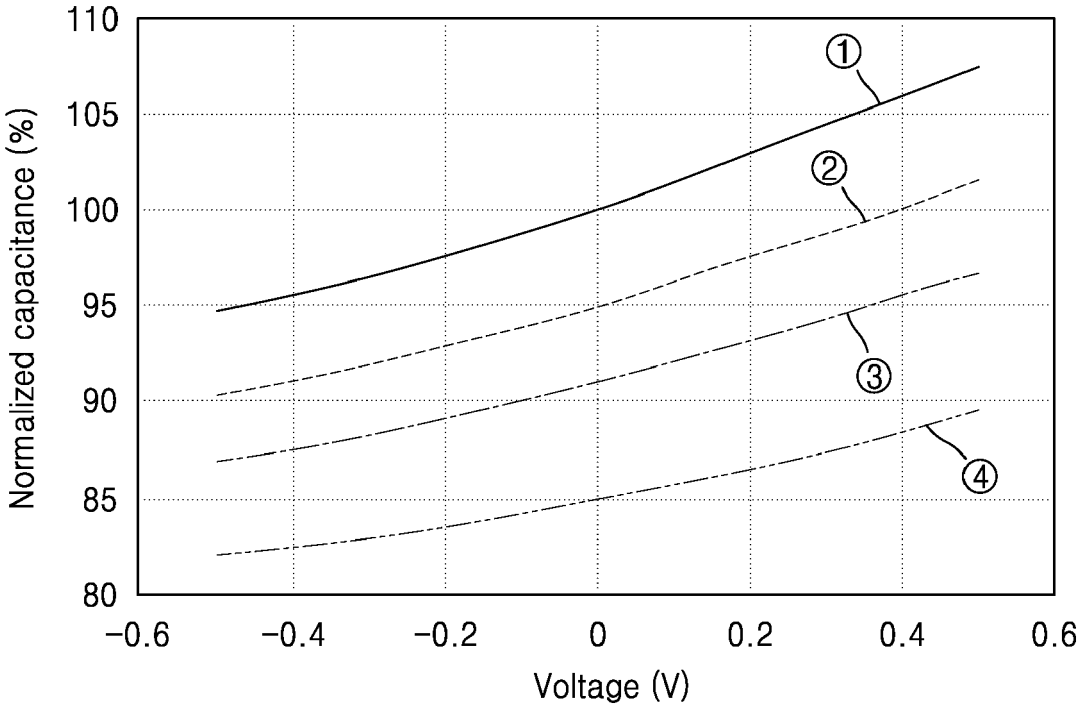

110
105
100
95
90
85
80
Normalized capacitance (%)
−0.6
−0.4
−0.2
0
0.2
0.4
0.6
Voltage (V)
①
②
③
④

FIG. 3

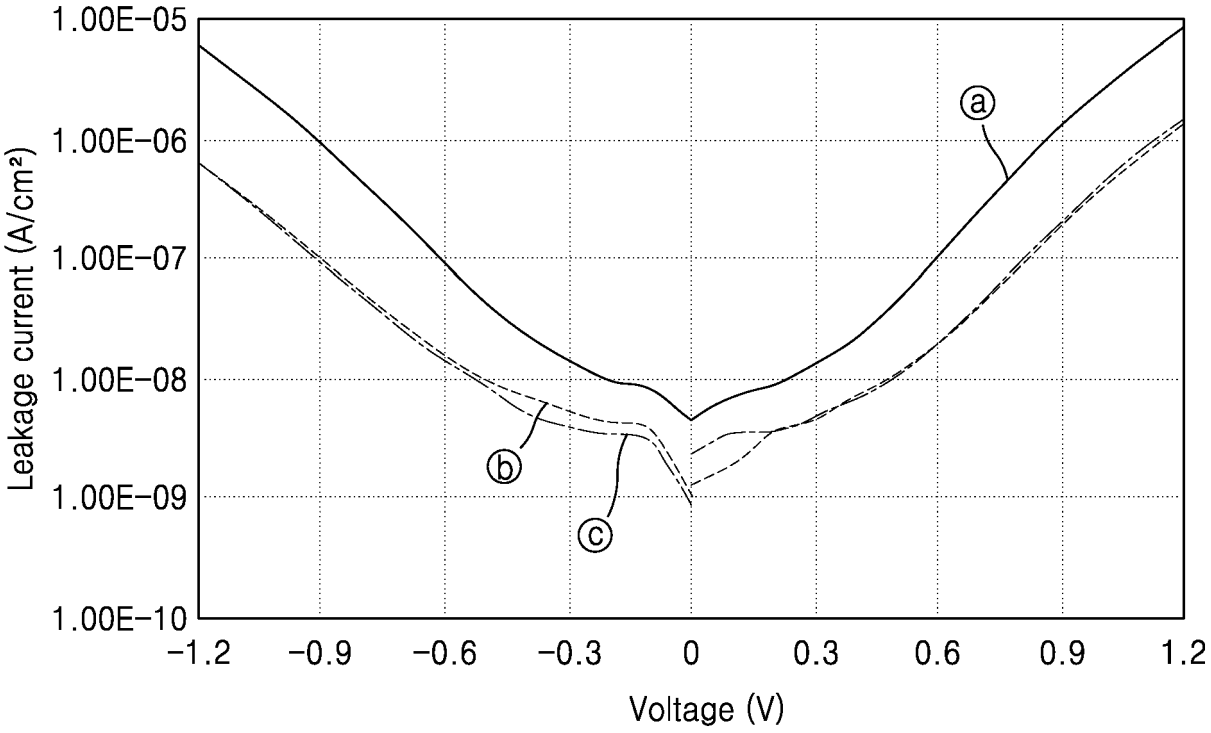

1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
Leakage current (A/cm²)
-1.2
-0.9
-0.6
-0.3
0
0.3
0.6
0.9
1.2
Voltage (V)
ⓐ
ⓑ
ⓒ

FIG. 4

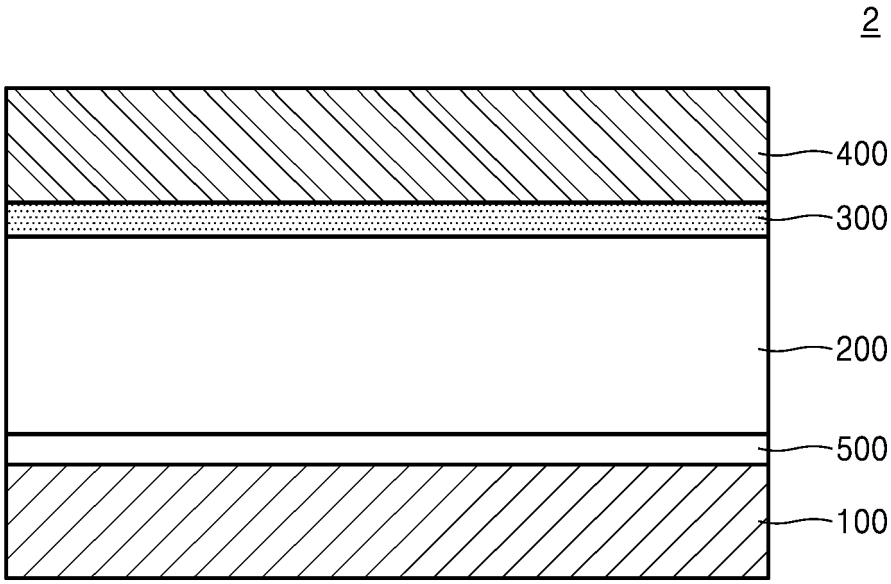


FIG. 5

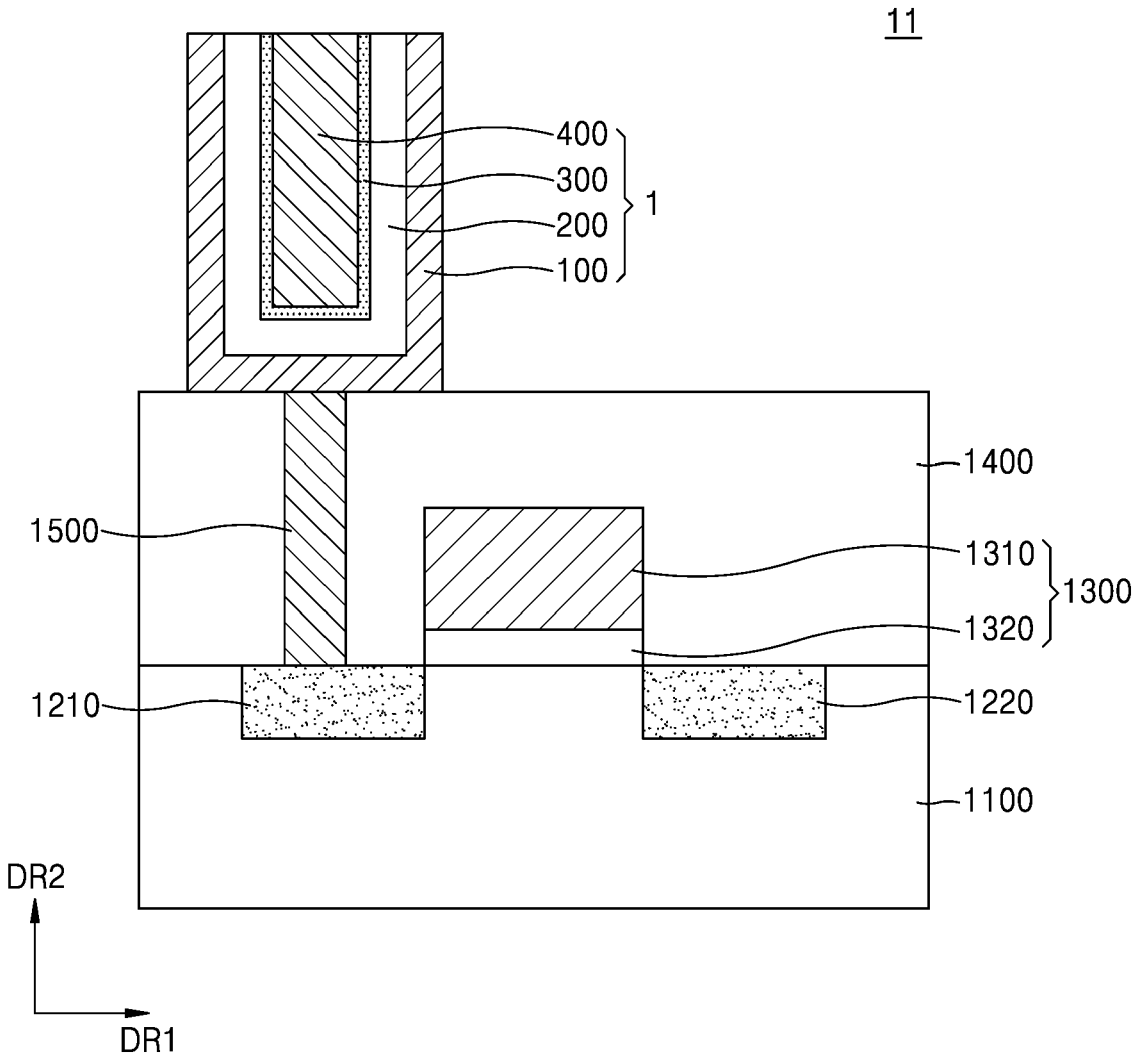

11
400
300
200
100
1
1400
1500
1310
1300
1320
1210
1220
1100
DR2
DR1

FIG. 6

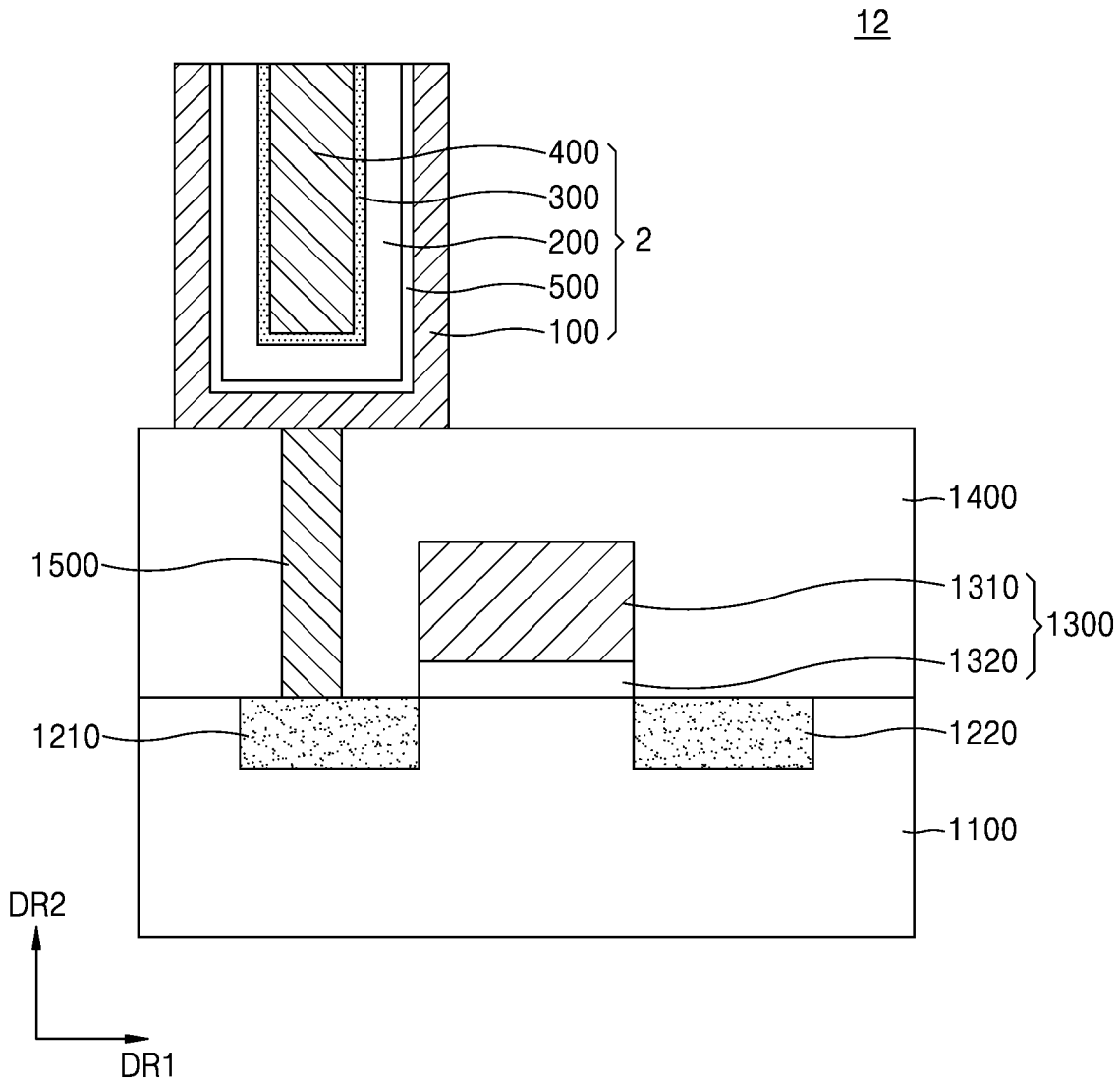

12
400
300
200
500
100
2
1400
1500
1310
1300
1320
1210
1220
1100
DR2
DR1

FIG. 7

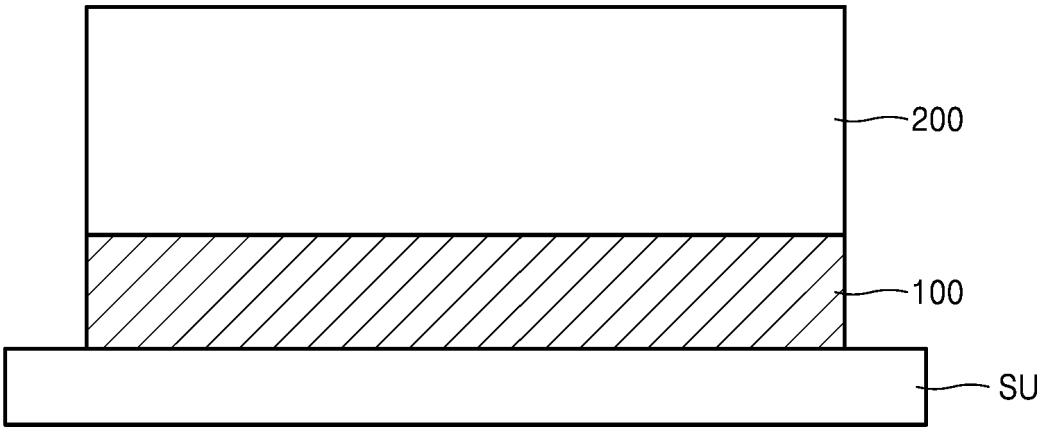


FIG. 8

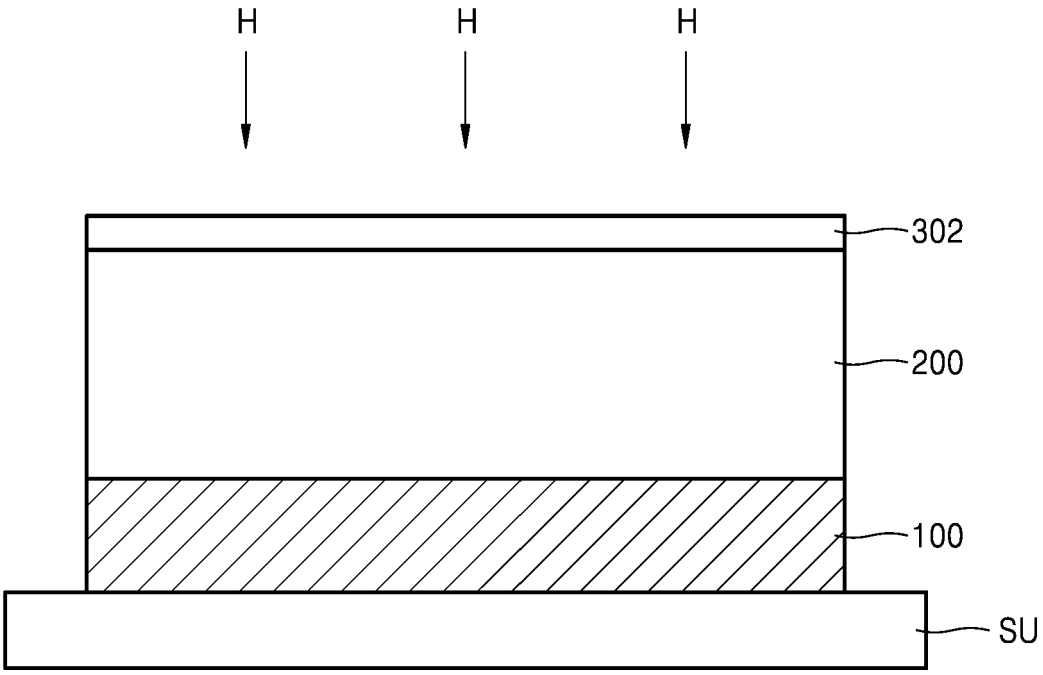


FIG. 9

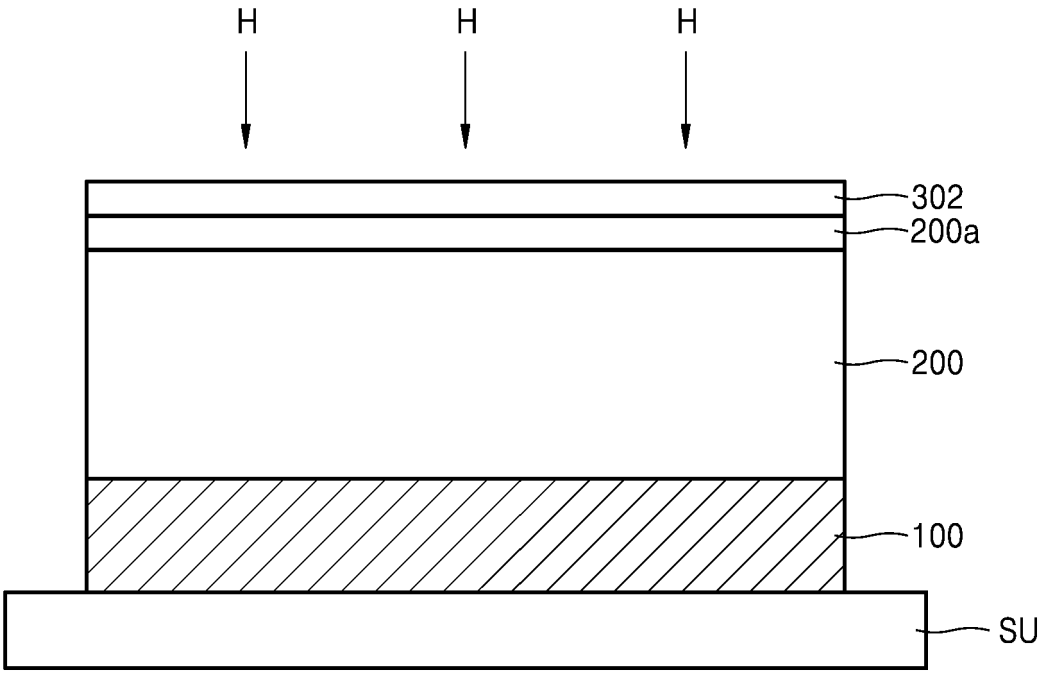


FIG. 10

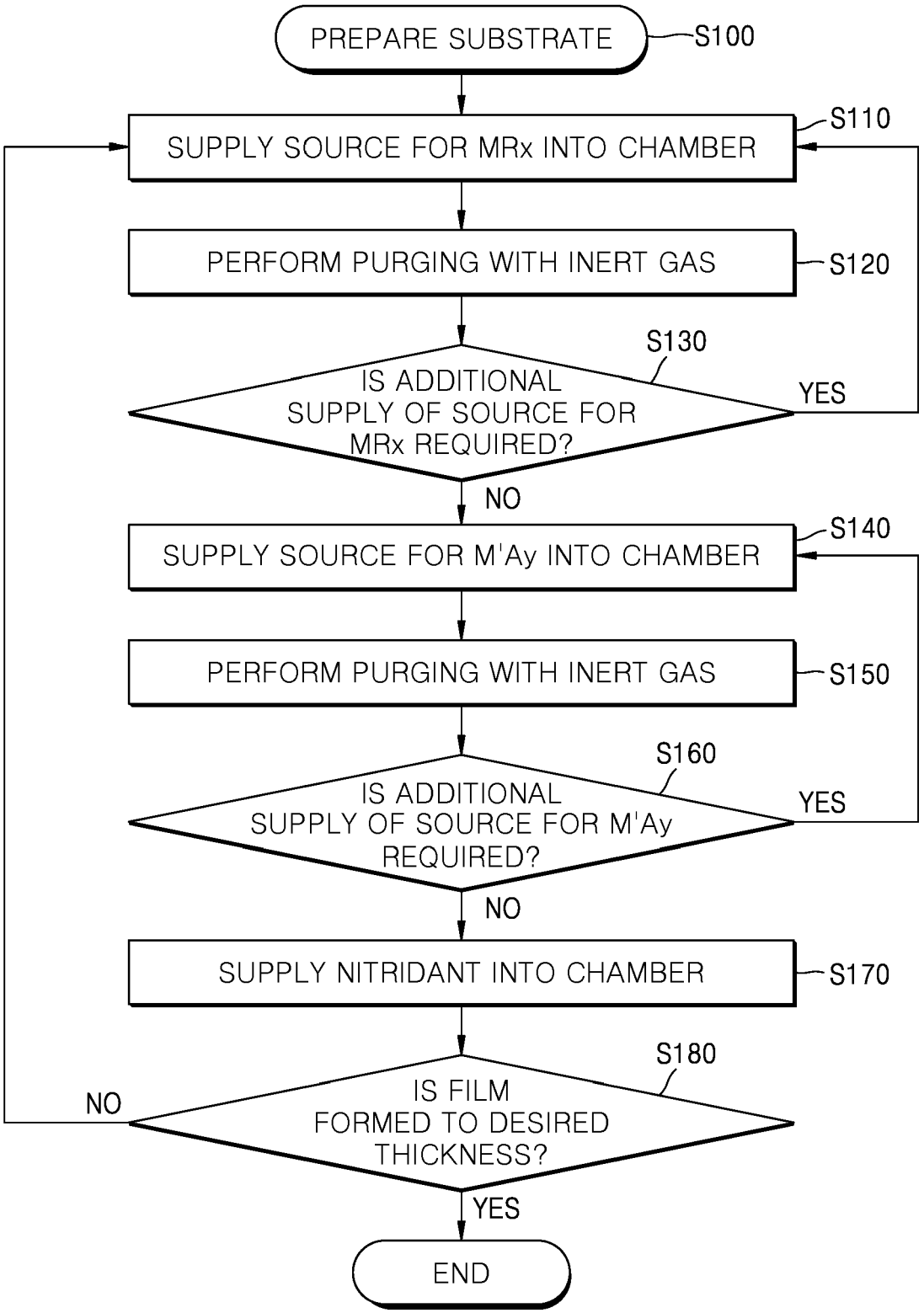

PREPARE SUBSTRATE
S100
SUPPLY SOURCE FOR MRx INTO CHAMBER
S110
PERFORM PURGING WITH INERT GAS
S120
S130
IS ADDITIONAL SUPPLY OF SOURCE FOR MRx REQUIRED?
YES
NO
SUPPLY SOURCE FOR M'Ay INTO CHAMBER
S140
PERFORM PURGING WITH INERT GAS
S150
S160
IS ADDITIONAL SUPPLY OF SOURCE FOR M'Ay REQUIRED?
YES
NO
SUPPLY NITRIDANT INTO CHAMBER
S170
S180
IS FILM FORMED TO DESIRED THICKNESS?
NO
YES
END

FIG. 11A

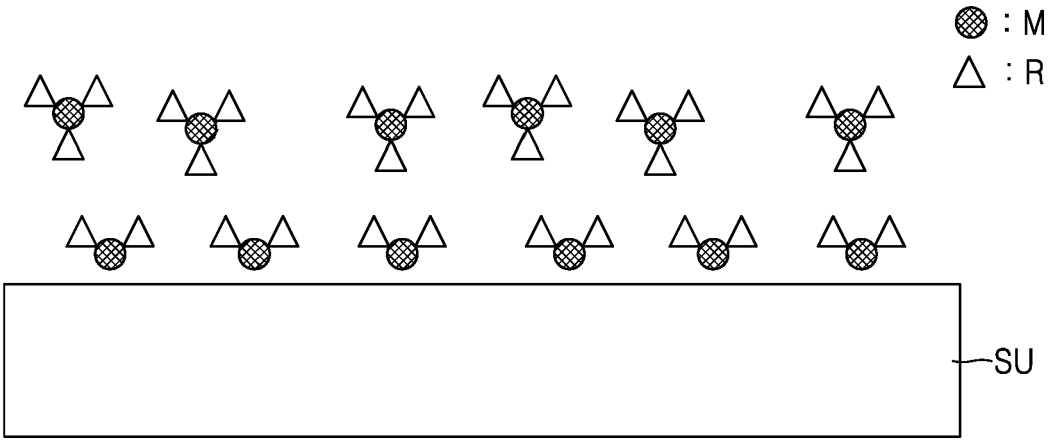


FIG. 11B

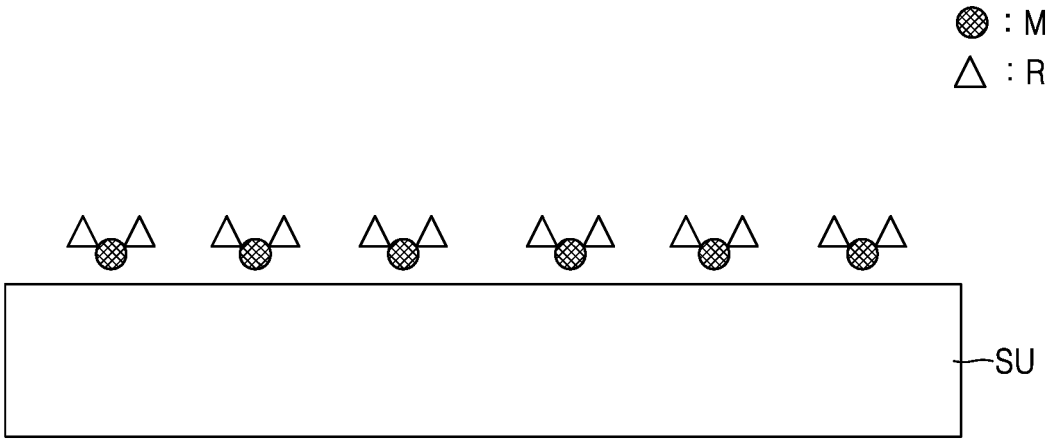


FIG. 11C

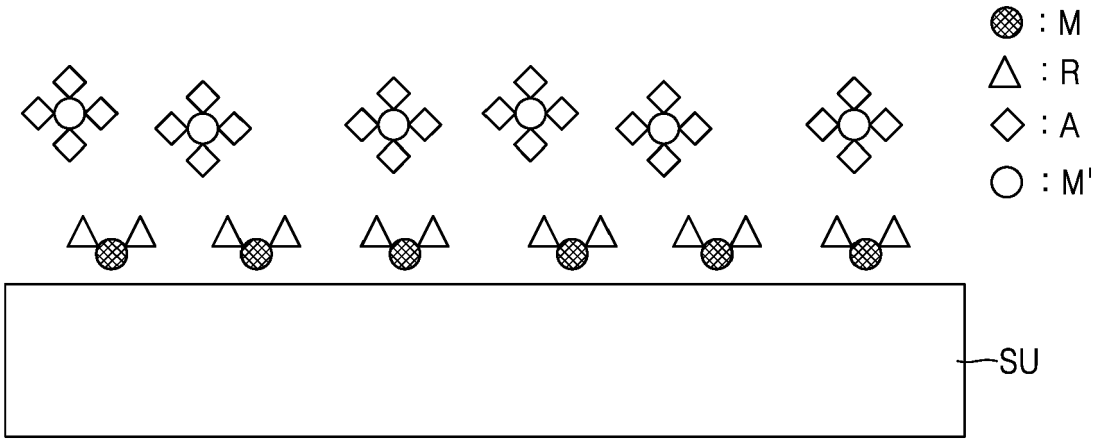


FIG. 11D

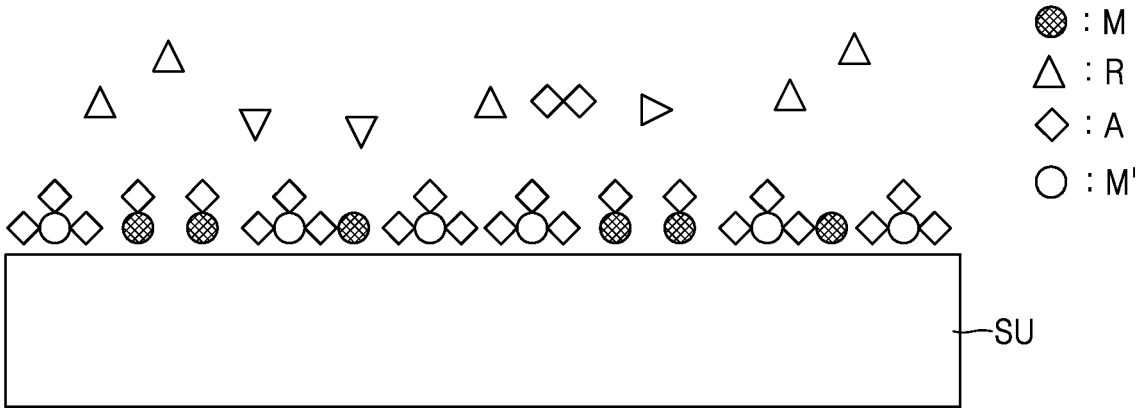


FIG. 11E

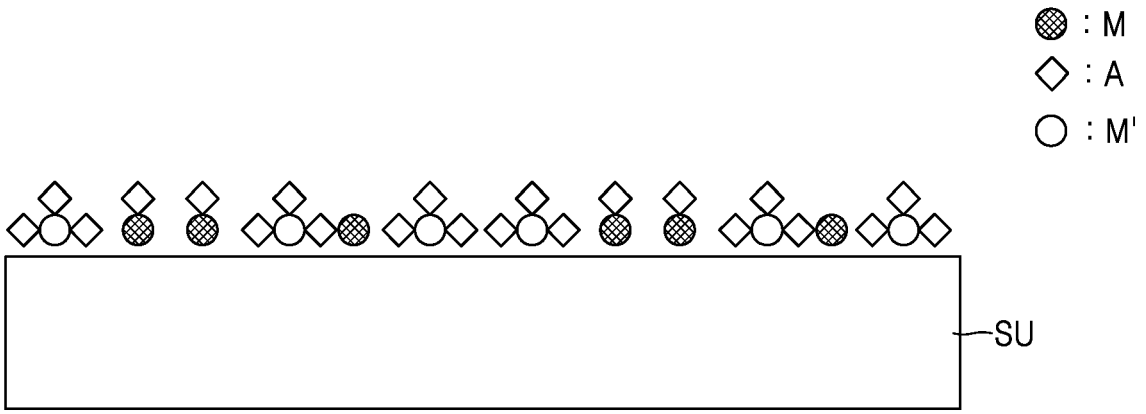


FIG. 11F

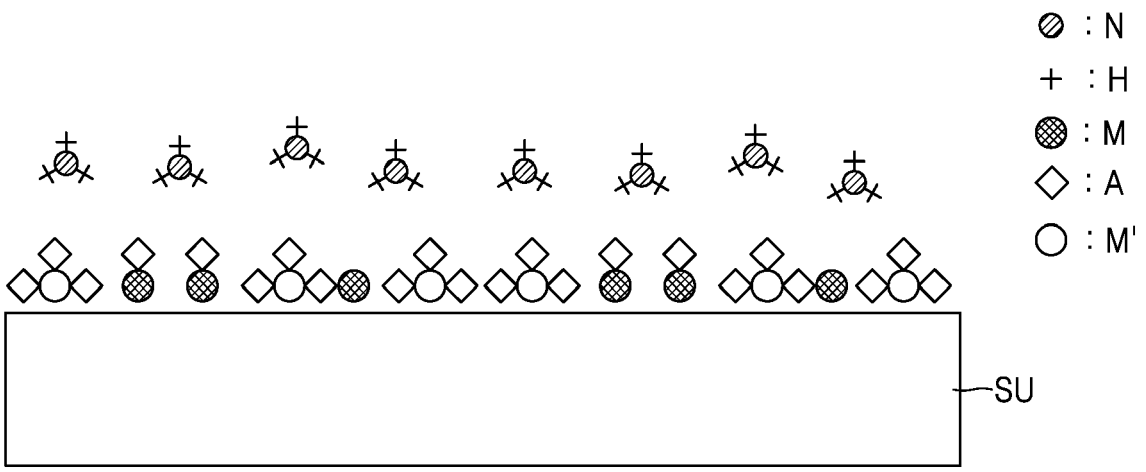


FIG. 11G

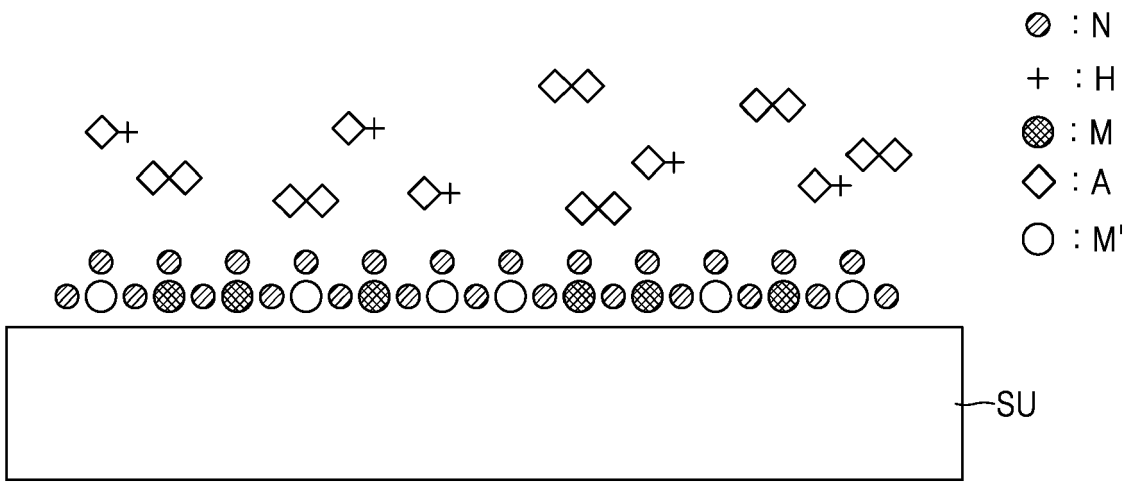


FIG. 11H

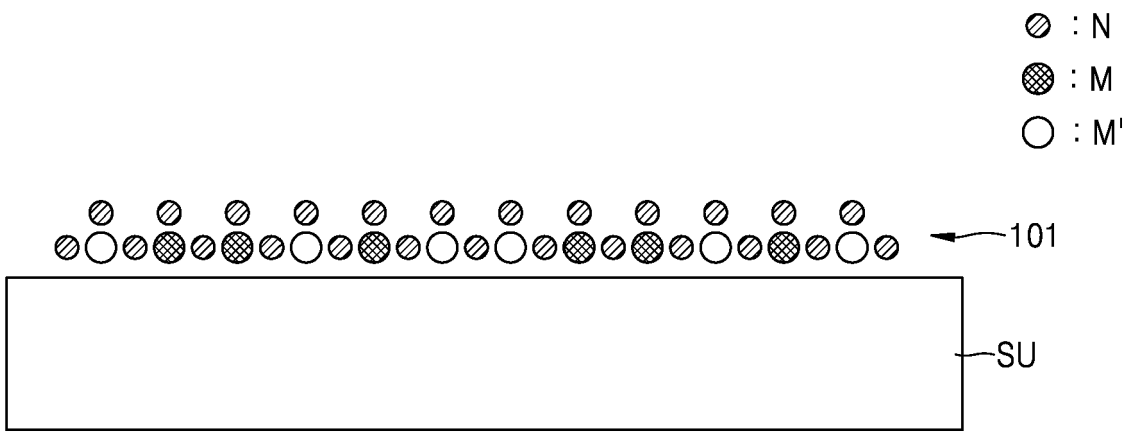


FIG. 12

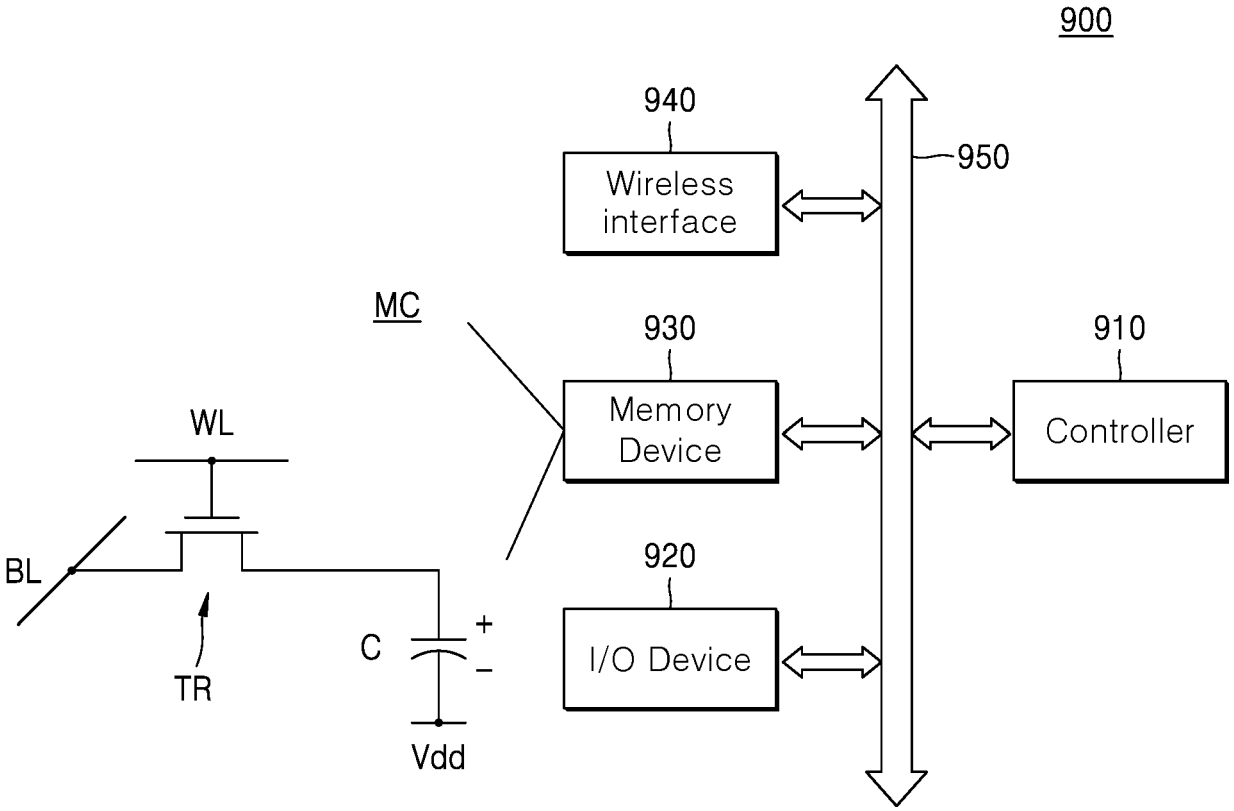
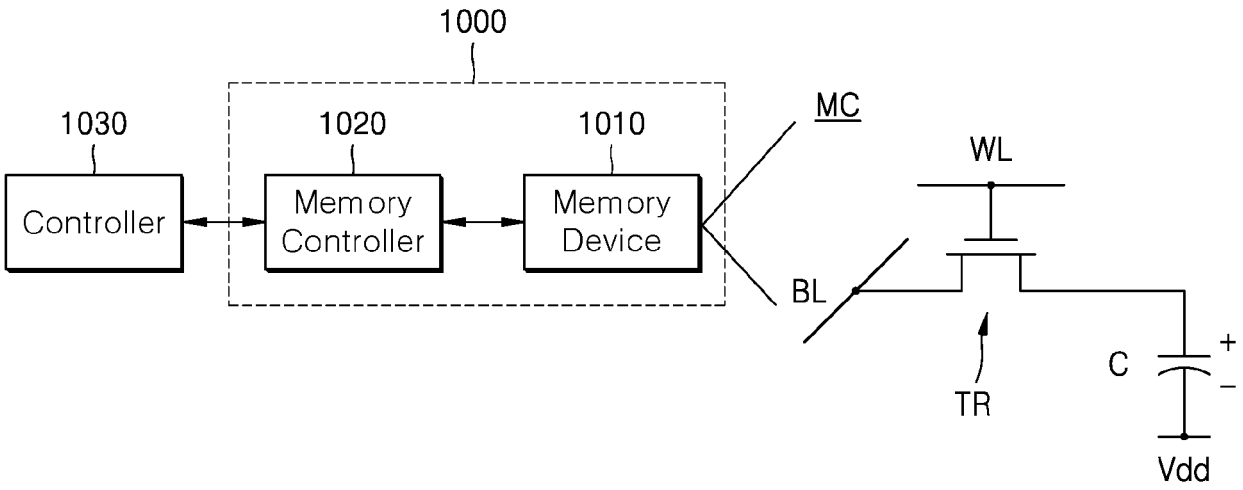

900
940
Wireless interface
950
MC
930
Memory Device
910
Controller
WL
BL
TR
C
+
−
920
I/O Device
Vdd

FIG. 13


1000
1030
1020
1010
Controller
Memory Controller
Memory Device
MC
WL
BL
TR
C
+
−
Vdd

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 21 15 5950

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X Y	KR 100 716 642 B1 (HYNIX SEMICONDUCTOR INC [KR]) 9 May 2007 (2007-05-09) * page 8 - page 10; claims 1,2; figures 4,5 * -----	1,2,5,7, 8,14,15 3,4,6, 9-13	INV. H01L49/02 ADD. H01L27/108
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X Y	US 2003/072126 A1 (BHATTACHARYYA ARUP [US]) 17 April 2003 (2003-04-17) * paragraphs [0051], [0053], [0057] - [0060]; figures 8, 10, 14 * -----	1,14 9,10	
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Place of search	Date of completion of the search	Examiner
Munich	12 July 2021	Mosig, Karsten

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X : particularly relevant if taken alone
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