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(54) **EDGE-EMITTING LASER DIODE WITH IMPROVED POWER STABILITY**

(57) An edge-emitting semiconductor laser diode chip (15) with mutually opposed front and back end facet mirrors (22, 24). First and second ridges (26₁, 26₂) extend between the chip end facets (22, 24) to define first and second waveguides in an active region layer (14). Low and high slope efficiency laser diodes (LD_L, LD_H) are thus formed that are independently drivable by respective electrode pairs (21₁, 23₁ and 21₂, 23₂). The single chip

(15) thus incorporates two laser diodes sharing a common heterostructure, one with low slope efficiency optimized for low power operation with good power stability against temperature variations and random threshold current fluctuations in the close-to-threshold power regime, and the other with high slope efficiency optimized for high wall plug efficiency operation at higher output powers when the chip is operating far above threshold.

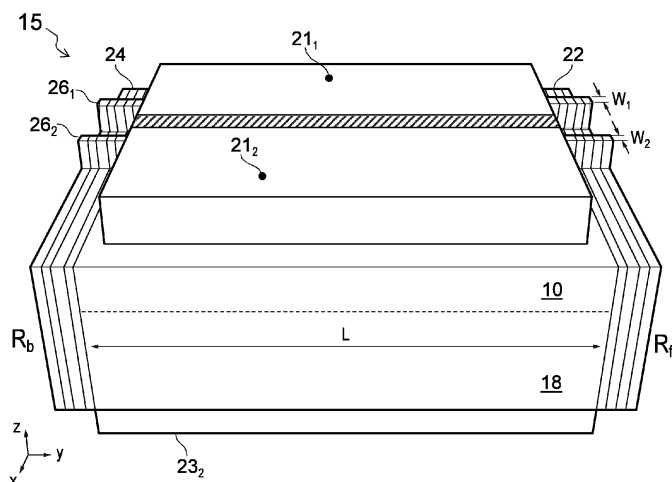


FIG. 13A

Description

BACKGROUND OF THE INVENTION

[0001] The invention relates to an edge-emitting laser diode with improved power stability.

[0002] Edge-emitting semiconductor laser diodes (LDs) are well known sources for visible light (400 nm to 700 nm) in the red, green and blue (RGB) and also in the near infra-red. The term edge-emitting LD is used, since the light is emitted with an optical axis in the plane of the active layer of the semiconductor heterostructure out of a side facet of the device structure. In the following when we refer to LDs we generally mean edge-emitting LDs, not vertical cavity surface emitting lasers (VCSELs), which are also LDs, but with their principal optical axis orthogonal to the layers which makes up the semiconductor heterostructure.

[0003] In recent decades, the main thrust of the development of LDs and related light emitting diodes (LEDs) has been to refine the design of blue and green LDs (and white light emitters) around the gallium nitride materials system, GaAlInN, so that green and blue emitters are available to complement the red emitters that were developed earlier around the GaAlInAsP materials system. Important areas of the development have been to increase power, efficiency, lifetime and reliability. Efficiency is commonly stated as wall plug efficiency (WPE) which is the ratio of output optical power to input electrical power. Current commercially available blue, green and red edge-emitting LDs now show excellent WPE and can be driven stably at high power levels. When integrated in complex light source modules, such LDs typically require the case (i.e. module) temperature to be controlled by means of an active cooling system to improve the power stability against temperature variations.

[0004] For virtual reality and augmented reality applications, high efficiency LDs are needed for RGB projection onto the inside of a visor or goggles or the inside surface of a window, such as a vehicle windscreen/windshield in a car or aircraft. More recently, interest in direct retinal projection has increased for virtual reality and augmented reality applications. In contrast to a classic projection system, or other applications such as telecoms transmitters, lighting and welding, where high power is needed, for direct or close-to-eye projection low power is needed. However, conventional LDs have not traditionally been optimised with low power applications in mind and tend to be relatively unstable when operated at low powers close to threshold.

[0005] Figure 1A shows by way of example the power, P, vs current, I, characteristics of a commercial blue edge-emitting LD emitting at 450 nm and Figure 1B shows its power variation $\Delta P/P$ in the different output regimes induced by threshold current variation from drive pulse to drive pulse (right). As can be seen, at low brightness the random variations in threshold current ΔI_{TH} cause $\pm 50\%$ power (=intensity) fluctuations in the output, whereas at high brightness the intensity fluctuations are only a few percent.

[0006] Figures 2A and 2B show the power vs current, and voltage vs current, characteristics and WPE characteristics of an example commercial blue LD emitting at 450 nm, referred to as Prior Art Example 1. The device shows a slope efficiency of ~ 1.6 W/A and a WPE of $\sim 20\%$ at full brightness (100 mW optical output power). Slope efficiency is the ratio of optical output power, P, to input drive current, I. These values are typical for devices available on the market and represent a good reference target in terms desirable performance in the high brightness power regime.

[0007] Figure 3 shows how the device power-current characteristics, P vs I, of the laser of Figures 2A and 2B change when the module case undergoes a temperature variation between 15° and 60° C. The laser is driven in pulsed mode with a pulse width of 1 microsecond and a 1% duty cycle (DC). As is evident, there is a significant change in threshold current as a function of temperature, whereas the slope efficiency does not vary significantly.

[0008] Figures 4A and 4B summarize the results from Figure 3 by showing the threshold current dependence on case temperature, dI_{th}/dT vs T, and the slope efficiency dependence on case temperature, dP/dI vs T. Assuming that the laser diode is working at a case temperature around 25° C, the relative power variation dependence on current and temperature can be easily determined as:

$$\Delta P_1 = \partial \frac{\partial P}{\partial I} (25^\circ \text{C})$$

$$\Delta P_2 = \frac{\partial P}{\partial T} = \Delta P_1 \times \frac{\partial I}{\partial T} (25^\circ \text{C})$$

[0009] Figure 5A shows for the same blue LD the significant, indeed dramatic, effect of fluctuations in the threshold current on power stability at low output power levels, with the power variation rising to more than 100%/mA in the sub-milliwatt range. Figure 5B shows for the same blue LD the effect of temperature on power stability. For case temperatures in the range 20 - 30° C, the relative power variation induced by temperature will be between less than 1% and a few

percent when working in the high-power regime, but this increases to more than 100% when working in the 100 μ W range. This example shows that precise power control in the low brightness range and, in general, close to threshold is a challenging task.

[0010] A second prior example, Prior Art Example 2, is of a commercially available green LD emitting at 510 nm. The general trends are similar to the blue LD example, but the specific values differ somewhat.

[0011] Figures 6 to 9 correspond to Figures 2 to 5 respectively.

[0012] Figures 10A and 10B show the effects of threshold current variation during pulsed, low power operation for both the blue LD example (Figure 10A) and the green LD example (Figure 10B). The current-power characteristics, P vs I , of the commercial blue and a green LDs are measured multiple times while keeping the same drive conditions and keeping the case temperature at a constant value of 25 °C. A threshold current variation of circa 40 μ A and circa 70 μ A can be observed on the blue and the green emitter respectively. Taking into account the corresponding slope efficiencies (1.6W/A for the blue LD and 0.7 W/A for the green LD), both devices show at a constant drive current a power variation of approximately $\pm 30\%$ with respect to a nominal power output value of 100 μ W. We note these results are with the case temperature being kept constant. The situation if the case temperature is not under good control will of course be worse.

[0013] The above two prior art examples are for blue and green commercially available LDs. Although not reported here, an equivalent analysis on red commercial LDs would lead to similar results and conclusions.

[0014] To address this problem, a low power ridge LD was proposed in US 2018/083422 A1 (now issued as US 10193310 B2) in which the slope efficiency is deliberately lowered. Slope efficiency is lowered by a careful choice of a combination of physical parameters, in particular front facet reflectivity R_f which can be increased to lower slope efficiency (typically $R_f = 0.7$ to 0.95), internal loss α_i which can be increased from its residual value, e.g. by doping, to lower slope efficiency (typically 5-20 cm^{-1}), and cavity length L which can be increased to lower slope efficiency (typically $L = 200$ -600 μm). With lower slope efficiency, the laser operates more stably at low output powers close to threshold, i.e. in the sub-mW output power range, and in particular has an output power that is less sensitive to temperature fluctuations and to random fluctuations in the threshold current each time the device is brought to lase.

[0015] Figure 11A is a graph plotting relative power variation per unit temperature, $\Delta P/dT/P$, as a function of output power, P , for six blue LDs with different slope efficiencies, but otherwise identical design parameters of cavity length, L : 500 μm , internal loss, α_i : 3 cm^{-1} , back reflectivity, R_b : 99%, ridge width, W : 2 μm and front reflectivity, R_f that is varied to vary the slope efficiency with values of: 25%, 70%, 88%, 96%, 97%, 98%, where slope efficiency decreases with increasing R_f . It is apparent how for a given laser (i.e. a given line in the plot) the power stability is good at higher output powers in the tens of mW range but becomes poor at sub-mW output powers. It is also apparent that relative power variation is reduced by reducing the slope efficiency.

[0016] Figure 11B is a corresponding set of curves for five green LDs, where the curves show the same trends. Here the parameter values are L : 1000 μm , α_i : 3 cm^{-1} , R_b : 99%, W : 2 μm , and R_f at values of 40%, 82%, 88%, 94%, 98%, where slope efficiency decreases with increasing R_f . With this prior art design approach, some wall plug efficiency is sacrificed to improve the low-power output stability. However, owing to this compromise, the laser inevitably does not operate with optimum WPEs at higher output powers, e.g. in the range 50-100 mW.

SUMMARY OF THE INVENTION

[0017] According to an aspect of the invention there is provided a laser diode chip comprising:

a plurality of semiconductor layers arranged on a substrate, the semiconductor layers collectively defining an active region layer of higher refractive index sandwiched between upper and lower cladding layers of lower refractive index; mutually opposed front and back end facets on which are formed front and back mirrors; first and second ridges each extending laterally between the front and back end facets and having respective pairs of sides that extend part way to the active region layer to define first and second waveguides in the active region layer; a first laser diode having a first gain medium defined by the first waveguide and which is configured to operate with a first, low slope efficiency; a second laser diode having a second gain medium defined by the second waveguide and which is configured to operate with a second, high slope efficiency, wherein the second slope efficiency is higher than the first slope efficiency; a plurality of electrical contacts configured to allow the first and second laser diodes to be independently driven; and a controller configured to drive the electrical contacts in a first mode of operation to operate the laser diode chip with low slope efficiency for low output powers using the first laser diode, and in a second mode of operation to operate the laser diode chip with high slope efficiency for high output powers using the second laser diode.

[0018] According to this design, it is possible to provide an edge-emitting LD chip with improved power stability against

temperature variations and against random threshold current fluctuations in the close-to-threshold power regime.

[0019] First and second emitters are thus formed by the first and second ridges in the same LD chip that can share the same semiconductor heterostructure, i.e. the plurality of semiconductor layers grown on the substrate. With this design, the first and second laser diodes share a common cavity, since they are based on the same semiconductor heterostructure and since they share the same front and back mirrors. Although a plethora of parameters define the performance of such emitters, we use the parameter space defined by the following parameters to engineer two different slope efficiency emitters in the same chip:

- Chip cavity length, i.e. distance between front and back mirrors, L
- Ridge width, W
- Back mirror reflectivity, R_b
- Front mirror reflectivity, R_f
- Internal loss of gain medium, α_i

[0020] The chip cavity length may, for example, be in the range:

- $300 \mu\text{m} \leq L \leq 2000 \mu\text{m}$

[0021] It is further noted that the slope efficiency does not change significantly with ridge width for typical ridge width values, so we do not distinguish between the ridge width of the first and second ridges, W_1 and W_2 , which may be the same or different, with both typically being in the range 1 - 4 μm .

[0022] The difference between the slope efficiencies can be realized in various different ways within the parameter space, in particular by one or more of the following design approaches:

The difference between the slope efficiencies can be realized at least in part by providing the front mirror of the first, low slope efficiency, laser diode with a higher reflectivity than the front mirror of the second, high slope efficiency, laser diode. For example, the front and back reflectivities may be in the ranges:

- $10\% \leq R_b \leq 100\%$
- $10\% \leq R_f \leq 80\%$

[0023] The difference between the slope efficiencies can be realized at least in part by providing the first waveguide of the first, low slope efficiency, laser diode with a higher internal loss than that of the second waveguide of second, high slope efficiency, laser diode. For example, the respective internal losses of the low and high slope LDs - α_i^H and α_i^L - can be set in the following ranges:

- $0 \text{ cm}^{-1} \leq \alpha_i^H \leq 10 \text{ cm}^{-1}$
- $\alpha_i^H < \alpha_i^L \leq 30 \text{ cm}^{-1}$

[0024] The difference between the slope efficiencies can be realized at least in part by providing the second waveguide of the second, high slope efficiency, laser diode with an intermediate mirror arranged part way between the front end facet and the back end facet so that the second laser diode has a shortened cavity length compared to the first laser diode. For example, the respective cavity lengths of the high and low slope efficiency LDs - L_H and L_L - can be set in the following ranges:

- $300 \mu\text{m} \leq L_H \leq 2000 \mu\text{m}$
- $300 \mu\text{m} \leq L_L \leq 2000 \mu\text{m}$

[0025] The difference between the first and second slope efficiencies can be realized at least in part by providing the first waveguide of the first, low slope efficiency, laser diode with a bend so that it meets the back end facet at a non-orthogonal angle, thereby inducing additional coupling losses for light reflected back into the first waveguide from the back mirror. For example, the non-orthogonal angle may deviate from the orthogonal by an amount in the following range:

- $0 \text{ deg} < \theta \leq 5 \text{ deg}$

[0026] The ridges may be buried or unburied. By buried ridges we refer to the presence of semiconductor material either side of the ridges in an infill region. The infill region may, for example, be fabricated by regrowth after the ridges have been formed by etching. By unburied ridges, we refer to a structure that has no such infill, so the ridges are at the surface of the semiconductor layer stack. The unburied ridges may nevertheless be covered in some other material,

such as a dielectric material for electrical isolation and/or a metal or metallic material for forming an electric contact.

[0027] These designs require at least the above-mentioned first and second ridges. However, it will be understood that multiple ones of either or both of type of ridge may be included in a single chip as an array, e.g. multiple pairs of first and second ridges.

[0028] In examples of the laser diode chip, the second slope efficiency is at least 1.5, 2, 3, 4, 5, 6, 7, 8, 9, 10, or 20 times greater than the first slope efficiency.

[0029] The laser diode chip can be configured to emit in the blue spectral region, the first slope efficiency is less than 0.8 W/A and the second slope efficiency is greater than 1.2 W/A. The laser diode chip can be configured to emit in the green spectral region, the first slope efficiency is less than 0.3 W/A and the second slope efficiency is greater than 0.5 W/A. The laser diode chip can be configured to emit in the red spectral region, the first slope efficiency is less than 0.3 W/A and the second slope efficiency is greater than 0.8 W/A.

[0030] Another aspect of the invention relates to a light module comprising at least one laser diode chip as described above. A still further aspect of the invention relates to a vision system configured to be placed on a human head incorporating such a light module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] This invention will now be further described, by way of example only, with reference to the accompanying drawings.

Figures 1A and 1B show by way of example the power, P , vs current, I , characteristics of an example commercial blue edge-emitting LD

Figures 2A and 2B show the LIV characteristics and WPE characteristics of an example commercial blue LD.

Figure 3 shows the temperature dependence of the power-current characteristics of the blue LD of Figure 2.

Figures 4A and 4B summarize the results from Figure 3 by showing the threshold current dependence on case temperature (Figure 4A) and the slope efficiency dependence on case temperature (Figure 4B).

Figures 5A and 5B are graphs plotting the relative power variation dependence on current and on temperature respectively as a function of output power for the blue LD of Figures 2A and 2B.

Figures 6 to 9 correspond to Figures 2 to 5 respectively for a green edge-emitting LD.

Figure 10A shows the effects of threshold current variation during pulsed operation for the blue LD example of Figures 2 to 5; and Figure 10B shows the effects of threshold current variation during pulsed operation for the green LD example of Figures 6 to 9.

Figure 11A is a graph of relative power variation per unit temperature as a function of output power for otherwise identical blue LDs with different slope efficiencies; and Figure 11B is a graph of relative power variation per unit temperature as a function of output power for otherwise identical green LDs with different slope efficiencies.

Figure 12 shows a semiconductor heterostructure suitable for fabricating a LD chip according to embodiments of the disclosure.

Figure 13A is a schematic perspective drawing of a two-ridge edge-emitting LD chip according to some embodiments of the disclosure; Figure 13B is a schematic plan view of the two-ridge LD chip of Figure 13A; Figure 13C is a schematic perspective drawing of the two-ridge LD chip of Figures 13A & 13B; Figure 13D is a schematic cross-section showing one ridge of the two-ridge LD structure of Figures 13A to 13C; Figure 13E is a schematic perspective drawing of a buried ridge waveguide design comparable to Figure 13C showing a ridge waveguide design;

and Figure 13F is a schematic cross-section of a buried ridge waveguide design comparable to Figure 13D showing a ridge waveguide design.

Figure 14 is a schematic cross-section in more detail than Figure 13D showing the layer structure of an example LD chip with one of the ridges being shown.

Figure 15 is a table showing example materials choices for LD chip fabrication in each of four different materials systems.

Figure 16 shows LI-characteristics of a two-ridge LD chip where one emitter for use at low output powers has low slope efficiency and the other emitter for use at high output powers has high slope efficiency.

Figure 17 is a schematic plan view of a variant of the embodiment of Figures 13-14 with multiple pairs of ridges to provide multiple low slope efficiency LDs and multiple high slope efficiency LDs in an array.

Figures 18A, 18B and 18C are three pairs of graphs showing the parameter space that can be explored by varying the parameters front reflectivity R_f , cavity length L and internal loss α_i .

Figures 19 to 21 show embodiments according to a first design approach based on having different front reflectivities between the low and high slope lasers.

Figures 22 & 23 show embodiments according to a second design approach based on having different internal losses between the low and high slope lasers.

Figures 24 & 25 show embodiments according to a third design approach based on having different cavity lengths between the low and high slope lasers.

Figures 26 to 28 show embodiments according to a fourth design approach based on a tilted waveguide for the low slope laser to induce additional losses on reflection from the back reflector.

Figure 29 is a schematic perspective view of an RGB light module incorporating red, green and blue LDs.

Figure 30 is a schematic drawing of a light source unit including a drive circuit and other components suitable for integration of a three-emitter LD device or module.

Figures 31 & 32 show example near-to-eye projection systems in monocle and spectacles formats.

DETAILED DESCRIPTION

[0032] In the following detailed description, for purposes of explanation and not limitation, specific details are set forth in order to provide a better understanding of the present disclosure. It will be apparent to one skilled in the art that the present disclosure may be practiced in other embodiments that depart from these specific details.

[0033] Figure 12 shows the basic layer structure of a semiconductor heterostructure for a LD chip according to embodiments of the disclosure. This shows the situation prior to post-growth processing, e.g. to form ridges and deposit electrodes. The epitaxial semiconductor layers 10 are an active layer 14 sandwiched between p-type layers 12₁ and 12₂ and n-type layers 16₁ and 16₂, wherein the epitaxial layers 10 are grown on an n-type substrate 18. The heterostructure 10 further includes a p-type capping layer 19 to form a junction to a metallic top contact electrode. The p-type layers 12₁ and 12₂ are a top cladding layer 12₁ and thereunder a waveguide layer 12₂ adjacent the active layer 14. The n-type layers 16₁ and 16₂ are a waveguide layer 16₁ adjacent the active layer 14 and a bottom cladding layer 16₂ thereunder. The two waveguiding layers 12₂ and 16₁ have refractive indices lower than that of the active layer 14 and higher than layers 12₁ and 16₂, so as to support at least one guided mode in the active layer 14 in each of the waveguiding regions. The different layers are made of different materials (heterostructure) to provide the desired band gap profiles and refractive index profiles, as well as other desired properties. The person skilled in the art will know that each of these layers will in fact most likely be made of multiple layers, for example the active layer 14 may be a multi-quantum well (MQW) heterostructure. Quantum dots or other reduced dimensional structures may also be incorporated. Further, additional layers, such as buffer layers between the substrate and other layers may be included. Moreover, the order of the p-type and n-type layers can be reversed with respect to the substrate. To provide waveguiding in the active layer(s), the active and waveguiding layers are bounded in the stack direction (z-direction) by areas of lower refractive index (cladding layers 12₁ and 16₂). The vertically adjacent parts of the p-type and n-type layers are given a lower refractive index than the active layer by a suitable material choice in a heterostructure. It will be understood that reference to top and bottom are for convenience. For example, flip-chip bonding techniques may be applied which would reverse the layer sequence in a packaged device compared to the layer sequence as grown.

[0034] LD chips according to our designs can be used for green and blue emitters in particular, but also can be used for red emitters.

[0035] Commercially, the dominant materials system for current blue or green LDs is based around gallium nitride and related materials, principally those in which gallium is partially or wholly substituted with aluminium and/or indium in the quaternary system GaAlInN.

[0036] Gallium nitride and related semiconductor compounds have a Wurtzite crystal structure, which is hexagonal with the hexagonal axis being referred to as the c-axis, or {0001} in the usual notation. The plane perpendicular to the c-axis is referred to as the c-plane. The substrate orientation can be in the c-plane, which is polar, or some other plane where the polarity is reduced or eliminated, referred to as semi-polar (SP) or non-polar (NP) orientations respectively. Example NP planes are the a-plane {11-20} and m-plane {10-10}. Example SP planes are {11-22} and {20-21}. The advantage of reducing or eliminating the polarity is that any subsequent Wurtzite layers which are not lattice-matched and pseudomorphic with the substrate will have their electric polarization fields reduced or eliminated. The Wurtzite crystal orientation in relation to the LD structure can therefore have different permutations depending on what is desired. For example, the c-axis may be aligned with the z-axis (c-plane structure), or may be aligned with the y-axis (NP structure), or may have some intermediate alignment (SP structure).

[0037] It is usual to measure efficiency and other performance characteristics of a LD by various different parameters. The most fundamental parameter for efficiency from a physics perspective of the semiconductor part of the LD is quantum efficiency (QE), namely the percentage of photons emitted per the number of electron-hole pairs that should be generated in the pn-junction assuming that all the drive current is converted into such electron-hole pairs. QE can be subdivided into the efficiency with which photons are coupled out of the laser structure (light extraction efficiency) and the efficiency with which photons are generated in the gain medium from the drive current (internal quantum efficiency). In turn, the internal quantum efficiency is the product of radiative efficiency and current injection efficiency (usually referred to as η_{inj}). Current injection efficiency is the percentage of drive current that results in electron-hole pairs being injected into the gain medium. Radiative efficiency is the percentage of those electron-hole pairs which reach the gain medium that recombine as desired to create a photon of the desired wavelength.

[0038] Separately from this discussion of quantum efficiency, the cavity in any laser will have losses arising from the mirrors and from the light absorption in the epitaxial stack (doping or defect induced) or light scattering at the ridge waveguide boundaries. The sum of these last two gives the so-called internal loss and denoted α_i . While mirror losses are to a large extent a design choice, i.e. dictated by the choice of reflectivities of the end mirrors, the internal loss is a 'real' loss caused by intrinsic properties of the materials used for the epitaxial structure or induced by process imperfections, such as scattering or absorption at the lasing wavelength. The fact that the laser is emitting constitutes a loss, so the existing of the 'leaky' output coupler mirror constitutes a loss of photons which would otherwise continue circulating in the cavity. Moreover, the gain medium itself will cause loss of photons through various diverse physical effects which may be more or less prevalent depending on the nature and design of the epitaxial stack. Examples are photon absorption (by the crystal lattice or doping in our case) or scattering out of the cavity. Internal losses α_i are typically of the order of ones to low tens of inverse centimetres (say 3-30 cm^{-1}). Lower mirror losses and higher internal losses α_i mean that more drive current is needed to achieve a given increase in power, that is the so-called "slope efficiency" is reduced, i.e. the optical output power to input drive current ratio.

[0039] Commercially, what is most important is wall-plug efficiency (WPE) which as well as the QE incorporates any other losses that may occur. Namely, WPE is the ratio of output optical energy of the laser to input electrical energy, i.e. from the mains supply at the "wall plug". Although in principle WPE should include all system losses, including for example power supply losses, powering of coolers, losses in output coupling optics and so forth, usually WPE is defined more narrowly in terms of the LD itself without peripherals, as the ratio of output optical power from the LD (without any optics other than the cavity mirrors) and input electrical power to the laser diode (i.e. excluding any electrical power consumption or losses external to that). We adopt this common usage in the present document.

[0040] We also note that in the present document electrical power consumption is generally referred to as power consumption and is the product of the drive current and applied voltage V across the LD, which is averaged over a cycle in the case of pulsed operation.

[0041] The structure of a blue or a green LD chip may be made from the GaAlInN materials system in which one or a multiple number of light emitting, active layers are sandwiched between doped layers of different type. The active layers may contain Ga, Al and In elements in any desired alloy to provide the desired band gaps, refractive indices and other relevant properties in the heterostructure. The p-type layers are arranged above the active layers in the stack, i.e. towards the surface of the device structure. The n-type layers are arranged below the active layers, i.e. in between the light emitting, active layers and the substrate. The substrate may be a c-plane free-standing GaN substrate, or a GaN substrate of a non-polar or semi-polar orientation. Both n-type and p-type layers may contain different molar percentages of the substitutional elements Al, In and Ga to provide the desired band gaps, refractive indices and other relevant properties in the semiconductor heterostructure.

[0042] In blue and green LD chip embodiments, the heterostructure includes one or a multiple number of light emitting layers (active layers) that are sandwiched between doped layers of different type. The active layers may contain Al, In, Ga, N elements. P-type layers are above, towards the surface of the device. N-type layers are below, in between the

light emitting layers and a substrate (preferably c-plane free-standing GaN). Both n- and p-layers may contain Al, In, Ga, N elements. The blue and green LDs of certain examples include:

- n- and p-doped conducting (Al, In, Ga)N layers;
- (Al, In, Ga)N light emitting layers (light emitting layers / quantum wells - QWs); and/or
- Light confining layers: (Al, In, Ga)N cladding layers and waveguides (which may be included in the p-layers, in the n-layers or at the upper and lower boundaries of the emitting region).

[0043] In red LD chips, the semiconductor heterostructure may be made of one or a multiple number of light emitting layers that are sandwiched between doped layers of different type. The active layers may contain In, Al, Ga, As or In, Al, Ga, P elements. P-type layers are above, towards the surface of the device. N-type layers are below, in between the light emitting layers and a substrate (GaAs). Both n- and p-layers may contain In, Al, Ga, As or In, Al, Ga, P elements. Similar to blue and green LDs, the body of the red LDs may include n- and p- conducting layers, light emitting layers (quantum wells) and /or light confining layers (claddings and waveguides).

[0044] The structure of a red LD chip may be made from the GaAlInAsP materials system. The body of the red LD can be made of one or a multiple number of light-emitting layers that are sandwiched between doped layers of different type. The active layers may contain In, Ga and P elements in any desired alloy to provide the desired band gaps, refractive indices and other relevant properties in the semiconductor heterostructure. The p-type layers are arranged above the active layers, i.e. towards the surface of the device structure. The n-type layers are arranged below the active layers, i.e. in between the light emitting, active layers and the substrate, for example a GaAs substrate. Both the n-type and p-type layers may contain Al, In, Ga, P elements in any desired alloy to provide the desired band gaps, refractive indices and other relevant properties in the heterostructure.

[0045] The semiconductor heterostructures are processed through standard process technology into devices having waveguiding structures (ridges), isolating dielectric layers, p- and n-electrode metallizations, and two end facets (mirrors). The end facets may be finally covered by dielectric coatings with a specified reflectivity.

[0046] We now discuss several different embodiments in which a single LD chip accommodates first and second emitters that are separately optimised for low and high slope operation.

[0047] Figure 13A is a schematic perspective drawing of an edge-emitting LD chip 15 according to such embodiments. The edge-emitting LD chip 15 has first and second ridges 26₁, 26₂ arranged side by side, instead of the usual one in a conventional ridge LD, and thus incorporates two emitters in the same chip sharing the same semiconductor heterostructure, namely the semiconductor heterostructure 10 on substrate 18 of Figure 12. The chip 15 has a length L in the y-direction between opposed mutually parallel cleaved end facets lying in the xz-plane which is common to both ridges and their underlying waveguides. In the vertical stack direction (z-direction), the semiconductor layer structure 10 is bounded by first and second metallic top contact electrodes 21₁, 21₂ and first and second metallic bottom contact electrodes 23₁, 23₂ for independently contacting the p-type layers and n-type substrate in the region of the first and second ridges 26₁, 26₂ respectively. In one lateral direction (y-direction), the active layer (not shown) of the semiconductor layer structure 10 is bounded by a front reflector (i.e. mirror) 22 and a back or back reflector (i.e. mirror) 24. The front and back reflectors 22 and 24 thus form the output coupler and high reflector respectively of the laser cavity. The semiconductor layer structure 10 is etched away on its upper surface to form first and second ridges 26₁, 26₂ of widths W₁, W₂ respectively (and the same length L). The ridge widths may be equal or different. The purpose of the etching is to bring the active layer (not visible in Figure 13A) sufficiently close to the surface to achieve good lateral optical confinement perpendicular to the ridge direction, i.e. in the x-direction, so as to form a linear waveguide, i.e. the gain material in the laser cavity, but not so close to the surface that scattering losses become significant. The ridges thus induce stripe portions of the active layer underlying the ridges 26₁ and 26₂ to form respective gain media between the reflectors 22 and 24 where population inversion is induced through injecting carriers via the pn-junction, which then recombine across the band gap generating photons of the desired wavelength. The provision of separate pairs of electrodes 21₁ & 23₁ and 21₂ & 23₂ allow the carrier injection in the two gain regions to be independently controlled. In a variant one of the top and bottom electrodes could be a single electrode covering both ridges, so there is one split electrode pair (either the top or the bottom) and one blanket electrode which is common to both ridges, wherein, the blanket electrode could be the ground electrode. The principal optical axes of the laser are in the y-direction. Each reflector 22, 24 is schematically illustrated as being a multilayer which would be a typical construction. It is noted that both gain media share the same end reflectors 22, 24. The front and back reflectors 22, 24 are formed on one opposed pair of cleaved end facets of the crystal which are perpendicular to the surface of the device, and these end facets are coated with high reflection dielectric mirrors to form the reflectors. The mirror materials can be deposited onto the end facets of the semiconductor structure using a physical deposition technique. The reflectivities of the front and back reflectors 22 and 24 are denoted R_f and R_b respectively.

[0048] Figure 13B is a schematic plan view of the two-ridge LD chip of Figure 13A. The LD chip 15 accommodates two laser diodes as defined by the two ridges 26_1 and 26_2 which share a common cavity having been based on the same semiconductor structure 10, 18 (Figure 12) and also sharing the same front and back reflectors 22, 24 (Figure 13A). The laser diode, whose waveguiding region is formed in the active layer 14 under the ridge 26_1 , labelled LD_L , has a lower slope efficiency. The laser diode whose waveguiding region is formed in the active layer 14 under the ridge 26_2 , labelled LD_H , has a higher slope efficiency. The LD chip 15 can be driven using the laser diode LD_L with a low slope efficiency when low power output and better power stability are required. The LD chip 15 can be driven using the laser diode LD_H with a high slope efficiency when high power output and high-power efficiency are required. In the following, we sometimes refer to a low slope emitter or a high slope emitter as a short form for a low slope *efficiency* emitter or a high slope *efficiency* emitter respectively.

[0049] Figure 13C is a schematic perspective drawing of the ridge LD chip structure 15 of Figures 13A & 13B. Under each of the first and second ridges 26_1 and 26_2 in the active region layers 14, an optical mode 'M' is formed, as shown schematically with the cross-hatched oval.

[0050] Figure 13D (left-hand part) is a schematic cross-section showing one ridge of the ridge LD structure of Figures 13A to 13C combined with a schematic graph of the variation of refractive index ' n ' with depth (right-hand part). An optical mode 'M' is supported in a waveguide that is defined laterally by the ridge 26 and vertically by the epitaxial design. The epitaxial layers 10 are grown on a substrate 18 by a suitable epitaxy process, such as metal-organic vapour phase epitaxy (MOVPE) or molecular beam epitaxy (MBE). The epitaxial layers 10 from the bottom up that are deposited on the substrate 18 are: lower cladding layer 16_2 , lower waveguide layer 16_1 , active regions layer(s) 14, upper waveguide layer 12_2 , upper cladding layer 12_1 (which extends upwards into a lower part of the ridge 26), and cap layer 19. As shown schematically in the right-hand part of the drawing, the active region layer(s) 14 are of higher refractive index than the waveguide layers 12_2 and 16_1 , which are, in turn, of higher refractive index than the cladding layers 12_1 and 16_2 . In terms of carriers, the outer cladding layers 12_1 and 16_2 are respectively doped p-type and n-type (or vice versa) to enable carrier injection across the active region layer(s) 14. The active region layer(s) 14 host in operation a reservoir of carriers that are available for stimulated emission across a suitable band gap of or within the active region, thereby providing the amplification. A functional definition of the active region layer(s) is therefore those layers which, in operation, host carriers that are available for providing amplified stimulated emission for photons propagating along the waveguide. The (vertical) thickness of the layers 16_1 , 14, 12_2 , collectively referred to as the waveguide layers, is marked as ' d_w ' and the (vertical) thickness of the fundamental mode of the waveguide is marked as ' d_m '. The mode (vertical) thickness is somewhat larger than the waveguide layer thickness owing to the evanescent wave components. Laterally, the (horizontal) width of the ridge is marked as ' w_r ' and the width of the fundamental mode of the waveguide as ' w_m ', where in this schematic cross-section $w_m < w_r$, although this inequality may be reversed by adjusting the etch depth of the ridge relative to the active region. The thickness of the total LD structure is labelled ' d_c '.

[0051] Figure 13E is a schematic perspective drawing of a buried waveguide design comparable to Figure 13C showing an "unburied" ridge waveguide design. Compared to Figure 13C, Figure 13E shows regrown infill regions 29 which together with the ridges 26_1 and 26_2 (and optionally also capping layer 19) form a layer of the structure. The infill regions 29 may be undoped semiconductor material. The material of the infill is preferably chosen to have a refractive index less than that of the ridge material so that waveguiding occurs under the buried ridge. In addition, dielectric material (not shown) may be deposited on the overgrown infill material around the ridge to promote guiding of the injection current into the gain medium.

[0052] Figure 13F is a schematic cross-section of a buried waveguide design as shown in Figure 13E with the infill region 29. Figure 13F is comparable to Figure 13D for the ridge waveguide design.

[0053] Figure 14 is a schematic cross-section showing an example layer structure in more detail than Figure 13D. Only one of the two ridges is shown. The other ridge has the same layer sequence, but may differ as a result of different processing, e.g. may have a different ridge width, ridge etch depth or ridge shape. The semiconductor epitaxial layers 10 are arranged on a substrate 18. The epitaxial layers 10 are, from the substrate 18 up: lower outer cladding layer 16_2 , lower inner cladding layer 16_1 , active regions layers 4, 5 and 6 (collectively labelled as 14), upper inner cladding layer 12_2 , upper outer cladding layer 12_1 , and cap layer 19. The active region layers 4, 5, 6 are of higher refractive index than the waveguide layers 16_1 , 12_2 , which are in turn of higher refractive index than the cladding layers 16_2 , 12_1 . In terms of carriers, the cladding layers 16_2 , 12_1 are respectively doped p-type and n-type (or vice versa) to enable carrier injection across the active region layer(s) 14. The active region layers 4, 5, 6 form a QW structure, with a well layer 5 sandwiched between lower and upper barrier layers 4 and 6. If the active region includes multiple QWs, then this layer structure will be repeated for each QW. In operation, each well hosts a reservoir of carriers that are available for stimulated emission, each well having a suitable band gap (or band gaps) for providing the amplification. Each ridge 26 is formed after growth of the epitaxial structure by etching away the cap layer 19 and a part of the cladding layer 12_1 . A dielectric layer 13 is then deposited to cover the surface of the outer cladding layer 13. A top contact layer 21 is deposited on the top of each ridge 26 over the cap layer 19, and a base contact layer 23 is deposited on the underside of the substrate 18, the contacts serving as electrodes to allow the drive current to be applied across the active region 14. It will be appreciated that each

of the illustrated layers may be made of multiple layers. Additional layers may also be included, e.g. buffer layers immediately on top of the substrate. Moreover, other structures are possible, e.g. with graded refractive index designs.

[0054] Regarding the thickness of the active region 14, this is principally defined by the thickness of the waveguide core between the waveguide layers, the core being formed by the QW region and the cladding being formed by the inner cladding layers. We define the active region thickness in this document as either the sum of the thicknesses of the layers 4, 5, 6 between the lower and upper waveguide layers 16₁ and 12₂, or the distance between the bottom of the upper waveguide layer 12₂ and the top of the lower waveguide layer 16₁. In a typical implementation using a single QW or multiple QWs made up of one or more QW layers and corresponding barrier layers, the active region thickness will be the sum of the thicknesses of the well and barrier layers, possibly including any additional layers that may be present between the (M)QW structure and the waveguide cladding layers. Another alternative is to have an active region without quantum wells, i.e. based on a conventional pn-junction across a bulk, i.e. 3D, band gap.

[0055] Each LD emitter is split in two independently controllable lasers that are arranged side by side separated by a short lateral distance: one LD with low slope efficiency (LD_L) and one with high slope efficiency (LD_H). The two LD emitters are arranged in different regions of the same chip. Each emitter can be independently addressed by the drive electrodes depending on the required output power regime.

[0056] Figure 15 is a table summarising material choice options for the different epitaxial layers for each of four known materials systems for fabricating LDs. In the left-hand column: the label 'cladding' corresponds to the outer cladding layers 16₂, 12₁; and 'waveguide' the inner cladding layers 16₁, 12₂. The principal materials systems of choice for fabricating LDs, as set out from left to right in the table are GaAlInN (sometimes referred to as GaN-based or nitride-based) for the wavelength range 390-570 nm, GaAlAs (sometimes referred to as arsenide-based) for the wavelength range 570-1150 nm, GaAlInP (sometimes referred to as phosphide-based) for the wavelength range 1150-2000 nm, and GaAlInAsSb (sometimes referred to as antimonide-based) for the wavelength range 2000-2700 nm. For current commercial LDs in the visible and near infrared (NIR) ranges, phosphide- and arsenide-based systems are predominantly used for red wavelengths and nitride-based systems for blue and green wavelengths.

[0057] Figure 16 shows output power, P, vs current, I, for the LD emitter chip, where laser LD_L has a slope efficiency of approximately 0.2 mW/mA and laser LD_H has a slope efficiency of approximately 1.6 mW/mA. How two lasers with different slope efficiencies can be accommodated in the same chip is described in detail below. The specific examples reported below are for LD chips emitting in the blue spectral region, but the design can be extended to chips emitting in the green and red spectral regions.

[0058] Figure 17 is a schematic plan view of a variant with multiple pairs of ridges 26₁ and 26₂ to provide multiple low slope efficiency LDs and multiple high slope efficiency LDs.

[0059] Although a plethora of parameters define the performance of a ridge LD, we use the parameter space defined by the following parameters to engineer two different slope efficiency laser diodes in the same chip:

Parameter	Symbol	Unit	Type
Cavity Length	L	m	geometric
Ridge width	W	m	geometric
Back reflector reflectivity	R _b	%	physical
Front reflector reflectivity	R _f	%	physical
Internal loss of gain medium	α _i	m ⁻¹	physical

[0060] The general effect of varying these parameters is known and is as follows.

[0061] The slope efficiency increases when:

- R_f is decreased
- R_b is increased
- α_i is decreased
- L is decreased

[0062] The threshold current decreases when:

- R_f or R_b is increased
- α_i is decreased
- L is decreased

[0063] Additionally, when the back-facet reflectivity R_b is decreased, the LD threshold current increases while the slope efficiency decreases.

[0064] The slope efficiency does not change significantly with ridge width for typical ridge width values in the range 1 - 4 μm . In the following examples, if not stated, the ridge width, W , is 2 μm .

[0065] Figures 18A, 18B and 18C are three pairs of graphs showing the parameter space that can be explored by varying the parameters R_f , α_i and L . Figure 18A shows the effect of varying front reflectivity R_f when cavity length L and internal loss α_i are fixed. Figure 18B shows the effect of varying cavity length L when internal loss α_i and front reflectivity R_f are fixed. Figure 18C shows the effect of varying front reflectivity R_f when cavity length L and internal loss α_i are fixed. The illustrated ranges are by way of example only and should not be taken as target values.

[0066] Based on those considerations, a low slope emitter LD_L may be produced by:

a. Higher front facet reflectivity R_f (lower slope and lower threshold compared to the high slope emitter LD_H on the same chip);

b. Higher internal α_i (higher threshold and lower slope compared to the high slope emitter LD_H on the same chip);

c. Longer cavity length L (higher threshold and lower slope compared to the high slope emitter LD_H on the same chip).

d. Lower back facet reflectivity R_b (lower slope and higher threshold compared to the high slope emitter LD_H on the same chip).

[0067] Certain embodiments of the disclosure can have design parameters values for both LD_L and LD_H lying in the following ranges:

- Cavity length: $300 \mu\text{m} \leq L \leq 2000 \mu\text{m}$
- Internal loss: $0 \text{ cm}^{-1} \leq \alpha_i \leq 30 \text{ cm}^{-1}$
- Back facet reflectivity: $10\% \geq R_b \geq 100\%$
- Front facet reflectivity: $10\% \leq R_f \leq 80\%$
- Monolithic mirror reflectivity: $10\% \leq R_M \leq 95\%$
- Waveguide tilt angle at the back facet: $0^\circ \leq \theta \leq 5^\circ$

[0068] Several different design approaches for designing a dual-slope LD chip having at least one low slope and at least one high slope emitter are now disclosed. These design approaches are discussed in turn with reference to a single pair of emitters LD_L and LD_H . Each of these design approaches may however be adapted to conform to the array design of Figure 17 with multiple low slope and/or multiple high slope emitters, e.g. arranged in pairs.

[0069] A first design approach provides the low slope efficiency emitter LD_L with a higher front reflectivity R_f compared to the high slope efficiency emitter LD_H . The emitters LD_L and LD_H share the same cavity length L , internal loss α_i and back facet reflectivity R_b .

[0070] To provide a different front reflectivity R_f for the two emitters, one option is to coat the whole front facet to provide the desired front reflectivity for the high slope efficiency emitter and then apply an additional coating locally to the low slope efficiency emitter to increase the front reflectivity for the low slope efficiency emitter. Another option is to first fabricate a monolithic mirror a reflectivity R_M at or near the front facet locally to the low slope efficiency emitter LD_L and then a blanket front coating is deposited over the whole front facet. The slope efficiency on the LD_L emitter can thus be set lower or higher by respectively increasing or decreasing R_M .

[0071] Figures 19A and 19B show respectively in plan view and cross-section schematic representations of a laser diode chip according to this design approach with a monolithic mirror with reflectivity R_M for the low slope laser diode LD_L .

[0072] The monolithic mirror can be produced during the LD fabrication process by standard processing techniques including standard and e-beam lithography, semiconductor etching and dielectric coating deposition.

[0073] Figure 20 shows an example to realize a monolithic mirror. Periodic channel structures with properly chosen dimensions (L_1 and L_2) are defined by e-beam lithography and by dry etching the channels. The air gaps in the channels are then filled with an insulating material. This forms a Bragg reflector 25 with a desired reflectivity R_M . The reflectivity can be set to a design value by appropriate choice of the parameters L_1 , L_2 and by using an insulating material with a suitable optical refractive index. Oxides and nitrides such as SiO_2 , SiN , AlN , Al_2O_3 , Ta_2O_5 , HfO_2 , ZrO_2 , TiO_2 can be used for this purpose.

[0074] Figure 21 shows power, P , vs current, I , curves for an example blue LD according to a high R_f design as shown in Figure 20. The example LD chip has the following parameter values:

- Cavity length: $L = 600 \mu\text{m}$

- Internal loss: $\alpha_i = 5 \text{ cm}^{-1}$
- Back facet reflectivity: $R_b = 80\%$
- Front facet reflectivity (high slope emitter): $R_f = 20\%$
- Front facet reflectivity (low slope emitter): $R_f = 90\%$ (combined value from Bragg reflector 25 and end facet coating)

5

[0075] The high slope emitter (solid line) has a slope efficiency of approximately 1.4 W/A and the low slope emitter (dash-dotted line) has a slope efficiency of approximately 0.2 W/A.

[0076] The LD chip can be run using the low slope emitter at low output powers, e.g. up to a few mW and run using the high slope emitter at high output powers, e.g. from about 10-100 mW.

10 **[0077]** The design parameters are not limited to the values used in the example as there are multiple combinations of parameters allowing the achievement of a desired performance for the low slope and the high slope LD emitters.

[0078] A second design approach provides the low slope efficiency emitter LD_L with a higher internal loss α_i' compared to the high slope efficiency emitter LD_H having a low internal loss α_i . The emitters LD_L and LD_H share the same cavity length L , front reflectivity R_f and back facet reflectivity R_b .

15 **[0079]** Figure 22 is a schematic plan view of an embodiment according to this design, which is one way to increase the internal loss for the low slope emitter. The internal loss is increased by structuring the LD_L waveguide during the device fabrication process with lossy regions 27 in order to increase the scattering loss at the waveguide sidewalls. Scattering loss at the waveguide sidewall can be increased by increasing the sidewall roughness and/or increasing the ridge etch depth.

20 **[0080]** Figure 23 shows power, P , vs current, I , curves for an example blue LD chip according to a raised internal loss design as shown in Figure 22. The example LD chip has the following parameter values:

- Cavity length: $L = 600 \text{ }\mu\text{m}$
- Internal loss (LD_H): $\alpha_i^H = 5 \text{ cm}^{-1}$
- 25 • Internal loss (LD_L): $\alpha_i^L = 30 \text{ cm}^{-1}$
- Back facet reflectivity: $R_b = 95\%$
- Front facet reflectivity: $R_f = 20\%$

30 **[0081]** The high slope emitter (solid line) has a slope efficiency of approximately 1.5 W/A and the low slope emitter (dash-dotted line) has a slope efficiency of approximately 0.6 W/A.

[0082] The design parameters are not limited to the values used in the example as there are multiple combinations of parameters allowing the achievement of a desired performance for the low slope and the high slope LD emitters.

35 **[0083]** A third design approach shortens the cavity length for the high slope emitter. The low and high slope emitters share the front mirror, but the high slope cavity is shortened and uses a monolithic mirror as its back reflector which is fabricated within the chip part way between the front and back chip facets. The low and high slope emitters share the same internal loss α_i as well as the same front facet reflectivity R_f .

[0084] Figures 24A and 24B are schematic drawings in plan and section showing an example structure according to this design approach. To decrease the cavity length L for the high slope laser diode LD_H , a monolithic back mirror R_M is fabricated by standard lithography and semiconductor etching processes.

40 **[0085]** Figure 25 shows power, P , vs current, I , curves for an example blue LD according to shortened cavity high slope laser design as shown in Figures 24A and 24B. The example LD chip has the following parameter values:

- Cavity length LD_L : $L_L = 1000 \text{ }\mu\text{m}$
- Cavity length LD_H : $L_H = 600 \text{ }\mu\text{m}$
- 45 • Internal loss: $\alpha_i = 5 \text{ cm}^{-1}$
- Back facet reflectivity (= LD_L back reflectivity): $R_b = 20\%$
- Monolithic mirror reflectivity (= LD_H back reflectivity): $R_M = 90\%$
- Front facet reflectivity: $R_f = 20\%$

50 **[0086]** The high slope emitter (solid line) has a slope efficiency of approximately 1.5 W/A and the low slope emitter (dash-dotted line) has a slope efficiency of approximately 0.8 W/A.

[0087] The design parameters are not limited to the values used in the example as there are multiple combinations of parameters allowing the achievement of a desired performance for the low slope and the high slope LD emitters.

55 **[0088]** A fourth design approach is to reduce the effective back reflectivity for the low slope laser by bending the waveguide where it meets the back facet. The bend has the effect that a higher proportion of the light reflected from the back facet is not coupled back into the waveguide, thereby increasing round trip loss. The low and high slope lasers share the same cavity length L , internal loss α_i , front reflectivity R_f and (intrinsic) back reflectivity R_b .

[0089] Figure 26 is a schematic plan view of an example structure according to this design approach. The ridge 26₁,

and hence the underlying waveguide, of the low slope efficiency emitter LD_L is bent by an angle θ so that the waveguide meets the back facet at a non-orthogonal angle. This has the effect of reducing the modal back reflectivity for the low slope emitter.

[0090] Figure 27 is a graph showing the attenuation in the reflectivity as a function of tilt angle θ . The reflection attenuation coefficient c_r that is desired will typically be in the range 10^0 to 10^{-1} , which for this example means a tilt angle $\theta \leq 2^\circ$.

[0091] Figure 28 shows power, P, vs current, I, curves for an example blue LD chip according to the tilted waveguide design as shown in Figure 26. The example LD chip has the following parameter values:

- Cavity length: $L = 600 \mu\text{m}$
- Internal loss: $\alpha_i = 5 \text{ cm}^{-1}$
- Back facet reflectivity (intrinsic): $R_b = 95\%$
- Front facet reflectivity: $R_f = 20\%$
- Tilt angle at the back facet: $\theta = 2^\circ$

[0092] The high slope emitter (solid line) has a slope efficiency of approximately 1.5 W/A and the low slope emitter (dash-dotted line) has a slope efficiency of approximately 0.5 W/A.

[0093] The design parameters are not limited to the values used in the example as there are multiple combinations of parameters allowing the achievement of a desired performance for the low slope and the high slope LD emitters.

[0094] It will be understood that further design permutations are possible by combining two or more of the first to fourth design approaches of the dual-slope LD chip embodiments.

[0095] Figure 29 is a schematic perspective view of an RGB light module 50. The light module 50 has a unitary construction and includes red, green and blue LD chips 60, 70 and 80. Any one or more of the LD chips 60, 70 or 80 may be according to embodiments of the disclosure. For example, the blue and green LD chips may be according to embodiments of the disclosure and the red LD chip may be some other design, or all of LD chips 60, 70 and 80 may be according to embodiments of the disclosure. The LD chips 60, 70 and 80 are arranged side by side on a common circuit board with a common n-electrode 17, which may or may not involve the different LDs having a common n-electrode. Alternatively, individual n-electrodes may be provided. Each emitter 60, 70 and 80 has its own pair of p-electrodes 21r, 21g and 21b, which are contacted by respective pairs of drive wire bridges 28r, 28g and 28b connected to pairs of p-drive pads 30r, 30g and 30b. The light emitted from each LD is schematically shown as being in a cone with a certain solid angle. (The outputs from the two side-by-side waveguides in each emitter may be guided to a common beam path or may be slightly laterally offset in the x-direction.) It will be understood that micro-lenses, optical fibres and other optical components may be coupled to the light module to form whatever output is desired.

[0096] Figure 30 is a schematic drawing of a light source unit 145 including a drive circuit and other components suitable for integration of a three-emitter device or module 125 embodying the invention, the three emitters, each with one LD chip, being labelled R, G and B for red, green and blue. The three LD chips are controlled by respective dual lines 132r, 132g and 132b from a driver unit 130 to supply suitable drive currents (and bias voltages) to the electrodes. Suitable drive currents (and voltages) I_{SET} (V_{SET}) are received from a controller 138 for each of the six components, i.e. one pair for each of the R, G and B laser diodes, these signal pairs being labelled I1, h1; 12, h2; 13, h3. The arrangement is suitable for any of the embodiments of the disclosure.

[0097] Figure 31 shows an example of a near-to-eye projection system in a monocle format, i.e. glasses or spectacles for a single eye. A housing 37 is integrated midway along a temple 40 and houses the light source unit 145 of Figure 50. The combined RGB light beam 35 output by the light source unit 145 is directed to a scanning element 36 which projects and couple the light beam 35 into a waveguide lens 42. The guided light beam is then extracted under the form of a virtual image 43 in front of a wearer's eye E through an outcoupling element 45.

[0098] Figure 32 shows an example near-to-eye projection system in a spectacles format which is essentially a doubled-up version of the single-eye system of Figure 31 for near-to-eye projection into the left eye E_L and right eye E_R. The same reference numerals are used. Projection in front of both eyes allows for additional possibilities, such as stereoscopic imaging for 3D.

[0099] It will be clear to one skilled in the art that many improvements and modifications can be made to the foregoing exemplary embodiments without departing from the scope of the present disclosure.

Claims

1. A laser diode chip (15) comprising:

a plurality of semiconductor layers (10) arranged on a substrate (18), the semiconductor layers collectively

defining an active region layer (14) of higher refractive index sandwiched between upper and lower cladding layers (12, 16) of lower refractive index;

mutually opposed front and back end facets (22, 24) on which are formed front and back mirrors;

first and second ridges (26) each extending laterally between the front and back end facets (22, 24) and having respective pairs of sides that extend part way to the active region layer (14) to define first and second waveguides in the active region layer (14);

a first laser diode (LD_L) having a first gain medium defined by the first waveguide and which is configured to operate with a first, low slope efficiency;

a second laser diode (LD_H) having a second gain medium defined by the second waveguide and which is configured to operate with a second, high slope efficiency, wherein the second slope efficiency is higher than the first slope efficiency;

a plurality of electrical contacts (21, 23) configured to allow the first and second laser diodes to be independently driven; and

a controller (138) configured to drive the electrical contacts (21, 23) in a first mode of operation to operate the laser diode chip with low slope efficiency for low output powers using the first laser diode, and in a second mode of operation to operate the laser diode chip with high slope efficiency for high output powers using the second laser diode (LD_H).

2. The laser diode chip of claim 1, wherein the difference between the first and second slope efficiencies is realized at least in part by providing the front mirror of the first, low slope efficiency, laser diode (LD_L) with a higher reflectivity than the front mirror of the second, high slope efficiency, laser diode (LD_H).

3. The laser diode chip of claim 1 or 2, wherein the difference between the first and second slope efficiencies is realized at least in part by providing the first waveguide of the first, low slope efficiency, laser diode (LD_L) with a higher internal loss than that of the second waveguide of second, high slope efficiency, laser diode (LD_H).

4. The laser diode chip of claim 1, 2 or 3, wherein the difference between the first and second slope efficiencies is realized at least in part by providing the second waveguide of the second, high slope efficiency, laser diode (LD_H) with an intermediate mirror (25) arranged part way between the front end facet and the back end facet so that the second laser diode (LD_H) has a shortened cavity length compared to the first laser diode (LD_L).

5. The laser diode chip of any preceding claim, wherein the difference between the first and second slope efficiencies is realized at least in part by providing the first waveguide of the first, low slope efficiency, laser diode (LD_L) with a bend so that it meets the back end facet (24) at a non-orthogonal angle, thereby inducing additional coupling losses for light reflected back into the first waveguide from the back mirror.

6. The laser diode chip of any preceding claim, wherein the second slope efficiency is at least 1.5, 2, 3, 4, 5, 6, 7, 8, 9, 10, or 20 times greater than the first slope efficiency.

7. The laser diode chip of any of claims 1 to 6, wherein the laser diode chip is configured to emit in the blue spectral region, the first slope efficiency is less than 0.8 W/A and the second slope efficiency is greater than 1.2 W/A.

8. The laser diode chip of any of claims 1 to 6, wherein the laser diode chip is configured to emit in the green spectral region, the first slope efficiency is less than 0.3 W/A and the second slope efficiency is greater than 0.5 W/A.

9. The laser diode chip of any of claims 1 to 6, wherein the laser diode chip is configured to emit in the red spectral region, the first slope efficiency is less than 0.3 W/A and the second slope efficiency is greater than 0.8 W/A.

10. A light module (50) comprising at least one laser diode chip according to any preceding claim.

11. A vision system configured to be placed on a human head incorporating a light module (50) according to claim 10.

FIG. 1A

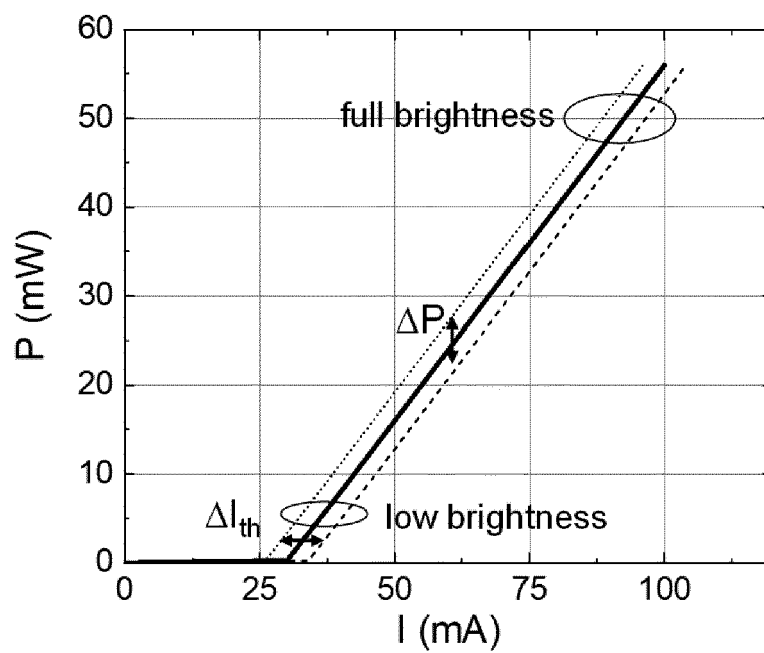
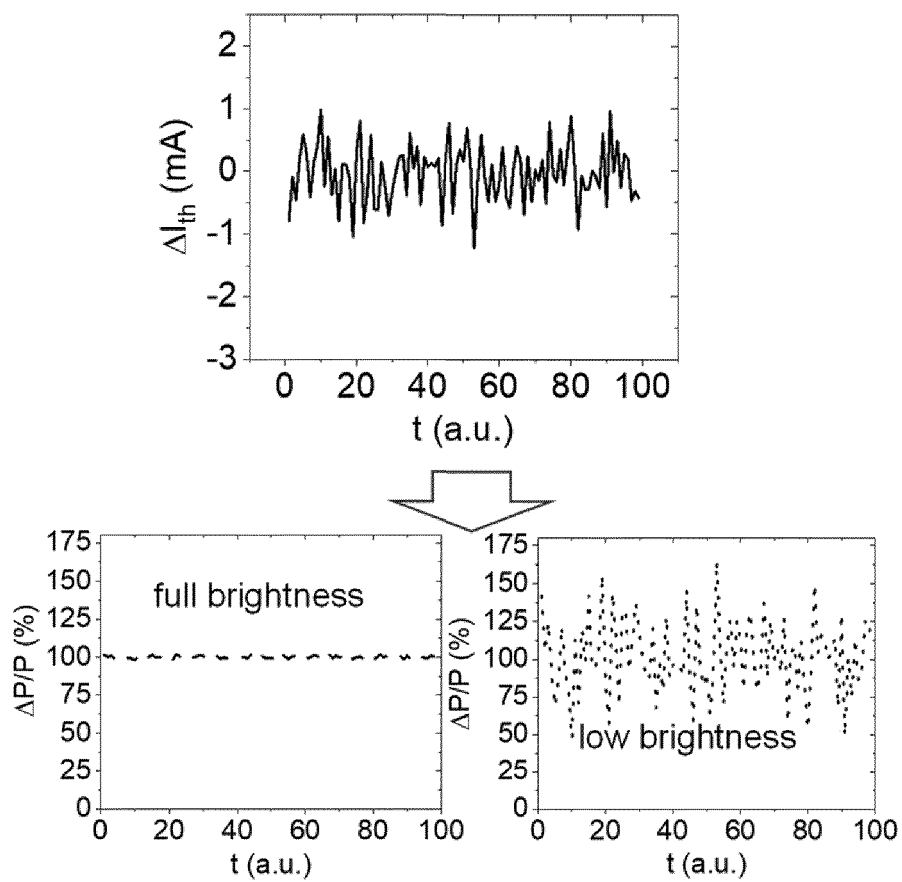


FIG. 1B



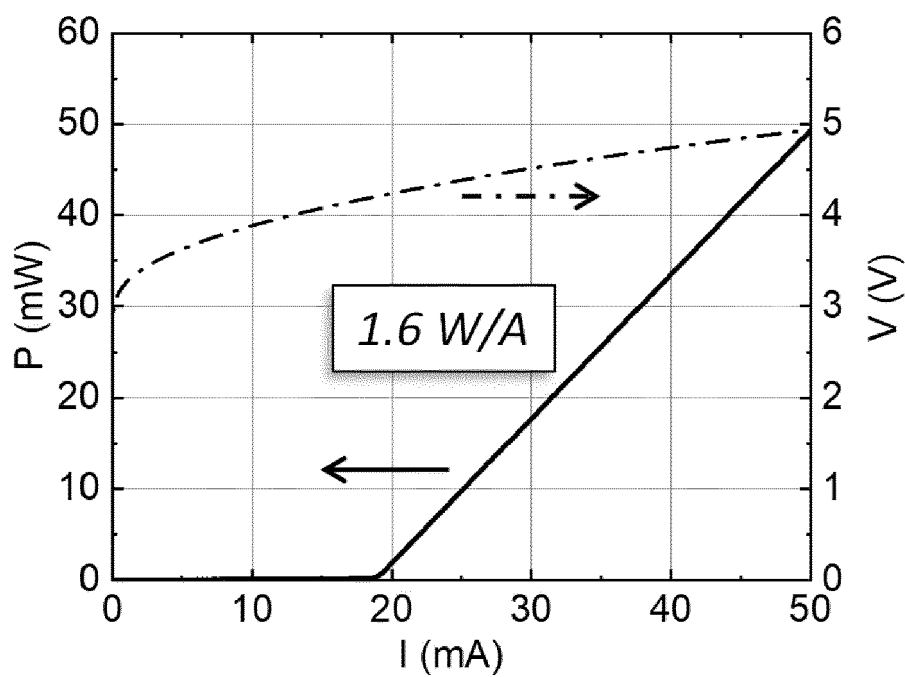


FIG. 2A

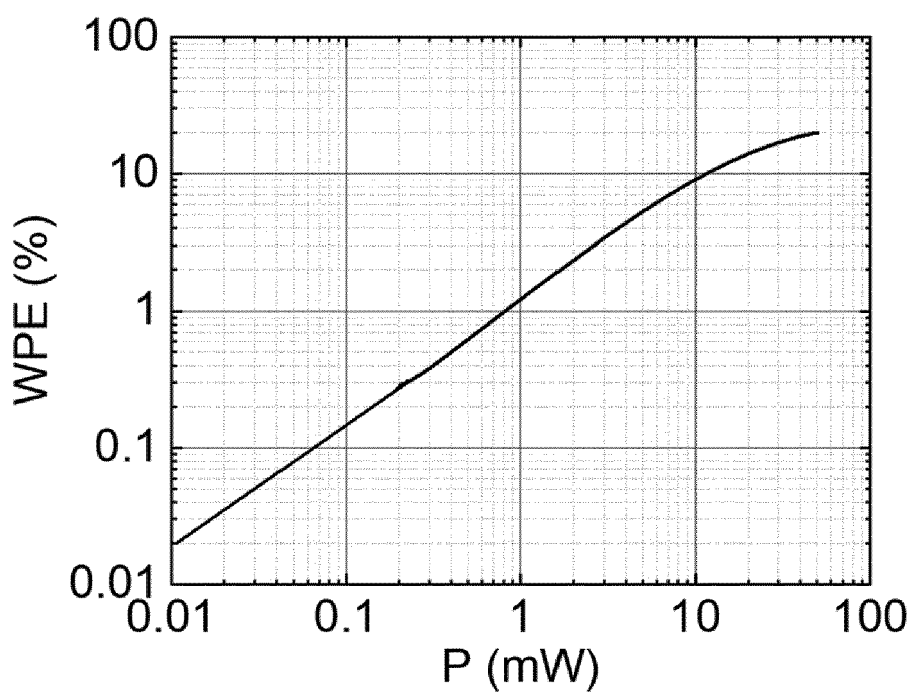


FIG. 2B

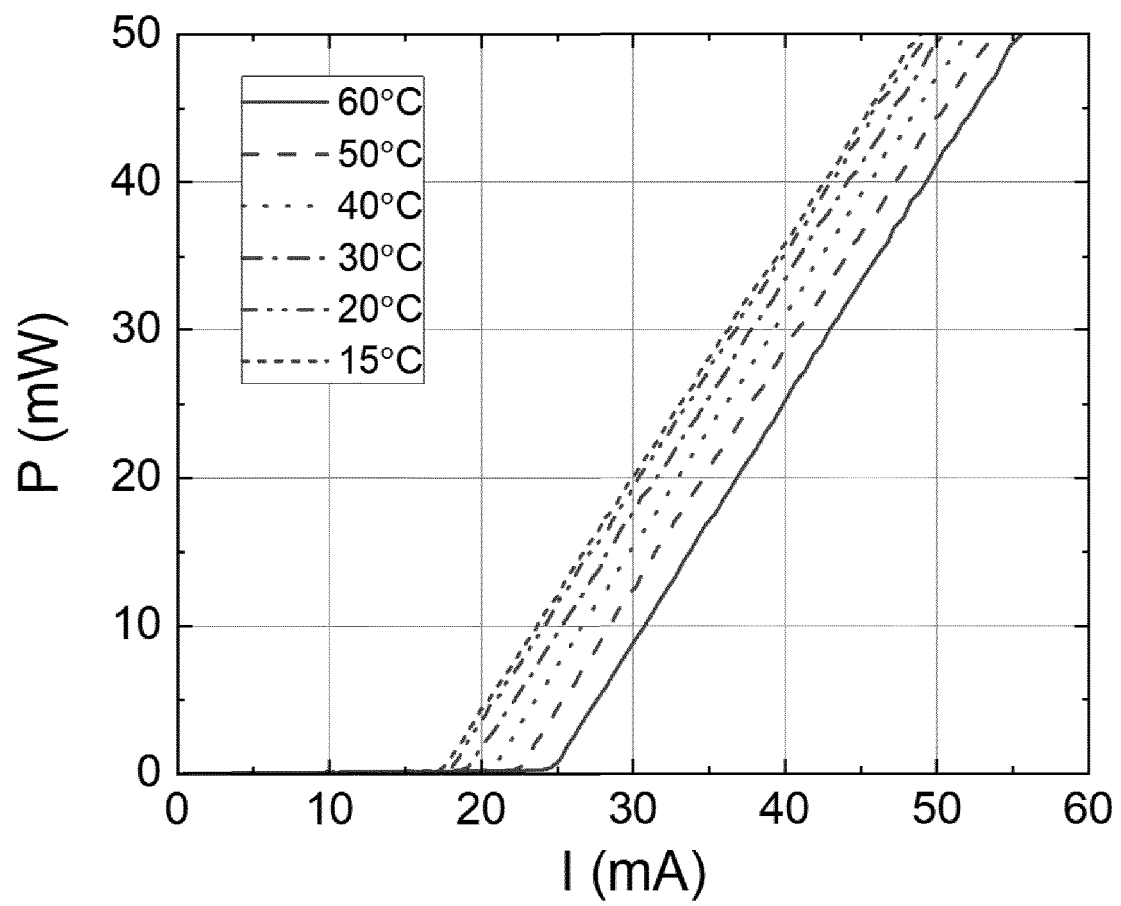


FIG. 3

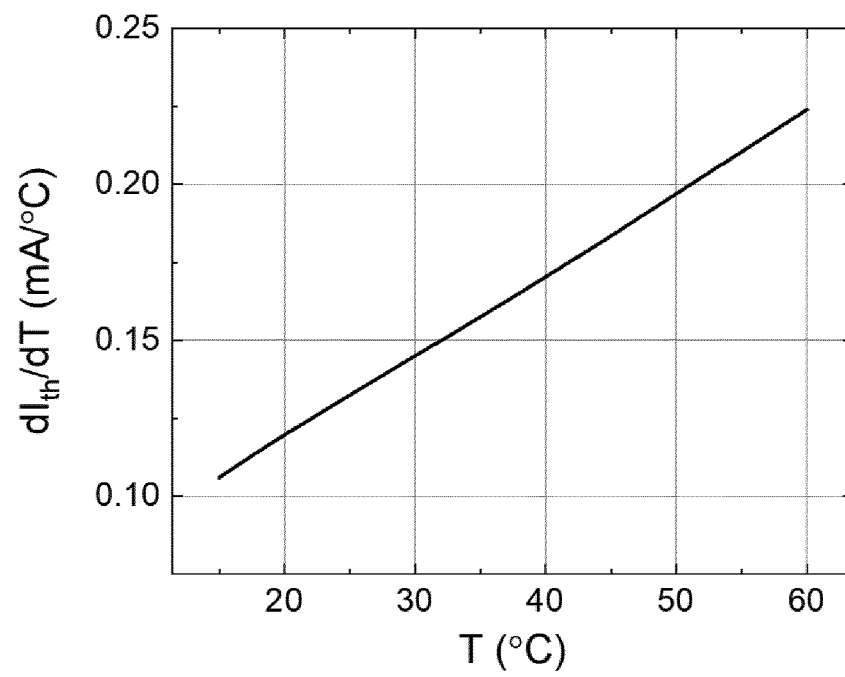


FIG. 4A

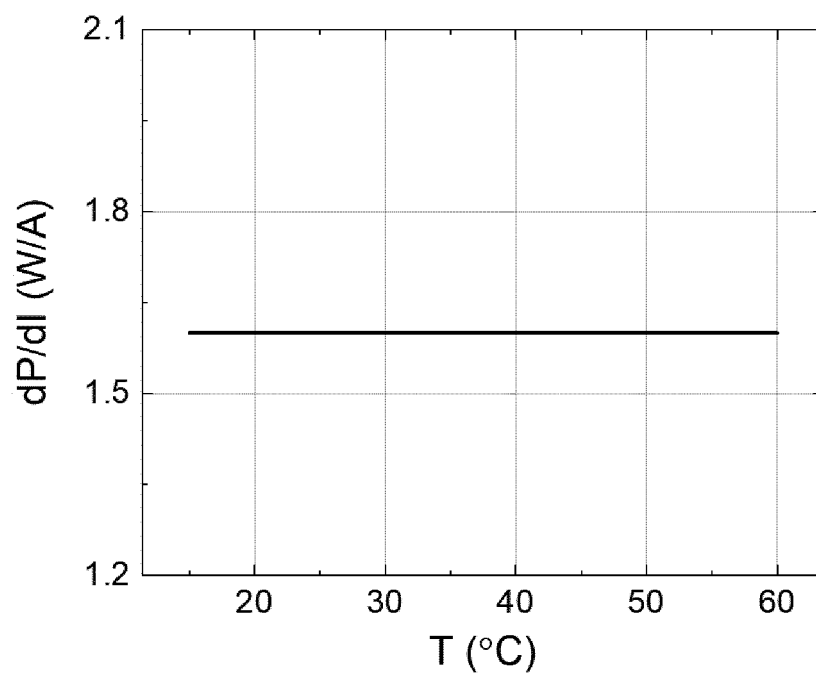


FIG. 4B

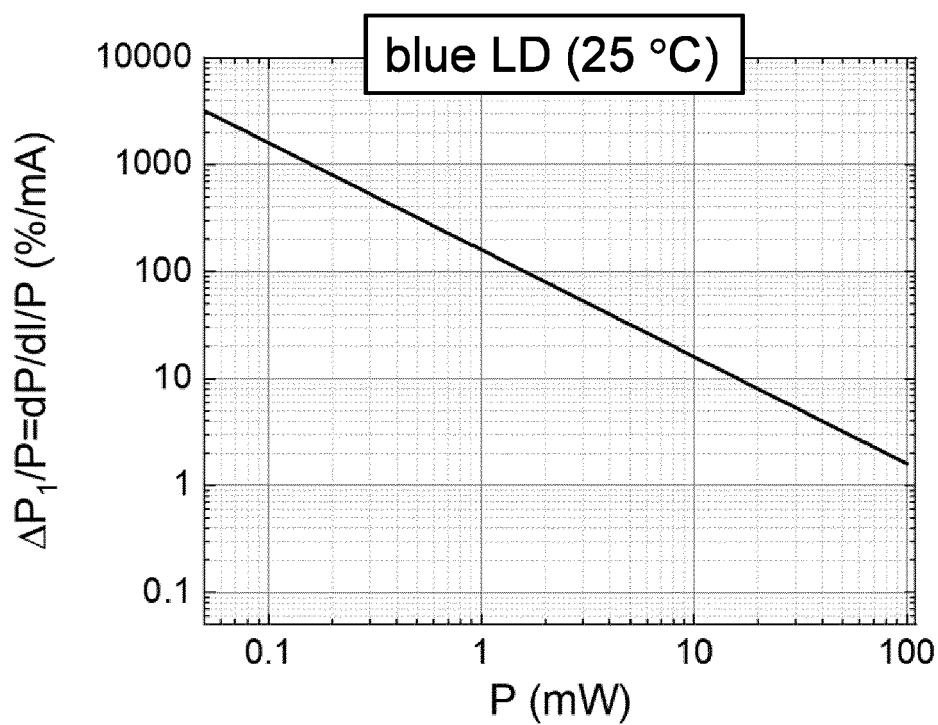


FIG. 5A

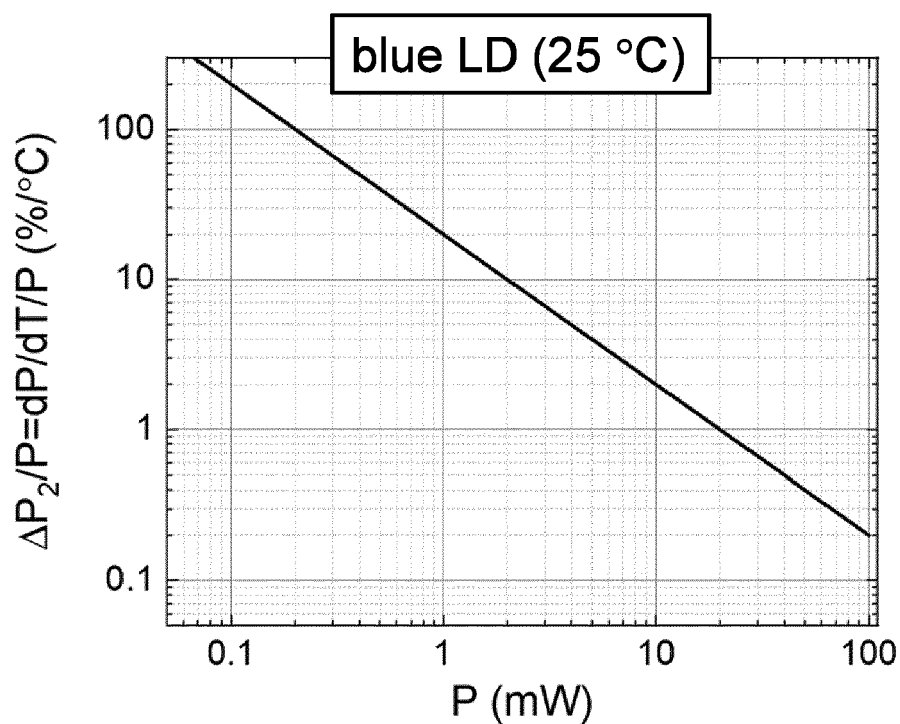


FIG. 5B

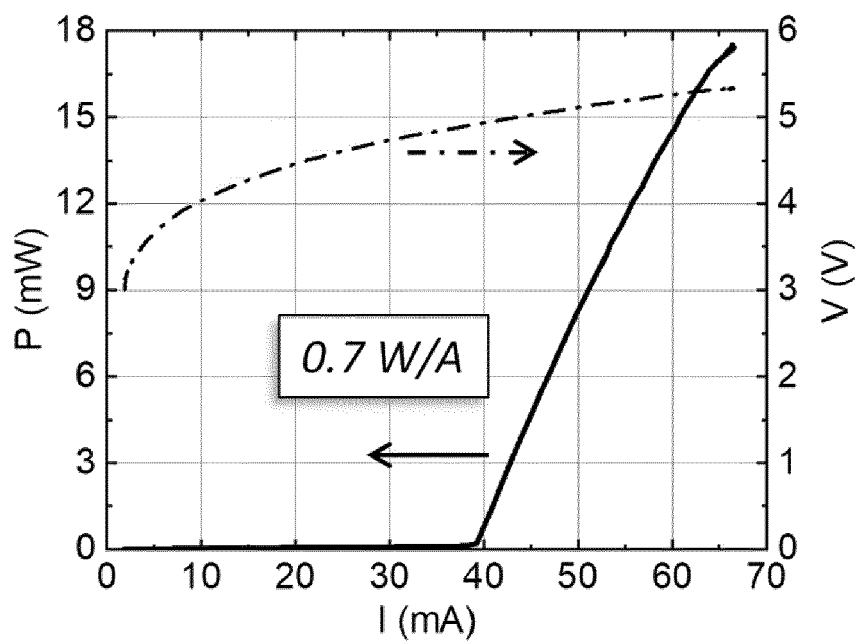


FIG. 6A

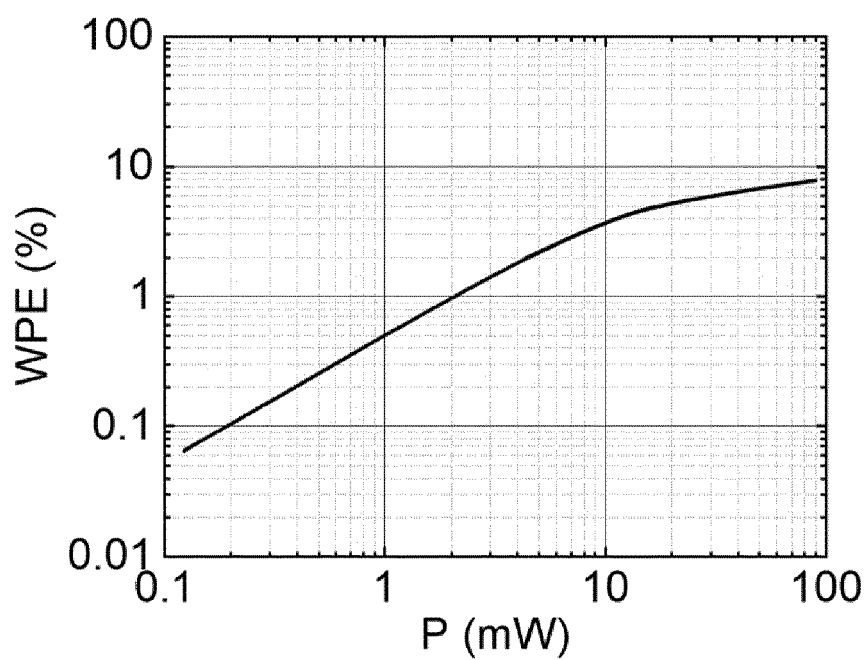


FIG. 6B

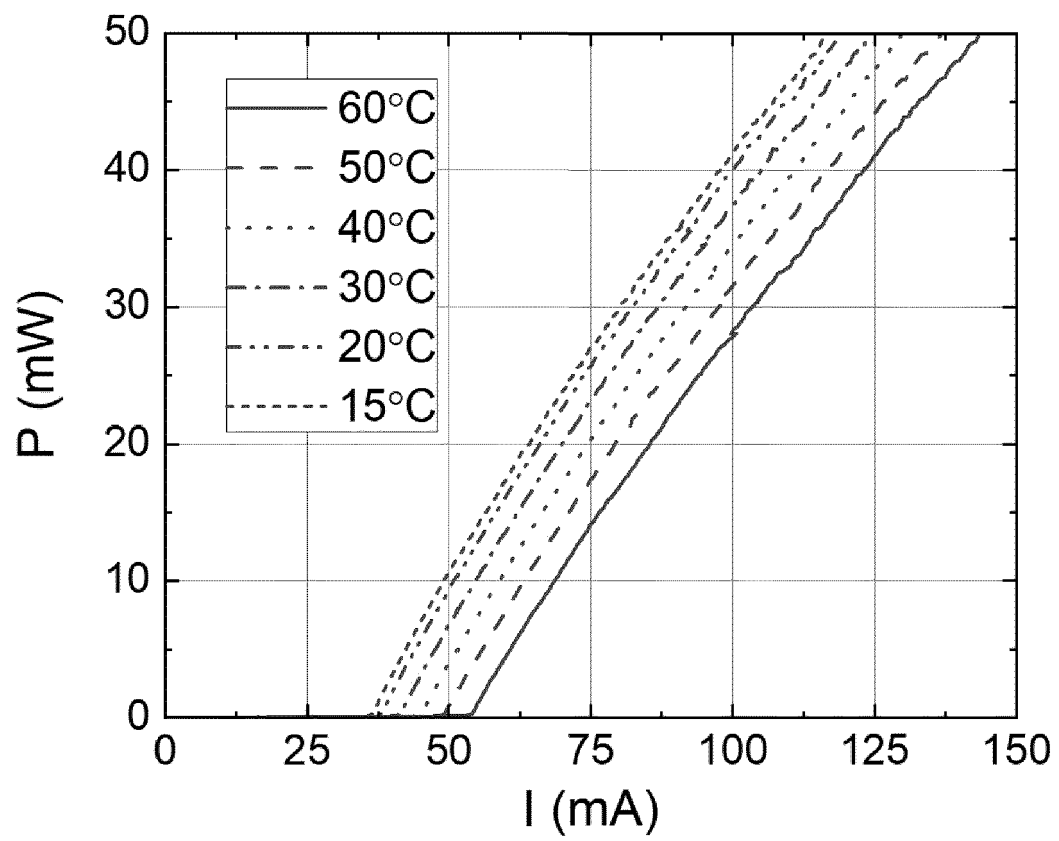


FIG. 7

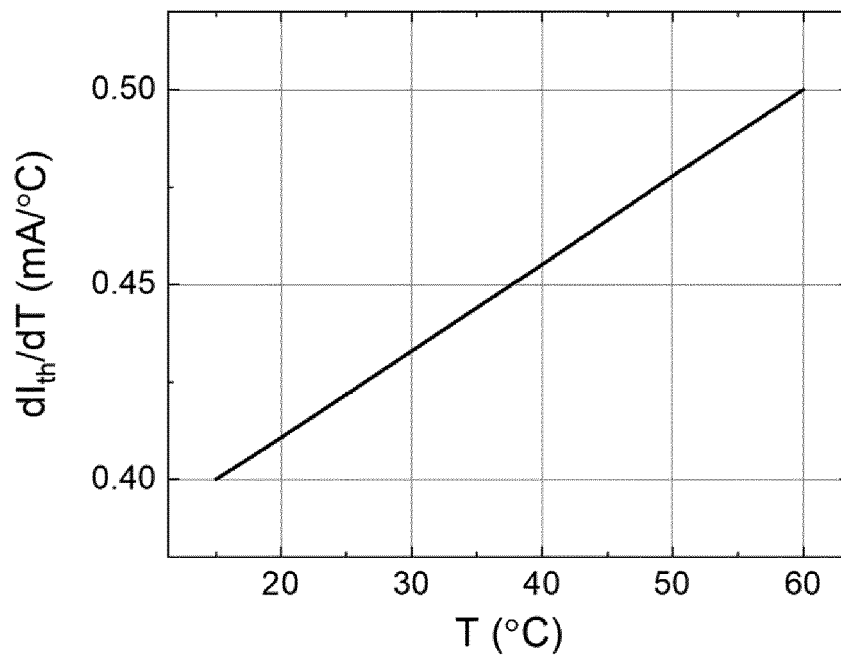


FIG. 8A

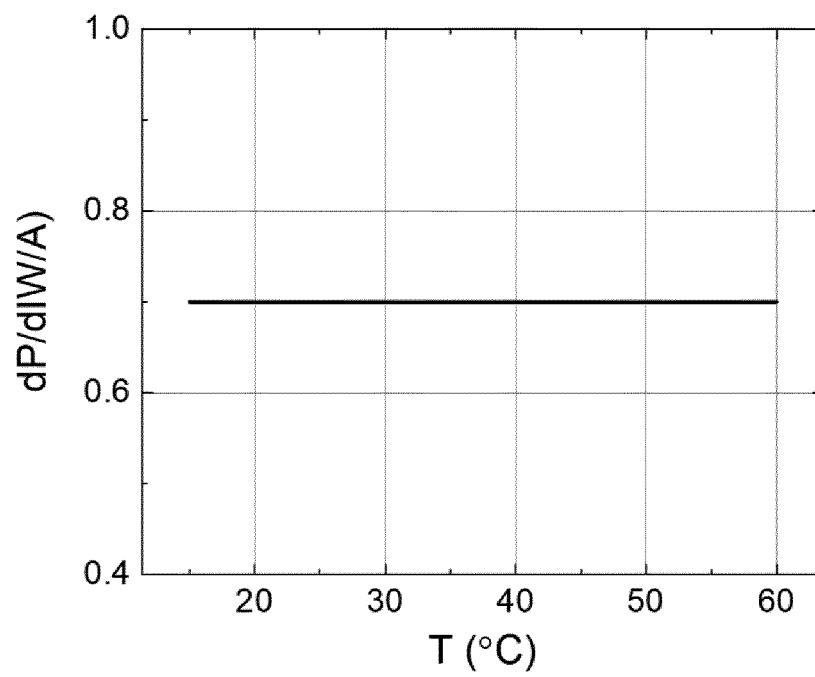


FIG. 8B

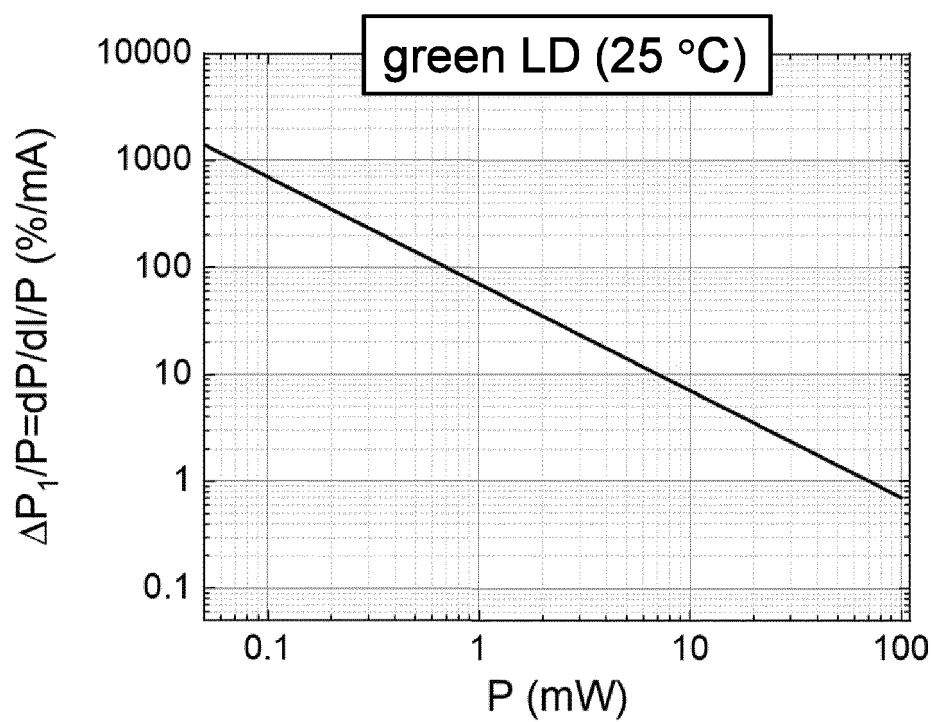


FIG. 9A

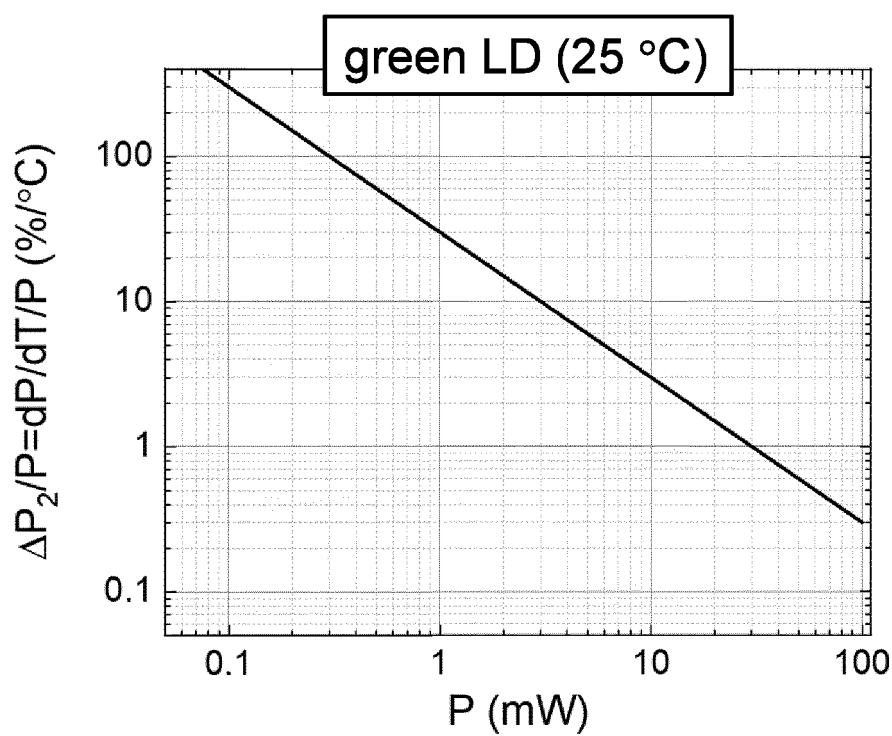


FIG. 9B

FIG. 10A

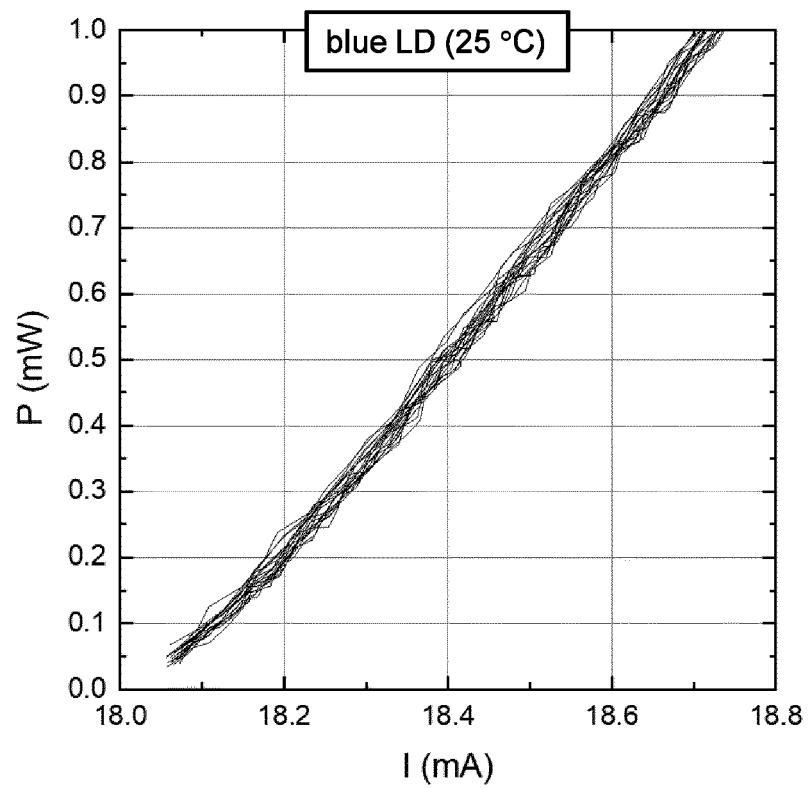


FIG. 10B

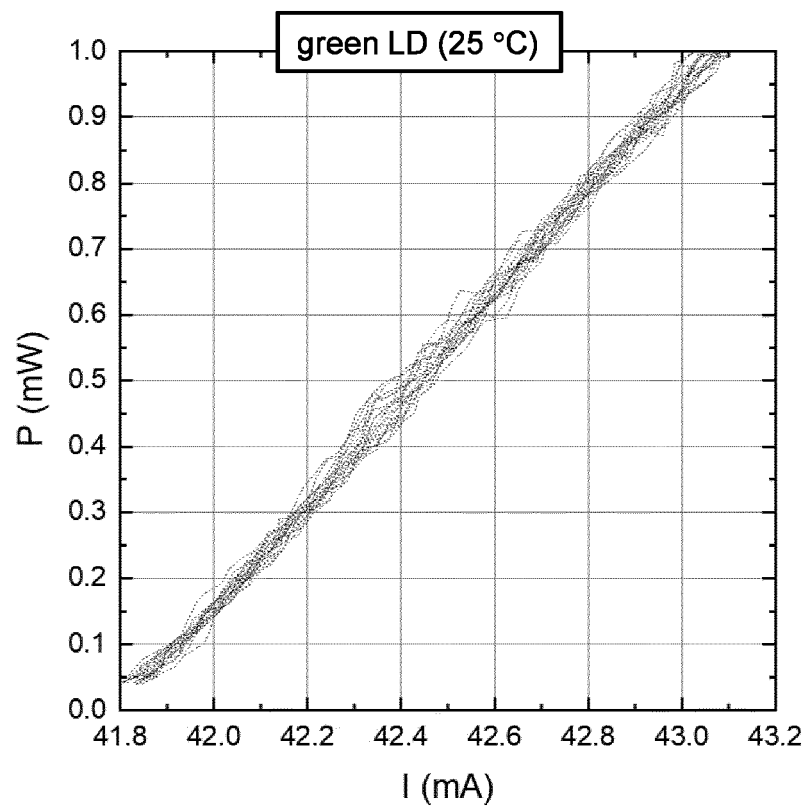


FIG. 11A

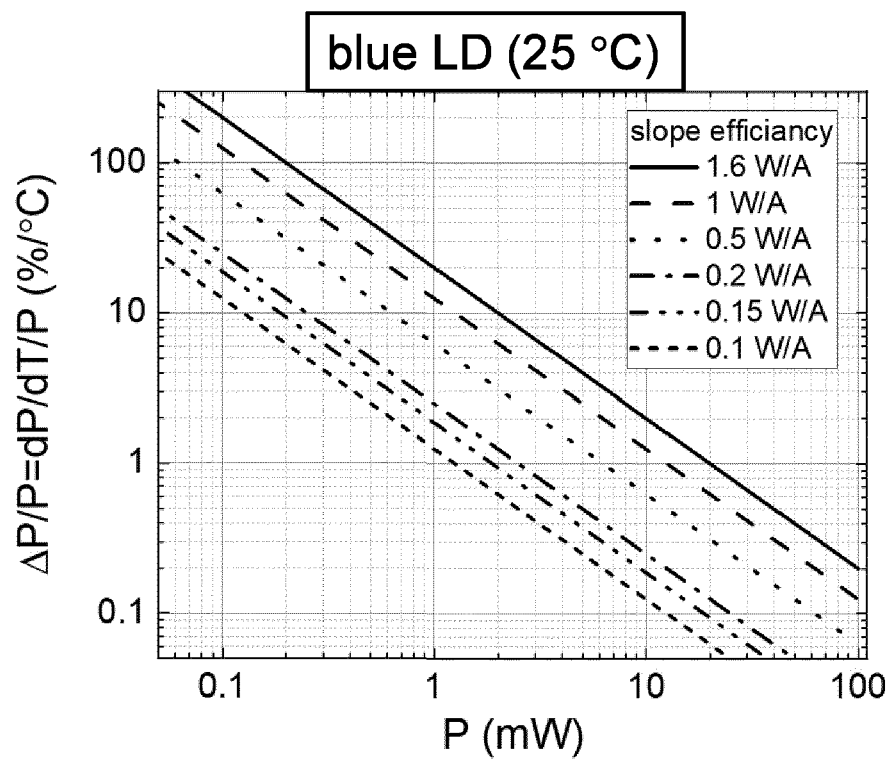
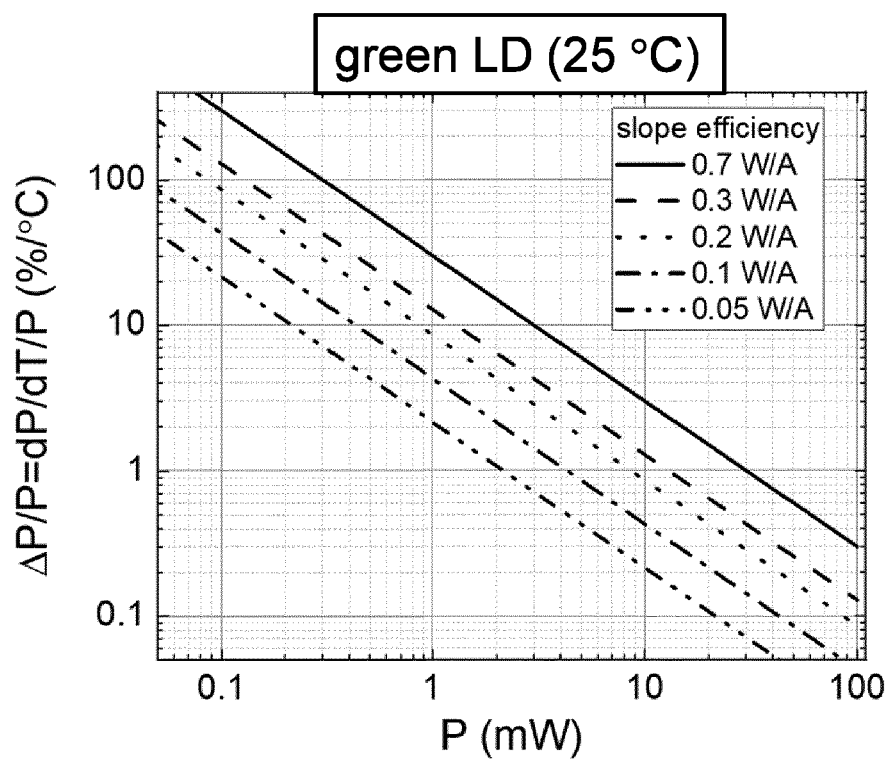


FIG. 11B



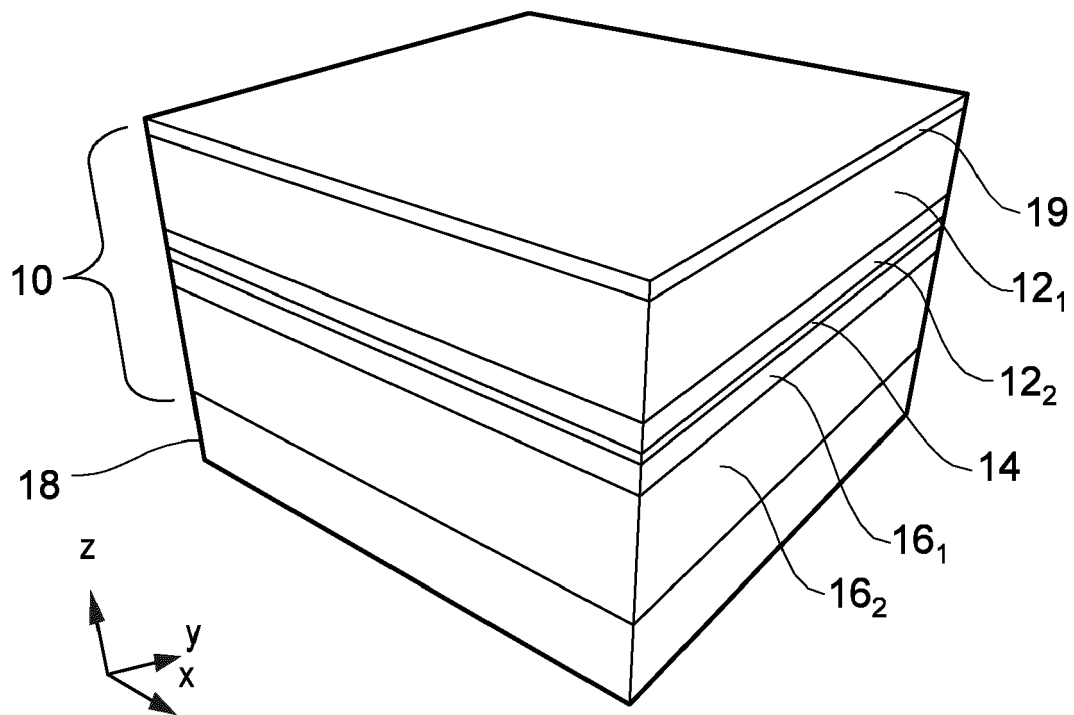


FIG. 12

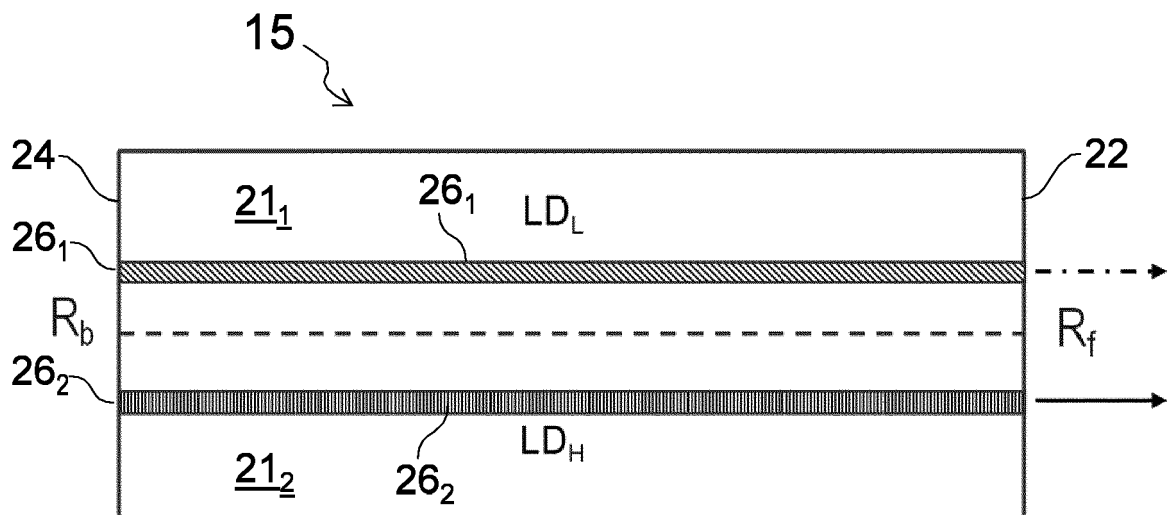


FIG. 13B

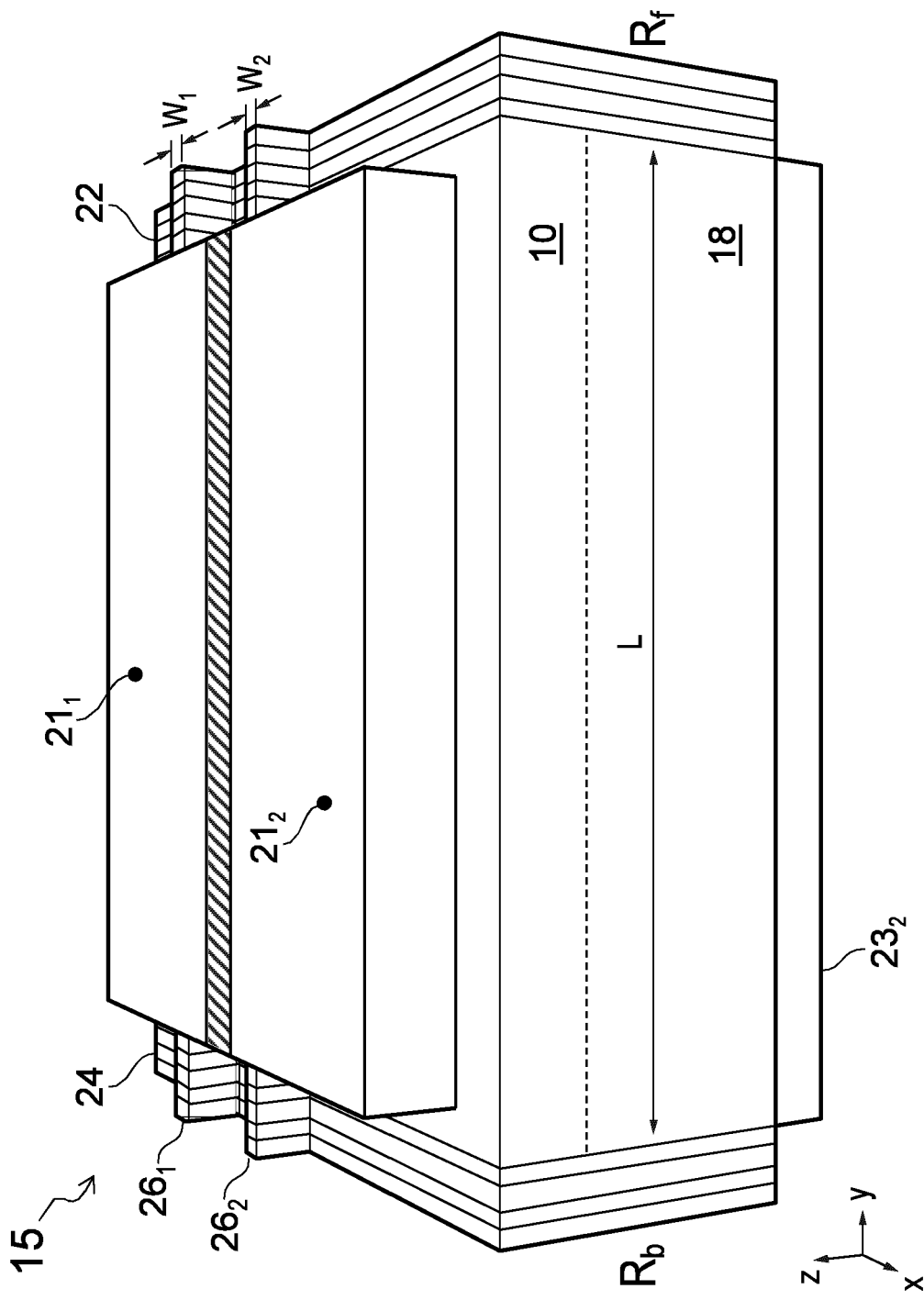


FIG. 13A

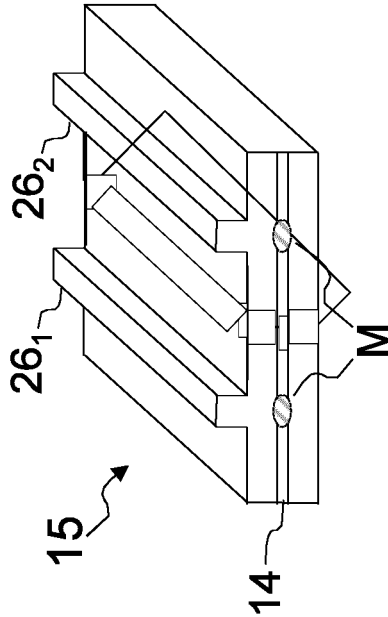


FIG. 13C

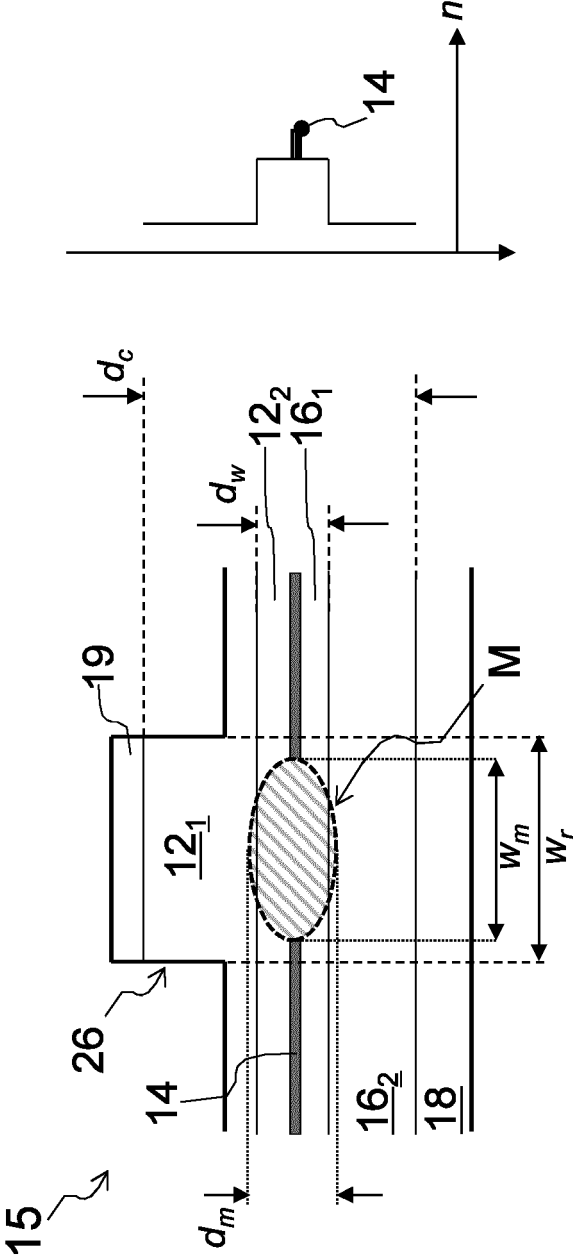


FIG. 13D

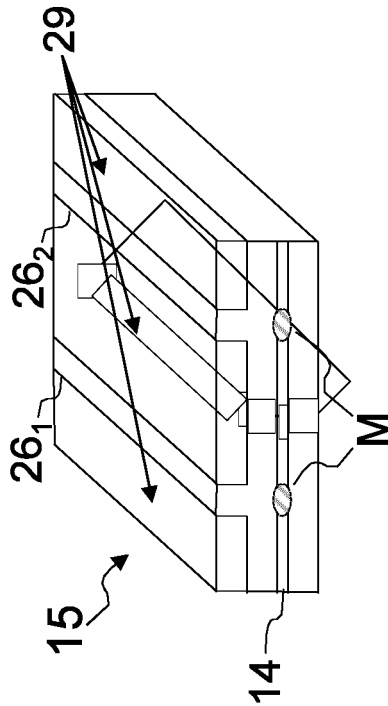


FIG. 13E

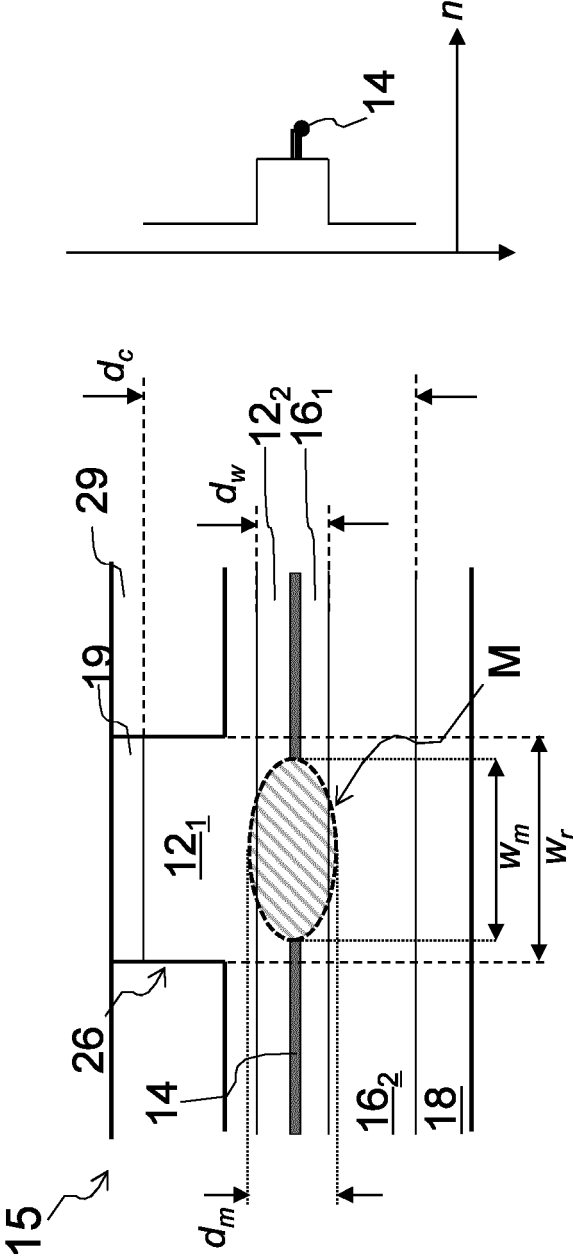


FIG. 13F

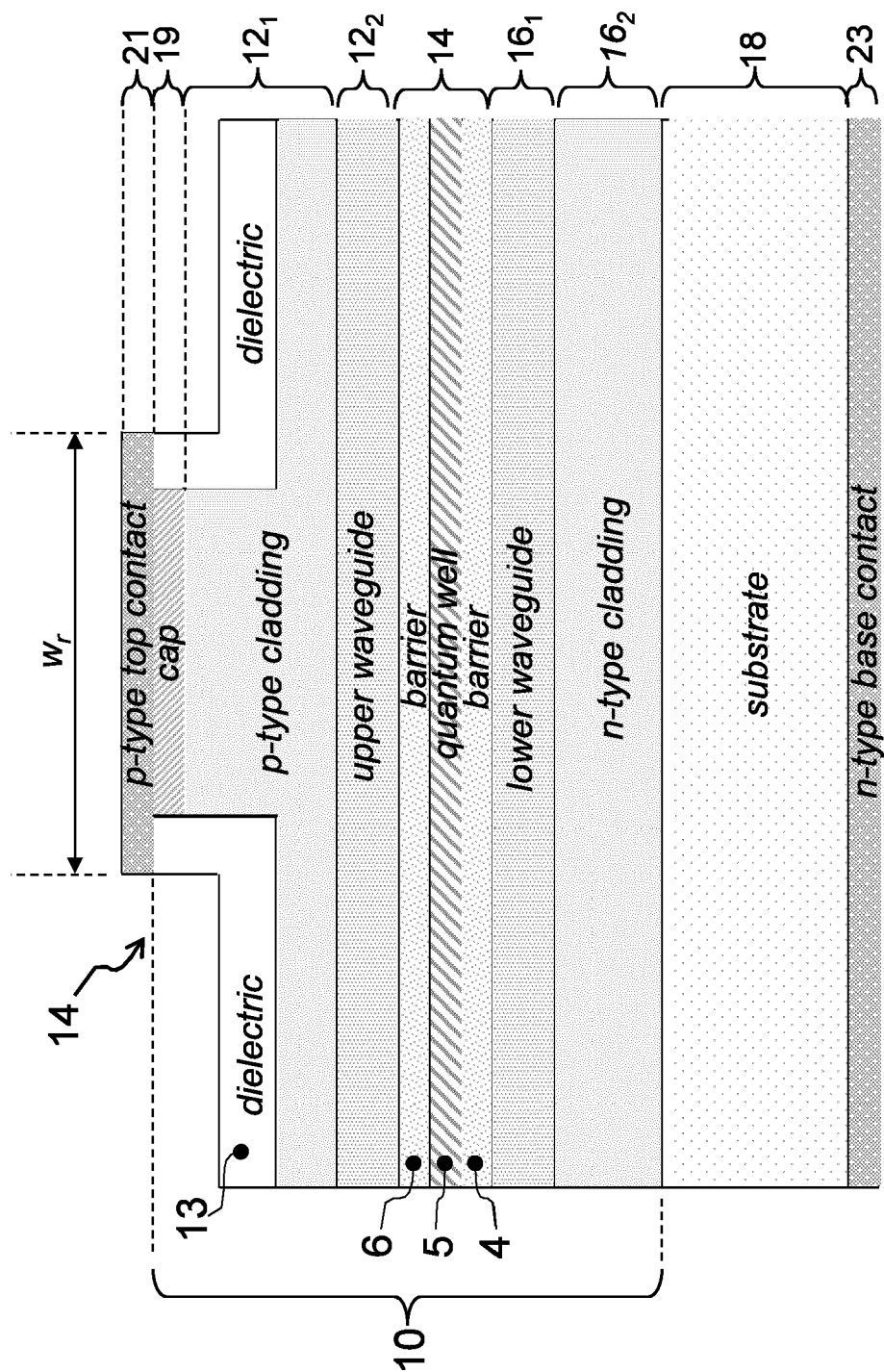


FIG. 14

Wavelength Range	390–570 nm	570–1150 nm	1150–2000 nm	2000–2700 nm
Substrate	GaN	GaAs	InP	GaSb
Cladding	$\text{Al}_x\text{Ga}_{1-x}\text{N}$	$\text{Al}_x\text{Ga}_{1-x}\text{As}$ $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{P}$	InP $\text{Al}_x\text{In}_{1-x}\text{As}$	$\text{Al}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{Sb}_y$
Waveguide	GaN	$\text{Al}_x\text{Ga}_{1-x}\text{As}$ $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{P}$	$\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{As}$ $\text{In}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{P}_y$	$\text{Al}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{Sb}_y$
Active region (QWs + barriers)	$\text{In}_x\text{Ga}_{1-x}\text{N}$	$\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{P}$ $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{As}$ $\text{In}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{P}_y$	$\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{As}$ $\text{In}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{P}_y$	$\text{Al}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{Sb}_y$ $\text{In}_x\text{Ga}_{1-x}\text{As}_{1-y}\text{Sb}_y$

FIG. 15

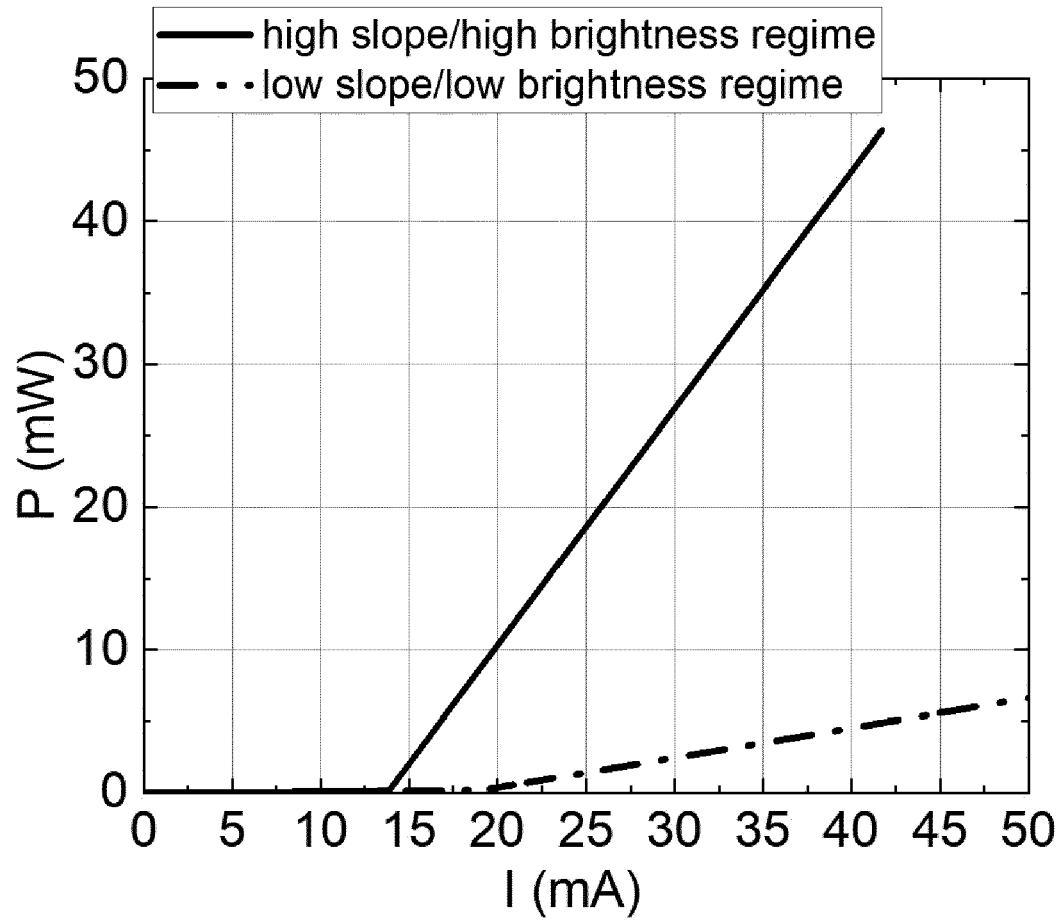


FIG. 16

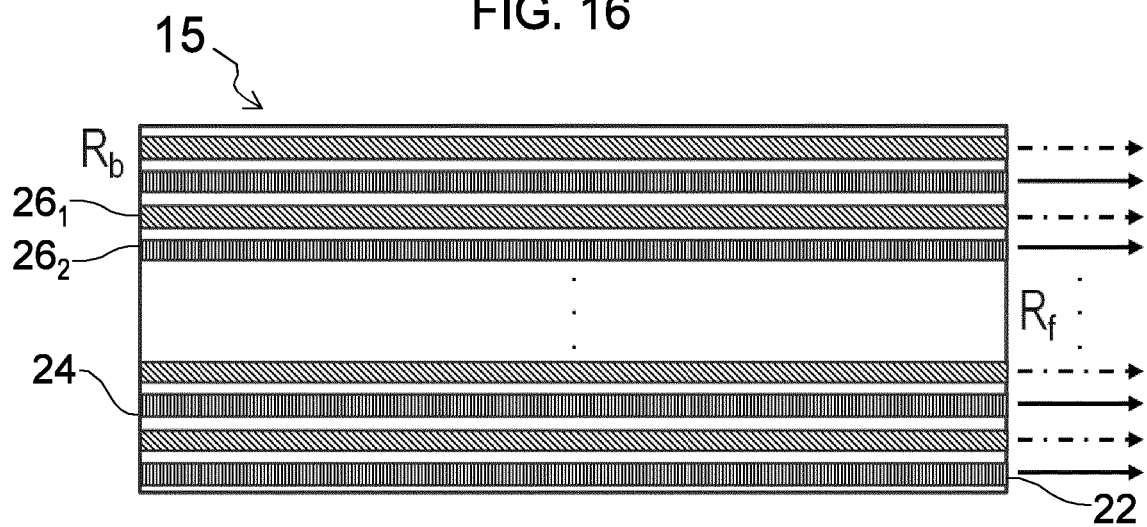


FIG. 17

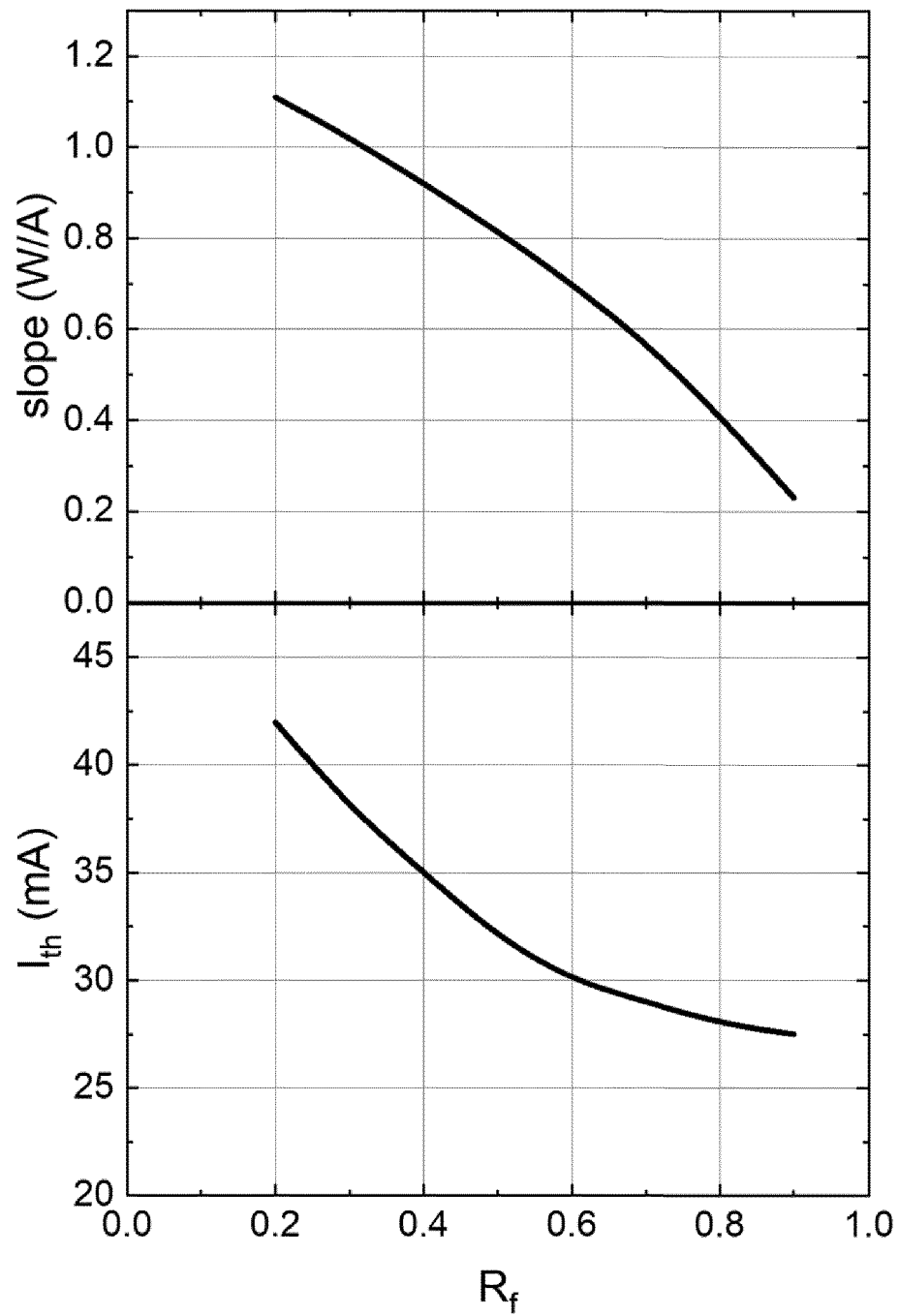
Fixed L & α_i 

FIG. 18A

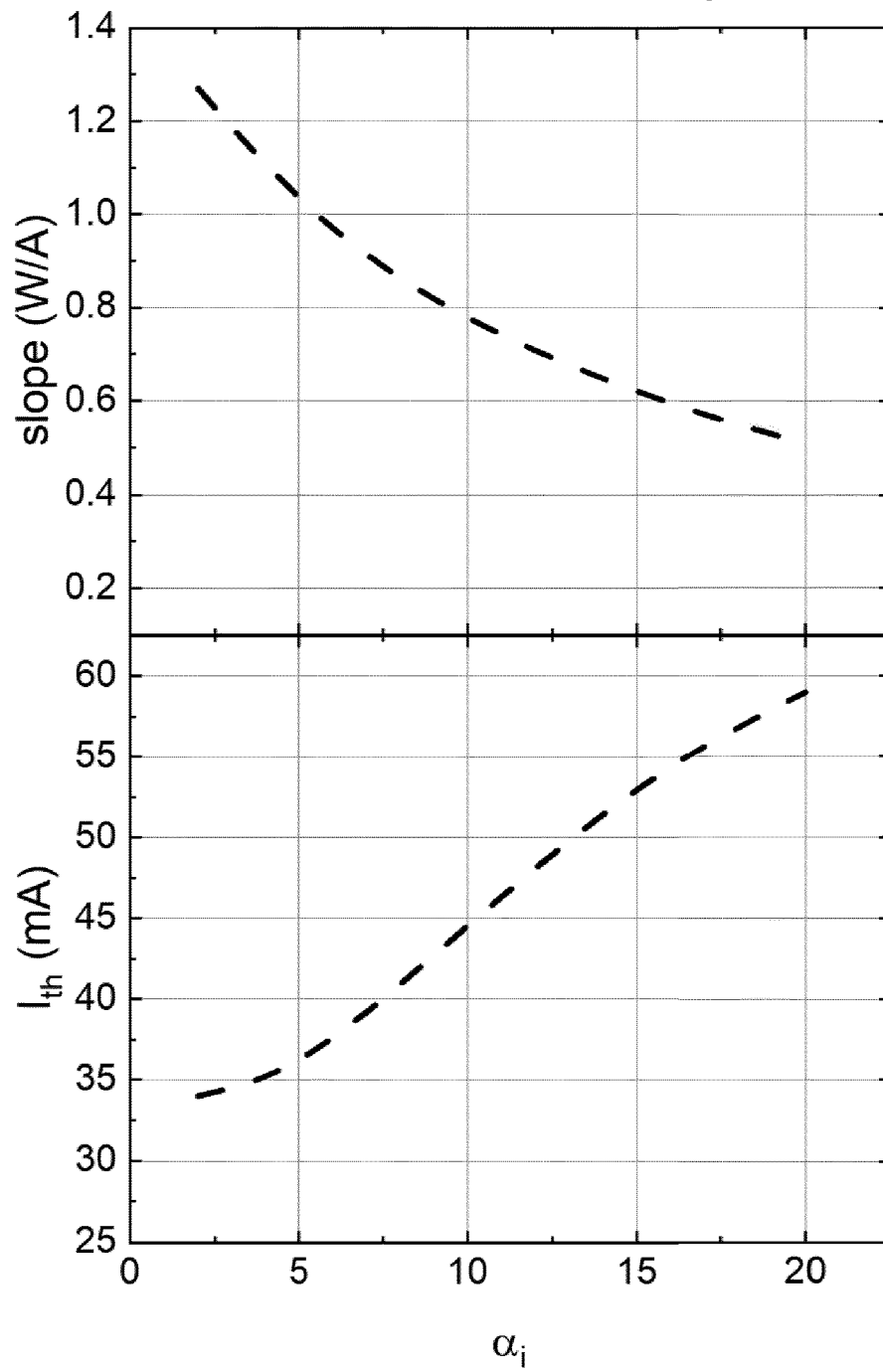
Fixed L & R_f

FIG. 18B

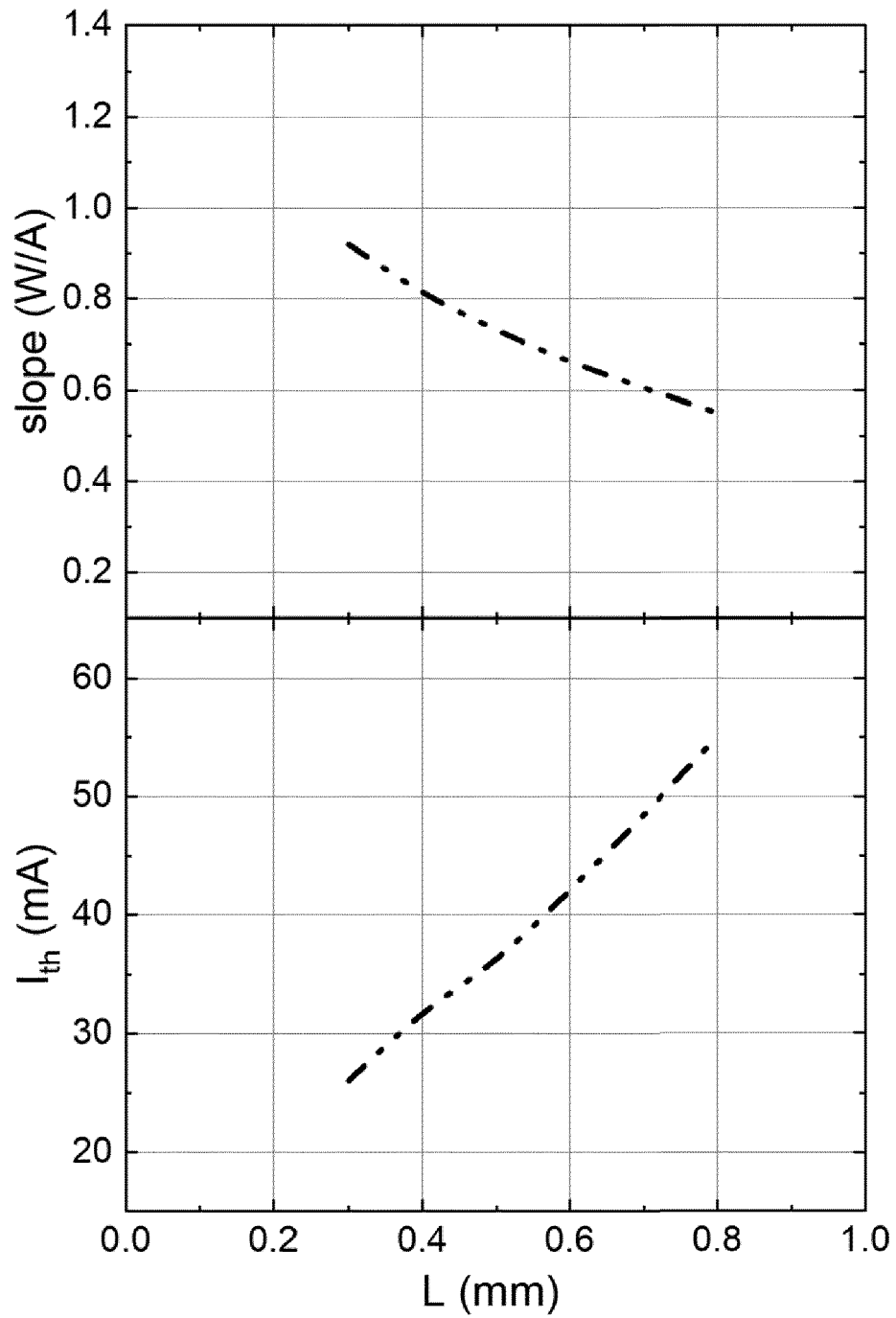
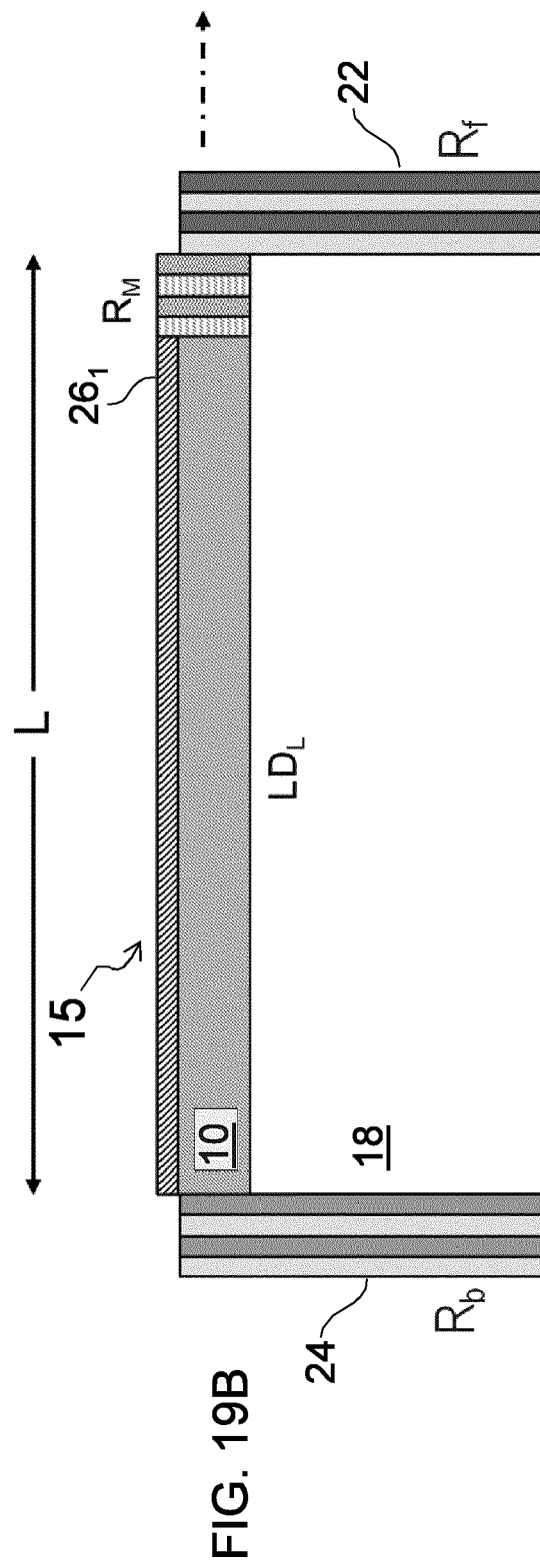
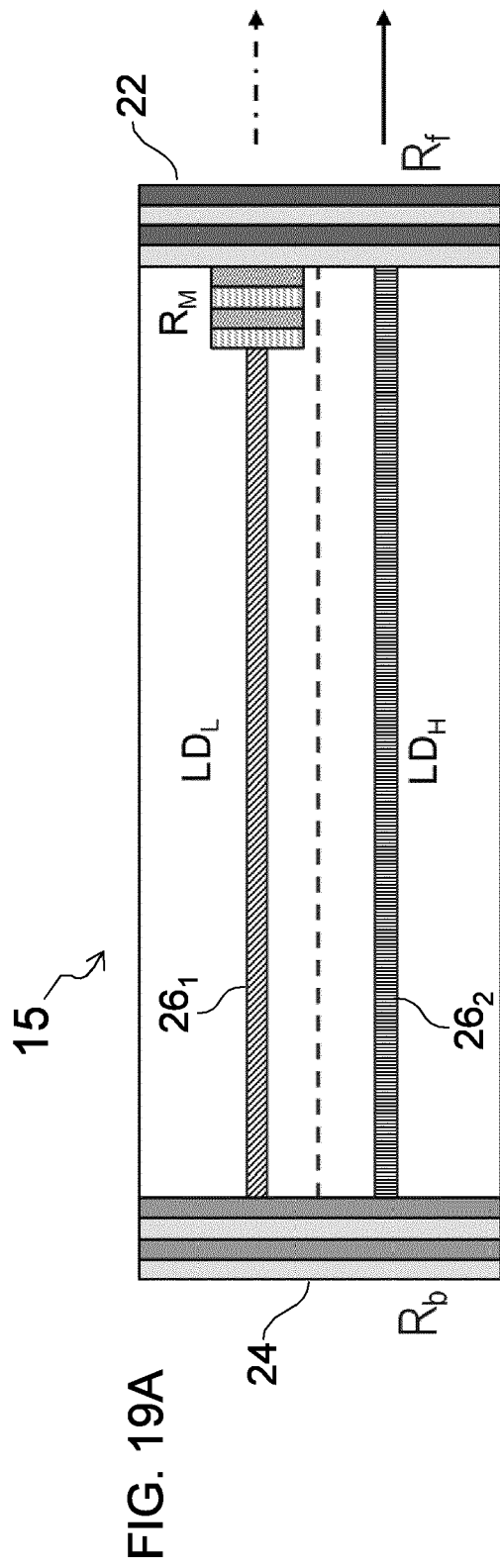
Fixed α_i & R_f 

FIG. 18C



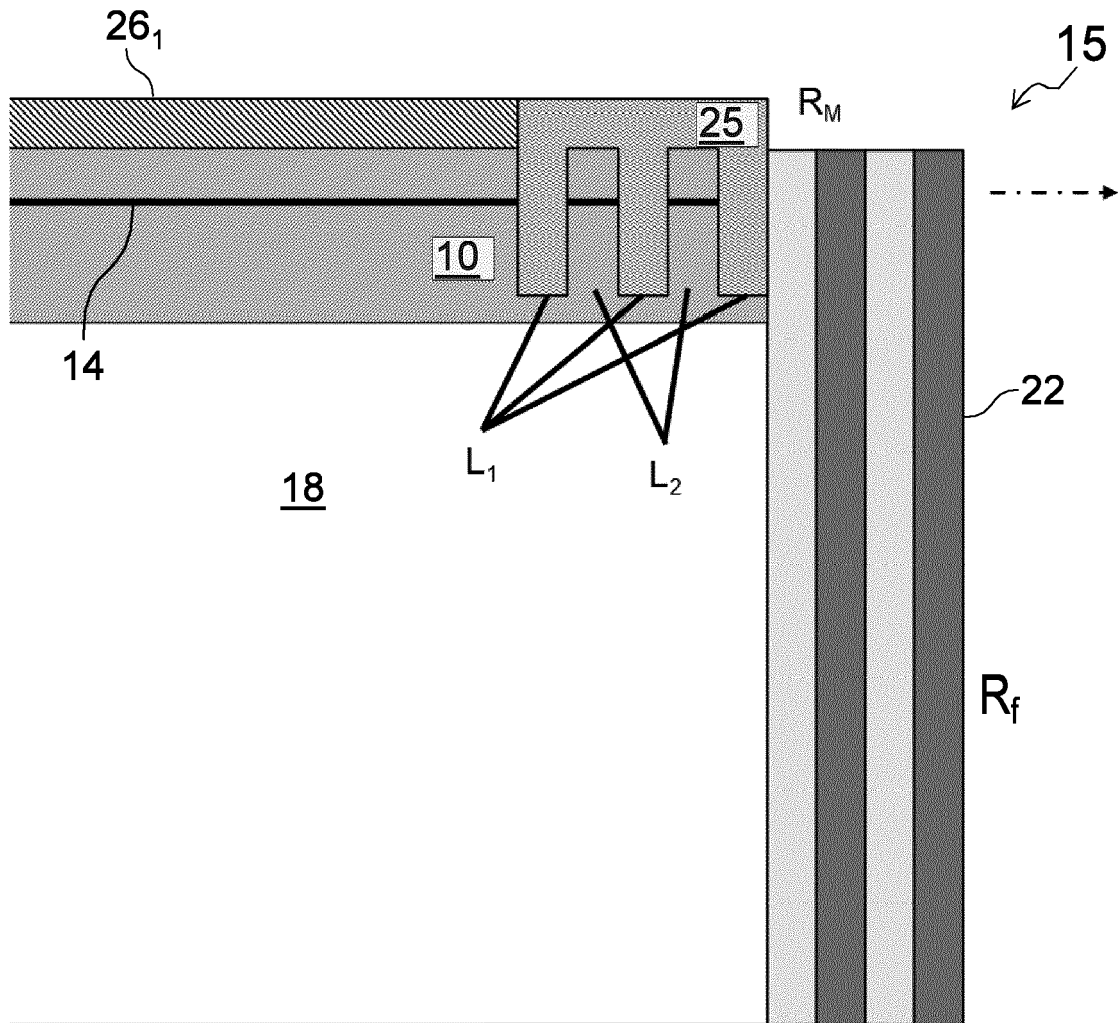


FIG. 20

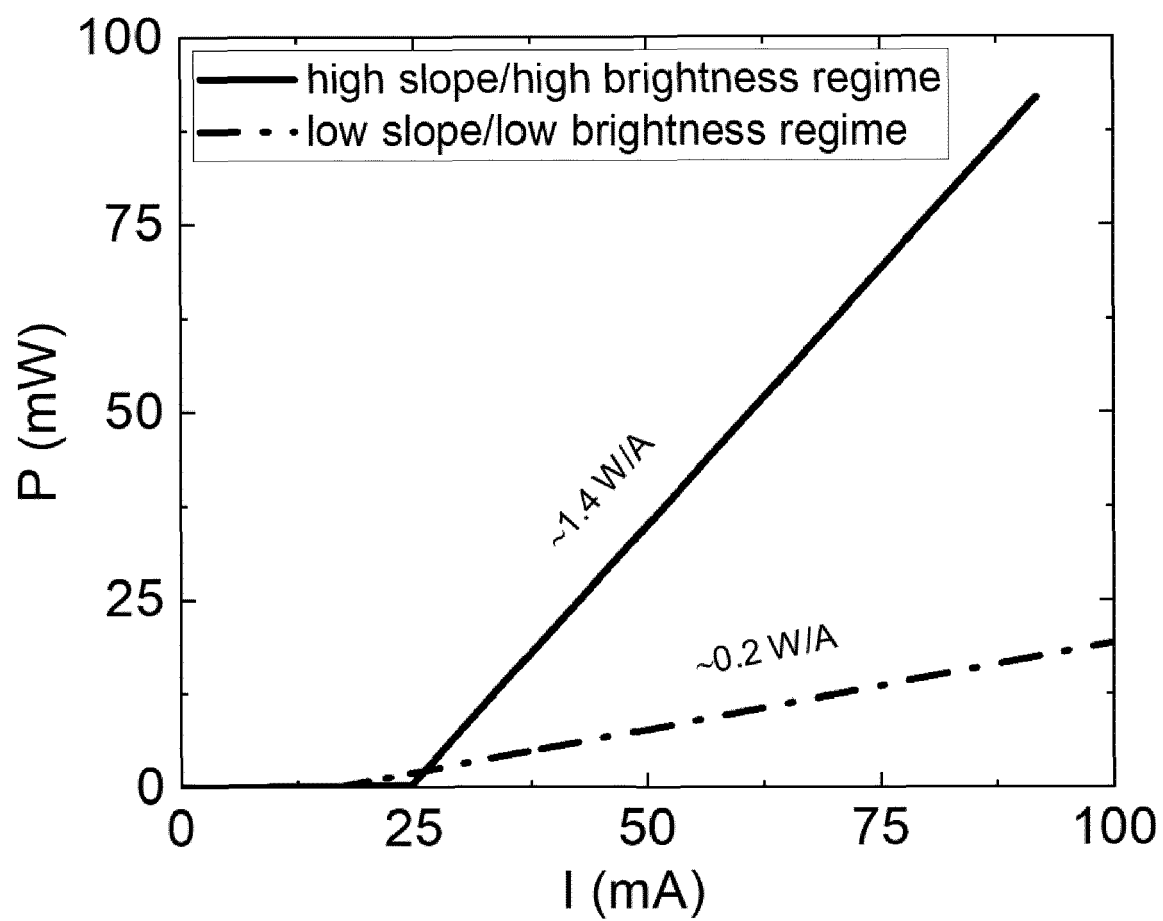


FIG. 21

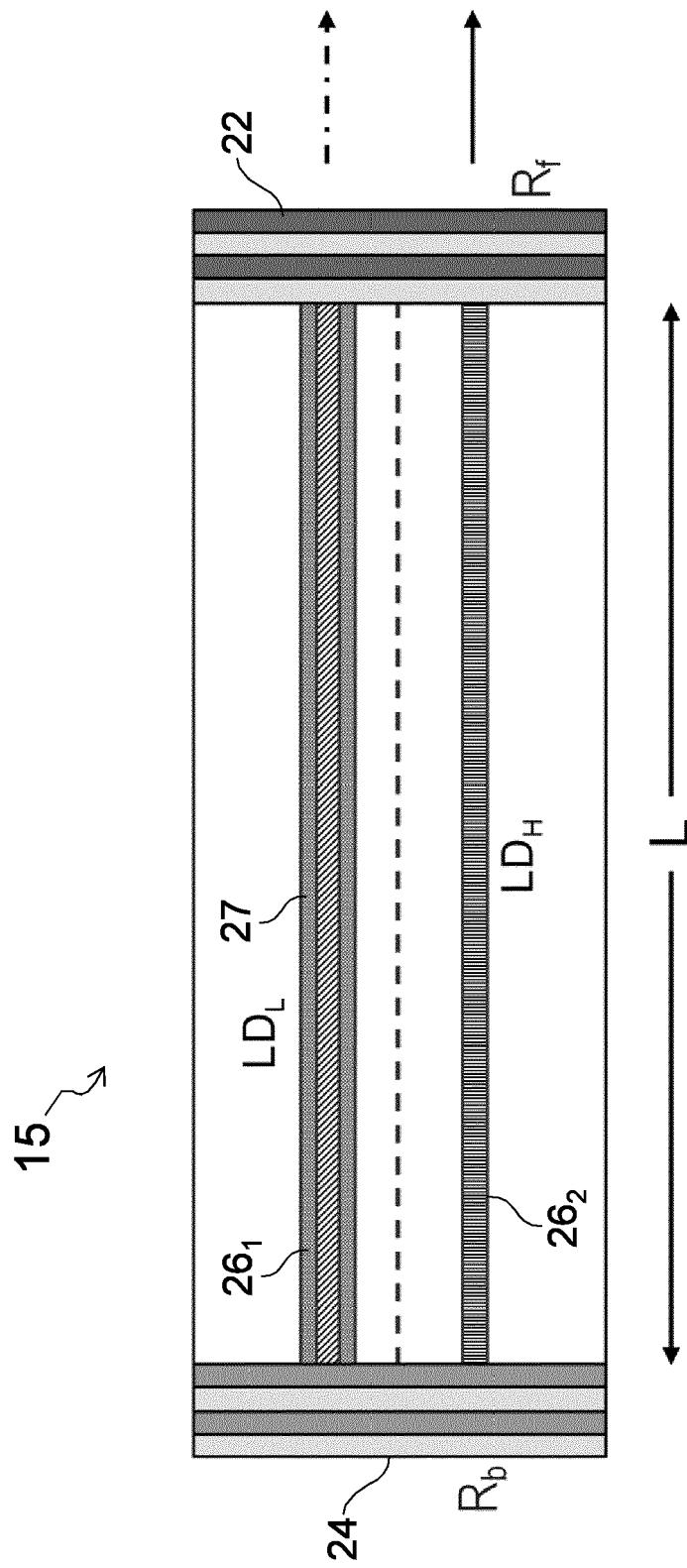


FIG. 22

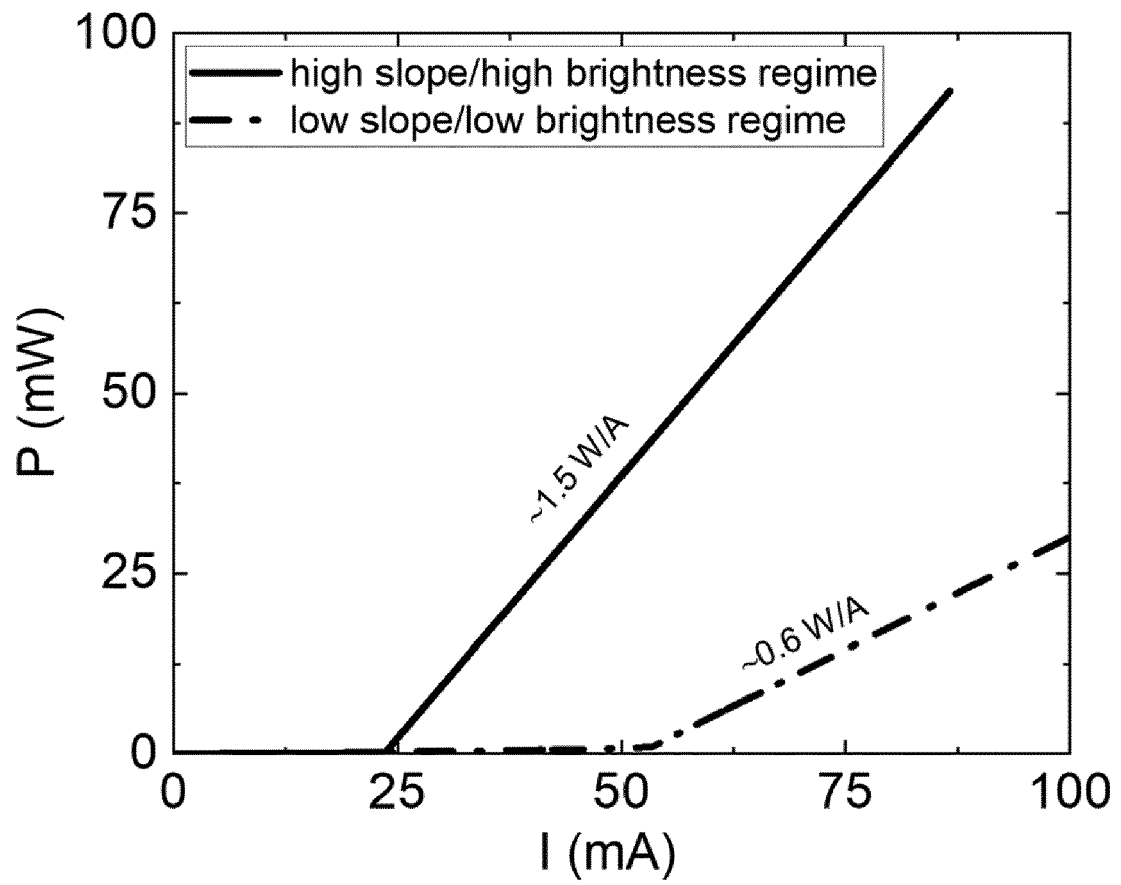
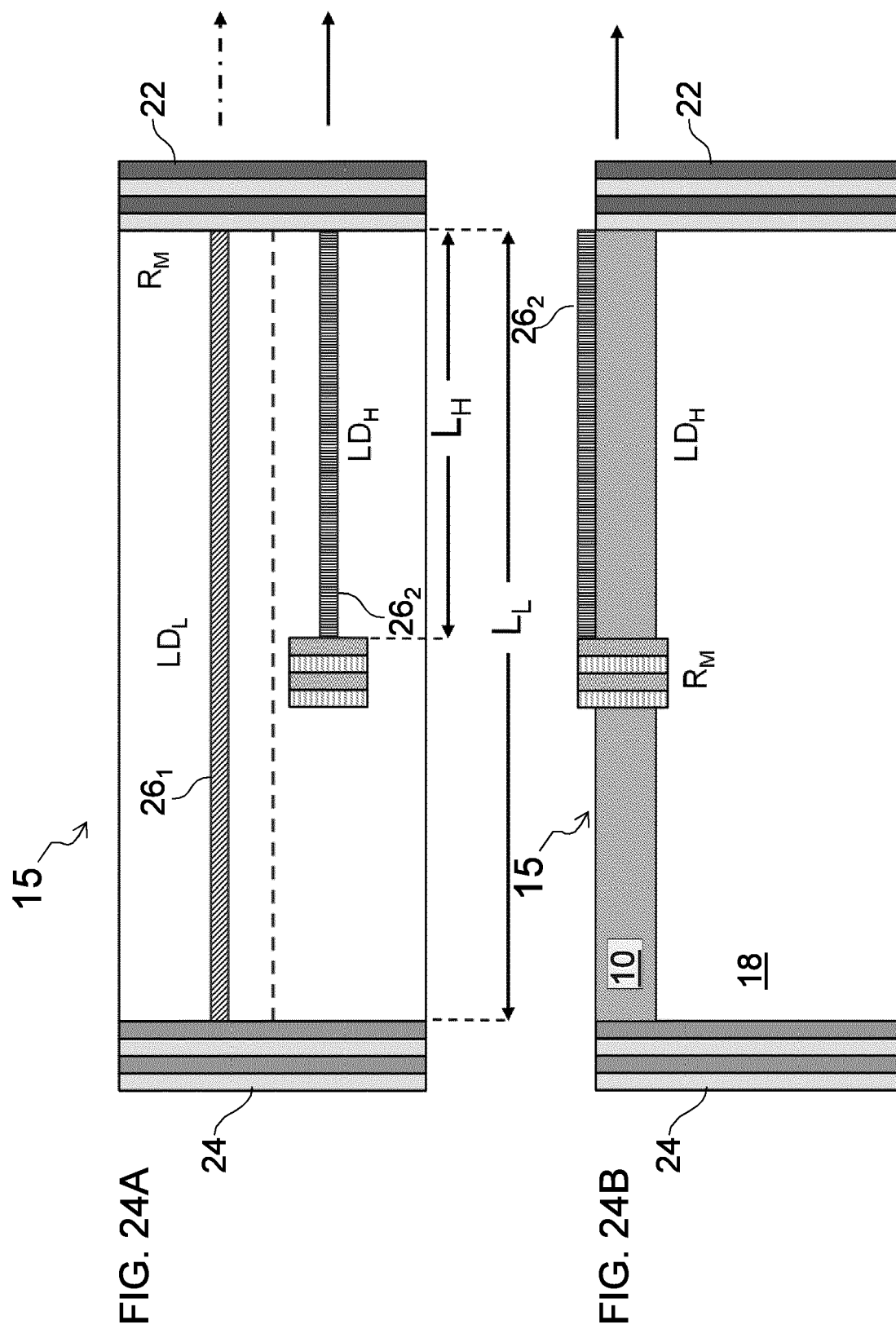


FIG. 23



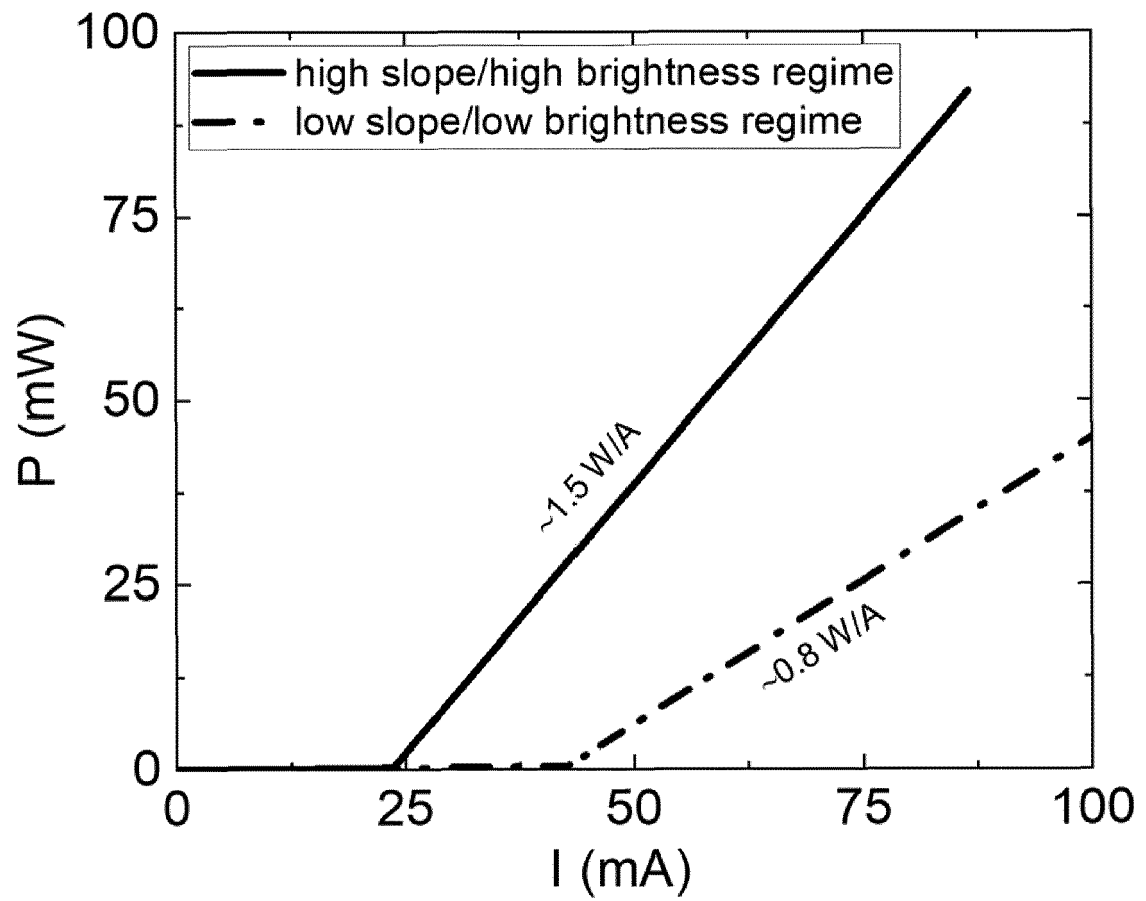


FIG. 25

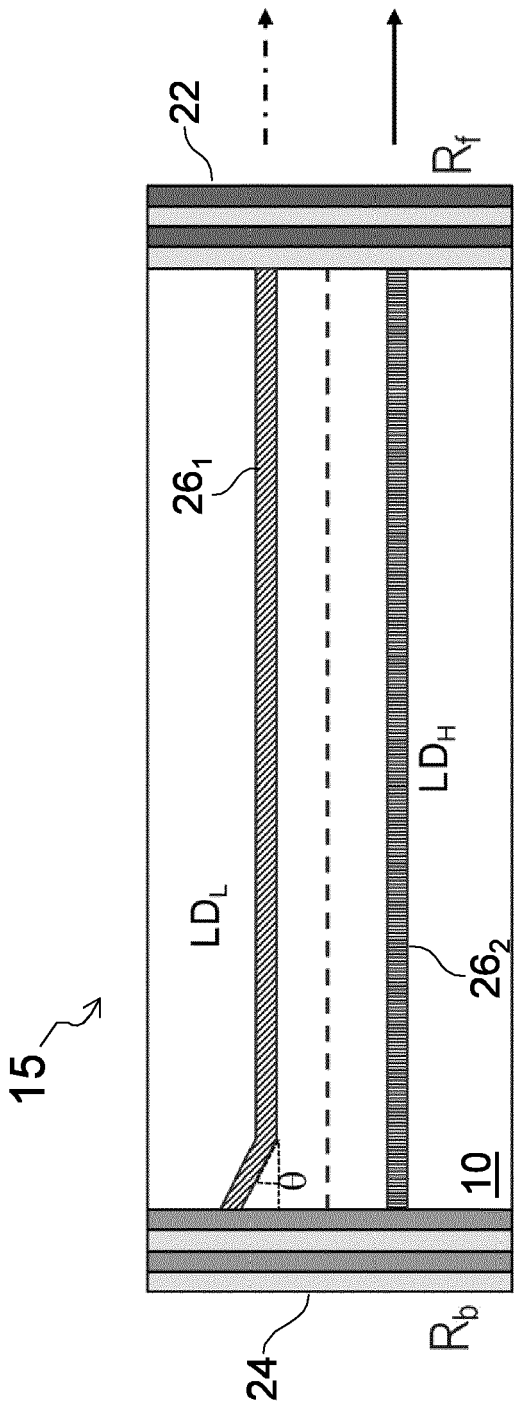


FIG. 26

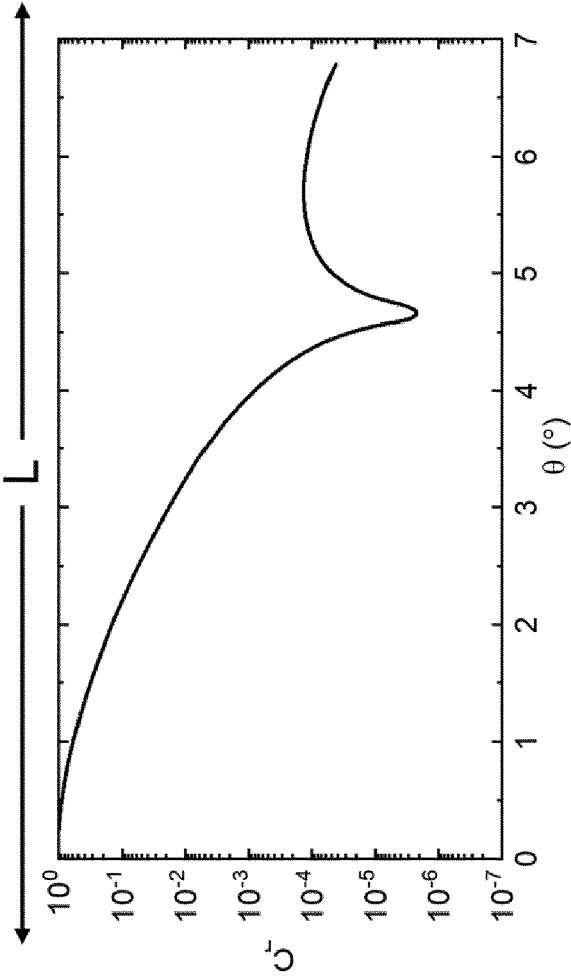


FIG. 27

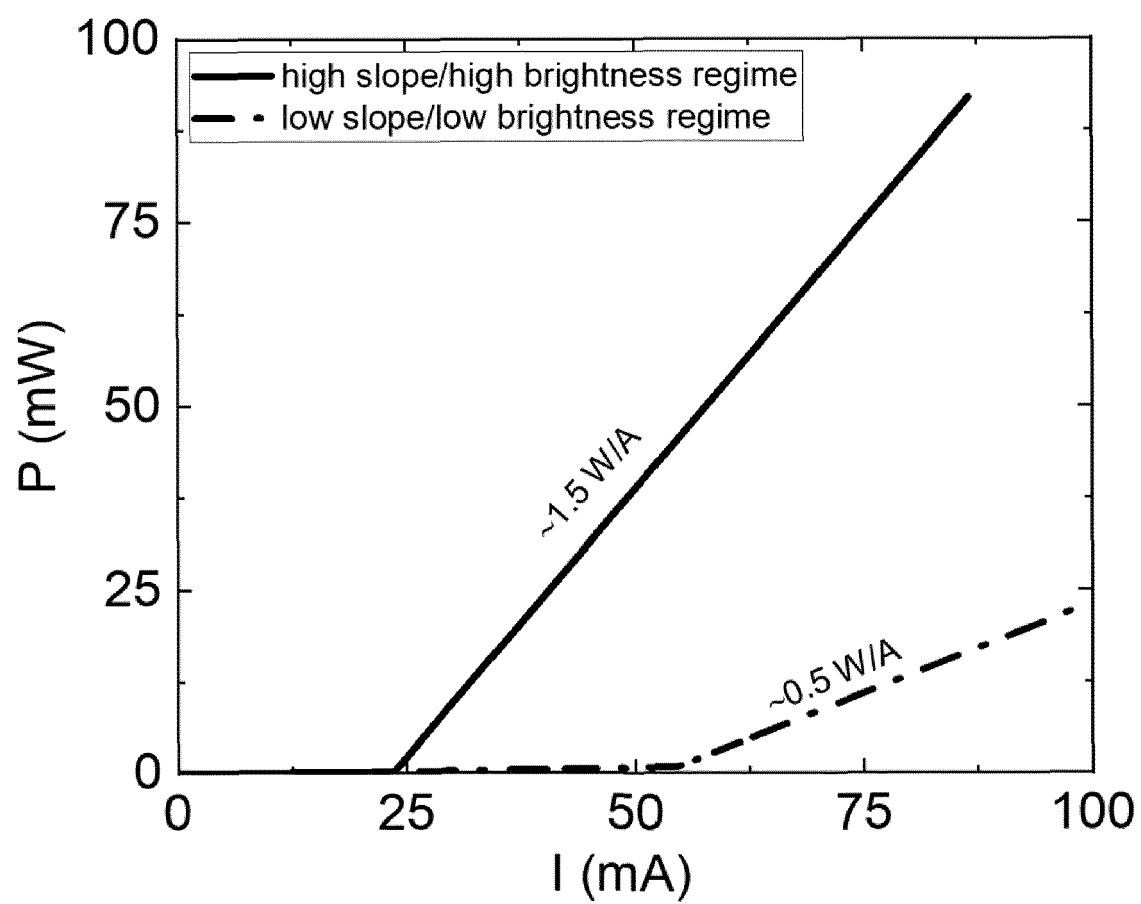


FIG. 28

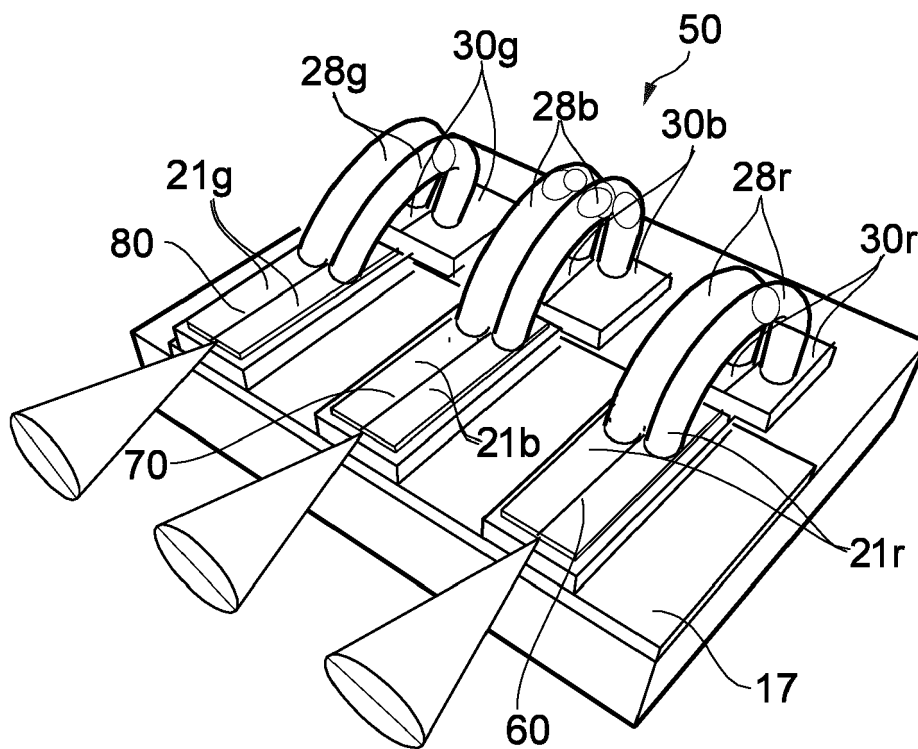


FIG. 29

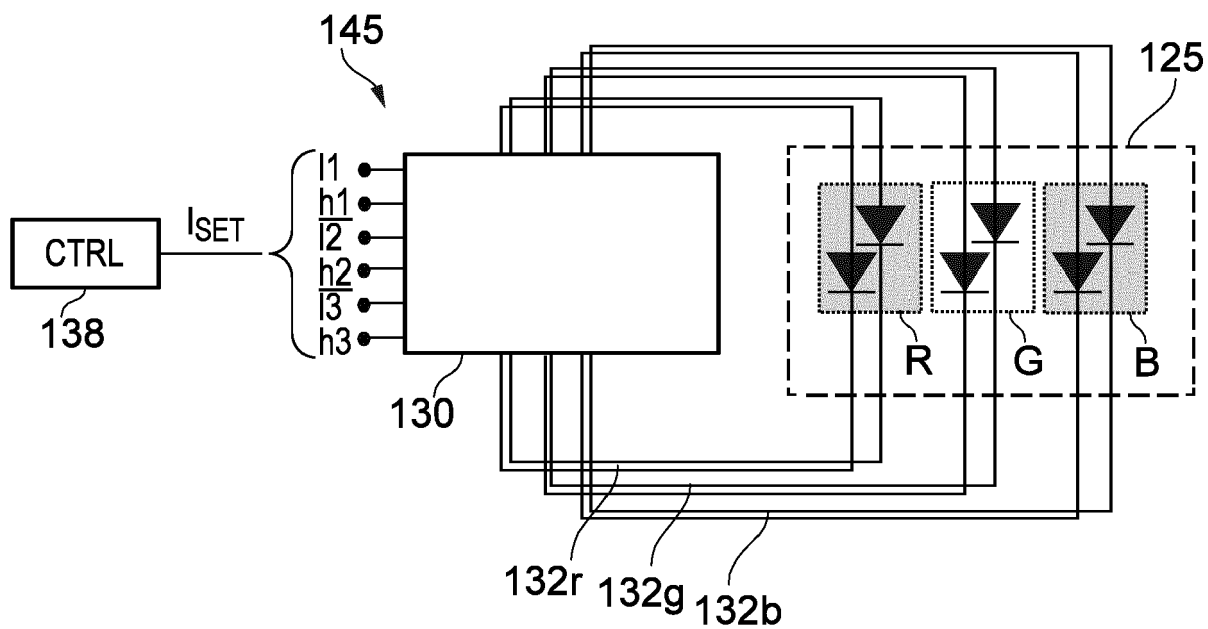


FIG. 30

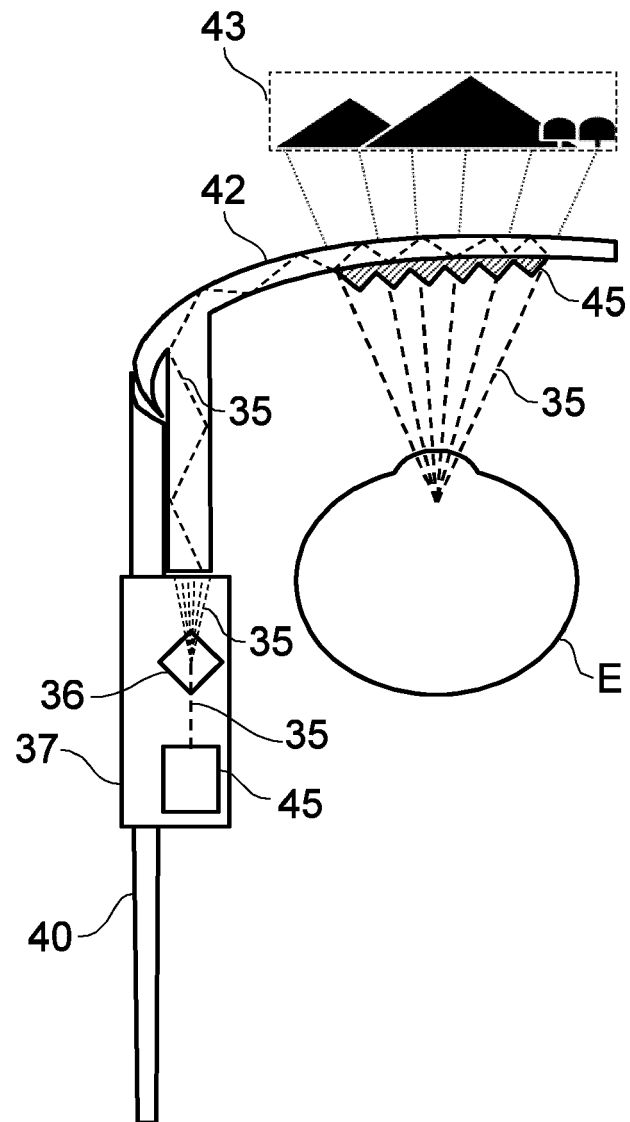


FIG. 31

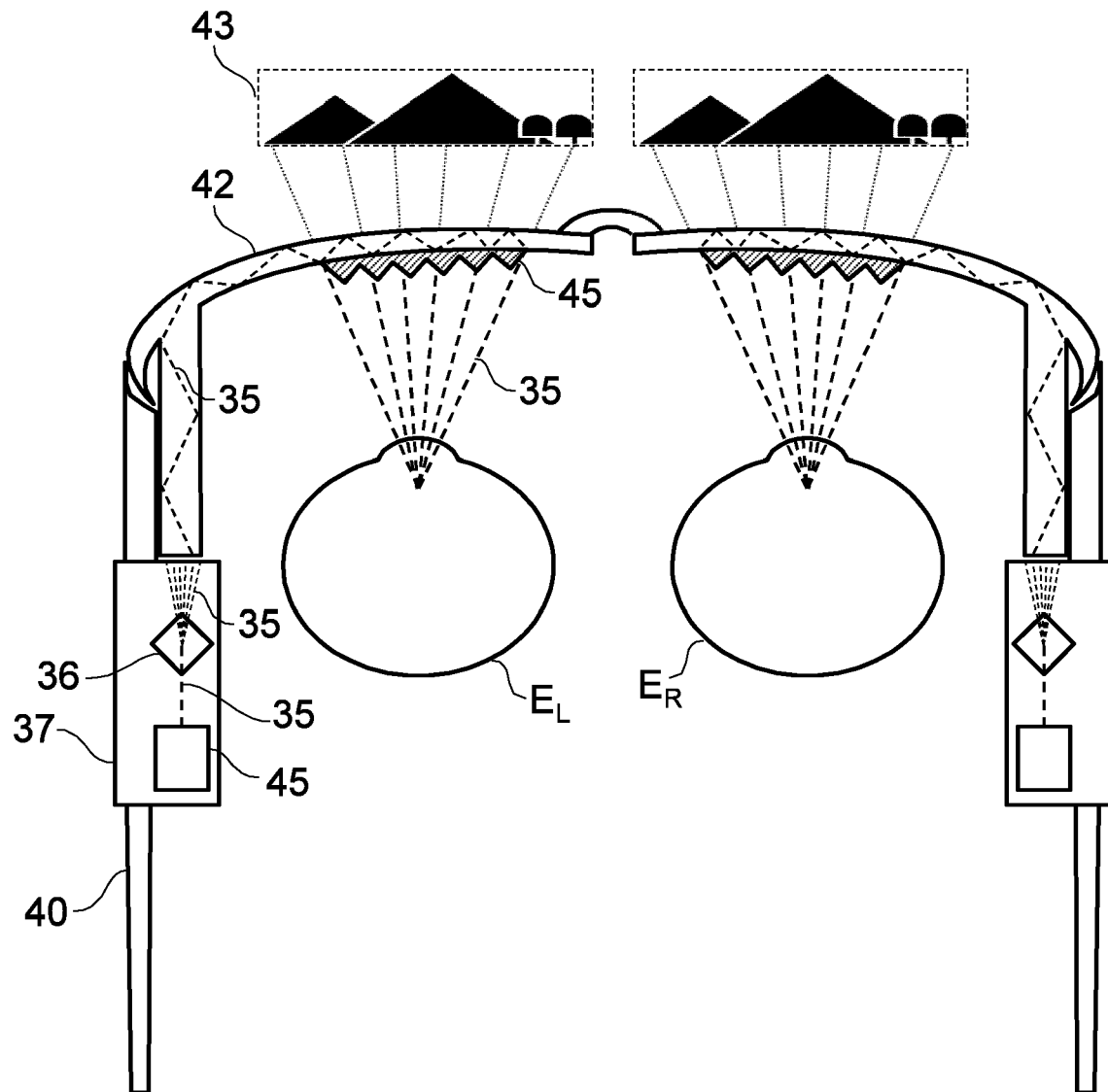


FIG. 32



EUROPEAN SEARCH REPORT

Application Number
EP 21 17 2851

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The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 21 October 2021	Examiner Riechel, Stefan
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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