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(54) **A METHOD FOR PRODUCING AN INTERCONNECT VIA**

(57) The method of the invention is a method for producing an interconnect via (16) that connects a lower conductive line (6) to a transversely oriented upper conductive line (21), wherein the method is configured so that the via is self-aligned to the width of the lower line and to at least the line end of the upper line. This construct is produced by using different interlayer dielectric materials (ILD) which can be etched selectively, one with respect to the other. A layer (1) of a first ILD material is deposited followed by an etch stop layer (3) and an additional layer (4) of an ILD material. The lower conductive line is formed by etching a trench (5) and filling it with a conductive material. Then the trench (above the lower line) is filled with a second ILD material (7), preferably to about the level of the etch stop layer (3). Then the ILD material of the top layer is removed at one side of at least part of the trench, while maintaining a portion (11) of the ILD material on the opposite side of the trench, the remaining portion being self-aligned to said opposite side. The remaining portion of ILD material, along with other masking material, is then used for etching a via opening (14) in the second ILD material, the via opening being self-aligned to the width of the lower conductive line. By filling the via opening and producing a patterned metal layer around the remaining portion (11) of ILD material, the upper line (21) is formed.

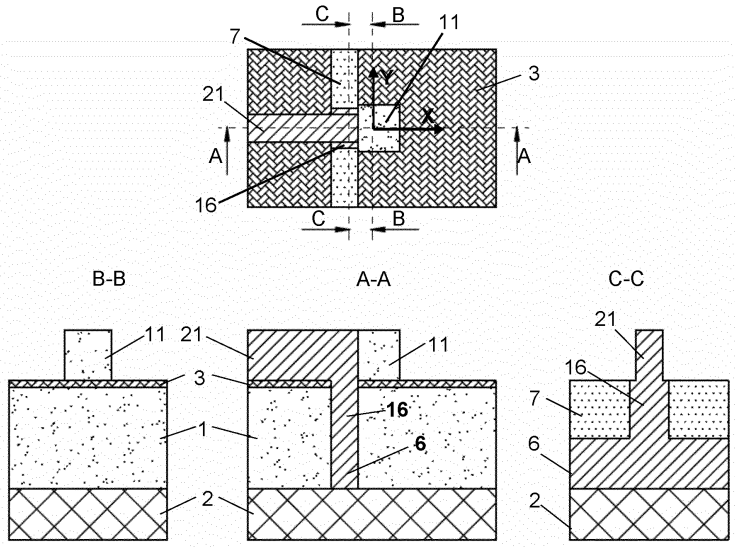

FIG. 1k

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Description

Field of the Invention

[0001] The present invention is related to semiconductor processing, in particular to the fabrication of electrically conductive multi-layer structures, applicable in back end of line processing.

State of the art.

[0002] Semiconductor-based integrated circuits continue to evolve towards shrinking dimensions, leading to ongoing processing challenges. Multilayer conductive structures are typically built as layers of arrays of parallel conductive lines, wherein the arrays of two consecutive levels are arranged crosswise relative to each other, with vias formed between lines of the respective arrays. As dimensions shrink, traditional lithography and etch processes are no longer able to ensure acceptable alignment between a via and the underlying and overlying lines to which the via is connected.

[0003] One example of a particular context in which this problem is encountered is in the interconnect routing to standard logic cells of 2-dimensional layout. As the chip surface area occupied by the standard cells decreases, tip-to-tip spacing between collinear conductive lines in the M1 level of the back end of line decreases accordingly, posing challenges when it comes to connecting the line ends of the collinear conductors to conductors in the underlying and overlying layers. This may also be the case for lines in the M3 level. Self-aligned processing techniques have therefore been developed, enabling constructs which are unattainable by traditional lithography. For example, patent publication document US2016/0197011 discloses a method wherein 'photobuckets' are used, i.e. deposition of material which acts as a photo-sensitive switch, in orderto create a via that is self-aligned to two neighbouring crosswise oriented conductors. This method requires rather a large number of process steps. Patent publication document WO2015/047321 discloses a method for obtaining the same construct, using block copolymers. This process is however not scalable to pitch dimensions in the order of a few tens of nanometres.

[0004] In order to increase the flexibility of semiconductor processing and its adaptability to further shrinking dimensions, further alternatives to these existing methods are therefore required.

Summary of the invention

[0005] The invention aims to provide a solution to the problems and/or required alternatives indicated above. The method of the invention is a method for producing an interconnect via that connects a lower conductive line to a transversely oriented upper conductive line, the upper line having one line end that is aligned with the lower line, wherein the method is configured so that the via is self-aligned to the width of the lower line and to at least the line end of the upper line. According to the invention, this construct is produced by using different interlayer dielectric materials (ILD) which can be etched selectively, one with respect to the other. As known to the skilled person, interlayer dielectric materials are materials suitable for insulating electrically conductive lines in an interconnect structure of a semiconductor component, such as the back and of line (BEOL) stack of an integrated circuit chip. A layer of a first ILD material is deposited followed by an etch stop layer and an additional layer of an ILD material, preferably the same material as the first ILD material. The lower conductive line is formed by etching a trench and filling it with a conductive material, preferably a metal, for example Cu, Co or Ru. Then the trench (above the lower line) is filled with a second ILD material, preferably to the level of the upper surface of the etch stop layer or slightly above said upper surface. Then the ILD material of the top layer is removed at one side of at least part of the trench by etching down to the etch stop layer, while maintaining a portion of the ILD material of said top layer on the opposite side of the trench, the remaining portion being self-aligned to said opposite side. The remaining portion of ILD material, along with other masking material, is then used for etching a via opening in the second ILD material, the via opening being self-aligned to the width of the lower conductive line. By filling the via opening and producing a patterned metal layer around the remaining portion of ILD material, the upper line is formed.

[0006] According to a first embodiment, the 'other masking material' is a hardmask that defines the width of the via opening in the direction of the lower line. According to a second embodiment, the 'other masking material' comprises portions of a third ILD material , said portions being placed on either side of the via opening by preliminary steps of depositing the third ILD material in the trench above the second ILD material, and patterning the third ILD material in accordance with the width of the upper line.

[0007] The first and second embodiment can be applied for fabricating two collinear lines in the upper level, spaced apart by a tip-to-tip spacing that is self-aligned to the distance between adjacent lines in the lower level, and connected to said lower lines by interconnect vias which are self-aligned to the width of the respective lower lines and to at least the line ends of the collinear upper lines.

[0008] The invention is in particular related to a method for producing an interconnect via for a semiconductor component, wherein the via is connected to two electrically conductive lines running in mutually transverse directions, the via being self-aligned at its lower end to the width of a lower electrically conductive line and at its upper end to at least the line end of an upper electrically conductive line, characterized in that the method comprises the steps of :

- producing on a semiconductor base substrate a stack of:
    - A bottom layer of a first intermetal dielectric (ILD) material,
    - An etch stop layer on the bottom layer,
    - A top layer of ILD material on the etch stop layer, wherein the etch stopping function of the etch stop layer is relative to an etch recipe for etching the ILD material of the top layer,
- etching at least one trench through the complete thickness of the stack,
- producing said lower electrically conductive line at the bottom of the trench, i.e. filling a lower portion of the trench,
- producing a layer of a second ILD material in the trench and on top of the lower line, wherein the second ILD material is etchable selectively with respect to the ILD material of the top layer and vice versa, and wherein the second ILD material is also etchable selectively with respect to the etch stop layer,
- by applying one or more etch masks and etching back the ILD material of the top layer and stopping on the etch stop layer, removing the ILD material of said top layer along at least a longitudinal portion of the trench located to one side of the trench, while maintaining the ILD material of the top layer at least along said same longitudinal portion located on the opposite side of the trench, so that a remaining portion of ILD material of the top layer protrudes above the etch stop layer, the remaining portion being self-aligned to said opposite side of the trench,
- etching a via opening through the second ILD material in the trench, using at least the remaining portion of the ILD material of the top layer as a mask, so that the via opening is self-aligned to said opposite side of the trench, along at least a part of said longitudinal portion of the trench,
- producing the upper line and the interconnect via, by depositing an electrically conductive material, thereby filling the via opening, and by producing a patterned layer of the conductive material on top of the interconnect via.

[0009] According to an embodiment, the lower conductive line is formed by filling the trench (5) with an electrically conductive material and etching back the conductive material down to the required thickness of the lower line.

[0010] According to an embodiment, the layer of the second ILD material is produced by filling the trench with said second ILD material and etching back the second ILD material in the trench, selectively with respect to the top layer.

[0011] According to an embodiment, after the step of producing the layer of the second ILD material in the trench, a first mask is applied and the ILD material of the top layer is removed except at the location of the mask, thereby creating said remaining portion of ILD material in the form of a pillar that is self-aligned to said opposite side of the trench, followed, after stripping the first mask, by the application of a second mask configured to define said at least part of the longitudinal portion of the trench, and the upper line is produced by depositing an electrically conductive layer, thereby filling the via opening and enclosing the pillar, and thereafter patterning the electrically conductive layer to thereby form the upper line.

[0012] According to an embodiment, after the step of producing the layer of the second ILD material in the trench, the trench is not completely filled, and a third ILD material is deposited in the trench on top of the layer of the second ILD material, wherein the third ILD material is etchable selectively with respect to the ILD material of the top layer, wherein the second ILD material is etchable selectively with respect to the third ILD material, and wherein the third ILD material is removed from the trench in an area corresponding to the width of the upper line, so that the remaining portions of the third ILD material on either side of said width serve as portions of a mask for etching the via opening, so that the opening is self-aligned to said width of the upper line.

[0013] The method according to the latter embodiment may comprise the steps of :

- Depositing a layer of the third ILD material, thereby filling the trench, and planarizing the layer of the third ILD material until the upper surface of the top layer of ILD material is exposed,
- Applying a first mask that defines the position and width of the upper line,
- Removing the third ILD material from the trench, in an area defined by the first mask and by the ILD material of the top layer,
- With the first mask in place, applying a second mask which covers the ILD material of the top layer to said opposite side of the trench, while leaving the ILD material of the top layer on said one side of the trench exposed in an area corresponding to the upper line,
- With both masks in place, etching the ILD material of the top layer, stopping on the etch stop layer, and stripping the masks, thereby obtaining the remaining portion of ILD material that is self-aligned to said opposite side of the trench, while creating a transverse trench in the top layer on the other side of the trench, the transverse trench defining the position of the upper line,
- Etching the via opening, using at least the ILD material of the top layer, the etch stop layer and the third ILD material as a mask,
- Filling the via opening and the transverse trench with an electrically conductive material, thereby obtaining the interconnect via and the upper line.

According to an embodiment, two interconnect vias are produced, connecting a first and second mutually parallel

lower line respectively to a first and second collinear upper line, the interconnect vias being self-aligned to the width of the respective lower lines and to at least the line ends of the respective upper lines.

[0014] According to an embodiment, the ILD material of the top layer is the same as the first ILD material.

[0015] The invention is equally related to a semiconductor component comprising a semiconductor base substrate and on this base substrate a front end of line portion and a back and of line portion, the back end of line portion comprising multiple levels (M0,M1,...) of interconnected electrical conductors, the levels being interconnected by interconnect vias, and wherein the BEOL portion comprises an interconnect via that is connected to two electrically conductive lines running in mutually transverse directions, the via being self-aligned at its lower end to the width of a lower electrically conductive line in a level M_x of the BEOL portion and at its upper end to at least the line end of an upper electrically conductive line of a level M_{x+1} of the BEOL portion, the electrically conductive lines and the interconnect via being embedded in at least two different ILD materials,
characterized in that:

- at least said line end of the upper line is in direct contact with a portion of ILD material,
- in the direction of the lower line, the interconnect via is isolated on both sides by a second ILD material, that is etchable selectively with respect to the ILD material of said portion in direct contact with the line end of the upper line and vice versa,
- an etch stop layer is present underneath the upper line, wherein the etch stopping function of the etch stop layer is relative to an etch recipe for etching the ILD material of said portion in direct contact with the line end of the upper line.

[0016] The invention is also related to a semiconductor substrate comprising at least one level of a multilevel interconnect structure, said at least one level comprising a line-shaped conductor oriented in a given direction and embedded in a layer of a first ILD material, said layer having a thickness higher than the conductor, wherein the conductor is located at the bottom of a trench through said layer of the first ILD material, the substrate further comprising :

- an etch stop layer on the first layer of the first ILD material, and a portion of an ILD material extending above the etch stop layer and being aligned to one side of the trench, wherein the etch stopping function of the etch stop layer is relative to an etch recipe for etching the ILD material of said portion extending above the etch stop layer,
- an elongate portion of a second ILD material that is selectively etchable with respect to the material of the portion extending above the etch stop layer and vice versa, the second material also being selectively etchable with respect to the etch stop layer, said elongate portion being present on top of the conductor, the elongate portion of the second ILD material being interrupted by a via adjacent to the ILD portion extending above the etch stop layer.

Brief description of the figures

[0017]

Figures 1a to 1l illustrate key steps of a first embodiment of the method of the invention.
Figures 2a to 2g illustrate key steps of a second embodiment of the method of the invention.
Figures 3a to 3j illustrate the first embodiment, applied for producing two interconnect vias from the line ends of two collinear lines to underlying transverse and mutually parallel lines.
Figures 4a to 4h illustrate the second embodiment, applied for producing two interconnect vias from the line ends of two collinear lines to underlying transverse and mutually parallel lines.

[0018] Section views along planes A-A, B-B and C-C indicated in the drawings show the sections as such, not what lies behind the section planes.

Detailed description of the invention

[0019] A first embodiment of the method of the invention is described with reference to Figures 1a to 1l. As shown in Figure 1a, a layer 1 of a first interlayer dielectric material (ILD) is deposited on a substrate 2. An etch stop layer 3 is deposited on top of the ILD layer 1, followed by a further layer 4 of the first ILD. The ILD material of the top layer 4 could however be a different ILD material than the material of layer 1. The etch stopping function of the etch stop layer 3 is relative to an etch recipe for etching the ILD material of the top layer 4, i.e. the first ILD material in this case. The first ILD material of layers 1 and 4 could be SiCO. The etch stop layer 3 could be a layer of SiN. When these materials are used, the thickness of layer 1 could be about 20nm, the thickness of layer 3 could be about 10nm and the thickness of layer 4 could be about 20nm. These materials and thicknesses are however merely exemplary. Depending on the material choice, and as depicted in the drawings, the etch stop layer 3 can be thinner relative to the ILD layers 1 and 4 than in the above-named example. The images show a top view and cross sections of a small portion of the substrate 2 and the layers 1,3 and 4, said portion being configured to contain the specific construct of conductive lines coupled by a via, to be processed in accordance with the invention.

[0020] The substrate 2 could be a device wafer, i.e. a wafer comprising several integrated circuit chips, each chip comprising a large number of semiconductor devices, for example transistors arranged in multiple 2-dimen-

sional standard logic cell arrangements. The requirement is then to form a lower metal level M0 comprising conductive lines connected directly to the semiconductor devices according to a predefined connection design, and above M0 an upper metal level M1 comprising conductive lines running transversely to the M0 lines and connected to the M0 lines by multiple via interconnects. The method of the invention is suitable for producing such a construct, not only at the deep levels M0-M1 of the back end of line (BEOL) interconnect structure of an integrated circuit, but in fact at any pair of consecutive levels located anywhere in the BEOL stack. So generally, the substrate 2 could be a device wafer including a partially processed BEOL stack, the top level corresponding to level M_{x-1}. The method of the invention is then applicable for producing levels M_x and M_{x+1}, interconnected by interconnect vias between the two.

[0021] Especially at the deeper levels, the conductive lines are arranged in closely spaced arrays of parallel lines, and an example of applying the method of the invention to such an arrangement is given further in this description, wherein it is demonstrated that the method of the invention enables a very tight tip-to-tip spacing between two collinear lines in the upper level, the line ends of the collinear lines being connected by self-aligned interconnect vias to two adjacent parallel lines in the lower level. However In order to focus on the main characteristics, an embodiment is first described wherein a single lower metal line of a lower level M_x is connected to a single upper metal line of upper level M_{x+1}, by a single metal interconnect via. Any electrically conductive material is applicable apart from a metal, but metal interconnects are most widely used and are therefore applied in the context of the detailed description.

[0022] The combined thickness of the layer 1 of the first ILD and the etch stop layer 3 corresponds to the combined thickness of the eventual lower interconnect level M_x and the height of the interconnect via. The top layer 4 is preferably somewhat higher than the eventual thickness of the upper level M_{x+1}, in order to take into account a degree of thinning ofthis layer 4 during multiple planarization and/oretch steps performed during the method (see further).

[0023] As illustrated in Figure 1b, a trench 5 is formed in the stack of layers 1+3+4 and filled with a metal, for example Cu, Ru or Co, after which the metal in the trench is recessed to form the lower conductive line 6. Etching of the trench 5 requires different etch recipes, as the etch takes place through different materials, namely the first ILD material (layers 1 and 4), and the etch stop layer 3. Etch recipes as such for etching suitable materials for these layers (as in the example mentioned above) are known per se and not detailed here. Due to the use of different etch recipes, the walls of the trench 5 may slightly differ from the straight walls illustrated in the drawings.

[0024] The recessing of the metal in the trench 5 may be done by standard lithography+etching, using a first hardmask (not shown) that defines the position of the trench 5. After stripping the first mask, metal is deposited in the trench 5 and on the surface of the ILD layer 4, the metal deposition being possibly preceded by the formation of a diffusion barrier (not shown) conformally in the trench 5. Chemical Mechanical Polishing according to known recipes may be used to planarize the deposited metal to become level with the upper surface of the top ILD layer 4, possibly slightly thinning the ILD layer 4. Recessing the metal may be done by known dry or wet etching by a suitable etch recipe that removes the metal relative to the ILD layers 1 and 4 and relative to the etch stop layer 3. A timed etch may be used to stop the etch process when the required thickness of the lower line 6 is reached. What remains is the trench 5 with the line 6 at its bottom, as shown in Figure 1b. An alternative way of producing the line 6 is by depositing metal only at the bottom of the trench 5, by a local deposition technique such as area-selective atomic layer deposition (ALD) wherein a layer of metal is built from the bottom up, starting from the bottom of the trench 5, until reaching the required line thickness.

[0025] As illustrated in Figures 1c and 1d, the trench 5 is filled (i.e. the portion of the trench above the line 6), with a second ILD material 7 different from the first ILD material after which the second ILD material 7 is recessed in the trench 5. An alternative way of producing the layer 7 of Figure 1d is to deposit the second ILD material locally on top of the metal line 6 in the trench, and building up the layer 7 from the bottom up, for example by area-selective ALD, until reaching the required thickness of the layer 7. In the embodiment shown, this thickness is such that the upper surface of layer 7 is at the same level as the upper surface of the etch stop layer 3. Depending on the materials chosen and the applicable embodiment (layer 7 is present according to any embodiment of the invention), the upper surface of layer 7 may be lower or higher than the etch stop layer 3, or between the upper and lower surface of the etch stop layer 3. According to a preferred embodiment, the upper surface of the recessed layer 7 is slightly higher than the upper level of the etch stop layer 3.

[0026] The second ILD material 7 is chosen on the basis of etch selectivity with respect to the ILD material of the top layer 4 and with respect to the etch stop layer 3. To be more precise, etch recipes must be available by which it is possible to :

- etch the ILD material of the top layer 4 selectively with respect to the second ILD material and vice versa, i.e. the one material can serve as a mask for anisotropic etching of the other.
- etch the second ILD material of layer 7 selectively with respect to the etch stop layer 3 i.e. the etch stop layer can serve as a mask for anisotropic etching of the second ILD material.

The nature of these etch recipes is known per se for various choices of the ILD materials and the etch stop ma-

terial, and are therefore not detailed in this description. The result in Figure 1d can be obtained by depositing a layer of the second ILD material 7 that fills the trench 5 and covers the upper ILD layer 4, followed by thinning and planarizing the layer by CMP to the upper level of the first ILD material of layer 4 (possibly slightly thinning the latter) to arrive at the situation shown in Figure 1c, and recessing the second ILD material 7 in the trench by a timed wet or dry etch, using one of the above-referenced selective etch recipes known in the art. When the first ILD material is SiCO, the second ILD material can be SiO_2.

[0027] Then, as shown in Figure 1e, a second hardmask 10 is formed, partially covering the trench 5, as well as covering a portion of the upper ILD layer 4 to one side of the trench 5. This is followed by anisotropic etching of the first ILD material of layer 4, stopping on the etch stop layer 3, and by stripping of the hardmask 10, resulting in the situation shown in Figure 1f. A local pillar 11 of the first ILD material remains, to one side of the trench 5, and perfectly aligned with the edge of said trench.

[0028] A third hardmask 12 is now formed, as shown in Figure 1g, covering the etch stop layer 3 around the remaining pillar 11, except for an opening 13 which overlaps both the trench 5 and the remaining pillar 11. In the vertical direction (the Y-direction of the X-Y orthogonal axes indicated in the drawing), the opening is more narrow than the pillar 11. In the X-direction, the opening exposes the full width of the trench 5 and the pillar 11, and a portion of the etch stop layer 3 on either side thereof.

[0029] Now, an anisotropic etch process is applied that removes the second ILD material 7 relative to the first ILD material of the pillar 11 and relative to the etch stop layer 3, and stopping on the metal line 6 (either by a timed etch or through etch selectivity relative to the metal of line 6), resulting in the creation of a via opening 14 in the trench 5, after which the third mask 12 is stripped, see Figure 1h. The via opening is therefore created using the mask 12, the pillar 11 and the etch stop layer 3 as mask material. The via opening 14 is self-aligned to the pillar 11 in the Y-direction, i.e. along the longitudinal direction of the trench 5. In the X-direction, the via opening 14 is self-aligned to the width of the conductive line 6.

[0030] Then a metal layer 15 is deposited over the entire surface of the etch stop layer 3 (Figure 1i). The metal fills the via opening 14, thereby creating the interconnect via 16 that is self-aligned to the width of the lower conductive line 6. The metal layer 15 is planarized to the height of the pillar 11 formed of the first ILD material (possibly slightly reducing the height of this pillar).

[0031] Then a fourth hardmask 20 is applied that defines the width of the upper conductive line, as shown in Figure 1j. The mask 20 covers the planarized metal layer 15 along a line which fully overlaps the trench 5 and which partially overlaps the pillar 11. The metal layer 15 is anistropically etched, selectively with respect to the pillar 11, and stopping on the etch stop layer 3 and on the layer 7 of the second ILD material. If the upper surface of the layer 7 is not at the same level as the upper surface of the etch stop layer, the etch of the metal 15 continues at least until all metal is removed from the top of the layer 7.

[0032] Then the fourth hardmask 20 is stripped (see Figure 1k), leading to the required metal construct, comprising a lower line 6, an interconnect via 16 and an upper line 21. The interconnect via 16 is self-aligned to the width of the lower line 6 and to the line end of the upper line 21. Finally, the upper line 21 is embedded in an additional layer 22 of the first ILD material, see Figure 1l, which is planarized to the level of the upper line 22. Layer 22 could also be another ILD material than the first.

[0033] According to a second embodiment, the same construct is produced, but now the interconnect via is fully aligned to the lower and upper conductive lines, in both the X and Y directions. To do this, a third interlayer dielectric material is required. The third ILD material must be etchable selectively with respect to the ILD material of the top layer 4, i.e. the top layer 4 can serve as a mask for anistropically etching the third ILD material. Furthermore, the second ILD material of layer 7 must be etchable selectively with respect to the third ILD material, i.e. a layer of the third ILD material can serve as a mask for anisotropically etching the second ILD material. When the first and second ILD materials are SiCO and SiN, the third ILD material could be SiCN. The steps are the same up to and including the step resulting in the situation shown in Figure 1d. Now however, the third ILD material 25 is deposited in the trench 5, and planarized to the level of the upper layer 4 of the first ILD material (possibly slightly thinning layer 4), as illustrated in Figure 2a. Then a second hardmask 26 (the first being the one used for etching the trench 5) is formed which defines the width of the eventual upper conductive line, see Figure 2b. The mask 26 covers the whole surface except for an opening 27 having the width of the upper line. The opening 27 extends to one side of the trench 5, while also overlapping the trench itself and a portion of the first ILD material of layer 4 on the opposite side of the trench 5.

[0034] As shown in Figure 2c, the third ILD material 25 is then removed by anisotropic etching, within the mask opening 27, relative to the ILD material of the top layer 4 and stopping on the second ILD material 7 in the trench (by a timed etch or because the etch of the third ILD material 25 is selective with respect to the second ILD material 7), creating a partial via opening 28 that is self-aligned to the side of the trench 5 and to the width of the mask opening 27.

[0035] Then a third mask 29 is formed in addition to the second mask 26, see Figure 2d. The third mask 29 covers one side of the trench 5 along a longitudinal portion thereof, as well as the first ILD material of the top layer 4 to said one side of the trench 5. With the two masks 26 and 29 in place, the first ILD material of the top layer 4 is removed within the opening 30 defined by the two masks, by etching the first ILD material of the top layer 4 relative to the second ILD material 7, and stopping on the etch stop layer 3. Both masks 26 and 29 are then

stripped, resulting in the situation shown in Figure 2e : along line A-A, the first ILD material of the top layer 4 is removed at one side of the trench, and a remaining portion 11 of the top layer 4 is maintained at the opposite side of the trench, the remaining portion being self-aligned to said opposite side of the trench. Opposite said remaining portion 11, a second trench 31 is formed, extending in the X-direction and overlapping the first trench 5, and with the end face of the second trench 31 self-aligned to the side of the first trench 5.

[0036] The second ILD material 7 is then removed by etching relative to the remaining portion 11 of the first ILD material, the etch layer 3, and the third ILD material 25, and stopping on the metal of the lower line 6 (either by a timed etch or through etch selectivity with respect to the metal of line 6), see Figure 2f. This creates a via opening 14 that is self-aligned to the width of the lower line 6 and to the end face and the width of the second trench 31. The mask for producing the via opening 14 thus consists of the remaining first ILD portion 11, the etch stop layer 3 and the third ILD material 25.

[0037] Finally, a metal layer is deposited, filling the via opening 14 and the second trench 31. The metal is planarized, thereby creating the metal interconnect via 16 and the upper line 21, see Figure 2g, this time with the via 16 being aligned not only to the line end of the upper line 21 but also to the line width of said upper line 21.

[0038] Figures 3a to 3j illustrate how the first embodiment can be applied for producing a construct with two sets of parallel lines in levels M_x and M_{x+1}, having the same line width and pitch, the sets being mutually perpendicular, and wherein two collinear lines of level M_{x+1} are spaced apart from each other. The invention enables this construct in such a way that the line ends of the two spaced-apart lines in level M_{x+1} are respectively connected to two adjacent lines in level M_x through a pair of interconnect vias which are self-aligned to the line width of the lower lines and to the line ends of the collinear upper lines.

[0039] As seen in Figure 3a, a set of parallel trenches 5 is now produced through layers 1, 3 and 4, and filled with metal, which is subsequently etched back, creating thereby the parallel lines 6 of level M_x. Alternatively, the lines 6 could be formed by area selective deposition. The trenches are filled with the second ILD material 7 which is then etched back, see Figure 3b (or alternatively by area selective deposition). Then the second hardmask 10 is formed (the first hardmask being the one used for etching the trenches 5), as shown in Figure 3c. In the X-direction, the hardmask 10 now covers one portion of the first ILD material of the top layer 4 between two adjacent trenches 5a and 5b.

[0040] Following this, the first ILD material of the top layer4 is removed by etching this material selectively relative to the second ILD material 7, and stopping on the etch stop layer 3, and the second mask 10 is stripped, see Figure 3d. A pillar 11 of the first ILD material remains.

[0041] The third hardmask 12 is formed, see Figure 3e. In this case, the opening 13 in the mask 12 is placed above and transversely to the pillar 11, revealing two equal portions 7a and 7b of the second ILD material on either side of said pillar 11, as well as (preferably) equal portions 3a and 3b of the etch stop layer 3 on either side of said equal portions 7a,7b of the second ILD material.

[0042] With the mask 12 in place, the portions 7a and 7b of the second ILD material are anisotropically etched, stopping on two adjacent metal lines 6a and 6b, after which the mask 12 is stripped, see Figure 3f, so that two via openings 14a and 14b are created, which are self-aligned to the pillar 11 in the Y-direction.

[0043] The metal layer 15 is then produced and planarized, see Figure 3g, creating two via connections 16a and 16b, which are self-aligned to the width of the two adjacent lower lines 6a and 6b.

[0044] Then the fourth mask 20 is formed, see Figure 3h. The fourth mask is now designed to create parallel lines in the X-direction, i.e. perpendicular to the lower lines 6. One of the lines of the mask 20 overlaps the pillar 11.

[0045] With the fourth mask 20 in place, the metal 15 is anisotropically etched and the mask 20 is then stripped, leading to the situation shown in Figure 3i. Two mutually perpendicular sets of parallel lines 6 and 21 are created in levels M_x and M_{x+1} respectively. Two colinear lines 21a and 21b in the upper level are connected to two adjacent lines 6a and 6b in the lower level through the via connections 16a and 16b. In the last step, illustrated in Figure 3j, a layer 22 of (preferably) the first ILD material is deposited and planarized, completing the levels M_x and M_{x+1}.

[0046] The same construct having two collinear lines and two self-aligned via connections can also be realized by applying the second embodiment, as illustrated in Figures 4a to 4h. After the step pictured in Figure 3b, the trenches 5 are now filled with the third ILD material 25, and the wafer is then planarized, as shown in Figure 4a.

[0047] Then the second mask 26 is formed, which now defines multiple parallel lines in the X-direction. With this mask in place, the third ILD material 25 is etched anisotropically relative to the first ILD material of the top layer 4, and stopping on the second ILD material 7, leading to the image shown in Figure 4b.

[0048] Then the third mask 29 is added, as shown in Figure 4c, covering a portion of the central wall of the first ILD material of the top layer 4, and bridging the gap between two parallel lines of the mask 26. With the two masks 26 and 29 in place, the first ILD material of the top layer 4 is then removed selectively with respect to the second ILD material 7, and stopping on the etch stop layer 3. After the masks 26 and 29 are stripped, the image in Figure 4d is obtained. Along the line A-A, the first ILD material is removed except in a central remaining portion 11 that is self-aligned to the space between two adjacent lower metal lines 6a and 6b. Outside the central remaining portion 11, parallel trenches 39 are formed extending

in the direction perpendicular to the lower metal lines 6.

[0049] A fourth mask 40 is now applied (not needed in the sequence shown in Figures 2a-2g), as shown in Figure 4e, covering the whole surface except for a central opening that reveals two portions 7a and 7b of the second ILD material 7 immediately adjacent to the remaining central portion 11 of the first ILD material. The opening furthermore partially reveals portions of the first and second ILD materials and of the etch stop layer 3 surrounding said two portions 7a and 7b of the second ILD material. These latter portions 7a and 7b are then removed by anisotropic etching selectively with respect to the first ILD material, the third ILD material and the etch stop layer, see Figure 4f, creating two via openings 14a and 14b, which are self-aligned in the X-direction to the width of the underlying metal lines 6a and 6b and in the Y-direction to the width of the trenches 39.

[0050] The mask 40 is then stripped (Figure 4g), and then the via openings 14a and 14b and the trenches 39 in the upper level are filled with metal (Figure 4h), leading to the required construct, comprising the via connections 16a and 16b and the collinear metal lines 21a and 21b. The via connections are now self-aligned to the lower lines 6a and 6b and the upper lines 21a and 21b in both the X and Y directions.

[0051] In the above-described embodiments, the top layer 4 is formed of the same ILD material as the bottom layer 1, which represents the preferred case. The top layer 4 could however be formed from an ILD material different from the first ILD layer 1, with the understanding that the ILD material of the top layer 4 must behave in the same manner as the first ILD material in terms of etch selectivity relative to the second and third ILD materials 7 and 25, and relative to the etch stop layer 3.

[0052] Furthermore, the 'first', 'second' and 'third' ILD materials are not limited to single materials, but each of the layers 1, 4, 7 and 25 could for example consist of a stack of different ILD materials, which all have the above-described characteristics of selectivity. Etching either one of these layer could then require different etch recipes for etching through the different materials.

[0053] The requirements for etch selectivity of one ILD material with respect to the other as defined above are the minimum requirements for realizing the invention in accordance with the above-described embodiments. These requirements may be fulfilled by choosing ILD materials for layers 4, 7 and 25 which are all selectively etchable with respect to each other, i.e. each material may serve as a mask for anisotropically etching the other.

[0054] The invention is also related to a semiconductor component, such as an integrated circuit obtainable by the method of the invention. Such a component comprises a semiconductor base substrate (2) and on this base substrate a front end of line portion and a back and of line portion, the back end of line portion comprising multiple levels (M0,M1,...) of interconnected electrical conductors, the levels being interconnected by interconnect vias, and wherein the BEOL portion comprises an interconnect via (16) that is connected to two electrically conductive lines (6,21) running in mutually transverse directions, the via (16) being self-aligned at its lower end to the width of a lower electrically conductive line (6) in a level M_x of the BEOL portion and at its upper end to at least the line end of an upper electrically conductive line (21) of a level M_{x+1} of the BEOL portion, the electrically conductive lines (6,21) and the interconnect via (16) being embedded in at least two different ILD materials, characterized in that:

- at least said line end of the upper line (21) is in direct contact with a portion (11) of ILD material. In the first embodiment, this is the pillar 11 illustrated in Figure 1k. In the second embodiment, this is the portion 11 shown in Figure 2g.
- in the direction of the lower line (6), the interconnect via (16) is isolated on both sides by a second ILD material (7), that is etchable selectively with respect to the ILD material of said portion (11) in direct contact with the line end of the upper line (21) and vice versa. In both the first and the second embodiment, the second ILD material is the material 7 present on either side of the interconnect via 16 in the Y direction (see for example figure 1k),
- an etch stop layer (3) is present underneath the upper line (21), wherein the etch stopping function of the etch stop layer (3) is relative to an etch recipe for etching the ILD material of said portion (11) in direct contact with the line end of the upper line (21).

[0055] The invention is also related to the intermediary product obtained in the course of performing the method, and defined as a semiconductor substrate comprising at least one level of a multilevel interconnect structure, said at least one level comprising a line-shaped conductor (6) oriented in a given direction and embedded in a layer (1) of a first ILD material, said layer having a thickness higher than the conductor (6), wherein the conductor is located at the bottom of a trench (5) through said layer of the first ILD material (1), the substrate further comprising :

- an etch stop layer (3) on the first layer (1) of the first ILD material, and a portion (11) of an ILD material extending above the etch stop layer (3) and being aligned to one side of the trench (5), wherein the etch stopping function of the etch stop layer (3) is relative to an etch recipe for etching the ILD material of said portion (11) extending above the etch stop layer (3),
- an elongate portion (7) of a second ILD material that is selectively etchable with respect to the material of the portion (11) extending above the etch stop layer and vice versa, the second material also being selectively etchable with respect to the etch stop layer (3), said elongate portion (7) being present on top of the conductor (6) the elongate portion (7) of the second ILD material being interrupted by a via (14) adjacent to the ILD portion (11) extending above the

etch stop layer (3).

The intermediate product is illustrated for the first embodiment in Figures 1h and 3f and for the second embodiment in Figures 2f and 4g.

[0056] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

Claims

1. A method for producing an interconnect via (16) for a semiconductor component, wherein the via is connected to two electrically conductive lines (6,21) running in mutually transverse directions, the via (16) being self-aligned at its lower end to the width of a lower electrically conductive line (6) and at its upper end to at least the line end of an upper electrically conductive line (21), **characterized in that** the method comprises the steps of :

    - producing on a semiconductor base substrate (2) a stack of:

        ◦ A bottom layer (1) of a first intermetal dielectric (ILD) material,
        ◦ An etch stop layer (3) on the bottom layer (1),
        ◦ A top layer (4) of ILD material on the etch stop layer (3), wherein the etch stopping function of the etch stop layer (3) is relative to an etch recipe for etching the ILD material of the top layer (4),

    - etching at least one trench (5) through the complete thickness of the stack,
    - producing said lower electrically conductive line (6) at the bottom of the trench (5), i.e. filling a lower portion of the trench (5),
    - producing a layer (7) of a second ILD material in the trench (5) and on top of the lower line (6), wherein the second ILD material is etchable selectively with respect to the ILD material of the top layer (4) and vice versa, and wherein the second ILD material (7) is also etchable selectively with respect to the etch stop layer (3),
    - by applying one or more etch masks and etching back the ILD material of the top layer (4) and stopping on the etch stop layer (3), removing the ILD material of said top layer (4) along at least a longitudinal portion of the trench (5) located to one side of the trench, while maintaining the ILD material of the top layer (4) at least along said same longitudinal portion located on the opposite side of the trench, so that a remaining portion (11) of ILD material of the top layer (4) protrudes above the etch stop layer (3), the remaining portion (11) being self-aligned to said opposite side of the trench (5),
    - etching a via opening (14) through the second ILD material (7) in the trench (5), using at least the remaining portion (11) of the ILD material of the top layer (4) as a mask, so that the via opening is self-aligned to said opposite side of the trench, along at least a part of said longitudinal portion of the trench (5),
    - producing the upper line (21) and the interconnect via (16), by depositing an electrically conductive material, thereby filling the via opening (14), and by producing a patterned layer of the conductive material on top of the interconnect via (16).

2. The method according to claim 1, wherein the lower conductive line (6) is formed by filling the trench (5) with an electrically conductive material and etching back the conductive material down to the required thickness of the lower line (6).

3. The method according to claim 1 or 2, wherein the layer (7) of the second ILD material is produced by filling the trench with said second ILD material and etching back the second ILD material (7) in the trench (5), selectively with respect to the top layer (4).

4. The method according to any one of claims 1 to 3, wherein after the step of producing the layer of the second ILD material (7) in the trench (5), a first mask (10) is applied and the ILD material of the top layer (4) is removed except at the location of the mask, thereby creating said remaining portion of ILD material in the form of a pillar (11) that is self-aligned to said opposite side of the trench (5), followed, after stripping the first mask (10), by the application of a second mask (12) configured to define said at least part of the longitudinal portion of the trench (5), and wherein the upper line (21) is produced by depositing an electrically conductive layer (15), thereby filling the via opening (14) and enclosing the pillar (11), and thereafter patterning the electrically conductive layer (15) to thereby form the upper line (21).

5. The method according to any one of claims 1 to 3 ,

wherein after the step of producing the layer (7) of the second ILD material in the trench (5), the trench (5) is not completely filled, and a third ILD material (25) is deposited in the trench (5) on top of the layer (7) of the second ILD material, wherein the third ILD material is etchable selectively with respect to the ILD material of the top layer (4), wherein the second ILD material is etchable selectively with respect to the third ILD material, and wherein the third ILD material (25) is removed from the trench (5) in an area corresponding to the width of the upper line (21), so that the remaining portions of the third ILD material on either side of said width serve as portions of a mask for etching the via opening (14), so that the opening is self-aligned to said width of the upper line (21).

6. The method according to claim 5, comprising the steps of :

- depositing a layer of the third ILD material (25), thereby filling the trench (5), and planarizing the layer of the third ILD material until the upper surface of the top layer (4) of ILD material is exposed,
- applying a first mask (26) that defines the position and width of the upper line (21),
- removing the third ILD material (25) from the trench (5), in an area defined by the first mask (26) and by the ILD material of the top layer (4),
- With the first mask (26) in place, applying a second mask (29) which covers the ILD material of the top layer (4) to said opposite side of the trench, while leaving the ILD material of the top layer (4) on said one side of the trench exposed in an area corresponding to the upper line (21),
- with both masks (26,29) in place, etching the ILD material of the top layer (4), stopping on the etch stop layer (3), and stripping the masks (26,29), thereby obtaining the remaining portion (11) of ILD material that is self-aligned to said opposite side of the trench (5), while creating a transverse trench (31) in the top layer (4) on the other side of the trench (5), the transverse trench (31) defining the position of the upper line (21),
- etching the via opening (14), using at least the ILD material of the top layer (4), the etch stop layer (3) and the third ILD material (25) as a mask,
- filling the via opening (14) and the transverse trench (31) with an electrically conductive material, thereby obtaining the interconnect via (16) and the upper line (21).

7. The method according to any one of the preceding claims, wherein two interconnect vias (16a,16b) are produced, connecting a first and second mutually parallel lower line (6a,6b) respectively to a first and second collinear upper line (21a,21b), the interconnect vias (16a,16b) being self-aligned to the width of the respective lower lines (6a,6b) and to at least the line ends of the respective upper lines (21a,21 b).

8. The method according to any one of the preceding claims, wherein the ILD material of the top layer (4) is the same as the first ILD material.

9. A semiconductor component comprising a semiconductor base substrate (2) and on this base substrate a front end of line portion and a back and of line portion, the back end of line portion comprising multiple levels (M0,M1,...) of interconnected electrical conductors, the levels being interconnected by interconnect vias, and wherein the BEOL portion comprises an interconnect via (16) that is connected to two electrically conductive lines (6,21) running in mutually transverse directions, the via (16) being self-aligned at its lower end to the width of a lower electrically conductive line (6) in a level M_x of the BEOL portion and at its upper end to at least the line end of an upper electrically conductive line (21) of a level M_{x+1} of the BEOL portion, the electrically conductive lines (6,21) and the interconnect via (16) being embedded in at least two different ILD materials, **characterized in that**:

- at least said line end of the upper line (21) is in direct contact with a portion (11) of ILD material,
- in the direction of the lower line (6), the interconnect via (16) is isolated on both sides by a second ILD material (7), that is etchable selectively with respect to the ILD material of said portion (11) in direct contact with the line end of the upper line (21) and vice versa,
- an etch stop layer (3) is present underneath the upper line (21), wherein the etch stopping function of the etch stop layer (3) is relative to an etch recipe for etching the ILD material of said portion (11) in direct contact with the line end of the upper line (21).

10. A semiconductor substrate comprising at least one level of a multilevel interconnect structure, said at least one level comprising a line-shaped conductor (6) oriented in a given direction and embedded in a layer (1) of a first ILD material, said layer having a thickness higher than the conductor (6), wherein the conductor is located at the bottom of a trench (5) through said layer of the first ILD material (1), the substrate further comprising :

- an etch stop layer (3) on the first layer (1) of the first ILD material, and a portion (11) of an ILD material extending above the etch stop layer (3) and being aligned to one side of the trench

(5), wherein the etch stopping function of the etch stop layer (3) is relative to an etch recipe for etching the ILD material of said portion (11) extending above the etch stop layer (3),

- an elongate portion (7) of a second ILD material that is selectively etchable with respect to the material of the portion (11) extending above the etch stop layer and vice versa, the second material also being selectively etchable with respect to the etch stop layer (3), said elongate portion (7) being present on top of the conductor (6), the elongate portion (7) of the second ILD material being interrupted by a via (14) adjacent to the ILD portion (11) extending above the etch stop layer (3) .

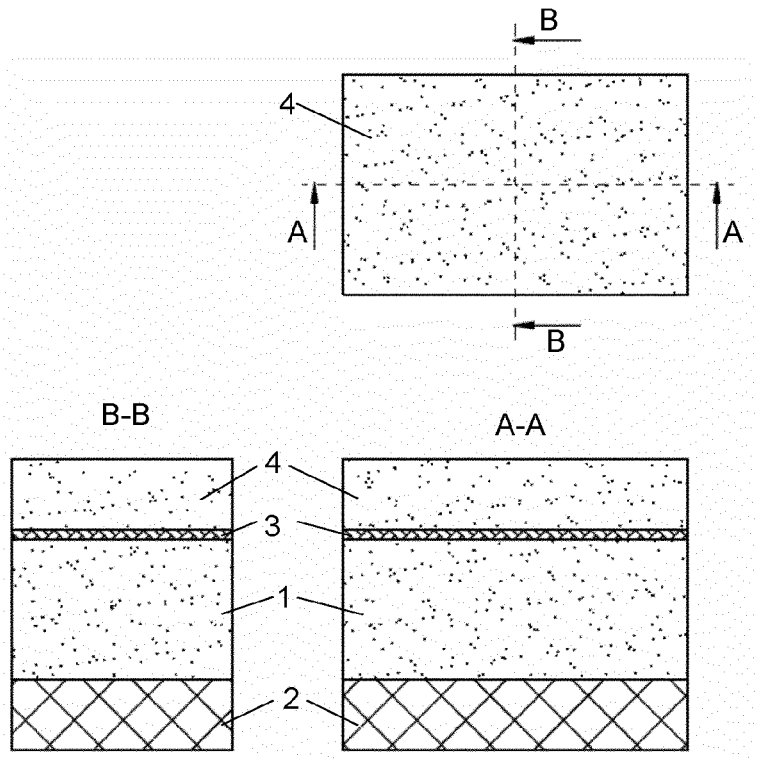


FIG. 1a

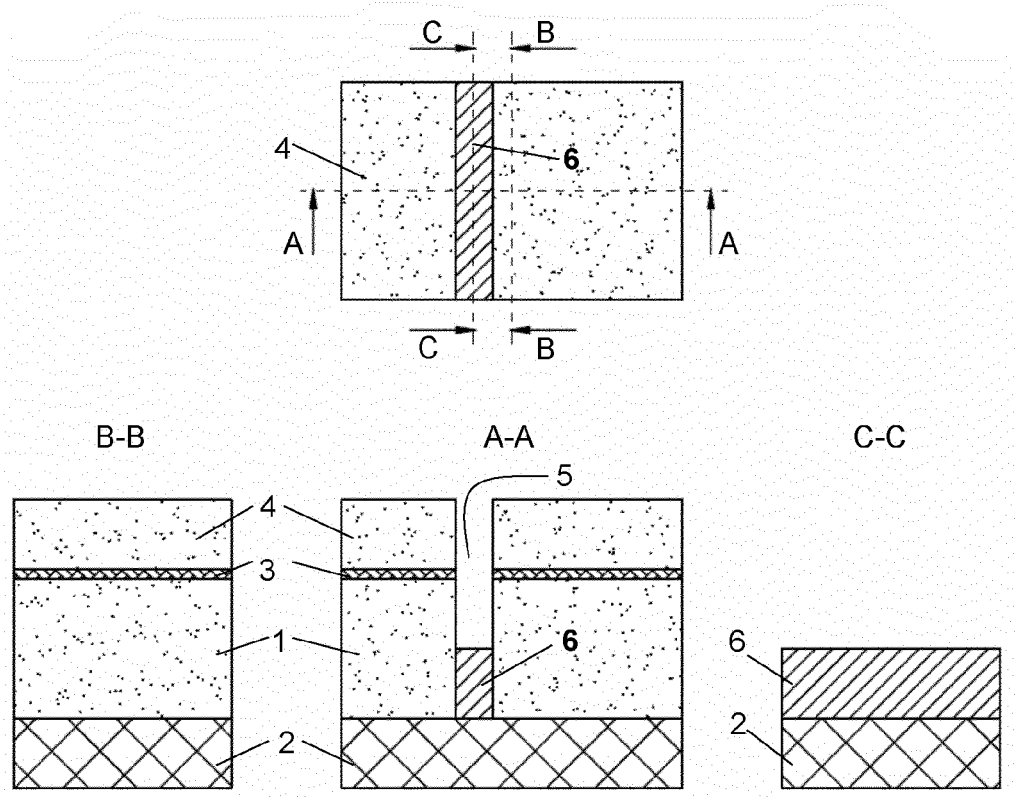


FIG. 1b

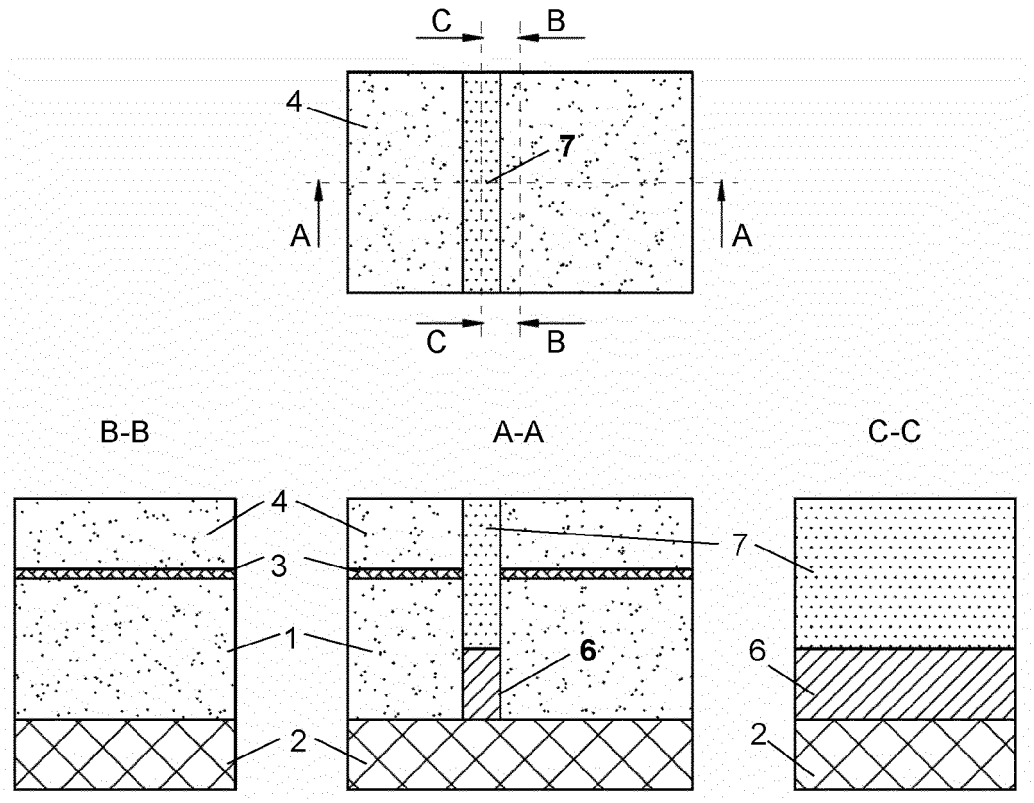


FIG. 1c

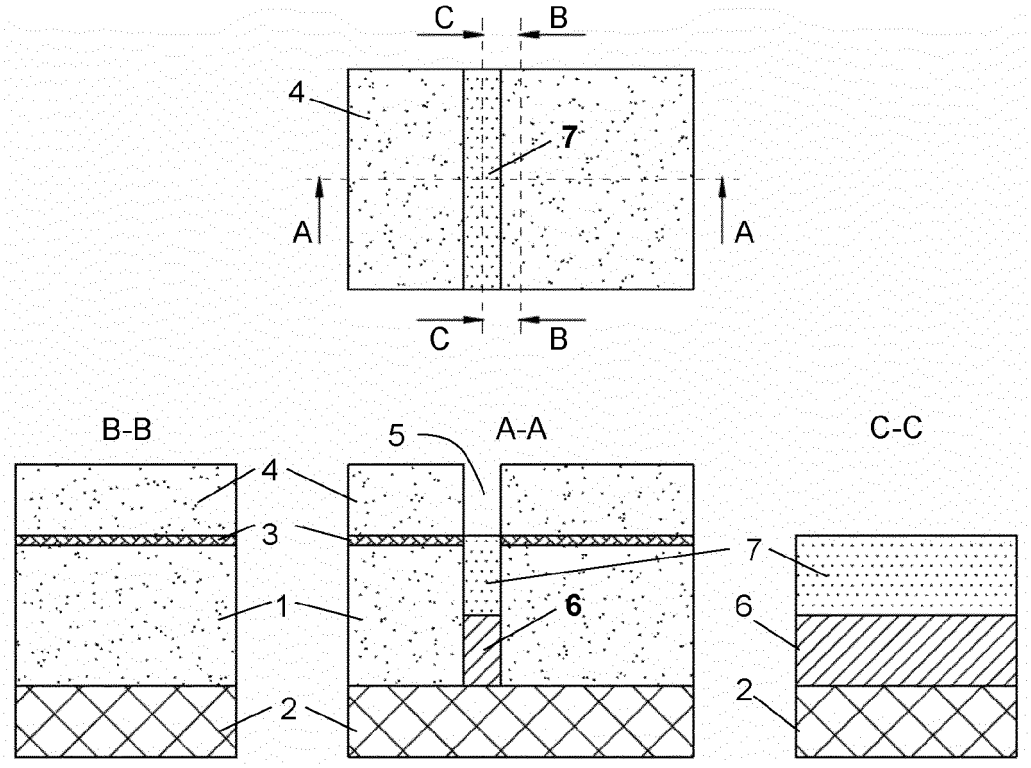


FIG. 1d

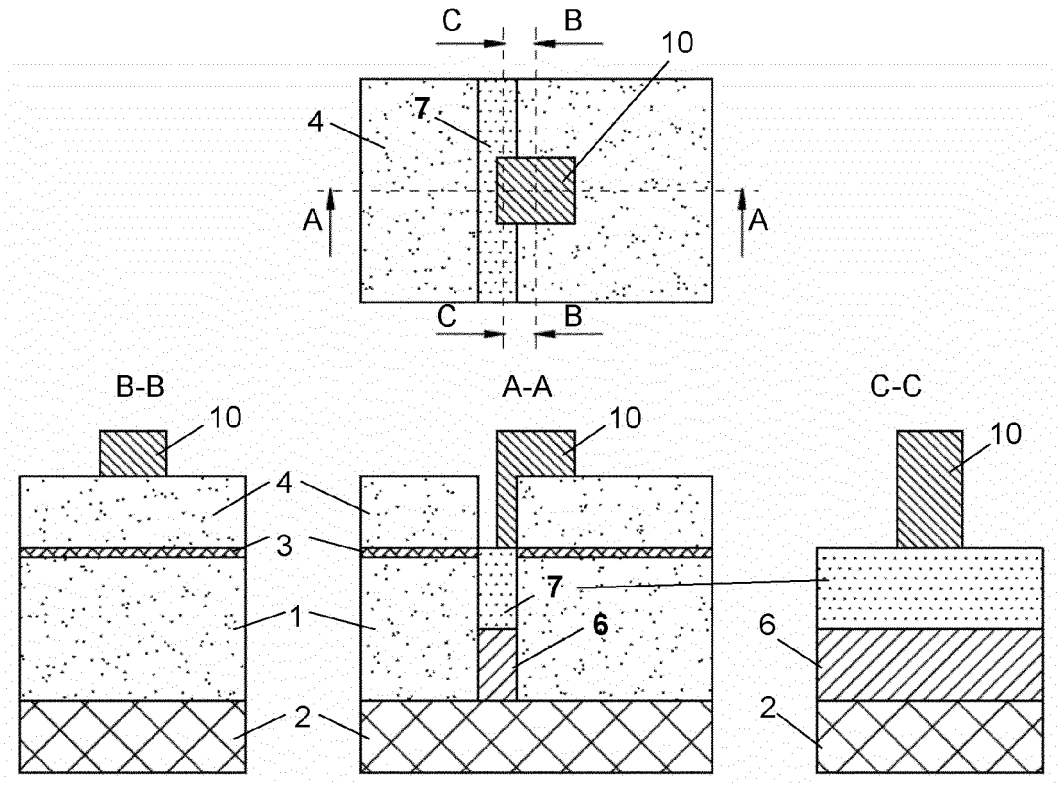

C
B
10
4
7
A
A
C
B
B-B
A-A
C-C
10
10
10
4
3
1
2
7
6
6
2

FIG. 1e

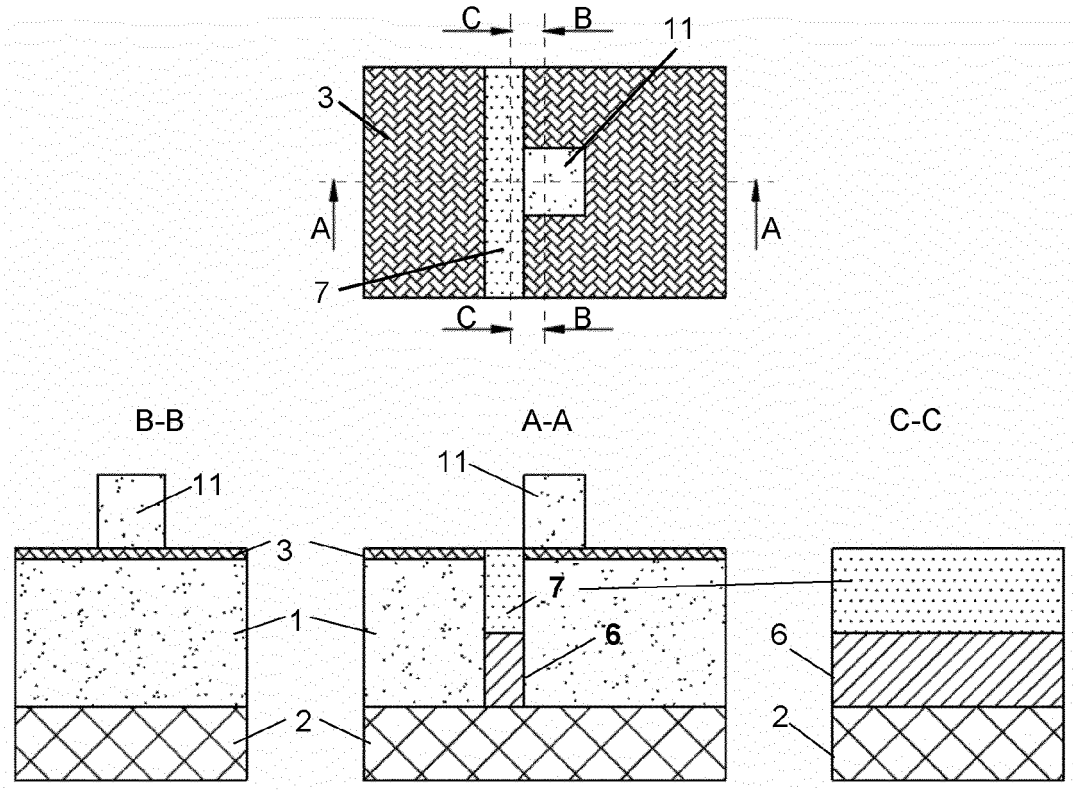
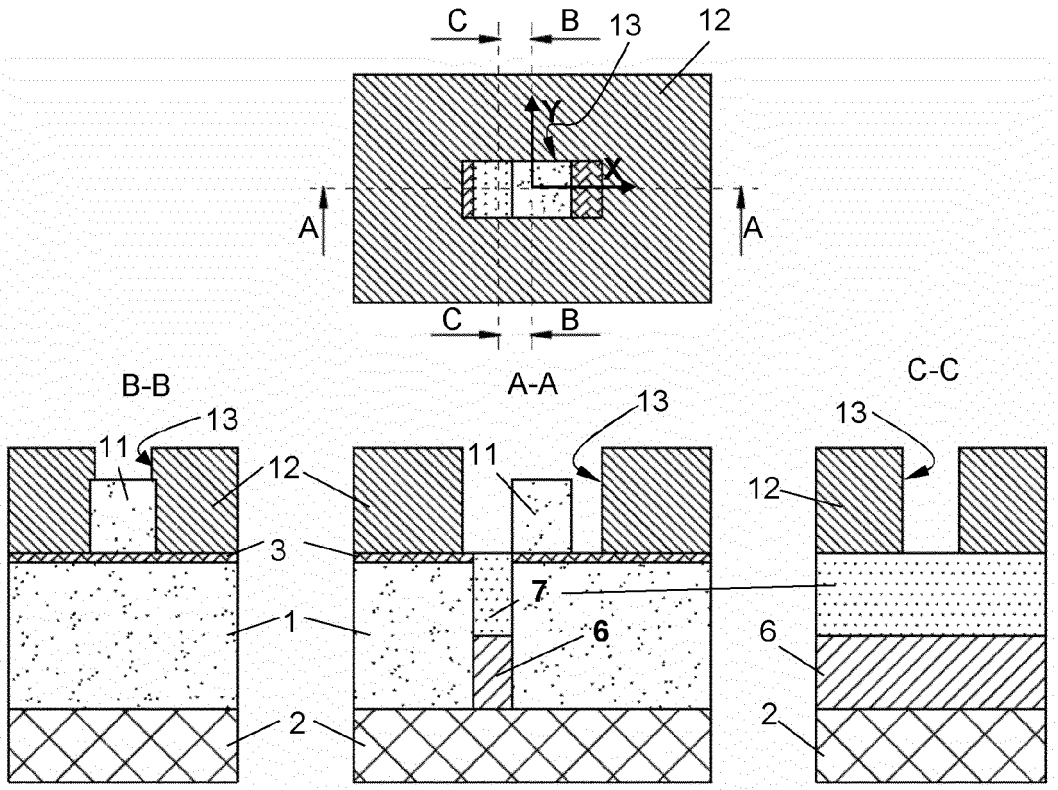

C
B
11
3
A
A
7
C
B
B-B
A-A
C-C
11
11
3
1
2
7
6
6
2

FIG. 1f


C
B
13
12
Y
X
A
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C
B
B-B
A-A
C-C
13
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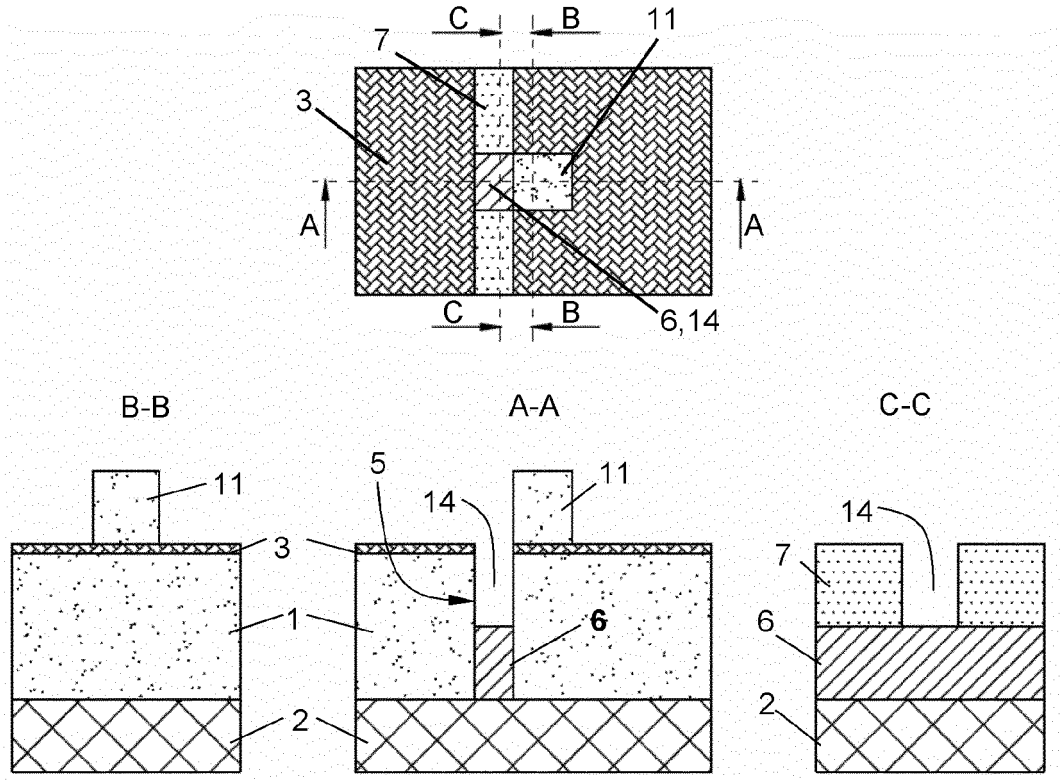
12
3
1
2
7
6

FIG. 1g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B
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7
3
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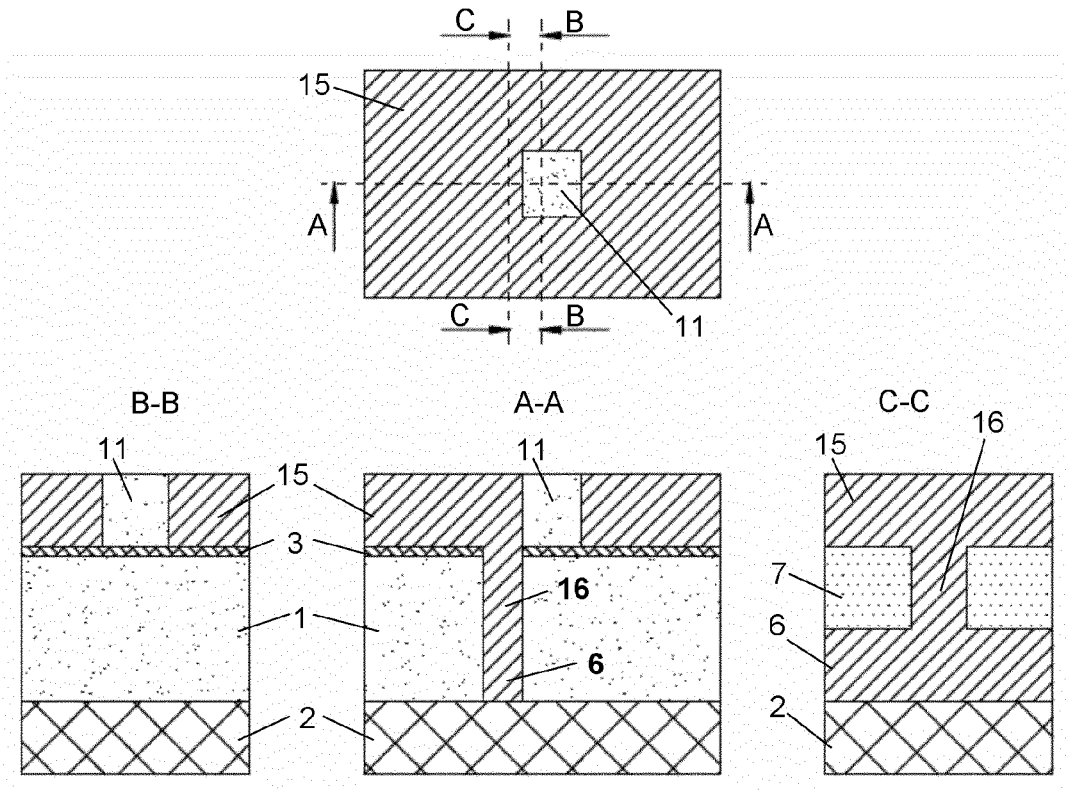
A
6,14
C
B
B-B
A-A
C-C
11
5
14
3
1
2
6
7

FIG. 1h


C
B
15
A
A
C
B
11
B-B
A-A
C-C
11
15
3
1
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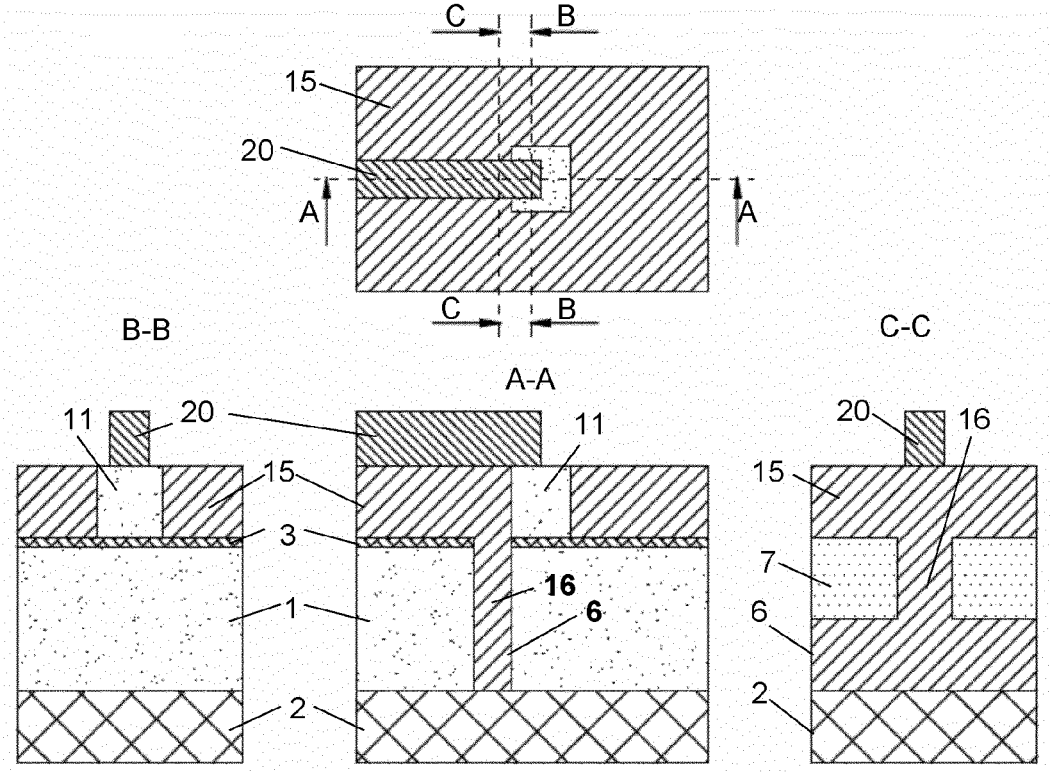
16
6
15
16
7
6
2

FIG. 1i


C
B
15
20
A
A
C
B
B-B
A-A
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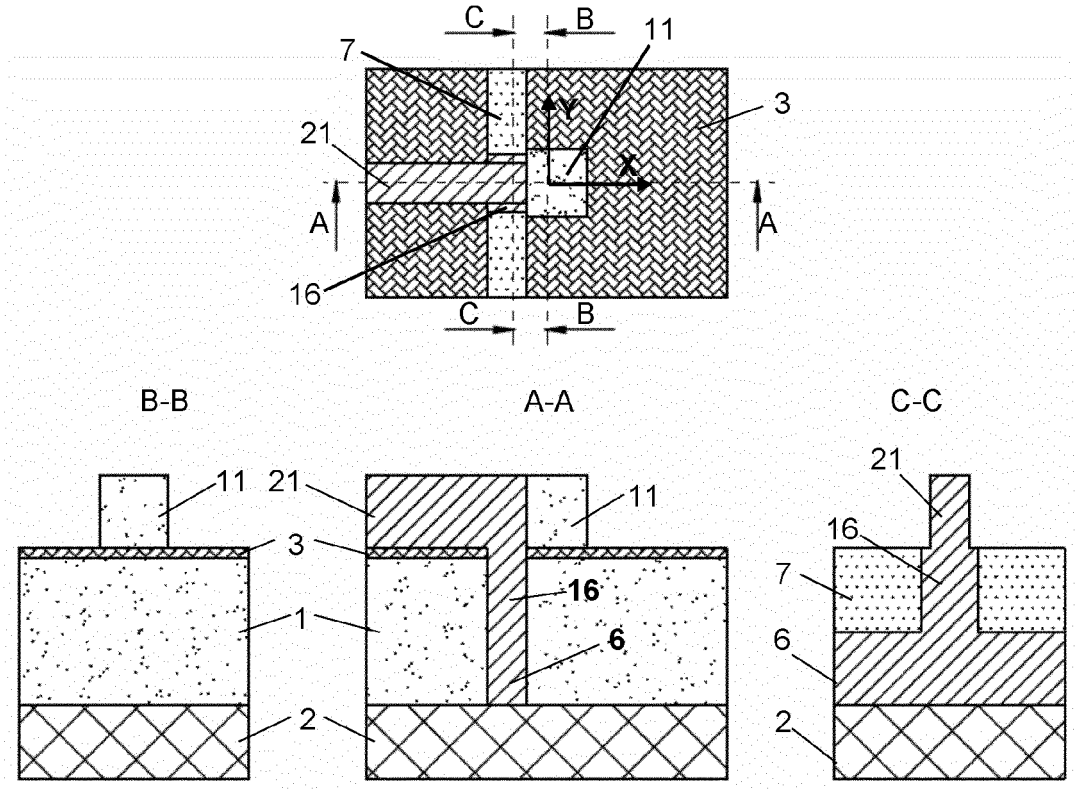
1
2
11
16
6
20
16
15
7
6
2

FIG. 1j


C
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7
Y
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21
X
A
A
16
C
B
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C-C
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16
16
7
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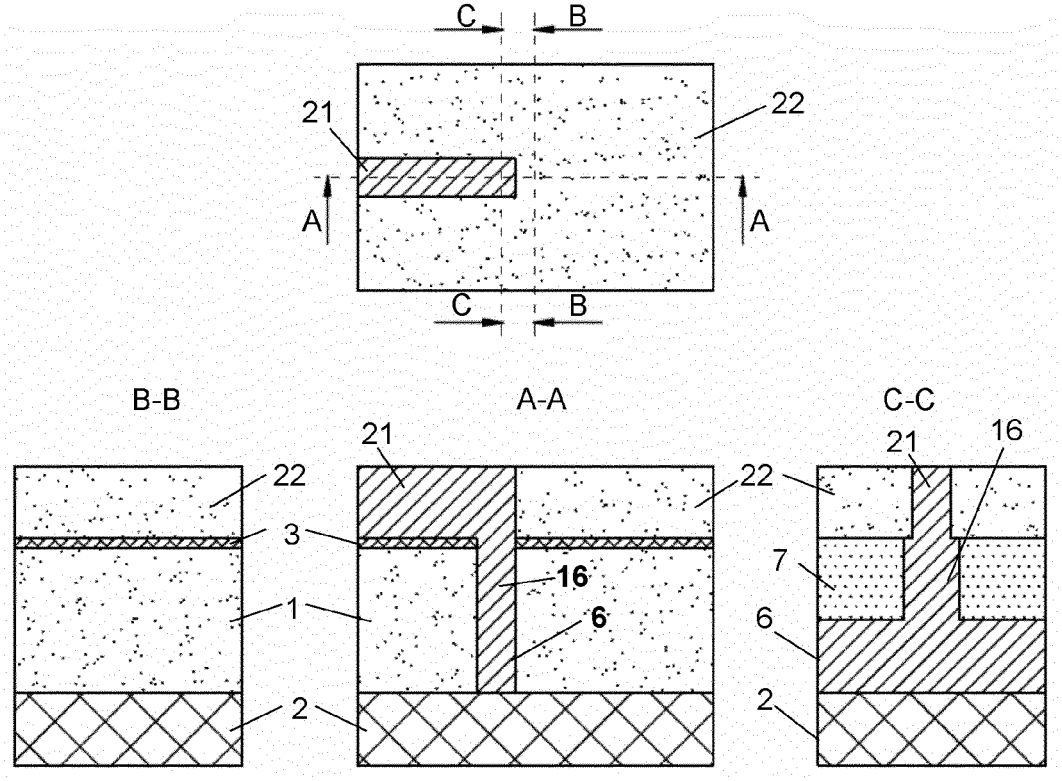
6
6
2
2

FIG. 1k


C
B
21
22
A
A
C
B
B-B
A-A
C-C
21
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16
22
22
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16
7
1
6
6
2
2

FIG. 1l

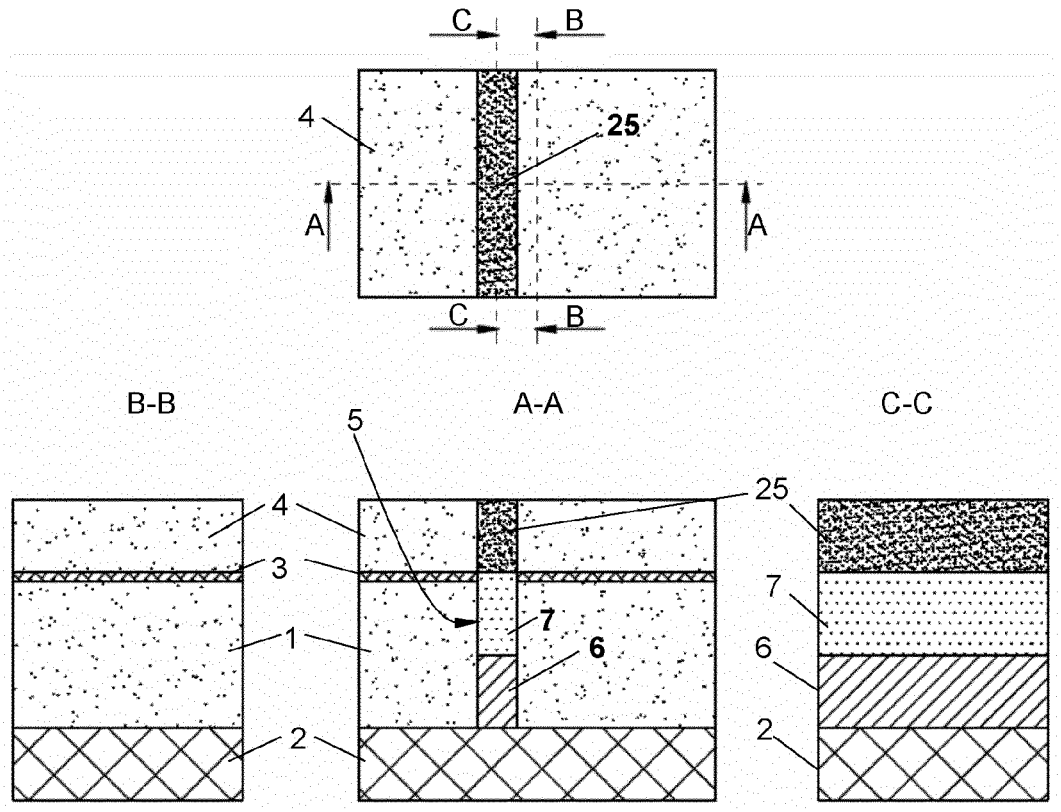
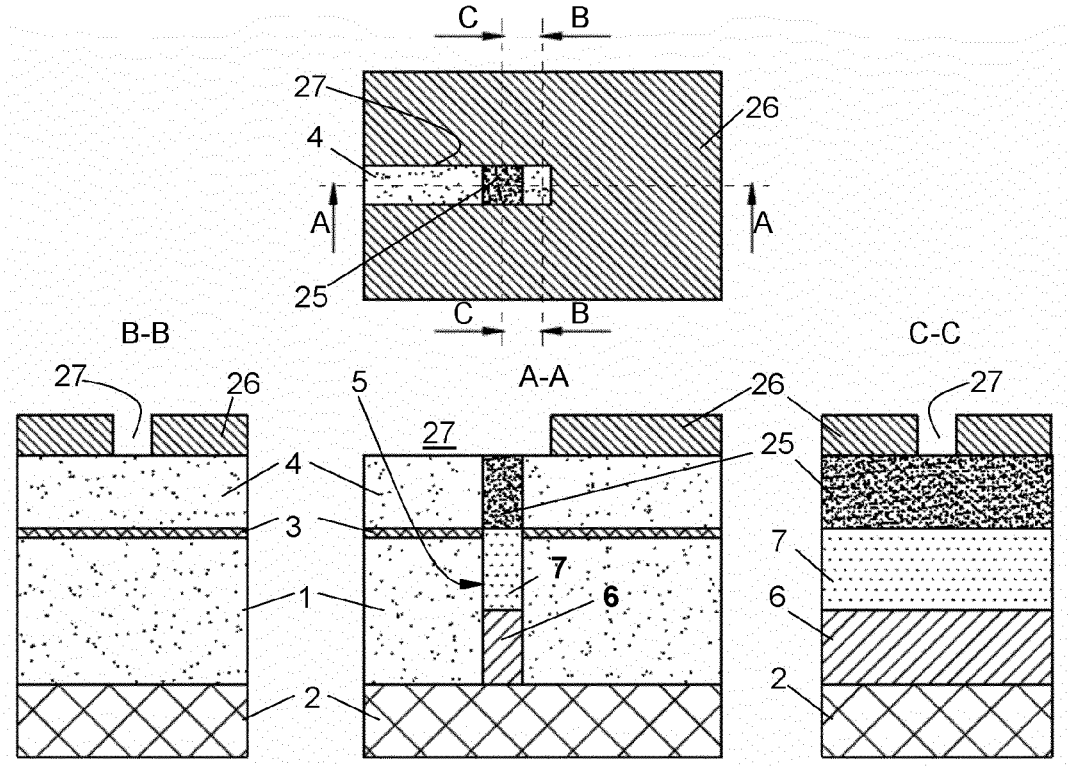

C
B
4
25
A
A
C
B
B-B
A-A
C-C
5
4
25
3
7
1
6
2
7
6
2

FIG. 2a


C
B
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26
4
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25
C
B
B-B
C-C
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A-A
26
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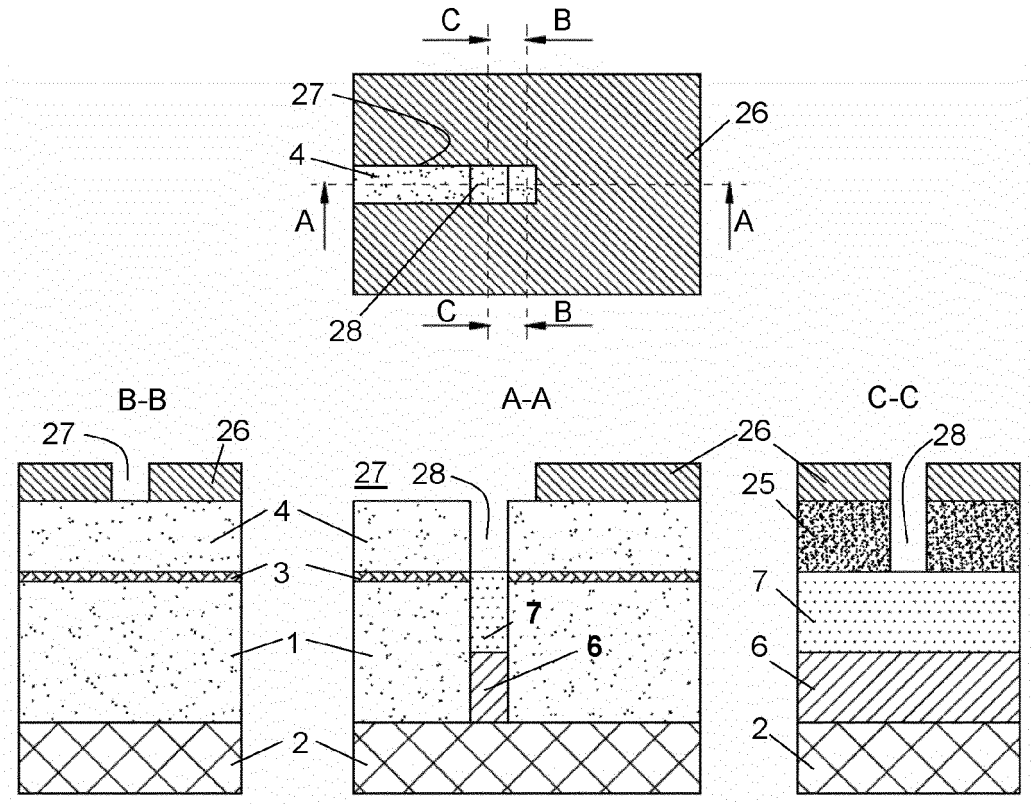
27
25
4
3
7
1
6
2
7
6
2

FIG. 2b


C
B
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26
4
A
A
C
B
28
B-B
A-A
C-C
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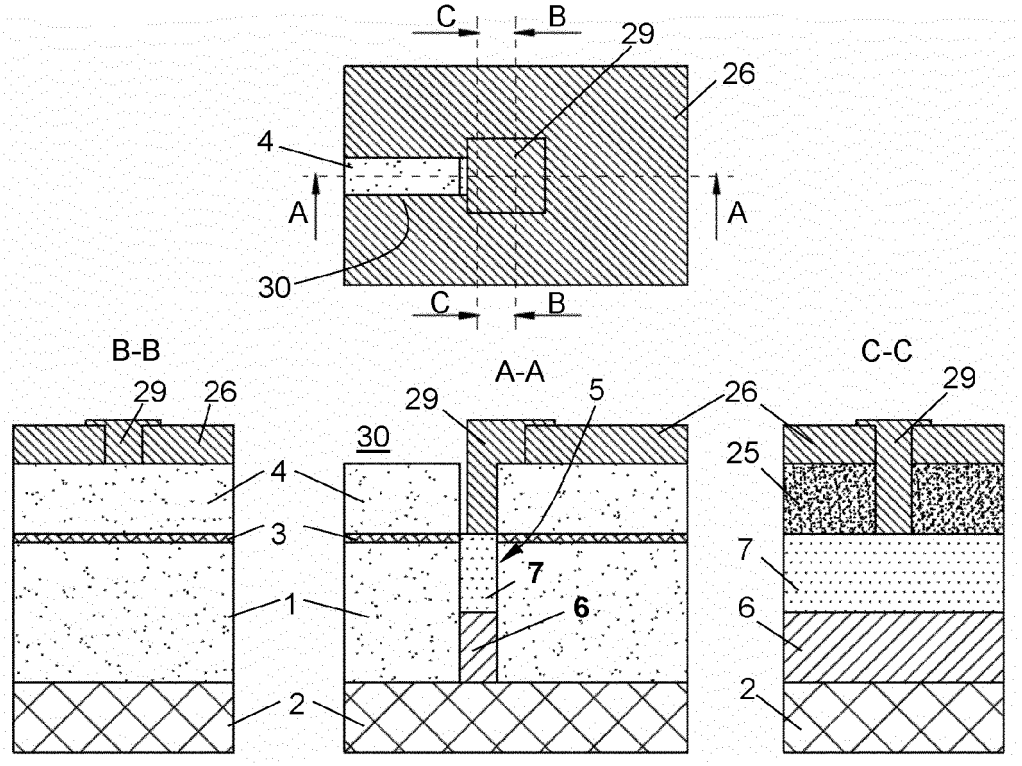
28
25
4
3
7
1
6
6
7
2
2

FIG. 2c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B
29
26
4
A
A
30
C
B
B-B
A-A
C-C
29
26
29
5
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30
25
4
3
7
7
1
6
6
2
2

FIG. 2d

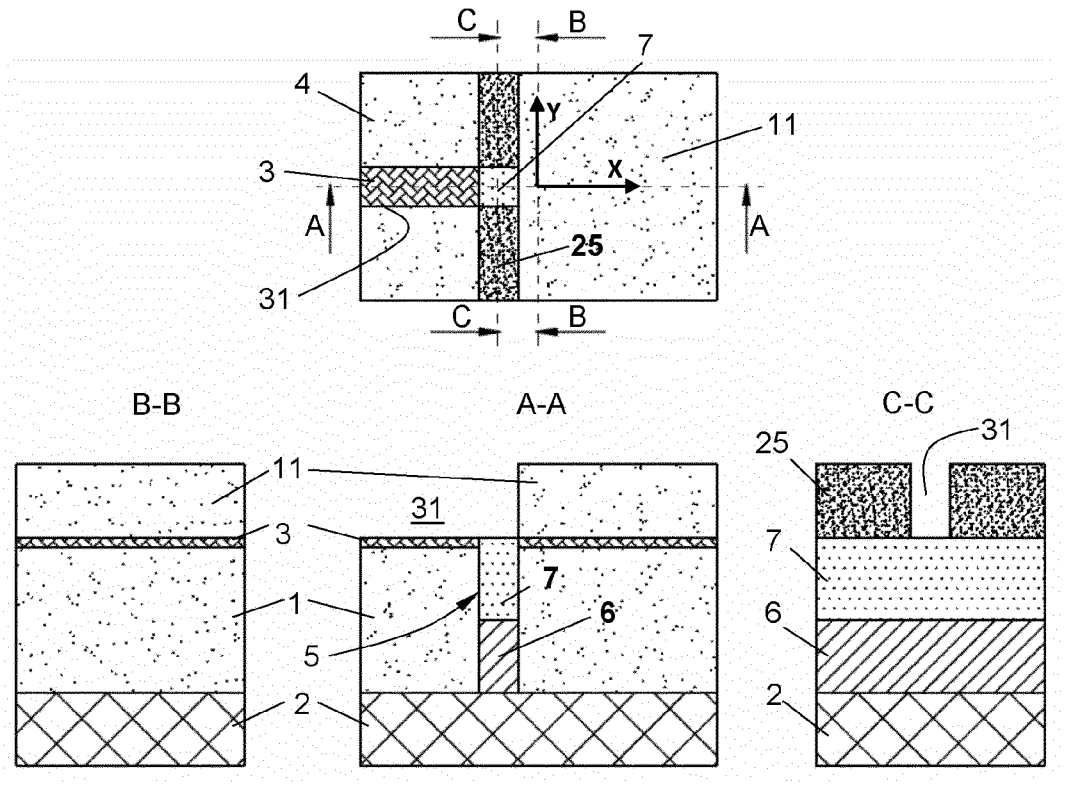

C
B
7
4
y
11
3
x
A
A
25
31
C
B
B-B
A-A
C-C
11
31
25
3
7
7
1
6
6
5
2
2

FIG. 2e

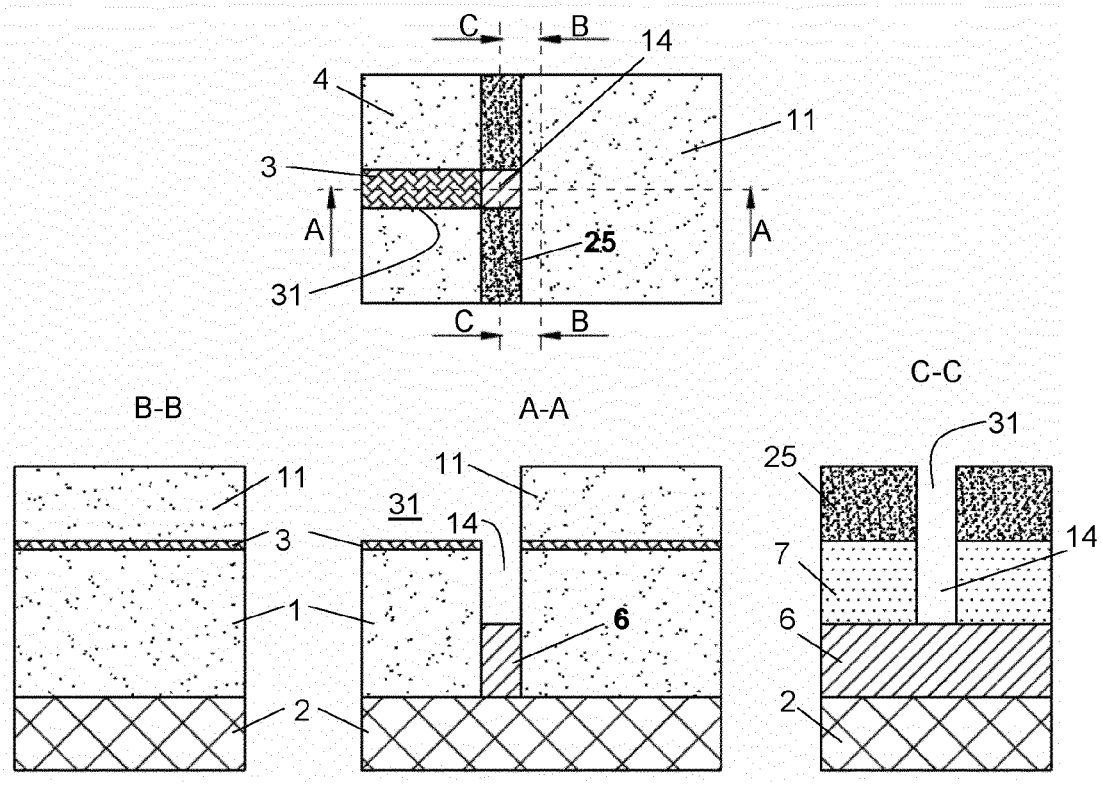

C
B
14
4
11
3
A
A
25
31
C
B
C-C
B-B
A-A
31
11
11
25
3
31
14
14
7
1
6
6
2
2

FIG. 2f

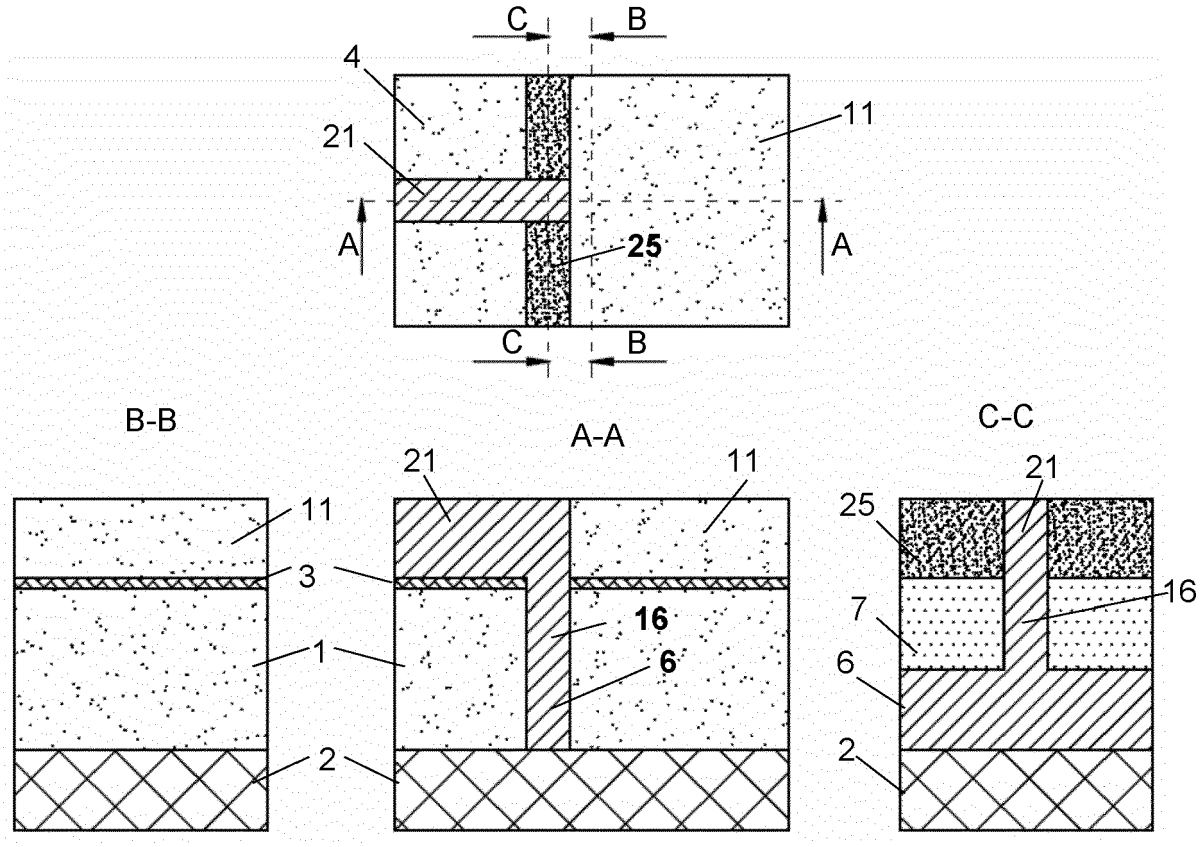


FIG. 2g

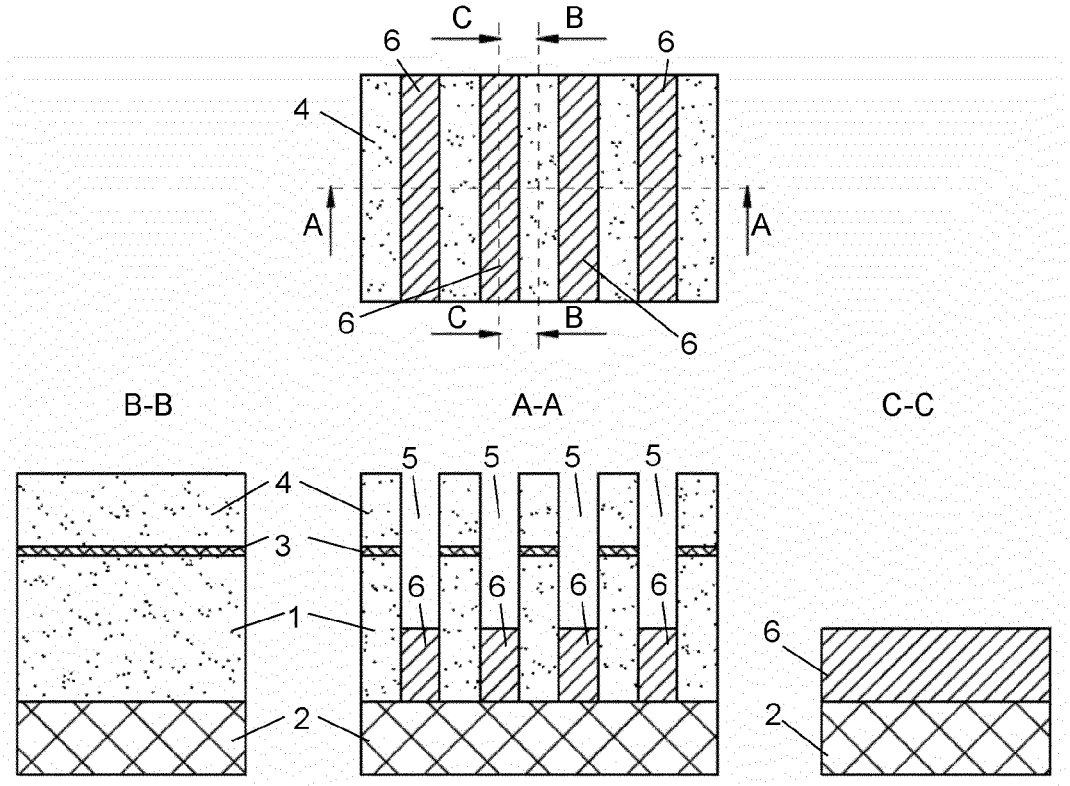

C
B
6
6
4
A
A
6
C
B
6
B-B
A-A
C-C
5
5
5
5
4
3
6
6
6
6
1
6
2
2

FIG. 3a

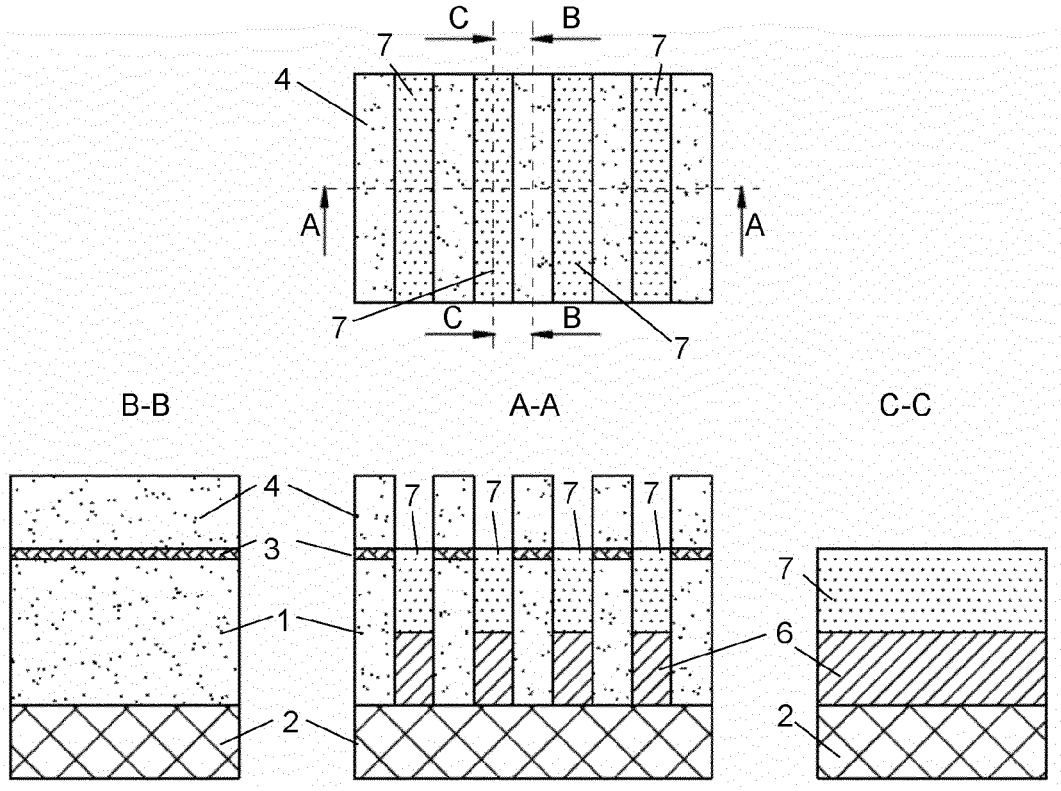

C
B
7
7
4
A
A
7
C
B
7
B-B
A-A
C-C
4
7
7
7
7
3
1
7
6
2
2

FIG. 3b

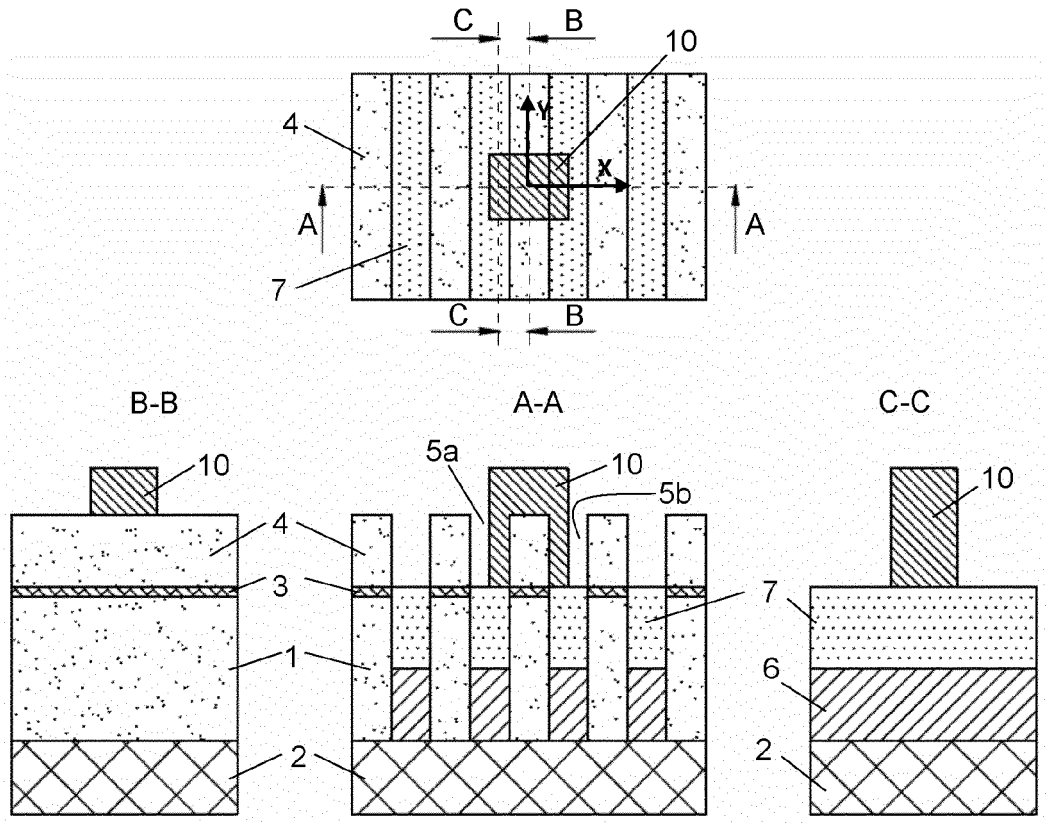

C
B
10
Y
X
4
A
A
7
C
B
B-B
A-A
C-C
10
5a
10
5b
10
4
3
7
1
6
2
2

FIG. 3c

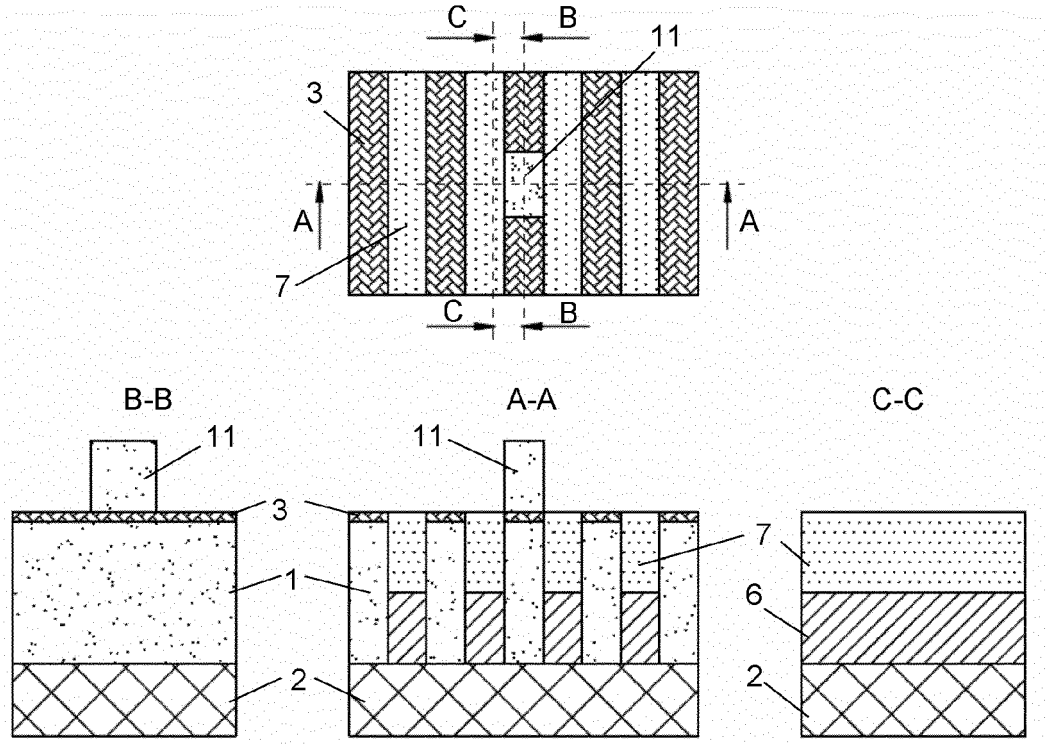

C
B
11
3
A
A
7
C
B
B-B
A-A
C-C
11
11
3
7
1
6
2
2

FIG. 3d

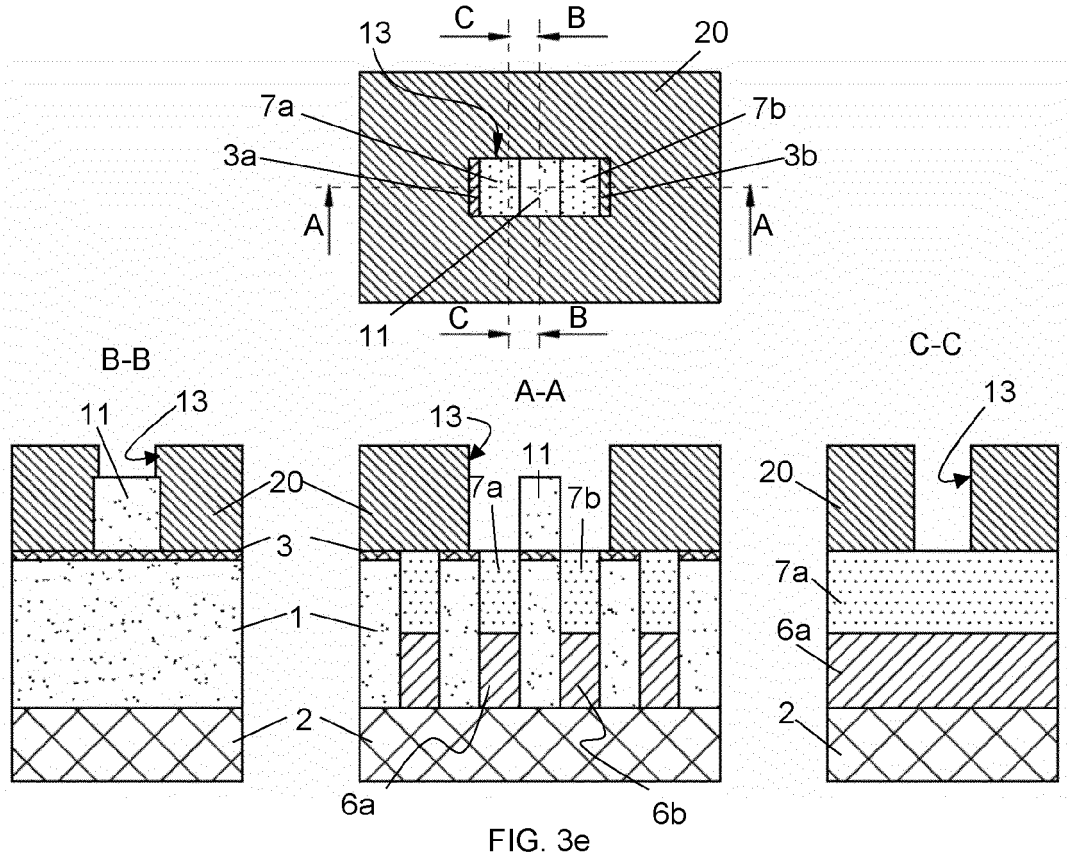

C
B
13
20
7a
7b
3a
3b
A
A
C
B
11
B-B
A-A
C-C
11
13
13
13
11
20
7a
7b
20
3
7a
1
6a
2
2
6a
6b

FIG. 3e

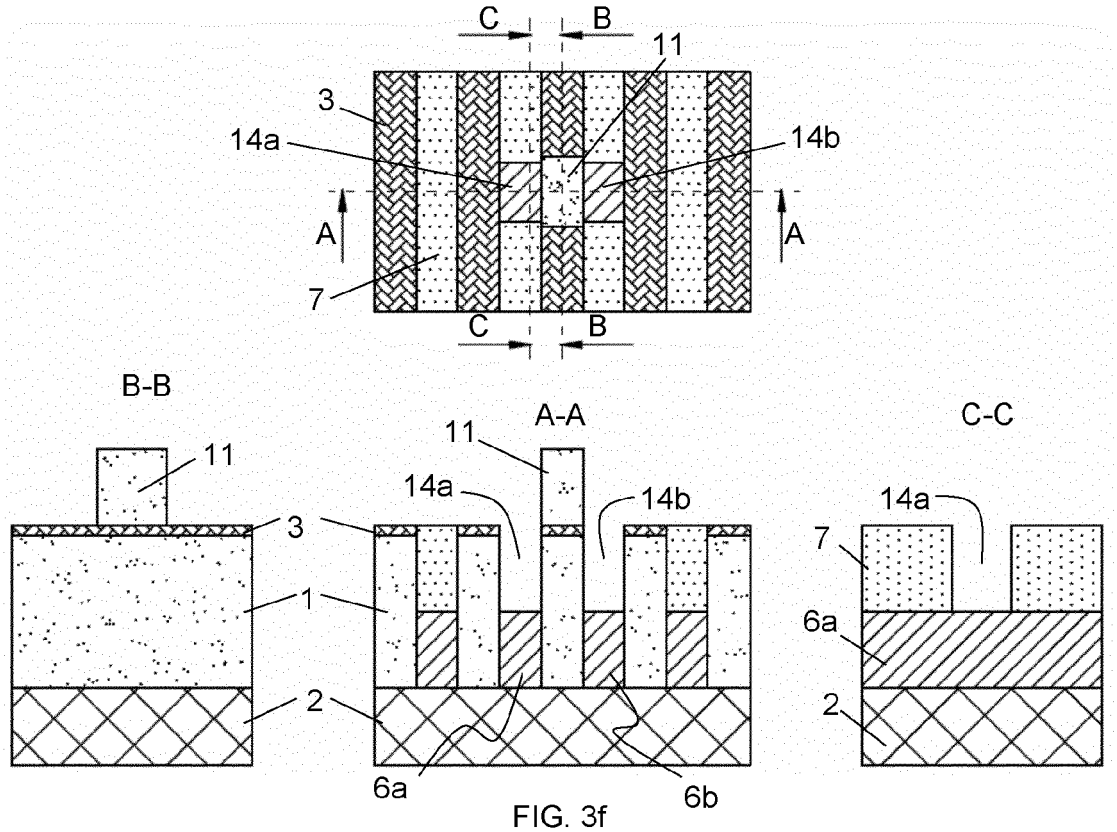

C
B
11
3
14a
14b
A
A
7
C
B
B-B
A-A
C-C
11
11
14a
14b
14a
3
7
1
6a
2
2
6a
6b

FIG. 3f

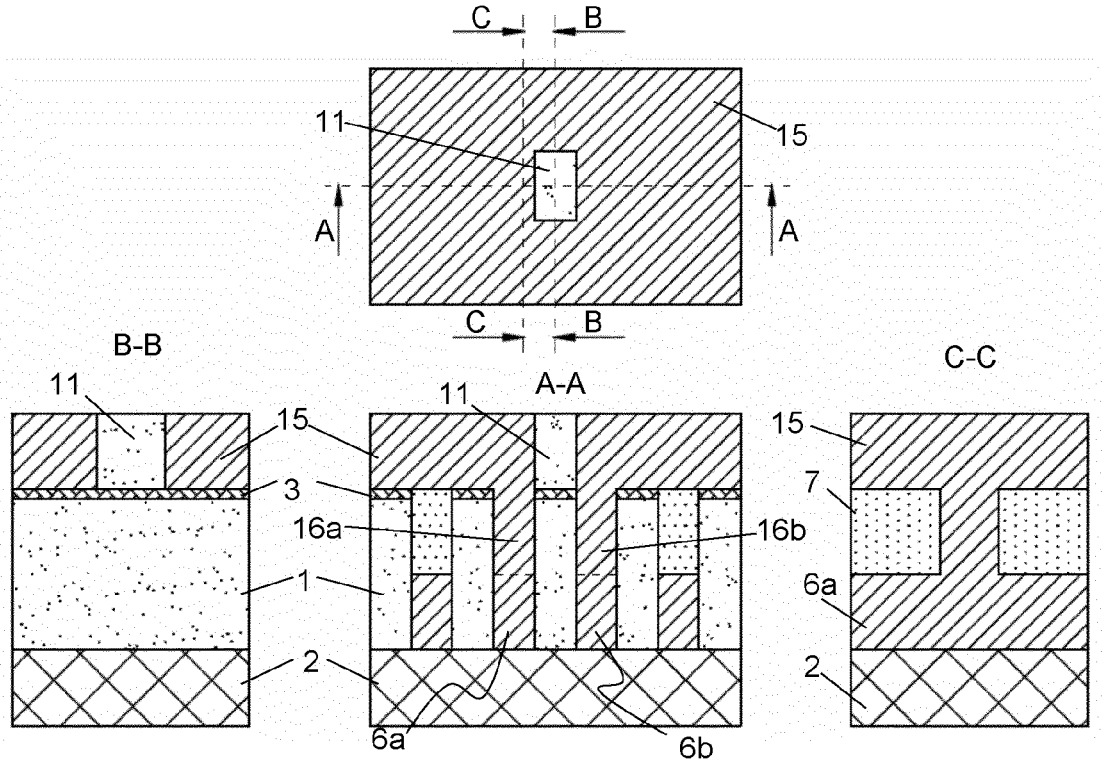
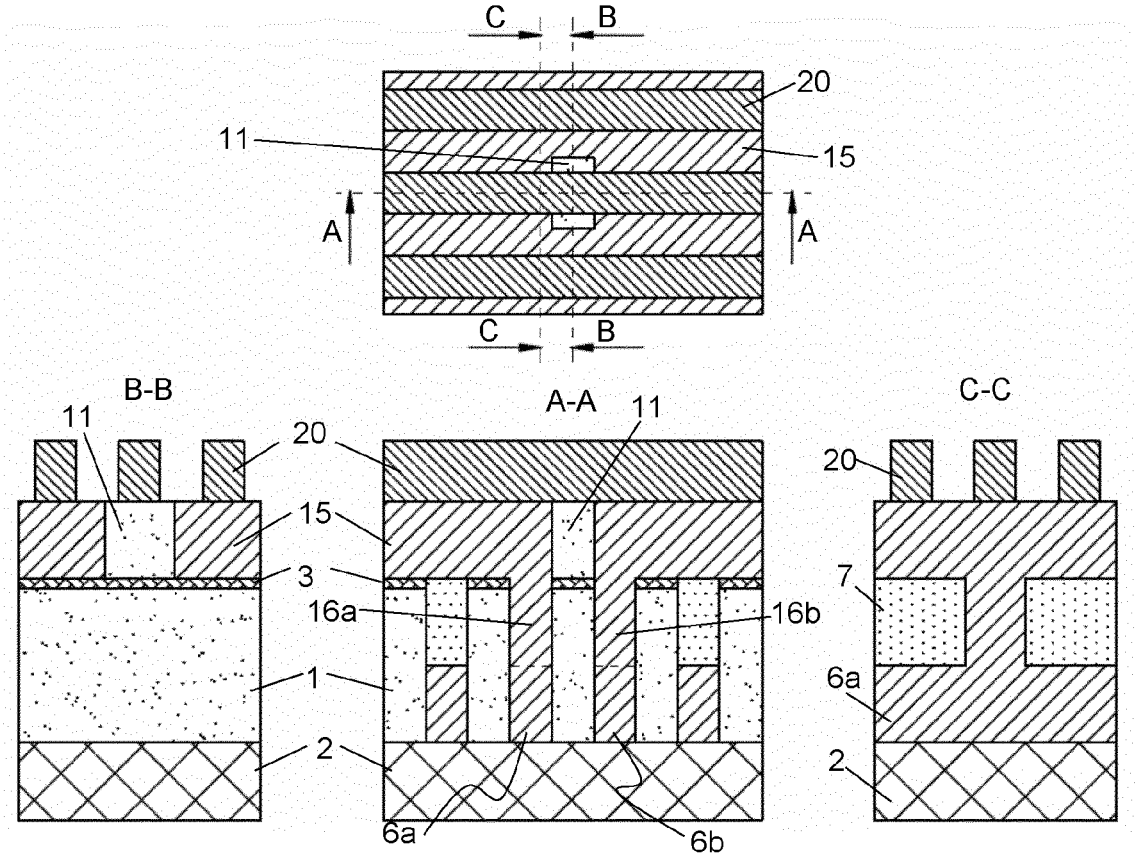

C
B
11
15
A
A
C
B
B-B
A-A
C-C
11
11
15
15
3
7
16a
16b
1
6a
2
2
6a
6b

FIG. 3g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B
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11
15
A
A
C
B
B-B
A-A
C-C
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11
20
20
15
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16a
16b
1
6a
2
2
6a
6b

FIG. 3h

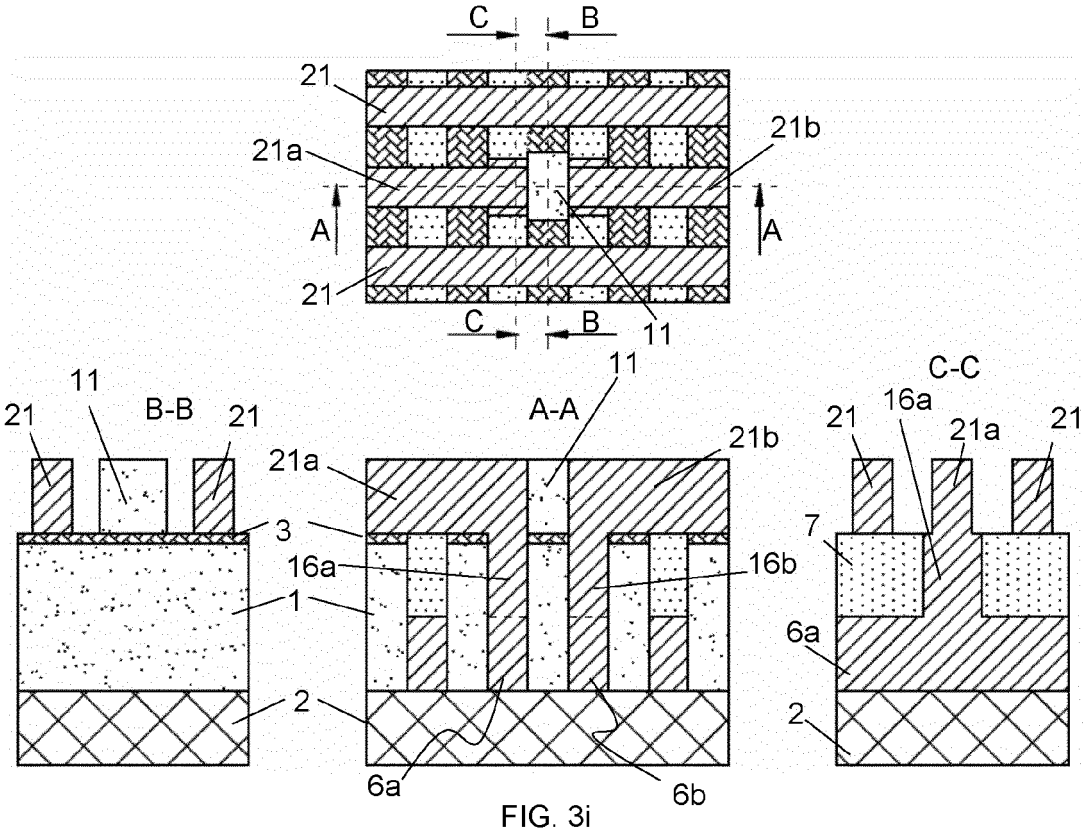
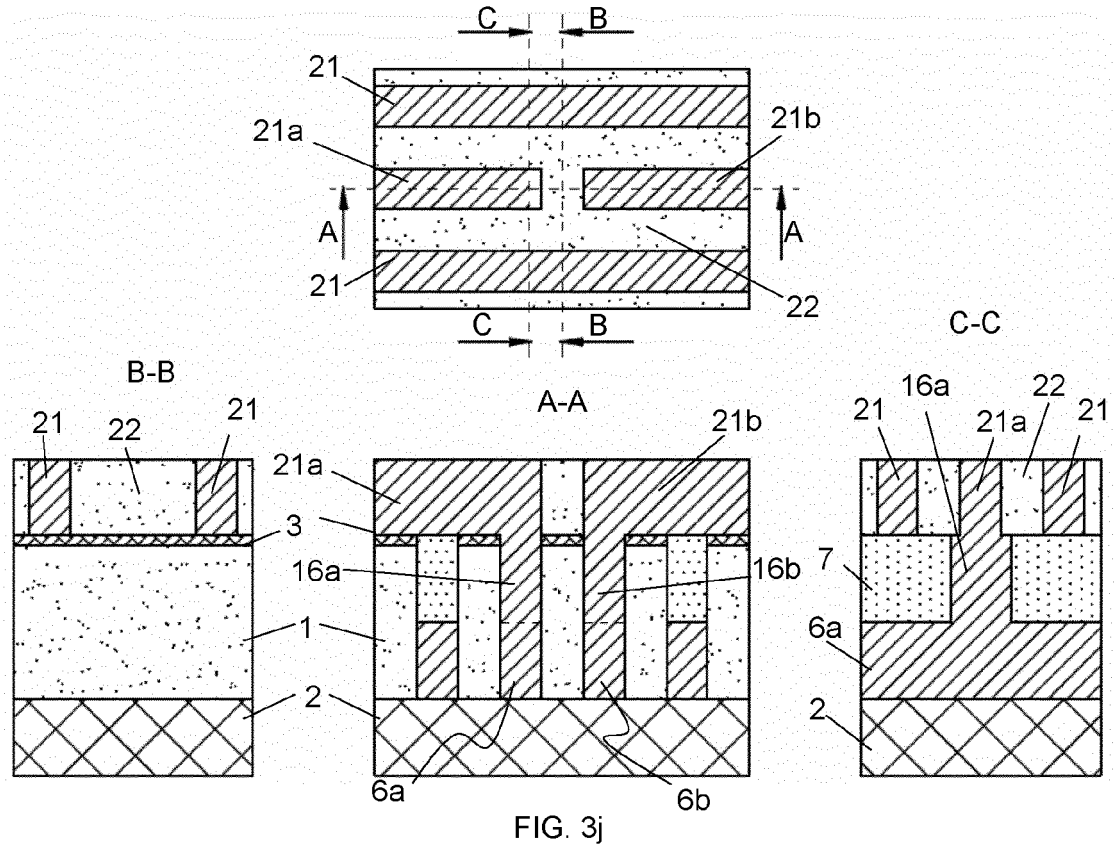

C
B
21
21a
21b
A
A
21
C
B
11
11
B-B
21
21
A-A
21b
21a
3
16a
16b
1
2
6a
6b
C-C
21
16a
21a
21
7
6a
2

FIG. 3i


C
B
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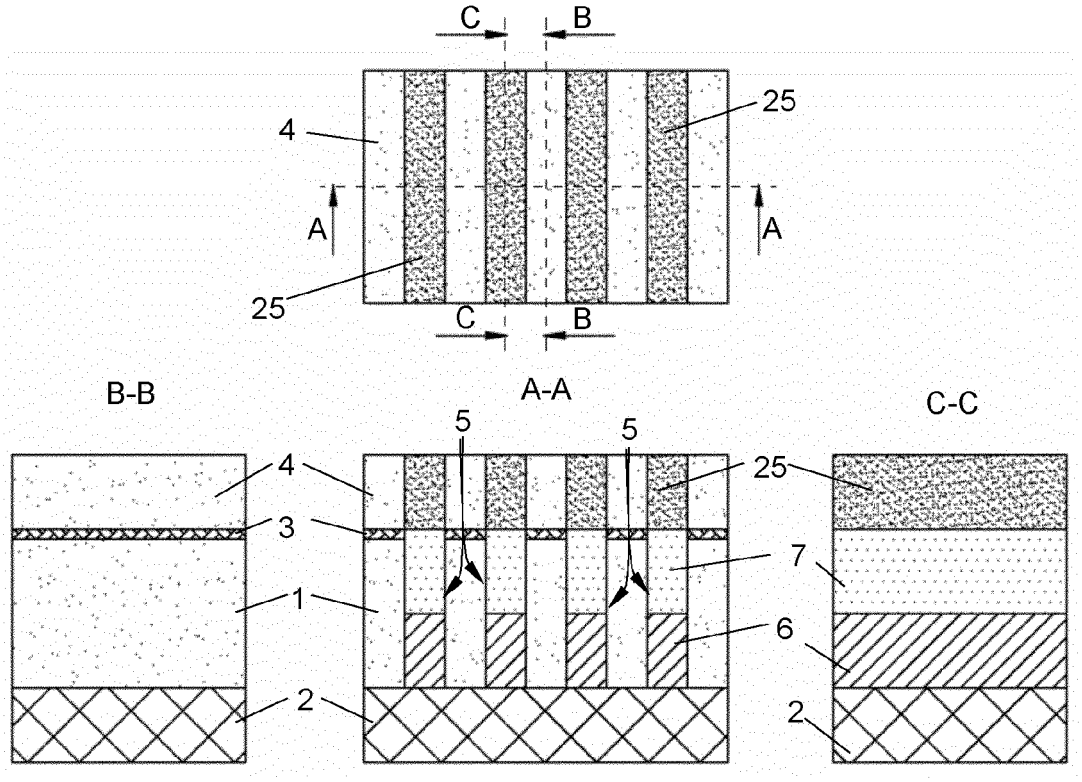
21a
21b
A
A
21
22
C
B
B-B
21
22
21
A-A
21b
21a
3
16a
16b
1
2
6a
6b
C-C
21
16a
22
21
21a
21
7
6a
2

FIG. 3j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B
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25
A
A
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C
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B-B
A-A
C-C
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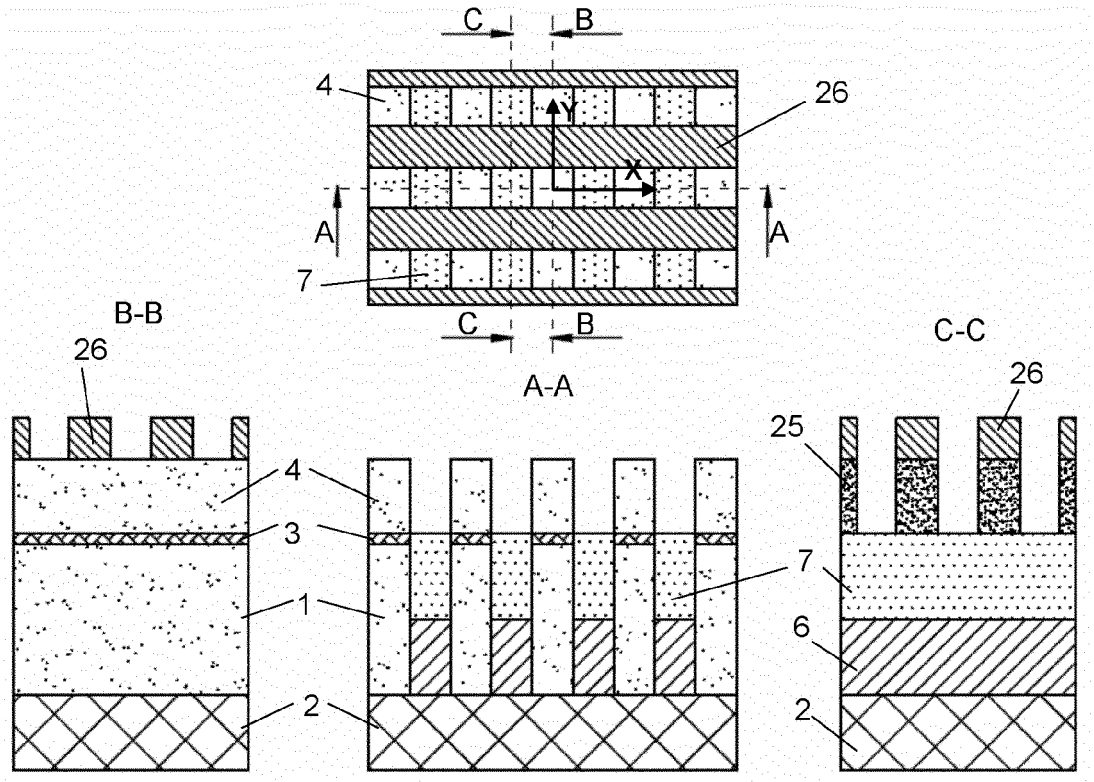
5
4
25
3
7
1
6
2
2

FIG. 4a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A
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C
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B-B
A-A
C-C
26
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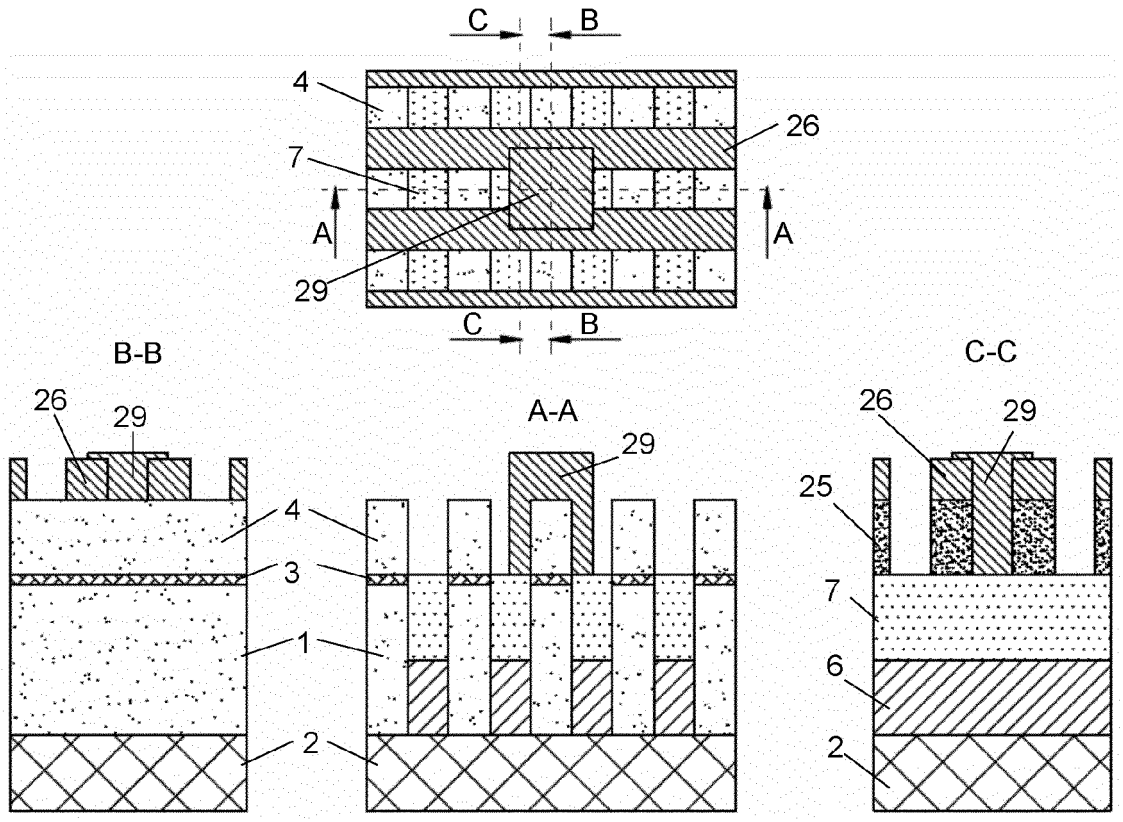
25
4
3
7
1
6
2
2

FIG. 4b


C
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26
7
A
A
29
C
B
B-B
C-C
26
29
A-A
29
26
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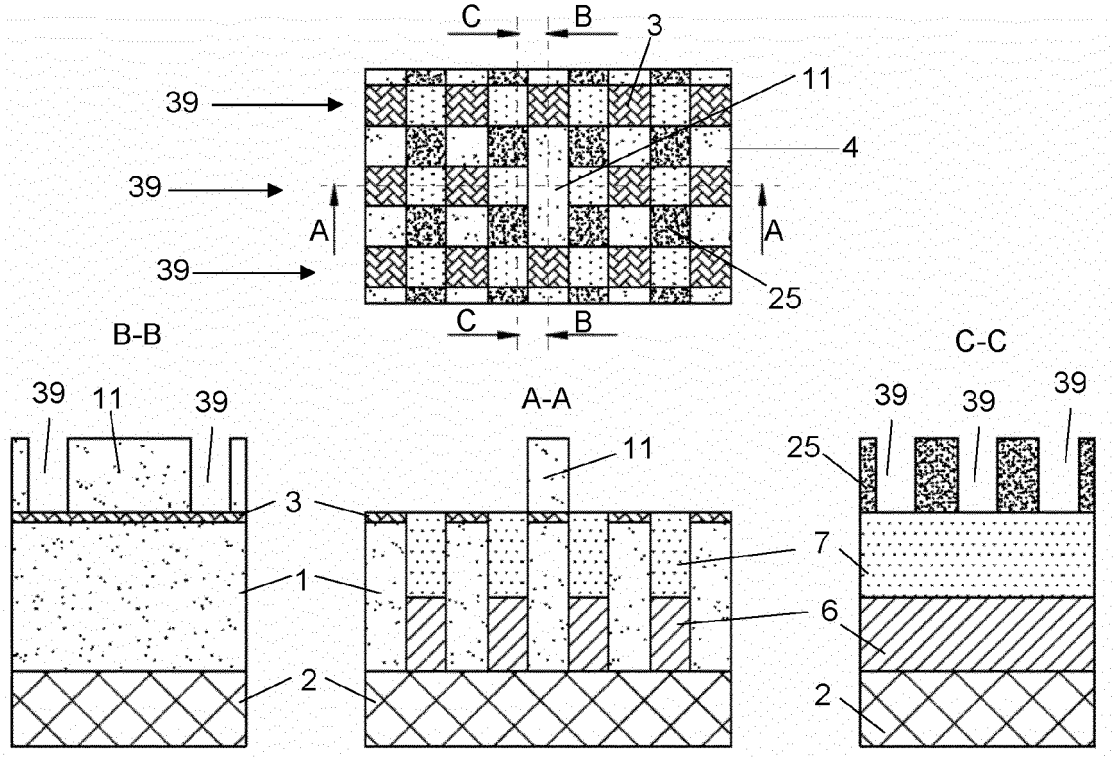
25
4
3
7
1
6
2
2

FIG. 4c


C
B
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11
4
39
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25
C
B
B-B
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11
39
A-A
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25
11
3
7
1
6
2
2

FIG. 4d

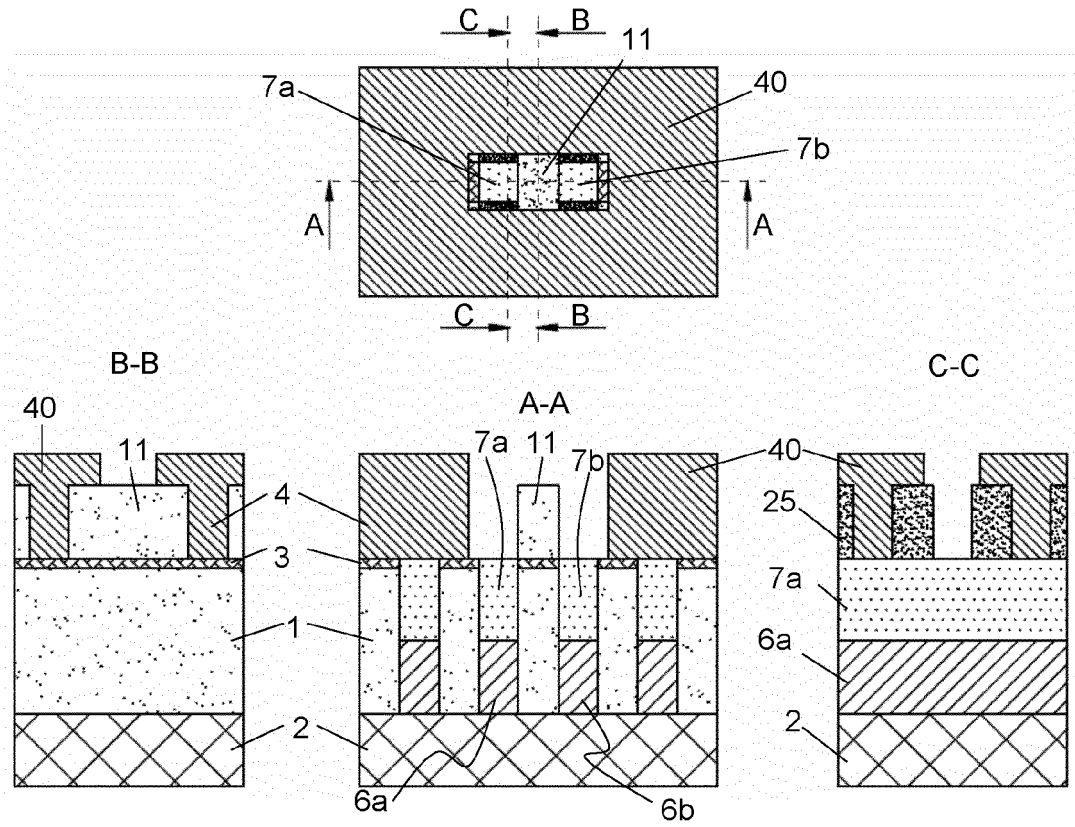

C
B
11
7a
40
7b
A
A
C
B
B-B
A-A
C-C
40
11
7a
11
7b
40
4
25
3
7a
1
6a
2
2
6a
6b

FIG. 4e

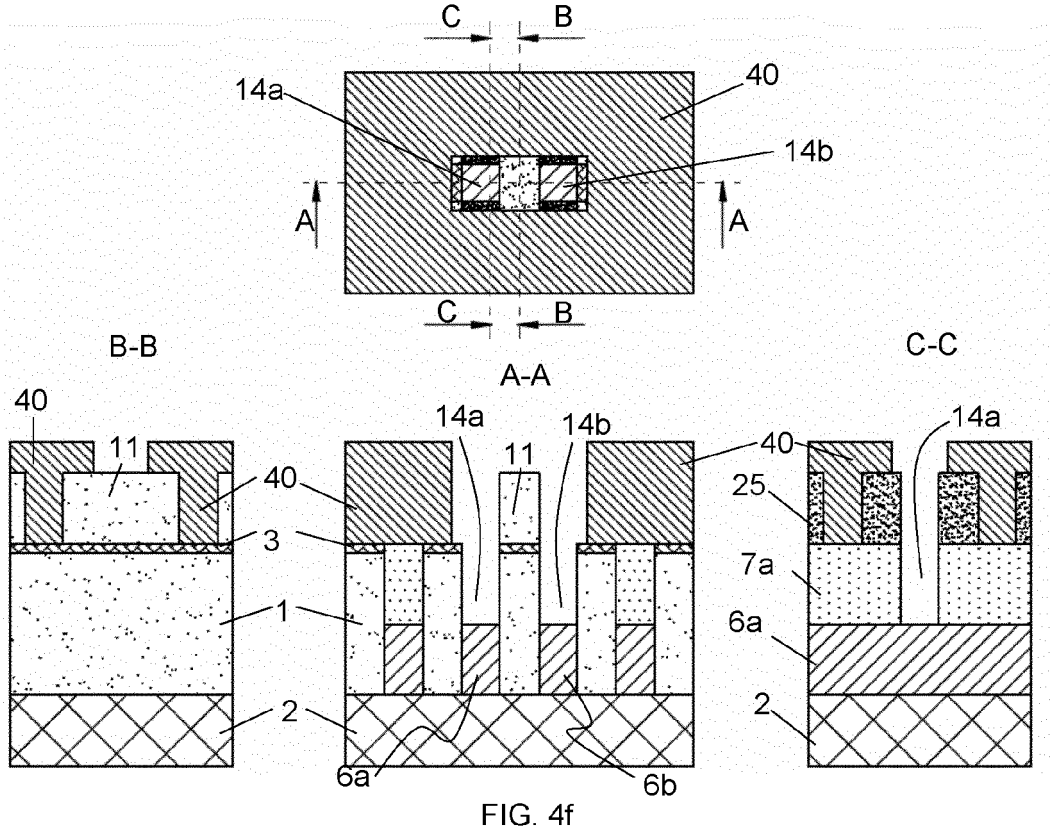
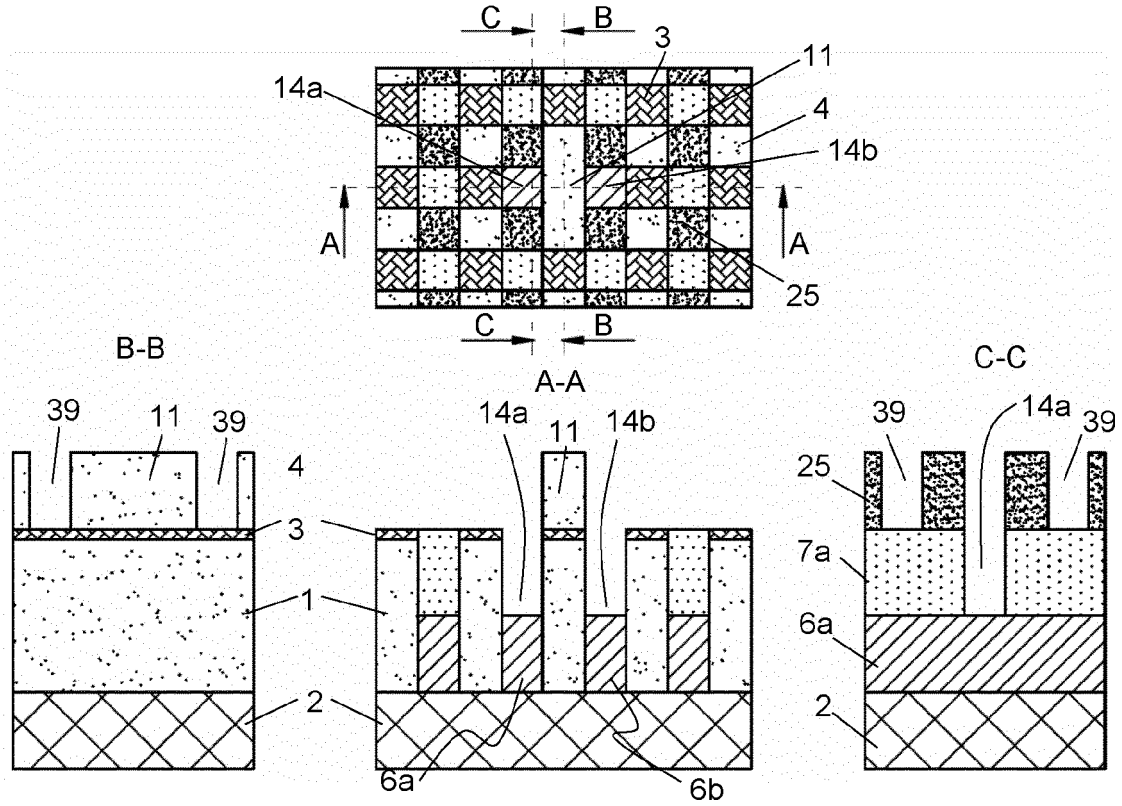

C
B
14a
40
14b
A
A
C
B
B-B
A-A
C-C
40
11
14a
14b
40
11
40
25
3
7a
1
6a
2
2
6a
6b

FIG. 4f


C
B
3
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14a
4
14b
A
A
25
C
B
B-B
A-A
C-C
39
11
39
14a
11
14b
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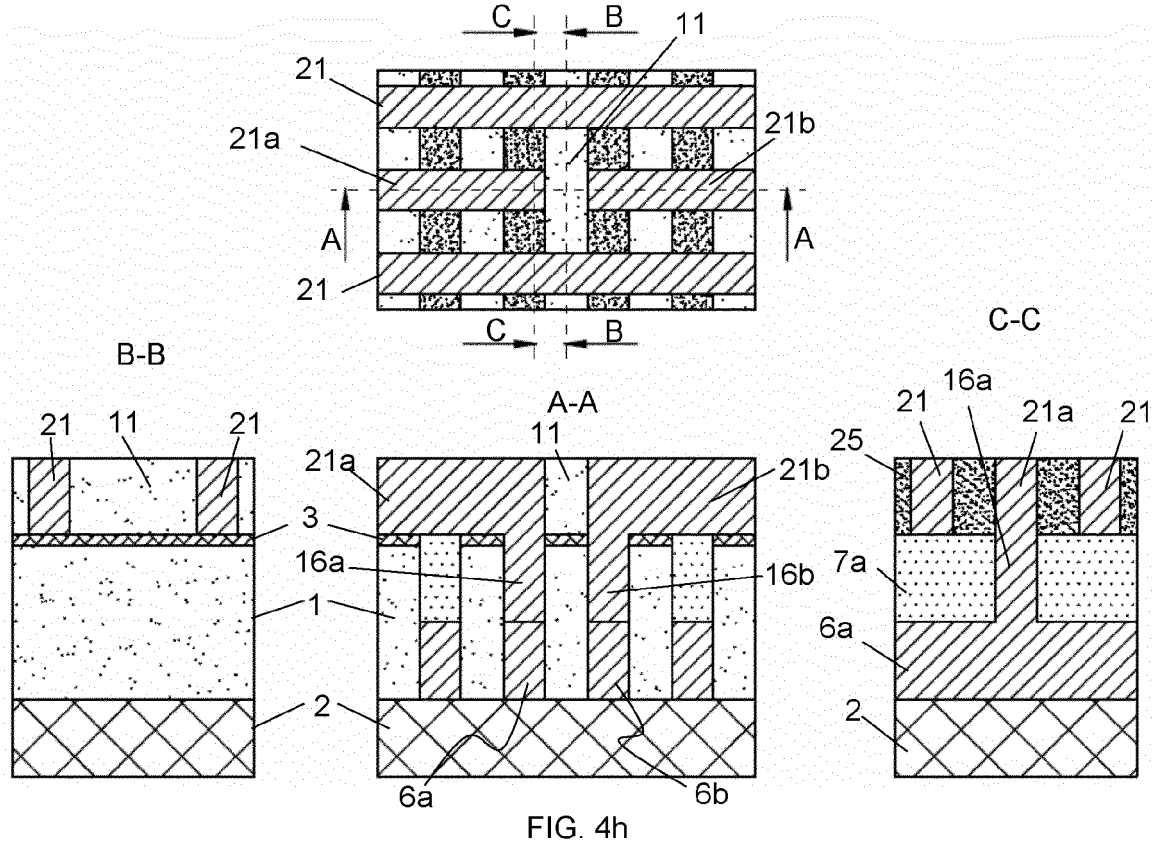
14a
39
4
25
3
7a
1
6a
2
2
6a
6b

FIG. 4g


C
B
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21
21a
21b
A
A
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C
B
B-B
A-A
C-C
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21a
11
21b
21
16a
21a
21
25
3
16a
16b
7a
1
6a
2
2
6a
6b

FIG. 4h

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EUROPEAN SEARCH REPORT

Application Number
EP 20 20 0264

DOCUMENTS CONSIDERED TO BE RELEVANT

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	23 March 2021	Ploner, Guido

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		US 6455436 B1	24-09-2002
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