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(54) MULTILEVEL PHASE-CHANGE MEMORY, METHOD FOR MANUFACTURING THE MULTILEVEL PHASE-CHANGE MEMORY AND METHODS FOR PROGRAMMING AND READING THE MULTILEVEL PHASE-CHANGE MEMORY

(57) A phase-change memory block (1), comprising: a semiconductor body (102) housing a selection transistor (15); a electrical-insulation body (112, 121) on the semiconductor body (102); a conductive region (11), extending through the electrical-insulation body (112, 121), electrically coupled to the selection transistor (15); a plurality of heater elements (34) in the electrical-insulation body (112, 121), each including a first end in electrical contact with a respective portion of the conductive region (11) and a second end that extends away from the conductive region (11); and a plurality of phase-change data-storage regions (50) extending in the electrical-insulation body (112, 121), each being electrically and thermally coupled to one respective heater element (34) at the second end of the respective heater element (34).

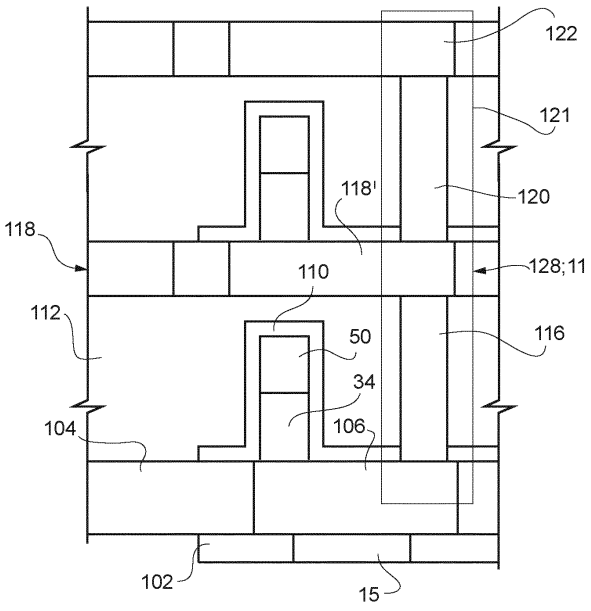

FIG. 11

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Description

[0001] The present invention relates to a phase-change memory (PCM) block, a phase-change memory including a plurality of PCM blocks, a method for manufacturing the PCM block and methods for programming and reading the PCM block. In particular, the PCM block is of a physical multilevel type.

[0002] As is known, phase-change memories use a class of materials having the property of switching between two phases having distinct electrical characteristics, associated to two different crystallographic structures of the material, and precisely a non-orderly amorphous phase and an orderly crystalline or polycrystalline phase. The two phases are thus associated to values of resistivity that differ considerably from one another, even by two or more orders of magnitude.

[0003] Currently, the elements of Group XVI of the periodic table, such as for example Te or Se, also known as chalcogenide materials or chalcogenides, may be used in phase-change memory cells. As is known, for example, from P. Zuliani, et al., "Overcoming Temperature Limitations in Phase Change Memories With Optimized GexSbyTez", IEEE Transactions on Electron Devices, Volume 60, Issue 12, pages 4020-4026, Nov. 1, 2013, it is possible to use alloys of Ge, Sb, and Te ($Ge_xSb_yTe_z$, for example $Ge_2Sb_2Te_5$) optimised by appropriately choosing the percentages of the elements that form said alloys.

[0004] The temperature at which phase transition occurs depends upon the phase-change material used. In the case of $Ge_2Sb_2Te_5$ alloy, for example, below 150°C both the amorphous phase and the crystalline phase are stable. If the temperature is increased beyond 200°C, there is noted a fast re-arrangement of the crystals, and the material becomes crystalline. To bring the chalcogenide into the amorphous state, it is necessary to increase further the temperature up to melting point (approximately 600°C) and then cool it rapidly.

[0005] Numerous memories are known that exploit phase-change materials as elements for storage of the two stable states (amorphous and crystalline states), which may each be associated to a respective bit at "1" or at "0". In these memories, a plurality of memory cells are arranged in rows and columns to form an array. Each memory cell is coupled to a respective selection element, which may be implemented by any switching device, such as PN diodes, bipolar junction transistors, or MOS transistors, and typically includes a chalcogenide region in contact with a resistive contact, also known as heater. A storage element is formed in a contact area between the chalcogenide region and the heater. The heater is connected to a conduction terminal of the selection element.

[0006] From an electrical standpoint, the crystallization temperature and the melting temperature are obtained by causing flow of an electric current through the resistive contact that extends in direct contact with or is functionally coupled to the chalcogenide material, thus heating it by the Joule effect.

[0007] According to the prior art, various processes of production of phase-change memory cells are known, which, however, present some disadvantages and limitations. In particular, in PCM of know type, each storage element is typically configured to store one bit only. To overcome this limitation, multilevel storage elements have been proposed, wherein one cell can be programmed according to more than two resistance values, so that a respective plurality of information can be stored in the cell. The plurality of resistance values can be achieved by using controlled writing pulses that can set intermediate resistance states between the "SET" state and the "RESET" state.

[0008] The stability of the intermediate levels of the resistance is a critical aspect due to the drift in resistance values in time and temperature.

[0009] There is thus felt the need to provide a phase-change memory (PCM) block, a phase-change memory including a plurality of PCM blocks, a method for manufacturing the PCM block and methods for programming and reading the PCM block, that meet the need identified above.

[0010] Patent document US2010/259962 relates to structure, use and making of re-programmable non-volatile memory cell arrays, and, more specifically, to three-dimensional arrays of memory storage elements formed on semiconductor substrates.

[0011] Patent document US2010/270593 relates to high density memory devices, and particularly to memory devices in which multiple planes of memory cells are arranged to provide a three-dimensional 3D array.

[0012] Patent document US2013/170283 relates to technology for non-volatile storage.

[0013] However, the above-mentioned drawbacks are not overcome.

[0014] According to the present invention, a phase-change memory (PCM) block, a phase-change memory including a plurality of PCM blocks, a method for manufacturing the PCM block and methods for programming and reading the PCM block are consequently provided, as defined in the annexed claims.

[0015] For a better understanding of the present invention, preferred embodiments thereof are now described, purely by way of non-limiting example and with reference to the attached drawings, wherein:

- Figures 1A and 1B show respective views of a PCM block according to the present invention;
- Figure 1C shows a PCM memory including a plurality of PCM blocks of Figure 1B;
- Figure 2 is a schematic electrical representation of the PCM block of Figure 1B;
- Figure 3 sows SET and RESET pulses to be applied to a PCM cell in order to program the PCM cell in respective logic states;
- Figures 4A, 4B show schematically a circuit repre-

sentation of one PCM block of Figure 1A, with an exemplary biasing scheme for programming the PCM block;

- Figures 5A, 5B show schematically a circuit representation of a PCM memory of Figure 1C including a plurality of PCM blocks, with an exemplary biasing scheme method for programming the PCM memory;
- Figure 6 shows schematically a circuit representation of one PCM block of Figure 1A, with an exemplary biasing scheme for reading the PCM block;
- Figures 7-11 show subsequent method steps to manufacture a PCM block of Figure 1A;
- Figure 12 schematically shows a system that includes one or more PCM blocks of Figure 1A or 1B, or a PCM memory of Figure 1C; and
- Figure 13 is a further embodiment of a PCM block.

[0016] Figure 1A illustrates a portion of a PCM memory (in the following referred to as "PCM block" 1) in a triaxial system of mutually orthogonal axes X, Y, Z. Figure 1B shows the PCM block 1 of Figure 1A in the XZ plane. Figure 1C shows a portion 1' of a PCM memory including a plurality of PCM blocks 1.

[0017] The PCM block 1 is manufactured by processing a substrate of a silicon wafer through front-end processing steps, in particular manufacturing steps of a CMOS process. In particular, formed in the substrate are insulation regions (not illustrated in Figure 1A), which delimit active areas. Formed (e.g., by implants of dopant species) in the active areas are drain regions, source regions, and gate regions of respective MOS transistors 15.

[0018] The PCM block 1 further includes a plurality of contacts 11 (e.g., of tungsten) having the function of electrical contacts with the aforementioned MOS transistors 15. Each contact 11 extends with electrical continuity in the direction of the Z axis. The MOS transistors 15 are also referred to as selection transistors, operable to address, during use, memory cells of PCM block 1.

[0019] With reference to Figure 1A, the contacts 11 extend, in one embodiment, in the form of pillars.

[0020] A plurality of phase-change material elements (in what follows, "PCM element") 50, for example a chalcogenide such as a GST (Ge-Sb-Te) compound, in particular $Ge_2Sb_2Te_5$ extend in a strip-like form along a respective direction parallel to the Y-axis; each PCM element 50 is thermally and electrically separated (or isolated) from the other PCM elements 50.

[0021] A plurality of resistive regions 34 (i.e., heaters, having the function of locally heating the PCM element 50 for triggering a selective phase-change of the heated portion) are further present. With reference to Figure 1B, a plurality of resistive regions 34 extend laterally to each contact 11. Considering one contact 11, each resistive region 34 of such plurality of resistive regions 34 arranged laterally to the considered contact 11, has one end electrically coupled to that contact 11 and the other end electrically and thermally coupled to a portion of the PCM element 50 designed to store a logic datum (i.e., designed to undergo a phase-change of SET or RESET type). In other words, a plurality (two or more) of resistive regions 34 are electrically coupled to each contact 11. More in particular, for each contact 11, the resistive regions 34 are coupled between that contact 11 and a respective PCM element 50.

[0022] Figure 2 is a schematic electrical illustration of Figure 1B (showing one column 11 to which resistive regions 34 and PCM elements 50 are coupled). With further reference to Figure 2, one end of each of the resistive regions 34 is in electrical contact with a respective portion of one contact 11; the other end of each resistive region 34 is electrically coupled to an electrical terminal of a respective control switch M1, M2, ..., MN (switches are not shown in Figures 1A-1C) through a portion of the phase-change material (PCM element 50). The other electrical terminal of each control switch M1-MN is connected to a biasing voltage V_{DD}. (Each control switch M1-MN is, for example, a MOS transistor and the electrical terminals are source and drain terminals. The gate terminal of each control switch M1-MN can be biased by a respective control signal Vb1-VbN provided by a respective control line, to turn on/off the respective control switch M1-MN.

[0023] The portion of the PCM element 50 directly coupled to one respective resistive region 34, and such resistive region 34, form a PCM cell, which can be programmed (in logic states known as SET and RESET) and read to write and, respectively, acquire a logic datum stored in the phase-change memory element.

[0024] During a writing (programming) operation, by activating (i.e., turning on) a control switch M1, M2, ..., MN and the selector transistor 15 to which the respective contact 11 is coupled, an electrical current flows through the PCM cell, to cause the respective resistive region 34 to generate heat by Joule effect. During use, to program a SET or RESET state of the memory element, the PCM cell is biased at a writing voltage by applying a voltage V_{DD} across it. The PCM element 50 is coupled to each resistive region 34 in a per se known way, to receive the heat generated through Joule effect by the resistive region 34.

[0025] The electrical resistance of the contact 11 (in the range of few Ω, or few tens of Ω) is negligible with respect to the resistance of the resistive region (heater) 34 (in the range of some kΩ, or few tens of kΩ). Accordingly, the programming voltage drops almost completely across the resistive region 34.

[0026] With reference to Figure 3, SET and RESET pulses are shown; during a time interval T1 a RESET pulse is generated, that is an electric pulse adapted to program the addressed PCM cells in the logic state "0". Similarly, during a time interval T2, a SET pulse is generated, that is an electric pulse adapted to program the addressed PCM cells in the logic state "1". The SET and RESET pulses are known to have different shapes both in terms of duration in time and in maximum voltage/cur-

rent values. In particular, the RESET voltage pulse has a duration T1 lower than the duration T2 of the SET pulse; however, the maximum voltage value V1 (or corresponding current value) needed for the RESET pulse is higher than the maximum voltage value V2 (or corresponding current value) needed for the SET pulse. In the present description, the voltage value to be applied to the PCM element 50 to program the RESET state is considered to be V1=3V; the voltage value to be applied to the PCM element 50 to program the SET state is considered to be V2=2V; the voltage value to be applied to the PCM element 50 not to change the already programmed state is considered to be V3<1V (equal to 0.6V during a reading operation). It is apparent that these values are not limiting the present invention, and are used in the following disclosure for merely improving the understanding of the present invention. Of course, other voltage values can be used depending upon the specific design of the memory, the phase-change material used, etc. In general terms, provided that V1=Vreset according to the technology and design parametrs, V2 is chosen equal to 2/3·Vreset and V3 is chosen lower than, or equal to, 1/3·Vreset (in any case, lower than the "RESET" threshold).

[0027] Writing or programming operations of the PCM block 1 and PCM memory 1' are described with reference to Figures 4A, 4B and 5A, 5B. Figures 4A, 4B show a simplified electrical representation of one PCM block 1 of the PCM memory 1'; Figures 5A, 5B show a simplified electrical representation of a plurality of PCM blocks 1.

[0028] In figures 4A, 4B and 5A, 5B, each line r1-r3 corresponds to a respective stripe of PCM element 50 to be biased, and each line c1-c3 corresponds to the biasing lines used to bias the gate terminals of selection transistors 15 belonging to different PCM blocks 1 and aligned along the X-axis. For ease of representation, Figures 4A, 4B and 5A, 5B show only three lines r1-r3 and three lines c1-c3; it is apparent that the teaching applies to any number of lines.

[0029] PCM cells are connected between lines r1-r3 and lines c1-c3, forming a matrix. To program the PCM cells, the present invention foresees a double writing step.

[0030] Figures 4A and 5A show the voltage distribution during a first writing step aimed at writing (i.e., program) the PCM cells connected to the same line r2. During this operation, all the cells in the addressed line r2 are written to the "RESET" or "0" state (i.e., by applying a pulse of V1=3V across them), irrespective of whether such PCM cells are to be programmed at the RESET state or the SET state. To this end, line r2 is biased at a reference voltage of 0V (e.g., ground), while lines r1 and r3 are biased at V1=3V. In order to have the required voltage drop across the PCM cell to be programmed, all lines c1-c3 are biased at V1=3V. Therefore, only the PCM cells coupled to r2 undergoes a voltage drop of 3V, while the PCM cells coupled to r1 and r3 undergoes a voltage drop of 0V. Consequently, the PCM cell coupled between r2 and c1-c3 are all programmed at the RESET state, while the remaining PCM cells retain their current state.

[0031] In a second writing step, Figures 4B and 5B, carried out after the first writing step, the SET pulse is applied selectively to those PCM cells coupled to the line r2 that are to be programmed at the SET state, while maintaining unaltered the already programmed RESET state in those PCM cells that are to be programmed at the RESET state. To this end, line r2 is biased at the reference potential of 0V, while lines r1 and r3 are biased at an intermediate voltage of 1V.

[0032] It is supposed in this example that only the PCM cell coupled between r2 and c1 is to be programmed at the SET state. Therefore, line c1 is biased at V2=2V, so that the voltage drop across the PCM cell coupled between r2 and c1 is V2=2V, and the PCM cell is programmed at the SET state.

[0033] Lines c2 and c3 are biased at the intermediate voltage of 1V, so that the voltage drop across all the other PCM cells is 0V or 1V and, in any case, in a voltage range that do not alter the already programmed state of such cells. In this situation, a spurious power consumption exists, but is the limited to the size of the PCM block 1 considered.

[0034] With specific reference to Figures 5A and 5B, it can be appreciated that the required voltage values for the columns 11 can be obtained by biasing the gate terminals of the selection transistors 15 using lines c1-c3 and use the threshold voltage drop to have the required voltage on the respective contacts 11. The gate terminals are, in this example, biased at 4V and, with a threshold supposed to be equal to 1V, one can have V1=3V on the respective contact 11. It is noted, as represented in Figures 5A and 5B, that the other PCB block that are not currently programmed are not stressed (all their lines are biased at 0V).

[0035] Figure 6 shows graphically a possible reading scheme, according to a schematic representation of a PCM memory having a matrix-like arrangement of rows and columns, and PCM cells coupled between such rows and columns. Only the addressed PCM cells are read, while all the others are not stressed, i.e. voltage applied to the PCM cells not to be read is zero.

[0036] Line r2, to which the PCM cells to be read are coupled, is biased at reference voltage of 0V, while all other lines r1 and r3 are biased at V3=0.6V. All lines c1-c3 are biased at V3=0.6V. Therefore, a voltage drop of V3=0.6V is applied only across the PCM cells coupled between line r2 and lines c1-c3; the remaining PCM cells are subject to a null voltage drop. It is therefore apparent that during the reading operations there is no spurious current consumption. The actual reading operation is performed through sense amplifiers 16, in a per se known way. Sense amplifiers 16 carry out reading of the data stored in the PCM cells, comparing the current that flows in the PCM cell selected (or an electrical quantity correlated thereto) with a reference current that flows in a reference cell (so-called double-ended reading) or else with a reference current supplied by a reference-current gen-

erator (so-called single-ended reading).

[0037] It is noted that each line c1-c3 and r1-r3 is connected to a respective transistor the connects / disconnects such line to / from the biasing voltage. In practice all of these transistors are not equivalent in term of size (they are designed according to the maximum voltage/current they must sustain during use). To perform the write operation, a current is needed to flow through the transistors associated to the lines r1-r3, thus implementing a write operation "by row" and allowing the corresponding transistors to sink only the current related to the single PCM cell to be written. During reading, the sense amplifiers 16 should not be connected "by row", because, as shown in Figure 6, line r2 "sees" the total current of all PCM cells connected to it. Taking the above into account, a solution is to write "by row" and read "by column", that is to say connect the sense amplifiers 16 to the lines c1-c3 during reading operations, to read the current flowing through the line r2, which is the only line selected for reading. Since the matrix shown in Figure 6 is symmetric, the comparators may be connected to the lines r1-r3 as well, to perform the reading operation. Figures 5A and 5B shown a 3D representation of the matrix; in this case, the comparators must be connected to the lines r1-r3 to perform a reading operation. In any case, it is noted that the currently known method for reading a PCM memory can be applied analogously to the PCM memory according to the present application.

[0038] With reference to Figures 7-11, a method for manufacturing the PCM memory 1' is disclosed, according to an embodiment of the present invention.

[0039] With reference to Figure 7, a wafer 100 is provided, including a semiconductor body 102 (including a substrate and, optionally, one or more epitaxial layers on the substrate, for example of silicon). By known techniques, for example belonging to a standard CMOS process, a plurality of selection transistors 15 are formed in the semiconductor body 102. The selection transistors 15 defines active areas of semiconductor body 102. A dielectric or insulating layer 104 is formed over the semiconductor body 102, e.g. by growing or depositing silicon oxide or silicon nitride.

[0040] Through a lithographic step, trenches are formed within the dielectric layer 104, reaching and exposing the conductive terminals of the selection transistors 15. A conductive material (e.g., metal) is deposited within the trenches thus forming respective local interconnection lines, LIL, or plugs 106 that are in electrical contact with the selection transistors 15 (in particular with a conductive terminal, such as the drain terminal) of the selection transistors 15. The plugs 106 connect the selection transistors 15 to further conductive layers that will be formed above the dielectric layer 104 (such as the contacts 11) .

[0041] Then, Figure 8, steps are carried out to form the resistive regions 34 (heaters) and the PCM elements 50. To this end, a step of deposition a resistive layer, for example doped titanium nitride (doped-TiN), is carried out on the dielectric layer 104 and the plugs 106. This step is followed by formation, in a per se known manner, of a layer of phase-change material, for example by depositing a chalcogenide, such as a GST (Ge-Sb-Te) compound, e.g., $Ge_2Sb_2Te_5$. Other phase-change materials may be used. Formation of the PCM layer is carried out over the resistive layer.

[0042] The resistive layer and the PCM layer thus formed are patterned, e.g. through lithography and etching, to form a stack including the resistive region 34 and the PCM element 50 previously described, having a shape and an extension according to the design of the PCM memory 1'. It is noted that the PM element 50 is a continuous strip along Y-axis, while the resistive regions 34 extend at selective regions of the PCM element 50, i.e. at the regions of the PCM element 50 that are designed to form a memory cell. Between one resistive region 34 and another resistive region 34, along the Y-axis extension of the PM element 50, dielectric or insulating material can be deposited.

[0043] A protective layer 110, e.g. of silicon nitride, is formed on the resistive region 34 and the PCM element 50. The protective layer 110 may also extend over the dielectric layer 104 and the portions of the plugs 106 not covered by the resistive layer 34.

[0044] Then, Figure 9, a further dielectric or insulating layer 112 is formed (e.g., deposited) over the resistive region 34, the PCM element 50, the protective layer 110, the dielectric layer 104 and the plugs 106. A CMP ("Chemical-Mechanical-Polishing") step on the is dielectric layer 112 carried out. Trenches are opened through the dielectric layer 112 and the protective layer 110, reaching a region of the plugs 106 lateral to the stack formed by the resistive region 34 and the PM layer 50. The trenches are then filled with conductive material, in particular metal, more in particular tungsten. Plugs 116 extending entirely through the dielectric layer 112, in electrical contact with respective plugs 106 are thus formed.

[0045] Then, Figure 10, a step is carried out to deposit and pattern a metal layer 118 over the dielectric layer 112. The metal layer 118 is patterned in such a way to define a plurality of local interconnections 118', each of them being electrically connected to one respective plug 116.

[0046] The structure of Figure 10 (with the exception of the formation of transistors 15 and plugs 106) is then replicated, as shown in Figure 11.

[0047] With reference to Figure 11, the steps previously described are repeated in order to form further stacks of resistive regions 34 and PCM elements 50 and further plugs 120 (analogous to plugs 116 previously described) above the local interconnections 118' and in electrical contact with respective local interconnections 118'. A dielectric or insulating layer 121 is formed analogously to the dielectric layer 112 and further metal interconnections 122 (analogous to metal interconnections 118') are formed on the dielectric layer 121.

[0048] In particular, the stack identified with reference numeral 128 in Figure 11, including the plug 106 extending in electrical contact with one selection transistor 15, the plug 116 extending in electrical contact with such plug 106, the metal interconnection 118' extending in electrical contact with such plug 116, the further plug 120 and the further metal interconnection 122 extending in electrical contact with such further plug 120 form (at least in part) one contact 11 previously described. A plurality over PCM elements 50, each one including the respective heaters 34, extend one above the other along the Z-axis and are electrically connected to the same stack 128 (contact 11), as in the embodiments of Figures 1A-1C.

[0049] The steps of Figure 11 can be replicated as many time as desired, according to the design of the PCM memory 1'.

[0050] Figure 12 illustrates a portion of a system 200 that may be implemented in various devices, such as for example PDAs, portable computers, phones, photographic cameras, video cameras, etc. The system 200 may include one or more among a controller 210 (e.g., a microprocessor), an input/output device 220, for example a keypad and a display, a chip housing in an integrated form the PCM memory 1', a wireless interface 240, and a random-access memory (RAM) 260, connected together by a bus system 250. According to one embodiment, the system 200 may be supplied by a battery 280, or alternatively by a mains supply source. It is clear that the scope of the present disclosure is not limited to embodiments comprising all the components of Figure 12. For example, one or more from among the random-access memory (RAM) 260, the wireless interface 240, the battery 280, and the input/output device 220 may be omitted.

[0051] The advantages of the present disclosure emerge clearly from the foregoing description.

[0052] For example, the area/bit of a PCM memory according to the present invention is considerably reduced with respect to known PCM memories. The increase of the level also increases the area gain depending of the number of the cells stacked.

[0053] Finally, it is clear that modifications and variations may be made to what has been described and illustrated herein, without thereby departing from the scope of the present invention, as defined in the annexed claims.

[0054] For example, Figure 13 shown a PCM block 300 according to a further embodiment of the present invention. Elements of the PCM block 300 common to the PCM block 1 of Figure 1B are identified with the same reference numerals. As shown in Figure 13, further resistive regions (heaters) 34' extend away from the contact 11 at a side of the contact 11 opposite to the side facing the resistive regions 34. Resistive regions 34' have characteristics analogous to the resistive regions 34, and are manufactured accordingly during the same process steps, in a way that is per se apparent to the skilled person. PCM elements 50 are electrically and thermally coupled to the resistive regions 34', analogously to PCM elements 50. The functioning of the PCM block 300 is the same as that of PCM block 1 and is therefore not further described.

Claims

1. A phase-change memory, PCM, block (1), comprising:

   a semiconductor body (102) housing a selection transistor (15);
   a electrical-insulation body (112, 121) on the semiconductor body (102);
   a conductive region (11), extending through the electrical-insulation body (112, 121), electrically coupled to the selection transistor (15);
   a plurality of heater elements (34) in the electrical-insulation body (112, 121), each including a first end in electrical contact with a respective portion of the conductive region (11) and a second end that extends away from the conductive region (11); and
   a plurality of phase-change elements (50) extending in the electrical-insulation body (112, 121) and including data storage regions, each data storage region being electrically and thermally coupled to one respective heater element (34) at the second end of the respective heater element (34).

2. The PCM block according to claim 1, wherein said electrical-insulation body (112, 121) includes a plurality of overlying electrical-insulation layers (112, 121), each heater element (34) and the associated data-storage region (50) extending in a respective one of said electrical-insulation layers (112; 121).

3. The PCM block according to claim 2, wherein said conductive region (11) includes a plurality of electrically interconnected plugs (116, 120), each plug extending in a respective one of said electrical-insulation layers (112; 121) .

4. The PCM block according to claim 2 or 3, wherein said plurality of electrical-insulation layers (112; 121) includes one or more stacks of overlying electrical-insulation layers (112; 121), each stack including a respective first electrical-insulation layer (121) on a respective second electrical-insulation layer (112),

   and wherein for each stack a respective interconnection conductive line (118') extends between said first (112) and second (121) electrical-insulation layers,
   the interconnection conductive line (118') being electrically connected to the plug extending in

said first electrical-insulation layer (112) and to the plug extending in said second electrical-insulation layer (121) thus forming a conductive path between the first and the second electrical-insulation layers (112, 121).

5. The PCM block according to claim 4, wherein said interconnection conductive line (118') is further electrically connected to the heater element (34) extending in the first electrical-insulation layer (121).

6. The PCM block according to anyone of the preceding claims, wherein each heater element (34) and the data-storage region (50) coupled to it are covered by a sealing layer (110) of dielectric or insulating material.

7. The PCM block according to anyone of the preceding claims, wherein said heater elements (34) are aligned to one another along a vertical direction (Z) orthogonal to a plane of lie (XY) of said substrate (102).

8. The PCM block according to anyone of the preceding claims, wherein the conductive region (11) has a main extension along a first direction (Z) orthogonal to a plane of lie (XY) of the substrate (102), each heater element (34) being arranged laterally to the conductive region (11).

9. The PCM block according to any one of the preceding claims, further comprising a plurality of switching transistors (M1-MN), each one having an own first conduction terminal coupled to one respective phase-change element (50), an own second conduction terminal coupled to a bias potential (V_{DD}) and an own control terminal,

wherein the selection transistor (15) includes an own first conduction terminal coupled to the conductive region (11), an own second conduction terminal coupled to a reference-potential (GND), and an own control terminal,
the control terminals of the selection transistor (15) and of the switching transistors (M1-MN) being operable to selectively connect one respective heater element (34) and the associated phase-change element (50) between the reference-potential (GND) and the bias potential (V_{DD}).

10. The PCM block according to any one of the preceding claims, wherein the conductive region (11) has a value of electrical resistance negligible with respect to the electrical resistance of each heater element (34).

11. A phase-change memory (1'), including a plurality of PCM blocks (1) according to anyone of claims 1-10.

12. A chip comprising:

- one or more PCM blocks (1) according to anyone of claims 1-10;
- a biasing circuitry comprising:

a programming stage including voltage generators configured to cause a SET or RESET programming current to flow through selected heater elements (34) to generate heath by Joule effect, so as to cause a controlled phase-transition of the associated data-storage region of the phase-change element (50);
a reading stage including a plurality of sense amplifiers (16), each coupled to one respective data-storage region (50) to read a current flowing through the respective data-storage region (50) during a read operation of the PCM block (1).

13. A system (200) comprising:
a processing unit (210); and one among:

at least one PCM block (1) according to anyone of claims 1-10;
a phase-change memory (1') according to claim 11;
a chip according to claim 12.

14. A method of manufacturing a phase-change memory, PCM, block (1), comprising the steps of:

forming, in a semiconductor body (102), a selection transistor (15);
forming an electrical-insulation body (112, 121) on the semiconductor body (102);
forming a conductive region (11) through the electrical-insulation body (112, 121), electrically coupled to the selection transistor (15);
forming a plurality of heater elements (34) in the electrical-insulation body (112, 121), each including a first end in electrical contact with a respective portion of the conductive region (11) and a second end that extends away from the conductive region (11); and
forming a plurality of phase-change elements (50) extending in the electrical-insulation body (112, 121) and including data-storage regions, each data-storage region being electrically and thermally coupled to one respective heater element (34) at the second end of the respective heater element (34).

15. The method according to claim 14, wherein forming said electrical-insulation body (112, 121) includes

forming a plurality of overlying electrical-insulation layers (112, 121), and wherein forming the heater elements (34) and the data-storage region (50) includes burying each heater element (34) and the associated data-storage region (50) in a respective one of said electrical-insulation layers (112; 121) .

16. The method according to claim 15, wherein forming the conductive region (11) includes forming a plug in a respective one of said electrical-insulation layers (112; 121) and electrically connecting each of said plugs to one another.

17. The method according to claim 15 or 16, wherein forming said plurality of electrical-insulation layers (112; 121) includes forming one or more stacks of overlying electrical-insulation layers (112; 121), each stack including a respective first electrical-insulation layer (121) on a respective second electrical-insulation layer (112),

the method further comprising forming, for each stack, a respective interconnection conductive line (118') between said first (112) and second (121) electrical-insulation layers,
the interconnection conductive line (118') being formed in electrical connection with the plug extending in said first electrical-insulation layer (112) and with the plug extending in said second electrical-insulation layer (121) thus forming a conductive path between the first and the second electrical-insulation layers (112, 121).

18. The method according to claim 17, wherein said interconnection conductive line (118') is further electrically connected to the heater element (34) extending in the first electrical-insulation layer (121).

19. The method according to anyone of claims 14-18, further comprising the step of forming a sealing layer (110) of dielectric or insulating material covering a respective heater element (34) and data-storage region (50) coupled to that heater element (34).

20. The method according to anyone of claims 14-19, wherein said heater elements (34) are formed aligned to one another along a vertical direction (Z) orthogonal to a plane of lie (XY) of said substrate (102).

21. The method according to anyone of claims 14-20, wherein the conductive region (11) is formed with a main extension along a first direction (Z) orthogonal to a plane of lie (XY) of the substrate (102), each heater element (34) being formed laterally to the conductive region (11).

22. A method for programming a phase-change memory (1'), said phase-change memory device (1) comprising:

at least one row line (r2);
a plurality of column line (c1-c3);
a plurality of phase-change memory cells, each of them being coupled between the row line (r2) and one respective column line (c1-c3);
the method comprising the steps of:

in a first operating condition associated with a first time interval (T1), applying a RESET programming voltage to the plurality of phase-change memory cells, thus programming said plurality of phase-change memory cells to a first logic state; and
in a second operating condition associated with a second time interval (T2) that is subsequent to the first time interval (T1), applying a SET programming voltage to selected phase-change memory cells among said plurality of phase-change memory cells, thus programming said selected phase-change memory cells to a second logic state,
wherein the maximum voltage value of the RESET programming voltage is higher than that of the SET programming voltage.

23. A method for reading a phase-change memory (1'), said phase-change memory device (1) comprising:

a plurality of row lines (r1-r3);
a plurality of column line (c1-c3);
a plurality of phase-change memory cells, each of them being coupled between the row line (r2) and one respective column line (c1-c3);
the method comprising the steps of:

bias one row line to which a phase-change memory cell to be read is connected, among said plurality of row lines, at a ground reference voltage;
bias the remaining row line of said plurality of row lines at a reading voltage;
bias the plurality of column line (c1-c3) at said reading voltage;
acquire, through a sense amplifier (16), a current flowing through the column line (c1-c3) to which the phase-change memory cells to be read is connected.

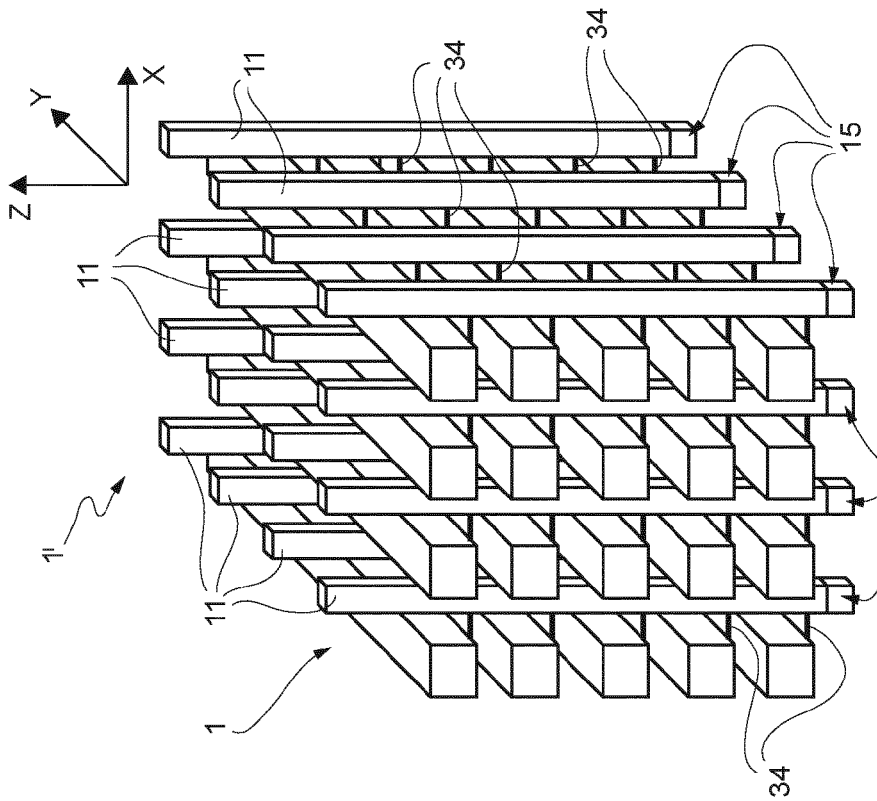

FIG. 1C

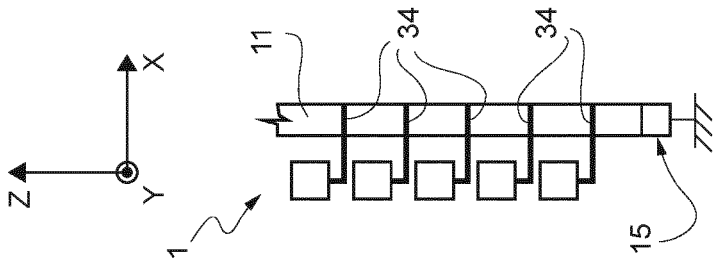

FIG. 1B

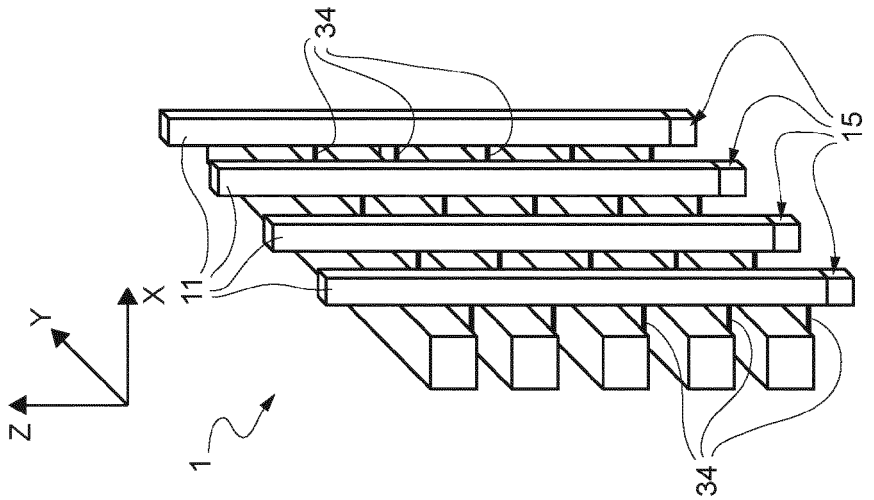

FIG. 1A

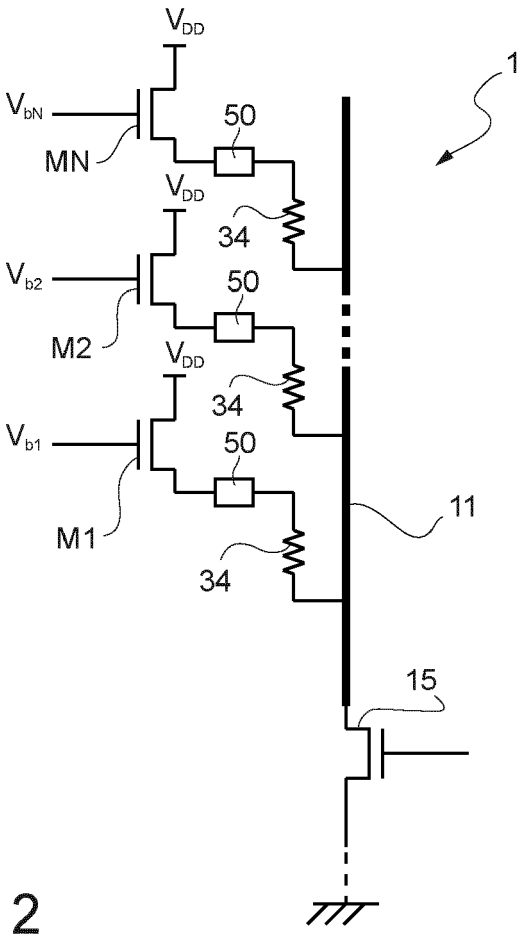
V_{DD}
V_{bN}
MN
50
1
V_{DD}
34
V_{b2}
50
M2
V_{DD}
34
V_{b1}
50
11
M1
34
15

FIG. 2

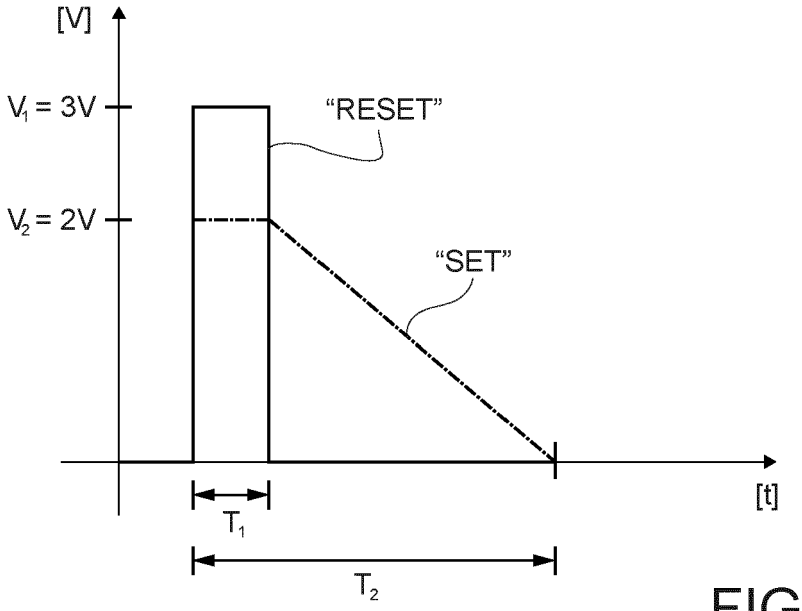
[V]
V_1 = 3V
"RESET"
V_2 = 2V
"SET"
[t]
T_1
T_2

FIG. 3

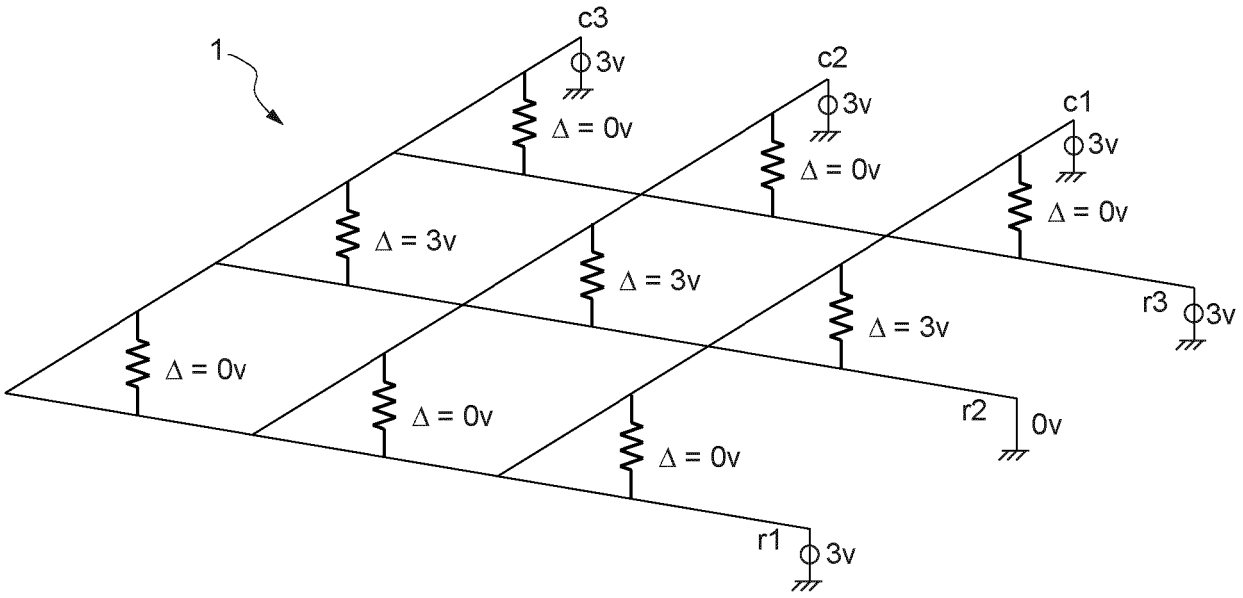
1
c3
3v
c2
3v
c1
3v
Δ = 0v
Δ = 0v
Δ = 0v
Δ = 3v
Δ = 3v
Δ = 3v
r3
3v
Δ = 0v
Δ = 0v
Δ = 0v
r2
0v
r1
3v

FIG. 4A

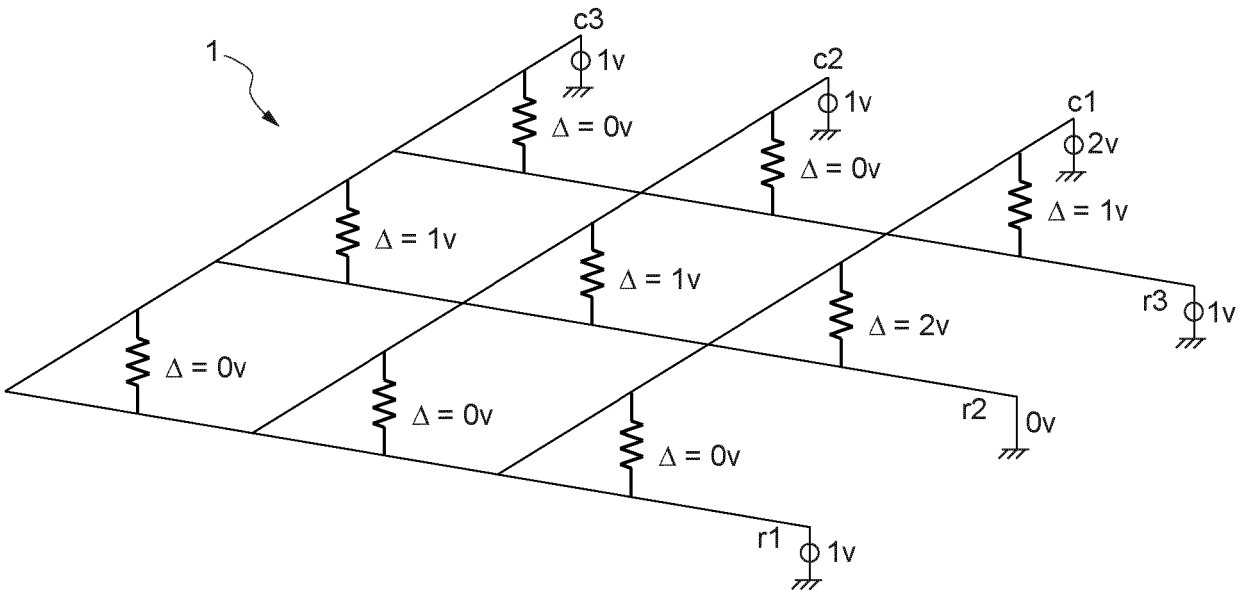
1
c3
1v
c2
1v
c1
2v
Δ = 0v
Δ = 0v
Δ = 1v
Δ = 1v
Δ = 1v
Δ = 2v
r3
1v
Δ = 0v
Δ = 0v
Δ = 0v
r2
0v
r1
1v

FIG. 4B

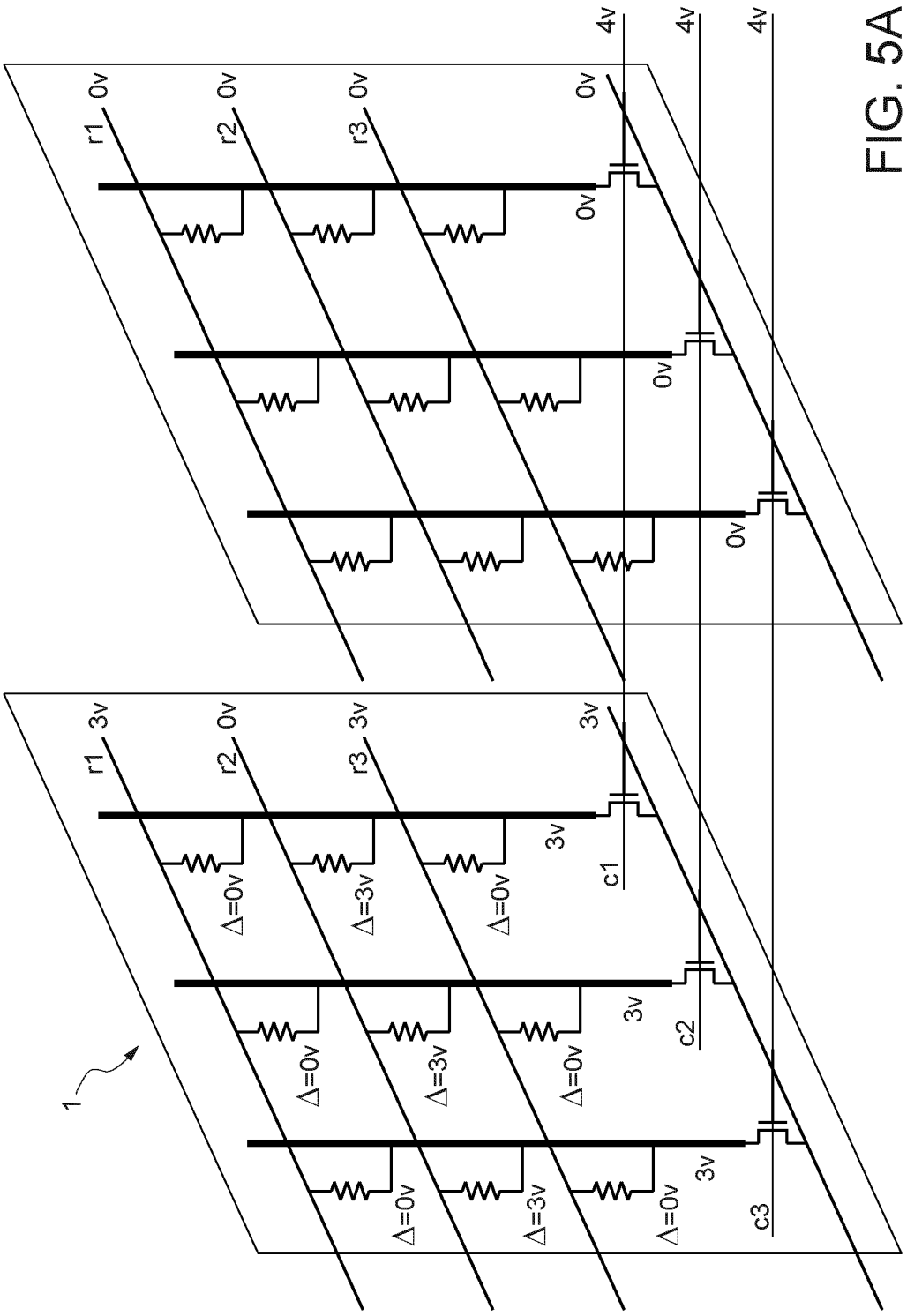

FIG. 5A

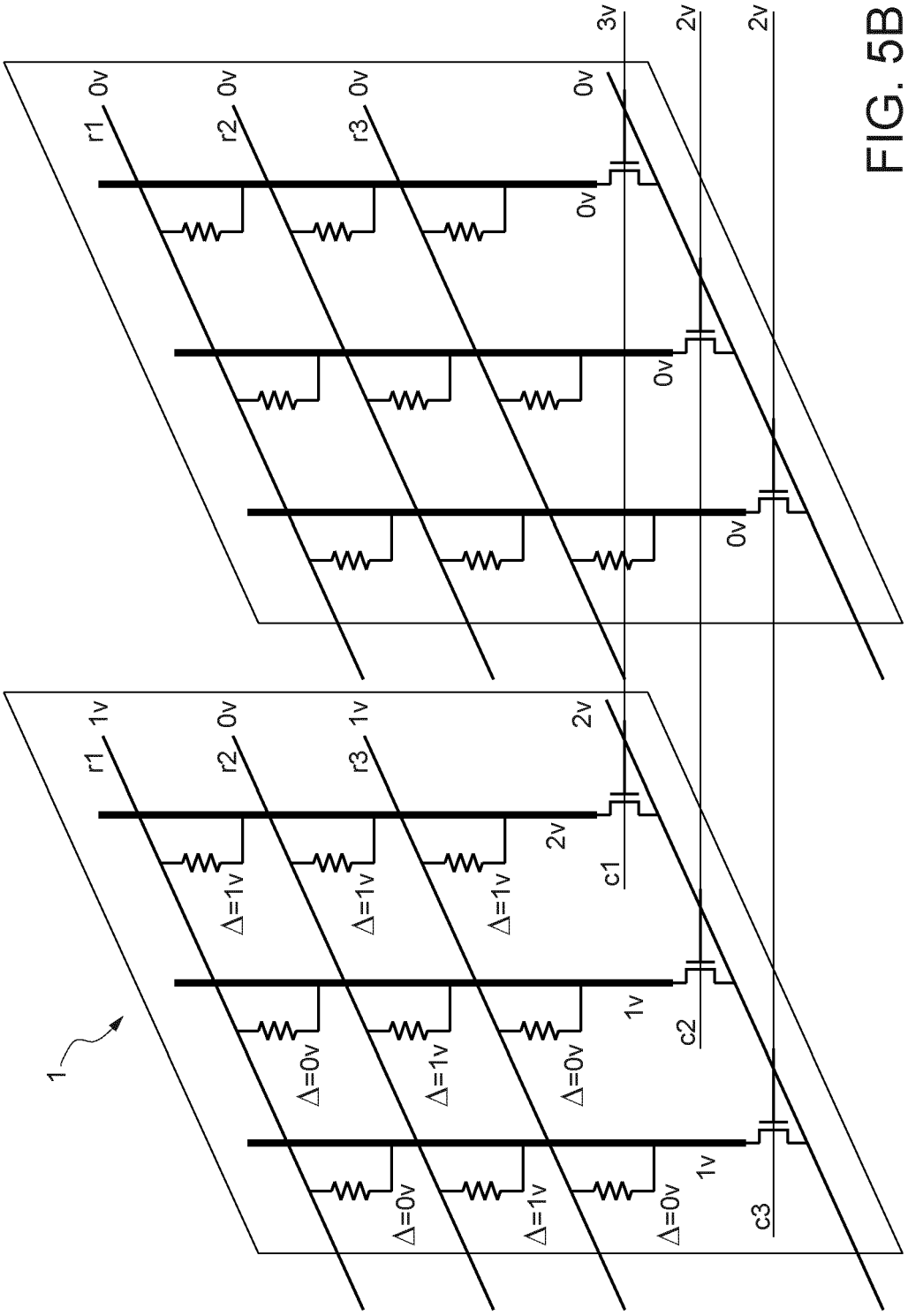
r1 0v
r2 0v
r3 0v
0v
3v
2v
2v
0v
0v
0v
r1 1v
r2 0v
r3 1v
2v
Δ=1v
Δ=1v
Δ=1v
2v
c1
Δ=0v
Δ=1v
Δ=0v
1v
c2
Δ=0v
Δ=1v
Δ=0v
1v
c3
1

FIG. 5B

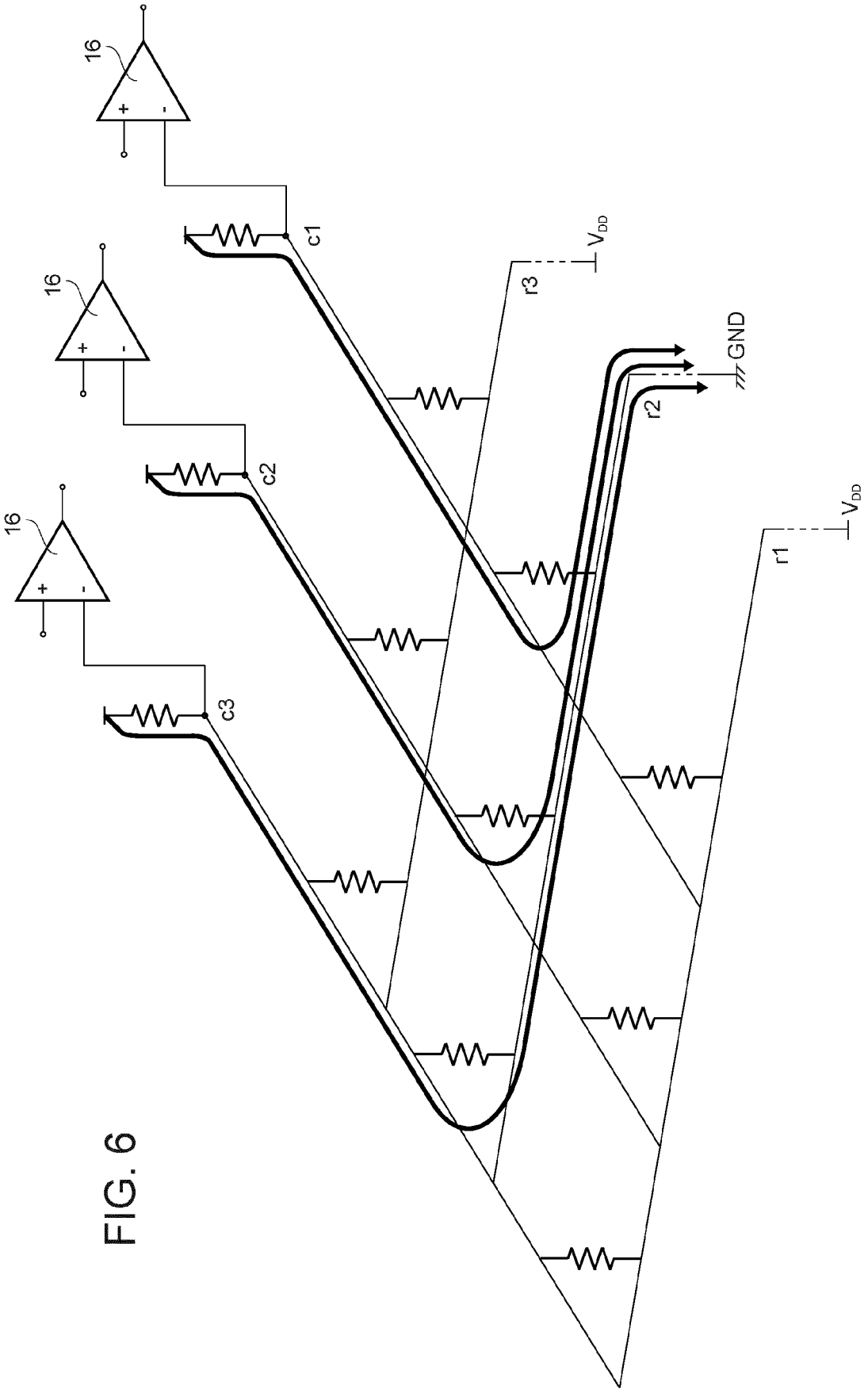

FIG. 6

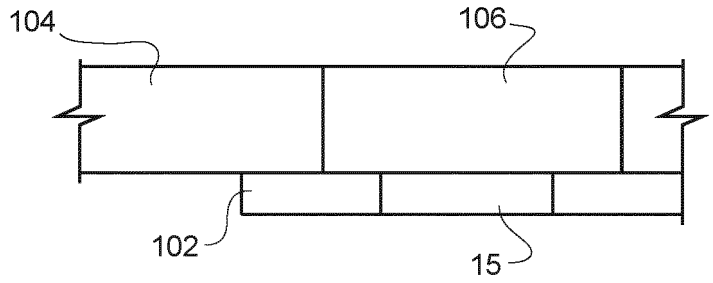

FIG. 7

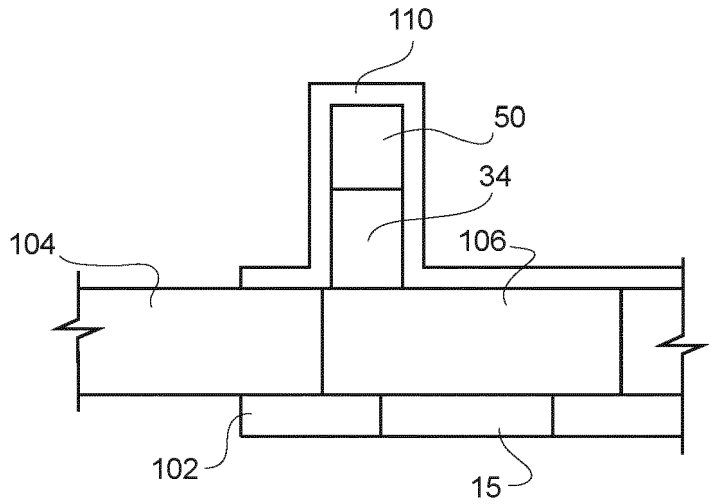

FIG. 8

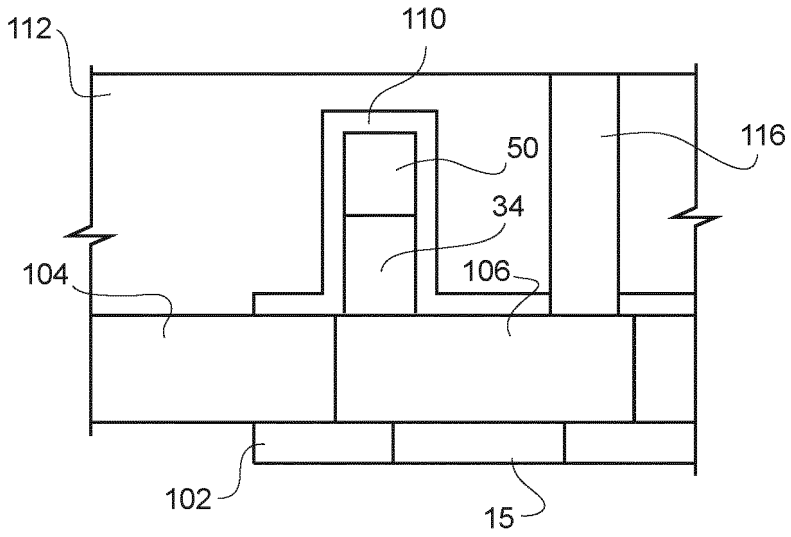

FIG. 9

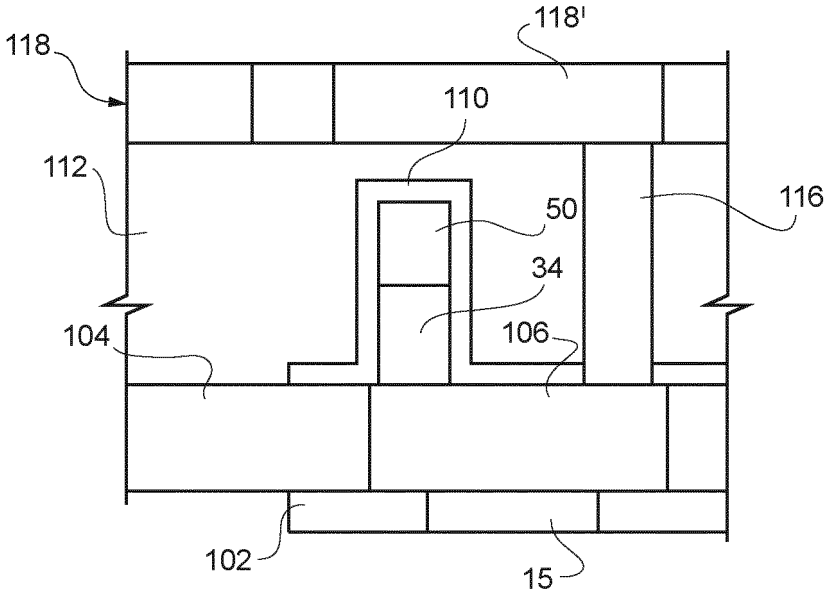
118'
118
110
112
116
50
34
104
106
102
15

FIG. 10

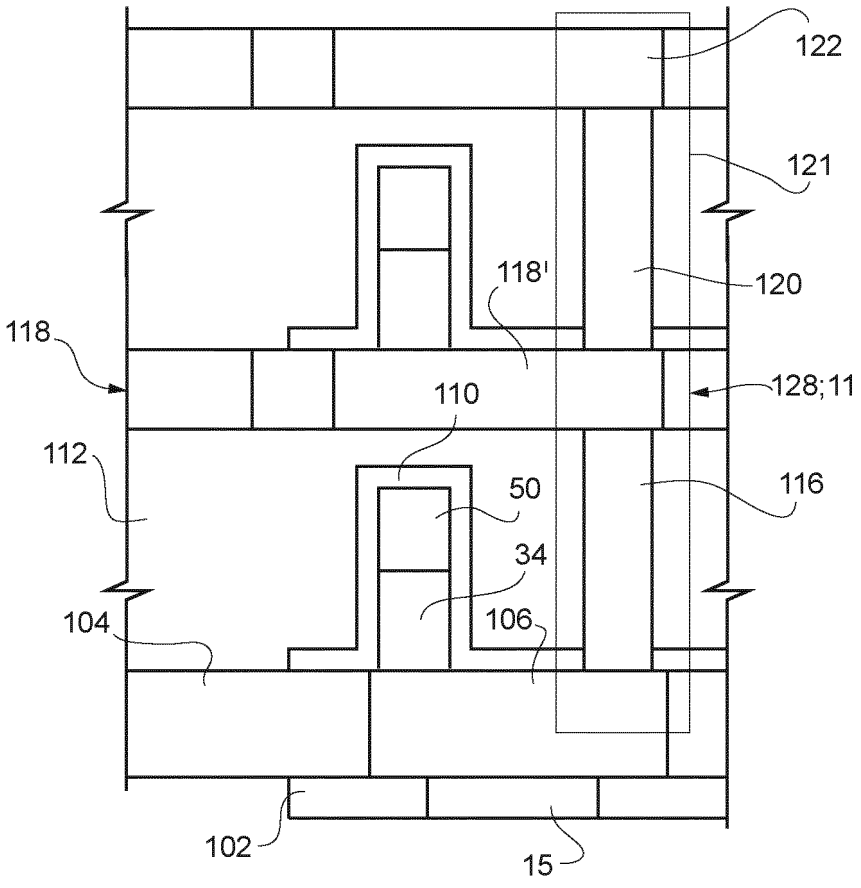
122
121
118'
120
118
128;11
110
112
50
116
34
104
106
102
15

FIG. 11

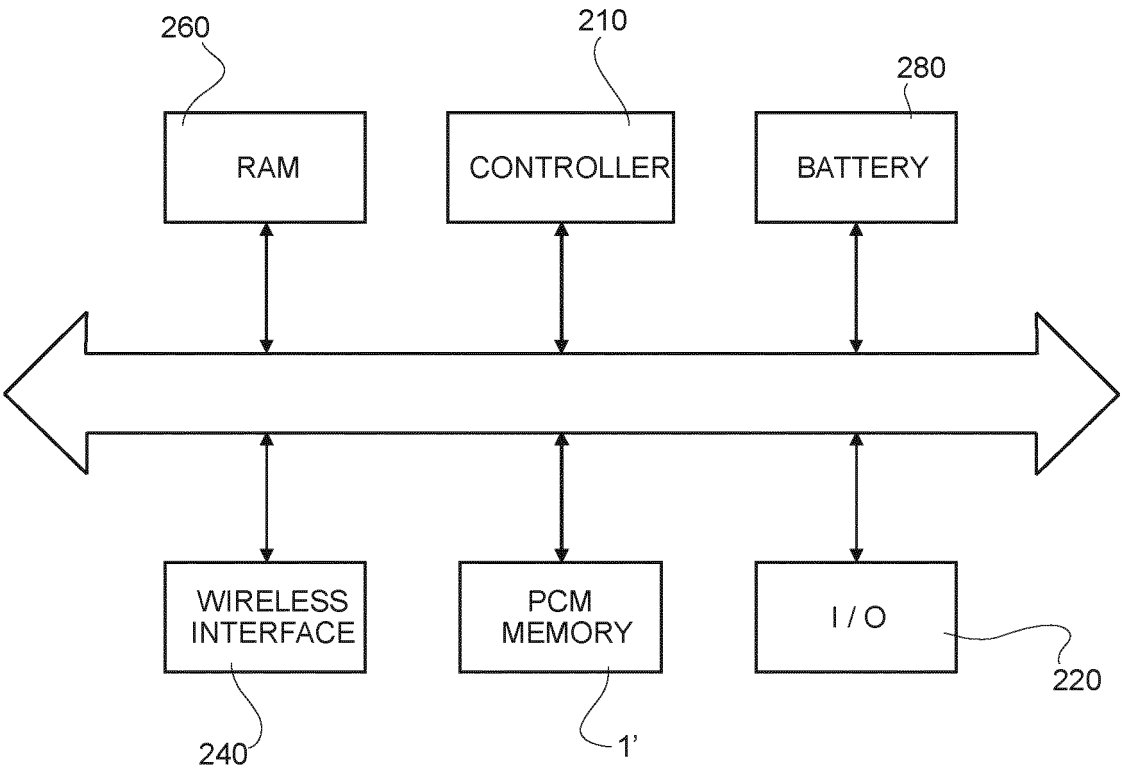
260
210
280
RAM
CONTROLLER
BATTERY
WIRELESS INTERFACE
PCM MEMORY
I / O
220
240
1'

FIG.12

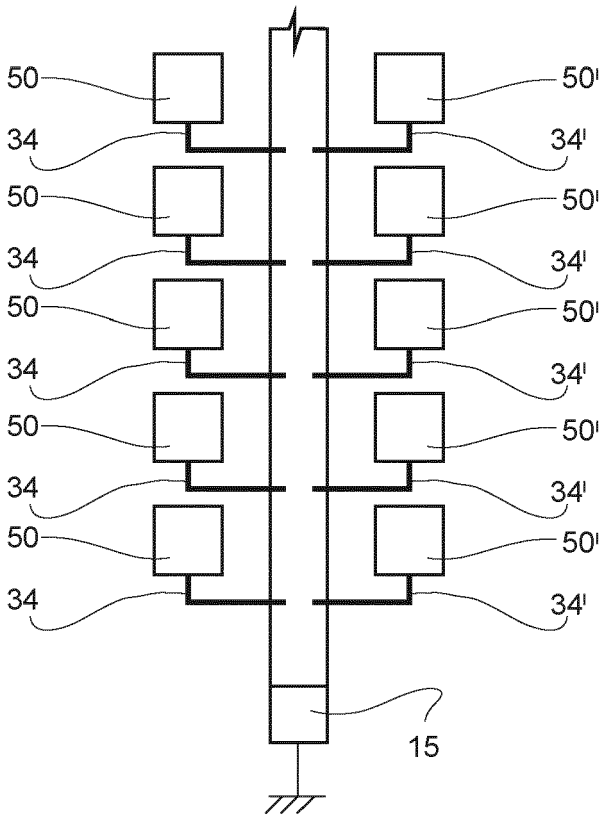
50
34
50'
34'
15

FIG. 13

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EUROPEAN SEARCH REPORT

Application Number
EP 21 21 7194

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2010/259962 A1 (YAN TIANHONG [US] ET AL) 14 October 2010 (2010-10-14)	1,2,6-8, 10-15, 19-23	INV. H01L27/24 H01L45/00
Y	* paragraph [0103] * * paragraph [0121] - paragraph [0143]; figure 8 * * paragraph [0063] - paragraph [0074]; figures 3,4 * * paragraph [0075] - paragraph [0081]; figures 1,5 *	3-5,9, 16-18	
Y	US 2010/270593 A1 (LUNG HSIANG-LAN [US] ET AL) 28 October 2010 (2010-10-28) * paragraph [0083] - paragraph [0084]; figure 16 *	3-5, 16-18	
Y	US 2013/170283 A1 (LAN ZHIDA [US] ET AL) 4 July 2013 (2013-07-04) * paragraph [0139] - paragraph [0141] * * paragraph [0160] * * figure 13 *	9	

TECHNICAL FIELDS SEARCHED (IPC)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	5 May 2022	Gröger, Andreas

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05-05-2022

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- US 2013170283 A **[0012]**

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- **P. ZULIANI et al.** Overcoming Temperature Limitations in Phase Change Memories With Optimized GexSbyTe. *IEEE Transactions on Electron Devices,* 01 November 2013, vol. 60 (12), 4020-4026 **[0003]**