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## Description

### TECHNICAL FIELD

[0001] The present disclosure relates to a drive circuit, an LED circuit and a related device.

### BACKGROUND

[0002] LED light source is a light source based on light-emitting diodes, which has the advantages of low-voltage power supply, low energy consumption, strong applicability, high stability, short response time, no pollution to the environment, multi-color light emission, etc. With the continuous development of LED technology, LED light sources have been widely used. Shopping malls, factories, houses and other scenarios use a large number of LED light sources as lighting or decoration, and adjust the brightness of these LED light sources when needed to provide comfortable lighting.

[0003] At present, LED drivers need to meet certain performance requirements. For example, referring to the LED drive circuit shown in FIG 1, it includes: a rectifier module connected to an AC input power supply, an LED light source connected to the rectifier module, and a power controlling module connected to the LED light source, and a capacitor in parallel with the LED light source. Referring to FIG 2, the AC input voltage and AC input current of the LED drive circuit have good symmetry and a high power factor (PF), which can reduce or eliminate harmonic pollution to the power grid. However, this kind of high PF drive circuit cannot solve the flicker problem, it will cause harm to human eyes when used, and cannot well meet the needs of LED lighting.

### SUMMARY

[0004] The purpose of the embodiments of the present disclosure is to provide a drive circuit, an LED circuit and a related device capable of realizing high PF and no flicker to meet the drive requirements of the actual controlled load.

[0005] As a first aspect of the embodiments of the present disclosure, the embodiments of the present disclosure provide a drive circuit. The circuit may include a load current control circuit, a rectifier module, an energy storage component and a charge-discharge generating circuit, wherein: the charge-discharge generating circuit is connected to the energy storage component and the load current control circuit; the energy storage component and the charge-discharge generating circuit are connected at both ends of the rectifier module; the charge-discharge generating circuit is configured to: form a charging loop with the energy storage component during a charging process of the energy storage component, and control a charging current of the energy storage component; and form a discharging loop with the energy storage component during a discharging process of the en-

ergy storage component.

[0006] In some optional embodiments, the charge-discharge generating circuit includes a first controlled switch tube and a first switch controlling module connected to a control terminal of the first controlled switch tube, the first switch controlling module is configured to control the on-off state of the first controlled switch tube.

[0007] In some optional embodiments, the drive circuit further includes: a unidirectional current path connected in parallel with the charge-discharge generating circuit, the unidirectional current path being turned on when the energy storage component is discharged.

[0008] In some optional embodiments, the unidirectional current path includes a diode, or a body diode of the first controlled switch tube.

[0009] In some optional embodiments, the drive circuit further includes at least one first resistor connected to the first controlled switch tube.

[0010] In some optional embodiments, a circuit formed by connecting the at least one first resistor in series with the first controlled switch tube is connected in parallel with the unidirectional current path.

[0011] In some optional embodiments, the first controlled switch tube is connected to the at least one first resistor after being connected in parallel with the unidirectional current path.

[0012] In some optional embodiments, the first switch controlling module includes a first operational amplifier; a forward input terminal of the first operational amplifier is configured to connect a first reference voltage, a negative input terminal of the first operational amplifier is connected to a current output terminal of the first controlled switch tube; an output terminal of the first operational amplifier is connected to the control terminal of the first controlled switch tube.

[0013] In some optional embodiments, the first controlled switch tube is an NMOS transistor, and the current output terminal of the first controlled switch tube is a source of the NMOS transistor, or, when the charge-discharge generating circuit is connected in parallel with the unidirectional current path, the first controlled switch tube is a bipolar transistor, and the current output terminal of the first controlled switch tube is an emitter of the bipolar transistor.

[0014] In some optional embodiments, the first switch controlling module further includes a current source, a second resistor, a third resistor, a second controlled switch tube and a third controlled switch tube, wherein after the current source is connected in series with the second resistor, it is connected in parallel with the charging loop formed by the energy storage component and the first controlled switch tube; a forward input terminal of the first operational amplifier is connected between the current source and the second resistor; a drain of the third controlled switch tube is connected to the rectified busbar voltage through the third resistor, or the drain of the third controlled switch tube is configured to connect an output terminal of a controlled load through the third

resistor; and the second controlled switch tube and the third controlled switch tube are connected to form a current mirror.

**[0015]** In some optional embodiments, the drive circuit further includes a unidirectional current path, the unidirectional current path being turned on when the energy storage component is discharged; and the charge-discharge generating circuit comprising at least one fourth resistor, and the unidirectional current path being connected in parallel with the at least one fourth resistor.

**[0016]** In some optional embodiments, the load current control circuit is a linear control circuit, a buck type circuit, a fly-back type circuit or a boost type circuit.

**[0017]** As a second aspect of the embodiment of the present disclosure, the embodiments of the present disclosure provide an LED circuit, wherein includes an LED load and the drive circuit described in any one of the above.

**[0018]** As a third aspect of the embodiments of the present disclosure, the embodiments of the present disclosure provide an LED lighting fixture, wherein the LED lighting fixture includes the above-mentioned LED circuit.

**[0019]** The beneficial effects of the above technical solutions provided by the embodiments of the present disclosure at least include: the above-mentioned drive circuit provided by the embodiment of the present disclosure, for the AC input power connected to the rectifier module, the drive circuit utilizes the characteristic that the busbar voltage changes as a sine wave to charge and discharge an energy storage component. By controlling the charging current of the energy storage component, a stable working voltage can be provided for the controlled load. When the busbar voltage is higher than the voltage of the energy storage component, the busbar voltage charges the energy storage component and provides load current at the same time. When the busbar voltage is lower than the voltage of the energy storage component, the energy storage component supplies power to the controlled load, so that the power supplied to the controlled load is stable and the ripple is eliminated. Especially for the LED load, the voltage of the energy storage component is always slightly larger than the load voltage of the LED load, which can achieve no flicker. In addition, the charging current of the energy storage component is a part of the AC input current, which can realize that the AC input current and the AC input voltage are in a common axis of symmetry, and the waveform consistency of the AC input current and the AC input voltage is improved, thereby improving the PF.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** In order to more clearly illustrate the embodiments of the present disclosure or the technical solutions in the prior art, the following will briefly introduce the drawings that need to be used in the description of the embodiments or the prior art. Obviously, the drawings in the following description are some embodiments of the

present disclosure, and for those of ordinary skill in the art, other drawings can also be obtained from these drawings without any creative effort.

**[0021]** The drawings are used to provide a further understanding of the present disclosure, and constitute a part of the specification, and together with the embodiments of the present disclosure, are used to explain the present disclosure, and are not construed to limit the present disclosure. In the drawings:

FIG. 1 illustrates a schematic structural diagram of an LED drive circuit in the prior art;

FIG. 2 illustrates a schematic diagram of the waveform change of current with voltage in the LED drive circuit shown in FIG. 1;

FIG. 3 illustrates a schematic structural diagram 1 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 4 illustrates a schematic structural diagram 2 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 5 illustrates a schematic structural diagram 3 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 6 illustrates a schematic structural diagram 4 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 7 illustrates a schematic structural diagram 5 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 8 illustrates a schematic structural diagram 6 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 9 illustrates a schematic structural diagram 7 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 10 illustrates a schematic structural diagram 8 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 11 illustrates a schematic structural diagram 9 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 12 illustrates a schematic diagram of current and voltage waveforms in the drive circuit shown in FIG. 11;

FIG. 13 illustrates a schematic structural diagram 10 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 14 illustrates a schematic structural diagram 11 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 15 illustrates a schematic structural diagram 12 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 16 illustrates a schematic diagram of current and voltage waveforms in the drive circuit shown in FIG. 15;

FIG. 17 illustrates a schematic structural diagram 12

of a drive circuit provided by an embodiment of the present disclosure;

FIG. 18 illustrates a schematic structural diagram 13 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 19 illustrates a schematic structural diagram 14 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 20 illustrates a schematic structural diagram 15 of a drive circuit provided by an embodiment of the present disclosure;

FIG. 21 illustrates a schematic structural diagram 16 of a drive circuit provided by an embodiment of the present disclosure.

## DETAILED DESCRIPTION

**[0022]** Exemplary embodiments of the present disclosure will be described in more detail below with reference to the diagrams. Even though exemplary embodiments of the present disclosure are shown in the diagrams, it should be apparent that the present disclosure may be embodied in various forms and should not be limited by the embodiments set forth herein. Rather, these embodiments are provided so that the present disclosure can be more thoroughly understood, and can fully convey the scope of the present disclosure to those skilled in the art.

**[0023]** In order to solve the problem that the LED drive circuit in the prior art cannot meet the requirements of high PF and no flicker, the embodiment of the present disclosure provides a drive circuit. Referring to FIG. 3, the drive circuit includes a rectifier module connected to an AC input power supply, a load current control circuit for controlling the connected controlled load current, an energy storage component and a charge-discharge generating circuit; the charge-discharge generating circuit is connected to the energy storage component and the load current control circuit; the energy storage component and the charge-discharge generating circuit are connected to the both ends of the rectifier module; the controlled load is connected between the rectifier module and the load current control circuit; the charge-discharge generating circuit is configured to form a charging loop with the energy storage component during a charging process of the energy storage component, and control a charging current of the energy storage component; and form a discharging loop with the energy storage component during a discharging process of the energy storage component.

**[0024]** In a specific embodiment, the energy storage component may be a capacitor, and the controlled load may be an LED.

**[0025]** In some optional embodiments, the drive circuit provided by the embodiment of the present disclosure controls the energy storage component to charge and discharge through the charge-discharge generating circuit. When the rectified input voltage is greater than the voltage of the energy storage component, the energy

storage component starts the charging process. At this time, the rectifier module, the energy storage component and the charge-discharge generating circuit may form a charging loop, and the charge-discharge generating circuit may generate a current from the current input terminal in to the current output terminal out. The current may be a constant current or a variable current that varies as one or some voltages or currents in the drive circuit changes. The charging current of the energy storage component can be controlled by the charge-discharge generating circuit. When the rectified input voltage is lower than the voltage of the energy storage component, the energy storage component starts the discharge process. At this time, the energy storage component, the LED load, the load current control circuit and the charge-discharge generating circuit form a discharging loop, and the current in the charge-discharge generating circuit flows from the current output terminal out to the current input terminal in.

**[0026]** The aforementioned drive circuit provided by the embodiment of the present disclosure, for the AC input power supply connected to the rectifier module, the drive circuit utilizes the characteristic that the line voltage changes as a sine wave to charge and discharge an energy storage component. By controlling the charging current of the energy storage component, a stable working voltage is provided for the controlled load. When the line voltage is higher than the voltage of the energy storage component, the line voltage charges the energy storage component and provides load current at the same time. When the line voltage is lower than the voltage of the energy storage component, the energy storage component supplies power to the controlled load, so as to provide stable power supply for the controlled load and remove the ripple. Especially for the LED load, the voltage of the energy storage component is always slightly larger than the load voltage of the LED load, which can achieve no flicker. In addition, the charging current of the energy storage component is a part of the AC input current, which can make the AC input current and the AC input voltage have a common symmetry axis relationship, and the waveform consistency of the AC input current and the AC input voltage is improved, thereby improving the PF.

**[0027]** The specific implementation of the present disclosure will be described in detail below through several specific embodiments:

### Embodiment 1

**[0028]** In some optional embodiments, the charge-discharge generating circuit may include a first controlled switch tube and a first switch controlling module connected to a control terminal of the first controlled switch tube, the first switch controlling module is configured to control the on-off of the first controlled switch tube.

**[0029]** In some optional embodiments, the drive circuit may further include a unidirectional current path connected in parallel with the charge-discharge generating circuit.

cuit, the unidirectional current path being turned on when the energy storage component is discharged.

**[0030]** In the Embodiment 1 of the present disclosure, the unidirectional current path may include a body diode of the first controlled switch tube.

**[0031]** As a specific embodiment of the present disclosure, the energy storage component may be a capacitor C1, and the first controlled switch tube of the charge-discharge generating circuit may be an NMOS transistor M1. Referring to FIG. 4, the AC input power supply is connected to the rectifier module, the rectifier module is connected to the capacitor C1, the capacitor C1 is connected to the lin terminal of the charge-discharge generating circuit, and the lout terminal of the charge-discharge generating circuit is grounded. The NMOS transistor M1 in the charge-discharge generating circuit may be a non-isolated MOS transistor, wherein the DRAIN of the NMOS transistor M1 is connected to the lin terminal, the SOURCE is connected to the lout terminal, the GATE is connected to the first switch controlling module, and the substrate SUB is connected to the lout terminal. The LED load is connected with the load current control circuit to form a current loop with the rectifier module. In the drive circuit, when the rectified line voltage  $V_{in}$  is higher than the voltage across the capacitor C1, the first switch controlling module controls the NMOS transistor M1 to conduct, generating a current from the lin terminal to the lout terminal, and the rectifier module, the capacitor C1 and the NMOS transistor M1 constitutes a charging loop, in which case the line voltage  $V_{in}$  supplies power to the LED load and capacitor C1; when the rectified busbar voltage  $V_{in}$  is lower than the voltage across the capacitor C1, the first switch controlling module controls the NMOS transistor M1 to cutoff. Since the substrate SUB terminal of the non-isolated NOMS transistor is connected to the lout terminal, the body diode D1' in the NMOS transistor M1 may generate a current from the lout terminal to the lin terminal, and the capacitor C1, the LED load, the load current control circuit and the body diode D1 of NMOS transistor M1 form a discharging loop, in which case the capacitor C1 supplies power to the LED load.

**[0032]** In a specific embodiment, the load current control circuit may include a power control module and a load-controlled switch tube, the power control module may be an operational amplifier, and the load-controlled switch tube may be an NMOS transistor M0, wherein, the DRAIN of the NMOS transistor M0 is connected to the controlled load, the output terminal of the operational amplifier is connected to the GATE of the NMOS transistor M0, the SOURCE of the NMOS transistor M0 is connected to the resistor  $R_{cs}$  and the negative input terminal of the operational amplifier. The forward input terminal of the operational amplifier is connected to the second reference voltage.

**[0033]** It should be noted that, in the embodiment of the present disclosure, for the specific implementation of the load current control circuit, reference may be made to other structures for realizing the controlled load current

control in the prior art. Its specific circuit implementation manner is not strictly limited here in the embodiment of the present disclosure, as long as the requirements of current control in the circuit can be realized, and in the embodiment of the present disclosure, no further description will be given.

**[0034]** In the afore-mentioned embodiments provided by the embodiments of the present disclosure, the body diode D1' of the NMOS transistor M1 generated by the integrated circuit process is configured to realize the unidirectional conduction of the circuit when the capacitor C1 is discharged and no external circuit devices are required, thereby reducing the circuit cost. While reducing the cost of the circuit, it is beneficial to reduce the size of the drive circuit, and facilitates the rational arrangement of each device in the drive circuit during production.

## Embodiment 2

**[0035]** In a specific embodiment, as shown in FIG. 5, the drive circuit further includes a unidirectional current path connected in parallel with the charge-discharge generating circuit, and the unidirectional current path is turned on when the energy storage component is discharged.

**[0036]** As a specific embodiment of the present disclosure, the charge-discharge generating circuit may include a first controlled switch tube and a first switch controlling module connected to a control terminal of the first controlled switch tube, the first switch controlling module is configured to control the on-off of the first controlled switch tube. Specifically, the energy storage component may be a capacitor C1, and the first controlled switch tube of the charge-discharge generating circuit may be an NMOS transistor M1. In the Embodiment 2 of the present disclosure, the unidirectional current path may include at least one diode D1. The first switch controlling module can realize the change of the current generated by the charge-discharge generating circuit by controlling the first controlled switch tube M1.

**[0037]** Referring to FIG. 6, the AC input power supply is connected to the rectifier module, the rectifier module is connected to the capacitor C1, the capacitor C1 is connected to the lin terminal of the charge-discharge generating circuit, and the lout terminal of the charge-discharge generating circuit is grounded. The NMOS transistor M1 in the charge-discharge generating circuit may be a non-isolated MOS transistor, wherein the DRAIN of the NMOS transistor M1 is connected to the lin terminal, the SOURCE is connected to the lout terminal, the GATE is connected to the first switch controlling module, and the diode D1 is connected in parallel between the DRAIN and SOURCE of the NMOS transistor M1. After the LED load is connected to the load current control circuit, it forms a current loop with the rectifier module. In the drive circuit, when the rectified line voltage  $V_{in}$  is higher than the voltage across the capacitor C1, the first switch controlling module may control the NMOS transistor M1 to

conduct, generating a current from the lin terminal to the lout terminal, and the rectifier module, the capacitor C1 and the NMOS transistor M1 constitutes a charging loop, in which case the line voltage Vin supplies power to the LED load and capacitor C1; when the rectified busbar voltage Vin is lower than the voltage across the capacitor C1, the first switch controlling module controls the NMOS transistor M1 to cutoff, generating a current from the lout terminal to the lin terminal in the diode D1, and the capacitor C1, the LED load, the load current control circuit and the diode D1 form a discharging loop, in which case the capacitor C1 supplies power to the LED load.

**[0038]** It should be noted that, in the drive circuit shown in FIG. 6, the first controlled switch tube may be an NMOS tube, which is only a specific implementation of the embodiment of the present disclosure, and the first controlled switch tube may also be other current-controlled switch tubes. For example, it may be a bipolar transistor BJT (not shown in the figure), as long as the current can be controlled so as to form a charging loop when the capacitor C1 is charged.

#### Embodiment 3

**[0039]** In some optional embodiments, referring to the drive circuit shown in FIG. 7 to FIG. 10, it may further include at least one first resistor connected to the first controlled switch tube.

**[0040]** In a specific embodiment, as shown in FIG. 7 or FIG. 8, a circuit formed by connecting the at least one first resistor in series with the first controlled switch tube is connected in parallel with the unidirectional current path.

**[0041]** The drive circuit shown in FIG. 7 is based on the drive circuit described in the Embodiment 2, and the first resistor R1 is connected between the NMOS transistor M1 and the lout terminal. When the capacitor C1 needs to be charged, after the NMOS transistor M1 is turned on, a current may be generated from the lin terminal to the lout terminal, and the lout terminal current flows through the first resistor R1, thereby flowing into or out of the power loop. The current regulation may be realized through the first resistor R1, and the current control may be realized when charging the energy storage component.

**[0042]** Similarly, the drive circuit shown in FIG. 8 is based on the drive circuit described in the Embodiment 1, and the first resistor R1 is connected between the NMOS transistor M1 and the lout terminal. So that, current regulation may be realized through the first resistor R1, and the current control may be realized when charging the energy storage component. In the embodiment, the same NMOS transistor M1 as in the Embodiment 1 is configured to achieve the same or similar technical effect. The specific circuit implementation scheme and the specific execution method of FIG. 7 or FIG. 8 have been described in detail in the aforementioned Embodiment 1 and Embodiment 2, and will not be described in

detail here.

**[0043]** In a specific embodiment, as shown in FIG. 9 or FIG. 10, the first controlled switch tube is connected to the at least one first resistor after being connected in parallel with the unidirectional current path. The drive circuit shown in FIG. 9 is based on the drive circuit described in the Embodiment 2, and the first resistor R1 is connected between the lout terminal and the ground terminal. So that, current regulation may be realized through the first resistor R1, and the current control may be realized when charging the energy storage component.

**[0044]** Similarly, the drive circuit shown in FIG. 10 is based on the drive circuit described in the Embodiment 1, and the first resistor R1 is connected between the lout terminal and the ground terminal. So that, current regulation may be realized through the first resistor R1, and the current control may be realized when charging the energy storage component. In the drive circuit, the substrate SUB terminal (not shown in the figure) of the NMOS transistor M1 is connected to the SOURCE, and the diode D1 described in FIG. 9 is replaced by its body diode D1'. Similar to the NMOS transistor M1 in the Embodiment 1, the body diode D1' of the NMOS transistor M1 manufactured by the integrated circuit process is configured to realize the unidirectional conduction of the circuit when the capacitor C1 is discharged and no external circuit device is required, thereby reducing the circuit cost. While reducing the cost of the circuit, it is beneficial to reduce the size of the drive circuit, and facilitates the rational arrangement of each device in the drive circuit during production.

**[0045]** The specific circuit implementation scheme and the specific implementation manner of FIG. 9 or FIG. 10 have been described in detail in the Embodiment 1 and Embodiment 2 above, and will not be described in detail here.

#### Embodiment 4

**[0046]** Based on the drive circuits described in Embodiment 1 to Embodiment 3, in some further embodiments, the first switch controlling module may include a first operational amplifier. A positive input terminal of the first operational amplifier is configured to connect a first reference voltage; a negative input terminal of the first operational amplifier is connected to the current output terminal of the first controlled switch tube; and the output terminal of the first operational amplifier is connected to the control terminal of the first controlled switch tube. When the first controlled switch tube is an NMOS transistor, the current output terminal of the first controlled switch tube is the SOURCE of the NMOS transistor. When the charge-discharge generating circuit is connected in parallel with the unidirectional current path, the first controlled switch tube may also be a bipolar transistor. In this case, the current output terminal of the first controlled switch may refer to the emitter of the bipolar transistor.

**[0047]** The following is a detailed description of a specific embodiment. Referring to the drive circuit shown in FIG. 11, the AC input power supply is connected to the rectifier module, the rectifier module is connected to the LED load, and the LED load is connected to the load current control circuit. The load current control circuit may include a power control module and a load-controlled switch tube, the power control module may be a second operational amplifier, the load-controlled switch tube may be an NMOS transistor M0. The DRAIN of the NMOS transistor M0 is connected to the LED load, the output terminal of the second operational amplifier AMP2 is connected to the GATE of the NMOS transistor M0, the SOURCE of the NMOS transistor M0 is connected to the resistor Rcs and the negative input terminal of the second operational amplifier AMP2, the positive input terminal of the second operational amplifier AMP2 is connected to the second reference voltage VREF2. The capacitor C1 is connected to the rectified line voltage Vin, and the diode D1 is connected in parallel with the charge-discharge generating circuit. The cathode of the diode D1 of the unidirectional current path is connected to the lin terminal of the charge-discharge generating circuit, and is connected to one terminal of the capacitor C1; the anode of the diode is connected to the lout terminal of the charge-discharge generating circuit. The DRAIN of the NMOS transistor M1 of the charge-discharge generating circuit is connected to the lin terminal, the SOURCE of the NMOS transistor M1 is connected to one terminal of the first resistor R1, and is also connected to the negative input terminal of the first operational amplifier AMP1, the other terminal of R1 of the first resistor is connected to lout terminal. The GATE of the NMOS transistor M1 is connected to the output terminal of the first operational amplifier AMP1; the positive input terminal of the first operational amplifier AMP1 is connected to the first reference voltage VREF1.

**[0048]** In the embodiment of the present disclosure, the first reference voltage VREF1 may be a constant value, and the current  $I_{chg} = VREF1/R1$  generated by the charge-discharge generating circuit is a constant value. The second reference voltage VREF2 may also be a constant value, and the load current  $I_{load} = VREF2/Rcs$  is also a constant value. The rectifier module may be a full-bridge rectifier bridge, so the relationship between the absolute value  $|I_{ac}|$  of the current  $I_{ac}$  before the rectification of the AC input current and the rectified input current  $I_{main}$  is:  $|I_{ac}| = I_{main}$ , and  $I_{main} = I_{chg} + I_{load}$ .

**[0049]** Referring to FIG. 11 and FIG. 12,  $V_{C1}$  is the voltage across the capacitor C1,  $V_{D1}$  is the forward voltage of the diode D1,  $V_{ac}$  is the AC input voltage, and  $|V_{ac}|$  is the input voltage after AC rectification. Usually, the voltage of  $V_{C1}$  is much larger than the forward voltage  $V_{D1}$  of the diode. For simplicity of analysis, the influence of  $V_{D1}$  is ignored in the following description. When  $|V_{ac}|$  is greater than  $V_{C1}$ , the current  $I_{chg}$  generated by the charge-discharge generating circuit charges the capacitor C1; When  $|V_{ac}|$  is less than  $V_{C1}$ , the charging process

ends, at this time D1 conducts forward, and capacitor C1 discharges to provide power to the LED load until  $|V_{ac}|$  is greater than  $V_{C1}$  again, and so on. Referring to FIG. 12, T1 indicates that the capacitor C1 is in the charging stage, at this time  $|V_{ac}|$  is greater than  $V_{C1}$ , the capacitor C1 is in the charging state. Since  $I_{chg}$  is a constant current, the voltage  $V_{C1}$  increases linearly, and the change in the voltage  $V_{C1}$  of the capacitor C1 during the charging phase is  $\Delta V_{C1} = (I_{chg} \cdot T1)/C1$ . T2 indicates that the capacitor C1 is in the discharging stage. Since  $I_{load}$  is a constant current, the voltage  $V_{C1}$  decreases linearly, and the change in the voltage  $V_{C1}$  of the capacitor C1 during the discharging phase is  $\Delta V_{C1} = (I_{load} \cdot T2)/C1$ . When the charging and discharging states of the capacitor C1 are stable, the change of the voltage  $V_{C1}$  in the charging state is equal to that in the discharging state, that is, the charge conservation is achieved. At this time:  $(I_{chg} \cdot T1)/C1 = (I_{load} \cdot T2)/C1$ , that is,  $I_{chg} \cdot T1 = I_{load} \cdot T2$ , in other words  $I_{chg} = I_{load} \cdot T2/T1$ . Since the input voltage  $|V_{ac}|$  after AC rectification changes periodically and the cycle is  $T_{vac}$ , if the voltage cycle of the input voltage  $|V_{ac}|$  after rectification is stable, then the charging time T1 and discharging time T2 of the capacitor C1 are also periodic, and the sum of the charging time and the discharging time is equal to the AC input voltage cycle, that is,  $T1 + T2 = T_{vac}$ . From the above analysis, it is not difficult to conclude that according to the load voltage  $V_{LED}$  and the load current  $I_{load}$ ,  $V_{C1} \geq V_{LED}$  can be achieved by setting  $\Delta V_{C1}$ , adjusting the size of the capacitor C1 and the charging current  $I_{chg}$ . It can be seen that the characteristics of the input current  $I_{main}$  after the bridge are: when  $V_{ac}$  is less than  $V_{C1}$ ,  $I_{main}$  is zero, and when  $V_{ac}$  is greater than  $V_{C1}$ ,  $I_{main} = I_{chg} + I_{load}$ . For the controlled load, since  $V_{C1} \geq V_{LED}$ ,  $I_{load}$  is always a constant value, and it is  $VREF2/Rcs$ , especially for the LED load, it ensures that there is no ripple current in the LED load, and no flicker occurs. Since the cycle of charging and discharging of the capacitor is stable, it is not difficult to conclude that in one cycle of the AC input voltage  $V_{ac}$ , the input current  $I_{main}$  after the bridge and the AC input voltage  $V_{ac}$  have a common symmetry axis relationship, that is, the waveforms of the AC input current and the AC input voltage are consistent, and the PF of the AC input power supply is high.

**[0050]** Of course, the afore-mentioned embodiment shown in FIG. 11 is only a specific implementation manner of the embodiment of the present disclosure. In the embodiment of the present disclosure, referring to FIG. 13, the NMOS transistor M1 in the first controlled switch transistor adopts a Non-isolated MOS transistor replaces the diode D1 described in FIG. 11 by its body diode D1'. Alternatively, as shown in FIG. 14, the NMOS transistor M1 in the first controlled switch transistor is an isolated MOS transistor, that is, the substrate SUB terminal of the NOMS transistor is connected to the SOURCE, and the body diode D1' of the NMOS transistor replaces the diode D1 in FIG. 11.

## Embodiment 5

**[0051]** Based on the drive circuit described in the fifth implementation, in some further embodiments, the first reference voltage VREF1 may also be changed with the change of a certain control parameter in the circuit, so that the current generated in the charge-discharge generating circuit changes accordingly.

**[0052]** As a specific embodiment of the present disclosure, on the basis of the drive circuit shown in FIG. 11, referring to FIG. 15, the first reference voltage may be a variable voltage. Specifically, the first switch controlling module may further include: a current source IREF1, a second resistor R2, a third resistor R3, a second controlled switch tube, and a third controlled switch tube. For example, the second controlled switch tube M2 and the third controlled switch tube M3 may be NMOS transistors of the same specification.

**[0053]** After the current source IREF1 is connected in series with the second resistor R2, it is connected in parallel with the charging loop formed by the capacitor C1, the NMOS transistor M1 and the first operational amplifier AMP1; the positive input terminal of the first operational amplifier AMP1 is connected between the current source and the second resistor R2; the DRAIN of the NMOS transistor M3 is connected to the rectified line voltage Vin through the third resistor R3, and the GATES of the NMOS transistor M2 and the NMOS transistor M3 are connected to form a current mirror.

**[0054]** Referring to FIG. 15 and FIG. 16, the current Ichg generated by the charge-discharge generating circuit in the embodiment varies with the line voltage. Specifically, in FIG. 15 and FIG. 16, the current source IREF1 is connected to the second resistor R2, and the aforementioned first reference voltage VREF1 is generated on the second resistor R2. When the AC input voltage Vac is low, the NMOS transistor M3 is not turned on, and the current Icomp flowing through the current mirror is zero. At this time, the first reference voltage VREF1 is  $IREF1 \cdot R2$ , and the current Ichg generated by the charge-discharge generating circuit is  $VREF1/R1$ . When the input voltage |Vac| after AC rectification increases, the NMOS transistors M2 and M3 are turned on, and the current Icomp increases. At this time, the first reference voltage VREF1 is  $(IREF1 - Icomp) \cdot R2$ , and the current Ichg generated by the charge-discharge generating circuit is  $(IREF1 - Icomp) \cdot R2/R1$ . The higher the AC input voltage Vac, the larger the Icomp, and the smaller the first reference voltage VREF1.

**[0055]** Referring to FIG. 16, if the current Ichg generated by the chargingdischarging generating circuit is constant, the AC input voltage changes during the operation of the circuit. For example, when the AC input voltage Vac increases, the charging time of the capacitor C1 increases. According to  $\Delta V_{C1} = (Ichg \cdot T1)/C1$ , as the charging time T1 increases,  $\Delta V_{C1}$  will inevitably increase. When the charge and discharge processes are rebalanced, the difference between  $V_{C1}$  and the load voltage

$V_{LED}$  will increase ( $V_{C1}$  is greater than  $V_{LED}$ ), resulting in power efficiency drops. On the contrary, when the AC input voltage Vac decreases, the charging time of the capacitor C1 decreases. According to  $\Delta V_{C1} = (Ichg \cdot T1)/C1$ , the charging time T1 decreases, so the  $\Delta V_{C1}$  inevitably decrease, and the result is that the difference between  $V_{C1}$  and  $V_{LED}$  is reduced, and even  $V_{C1}$  is smaller than  $V_{LED}$ , resulting in flicker. With the drive circuit shown in FIG. 15, the current Ichg generated by the charge-discharge generating circuit changes with the line voltage. When the AC input voltage Vac increases, the current Ichg generated by the charge-discharge generating circuit decreases, which can make  $V_{C1}$  remains close to the load  $V_{LED}$ , keeping the power supply efficiency at a consistently high level. When the AC input voltage Vac decreases, the current Ichg generated by the charge-discharge generating circuit increases, so that  $V_{C1}$  can always be slightly larger than  $V_{LED}$  to ensure that there is no ripple in the circuit, so as to avoid flicker, keeping the power supply efficiency at a consistently high level.

**[0056]** Of course, the drive circuit shown in FIG. 15 is only a specific embodiment in which the first reference voltage VREF1 changes with the change of the line voltage after rectification in the circuit. In other embodiments, the first reference voltage VREF1 may also change with changes of other control parameters in the circuit. For example, referring to FIG. 17, the DRAIN of the NMOS transistor M3 shown in FIG. 15 is connected to the output terminal of the controlled load through the third resistor R3, and it can be achieved that, when other circuit connections remain unchanged, the first reference voltage VREF1 varies with the difference between the rectified line voltage and the load voltage in the circuit to achieve the same technical effect as the drive circuit shown in FIG. 15.

## Embodiment 6

**[0057]** In one embodiment, the charge-discharge generating circuit in the drive circuit may include at least one fourth resistor and a unidirectional current path connected in parallel with the fourth resistor, and the unidirectional current path includes at least one diode D1. Referring to FIG. 18, the charge-discharge generating circuit includes a fourth resistor R4 and a diode D1, and the diode D1 is connected in parallel with the fourth resistor R4.

**[0058]** As a specific implementation of the embodiment of the present disclosure, the energy storage component may be a capacitor C1. One terminal of the rectifier module is connected to the AC input power supply, the other terminal of the rectifier module is connected to one terminal of the capacitor C1, and the other terminal of the capacitor C1 is connected to the fourth resistor R4 of the charge-discharge generating circuit. Using the characteristic that the AC input voltage is a sine wave, the capacitor C1 can be charged for a specific time. The charge-

discharge generating circuit may automatically stop charging when the voltage across the capacitor C1 reaches a certain value  $V_{ci}$ ; after the charging stops, the capacitor C1 discharges the controlled load through the diode D1, (the controlled load here refers to, for example, the LED load), so as to provide a basically stable voltage for the controlled load. For the LED load, it is ensured that there is no ripple in the circuit, and no flicker occurs. At the same time, the sum of the charging current of the capacitor C1 and the load current and the AC input voltage have a common symmetry axis relationship in a single cycle, so that the PF of the drive circuit is high. In some optional embodiments, the fourth resistor R4 may be a variable resistor.

**[0059]** In the drive circuits in the Embodiment 1 to Embodiment 6 above, the load current control circuit may be a linear control circuit or a switch-type control circuit, for example, referring to the BUCK circuit shown in FIG. 19, the fly-back type circuit shown in FIG. 20, or the BOOST circuit shown in FIG. 21. Since the implementation of the circuit including the other parts of the drive circuit of the switch-type control circuit is similar to that in the afore-mentioned embodiment, the specific implementation may refer to the detailed descriptions in the Embodiment 1 to Embodiment 6. In addition, it should be noted that, in the embodiment of the present disclosure, for the specific implementation of the constant current control module, reference may be made to other structures for realizing the constant current control of the controlled load in the prior art. The specific circuit implementation mode of the embodiment of the present disclosure is not strictly limited here, as long as the requirements of constant current control in the circuit can be achieved, and in this embodiment of the present disclosure, no further details are described.

**[0060]** Based on the same inventive concept, an embodiment of the present disclosure also provides an LED circuit, including an LED load and the drive circuit described in the afore embodiments.

**[0061]** Regarding the LED circuit in the afore-mentioned embodiment, the execution operation of the drive circuit and the specific way of implementing the solution have been described in detail in the afore-mentioned Embodiment 1 to Embodiment 6, and will not be described in detail here.

**[0062]** Based on the same inventive concept, an embodiment of the present disclosure also provides an LED lighting fixture, which includes the afore-mentioned LED circuit.

**[0063]** Regarding the LED lighting fixture in the afore-mentioned embodiments, the execution operations of the drive circuit of the LED circuit and the specific manner of implementing the solution have been described in detail in the afore-mentioned Embodiment 1 to Embodiment 6, and will not be described in detail here. It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit and scope of the invention. Thus,

if these modifications and variations of the present invention fall within the scope of the claims of the present invention and their equivalents, the present invention is also intended to include these modifications and variations.

## Claims

1. A drive circuit, comprising: a load current control circuit and a rectifier module, wherein the drive circuit further comprises: an energy storage component and a charge-discharge generating circuit, wherein:
  - the charge-discharge generating circuit is connected to the energy storage component and the load current control circuit;
  - the energy storage component and the charge-discharge generating circuit are connected to the both ends of the rectifier module;
  - the charge-discharge generating circuit is configured to:
    - form a charging loop with the energy storage component during a charging process of the energy storage component, and control a charging current of the energy storage component; and
    - form a discharging loop with the energy storage component during a discharging process of the energy storage component.
2. The drive circuit of claim 1, wherein the charge-discharge generating circuit comprises a first controlled switch tube and a first switch controlling module connected to a control terminal of the first controlled switch tube, the first switch controlling module is configured to control the on-off of the first controlled switch tube.
3. The drive circuit of claim 2, wherein the drive circuit further comprises a unidirectional current path connected in parallel with the charge-discharge generating circuit, the unidirectional current path being turned on when the energy storage component is discharged.
4. The drive circuit of claim 3, wherein the unidirectional current path comprises a diode, or a body diode of the first controlled switch tube.
5. The drive circuit of claim 2 or 3, wherein the drive circuit further comprises: at least one first resistor connected to the first controlled switch tube.

6. The drive circuit of claim 5, wherein a circuit, formed by connecting the at least one first resistor in series with the first controlled switch tube, is connected in parallel with the unidirectional current path. 5
7. The drive circuit of claim 5, wherein the first controlled switch tube is connected to the at least one first resistor after being connected in parallel with the unidirectional current path. 10
8. The drive circuit of claim 5, wherein the first switch controlling module comprises a first operational amplifier; 15
- a positive input terminal of the first operational amplifier is configured to connect a first reference voltage, a negative input terminal of the first operational amplifier is connected to a current output terminal of the first controlled switch tube; and 20
- an output terminal of the first operational amplifier is connected to the control terminal of the first controlled switch tube.
9. The drive circuit of claim 8, wherein the first controlled switch tube is an NMOS transistor, and the current output terminal of the first controlled switch tube is a SOURCE of the NMOS transistor, or, 25
- when the charge-discharge generating circuit is connected in parallel with the unidirectional current path, the first controlled switch tube is a bipolar transistor, and the current output terminal of the first controlled switch tube is an emitter of the bipolar transistor. 30
10. The drive circuit of claim 8, wherein the first switch controlling module further comprises 35
- a current source, a second resistor, a third resistor, a second controlled switch tube and a third controlled switch tube, wherein 40
- after connected in series with the second resistor, the current source is connected in parallel with the charging loop formed by the energy storage component and the first controlled switch tube; 45
- the positive input terminal of the first operational amplifier is connected between the current source and the second resistor; a DRAIN of the third controlled switch tube is connected to the rectified line voltage through the third resistor, 50
- or the DRAIN of the third controlled switch tube is configured to connect an output terminal of a controlled load through the third resistor; and
- the second controlled switch tube and the third controlled switch tube are connected to form a current mirror. 55
11. The drive circuit of claim 1, wherein the drive circuit further comprises
- a unidirectional current path, the unidirectional current path being turned on when the energy storage component is discharged; and
- the charge-discharge generating circuit comprises at least one fourth resistor, and the unidirectional current path is connected in parallel with the at least one fourth resistor.
12. The drive circuit of claim 8 or 11, wherein the load current control circuit is a linear control circuit, a BUCK circuit, a fly-back circuit or a BOOST circuit.
13. An LED circuit, wherein the LED circuit comprises an LED load and the drive circuit according to any one of claims 1-12.
14. An LED lighting fixture, wherein the LED lighting fixture comprises the LED circuit of claim 13.

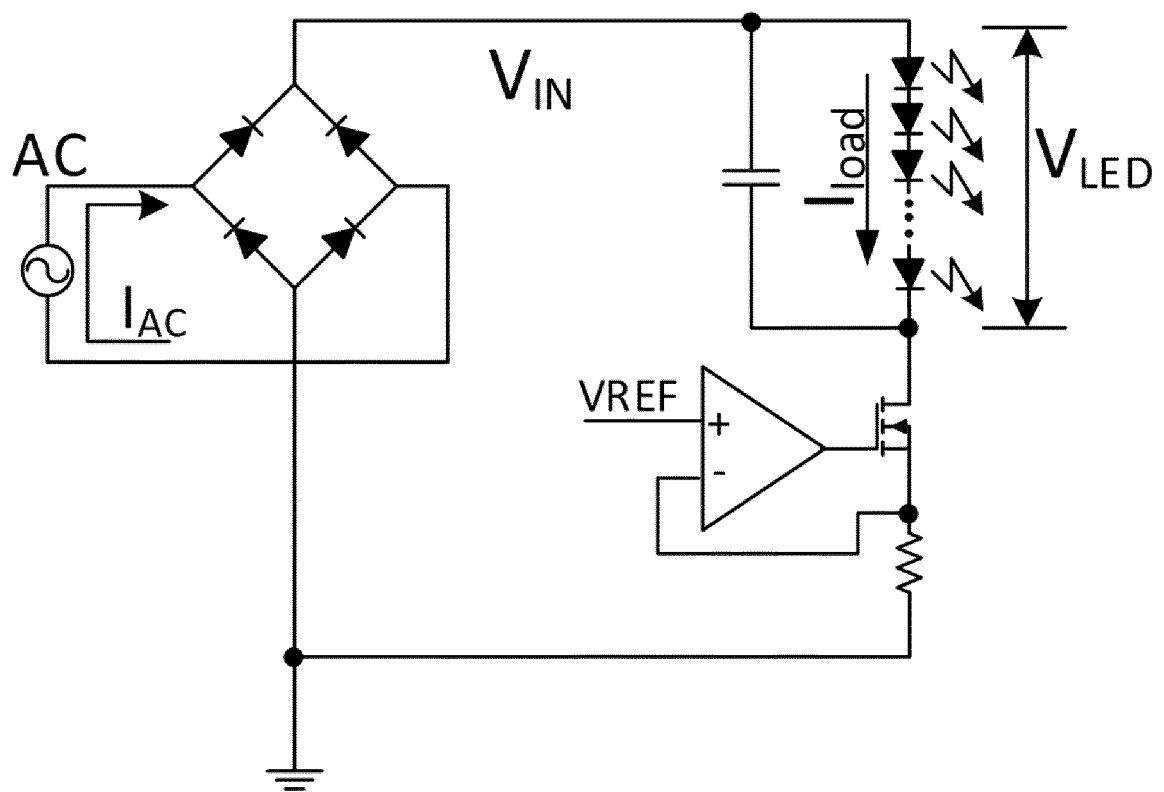


FIG. 1

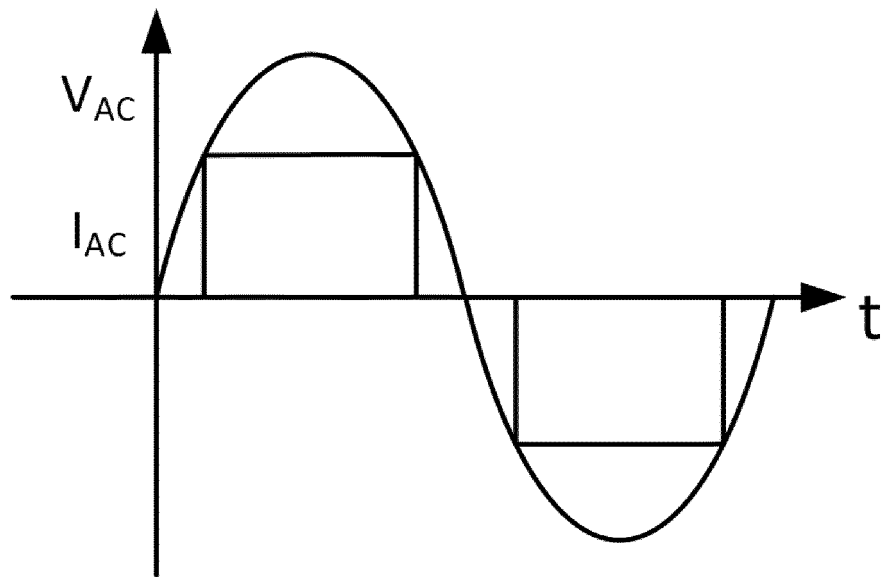


FIG. 2

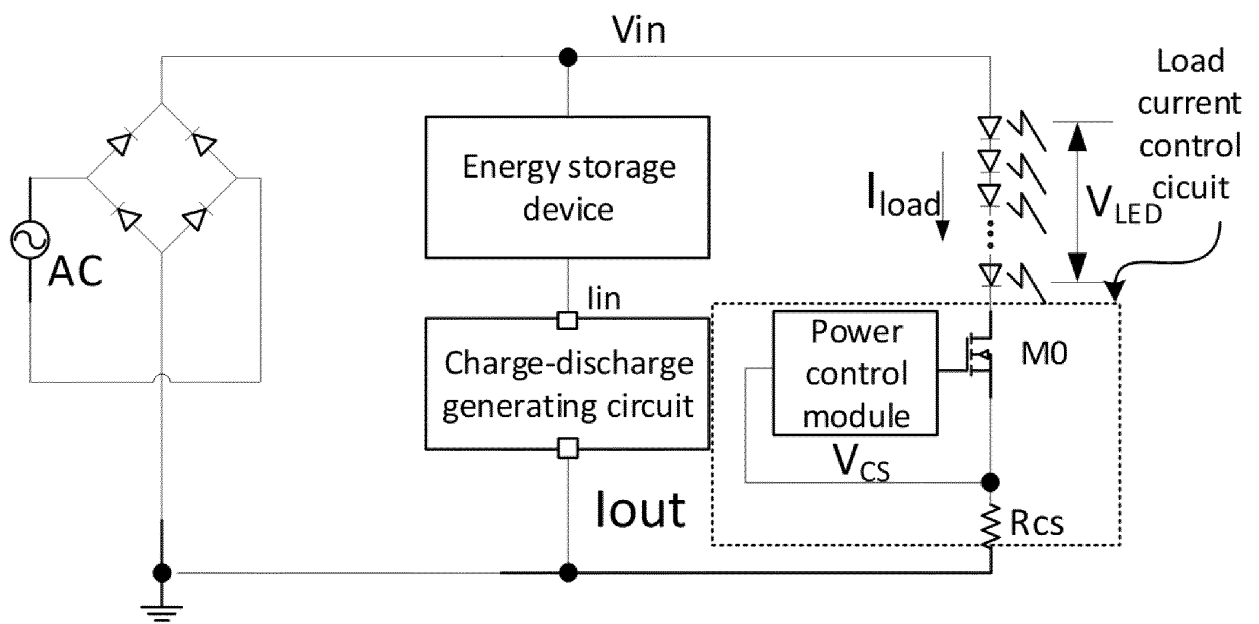


FIG. 3

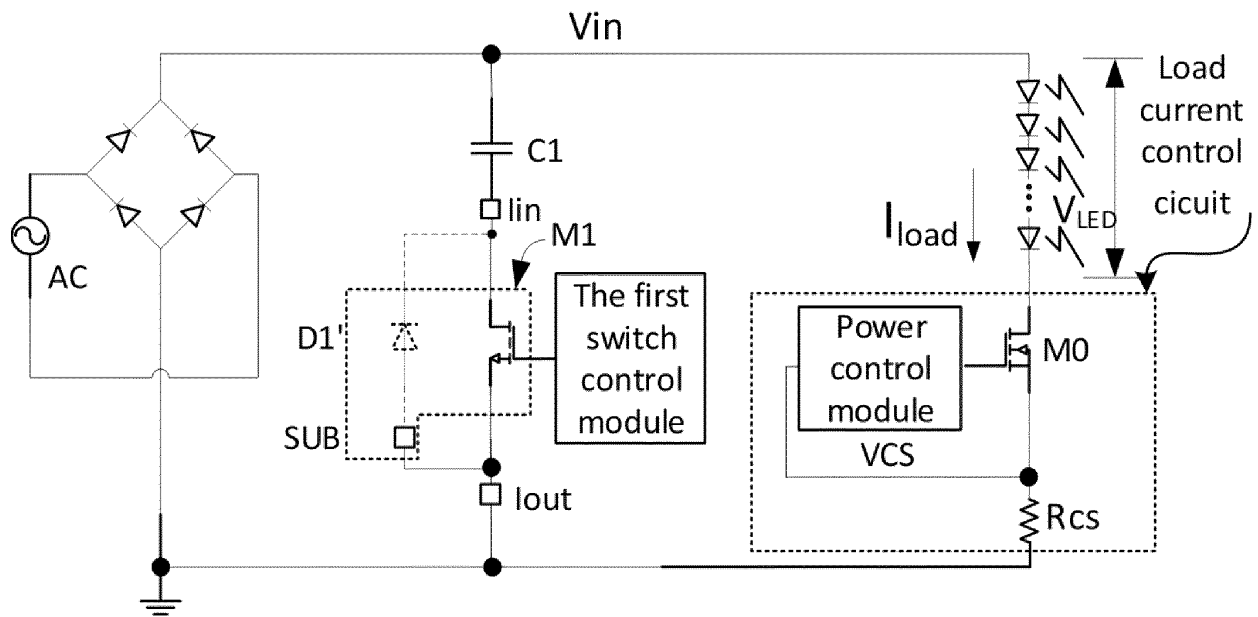


FIG. 4

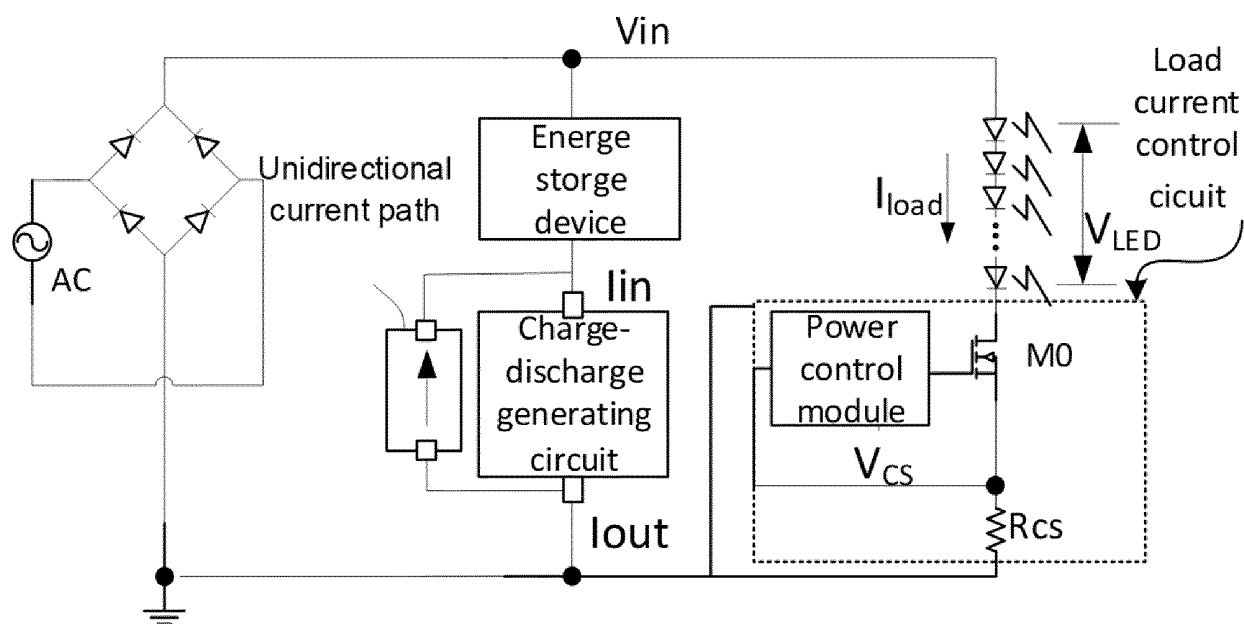


FIG. 5

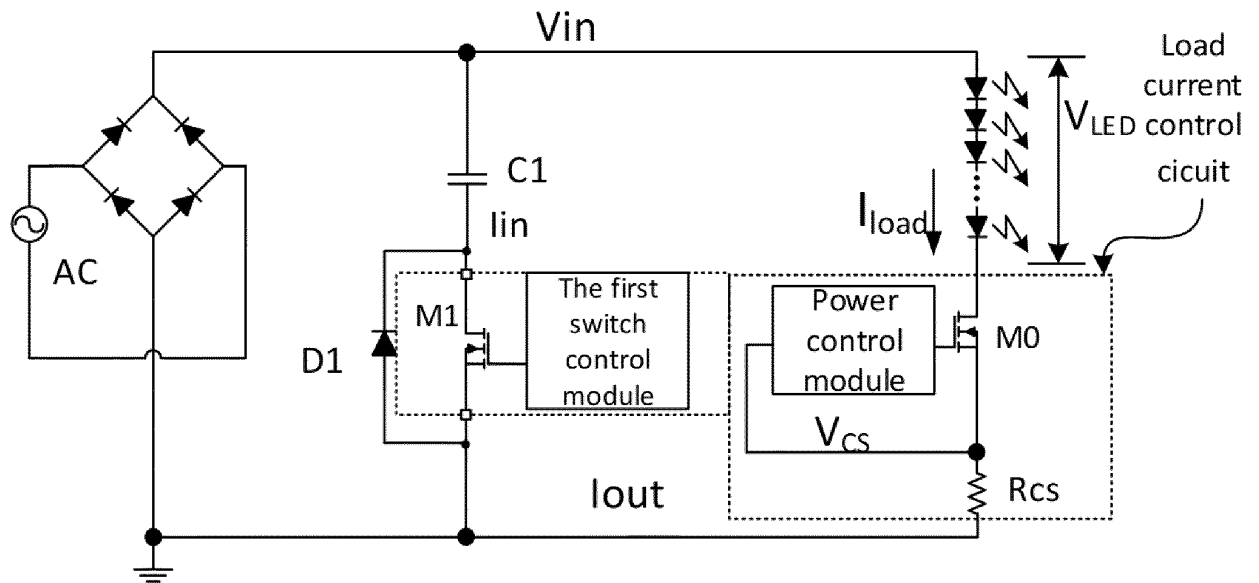


FIG. 6

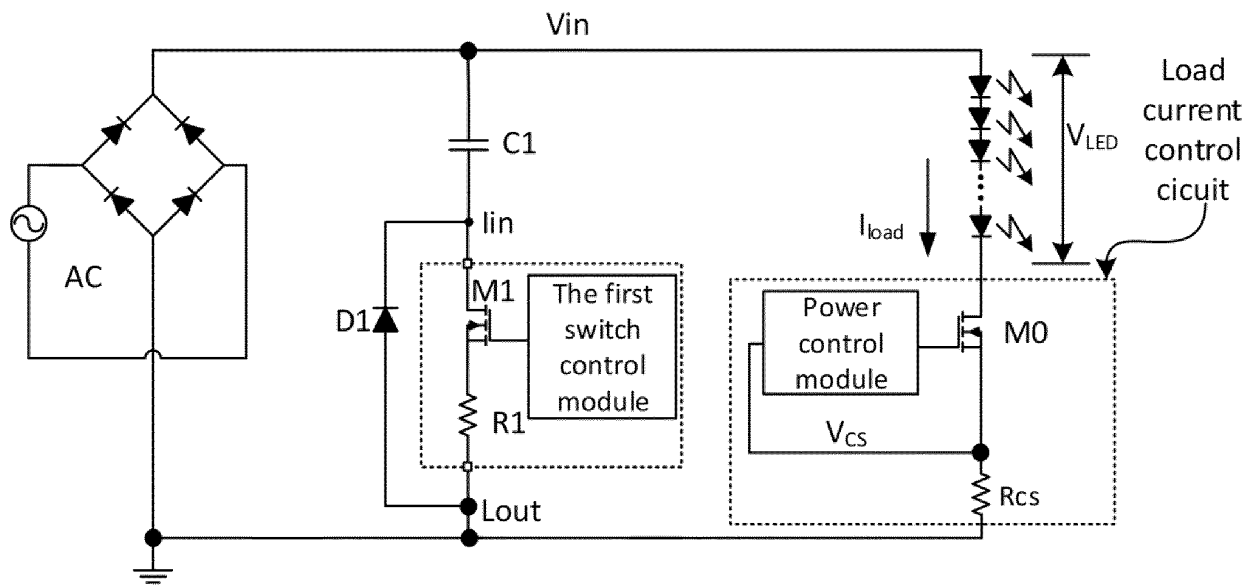


FIG. 7

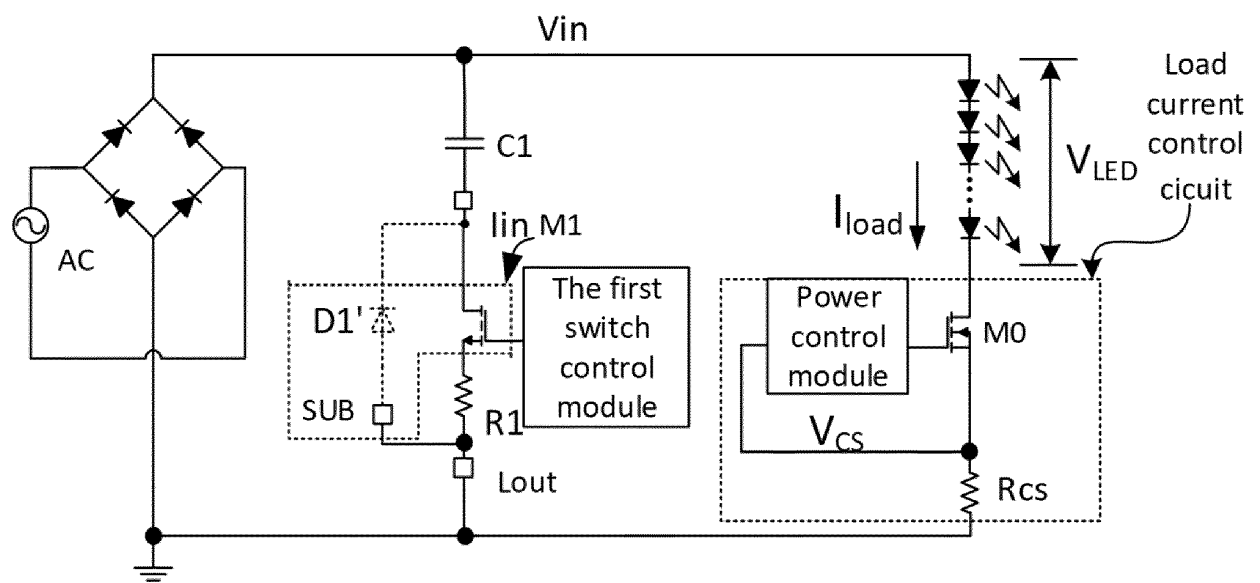


FIG. 8

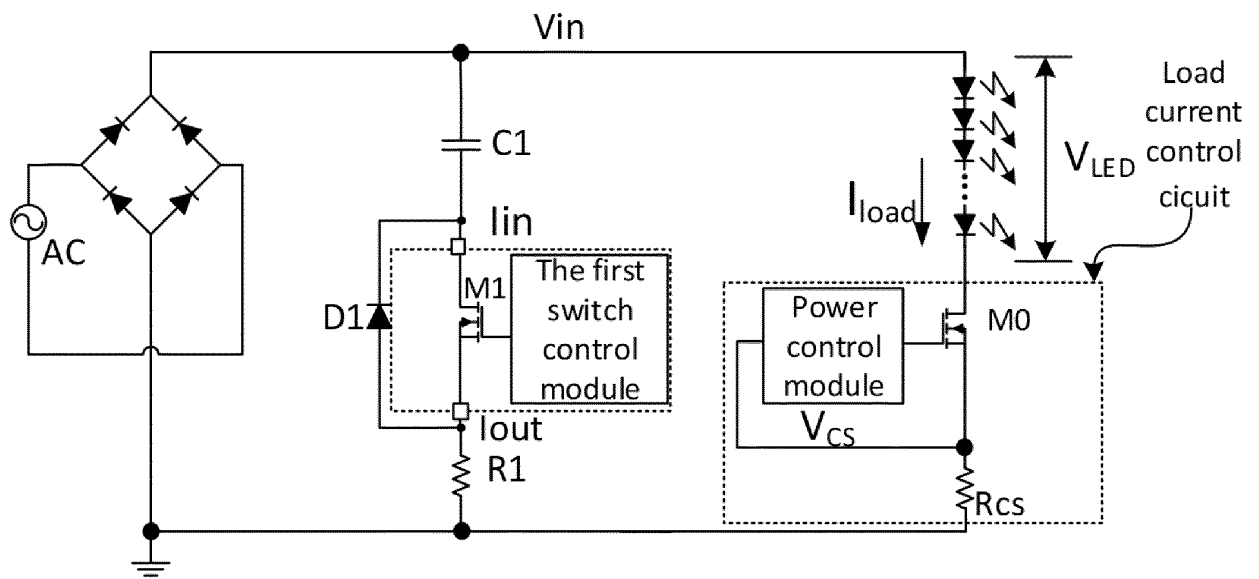


FIG. 9

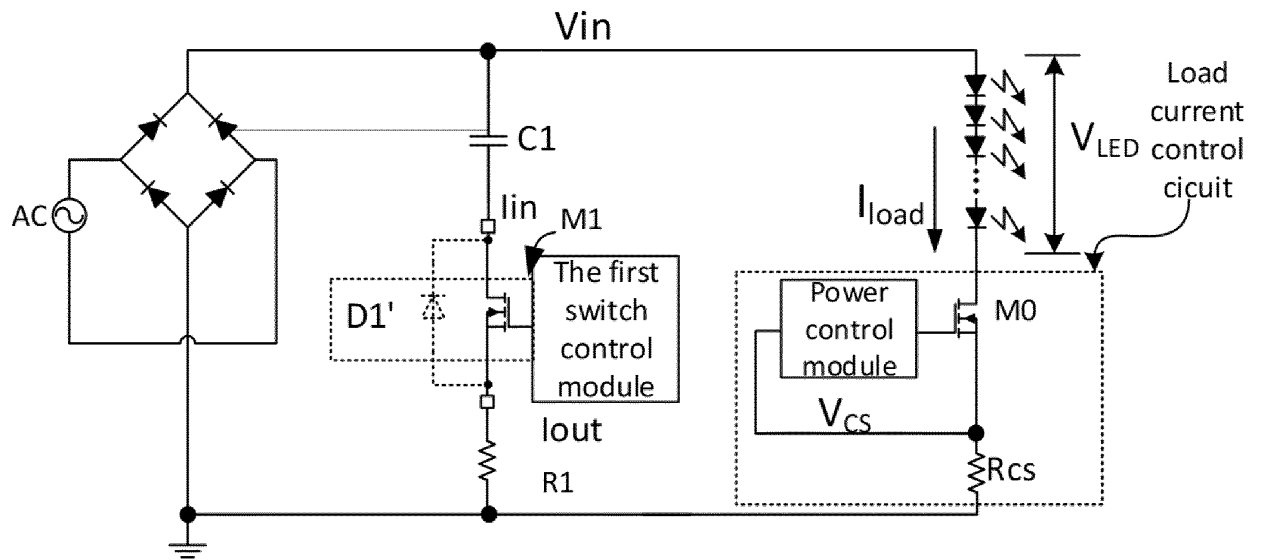


FIG. 10

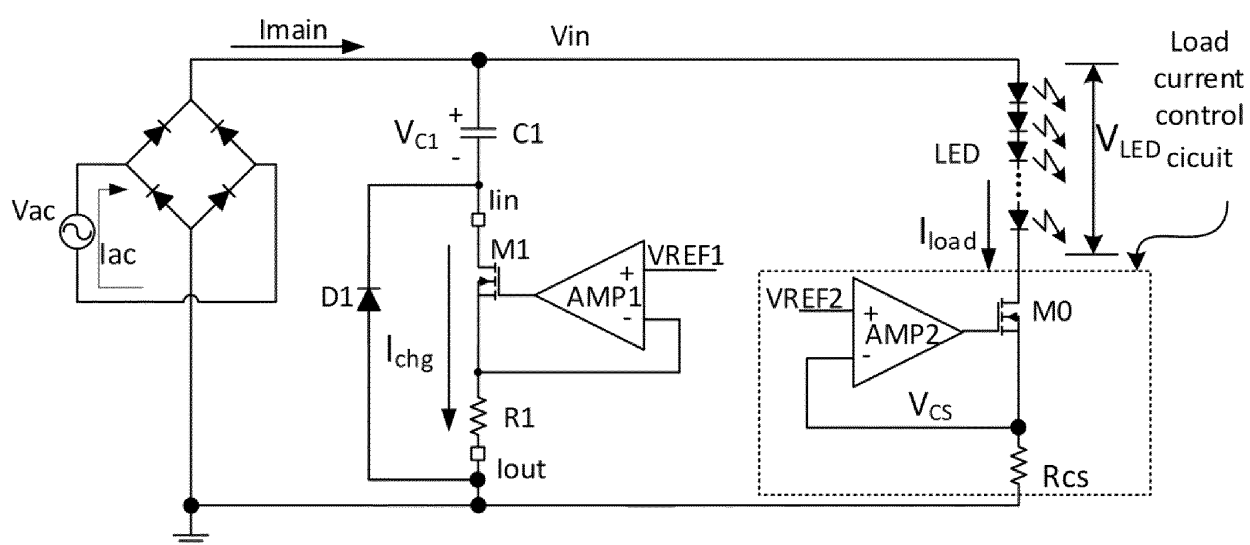


FIG. 11

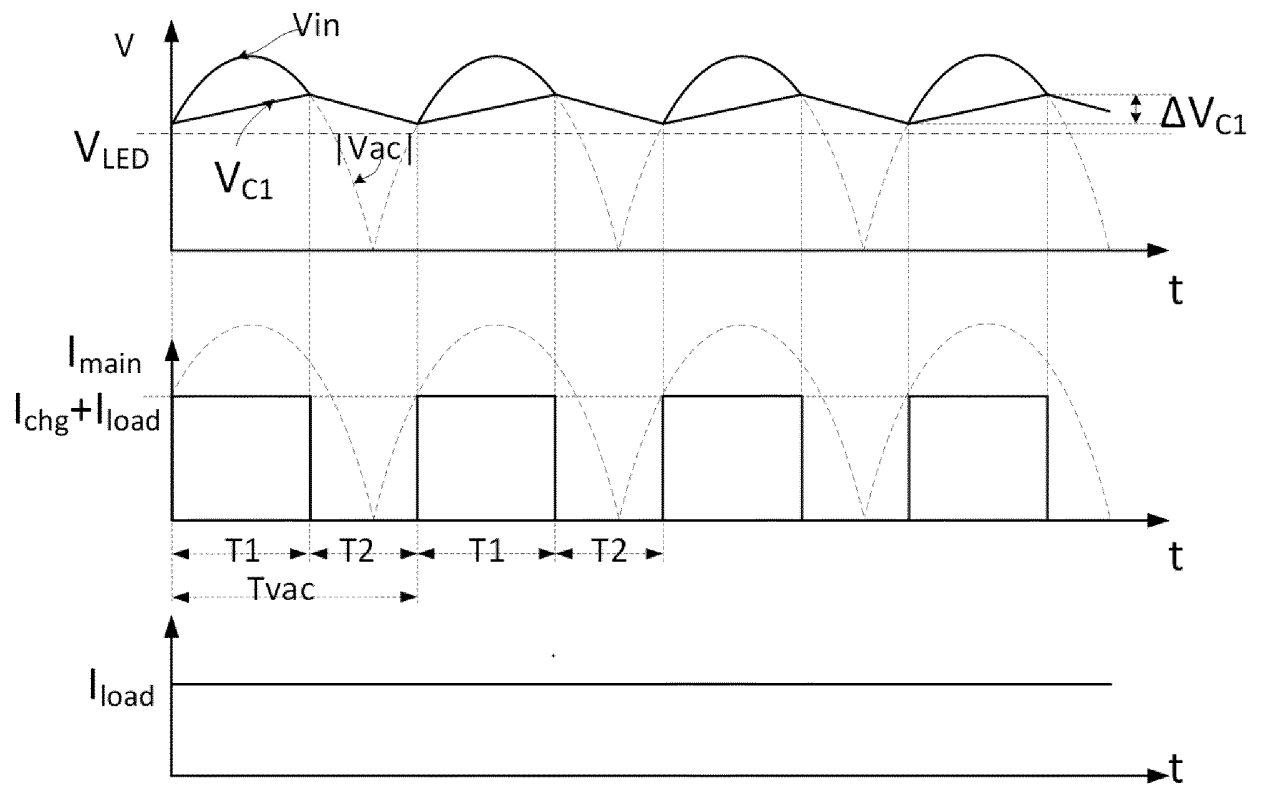


FIG. 12

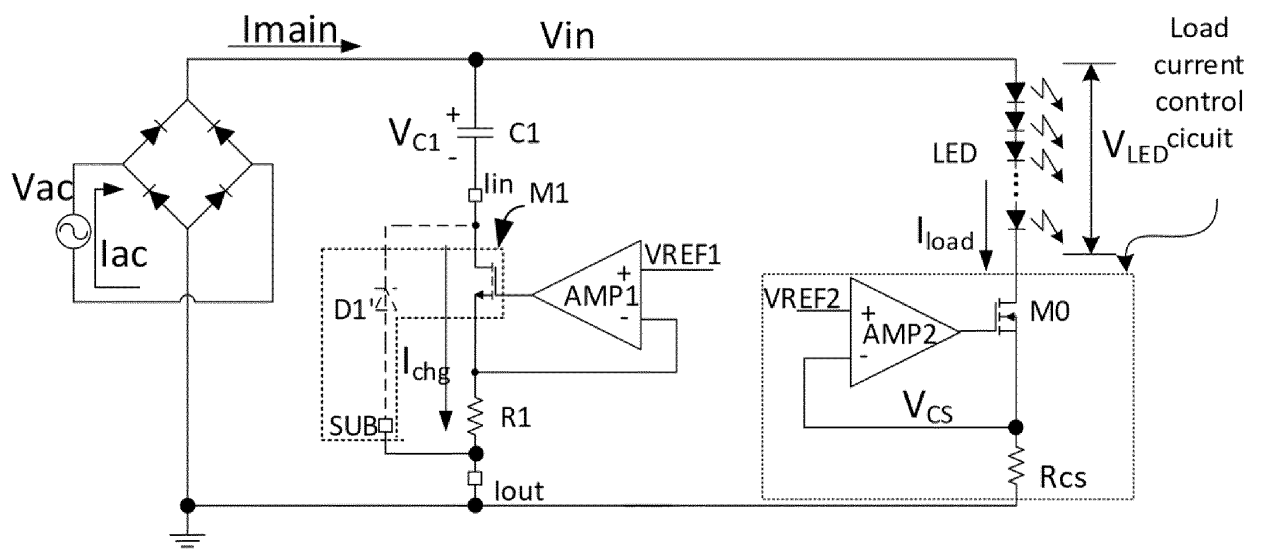


FIG. 13

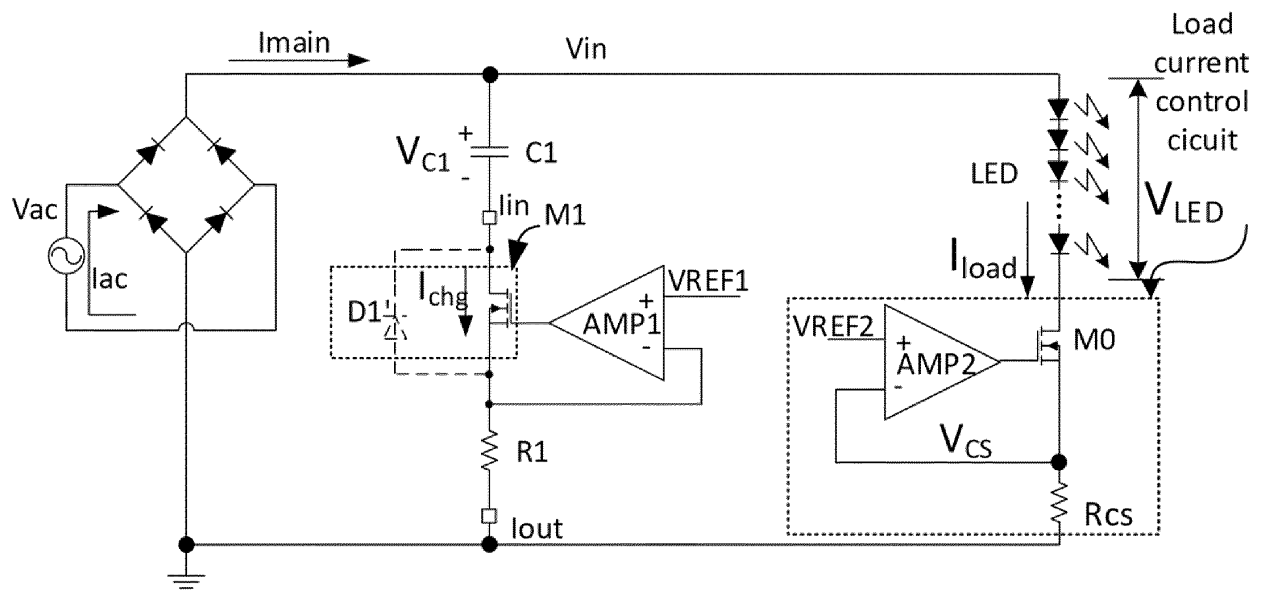


FIG. 14

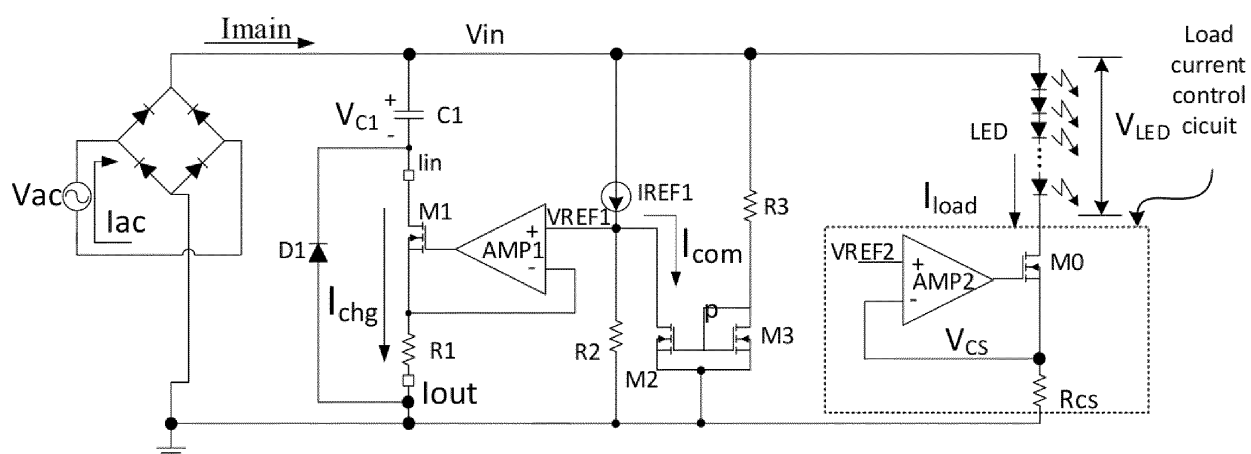


FIG. 15

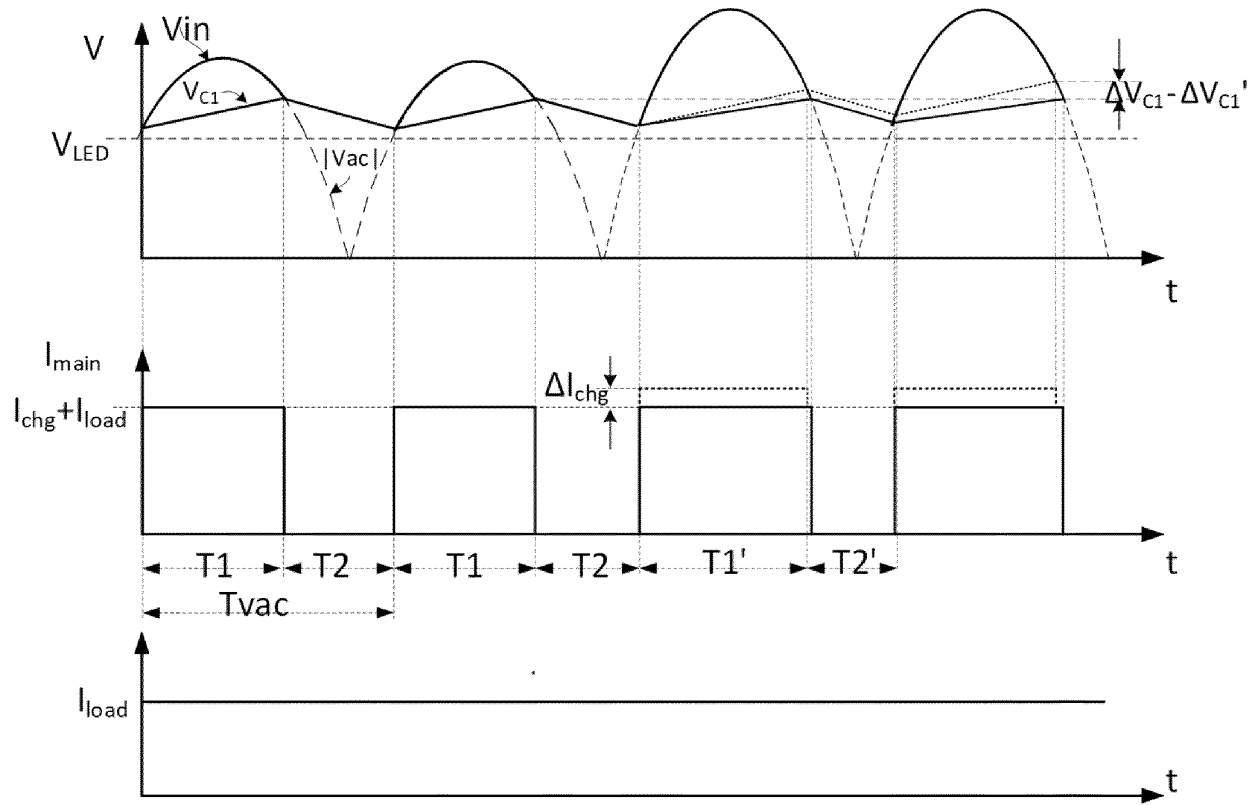


FIG. 16

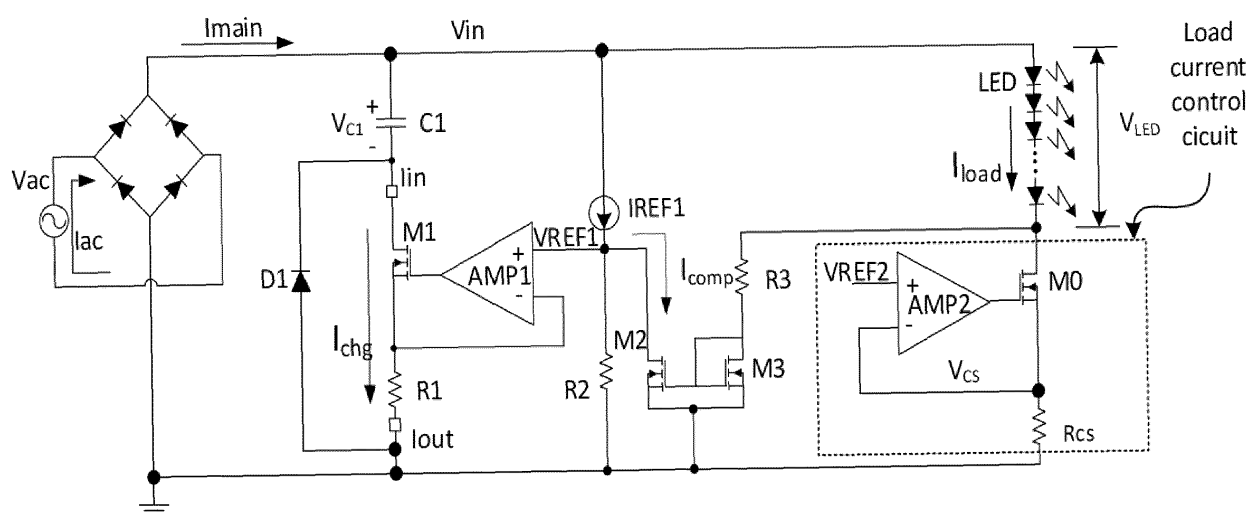


FIG. 17

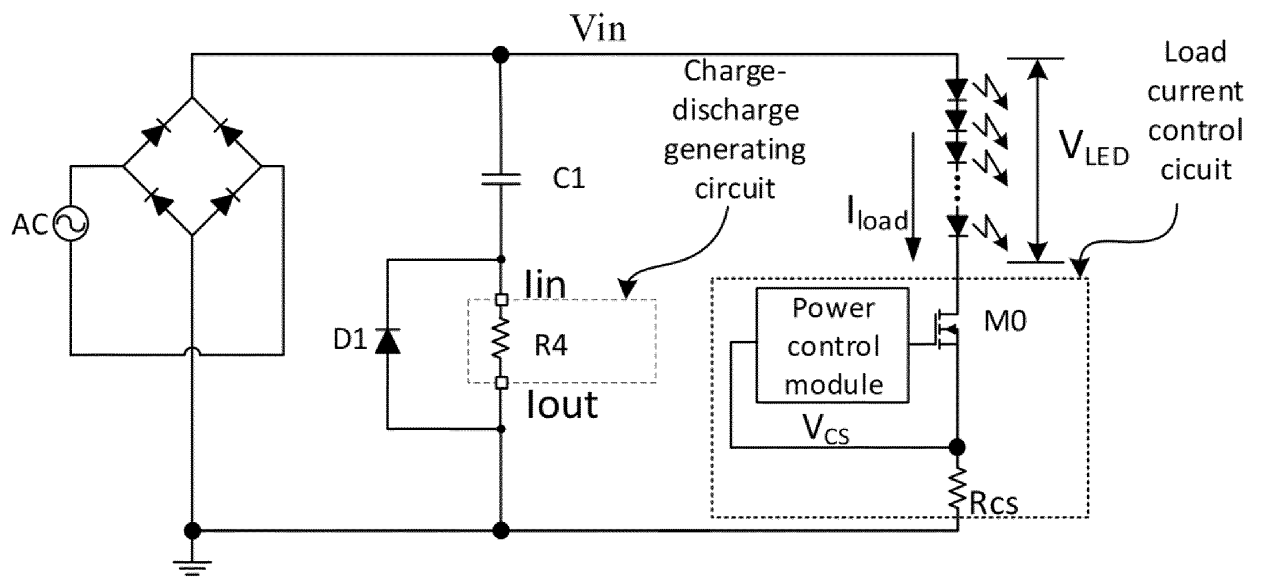


FIG. 18

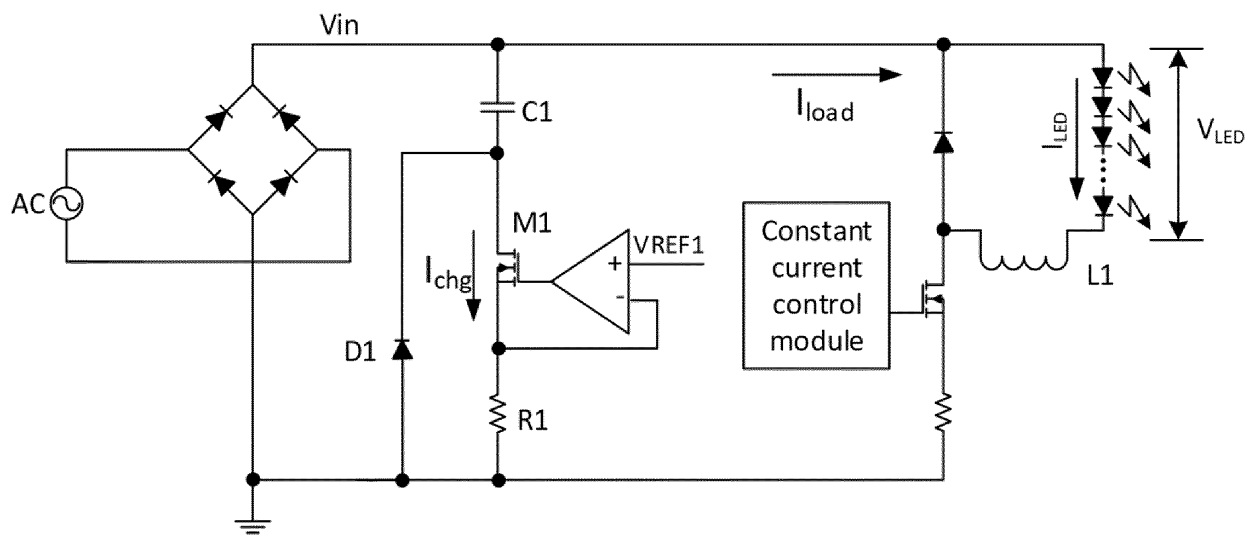


FIG. 19

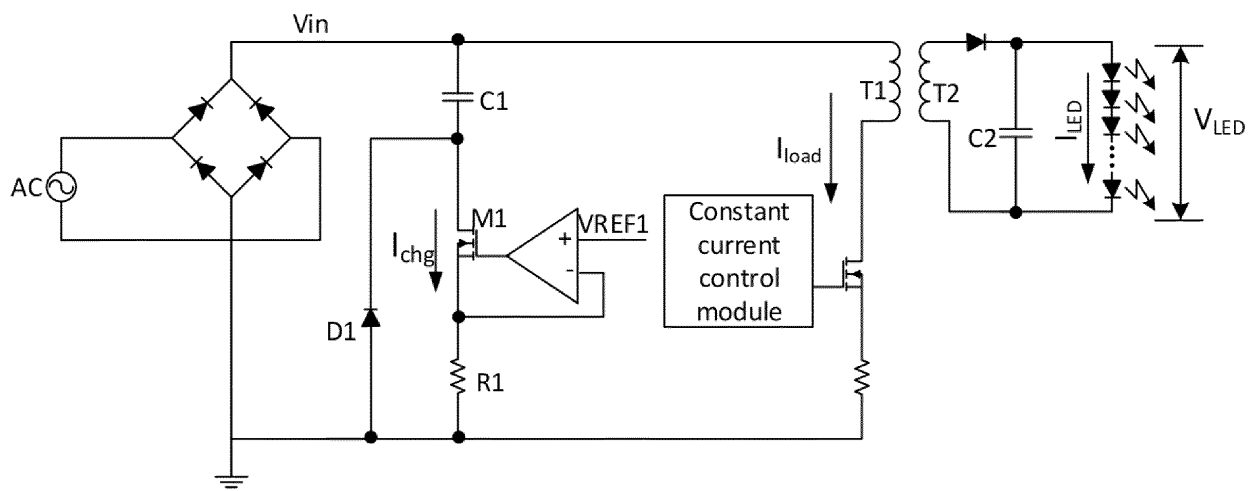


FIG. 20

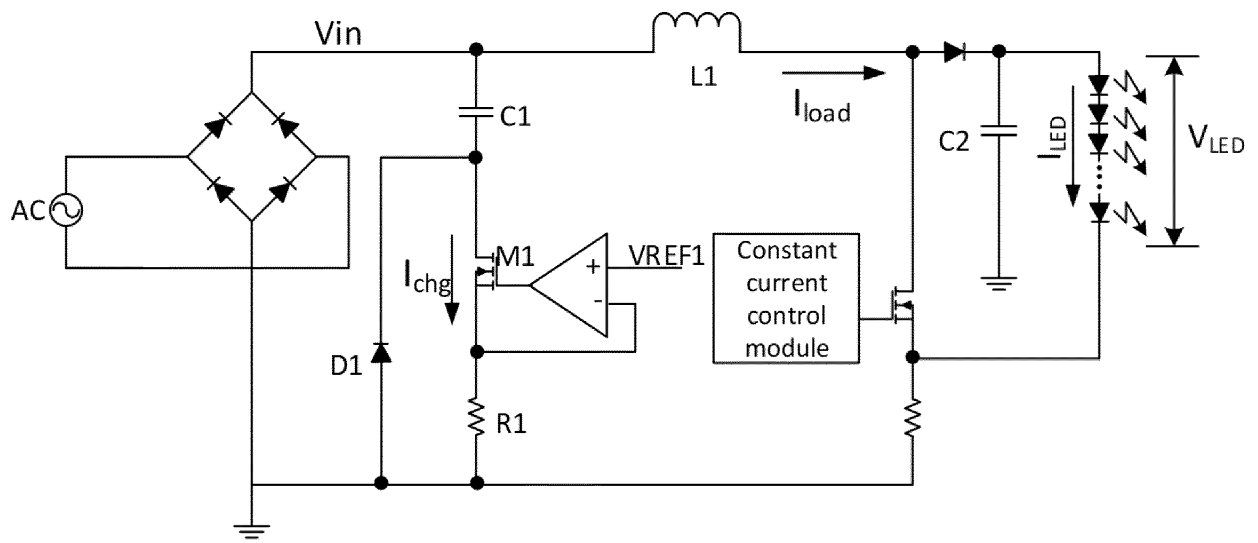


FIG. 21

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2020/082968

## A. CLASSIFICATION OF SUBJECT MATTER

H05B 33/08(2020.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT; CNKI; WPI; EPODOC; IEEE; LED, 功率因子, 功率因数, 频闪, 驱动, 控制, 充电, 放电, 恒流, 储能, 电容, MOS, 波纹, 电流, 母线, power factor, PF, strobe, drive, control, charge, discharge, constant, current, energy storage, capacitor, ripple, bus

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 109348587 A (POWER MICRO-ELECTRONICS CO., LTD.) 15 February 2019 (2019-02-15) description, paragraphs [0024]-[0049], and figures 2-3	1-14
X	CN 202652092 U (OSRAM GMBH) 02 January 2013 (2013-01-02) description paragraphs [0017]-[0032], figures 3, 5	1-14
A	CN 103857138 A (LI, Wenxiong et al.) 11 June 2014 (2014-06-11) entire document	1-14
A	CN 110519881 A (SHENZHEN WINSEMI MICROELECTRONICS CO., LTD.) 29 November 2019 (2019-11-29) entire document	1-14
A	CN 107979899 A (SUZHOU FAYTECH MICROELECTRONIC CO., LTD.) 01 May 2018 (2018-05-01) entire document	1-14
A	US 2013343095 A1 (BCD SEMICONDUCTOR MANUFACTURING CO., LTD.) 26 December 2013 (2013-12-26) entire document	1-14

☐ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

10 September 2020

Date of mailing of the international search report

30 September 2020

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT  
Information on patent family members

International application No.  
**PCT/CN2020/082968**

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)		Publication date (day/month/year)
CN	109348587	A	15 February 2019	None		
CN	202652092	U	02 January 2013	None		
CN	103857138	A	11 June 2014	None		
CN	110519881	A	29 November 2019	None		
CN	107979899	A	01 May 2018	None		
US	2013343095	A1	26 December 2013	CN	102723886	A 10 October 2012