(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 053 918 A8**

(12) **CORRECTED EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(15) Correction information:
Corrected version no 1 (W1 A1)
Corrections, see
Bibliography INID code(s) 71

(48) Corrigendum issued on:
21.12.2022 Bulletin 2022/51

(43) Date of publication:
07.09.2022 Bulletin 2022/36

(21) Application number: **21755884.0**

(22) Date of filing: **21.05.2021**

(51) International Patent Classification (IPC):
H01L 31/0216 *(2014.01)* ***H01L 31/18*** *(2006.01)*

(52) Cooperative Patent Classification (CPC):
H01L 31/02167; H01L 31/02168; H01L 31/068;
Y02E 10/50; Y02E 10/547; Y02P 70/50

(86) International application number:
PCT/CN2021/095128

(87) International publication number:
WO 2022/156102 (28.07.2022 Gazette 2022/30)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(30) Priority: **19.01.2021 CN 202110065969**
14.04.2021 CN 202110396614

(71) Applicant: **Trina Solar Co., Ltd**
Changzhou, Jiangsu 213031 (CN)

(72) Inventors:
- **ZHANG, Xueling**
  Changzhou, Jiangsu 213031 (CN)
- **LIU, Wei**
  Changzhou, Jiangsu 213031 (CN)
- **CHEN, Hong**
  Changzhou, Jiangsu 213031 (CN)
- **JIAN, Lei**
  Changzhou, Jiangsu 213031 (CN)
- **CHEN, Yifeng**
  Changzhou, Jiangsu 213031 (CN)

(74) Representative: **Cabinet Beaumont**
4, Place Robert Schuman
B.P. 1529
38025 Grenoble Cedex 1 (FR)

(54) **SOLAR CELL STACK PASSIVATION STRUCTURE AND PREPARATION METHOD THEREFOR**

(57) A laminated passivation structure of solar cell and a preparation method thereof are disclosed herein. The laminated passivation structure of solar cell comprises a P-type silicon substrate, and a first dielectric layer, a second dielectric layer, and a third dielectric layer sequentially arranged on the back side of the P-type silicon substrate from inside to outside. The preparation method comprises: generating a first dielectric layer on the back surface of the P-type silicon substrate, and then sequentially depositing a second dielectric layer and a third dielectric layer on the first dielectric layer.

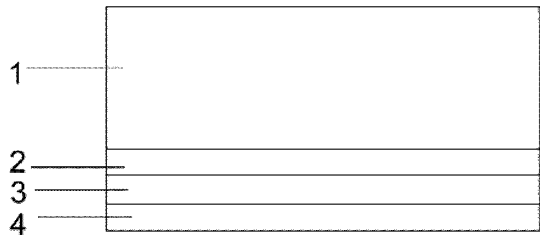

Fig. 3

EP 4 053 918 A8