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(54) ELECTRONIC COMPONENT, CIRCUIT BOARD HAVING SAME, AND ELECTRONIC DEVICE

(57) An electronic element (22), a circuit board (21) with an electronic element (22), and an electronic device are provided, and relate to the field of electronic device technologies, to shorten a heat dissipation path of the electronic element (22), improve heat dissipation efficiency of the electronic element (22), and ensure input/output impedance matching performance of the electronic element (22). The electronic element (22) includes a substrate (221) and a first input pad (222), at least one chip (223), and a first output pad (224) that are disposed on a first surface (221a) of the substrate(221), where the first input pad (222), the at least one chip (223), and the first output pad (224) are sequentially connected, the first input pad (222) and the first output pad (224) are directly disposed on the first surface (221a) of the substrate (221), and a surface of the first input pad (222) facing away from the substrate (221) and a surface of the first output pad (224) facing away from the substrate (221) constitute a partial area of an outer surface of the electronic element (22). The electronic element (22) is used as a power amplifier.

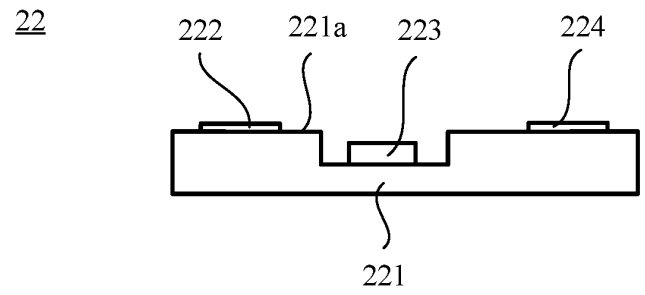

FIG. 7

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Description

TECHNICAL FIELD

[0001] This application relates to the field of electronic device technologies, and in particular, to an electronic element, a circuit board with an electronic element, and an electronic device.

BACKGROUND

[0002] In electronic devices such as a wireless base station, heat dissipation needs to be performed on a circuit board with a high integrated high-density arrangement of electronic elements on the circuit board. In addition, to integrate more electronic elements on the circuit board, the electronic elements tend to be modular.

[0003] For example, FIG. 1 is a modular electronic element 01 in the conventional technology. As shown in FIG. 1, the electronic element 01 includes a substrate 011, a chip 012, an input pad 013, an output pad 014, and a plastic packaging layer 015. The substrate 011 includes a first surface 011a and a second surface 011b that are opposite to each other. The chip 012 is disposed on the first surface 011a, the input pad 013 and the output pad 014 are disposed on the second surface 011b. An input terminal of the chip 012 is connected to the input pad 013 through a first metalized through hole 016, and an output terminal of the chip 012 is connected to the output pad 014 through a second metalized through hole 017. The plastic packaging layer 015 is disposed on the first surface 011a of the substrate 011, and wraps the chip 012.

[0004] The electronic element 01 shown in FIG. 1 is usually surface-mounted on a circuit board. FIG. 2 is a schematic diagram of a structure of the electronic element 01 surface-mounted on a circuit board 02. Refer to FIG. 2. The substrate 011 of the electronic element 01 is attached to the circuit board 02. The input pad and the output pad of the electronic element 01 are respectively welded to an output pad and an input pad of the circuit board 02. A surface of the circuit board 02 facing away from the electronic element 01 is attached to a radiator 03 by using a colloid heat conducting material. In this way, heat generated by the chip 012 in the electronic element 01 is transferred to the radiator 03 after sequentially passing through the substrate 011 and the circuit board 02, to cool the electronic element 01. This cooling path is long, and heat dissipation efficiency is low. To improve heat dissipation efficiency of an electronic element, in some conventional technologies, the electronic element 01 is attached to a surface of a circuit board facing a radiator in a flip-mounted manner. FIG. 3 is a schematic diagram of a structure of the electronic element 01 attached to the surface of the circuit board 02 facing the radiator 03 in a flip-mounted manner. Refer to FIG. 3. The substrate 011 of the electronic element 01 is directly attached to the radiator 03, and a heat dissipation path of the electronic element 01 is short, and heat dissipation efficiency is high. When the electronic element 01 is flip-mounted, an electrical connection structure needs to be disposed in the electronic element 01, to lead out the input terminal and the output terminal of the chip 012, to implement electrical connection to the circuit board 02. In some existing solutions, as shown in FIG. 3, the input pad 013 and the output pad 014 of the electronic element 01 are disposed on the first surface 011a of the substrate 011. The input terminal of the chip 012 is connected to the input pad 013, and the output terminal of the chip 012 is connected to the output pad 014. The input pad 013 and the output pad 014 each are welded with a copper pillar A, and the copper pillar A is encapsulated in the encapsulation layer 015. A surface of one terminal of the copper pillar A facing away from the substrate 011 is not covered by the encapsulation layer 015. The electronic element 01 is welded to the input pad and the output pad of the circuit board 02 through surfaces of two copper pillars A facing away from the substrate 011. To implement good impedance matching of the electronic element 01, processing accuracy and assembling accuracy of the copper pillar A are required to be high. However, because a size of the electronic element 01 is small, a diameter and a length of the copper pillar A that can be installed in the electronic element 01 are short, resulting in large processing difficulty, low accuracy, and low assembling accuracy of the copper pillar A on the substrate 011. This easily affects input/output impedance matching performance of the electronic element 01. In some other existing solutions, as shown in FIG. 4, a printed circuit board B with a metalized through hole is used to replace the copper pillar A in a solution shown in FIG. 3. The input pad 013 and the output pad 014 are respectively connected to the input pad and the output pad of the circuit board 2 through two metalized through holes on the printed circuit board B. Supported by the printed circuit board B, dimensional accuracy of the metalized through hole may be high, so that an influence on input/output impedance matching performance of the electronic element 01 can be reduced to some extent. However, in a process of processing and assembling of the printed circuit board B with a metalized through hole, there may be an unavoidable error, and the input/output impedance matching performance of the electronic element 01 is still affected.

SUMMARY

[0005] Embodiments of this application provide an electronic element, a circuit board with an electronic element, and an electronic device, to shorten a heat dissipation path of the electronic element, improve heat dissipation efficiency of the electronic element, and ensure input/output impedance matching performance of the electronic element.

[0006] To achieve the foregoing objectives, the following technical solutions are used in embodiments of this

application.

[0007] According to a first aspect, some embodiments of this application provide an electronic element, including a substrate, and a first input pad, at least one chip, and a first output pad that are disposed on a first surface of the substrate. The chip includes but is not limited to a power amplifier chip. The first input pad, the at least one chip, and the first output pad are sequentially connected. The first input pad and the first output pad are directly disposed on the first surface of the substrate. A surface of the first input pad facing away from the substrate and a surface of the first output pad facing away from the substrate constitute a partial area of an outer surface of the electronic element.

[0008] Compared with that in a conventional technology, when the electronic element provided in this embodiment of this application is flip-mounted on a circuit board and attached to a radiator, heat generated by the at least one chip in the electronic element during operation may be directly transferred to the radiator through the substrate. Therefore, the circuit board with the electronic element has a short heat dissipation path and high heat dissipation efficiency. In addition, the first input pad and the first output pad are directly disposed on the first surface of the substrate, and the surface of the first input pad facing away from the substrate and the surface of the first output pad facing away from the substrate constitute a partial area of the outer surface of the electronic element. Therefore, the surface of the first input pad facing away from the substrate and the surface of the first output pad facing away from the substrate are disposed to be exposed. That is, the surface of the first input pad facing away from the substrate and the surface of the first output pad facing away from the substrate are not covered. The first input pad and the first output pad may be directly welded to an output pad and an input pad that are on the circuit board. There is no intermediate connection structure between the first input pad and the output pad on the circuit board and between the first output pad and the input pad on the circuit board. A lead-out path of each of an input terminal and an output terminal of the chip in the electronic element is short, and accuracy of the lead-out line is high. Therefore, input/output impedance matching performance of the electronic element can be effectively ensured.

[0009] Optionally, the substrate includes a heat dissipation layer and a dielectric layer that are stacked. At least one accommodate groove is disposed on the dielectric layer, and the accommodate groove penetrates the dielectric layer. An area that is on a surface of the heat dissipation layer and that is opposite to the accommodate groove, a side of the accommodate groove, and a surface of the dielectric layer facing away from the heat dissipation layer constitute the first surface of the substrate. The at least one chip is disposed in the at least one accommodate groove and is fastened in the area that is on the surface of the heat dissipation layer and that is opposite to the accommodate groove. The first input pad and the first output pad are disposed on the surface of the dielectric layer facing away from the heat dissipation layer. In this way, because heat conducting performance of the heat dissipation layer is good, heat generated by the at least one chip during operation may be rapidly transferred from the heat dissipation layer to the radiator. This improves heat dissipation performance of the electronic element. In addition, because the dielectric layer has insulation performance, the dielectric layer may implement insulation isolation between the first input pad and the heat dissipation layer, between the first output pad and the heat dissipation layer, and between the heat dissipation layer and a connection line among the first input pad, the at least one chip, and the first output pad, to prevent a short circuit. In addition, because the at least one chip is disposed in the at least one accommodate groove, the at least one chip may be prevented from protruding beyond a contour of the substrate. This avoids interference between the at least one chip and the circuit board when the electronic element is connected to the circuit board.

[0010] Optionally, an impedance matching circuit is further included. The first input pad, the at least one chip, and the first output pad are connected through the impedance matching circuit. In this way, impedance matching is performed on an input, an output, or an interstage of the at least one chip through the impedance matching circuit, so that microwave signal energy is transmitted as much as possible to another load that is on the at least one chip or the circuit board and that is connected to an output terminal of the electronic element.

[0011] Optionally, the at least one chip includes one chip, and the impedance matching circuit includes a first impedance matching circuit and a second impedance matching circuit. The first input pad is connected to an input terminal of the chip through the first impedance matching circuit, and an output terminal of the chip is connected to the first output pad through the second impedance matching circuit. The first impedance matching circuit matches output impedance of a load that is on the circuit board and that is connected to the first input pad to input impedance of the chip. The second impedance matching circuit matches output impedance of the chip to input impedance of a load that is on the circuit board and that is connected to the first output pad. In this way, all signals output by the load that is on the circuit board and that is connected to the first input pad can be transmitted to the chip, and all signals output by the chip can be transmitted to the load that is on the circuit board and that is connected to the first output pad. Therefore, signal reflection is reduced, and a loss of signal energy is reduced.

[0012] Optionally, the at least one chip includes two chips, and the impedance matching circuit includes a first impedance matching circuit, a second impedance matching circuit, and a third impedance matching circuit. The first input pad is connected to an input terminal of one chip through the first impedance matching circuit. An out-

put terminal of the chip is connected to an input terminal of the other chip through the third impedance matching circuit. An output terminal of the other chip is connected to the first output pad through the second impedance matching circuit. The first impedance matching circuit matches output impedance of a load that is on the circuit board and that is connected to the first input pad to input impedance of the chip. The third impedance matching circuit matches output impedance of the chip to input impedance of the other chip. The second impedance matching circuit matches output impedance of the other chip to input impedance of a load that is on the circuit board and that is connected to the first output pad. In this way, all signals output by the load that is on the circuit board and that is connected to the first input pad can be transmitted to the chip, all signals output by the chip can be transmitted to the other chip, and all signals output by the other chip can be transmitted to the load that is on the circuit board and that is connected to the first output pad. Therefore, signal reflection is reduced, and a loss of signal energy is reduced.

[0013] Optionally, a connection line among the first input pad, the at least one chip, and the first output pad includes a first part and a second part. The first part is disposed on the surface of the dielectric layer facing away from the heat dissipation layer, and the second part is connected between the first part and the at least one chip. The electronic element further includes an encapsulation layer, the encapsulation layer is disposed on the first surface of the substrate, and the encapsulation layer warps the at least one chip and the second part. In this way, the chip and the second part are protected by using the encapsulation layer, so that the second part is prevented from being scratched and broken in a transport process of the electronic element, and water and dust are also prevented from touching the chip, thereby prolonging a service life of the chip.

[0014] Optionally, the encapsulation layer is disposed on the first surface of the substrate by using a glue dispensing process. When used for producing an encapsulation layer, the glue dispensing process has high accuracy, so that the encapsulation layer does not cover the first input pad and the first output pad, to avoid affecting welding between the circuit board and each of the first input pad and the first output pad.

[0015] Optionally, the at least one chip is a power amplifier chip.

[0016] Optionally, the at least one chip includes a plurality of chips, and the plurality of chips are connected in series between the first input pad and the first output pad.

[0017] According to a second aspect, some embodiments of this application provide a circuit board with an electronic element, including a circuit board and the electronic element described in any one of the foregoing technical solutions. A second output pad and a second input pad are disposed on a first surface of the circuit board, and the second output pad and the second input pad are connected to a circuit of the circuit board. The electronic element is located on a side of each of the second output pad and the second input pad facing away from the circuit board. A first surface of a substrate of the electronic element faces toward the circuit board. A first input pad of the electronic element is directly welded to the second output pad, and a first output pad of the electronic element is directly welded to the second input pad.

[0018] Compared with that in the conventional technology, when the circuit board with an electronic element provided in this embodiment of this application is attached to a radiator by using the electronic element, heat generated by at least one chip in the electronic element during operation may be directly transferred to the radiator by using the substrate. Therefore, the circuit board with an electronic element has a short heat dissipation path and high heat dissipation efficiency. In addition, the first input pad and the first output pad are directly disposed on the first surface of the substrate. The first input pad, the at least one chip, and the first output pad are sequentially connected. The electronic element is directly welded to the second output pad and the second input pad of the circuit board by using the first input pad and the first output pad. Therefore, there is no intermediate connection structure between the first input pad and the second output pad and between the first output pad and the second input pad. A lead-out path of each of an input terminal and an output terminal of the chip in the electronic element is short, and accuracy of the lead-out line is high. Therefore, input/output impedance matching performance of the electronic element can be effectively ensured.

[0019] Optionally, the electronic element includes an impedance matching circuit. The first input pad, the at least one chip of the electronic element, and the first output pad are connected through the impedance matching circuit. A groove is disposed on the circuit board opposite to the impedance matching circuit, and the impedance matching circuit is accommodated in the groove. In this way, a distance between the impedance matching circuit and stacked cabling in the circuit board is extended by the groove, so that the stacked cabling in the circuit board does not affect the impedance matching circuit. In addition, the impedance matching circuit is avoided by the groove, to avoid interference between the impedance matching circuit and the circuit board.

[0020] Optionally, a metal shield layer is disposed on both a side and a bottom of the groove. The metal shield layer can shield and isolate the impedance matching circuit from the stacked cabling in the circuit board, to prevent the impedance matching circuit from being affected by the stacked cabling in the circuit board.

[0021] Optionally, a depth of the groove is 2 mm to 3 mm. When the depth of the groove is within this range, the depth of the groove is moderate, so that the impedance matching circuit can be avoided, and structural strength of the circuit board and performance of the impedance matching circuit can also be considered.

[0022] Optionally, the circuit board with an electronic

element is a massive multi-input multi-output antenna transceiver circuit board.

[0023] According to a third aspect, some embodiments of this application provide an electronic device, including a radiator and the circuit board with an electronic element described in any one of the foregoing technical solutions. The radiator is located on a side of the electronic element facing away from the circuit board. A surface of the electronic element facing away from the circuit board is attached to a surface of the radiator. Alternatively, there is a gap between a surface of the electronic element facing away from the circuit board and a surface of the radiator, and the gap is filled with a heat conducting material.

[0024] According to the electronic device provided in this embodiment of this application, because the electronic device includes the circuit board with an electronic element described in any one of the foregoing technical solutions, the electronic device provided in this embodiment of this application can resolve a same technical problem and achieve a same expected effect as the circuit board with an electronic element described in any one of the foregoing technical solutions.

[0025] Optionally, the electronic device is a wireless base station.

BRIEF DESCRIPTION OF DRAWINGS

[0026]

FIG. 1 is a schematic diagram of a structure of an electronic element in the conventional technology;

FIG. 2 is a schematic diagram of a first assembly structure of an electronic element, a circuit board, and a radiator in the conventional technology;

FIG. 3 is a schematic diagram of a second assembly structure of an electronic element, a circuit board, and a radiator in the conventional technology;

FIG. 4 is a schematic diagram of a third assembly structure of an electronic element, a circuit board, and a radiator in the conventional technology;

FIG. 5 is a schematic diagram of a structure of an electronic device according to an embodiment of this application;

FIG. 6 is a schematic diagram of a structure of a first circuit board with an electronic element according to an embodiment of this application;

FIG. 7 is a schematic diagram of a structure of a first electronic element according to an embodiment of this application;

FIG. 8 is a schematic diagram of a structure of a second electronic element according to an embodiment of this application;

FIG. 9 is a sectional view of the electronic element shown in FIG. 8 along a section A-A;

FIG. 10 is a schematic diagram of a structure of a third electronic element according to an embodiment of this application;

FIG. 11 is a sectional view of the electronic element shown in FIG. 10 along a section B-B;

FIG. 12 is a schematic diagram of a structure of a fourth electronic element according to an embodiment of this application;

FIG. 13 is a sectional view of the electronic element shown in FIG. 12 along a section C-C;

FIG. 14 is a schematic diagram of a structure of a second circuit board with an electronic element according to an embodiment of this application; and

FIG. 15 is a schematic diagram of a structure of a fifth electronic element according to an embodiment of this application.

Reference numerals:

[0027] 01-electronic element; 011-substrate; 012-chip; 013-input pad; 014-output pad; 015-plastic packaging layer; 011a-first surface of a substrate; 011b-second surface of a substrate; 016-first metalized through hole; 017-second metalized through hole; 02-circuit board; 03-radiator; 1-radiator; 2-circuit board with an electronic element; 21-circuit board; 21a-first surface of a circuit board; 211-second output pad; 212-second input pad; 22-electronic element; 221-substrate; 221a-first surface of a substrate; 2211-heat dissipation layer; 2212-dielectric layer; 2213-accommodate groove; 221a1-area on a surface of a heat dissipation layer opposite to an accommodate groove; 221a2-side of an accommodate groove; 221a3-surface of a dielectric layer facing away from a heat dissipation layer; 222-first input pad; 223-chip; 224-first output pad; 225-impedance matching circuit; 2251-first impedance matching circuit; 2252-second impedance matching circuit; 2253-third impedance matching circuit; 226-encapsulation layer; 23-groove; 100-connection line; 101-first part of a connection line; and 102-second part of a connection line.

DESCRIPTION OF EMBODIMENTS

[0028] Embodiments of this application relate to an electronic element, a circuit board with an electronic element, and an electronic device. The following briefly describes concepts involved in the embodiments.

[0029] An electronic device is a device that has an electronic circuit inside and a function by applying electronic technology software.

[0030] A circuit board is a structure that is formed by a dielectric layer and a line, a pad, and a through hole that are disposed on the dielectric layer, and is configured to implement interconnection between electronic elements to constitute an electronic circuit with a specific function.

[0031] Electric polarization refers to a phenomenon that a macroscopic electric dipole moment that is not equal to zero is generated under an action of an external electric field, thereby forming a macroscopic bound charge.

[0032] A dielectric refers to a substance that can gen-

erate an electric polarization phenomenon, including a crystalline dielectric layer and an amorphous dielectric layer, where a resistivity of the dielectric is usually high, and the dielectric has insulation performance.

[0033] A dielectric layer is a layer structure formed by a dielectric.

[0034] An electronic element is a basic element in an electronic circuit, is usually individually encapsulated, and has two or more pins.

[0035] Impedance matching circuit: Impedance matching is a part of microwave electronics, is mainly used on a transmission line, to achieve that all high-frequency microwave signal can be transmitted to a load point, and almost no signal is reflected back to a source point, thereby improving energy efficiency.

[0036] In an electronic device such as a wireless base station, with a high integrated high-density arrangement of electronic elements on the circuit board, effective heat dissipation needs to be performed on the circuit board with an electronic element. In addition, accuracy of a lead-out line of each of an input terminal and an output terminal of a chip in the electronic element need to be high, to ensure impedance matching performance of the electronic element.

[0037] To achieve the foregoing two objectives, FIG. 5 is a schematic diagram of an electronic device according to some embodiments of this application. The electronic device includes but is not limited to a wireless base station. As shown in FIG. 5, the electronic device includes a radiator 1 and a circuit board 2 with an electronic element. The radiator 1 includes but is not limited to a fin radiator and a refrigerant cooled radiator.

[0038] FIG. 6 is a schematic diagram of a circuit board with an electronic element according to some embodiments of this application. The circuit board 2 with an electronic element is an electronic circuit structure with a specific function, for example, a massive multiple-input multiple-output (massive multiple-input multiple-output, Massive MIMO) antenna transceiver circuit board in the wireless base station. As shown in FIG. 6, the circuit board 2 with an electronic element includes a circuit board 21 and an electronic element 22.

[0039] FIG. 7 is a schematic diagram of an electronic element 22 according to some embodiments of this application. The electronic element 22 includes but is not limited to a power amplifier module (power amplifier module, PAM). As shown in FIG. 7, the electronic element 22 includes a substrate 221, and a first input pad 222, at least one chip 223, and a first output pad 224 that are disposed on a first surface 221a of the substrate 221. The chip 223 includes but is not limited to a power amplifier chip. The first input pad 222, the at least one chip 223, and the first output pad 224 are sequentially connected. The first input pad 222 and the first output pad 224 are directly disposed on the first surface 221a of the substrate 221. A surface of the first input pad 222 facing away from the substrate 221 and a surface of the first output pad 224 facing away from the substrate 221 constitute a partial area of an outer surface of the electronic element 22.

[0040] It should be noted that the first input pad 222 and the first output pad 224 are directly disposed on the first surface 221a of the substrate 221, that is, the first input pad 222 and the first output pad 224 are directly in contact with and fastened to the first surface 221a of the substrate 221. There is no intermediate connection structure between the first input pad 222 and the first surface 221a of the substrate 221 and between the first output pad 224 and the first surface 221a of the substrate 221.

[0041] It should be noted that the surface of the first input pad 222 facing away from the substrate 221 and the surface of the first output pad 224 facing away from the substrate 221 constitute a partial area of the outer surface of the electronic element 22. Therefore, the surface of the first input pad 222 facing away from the substrate 221 and the surface of the first output pad 224 facing away from the substrate 221 are disposed to be exposed. That is, the surface of the first input pad 222 facing away from the substrate 221 and the surface of the first output pad 224 facing away from the substrate 221 are not covered.

[0042] The at least one chip 223 may include one chip 223, or may include a plurality of chips 223, which is not specifically limited herein. In some embodiments, the at least one chip 223 includes a plurality of chips 223, and the plurality of chips 223 are connected in series between the first input pad 222 and the first output pad 224.

[0043] As shown in FIG. 6, a second output pad 211 and a second input pad 212 are disposed on a first surface 21a of the circuit board 21. The second output pad 211 and the second input pad 212 are connected to a circuit of the circuit board 21. The electronic element 22 is located on a side of each of the second output pad 211 and the second input pad 212 facing away from the circuit board 21. The first surface 221a of the substrate 221 of the electronic element 22 faces toward the circuit board 21. The first input pad 222 of the electronic element 22 is directly welded to the second output pad 212, and the first output pad 224 of the electronic element 22 is directly welded to the second input pad 211.

[0044] It should be noted that the first input pad 222 of the electronic element 22 is directly welded to the second output pad 212, that is, the first input pad 222 of the electronic element 22 is directly in contact with and welded to the second output pad 212. There is no intermediate connection structure between the first input pad 222 of the electronic element 22 and the second output pad 212.

[0045] Similarly, the first output pad 224 of the electronic element 22 is directly welded to the second input pad 211, that is, the first output pad 224 of the electronic element 22 is directly in contact with and welded to the second input pad 211. There is no intermediate connection structure between the first output pad 224 of the electronic element 22 and the second input pad 211.

[0046] As shown in FIG. 5, the radiator 1 is located on a side of the electronic element 22 facing away from the

circuit board 21, and a surface of the electronic element 22 facing away from the circuit board 21 is attached to a surface of the radiator 1.

[0047] Alternatively, there is a gap between a surface of the electronic element 22 facing away from the circuit board 21 and a surface of the radiator 1, and the gap is filled with a heat conducting material 3. The heat conducting material 3 includes but is not limited to thermally conductive silicone and thermal silica gel.

[0048] In this way, heat generated by the at least one chip 223 in the electronic element 22 during operation can be directly transferred to the radiator 1 by using the substrate 221. Therefore, a heat dissipation path of the circuit board 2 with an electronic element is short, and heat dissipation efficiency is high.

[0049] In addition, the first input pad 222 and the first output pad 224 are directly disposed on the first surface 221a of the substrate 221. The first input pad 222, the at least one chip 223, and the first output pad 224 are sequentially connected. The electronic element 22 is directly welded to the second output pad 212 and the second input pad 211 of the circuit board 21 by using the first input pad 222 and the first output pad 224. Therefore, there is no intermediate connection structure between the first input pad 222 and the second output pad 212 and between the first output pad 224 and the second input pad 211. A lead-out path of each of an input terminal and an output terminal of the chip 223 in the electronic element 22 is short, and accuracy of the lead-out line is high. Therefore, input/output impedance matching performance of the electronic element 22 can be effectively ensured.

[0050] To enable the substrate 221 to transfer the heat generated by the chip 223 during operation to the radiator, in some embodiments, as shown in FIG. 8 and FIG. 9, the substrate 221 includes a heat dissipation layer 2211 and a dielectric layer 2212 that are stacked. A material of the heat dissipation layer 2211 includes but is not limited to aluminum-based metal and copper. The dielectric layer 2212 has insulation performance. At least one accommodate groove 2213 is disposed on the dielectric layer 2212. The accommodate groove 2213 penetrates the dielectric layer 2212. An area 221a1 that is on a surface of the heat dissipation layer 2211 and that is opposite to the accommodate groove 2213, a side 221a2 of the accommodate groove 2213, and a surface 221a3 of the dielectric layer 2212 facing away from the heat dissipation layer 2211 constitute the first surface 221a of the substrate 221. The at least one chip 223 is disposed in the at least one accommodate groove 2213 and is fastened in the area 221a1 that is on the surface of the heat dissipation layer 2211 and that is opposite to the accommodate groove 2213. The first input pad 222 and the first output pad 224 are disposed on the surface 221a3 of the dielectric layer 2212 facing away from the heat dissipation layer 2211.

[0051] In this way, because heat conducting performance of the heat dissipation layer 2211 is good, the heat generated by the at least one chip 223 during operation may be rapidly transferred from the heat dissipation layer 2211 to the radiator. This improves heat dissipation performance of the electronic element 22. In addition, because the dielectric layer 2212 has the insulation performance, the dielectric layer 2212 may implement insulation isolation between the first input pad 222 and the heat dissipation layer 2211, between the first output pad 224 and the heat dissipation layer 2211, and between the heat dissipation layer 2211 and a connection line among the first input pad 222, the at least one chip 223, and the first output pad 224, to prevent a short circuit. In addition, because the at least one chip 223 is disposed in the at least one accommodate groove 2213, the at least one chip 223 may be prevented from protruding beyond a contour of the substrate 221. This avoids interference between the at least one chip 223 and the circuit board when the electronic element 22 is connected to the circuit board 21.

[0052] When the electronic element 22 operates under a microwave signal, to reduce input reflection and output reflection of the at least one chip 223 to enable microwave signal energy to be transmitted as much as possible to another load that is on the at least one chip 223 or the circuit board and that is connected to an output terminal of the electronic element 22, in some embodiments, as shown in FIG. 10 or FIG. 11, an impedance matching circuit 225 is further included, and the first input pad 222, the at least one chip 223, and the first output pad 224 are connected through the impedance matching circuit 225. A structure of the impedance matching circuit 225 includes but is not limited to an electronic circuit formed by connecting a microstrip and an electronic element.

[0053] In this way, impedance matching is performed on an input, an output, or an interstage of the at least one chip 223 through the impedance matching circuit 225, so that the microwave signal energy is transmitted as much as possible to the another load that is on the at least one chip 223 or the circuit board and that is connected to the output terminal of the electronic element 22.

[0054] The structure of the impedance matching circuit 225 may be described in detail by using the following two examples:

[0055] Example 1: As shown in FIG. 10 and FIG. 11, the at least one chip 223 includes one chip 223, and the impedance matching circuit 225 includes a first impedance matching circuit 2251 and a second impedance matching circuit 2252. The first input pad 222 is connected to an input terminal of the chip 223 through the first impedance matching circuit 2251, and an output terminal of the chip 223 is connected to the first output pad 224 through the second impedance matching circuit 2252. The first impedance matching circuit 2251 matches output impedance of a load that is on the circuit board and that is connected to the first input pad 222 to input impedance of the chip 223. The second impedance matching circuit 2252 matches output impedance of the chip 223 to input impedance of a load that is on the circuit

board and that is connected to the first output pad 224.

[0056] In this way, all signals output by the load that is on the circuit board and that is connected to the first input pad 222 can be transmitted to the chip 223, and all signals output by the chip 223 can be transmitted to the load that is on the circuit board and that is connected to the first output pad 224. Therefore, signal reflection is reduced, and a loss of signal energy is reduced.

[0057] Example 2: As shown in FIG. 12 and FIG. 13, the at least one chip 223 includes two chips 223, and the impedance matching circuit 225 includes a first impedance matching circuit 2251, a second impedance matching circuit 2252, and a third impedance matching circuit 2253. The first input pad 222 is connected to an input terminal of one chip 223 through the first impedance matching circuit 2251. An output terminal of the chip 223 is connected to an input terminal of the other chip 223 through the third impedance matching circuit 2253. An output terminal of the other chip 223 is connected to the first output pad 224 through the second impedance matching circuit 2252. The first impedance matching circuit 2251 matches output impedance of a load that is on the circuit board and that is connected to the first input pad 222 to input impedance of the chip 223. The third impedance matching circuit 2253 matches output impedance of the chip 223 to input impedance of the other chip 223. The second impedance matching circuit 2252 matches output impedance of the other chip 223 to input impedance of a load that is on the circuit board and that is connected to the first output pad 224.

[0058] In this way, all signals output by the load that is on the circuit board and that is connected to the first input pad 222 can be transmitted to the chip 223, all signals output by the chip 223 can be transmitted to the other chip 223, and all signals output by the other chip 223 can be transmitted to the load that is on the circuit board and that is connected to the first output pad 224. Therefore, signal reflection is reduced, and a loss of signal energy is reduced.

[0059] The circuit board 21 is stacked by a plurality of circuit board units, and cabling is disposed on each circuit board unit. In some embodiments, as shown in FIG. 14, a groove 23 is disposed on the circuit board 21 opposite to the impedance matching circuit 225, and the impedance matching circuit 225 is accommodated in the groove 23. Therefore, it is avoided that performance of the impedance matching circuit 225 is affected by stacked cabling in the circuit board 21 due to an excessively close distance between the impedance matching circuit 225 and the stacked cabling in the circuit board 21 when the electronic element 22 is connected to the circuit board 21, or interference between the impedance matching circuit 225 and the circuit board 21 generated when the electronic element 22 is connected to the circuit board 21 is avoided.

[0060] In this way, a distance between the impedance matching circuit 225 and the stacked cabling in the circuit board 21 is extended by the groove 23, so that the stacked cabling in the circuit board 21 does not affect the impedance matching circuit 225. In addition, the impedance matching circuit 225 is avoided by the groove 23, to avoid interference between the impedance matching circuit 225 and the circuit board 21.

[0061] In order to further avoid that the impedance matching circuit 225 is affected by the stacked cabling in the circuit board 21 when the electronic element 22 is connected to the circuit board 21, in some embodiments, a metal shield layer is disposed on both a side and a bottom of the groove 23. The metal shield layer can shield and isolate the impedance matching circuit 225 from the stacked cabling in the circuit board 21, to prevent the impedance matching circuit 225 from being affected by the stacked cabling in the circuit board 21.

[0062] A depth of the groove 23 may be 1 mm, 2 mm, 3 mm, or the like. This is not specifically limited herein. Specifically, a comprehensive design may be performed based on a height of the impedance matching circuit 225 protruding beyond the first surface 221a of the substrate 221, a structural strength requirement of the circuit board 21, and an influence of the depth of the groove 23 on the performance of the impedance matching circuit 225. Therefore, the groove 23 can accommodate the impedance matching circuit 225, structural strength of the circuit board 21 is ensured, and an influence of the stacked cabling in the circuit board 21 on the performance of the impedance matching circuit 225 is weakened as much as possible. In some embodiments, as shown in FIG. 14, the depth d of the groove 23 is 2 mm to 3 mm. When the depth d of the groove 23 is within this range, the depth of the groove 23 is moderate, so that the impedance matching circuit 225 can be avoided, and the structural strength of the circuit board 21 and the performance of the impedance matching circuit 225 can also be considered.

[0063] As shown in FIG. 8 and FIG. 9, on the first surface 221a of the substrate 221, a connection line 100 between the first input pad 222, the at least one chip 223, and the first output pad 224 includes a first part 101 and a second part 102. In some embodiments, the connection line 100 is the impedance matching circuit 225 shown in FIG. 10 to FIG. 13. The first part 101 is disposed on the surface 221a3 of the dielectric layer 2212 facing away from the heat dissipation layer 2211. The second part 102 is connected between the first part 101 and the at least one chip 223, and the second part 102 is suspended. The first part 101 is supported by the dielectric layer 2212, and is not easily scratched and broken by an external force in a process of moving the electronic element 22. However, because of suspension setting and a low strength of the connection line, the second part 102 is easily scratched and broken by an external force in the process of moving the electronic element 22. In addition, if the chip 223 is disposed to be exposed, in a long time transportation or storage process, the chip 223 may be eroded by water and dust in the air. Consequently, a service life of the chip 223 is shortened.

[0064] To resolve the foregoing problems, in some embodiments, as shown in FIG. 15, the electronic element 22 further includes an encapsulation layer 226. A material of the encapsulation layer 226 is an insulating material, including but not limited to epoxy and silicone plastics. The encapsulation layer 226 is disposed on the first surface 221a of the substrate 221, and the encapsulation layer 226 warps the at least one chip 223 and the second part 102.

[0065] In this way, the chip 223 and the second part 102 are protected by using the encapsulation layer 226, so that the second part 102 is prevented from being scratched and broken in a transport process of the electronic element 22, and water and dust are also prevented from touching the chip 223. This improves a product rate of the electronic element 22 in a processing and assembly process. The chip 223 is prevented from being eroded by external moisture and another factor, to ensure reliability of an electronic element product for long-term use.

[0066] The encapsulation layer 226 may be disposed on the first surface 221a of the substrate 221 by using a wrapper, or may be disposed on the first surface 221a of the substrate 221 by using a glue dispensing machine, which is not specifically limited herein. In some embodiments, the encapsulation layer 226 is disposed on the first surface 221a of the substrate 221 by using a glue dispensing process. When used for producing the encapsulation layer 226, the glue dispensing process has high accuracy, so that the encapsulation layer 226 does not cover the first input pad 222 and the first output pad 224, to avoid affecting welding between the circuit board and each of the first input pad 222 and the first output pad 224.

[0067] It should be noted that when the electronic element 22 having the encapsulation layer 226 is installed on the circuit board 21, the encapsulation layer 226 is accommodated in the groove 23, to avoid the encapsulation layer 226 by using the groove 23, to prevent interference between the encapsulation layer 226 and the circuit board 21.

[0068] In the descriptions of this specification, the specific features, structures, materials, or characteristics may be combined in an appropriate manner in any one or more of the embodiments or examples.

[0069] Finally, it should be noted that the foregoing embodiments are merely intended for describing the technical solutions of this application, but not for limiting this application. Although this application is described in detail with reference to the foregoing embodiments, persons of ordinary skill in the art should understand that they may still make modifications to the technical solutions described in the foregoing embodiments or make equivalent replacements to some technical features thereof, without departing from the spirit and scope of the technical solutions of embodiments of this application.

Claims

1. An electronic element, comprising a substrate and a first input pad, at least one chip, and a first output pad that are disposed on a first surface of the substrate, wherein the first input pad, the at least one chip, and the first output pad are sequentially connected, the first input pad and the first output pad are directly disposed on the first surface of the substrate, and a surface of the first input pad facing away from the substrate and a surface of the first output pad facing away from the substrate constitute a partial area of an outer surface of the electronic element.

2. The electronic element according to claim 1, wherein the substrate comprises a heat dissipation layer and a dielectric layer that are stacked; and
at least one accommodate groove is disposed on the dielectric layer, the accommodate groove penetrates the dielectric layer, an area that is on a surface of the heat dissipation layer and that is opposite to the accommodate groove, a side of the accommodate groove, a surface of the dielectric layer facing away from the heat dissipation layer constitute the first surface of the substrate, the at least one chip is disposed in the at least one accommodate groove and is fastened in the area that is on the surface of the heat dissipation layer and that is opposite to the accommodate groove, and the first input pad and the first output pad are disposed on the surface of the dielectric layer facing away from the heat dissipation layer.

3. The electronic element according to claim 2, further comprising an impedance matching circuit, wherein the first input pad, the at least one chip, and the first output pad are connected through the impedance matching circuit.

4. The electronic element according to claim 2 or 3, wherein a connection line among the first input pad, the at least one chip, and the first output pad comprises a first part and a second part, the first part is disposed on the surface of the dielectric layer facing away from the heat dissipation layer, and the second part is connected between the first part and the at least one chip; and
the electronic element further comprises an encapsulation layer, the encapsulation layer is disposed on the first surface of the substrate, and the encapsulation layer warps the at least one chip and the second part.

5. The electronic element according to claim 4, wherein the encapsulation layer is disposed on the first surface of the substrate by using a glue dispensing process.

6. The electronic element according to any one of claims 1 to 5, wherein the at least one chip is a power amplifier chip.

7. The electronic element according to any one of claims 1 to 6, wherein the at least one chip comprises a plurality of chips, and the plurality of chips are connected in series between the first input pad and the first output pad.

8. A circuit board with an electronic element, comprising a circuit board and the electronic element according to any one of claims 1 to 7, wherein a second output pad and a second input pad are disposed on a first surface of the circuit board, the second output pad and the second input pad are connected to a circuit of the circuit board, the electronic element is located on a side of each of the second output pad and the second input pad facing away from the circuit board, a first surface of a substrate of the electronic element faces toward the circuit board, a first input pad of the electronic element is directly welded to the second output pad, and a first output pad of the electronic element is directly welded to the second input pad.

9. The circuit board with an electronic element according to claim 8, wherein the electronic element comprises an impedance matching circuit, and the first input pad, at least one chip, and the first output pad of the electronic element are connected through the impedance matching circuit; and
a groove is disposed on the circuit board opposite to the impedance matching circuit, and the impedance matching circuit is accommodated in the groove.

10. The circuit board with an electronic element according to claim 9, wherein a metal shield layer is disposed on both a side and a bottom of the groove.

11. The circuit board with an electronic element according to claim 9 or 10, wherein a depth of the groove is 2 mm to 3 mm

12. The circuit board with an electronic element according to any one of claims 8 to 11, wherein the circuit board with an electronic element is a massive multi-input multi-output antenna transceiver circuit board.

13. An electronic device, comprising a radiator and the circuit board with an electronic element according to any one of claims 8 to 12, wherein the radiator is located on a side of the electronic element facing away from the circuit board; and a surface of the electronic element facing away from the circuit board is attached to a surface of the radiator, or there is a gap between a surface of the electronic element facing away from the circuit board and a surface of the radiator, wherein the gap is filled with a heat conducting material.

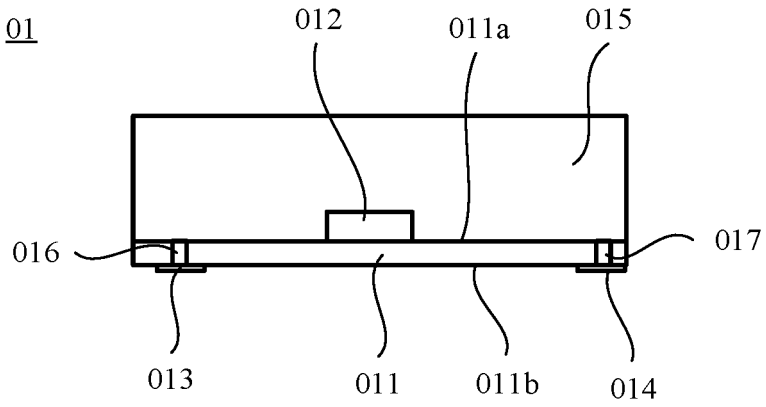


FIG. 1

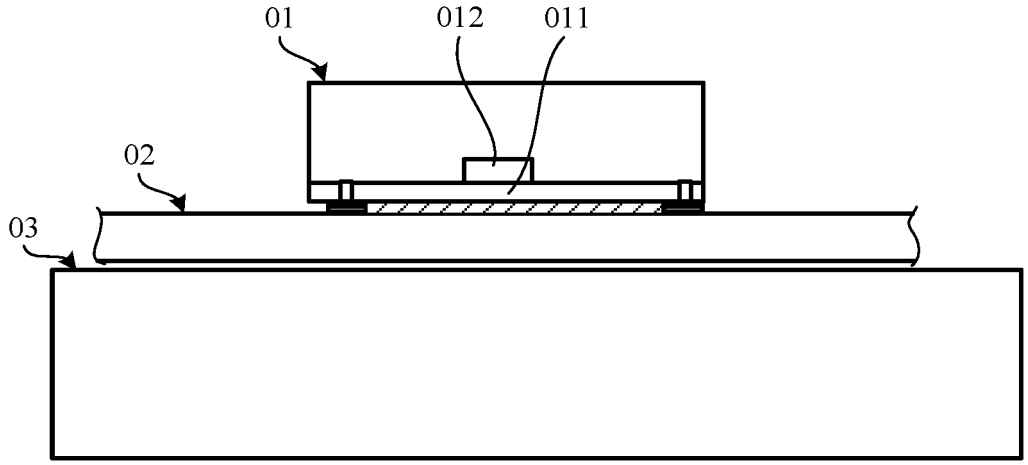


FIG. 2

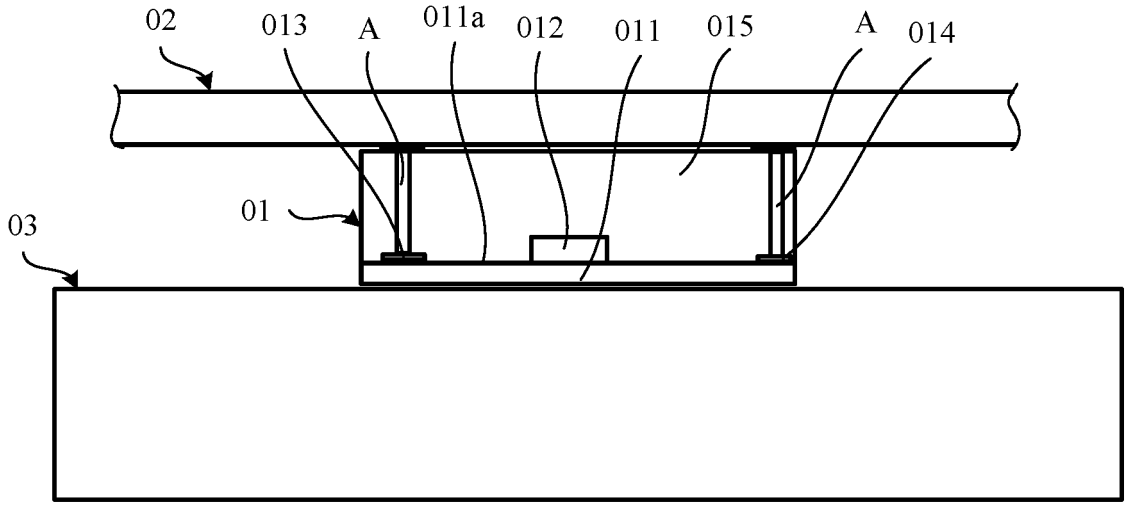


FIG. 3

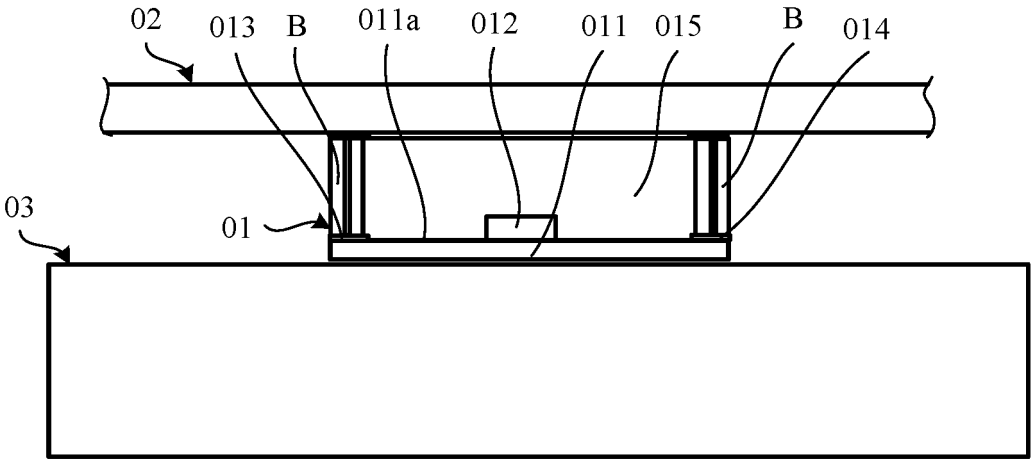


FIG. 4

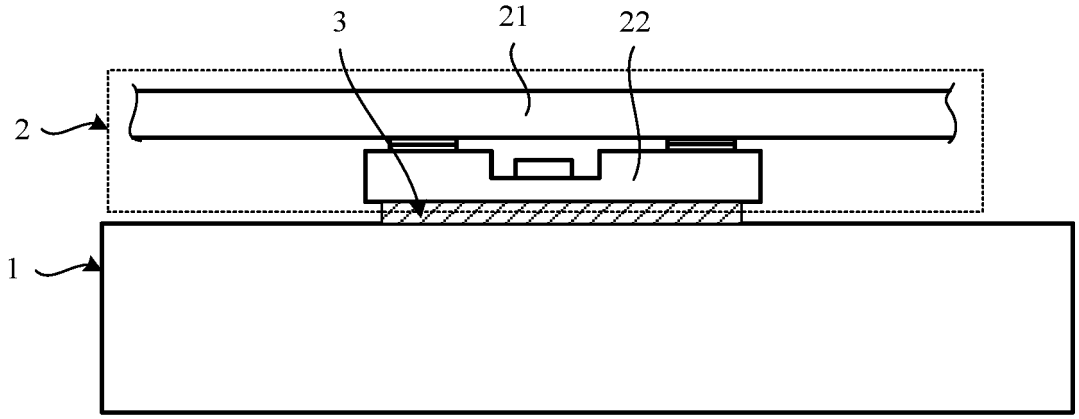


FIG. 5

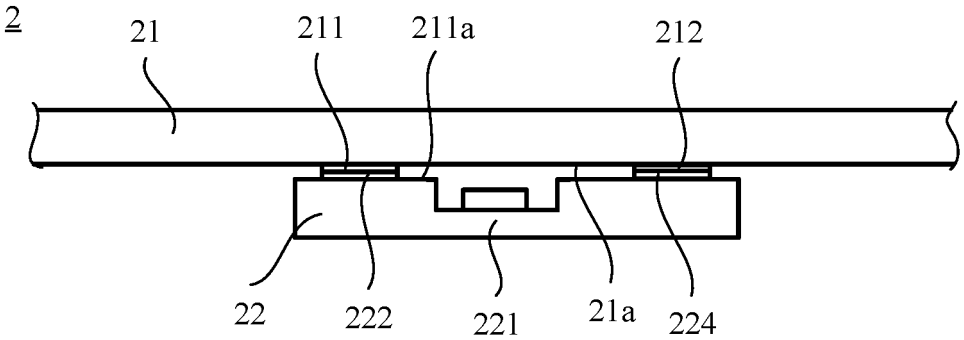
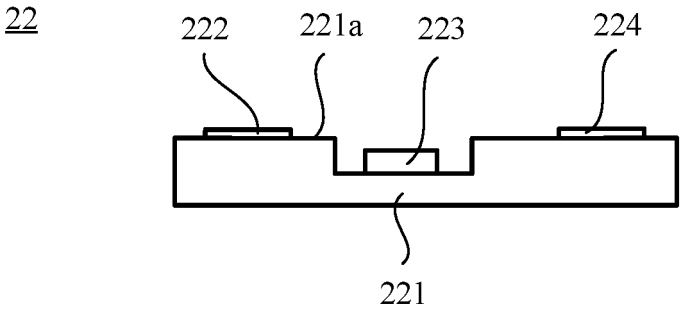


FIG. 6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224
221

FIG. 7

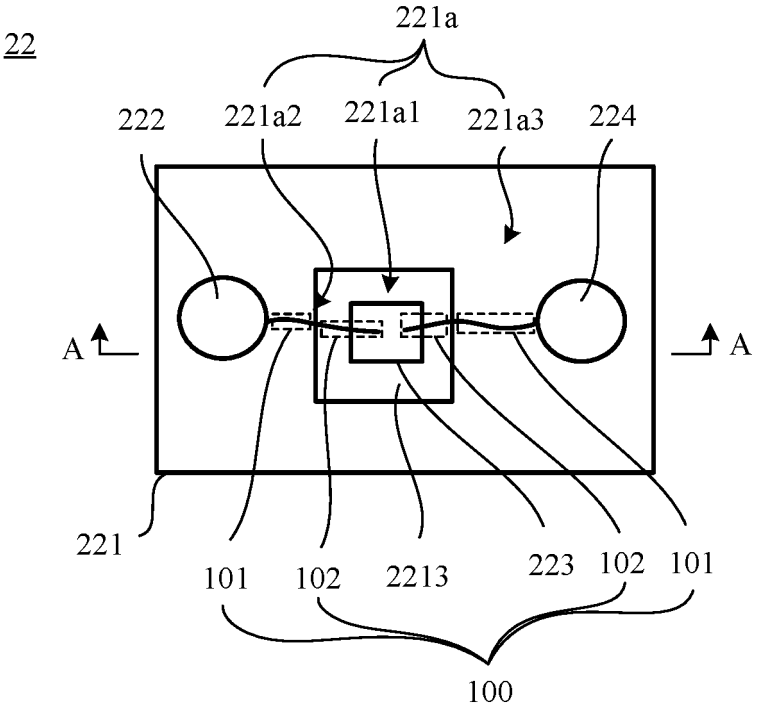
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FIG. 8

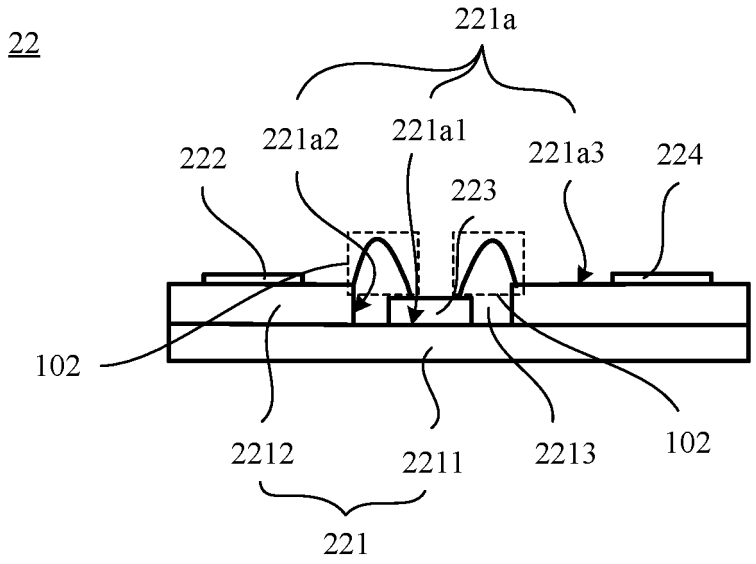
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FIG. 9

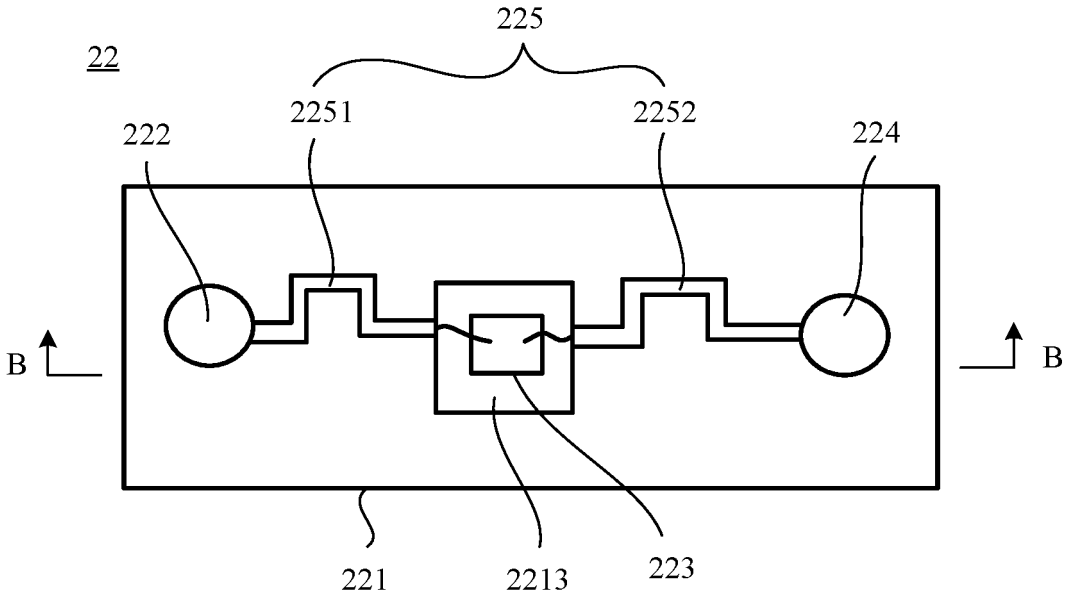
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FIG. 10

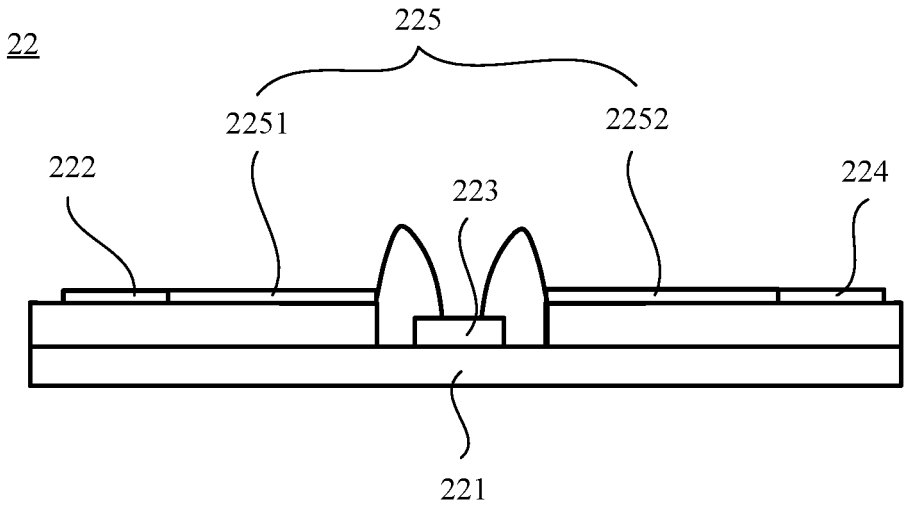
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FIG. 11

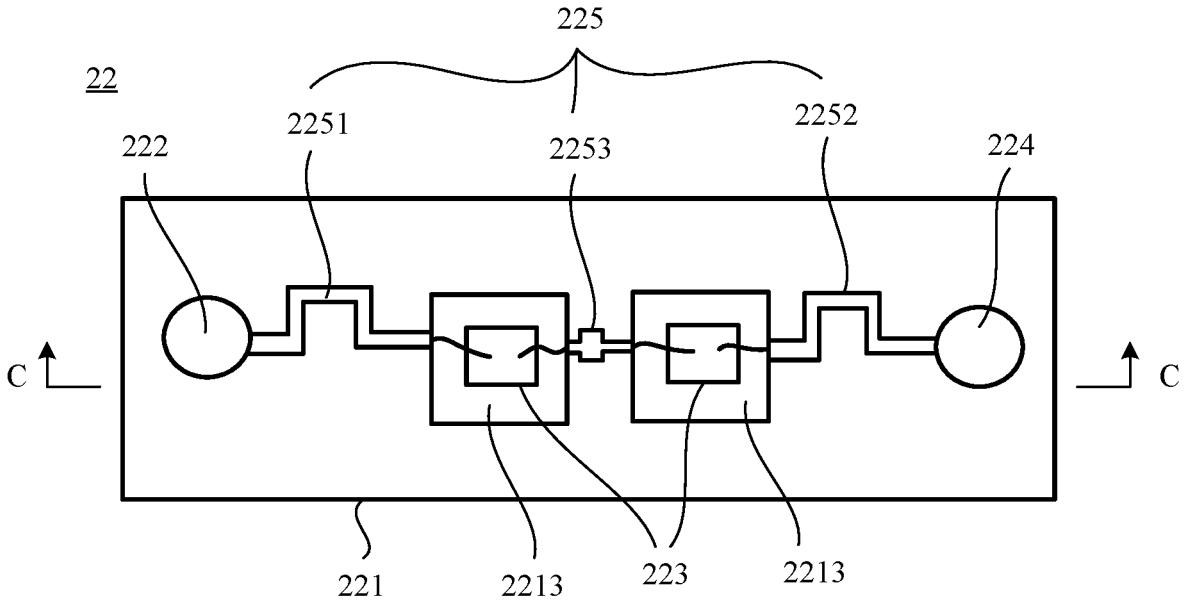
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FIG. 12

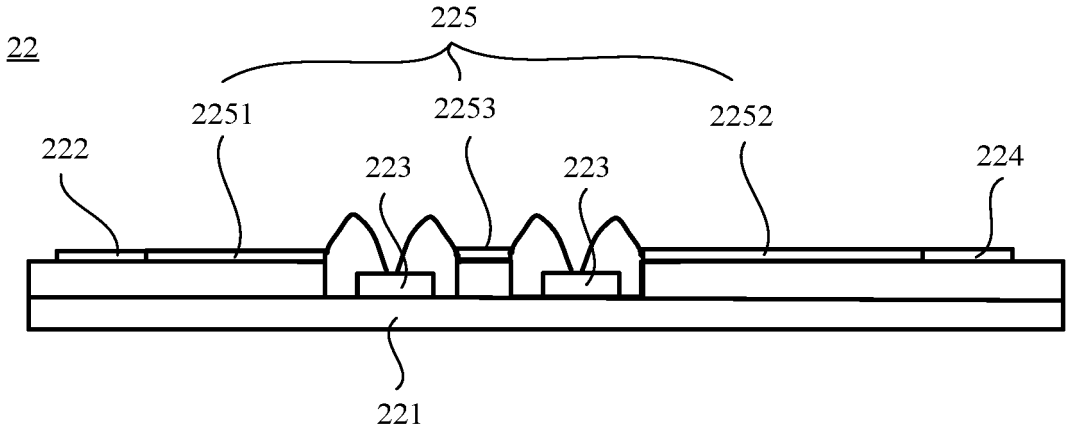

FIG. 13

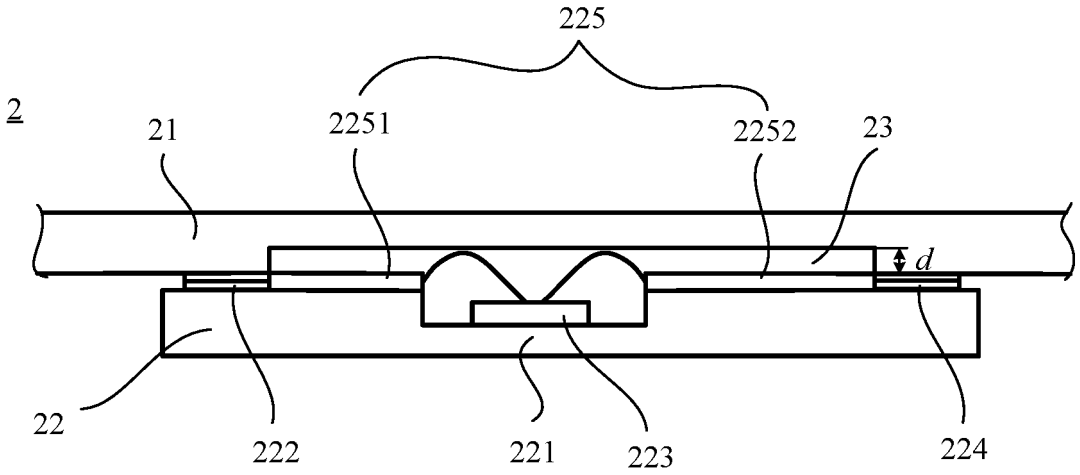

FIG. 14

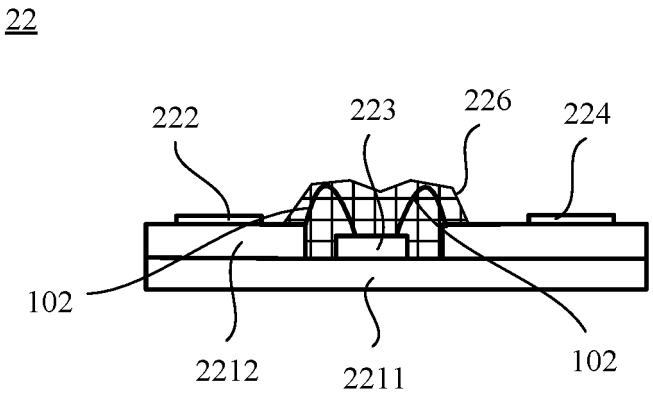

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/125365

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/48(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI: 散热, 路径, 短, 热沉, 凹, 槽, 焊盘, 焊球, 无需, 不需, 阻抗, 匹配, 电路板, 线路板, 容纳, 收容, PCB, heat, radiat+, path, short, sink, concave, recess, pad?, solder, need, impedance, match+, wir+, circuit, board, accommodat+; accept+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005104205 A1 (WANG, Chung-Cheng) 19 May 2005 (2005-05-19) description paragraphs [0005]-[0007], [0057], [0081], [0116]-[0125], figures 7, 16, 38A-40, 42, 51	1-6, 8, 12
Y	US 2005104205 A1 (WANG, Chung-Cheng) 19 May 2005 (2005-05-19) description paragraphs [0005]-[0007], [0057], [0081], [0116]-[0125], figures 7, 16, 38A-40, 42, 51	7, 13
Y	CN 1591862 A (ADVANCED SEMICONDUCTOR ENGINEERING, INC.) 09 March 2005 (2005-03-09) description page 7 lines 12-24, figures 4, 5	7
Y	CN 1440058 A (SHINKO ELECTRIC INDUSTRIES CO., LTD.) 03 September 2003 (2003-09-03) description page 8 line 26 to page 9 line 17, figures 7, 8	13
A	CN 108447852 A (CALTERAH SEMICONDUCTOR TECHNOLOGY (SHANGHAI) CO., LTD.) 24 August 2018 (2018-08-24) entire document	1-13

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 August 2020	**02 September 2020**

Name and mailing address of the ISA/CN	Authorized officer
China National Intellectual Property Administration (ISA/CN) **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088** **China**	
Facsimile No. **(86-10)62019451**	Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/125365

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2019/125365

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CN 1416160 A	07 May 2003	CN 1208821 C	29 June 2005

Form PCT/ISA/210 (patent family annex) (January 2015)