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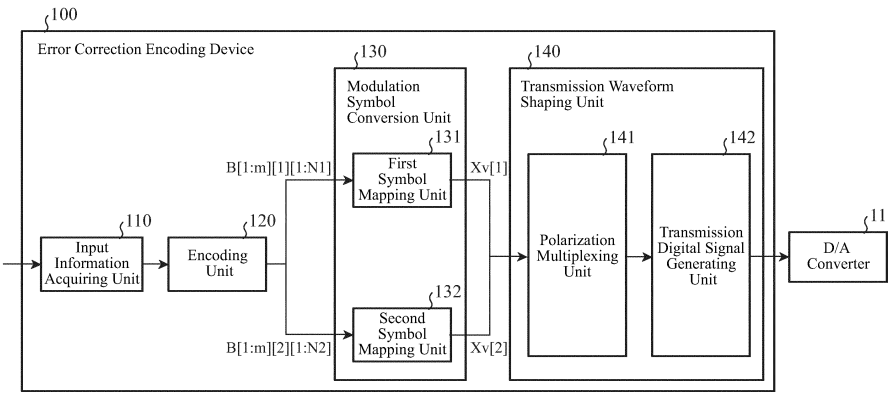
(54) ERROR CORRECTION ENCODING DEVICE, ERROR CORRECTION ENCODING METHOD, ERROR CORRECTION DEVICE, ERROR CORRECTION METHOD, COMMUNICATION METHOD, OPTICAL COMMUNICATION SYSTEM, AND SOFT DECISION ERROR CORRECTION FRAME DATA STRUCTURE

(57) An error correction encoding device (100) includes an encoding unit (120) to generate soft decision error correction frame information including a bit array of m rows and N columns obtained by combining first bit string group information and second bit string group information, the first bit string group information including a bit array of m rows and N1 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol by using a first symbol mapping rule, the second bit string group information including a bit array of m rows and N2 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol by using a second symbol mapping rule.

FIG. 2



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Description

TECHNICAL FIELD

[0001] The present disclosure relates to an error correction encoding device, an error correction encoding method, an error correction device, an error correction method, a communication method, an optical communication system, and a soft decision error correction frame data structure.

BACKGROUND ART

[0002] There is a communication system in which a transmission device performs error correction encoding on input information input to the transmission device and transmits a signal based on information after the error correction encoding to a reception device, and the reception device outputs output information corresponding to the input information by receiving the signal transmitted from the transmission device and performing error correction on information based on the signal.

[0003] For example, Non-Patent Literature 1 discloses a communication method using information generated by combining probability distribution shaping encoding processing and multi-level encoding processing in a field of optical communication systems, the information having a predetermined data structure in which multi-level modulation of a combination on a plurality of bits can be performed by selectively using two symbol mappings, first and second.

[0004] Specifically, a transmission device described in Non-Patent Literature 1 (Hereinafter, it is referred to as a "conventional transmission device".) generates information having the above-described data structure on the basis of the input information. More specifically, the conventional transmission device generates information having the above-described data structure by performing soft decision error correction encoding processing by using the least significant bit, and a plurality of middle bits that is a target of Gray encoding processing and disposing a soft decision parity bit acquired by the soft decision error correction encoding processing in the most significant bit. Further, the conventional transmission device performs division into a first symbol group in which the most significant bit is the soft decision parity bit and a second symbol group in which the most significant bit is not the soft decision parity bit. The conventional transmission device performs first symbol mapping with Gray code on symbols belonging to the first symbol group, and performs second symbol mapping different from the first symbol mapping on symbols belonging to the second symbol group.

[0005] In addition, a reception device described in Non-Patent Literature 1 (Hereinafter, it is referred to as a "conventional reception device".) acquires output information corresponding to input information by receiving a signal generated by the conventional transmission device on the basis of information having the above-described data structure and performing multi-stage decoding processing on information based on the signal. More specifically, the conventional reception device performs error correction on the least significant bit, and the plurality of middle bits that are the target of the Gray encoding processing by performing soft decision error correction processing using the soft decision parity bit. Further, the conventional reception device performs hard decision processing on a plurality of middle bits of a symbol and the most significant bit of the symbol by using a bit value of the least significant bit of the symbol after the soft decision error correction processing with respect to the symbol in which the most significant bit is not the soft decision parity bit, that is, a symbol corresponding to the symbol belonging to the first symbol group in the conventional transmission device.

CITATION LIST

NON-PATENT LITERATURE

[0006] Non-Patent Literature 1: K. Sugitani et al., "Partial multilevel coding with probabilistic shaping for low-power optical transmission", Proc. OECC/PSC 2019, Paper TuB1-5.

SUMMARY OF INVENTION

TECHNICAL PROBLEM

[0007] In general, as the number of bits to be protected by soft decision error correction increases, the amount of calculation is required more, in the soft decision error correction encoding processing. Thus, in the soft decision error correction encoding processing, it is desirable to reduce the number of bits to be protected by the soft decision error correction.

[0008] The soft decision error correction encoding processing described in Non-Patent Literature 1 (Hereinafter, it is referred to as "conventional soft decision error correction encoding processing".) uses the least significant bit, and the plurality of middle bits that is the target of the Gray encoding processing. For that reason, there has been a problem in the conventional soft decision error correction encoding processing that all bits other than the most significant bit are to be protected by the soft decision error correction.

[0009] The present disclosure is for solving the above-described problem, and is intended to provide an error correction encoding device capable of reducing the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing.

SOLUTION TO PROBLEM

[0010] An error correction encoding device according

to the present disclosure includes: an input information acquiring unit to acquire input information; an encoding unit to generate soft decision error correction frame information including a bit array of m rows and N columns on the basis of the input information acquired by the input information acquiring unit, the bit array being obtained by combining first bit string group information and second bit string group information, the first bit string group information including a bit array of m rows and N1 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol by using a predetermined first symbol mapping rule, the second bit string group information including a bit array of m rows and N2 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol by using a predetermined second symbol mapping rule, where m is a natural number of greater than or equal to 2, N1 is a natural number of greater than or equal to 2, N2 is a natural number of greater than or equal to 1, and N is a number obtained by adding N1 and N2 together; a modulation symbol conversion unit to generate modulation symbol group information including N pieces of the modulation symbols by performing pulse amplitude modulation of a combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit into the modulation symbol for each column of the soft decision error correction frame information by using the first symbol mapping rule or the second symbol mapping rule; and a transmission waveform shaping unit to generate a digital baseband modulation signal on the basis of the modulation symbol group information generated by the modulation symbol conversion unit and output the digital baseband modulation signal generated, wherein the encoding unit generates the soft decision error correction frame information by: generating first input bit array information including a bit array of m - 1 rows and N columns and second input bit array information including a bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit, where N3 is a natural number of greater than or equal to 1 and less than N1; storing the second input bit array information generated as a part of first MSB information including a bit array of one row and N1 columns in a predetermined area of a first row in the first bit string group information; generating shaped bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping encoding processing on the first input bit array information generated; generating first group bit array information including a combination of N1 predetermined columns and second group bit array information including a combination of N2 predetermined columns by separating the shaped bit array information generated; generating first LSB information including a bit array of one row and N1 columns by extracting, from the first group bit array information generated, a bit array of the (m - 1)-th row in the first group bit array information, generating inverted first LSB information including a bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in information of the first row in the first bit string group information after storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in the m-th row in the first bit string group information; generating second LSB information including a bit array of one row and N2 columns by extracting a bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated, and storing the second LSB information generated in the m-th row in the second bit string group information; generating a soft decision parity bit by performing systematic soft decision error correction encoding processing by using the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in the first row in the second bit string group information as second MSB information including a bit array of one row and N2 columns; in a case where m is greater than or equal to 3, generating first SSB information including a bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated, the first row to the (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in a second row to the (m - 1)-th row in the first bit string group information; and in the case where m is greater than or equal to 3, generating second SSB information including a bit array of m - 2 rows and N2 columns by extracting, from the second group bit array information generated, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the second row to the (m - 1)-th row in the second bit string group information.

ADVANTAGEOUS EFFECTS OF INVENTION

[0011] According to the present disclosure, the number of bits to be protected by the soft decision error correction can be reduced as compared with the conventional soft decision error correction encoding processing.

BRIEF DESCRIPTION OF DRAWINGS

[0012]

FIG. 1 is a configuration diagram illustrating an example of a configuration of a main part of a communication system according to a first embodiment.

FIG. 2 is a configuration diagram illustrating an example of a configuration of a main part of an error

correction encoding device according to the first embodiment.

FIG. 3 is a configuration diagram illustrating an example of a configuration of a main part of an encoding unit according to the first embodiment.

FIG. 4A is an explanatory diagram for describing an example of a first symbol mapping rule according to the first embodiment.

FIG. 4B is an explanatory diagram for describing an example of a second symbol mapping rule according to the first embodiment.

FIGS. 5A and 5B are diagrams illustrating examples of a hardware configuration of the error correction encoding device according to the first embodiment.

FIG. 6A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device according to the first embodiment.

FIG. 6B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the first embodiment.

FIG. 6C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the first embodiment.

FIG. 7 is a configuration diagram illustrating an example of a configuration of a main part of an error correction device according to the first embodiment.

FIG. 8 is a configuration diagram illustrating an example of a configuration of a main part of a decoding unit according to the first embodiment.

FIGS. 9A and 9B are diagrams illustrating examples of a hardware configuration of the error correction device according to the first embodiment.

FIG. 10A is a part of a flowchart illustrating an example of processing performed by the error correction device according to the first embodiment.

FIG. 10B is another part of the flowchart illustrating the example of the processing performed by the error correction device according to the first embodiment.

FIG. 10C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device according to the first embodiment.

FIG. 11 is a configuration diagram illustrating an example of a configuration of a main part of a communication system according to a second embodiment.

FIG. 12 is a configuration diagram illustrating an example of a configuration of a main part of an error correction encoding device according to the second embodiment.

FIG. 13 is a configuration diagram illustrating an example of a configuration of a main part of an encoding unit according to the second embodiment.

FIG. 14A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device according to the second embodiment.

FIG. 14B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the second embodiment.

FIG. 14C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the second embodiment.

FIG. 15 is a configuration diagram illustrating an example of a configuration of a main part of an error correction device according to the second embodiment.

FIG. 16 is a configuration diagram illustrating an example of a configuration of a main part of a decoding unit according to the second embodiment.

FIG. 17A is a part of a flowchart illustrating an example of processing performed by the error correction device according to the second embodiment.

FIG. 17B is another part of the flowchart illustrating the example of the processing performed by the error correction device according to the second embodiment.

FIG. 17C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device according to the second embodiment.

FIG. 18 is a configuration diagram illustrating an example of a configuration of a main part of a communication system according to a third embodiment.

FIG. 19 is a configuration diagram illustrating an example of a configuration of a main part of an error correction encoding device according to the third embodiment.

FIG. 20 is a configuration diagram illustrating an example of a configuration of a main part of an encoding unit according to the third embodiment.

FIG. 21Ais a part of a flowchart illustrating an example of processing performed by the error correction encoding device according to the third embodiment.

FIG. 21B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the third embodiment.

FIG. 21C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the third embodiment.

FIG. 22 is a configuration diagram illustrating an example of a configuration of a main part of an error correction device according to the third embodiment.

FIG. 23 is a configuration diagram illustrating an example of a configuration of a main part of a decoding unit according to the third embodiment.

FIG. 24A is a part of a flowchart illustrating an example of processing performed by the error correction device according to the third embodiment.

FIG. 24B is another part of the flowchart illustrating the example of the processing performed by the error

correction device according to the third embodiment.
FIG. 24C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device according to the third embodiment.
FIG. 25A is an explanatory diagram illustrating an example of a bit array space in which soft decision error correction frame information before an interleaving unit according to the third embodiment performs switching is stored.
FIG. 25B is an explanatory diagram illustrating an example of the bit array space in which soft decision error correction frame information after the interleaving unit according to the third embodiment performs switching is stored.
FIG. 26A is an explanatory diagram illustrating an example of modulation symbol group information in a case where the error correction encoding device according to the third embodiment does not include the interleaving unit.
FIG. 26B is an explanatory diagram illustrating an example of the modulation symbol group information in a case where the error correction encoding device according to the third embodiment includes the interleaving unit.
FIG. 27A is an explanatory diagram illustrating an example of a bit array space in which soft decision error correction frame information before an LSB interleaving unit according to the third embodiment performs switching is stored.
FIG. 27B is an explanatory diagram illustrating an example of the bit array space in which soft decision error correction frame information after the LSB interleaving unit according to the third embodiment performs switching is stored.
FIG. 28 is a configuration diagram illustrating an example of a configuration of a main part of a communication system according to a modification of the first embodiment.
FIG. 29 is a configuration diagram illustrating an example of a configuration of a main part of an error correction encoding device according to the modification of the first embodiment.
FIG. 30 is a configuration diagram illustrating an example of a configuration of a main part of an encoding unit according to the modification of the first embodiment.
FIG. 31A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device according to the modification of the first embodiment.
FIG. 31B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the modification of the first embodiment.
FIG. 31C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the modification of the first embodiment.
FIG. 32 is a configuration diagram illustrating an example of a configuration of a main part of an error correction device according to the modification of the first embodiment.
FIG. 33 is a configuration diagram illustrating an example of a configuration of a main part of a decoding unit according to the modification of the first embodiment.
FIG. 34A is a part of a flowchart illustrating an example of processing performed by the error correction device according to the modification of the first embodiment.
FIG. 34B is another part of the flowchart illustrating the example of the processing performed by the error correction device according to the modification of the first embodiment.
FIG. 34C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device according to the modification of the first embodiment.
FIG. 35 is a configuration diagram illustrating an example of a configuration of a main part of a communication system according to a modification of the second embodiment.
FIG. 36 is a configuration diagram illustrating an example of a configuration of a main part of an error correction encoding device according to the modification of the second embodiment.
FIG. 37 is a configuration diagram illustrating an example of a configuration of a main part of an encoding unit according to the modification of the second embodiment.
FIG. 38A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device according to the modification of the second embodiment.
FIG. 38B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the modification of the second embodiment.
FIG. 38C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device according to the modification of the second embodiment.
FIG. 39 is a configuration diagram illustrating an example of a configuration of a main part of an error correction device according to the modification of the second embodiment.
FIG. 40 is a configuration diagram illustrating an example of a configuration of a main part of a decoding unit according to the modification of the second embodiment.
FIG. 41Ais a part of a flowchart illustrating an example of processing performed by the error correction device according to the modification of the second embodiment.
FIG. 41B is another part of the flowchart illustrating

the example of the processing performed by the error correction device according to the modification of the second embodiment.

FIG. 41C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device according to the modification of the second embodiment.

DESCRIPTION OF EMBODIMENTS

[0013] Hereinafter, to explain the present disclosure in more detail, embodiments for carrying out the present disclosure will be described with reference to the accompanying drawings.

First Embodiment.

[0014] A configuration of a main part of a communication system 1 according to a first embodiment will be described with reference to FIG. 1.

[0015] FIG. 1 is a configuration diagram illustrating an example of the configuration of the main part of the communication system 1 according to the first embodiment.

[0016] In the first embodiment, as an example, the communication system 1 is described as an optical communication system, but the optical communication system is merely an example, and the communication system 1 is not limited to the optical communication system. For example, the communication system 1 may be a communication system by wireless communication, metal communication, or the like.

[0017] The communication system 1 includes a transmission device 10, a transmission path 30, and a reception device 20.

[0018] The transmission device 10 acquires input information and outputs a signal based on the acquired input information. Since the communication system 1 illustrated in FIG. 1 is the optical communication system, the transmission device 10 illustrated in FIG. 1 is an optical transmission device to output an optical signal.

[0019] The transmission path 30 transmits the signal output by the transmission device 10 to the reception device 20. Since the communication system 1 illustrated in FIG. 1 is the optical communication system, the transmission path 30 illustrated in FIG. 1 is an optical transmission path capable of transmitting the optical signal output by the transmission device 10 to the reception device 20. The transmission path 30 includes, for example, an optical cross-connect device, a transmission optical fiber, and an optical amplifier, all of which are not illustrated. The optical cross-connect device includes a wavelength selective switch, a wavelength multiplexing device, a wavelength separation device, an optical coupler, or the like. The transmission optical fiber includes a single-core single-mode fiber, a spatial multiplexing fiber, or the like. The optical amplifier includes an erbium-doped optical amplifier, a Raman optical amplifier, or the like.

[0020] The reception device 20 receives the signal output by the transmission device 10 via the transmission path 30, generates output information corresponding to the input information on the basis of the signal, and outputs the generated output information. Since the communication system 1 illustrated in FIG. 1 is the optical communication system, the reception device 20 illustrated in FIG. 1 is an optical reception device to receive the optical signal.

[0021] The transmission device 10 includes an error correction encoding device 100, a D/A converter 11, a transmission light source 12, and an optical modulator 13. The D/A converter 11, the transmission light source 12, and the optical modulator 13 constitute a transmission unit.

[0022] The error correction encoding device 100 acquires the input information input from the outside of the device, and generates a digital baseband modulation signal on the basis of the acquired input information. The error correction encoding device 100 outputs the generated digital baseband modulation signal to the D/A converter 11.

[0023] The D/A converter 11 receives the digital baseband modulation signal output from the error correction encoding device 100, converts the digital baseband modulation signal into a transmission electrical signal that is an analog baseband modulation signal, and outputs the transmission electrical signal after conversion. The D/A converter 11 may convert the digital baseband modulation signal into the analog baseband modulation signal, electrically amplify the analog baseband modulation signal, and output an amplified analog baseband modulation signal as the transmission electrical signal.

[0024] The transmission light source 12 outputs unmodulated light having a single wavelength. The transmission light source 12 includes an external resonator type wavelength tunable light source or the like. The transmission light source 12 generates, for example, unmodulated light having a center wavelength of 1550 nanometers (Hereinafter, it is denoted as "nm".), and outputs the generated unmodulated light to the optical modulator 13.

[0025] The optical modulator 13 receives the transmission electrical signal output by the D/A converter 11 and the unmodulated light output by the transmission light source 12, modulates the unmodulated light with the transmission electrical signal to generate modulated light, and outputs the generated modulated light to the transmission path 30 as a modulated optical signal. The optical modulator 13 includes a polarization multiplexing quadrature phase modulator or the like.

[0026] The reception device 20 includes a reception light source 22, an optical receiver 21, an A/D converter 23, and an error correction device 200. The reception light source 22, the optical receiver 21, and the A/D converter 23 constitute a reception unit.

[0027] The reception light source 22 outputs unmodulated light having a single wavelength corresponding to

the center wavelength of the modulated light that is the modulated optical signal output from the transmission device 10 to the transmission path 30. The reception light source 22 includes an external resonator type wavelength tunable light source or the like, generates unmodulated light having a center wavelength of 1550 nm, for example, and outputs the generated unmodulated light to the optical receiver 21.

[0028] The optical receiver 21 receives the modulated optical signal output by the transmission device 10 to the transmission path 30 and the unmodulated light output by the reception light source 22. The optical receiver 21 generates a reception electrical signal that is a reception analog baseband modulation signal by performing coherent detection using the modulated light that is modulated optical signal, and unmodulated light, and outputs the generated reception electrical signal to the A/D converter 23.

[0029] The A/D converter 23 receives the reception electrical signal output by the optical receiver 21, converts the reception electrical signal into a reception digital baseband modulation signal, and outputs the reception digital baseband modulation signal after conversion. Specifically, the A/D converter 23 samples the reception analog baseband modulation signal that is the reception electrical signal, converts the signal into the digital baseband modulation signal, and outputs the digital baseband modulation signal to the error correction device 200. The A/D converter 23 may amplify the reception electrical signal and convert an amplified reception electrical signal into the reception digital baseband modulation signal.

[0030] The error correction device 200 receives the reception digital baseband modulation signal output by the A/D converter 23, generates the output information corresponding to the input information on the basis of the reception digital baseband modulation signal, and outputs the generated output information.

[0031] A configuration of a main part of the error correction encoding device 100 according to the first embodiment will be described with reference to FIG. 2.

[0032] FIG. 2 is a configuration diagram illustrating an example of the configuration of the main part of the error correction encoding device 100 according to the first embodiment.

[0033] The error correction encoding device 100 includes an input information acquiring unit 110, an encoding unit 120, a modulation symbol conversion unit 130, and a transmission waveform shaping unit 140.

[0034] The input information acquiring unit 110 acquires input information.

[0035] The encoding unit 120 generates soft decision error correction frame information obtained by combining first bit string group information and second bit string group information on the basis of the input information acquired by the input information acquiring unit 110.

[0036] The first bit string group information is information including a bit array of m (m is a natural number of greater than or equal to 2) rows and N1 (N1 is a natural number of greater than or equal to 2) columns, and is information in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol by using a predetermined first symbol mapping rule.

[0037] The second bit string group information is information including a bit array of m rows and an N2 (N2 is a natural number of greater than or equal to 1) column, and is information in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol by using a predetermined second symbol mapping rule.

[0038] The soft decision error correction frame information is information obtained by combining the first bit string group information and the second bit string group information, and is information including a bit array of m rows and N columns (N is a number obtained by adding N1 and N2 together).

[0039] Details of the encoding unit 120 will be described later.

[0040] In the following description, it is assumed that the soft decision error correction frame information is stored in "D" that is a bit array space of m rows and N columns.

[0041] In addition, in D that is a bit array space, a bit array space of m rows and N1 columns in which the first bit string group information is stored is denoted as "Dd[1]", and a bit array space of m rows and N2 columns in which the second bit string group information is stored is denoted as "Dd[2]".

[0042] In addition, in the following description, q - p + 1 elements from p (p is a natural number of greater than or equal to 1) to q (q is a natural number of greater than or equal to p) are denoted as "p : q".

[0043] In addition, in Dd[1 : m] that is a bit array space, a bit array space of one row and N columns in which the most significant bit (MSB) is stored is denoted as "Dv[1][1 : 2]". In the following description, information stored in Dv[1][1] is referred to as first MSB information, and information stored in Dv[1][2] is referred to as second MSB information.

[0044] In addition, in Dd[1 : m] that is a bit array space, a bit array space of one row and N columns in which the least significant bit (LSB) is stored is denoted as "Dv[m][1 : 2]". In the following description, information stored in Dv[m][1] is referred to as first LSB information, and information stored in Dv[m][2] is referred to as second LSB information.

[0045] In addition, in Dd[1 : m] that is a bit array space, a bit array space of m - 2 rows and N columns in which a middle bit other than the MSB and the LSB is stored is denoted as "Dv[2 : m - 1][1 : 2]". In the following description, information stored in Dv[2 : m - 1][1] is referred to as first SSB information, and information stored in Dv[2 : m - 1][2] is referred to as second SSB information.

[0046] Note that, in a case where m is 2, the first bit

string group information includes only the first MSB information and the first LSB information, and the second bit string group information includes only the second MSB information and the second LSB information. Thus, in the case where m is 2, since the first SSB information and the second SSB information do not exist, Dv[2 : m - 1][1 : 2] is omitted.

[0047] In addition, in Dd[1 : m] that is a bit array space, a bit space of the k-th (k is a natural number of greater than or equal to 1 and less than or equal to N1 in Dd[1], and is a natural number of greater than or equal to 1 and less than or equal to N2 in Dd[2]) column is denoted as "D[1 : m][1 : 2][k]".

[0048] In addition, a bit value of the soft decision error correction frame information stored in D[1 : m][1 : 2][k] that is a bit space is denoted as "B[1 : m][1 : 2][k]".

[0049] The modulation symbol conversion unit 130 performs pulse amplitude modulation of a combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit 120 into a modulation symbol for each column of the soft decision error correction frame information, by using the first symbol mapping rule or the second symbol mapping rule. The modulation symbol conversion unit 130 generates modulation symbol group information including N modulation symbols by performing pulse amplitude modulation for each column of the soft decision error correction frame information.

[0050] Specifically, for example, the modulation symbol conversion unit 130 includes a first symbol mapping unit 131 and a second symbol mapping unit 132.

[0051] The first symbol mapping unit 131 performs pulse amplitude modulation of a combination of bit values of each column of the first bit string group information in the soft decision error correction frame information generated by the encoding unit 120 into a modulation symbol for each column of the first bit string group information, by using the predetermined first symbol mapping rule. The first symbol mapping unit 131 generates first modulation symbol group information including N1 modulation symbols by performing pulse amplitude modulation for each column of the first bit string group information.

[0052] The second symbol mapping unit 132 performs pulse amplitude modulation of a combination of bit values of each column of the second bit string group information in the soft decision error correction frame information generated by the encoding unit 120 into a modulation symbol for each column of the second bit string group information, by using the predetermined second symbol mapping rule. The second symbol mapping unit 132 generates second modulation symbol group information including N2 modulation symbols by performing pulse amplitude modulation for each column of the second bit string group information.

[0053] In the following description, a modulation symbol after the pulse amplitude modulation is referred to as a pulse-amplitude modulation (PAM) symbol.

[0054] In addition, the modulation symbol group information generated by the modulation symbol conversion unit 130 is denoted as [X], the first modulation symbol group information is denoted as "Xv[1]", and the second modulation symbol group information is denoted as "Xv[2]".

[0055] In addition, among PAM symbols belonging to Xv[1] that is the first modulation symbol group information, a PAM symbol corresponding to B[1 : m][1][k] that is a combination of bit values of the k-th column of the first bit string group information is denoted as "X[1][k]".

[0056] In addition, among PAM symbols belonging to Xv[2] that is the second modulation symbol group information, a PAM symbol corresponding to B[1 : m][2][k] that is a combination of bit values of the k-th column of the second bit string group information is denoted as "X[2][k]".

[0057] That is, the first symbol mapping unit 131 converts B[1 : m][1][k] that is a combination of bit values of the k-th row of the first bit string group information into X[1][k] by using the first symbol mapping rule, and the second symbol mapping unit 132 converts B[1 : m][2][k] that is a combination of bit values of the k-th row of the second bit string group information into X[2][k] by using the second symbol mapping rule, whereby the modulation symbol conversion unit 130 generates modulation symbol group information including N PAM symbols.

[0058] Details of the first symbol mapping rule and the second symbol mapping rule will be described later.

[0059] The transmission waveform shaping unit 140 generates a digital baseband modulation signal on the basis of the modulation symbol group information including the N PAM symbols generated by the modulation symbol conversion unit 130, and outputs the generated digital baseband modulation signal to the D/A converter 11.

[0060] Specifically, for example, the transmission waveform shaping unit 140 includes a polarization multiplexing unit 141 and a transmission digital signal generating unit 142.

[0061] The polarization multiplexing unit 141 generates polarization multiplexing modulation symbols (Hereinafter, the symbol is referred to as a "quadrature amplitude modulation (QAM) symbol".) on the basis of the modulation symbol group information generated by the modulation symbol conversion unit 130.

[0062] Specifically, for example, the polarization multiplexing unit 141 generates the QAM symbol by performing quadrature amplitude modulation on X[1][1 : N1] that is the first modulation symbol group information and X[2][1 : N2] that is the first modulation symbol group information on the basis of the modulation symbol group information generated by the modulation symbol conversion unit 130.

[0063] Note that, a method of performing quadrature amplitude modulation processing is known, and thus detailed description of the method will be omitted.

[0064] The transmission digital signal generating unit 142 generates a digital baseband modulation signal

based on the polarization multiplexing modulation symbol generated by the polarization multiplexing unit 141. The transmission digital signal generating unit 142 outputs the generated digital baseband modulation signal.

[0065] Note that, a method of generating a digital baseband modulation signal based on a QAM symbol is known, and thus detailed description of the method will be omitted.

[0066] Specifically, the transmission digital signal generating unit 142 outputs the digital baseband modulation signal generated on the basis of the QAM symbol to the D/A converter 11.

[0067] When generating the digital baseband modulation signal, the transmission digital signal generating unit 142 may perform up-sampling such as double up-sampling, or processing such as root raised cosine low-pass filtering. In addition, when generating the digital baseband modulation signal, the transmission digital signal generating unit 142 may perform band compensation, delay difference compensation, amplitude adjustment, or the like for the optical modulator 13, the transmission path 30, the optical receiver 21, or the like.

[0068] Note that, a processing method for up-sampling, root raised cosine low-pass filtering, band compensation, delay difference compensation, amplitude adjustment, or the like performed when the digital baseband modulation signal is generated on the basis of the QAM symbol is known, and thus detailed description of the method will be omitted.

[0069] For example, in a case where the transmission path 30 has a noise characteristic such as additive white Gaussian noise (Hereinafter, it is referred to as "additive white Gaussian noise (AWGN)".), a signal such as a modulated optical signal transmitted via the transmission path 30 needs to have a signal to noise ratio (Hereinafter, it is referred to as a "signal-to-noise ratio (SNR)".) necessary for obtaining desired communication quality. When generating the digital baseband modulation signal, to generate a signal having a desired SNR, the transmission digital signal generating unit 142 shapes the QAM symbol by adjusting a value of the QAM symbol so that an absolute value of the QAM symbol has a distribution close to a predetermined distribution such as a discrete Gaussian distribution.

[0070] Note that, the discrete Gaussian distribution is merely an example, and when generating the digital baseband modulation signal, the transmission digital signal generating unit 142 only needs to adjust the value of the QAM symbol so that the QAM symbol has a distribution conforming to a noise characteristic of the transmission path 30, and a method of adjusting the value of the QAM symbol by the transmission digital signal generating unit 142 is not limited to the method in which the QAM symbol is adjusted to have a distribution close to the discrete Gaussian distribution.

[0071] As described above, the error correction encoding device 100 acquires the input information input from the outside of the device, and generates the soft decision error correction frame information on the basis of the acquired input information. Further, the error correction encoding device 100 generates the digital baseband modulation signal based on the generated soft decision error correction frame information, and outputs the generated digital baseband modulation signal to the D/A converter 11.

[0072] In addition, the transmission device 10 converts the digital baseband modulation signal generated on the basis of the soft decision error correction frame information based on the input information into the modulated light that is the modulated optical signal via the D/A converter 11 and the optical modulator 13, and outputs the modulated light to the reception device 20.

[0073] A configuration of a main part of the encoding unit 120 according to the first embodiment will be described with reference to FIG. 3.

[0074] FIG. 3 is a configuration diagram illustrating an example of the main part of the encoding unit 120 according to the first embodiment.

[0075] The encoding unit 120 includes an input bit array information generating unit 121, a probability distribution shaping encoding unit 122, a bit inversion unit 123, and a soft decision error correction encoding unit 124.

[0076] On the basis of the input information acquired by the input information acquiring unit 110, the input bit array information generating unit 121 generates first input bit array information including a bit array of m - 1 rows and N columns and second input bit array information including a bit array of one row and N3 (N3 is a natural number of greater than or equal to 1 and less than N1) columns.

[0077] In a case where the input information is information including the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns, the input bit array information generating unit 121 generates the first input bit array information and the second input bit array information by extracting each of the first input bit array information and the second input bit array information from the input information, or separating the input information into the first input bit array information and the second input bit array information.

[0078] In a case where the input information is information corresponding to the first input bit array information and the information includes information of the number of bits less than $(m - 1) \times N$, the input bit array information generating unit 121 may generate the first input bit array information by extracting the information from the input information and shaping the extracted information into a bit array of m - 1 rows and N columns. For example, when shaping the information into the bit array of m - 1 rows and N columns, the input bit array information generating unit 121 generates the first input bit array information by setting a part of bit values in the bit array of m - 1 rows and N columns as the information and setting remaining bit values to predetermined values

(for example, "0").

[0079] In a case where the input information is information corresponding to the second input bit array information and the information includes information of the number of bits less than N3, the input bit array information generating unit 121 may generate the second input bit array information by extracting the information from the input information and shaping the extracted information into a bit array of one row and N3 columns. For example, when shaping the information into the bit array of one row and N3 columns, the input bit array information generating unit 121 generates the second input bit array information by setting a part of bit values in the bit array of one row and N3 columns as the information and setting remaining bit values to predetermined values (for example, "0").

[0080] In a case where the input information does not include the information corresponding to the first input bit array information or the second input bit array information, the input bit array information generating unit 121 may generate the first input bit array information or the second input bit array information not included in the input information by setting all the bit values of the first input bit array information or the second input bit array information not included in the input information to predetermined values (for example, "0").

[0081] In a case where the input information is information corresponding to the first input bit array information and the information includes information of the number of bits greater than $(m - 1) \times N$, the input bit array information generating unit 121 may divide the information into a plurality of pieces of the first input bit array information having the number of bits of less than or equal to $(m - 1) \times N$. For example, the error correction encoding device 100 generates a plurality of pieces of soft decision error correction frame information each corresponding to the plurality of pieces of first input bit array information divided, generates a plurality of digital baseband modulation signals each corresponding to the plurality of pieces of soft decision error correction frame information, and sequentially outputs the plurality of digital baseband modulation signals generated.

[0082] In a case where the input information is information corresponding to the second input bit array information and the information includes information of the number of bits greater than N3, the input bit array information generating unit 121 may divide the information into a plurality of pieces of the second input bit array information having the number of bits of less than or equal to N3. For example, the error correction encoding device 100 generates a plurality of pieces of soft decision error correction frame information each corresponding to the plurality of pieces of second input bit array information divided, generates a plurality of digital baseband modulation signals each corresponding to the plurality of pieces of soft decision error correction frame information, and sequentially outputs the plurality of digital baseband modulation signals generated.

[0083] With the above configuration, the error correction encoding device 100 can generate the soft decision error correction frame information for the input information having any number of bits and output the digital baseband modulation signal based on the generated soft decision error correction frame information.

[0084] The input bit array information generating unit 121 stores the generated second input bit array information as a part of the first MSB information including a bit array of one row and N1 columns in a predetermined area (Hereinafter, the area is referred to as a "second input bit area".) of the first row in the first bit string group information.

[0085] Specifically, the input bit array information generating unit 121 stores the second input bit array information in the second input bit area of Dv[1][1] that is a bit array space in which the first MSB is stored. Hereinafter, the description will be given assuming that the second input bit area is D[1][1][1 : N3].

[0086] The probability distribution shaping encoding unit 122 generates shaped bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping encoding processing on the generated first input bit array information.

[0087] The probability distribution shaping encoding unit 122 may collectively perform the probability distribution shaping encoding processing on the first input bit array information, or may divide the first input bit array information into a plurality of pieces of information and perform the probability distribution shaping encoding processing on each divided piece of information.

[0088] The probability distribution shaping encoding unit 122 performs the probability distribution shaping encoding processing by using, for example, a method described in "Hierarchical Distribution Matching for Probabilistically Shaped Coded Modulation" (Journal of Lightwave Technology, vol. 37, no. 6, pp. 1579-1589, March 2019.) by T. Yoshida et al.

[0089] The probability distribution shaping encoding unit 122 stores the generated shaped bit array information in Dv[2 : m][1 : 2] in D that is a bit array space.

[0090] Specifically, for example, the probability distribution shaping encoding unit 122 generates the first LSB information, the second LSB information, the first SSB information, and the second SSB information by performing processing as described below. The probability distribution shaping encoding unit 122 stores the shaped bit array information in Dv[2 : m][1 : 2] by storing the generated first LSB information, second LSB information, first SSB information, and second SSB information in areas in Dv[2 : m][1 : 2] respectively corresponding to the first LSB information, the second LSB information, the first SSB information, and the second SSB information.

[0091] First, the probability distribution shaping encoding unit 122 generates first group bit array information including a combination of N1 predetermined columns and second group bit array information including a combination of N2 predetermined columns by separating the

generated shaped bit array information.

[0092] Further, the probability distribution shaping encoding unit 122 generates the first LSB information including a bit array of one row and N1 columns by extracting information of the (m - 1)-th row in the first group bit array information from the generated first group bit array information, and stores the first LSB information in the m-th row in the first bit string group information.

[0093] Specifically, the probability distribution shaping encoding unit 122 stores the generated first LSB information in Dv[m][1] that is a bit array space.

[0094] In addition, the probability distribution shaping encoding unit 122 generates the second LSB information including a bit array of one row and N2 columns by extracting information of the (m - 1)-th row in the second group bit array information from the generated second group bit array information, and stores the generated second LSB information in the m-th row in the second bit string group information.

[0095] Specifically, the probability distribution shaping encoding unit 122 stores the generated second LSB information in Dv[m][2] that is a bit array space.

[0096] In addition, in a case where m is greater than or equal to 3, the probability distribution shaping encoding unit 122 generates the first SSB information including a bit array of m - 2 rows and N1 columns by extracting information from the first row to the (m - 2)-th row in the first group bit array information from the generated first group bit array information, and stores the generated first SSB information from the second row to the (m - 1)-th row in the first bit string group information.

[0097] Specifically, the probability distribution shaping encoding unit 122 stores the generated first SSB information in Dv[2 : m - 1][1] that is a bit array space.

[0098] In addition, in the case where m is greater than or equal to 3, the probability distribution shaping encoding unit 122 generates the second SSB information including a bit array of m - 2 rows and N2 columns by extracting information from the first row to the (m - 2)-th row in the second group bit array information from the generated second group bit array information, and stores the generated second SSB information from the second row to the (m - 1)-th row in the second bit string group information.

[0099] Specifically, the probability distribution shaping encoding unit 122 stores the generated second SSB information in Dv[2 : m - 1][2] that is a bit array space.

[0100] The bit inversion unit 123 generates inverted first LSB information including a bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information and each bit values of each columns in the first MSB information, the columns in the first MSB information each corresponding to the columns in the first LSB information.

[0101] Specifically, the bit inversion unit 123 calculates an exclusive OR of B[m][1][k] that is a bit value of each column in Dv[m][1] storing the first LSB information and B[1][1][k] that is a bit value of each column in Dv[1][1] storing the second input bit array information. The bit inversion unit 123 stores the inverted first LSB information that is a calculation result of the exclusive OR of all the columns from the first column to the N1-th column, in the m-th row in the first bit string group information. Specifically, the bit inversion unit 123 stores the inverted first LSB information that is the calculation result of the exclusive OR in Dv[m][1] storing the first LSB information, and overwrites B[m][1][1 : N1] with the inverted first LSB information.

[0102] The soft decision error correction encoding unit 124 generates a soft decision parity bit by performing systematic soft decision error correction encoding processing by using the inverted first LSB information generated by the bit inversion unit 123 and the second LSB information generated by the probability distribution shaping encoding unit 122. The soft decision error correction encoding unit 124 stores the generated soft decision parity bit as second MSB information including a bit array of one row and N2 columns in the first row of the second bit string group information.

[0103] Specifically, the soft decision error correction encoding unit 124 generates the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using B[m][1][1 : N1] that is a bit value of each column in Dv[m][1] storing the inverted first LSB information and B[m][2][1 : N2] that is a bit value of each column in Dv[m][2] storing the second LSB information. The soft decision error correction encoding unit 124 stores the generated soft decision parity bit as the second MSB information in Dv[1][2] that is a bit array space.

[0104] As the systematic soft decision error correction encoding processing, a turbo product code, a low density parity check code, a polar code, or the like is used.

[0105] With the above configuration, the encoding unit 120 generates the soft decision error correction frame information by storing the soft decision error correction frame information in Dv[1 : m][1 : 2] that is a bit array space.

[0106] As described above, the encoding unit 120 performs the systematic soft decision error correction encoding processing by using the bit value of each column in Dv[m][1] and the bit value of each column in Dv[m][2]. For that reason, a bit to be protected by the soft decision error correction encoding processing is only the least significant bit of each column in Dd[1 : 2] in the soft decision error correction frame information.

[0107] Thus, the encoding unit 120 can reduce the number of bits to be protected by soft decision error correction as compared with the conventional soft decision error correction encoding processing.

[0108] The first symbol mapping rule and the second symbol mapping rule according to the first embodiment will be described with reference to FIG. 4.

[0109] FIG. 4A is an explanatory diagram for describing an example of the first symbol mapping rule according to the first embodiment. Specifically, FIG. 4A is a diagram

illustrating a correspondence between B[1 : m][1][k] that is a combination of bit values of D[1 : m][1][k] that is a bit array space and X[1][k] that is a PAM symbol. Hereinafter, a correspondence between a combination of B[1 : m][1][k] and X[1][k] that is a PAM symbol will be referred to as the first symbol mapping rule and described.

[0110] FIG. 4B is an explanatory diagram for describing an example of the second symbol mapping rule according to the first embodiment. Specifically, FIG. 4B is a diagram illustrating a correspondence between B[1 : m][2][k] that is a combination of bit values of D[1 : m][2][k] that is a bit array space and X[2][k] that is a PAM symbol. Hereinafter, a correspondence between a combination of B[1 : m][2][k] and X[2][k] that is a PAM symbol will be referred to as the second symbol mapping rule.

[0111] FIG. 4 illustrates, as an example, a case where m is 4, and a case where the modulation symbol conversion unit 130 performs 16-value pulse amplitude modulation (Hereinafter, it is referred to as "16-PAM: 16-ary PAM".) processing by using a combination of four bit values.

[0112] The modulation symbol conversion unit 130 performs one-dimensional pulse amplitude modulation on a combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit 120 into a modulation symbol for each column of the soft decision error correction frame information, by using the first symbol mapping rule or the second symbol mapping rule indicated in FIG. 4 as an example of the symbol mapping rule.

[0113] In the following description, it is assumed that modulation symbol conversion unit 130 performs 16-PAM processing by using a combination of four bit values as an example, but the modulation symbol conversion unit 130 is not limited thereto. That is, m only needs to be greater than or equal to 2, and the modulation symbol conversion unit 130 only needs to perform 2^m-value pulse amplitude modulation processing.

[0114] In the first symbol mapping rule indicated in FIG. 4A, the relationship between B[1 : m - 1][1][k] and X[1][k] is equivalent to the binary reflected Gray code (Hereinafter, it is referred to as "Binary Reflected Gray Coding (BRGC)".). In addition, the relationship between B[m][1][k] and X[1][k] is one in which values of B[m][1][k] each corresponding to two adjacent X[1][k] are different from each other.

[0115] On the other hand, in the second symbol mapping rule indicated in FIG. 4B, the relationship between B[1 : m - 1][2][k] and X[2][k] is equivalent to BRGC. In addition, the relationship between B[m][2][k] and X[2][k] is one in which B[m][2][k] corresponding to X[2][k] of a positive value has the same value as B[m][1][k] corresponding to X[1][k] having the same value as the value of X[2][k], and B[m][2][k] corresponding to X[2][k] of a negative value has a value obtained by inverting the value of B[m][1][k] corresponding to X[1][k] having the same value as the value of X[2][k].

[0116] Note that, the first symbol mapping rule and the second symbol mapping rule indicated in FIG. 4 are merely examples, and the first symbol mapping rule and the second symbol mapping rule are not limited to those indicated in FIG. 4. A combination of m bit values in the first symbol mapping rule and the second symbol mapping rule is any combination of m bit values as long as the first symbol mapping rule and the second symbol mapping rule are those described above, and a value of the PAM symbol is uniquely determined by the combination of m bit values.

[0117] As indicated in FIG. 4, in a case where the maximum value of the number of PAM symbols is 16, the number of PAM symbols can be set to 8 or 4. In other words, 16-PAM can be used as 8-PAM or 4-PAM

[0118] For example, in the case where m is greater than or equal to 3, in a case where the number of valid bits is me (me is a natural number of greater than or equal to 2 and less than or equal to m) among combinations of m bit values, the modulation symbol conversion unit 130 only needs to perform 2^{me}-value pulse amplitude modulation processing by using a combination of me bit values.

[0119] Specifically, for example, in a case where m is 4 and me is 3, by setting the value of B[2][1 : 2][k] among B[1 : m][1 : 2][k] indicated in FIG. 4 to "0", the modulation symbol conversion unit 130 can perform 2^3-value pulse amplitude modulation processing that can perform conversion into eight PAM symbols from -7 to 7, that is, 8-value pulse amplitude modulation processing.

[0120] In addition, for example, in a case where m is 4 and me is 2, by setting the value of B[2 : 3][1 : 2][k] among B[1 : m][1 : 2][k] indicated in FIG. 4 to "0", the modulation symbol conversion unit 130 can perform 2^2-value pulse amplitude modulation processing that can perform conversion into four PAM symbols from -3 to 3, that is, 4-value pulse amplitude modulation processing.

[0121] Note that, in a case where there is an invalid bit among the combinations of m bit values, for example, in a case where the value of B[2][1 : 2][k] or the value of B[2 : 3][1 : 2][k] described in the above example is set to "0", the probability distribution shaping encoding unit 122 included in the encoding unit 120 may set information corresponding to a row in which all the values are set to "0" in the first input bit array information to be out of a target of the probability distribution shaping encoding.

[0122] Regarding X[2][k], referring to the first symbol mapping rule and the second symbol mapping rule indicated in FIG. 4, if absolute values of amplitude values of X[2][k] are the same, combinations of bit values of B[2 : m][2][k] are the same, and B[1][2][k] indicates positive and negative polarities of X[2][k].

[0123] Thus, the probability distribution shaping encoding unit 122 performs the probability distribution shaping coding on information corresponding to B[2 : m][2][k] in the first input bit array information, whereby the error correction encoding device 100 can control an appearance probability of a combination of bit values of B[2 : m][2][k], that is, an appearance probability of an absolute value of X[2][k].

[0124] On the other hand, regarding X[1][k], referring to the first symbol mapping rule and the second symbol mapping rule indicated in FIG. 4, in a case where X[1][k] is a positive value, the combination of bit values of B[1 : m][1][k] corresponding to the value of X[1][k] is the same as the combination of bit values of B[1 : m][2][k] corresponding to X[2][k] having the same value as X[1][k]. In addition, in a case where X[1][k] is a negative value, regarding X[1][k], the combination of bit values of B[2 : m][1][k] corresponding to the value of X[1][k] and the combination of bit values of B[2 : m][2][k] corresponding to X[2][k] having the same value as X[1][k] are the same, and the bit value of B[1][1][k] corresponding to X[1][k] is a value obtained by inverting the bit value of B[1][2][k] corresponding to X[2][k] having the same value as X[1][k].

[0125] Thus, the probability distribution shaping encoding unit 122 performs the probability distribution shaping coding on information corresponding to B[2 : m][1][k] in the first input bit array information, and, further an exclusive OR of B[1][1][k] and B[m][1][k] after the probability distribution shaping coding by the bit inversion unit 123 is set as B[2 : m][1][k], whereby the error correction encoding device 100 can control an appearance probability of a combination of bit values of B[2 : m][1][k], that is, an appearance probability of an absolute value of X[1][k].

[0126] A hardware configuration of the main part of the error correction encoding device 100 according to the first embodiment will be described with reference to FIG. 5.

[0127] FIGS. 5A and 5B are diagrams illustrating examples of the hardware configuration of the error correction encoding device 100 according to the first embodiment.

[0128] As illustrated in FIG. 5A, the error correction encoding device 100 includes a computer, and the computer includes a processor 501 and a memory 502. The memory 502 stores a program for causing the computer to function as the input information acquiring unit 110, the encoding unit 120, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140. The processor 501 reads and executes the program stored in the memory 502, whereby functions of the input information acquiring unit 110, the encoding unit 120, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140 are implemented.

[0129] In addition, as illustrated in FIG. 5B, the error correction encoding device 100 may include a processing circuit 503. In this case, the functions of the input information acquiring unit 110, the encoding unit 120, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140 may be implemented by the processing circuit 503.

[0130] In addition, the error correction encoding device 100 may include the processor 501, the memory 502, and the processing circuit 503 (not illustrated). In this case, some of the functions of the input information acquiring unit 110, the encoding unit 120, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140 may be implemented by the processor 501 and the memory 502, and remaining functions may be implemented by the processing circuit 503.

[0131] The processor 501 uses, for example, a central processing unit (CPU), a graphics processing unit (GPU), a microprocessor, a microcontroller, or a digital signal processor (DSP).

[0132] The memory 502 uses, for example, a semiconductor memory or a magnetic disk. Specifically, the memory 502 uses, for example, a random access memory (RAM), a read only memory (ROM), a flash memory, an erasable programmable read only memory (EPROM), an electrically erasable programmable read only memory (EEPROM), a solid state drive (SSD), or a hard disk drive (HDD).

[0133] The processing circuit 503 uses, for example, an application specific integrated circuit (ASIC), a programmable logic device (PLD), a field-programmable gate array (FPGA), a system-on-a-chip (SoC), or a system large-scale integration (LSI).

[0134] Operation of the error correction encoding device 100 according to the first embodiment will be described with reference to FIGS. 6A, 6B, and 6C.

[0135] FIG. 6A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device 100 according to the first embodiment.

[0136] FIG. 6B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100 according to the first embodiment.

[0137] FIG. 6C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100 according to the first embodiment.

[0138] Hereinafter, FIGS. 6A, 6B, and 6C are collectively denoted as FIG. 6.

[0139] The error correction encoding device 100 repeatedly executes the processing of the flowchart illustrated in FIG. 6.

[0140] First, in step ST601, the input information acquiring unit 110 acquires the input information.

[0141] Next, in step ST610, the encoding unit 120 generates the soft decision error correction frame information.

[0142] Specifically, the encoding unit 120 performs processing of step ST610 by performing processing from step ST611 to step ST618 in processing A below.

[0143] First, in step ST611, the input bit array information generating unit 121 included in the encoding unit 120 generates the first input bit array information and the second input bit array information.

[0144] Next, in step ST612, the input bit array information generating unit 121 included in the encoding unit 120 stores the second input bit array information in the second input bit area of Dv[1][1].

[0145] Next, in step ST613, the probability distribution shaping encoding unit 122 included in the encoding unit

120 generates the shaped bit array information.

[0146] Next, in step ST614, the probability distribution shaping encoding unit 122 included in the encoding unit 120 stores the shaped bit array information in Dv[2 : m][1 : 2].

[0147] Next, in step ST615, the bit inversion unit 123 included in the encoding unit 120 calculates exclusive ORs of bit values of each columns in Dv[m][1] and bit values of each columns in Dv[1][1].

[0148] Next, in step ST616, the bit inversion unit 123 included in the encoding unit 120 stores calculation results of the exclusive ORs in Dv[m][1] by overwriting the bit values of each columns in Dv[m][1] with the calculation results of the exclusive ORs.

[0149] Next, in step ST617, the soft decision error correction encoding unit 124 included in the encoding unit 120 generates the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the bit value of each column in Dv[m][1] and the bit value of each column in Dv[m][2].

[0150] Next, in step ST618, the soft decision error correction encoding unit 124 included in the encoding unit 120 stores the soft decision parity bit in Dv[1][2].

[0151] After step ST618, the encoding unit 120 ends the processing A. That is, after step ST618, the encoding unit 120 ends the processing of step ST610.

[0152] After step ST610, in step ST620, the modulation symbol conversion unit 130 generates the modulation symbol group information including the N PAM symbols.

[0153] Specifically, the modulation symbol conversion unit 130 performs processing of step ST620 by performing processing from step ST621 to step ST622 in processing B below.

[0154] In step ST621, the first symbol mapping unit 131 included in the modulation symbol conversion unit 130 generates the first modulation symbol group information including N1 PAM symbols.

[0155] Next, in step ST622, the second symbol mapping unit 132 included in the modulation symbol conversion unit 130 generates the second modulation symbol group information including N2 PAM symbols.

[0156] After step ST622, the modulation symbol conversion unit 130 ends the processing B. That is, after step ST622, the modulation symbol conversion unit 130 ends the processing of step ST620.

[0157] Note that, the order of the processing in steps ST621 and ST622 is any order.

[0158] After step ST620, in step ST630, the transmission waveform shaping unit 140 outputs the digital baseband modulation signal.

[0159] Specifically, the transmission waveform shaping unit 140 performs processing of step ST630 by performing processing from step ST631 to step ST633 in processing C below.

[0160] In step ST631, the polarization multiplexing unit 141 included in the transmission waveform shaping unit 140 generates the QAM symbol.

[0161] Next, in step ST632, the transmission digital signal generating unit 142 included in the transmission waveform shaping unit 140 generates the digital baseband modulation signal.

[0162] Next, in step ST633, the transmission digital signal generating unit 142 included in the transmission waveform shaping unit 140 outputs the digital baseband modulation signal.

[0163] After step ST633, the transmission waveform shaping unit 140 ends the processing C. That is, after step ST633, the transmission waveform shaping unit 140 ends the processing of step ST630.

[0164] After step ST630, the error correction encoding device 100 ends the processing of the flowchart illustrated in FIG. 6, and the error correction encoding device 100 returns to the processing of step ST601 and repeatedly executes the processing of the flowchart illustrated in FIG. 6.

[0165] A configuration of a main part of the error correction device 200 according to the first embodiment will be described with reference to FIG. 7.

[0166] FIG. 7 is a configuration diagram illustrating an example of the main part of the error correction device 200 according to the first embodiment.

[0167] The error correction device 200 includes a reception modulation symbol group information generating unit 210, a hard decision candidate generating unit 220, a soft decision information generating unit 230, a decoding unit 240, and an information output unit 290.

[0168] The reception modulation symbol group information generating unit 210 receives the reception digital baseband modulation signal that is the digital baseband modulation signal output by the A/D converter 23. The reception modulation symbol group information generating unit 210 generates reception modulation symbol group information including N reception modulation symbols (Hereinafter, the symbol is referred to as a "reception PAM symbol".) that is modulation symbol group information including N modulation symbols, on the basis of the reception digital baseband modulation signal.

[0169] The reception digital baseband modulation signal received by the reception modulation symbol group information generating unit 210 is a signal corresponding to the digital baseband modulation signal output by the transmission waveform shaping unit 140 included in the error correction encoding device 100.

[0170] In addition, the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210 is information corresponding to the modulation symbol group information including the N modulation symbols generated by the modulation symbol conversion unit 130 included in the error correction encoding device 100.

[0171] That is, the reception modulation symbol group information generating unit 210 restores the reception modulation symbol group information corresponding to the modulation symbol group information generated by the modulation symbol conversion unit 130 on the basis of the reception digital baseband modulation signal.

[0172] The reception modulation symbol group information generating unit 210 outputs the generated reception modulation symbol group information to the hard decision candidate generating unit 220 and the soft decision information generating unit 230.

[0173] Specifically, for example, the reception modulation symbol group information generating unit 210 includes a reception polarization multiplexing symbol generating unit 211 and a reception modulation symbol generating unit 212.

[0174] The reception polarization multiplexing symbol generating unit 211 receives the reception digital baseband modulation signal output by the A/D converter 23, and generates a reception polarization multiplexing modulation symbol (Hereinafter, it is referred to as "reception QAM symbol".) that is the polarization multiplexing modulation symbol, from the reception digital baseband modulation signal.

[0175] The reception QAM symbol generated by the reception polarization multiplexing symbol generating unit 211 corresponds to the QAM symbol generated by the polarization multiplexing unit 141 included in the transmission waveform shaping unit 140 in the error correction encoding device 100.

[0176] That is, the reception polarization multiplexing symbol generating unit 211 restores the reception PAM symbol corresponding to the QAM symbol generated by the polarization multiplexing unit 141 from the reception digital baseband modulation signal.

[0177] Note that, a method of generating a QAM symbol from a digital baseband modulation signal is known, and thus detailed description of the method will be omitted.

[0178] The reception modulation symbol generating unit 212 generates reception modulation symbol group information including N reception PAM symbols on the basis of the reception QAM symbol restored by the reception polarization multiplexing symbol generating unit 211.

[0179] Specifically, the reception modulation symbol generating unit 212 generates first reception modulation symbol group information including N1 reception PAM symbols and second reception modulation symbol group information including N2 reception PAM symbols.

[0180] The first reception modulation symbol group information generated by the reception modulation symbol generating unit 212 is information corresponding to the first modulation symbol group information generated by the first symbol mapping unit 131 included in the modulation symbol conversion unit 130.

[0181] In addition, the second reception modulation symbol group information generated by the reception modulation symbol generating unit 212 is information corresponding to the second modulation symbol group information generated by the second symbol mapping unit 132 included in the modulation symbol conversion unit 130.

[0182] In the following description, the reception modulation symbol group information generated by the reception modulation symbol generating unit 212 is denoted as "Y", the first reception modulation symbol group information is denoted as "Yv[1]", and the second reception modulation symbol group information is denoted as "Yv[2]" .

[0183] In addition, among the reception PAM symbols belonging to Yv[1] that is the first reception modulation symbol group information, a reception PAM symbol corresponding to X[1][k] that is the PAM symbol belonging to the first modulation symbol group information generated by the first symbol mapping unit 131 is denoted as "Y[1][k]".

[0184] In addition, among the reception PAM symbols belonging to Yv[2] that is the second reception modulation symbol group information, a reception PAM symbol corresponding to X[2][k] that is the PAM symbol belonging to the second modulation symbol group information generated by the second symbol mapping unit 132 is denoted as "Y[2][k]".

[0185] The reception modulation symbol generating unit 212 outputs the generated first reception modulation symbol group information and second reception modulation symbol group information to the hard decision candidate generating unit 220 and the soft decision information generating unit 230.

[0186] Note that, a method of generating a PAM symbol from a QAM symbol is known, and thus detailed description of the method will be omitted.

[0187] The hard decision candidate generating unit 220 generates first hard decision candidate bit array information, second hard decision candidate bit array information, and third hard decision candidate bit array information by using the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210 on the basis of the first symbol mapping rule or the second symbol mapping rule.

[0188] Specifically, for example, the hard decision candidate generating unit 220 includes a first hard decision candidate generating unit 221 to generate the first hard decision candidate bit array information, a second hard decision candidate generating unit 222 to generate the second hard decision candidate bit array information, and a third hard decision candidate generating unit 223 to generate the third hard decision candidate bit array information.

[0189] The first hard decision candidate generating unit 221 generates HI0v[1][1] and HI1v[1][1] each of which is the first hard decision candidate bit array information including a bit array of one row and N1 columns, by using Y[1][1 : N1] that is the first reception modulation symbol group information, on the basis of the first symbol mapping rule.

[0190] A bit value of the k-th column of HI0v[1][1] is a hard decision value obtained by performing hard decision on a value of Y[1][k] in a case where the bit value of B[m][1][k] that is the LSB of B[1 : m][1][k] that is a com-

bination of bit values corresponding to X[1][k] corresponding to Y[1][k] is "0".

[0191] Specifically, for example, the first hard decision candidate generating unit 221 determines the bit value of the k-th column of HI0v[1][1] on the basis of the first symbol mapping rule indicated in FIG. 4A.

[0192] More specifically, in a case where the bit value of B[m][1][k] is "0", referring to the first symbol mapping rule indicated in FIG. 4A, X[1][k] can take any one of eight values of -15, -11, -7, -3, 1, 5, 9, and 13. The first hard decision candidate generating unit 221 compares the above-described eight values with the value of Y[1][k], and determines that the value of X[1][k] having the maximum posterior probability among the above-described eight values is the value of Y[1][k]. The first hard decision candidate generating unit 221 generates HI0v[1][1] by setting B[m][1][k] that is the LSB of B[1 : m][1][k] that is a combination of bit values corresponding to the value of X[1][k] having the maximum posterior probability as the bit value of the k-th column of HI0v[1][1].

[0193] Similarly, a bit value of the k-th column of H21v[1][1] is a hard decision value obtained by performing hard decision on the value of Y[1][k] in a case where the bit value of B[m][1][k] that is the LSB of B[1 : m][1][k] that is a combination of bit values corresponding to X[1][k] corresponding to Y[1][k] is "1".

[0194] Specifically, for example, the first hard decision candidate generating unit 221 determines the bit value of the k-th column of HI1v[1][1] on the basis of the first symbol mapping rule indicated in FIG. 4A.

[0195] More specifically, in a case where the bit value of B[m][1][k] is "1", referring to the first symbol mapping rule indicated in FIG. 4A, X[1][k] can take any one of eight values of -13, -9, -5, -1, 3, 7, 11, and 15. The first hard decision candidate generating unit 221 compares the above-described eight values with the value of Y[1][k], and determines that the value of X[1][k] having the maximum posterior probability among the above-described eight values is the value of Y[1][k]. The first hard decision candidate generating unit 221 generates HI1v[1][1] by setting B[m][1][k] that is the LSB of B[1 : m][1][k] that is a combination of bit values corresponding to the value of X[1][k] having the maximum posterior probability as the bit value of the k-th column of HI1v[1][1].

[0196] In the case where m is greater than or equal to 3, the second hard decision candidate generating unit 222 generates HI0v[2 : m - 1][1] and HI1v[2 : m - 1][1] each of which is hard decision candidate bit array information of m - 2 rows and N1 columns, by using Y[1][1 : N1] that is the first reception modulation symbol group information, on the basis of the first symbol mapping rule.

[0197] A bit value of the k-th column of HI0v[2 : m - 1][1] is a hard decision value obtained by performing hard decision on the value of Y[1][k] in a case where the bit value of B[m][1][k] that is the LSB of B[1 : m][1][k] that is a combination of bit values corresponding to X[1][k] corresponding to Y[1][k] is "0".

[0198] Specifically, for example, the second hard decision candidate generating unit 222 determines the bit value of the k-th column of HI0v[2 : m - 1][1] on the basis of the first symbol mapping rule indicated in FIG. 4A.

[0199] More specifically, in a case where the bit value of B[m][1][k] is "0", referring to the first symbol mapping rule indicated in FIG. 4A, X[1][k] can take any one of eight values of -15, -11, -7, -3, 1, 5, 9, and 13. The second hard decision candidate generating unit 222 compares the above-described eight values with the value of Y[1][k], and determines that the value of X[1][k] having the maximum posterior probability among the above-described eight values is the value of Y[1][k]. The second hard decision candidate generating unit 222 generates HI0v[2 : m - 1][1] by setting B[2 : m - 1][1][k] as bit values of the k-th column of HI0v[2 : m - 1][1] of B[1 : m][1][k] that is a combination of bit values corresponding to the value of X[1][k] having the maximum posterior probability.

[0200] Similarly, a bit value of the k-th column of H21v[2 : m - 1][1] is a hard decision value obtained by performing hard decision on the value of Y[1][k] in a case where the bit value of B[m][1][k] that is the LSB of B[1 : m][1][k] that is a combination of bit values corresponding to X[1][k] corresponding to Y[1][k] is "1 ".

[0201] Specifically, for example, the second hard decision candidate generating unit 222 determines a bit value of the k-th column of HI1v[2 : m - 1][1] on the basis of the first symbol mapping rule indicated in FIG. 4A.

[0202] More specifically, in a case where the bit value of B[m][1][k] is "1", referring to the first symbol mapping rule indicated in FIG. 4A, X[1][k] can take any one of eight values of -13, -9, -5, -1, 3, 7, 11, and 15. The second hard decision candidate generating unit 222 compares the above-described eight values with the value of Y[1][k], and determines that the value of X[1][k] having the maximum posterior probability among the above-described eight values is the value of Y[1][k]. The second hard decision candidate generating unit 222 generates HI1v[2 : m - 1][1] by setting B[2 : m - 1][1][k] as bit values of the k-th column of HI1v[2 : m - 1][1] of B[1 : m][1][k] that is a combination of bit values corresponding to the value of X[1][k] having the maximum posterior probability.

[0203] In the case where m is greater than or equal to 3, the third hard decision candidate generating unit 223 generates HI0v[2 : m - 1][2] and HI1v[2 : m - 1][2] each of which is hard decision candidate bit array information of m - 2 rows and N2 columns, by using Y[2] that is the second reception modulation symbol group information, on the basis of the second symbol mapping rule.

[0204] A bit value of the k-th column of HI0v[2 : m - 1][2] is a hard decision value obtained by performing hard decision on the value of Y[2][k] in a case where the bit value of B[m][2][k] that is the LSB of B[1 : m][2][k] that is a combination of bit values corresponding to X[2][k] corresponding to Y[2][k] is "0".

[0205] Specifically, for example, the third hard decision candidate generating unit 223 determines a bit value of the k-th column of HI0v[2 : m - 1][2] on the basis of the second symbol mapping rule indicated in FIG. 4B.

[0206] More specifically, in a case where the bit value of B[m][2][k] is "0", referring to the second symbol mapping rule indicated in FIG. 4B, X[2][k] can take any one of eight values of -13, -9, -5, -1, 1, 5, 9, and 13. The third hard decision candidate generating unit 223 compares the above-described eight values with the value of Y[2][k], and determines that the value of X[2][k] having the maximum posterior probability among the above-described eight values is the value of Y[2][k]. The third hard decision candidate generating unit 223 generates HI0v[2 : m - 1][2] by setting B[2 : m - 1][2][k] as the bit value of the k-th column of HI0v[2 : m - 1][2] of B[1 : m][2][k] that is a combination of bit values corresponding to the value of X[2][k] having the maximum posterior probability.

[0207] Similarly, a bit value of the k-th column of H21v[2 : m - 1][2] is a hard decision value obtained by performing hard decision on the value of Y[2][k] in a case where the bit value of B[m][2][k] that is the LSB of B[1 : m][2][k] that is a combination of bit values corresponding to X[2][k] corresponding to Y[2][k] is "1 ".

[0208] Specifically, for example, the third hard decision candidate generating unit 223 determines a bit value of the k-th column of HI1v[2 : m - 1][2] on the basis of the second symbol mapping rule indicated in FIG. 4B.

[0209] More specifically, in a case where the bit value of B[m][2][k] is "1", referring to the second symbol mapping rule indicated in FIG. 4B, X[2][k] can take any one of eight values of -15, -11, -7, -5, 3, 7, 11, and 15. The third hard decision candidate generating unit 223 compares the above-described eight values with the value of Y[2][k], and determines that the value of X[2][k] having the maximum posterior probability among the above-described eight values is the value of Y[2][k]. The third hard decision candidate generating unit 223 generates HI1v[2 : m - 1][2] by setting B[2 : m - 1][2][k] that is the LSB of B[1 : m][2][k] that is a combination of bit values corresponding to the value of X[2][k] having the maximum posterior probability as the bit value of the k-th column of HI1v[2 : m - 1][2].

[0210] The soft decision information generating unit 230 generates a first posterior L value sequence, a second posterior L value sequence, and a third posterior L value sequence that are posterior L value sequences in which posterior L values are arranged, on the basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210.

[0211] Specifically, for example, the soft decision information generating unit 230 includes a first soft decision information generating unit 231 to generate the first posterior L value sequence, a second soft decision information generating unit 232 to generate the second posterior L value sequence, and a third soft decision information generating unit 233 to generate the third posterior L value sequence.

[0212] The posterior L value is a posterior logarithmic probability ratio, and the posterior L value is calculated on the basis of a value indicated by Y[1 : 2][k] that is a reception PAM symbol.

[0213] Specifically, the posterior L value is a logarithmic value of a ratio between a posterior probability that a target bit value is "0" and a posterior probability that the target bit value is "1", of B[1 : m][1][k] or B[1 : m][2][k] that is a combination of bit values corresponding to X[1][k] or X[1][k] corresponding to Y[1][k] or Y[2][k], that is, a soft decision value. The posterior L value is expressed by a combination of a plurality of bit values of about three bits to six bits.

[0214] For example, in a case where the posterior L value is a positive value, the hard decision value of the target bit is "0", and in a case where the posterior L value is a negative value, the hard decision value of the target bit is "1".

[0215] The magnitude of the absolute value of the posterior L value indicates a degree of reliability when hard decision of the target bit is performed.

[0216] The soft decision information generating unit 230 generates a posterior L value sequence by calculating a posterior L value corresponding to a target bit for each reception PAM symbol.

[0217] The first soft decision information generating unit 231 generates the first posterior L value sequence in which N2 posterior L values are arranged by calculating a posterior L value for each reception PAM symbol on the basis of a value indicated by the reception PAM symbol belonging to the second reception modulation symbol group information.

[0218] Specifically, a posterior L value of the k-th column in the first posterior L value sequence generated by the first soft decision information generating unit 231 corresponds to B[1][2][k] that is the MSB of B[1 : m][2][k] that is a combination of bit values corresponding to X[2][k] corresponding to Y[2][k].

[0219] Hereinafter, the first posterior L value sequence is expressed as Lv[1][2], and the k-th posterior L value of Lv[1][2] that is the first posterior L value sequence is expressed as L[1][2][k].

[0220] That is, the k-th posterior L value L[1][2][k] of Lv[1][2] that is the first posterior L value sequence corresponds to B[1][2][k] of B[1 : m][2][k] that is a combination of bit values corresponding to X[2][k] corresponding to Y[2][k].

[0221] The second soft decision information generating unit 232 generates the second posterior L value sequence in which N1 posterior L values are arranged by calculating a posterior L value for each reception PAM symbol on the basis of a value indicated by the reception PAM symbol belonging to the first reception modulation symbol group information.

[0222] Specifically, a posterior L value of the k-th column in the second posterior L value sequence generated by the second soft decision information generating unit 232 corresponds to B[m][1][k] that is the LSB of B[1 : m][1][k] that is a combination of bit values corresponding to X[1][k] corresponding to Y[1][k].

[0223] Hereinafter, the second posterior L value sequence is expressed as Lv[m][1], and the k-th posterior L value of Lv[m][1] that is the second posterior L value sequence is expressed as L[m][1][k].

[0224] That is, the k-th posterior L value L[m][1][k] of Lv[m][1] that is the second posterior L value sequence corresponds to B[m][2][k] of B[1 : m][1][k] that is a combination of bit values corresponding to X[1][k] corresponding to Y[1][k].

[0225] The third soft decision information generating unit 233 generates the third posterior L value sequence in which N2 posterior L values are arranged by calculating a posterior L value for each reception PAM symbol on the basis of a value indicated by the reception PAM symbol belonging to the second reception modulation symbol group information.

[0226] Specifically, a posterior L value of the k-th column in the third posterior L value sequence generated by the third soft decision information generating unit 233 corresponds to B[m][1][k] that is the LSB of B[1 : m][2][k] that is a combination of bit values corresponding to X[2][k] corresponding to Y[2][k].

[0227] Hereinafter, the third posterior L value sequence is expressed as Lv[m][2], and the k-th posterior L value of Lv[m][2] that is the third posterior L value sequence is expressed as L[m][2][k].

[0228] That is, the k-th posterior L value L[m][2][k] of Lv[m][2] that is the third posterior L value sequence corresponds to B[m][2][k] of B[1 : m][2][k] that is a combination of bit values corresponding to X[2][k] corresponding to Y[2][k].

[0229] The decoding unit 240 generates output information by performing multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230.

[0230] Details of the decoding unit 240 will be described later.

[0231] The information output unit 290 outputs the output information generated by the decoding unit 240.

[0232] A configuration of a main part of the decoding unit 240 according to the first embodiment will be described with reference to FIG. 8.

[0233] FIG. 8 is a configuration diagram illustrating an example of the configuration of the main part of the decoding unit 240 according to the first embodiment.

[0234] The decoding unit 240 includes a soft decision error correction decoding unit 241, a selection unit 242, a reception side bit inversion unit 243, a probability distribution shaping decoding unit 244, a second output bit array generating unit 245, and an output information generating unit 246.

[0235] The soft decision error correction decoding unit 241 performs first decoding processing in the multi-stage error correction processing.

[0236] Specifically, the soft decision error correction decoding unit 241 performs soft decision error correction processing by using the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence.

[0237] The soft decision error correction decoding unit 241 generates inverted first reception LSB information including a bit array of one row and N1 columns corresponding to the inverted first LSB information generated by the bit inversion unit 123 by performing the soft decision error correction processing.

[0238] In addition, the soft decision error correction decoding unit 241 generates second reception LSB information including a bit array of one row and N2 columns corresponding to the second LSB information generated by the probability distribution shaping encoding unit 122 by performing the soft decision error correction processing.

[0239] A method of performing the soft decision error correction processing by using the posterior L value sequence is known, and thus detailed description of the method will be omitted.

[0240] The selection unit 242 performs second decoding processing in the multi-stage error correction processing.

[0241] Specifically, for example, a first selection unit 2421, a second selection unit 2422, and a third selection unit 2423 are included.

[0242] The first selection unit 2421 generates first reception MSB information including a bit array of one row and N1 columns corresponding to the first MSB information on the basis of the first hard decision candidate bit array information and the inverted first reception LSB information.

[0243] Specifically, in a case where a bit value of the k-th column in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241 is "0", the first selection unit 2421 selects HI0v[1][1] out of HI0v[1][1] and HI1v[1][1] each being the first hard decision candidate bit array information generated by the first hard decision candidate generating unit 221. The first selection unit 2421 substitutes the bit value of the k-th column of HI0v[1][1] for a bit of the k-th column of the first reception MSB information.

[0244] In addition, in a case where the bit value of the k-th column in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241 is "1", the first selection unit 2421 selects HI1v[1][1] out of HI0v[1][1] and HI1v[1][1] each being the first hard decision candidate bit array information generated by the first hard decision candidate generating unit 221. Further, the first selection unit 2421 substitutes the bit value of the k-th column of HI1v[1][1] for the bit of the k-th column of the first reception MSB information.

[0245] The first selection unit 2421 generates the first

reception MSB information by substituting a bit value of a column of HI0v[1][1] or HI1v[1][1] corresponding to a column of the first reception MSB information for each column of the first reception MSB information.

[0246] In the case where m is greater than or equal to 3, the second selection unit 2422 generates first reception SSB information including a bit array of m - 2 rows and N1 columns corresponding to the first SSB information on the basis of the second hard decision candidate bit array information and the inverted first reception LSB information.

[0247] Specifically, in the case where the bit value of the k-th column in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241 is "0", the second selection unit 2422 selects HI0v[2 : m - 1][1] out of HI0v[2 : m - 1][1] and HI1v[2 : m - 1][1] each being the second hard decision candidate bit array information generated by the second hard decision candidate generating unit 222. The second selection unit 2422 substitutes each of m - 2 bit values of the k-th column of HI0v[2 : m - 1][1] for each of m - 2 bits of the k-th column of the first reception SSB information.

[0248] In addition, in the case where the bit value of the k-th column in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241 is "1", the second selection unit 2422 selects HI1v[2 : m - 1][1] out of HI0v[2 : m - 1][1] and HI1v[2 : m - 1][1] each being the second hard decision candidate bit array information generated by the second hard decision candidate generating unit 222. The second selection unit 2422 substitutes each of m - 2 bit values of the k-th column of HI1v[2 : m - 1][1] for each of m - 2 bits of the k-th column of the first reception SSB information.

[0249] The second selection unit 2422 generates the first reception SSB information by substituting a bit value of a column of HI0v[2 : m - 1][1] or HI1v[2 : m - 1][1] corresponding to a column of the first reception SSB information for each column of the first reception SSB information.

[0250] In the case where m is greater than or equal to 3, the third selection unit 2423 generates second reception SSB information including a bit array of m - 2 rows and N2 columns corresponding to the second SSB information on the basis of the third hard decision candidate bit array information and the second reception LSB information.

[0251] Specifically, in a case where a bit value of the k-th column in the second reception LSB information generated by the soft decision error correction decoding unit 241 is "0", the third selection unit 2423 selects HI0v[2 : m - 1][2] out of HI0v[2 : m - 1][2] and HI1v[2 : m - 1][2] each being the third hard decision candidate bit array information generated by the third hard decision candidate generating unit 223. The third selection unit 2423 substitutes each of m - 2 bit values of the k-th column of HI0v[2 : m - 1][2] for each of m - 2 bits of the k-th column of the second reception SSB information.

[0252] In addition, in a case where the bit value of the k-th column in the second reception LSB information generated by the soft decision error correction decoding unit 241 is "1", the third selection unit 2423 selects HI1v[2 : m - 1][2] out of HI0v[2 : m - 1][2] and HI1v[2 : m - 1][2] each being the third hard decision candidate bit array information generated by the third hard decision candidate generating unit 223. The third selection unit 2423 substitutes each of m - 2 bit values of the k-th column of HI1v[2 : m - 1][2] for each of m - 2 bits of the k-th column of the second reception SSB information.

[0253] The third selection unit 2423 generates the second reception SSB information by substituting a bit value of a column of HI0v[2 : m - 1][2] or HI1v[2 : m - 1][2] corresponding to a column of the second reception SSB information for each column of the second reception SSB information.

[0254] As described above, HI0v[1][1] and HI0v[1][1], HI0v[2 : m - 1][1] and HI0v[2 : m - 1][1], and HI0v[2 : m - 1][2] and HI0v[2 : m - 1][2] are generated by the hard decision candidate generating unit 220 by performing case classification between a case where the bit value of B[m][1 : 2][k] is "0" and a case where the bit value is "1".

[0255] For example, in a case where the first symbol mapping rule and the second symbol mapping rule are the first symbol mapping rule and the second symbol mapping rule indicated in FIG. 4 as examples of the first symbol mapping rule and the second symbol mapping rule, in the same symbol mapping rule, the minimum Euclidean distance between two PAM symbols adjacent to each other is "2", whereas the minimum Euclidean distance in the case of performing the case classification as described above is "4" that is twice as large. When the Euclidean distance is doubled, the SNR is improved by four times that is 2^2 times.

[0256] Thus, by performing the case classification as described above, as compared with a case where the case classification is not performed, accuracy of determination of the bit value selected when the selection unit 242 substitutes the bit value of the first reception MSB information, the first reception SSB information, or the second reception SSB information can be improved by four times.

[0257] The reception side bit inversion unit 243 performs third decoding processing in the multi-stage error correction processing.

[0258] Specifically, the reception side bit inversion unit 243 generates the first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241 and each bit values of each columns in the first reception MSB information generated by the first selection unit 2421 each corresponding to the columns in the inverted first reception LSB information.

[0259] The probability distribution shaping decoding

unit 244 performs fourth decoding processing in the multi-stage error correction processing.

[0260] Specifically, the probability distribution shaping decoding unit 244 generates first output bit array information including a bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information generated by the second selection unit 2422, the second reception SSB information generated by the third selection unit 2423, the first reception LSB information generated by the reception side bit inversion unit 243, and the second reception LSB information generated by the soft decision error correction decoding unit 241.

[0261] Specifically, for example, the probability distribution shaping decoding unit 244 prepares DRv[1 : m - 1][1 : 2] that is a bit array space of m - 1 rows and N columns including DRv[1 : m - 1][1] that is a bit array space of m - 1 rows and N1 columns and DRv[1 : m - 1][2] that is a bit array space of m - 1 rows and N2 columns.

[0262] In the following description, a bit value of the k-th column of DRv[1 : m - 1][1] is denoted as "BR[1 : m - 1][1][k]", and a bit value of the k-th column of DRv[1 : m - 1][2] is denoted as "BR[1 : m - 1][2][k]".

[0263] The probability distribution shaping decoding unit 244 stores the first reception SSB information in DRv[1 : m - 2][1], stores the second reception SSB information in DRv[1 : m - 2][2], stores the first reception LSB information in DRv[m - 1][1], and stores the second reception LSB information in DRv[m - 1][2].

[0264] The probability distribution shaping decoding unit 244 performs the probability distribution shaping decoding processing on BR[1 : m - 1][1 : 2][k].

[0265] The probability distribution shaping decoding unit 244 overwrites BR[1 : m - 1][1 : 2][k] with a processing result of the probability distribution shaping decoding processing.

[0266] BR[1 : m - 1][1 : 2][k] after the probability distribution shaping decoding unit 244 overwrites BR[1 : m - 1][1 : 2][k] with the processing result of the probability distribution shaping decoding processing is the first output bit array information.

[0267] Note that, the probability distribution shaping decoding processing is processing paired with the probability distribution shaping encoding processing, and a method of performing the probability distribution shaping decoding processing is known, and thus detailed description of the method will be omitted.

[0268] The second output bit array generating unit 245 performs fifth decoding processing in the multi-stage error correction processing.

[0269] Specifically, the second output bit array generating unit 245 generates second output bit array information including a bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of an area corresponding to the second input bit area in the first MSB information, of the first reception MSB information.

[0270] The output information generating unit 246 performs sixth decoding processing in the multi-stage error correction processing.

[0271] Specifically, the output information generating unit 246 generates the output information corresponding to the input information on the basis of the first output bit array information and the second output bit array information.

[0272] A hardware configuration of the main part of the error correction device 200 according to the first embodiment will be described with reference to FIG. 9.

[0273] FIGS. 9A and 9B are diagrams illustrating examples of a hardware configuration of the error correction device 200 according to the first embodiment.

[0274] As illustrated in FIG. 9A, the error correction device 200 includes a computer, and the computer includes a processor 901 and a memory 902. The memory 902 stores a program for causing the computer to function as the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240, and the information output unit 290. The processor 901 reads and executes the program stored in the memory 902, whereby functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240, and the information output unit 290 are implemented.

[0275] In addition, as illustrated in FIG. 9B, the error correction device 200 may include a processing circuit 903. In this case, the functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240, and the information output unit 290 may be implemented by the processing circuit 903.

[0276] In addition, the error correction device 200 may include the processor 901, the memory 902, and the processing circuit 903 (not illustrated). In this case, some of the functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240, and the information output unit 290 may be implemented by the processor 901 and the memory 902, and remaining functions may be implemented by the processing circuit 903.

[0277] Note that, the processor 901, the memory 902, and the processing circuit 903 are similar to the processor 501, the memory 502, and the processing circuit 503 illustrated in FIG. 5, and thus description thereof will be omitted.

[0278] Operation of the error correction device 200 according to the first embodiment will be described with reference to FIGS. 10A, 10B, and 10C.

[0279] FIG. 10A is a part of a flowchart illustrating an example of processing performed by the error correction

device 200 according to the first embodiment.

[0280] FIG. 10B is another part of the flowchart illustrating the example of the processing performed by the error correction device 200 according to the first embodiment.

[0281] FIG. 10C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device 200 according to the first embodiment.

[0282] Hereinafter, FIGS. 10A, 10B, and 10C are collectively denoted as FIG. 10.

[0283] The error correction device 200 repeatedly executes the processing of the flowchart illustrated in FIG. 10.

[0284] First, in step ST1000, the reception modulation symbol group information generating unit 210 generates the reception modulation symbol group information.

[0285] Specifically, the reception modulation symbol group information generating unit 210 performs processing of step ST1000 by performing processing from step ST1001 to step ST1002 in processing D below.

[0286] In step ST1001, the reception polarization multiplexing symbol generating unit 211 included in the reception modulation symbol group information generating unit 210 generates the reception QAM symbol.

[0287] Next, in step ST1002, the reception modulation symbol generating unit 212 included in the reception modulation symbol group information generating unit 210 generates the reception modulation symbol group information.

[0288] After step ST1002, the reception modulation symbol group information generating unit 210 ends the processing D. That is, after step ST1002, the reception modulation symbol group information generating unit 210 ends the processing of step ST1000.

[0289] After step ST1000, in step ST1010, the hard decision candidate generating unit 220 generates the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information.

[0290] Specifically, the hard decision candidate generating unit 220 performs processing of step ST1010 by performing processing from step ST1011 to step ST1013 in processing E below.

[0291] In step ST1011, the first hard decision candidate generating unit 221 included in the hard decision candidate generating unit 220 generates the first hard decision candidate bit array information.

[0292] Next, in step ST1012, the second hard decision candidate generating unit 222 included in the hard decision candidate generating unit 220 generates the second hard decision candidate bit array information.

[0293] Next, in step ST1013, the third hard decision candidate generating unit 223 included in the hard decision candidate generating unit 220 generates the third hard decision candidate bit array information.

[0294] Note that, the order of the processing from step ST1011 to step ST1013 is any order.

[0295] After step ST1013, the hard decision candidate generating unit 220 ends the processing E. That is, after step ST1013, the hard decision candidate generating unit 220 ends the processing of step ST1010.

[0296] After step ST1010, in step ST1020, the soft decision information generating unit 230 generates the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence.

[0297] Specifically, the soft decision information generating unit 230 performs processing of step ST1020 by performing processing from step ST1021 to step ST1023 in processing F below.

[0298] In step ST1021, the first soft decision information generating unit 231 included in the soft decision information generating unit 230 generates the first posterior L value sequence.

[0299] Next, in step ST1022, the second soft decision information generating unit 232 included in the soft decision information generating unit 230 generates the second posterior L value sequence.

[0300] Next, in step ST1023, the third soft decision information generating unit 233 included in the soft decision information generating unit 230 generates the third posterior L value sequence.

[0301] After step ST1023, the soft decision information generating unit 230 ends the processing F. That is, after step ST1023, the soft decision information generating unit 230 ends the processing of step ST1020.

[0302] Note that the order of the processing from step ST1021 to step ST1023 is any order.

[0303] In addition, the processing order of the processing of step ST1010 and the processing of step ST1020 is any order.

[0304] After step ST1020, in step ST1030, the decoding unit 240 generates the output information by performing the multi-stage error correction processing.

[0305] Specifically, the decoding unit 240 performs processing of step ST1030 by performing processing from step ST1031 to step ST1036 in processing G below.

[0306] In step ST1031, the soft decision error correction decoding unit 241 included in the decoding unit 240 generates the inverted first reception LSB information and the second reception LSB information by performing the soft decision error correction processing.

[0307] Next, in step ST1032, the selection unit 242 included in the decoding unit 240 generates the first reception MSB information, the first reception SSB information, and the second reception SSB information.

[0308] Specifically, the selection unit 242 performs processing of step ST1032 by performing processing from step ST1041 to step ST1043 in processing H below.

[0309] In step ST1041, the first selection unit 2421 included in the selection unit 242 generates the first reception MSB information.

[0310] Next, in step ST1042, the second selection unit 2422 included in the selection unit 242 generates the first reception SSB information.

[0311] Next, in step ST1043, the third selection unit

2423 included in the selection unit 242 generates the second reception SSB information.

[0312] After step ST1043, the selection unit 242 included in the decoding unit 240 ends the processing H. That is, after step ST1043, the selection unit 242 included in the decoding unit 240 ends the processing of step ST1032.

[0313] Note that, the order of the processing from step ST1041 to step ST1043 is any order.

[0314] After step ST1032, in step ST1033, the second output bit array generating unit 245 included in the decoding unit 240 generates the first reception LSB information.

[0315] Next, in step ST1034, the probability distribution shaping decoding unit 244 included in the decoding unit 240 generates the first output bit array information.

[0316] Next, in step ST1035, the second output bit array generating unit 245 included in the decoding unit 240 generates the second output bit array information.

[0317] Next, in step ST1036, the output information generating unit 246 included in the decoding unit 240 generates the output information.

[0318] After step ST1036, the decoding unit 240 ends the processing G. That is, after step ST1036, the decoding unit 240 ends the processing of step ST1030.

[0319] After step ST1030, in step ST1050, the information output unit 290 outputs the output information.

[0320] After step ST1050, the error correction device 200 ends the processing of the flowchart illustrated in FIG. 10, and the error correction device 200 returns to the processing of step ST1000 and repeatedly executes the processing of the flowchart illustrated in FIG. 10.

[0321] As described above, the error correction encoding device 100 includes: the input information acquiring unit 110 to acquire the input information; the encoding unit 120 to generate the soft decision error correction frame information including the bit array of m rows and N columns on the basis of the input information acquired by the input information acquiring unit 110, the bit array being obtained by combining the first bit string group information and the second bit string group information, the first bit string group information including the bit array of m rows and N1 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the first bit string group information into the modulation symbol by using the predetermined first symbol mapping rule, the second bit string group information including the bit array of m rows and N2 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the second bit string group information into the modulation symbol by using the predetermined second symbol mapping rule; the modulation symbol conversion unit 130 to generate the modulation symbol group information including N pieces of the modulation symbols by performing the pulse amplitude modulation of the combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit 120 into the modulation symbol for each column of the soft decision error correction frame information by using the first symbol mapping rule or the second symbol mapping rule; and the transmission waveform shaping unit 140 to generate the digital baseband modulation signal on the basis of the modulation symbol group information generated by the modulation symbol conversion unit 130 and output the digital baseband modulation signal generated, in which the encoding unit 120 generates the soft decision error correction frame information by: generating the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit 110; storing the second input bit array information generated as a part of the first MSB information including the bit array of one row and N1 columns in the predetermined area of the first row in the first bit string group information; generating the shaped bit array information including the bit array of m - 1 rows and N columns by performing the probability distribution shaping encoding processing on the first input bit array information generated; generating the first group bit array information including the combination of N1 predetermined columns and the second group bit array information including the combination of N2 predetermined columns by separating the shaped bit array information generated; generating the first LSB information including the bit array of one row and N1 columns by extracting, from the first group bit array information generated, the bit array of the (m - 1)-th row in the first group bit array information, generating the inverted first LSB information including the bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in the information of the first row in the first bit string group information after storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in the m-th row in the first bit string group information; generating the second LSB information including the bit array of one row and N2 columns by extracting the bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated, and storing the second LSB information generated in the m-th row in the second bit string group information; generating the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in the first row in the second bit string group information as the second MSB information including the bit array of one row and N2 columns; in the case where m is greater than or equal to 3, generating the first SSB information

including the bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated, the first row to the (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in the second row to the (m - 1)-th row in the first bit string group information; and in the case where m is greater than or equal to 3, generating the second SSB information including the bit array of m - 2 rows and N2 columns by extracting, from the second group bit array information generated, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the second row to the (m - 1)-th row in the second bit string group information.

[0322] With this configuration, the error correction encoding device 100 can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction encoding device 100 can reduce the amount of calculation of the soft decision error correction encoding processing as compared with the conventional soft decision error correction encoding processing.

[0323] In addition, with this configuration, the error correction encoding device 100 can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction encoding device 100 can make the amount of calculation of the soft decision error correction encoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction encoding device 100 does not need to change the program or the processing circuit for performing the soft decision error correction encoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0324] In addition, as described above, in the above-described configuration, the error correction encoding device 100 is configured to use a symbol mapping rule such as: the first symbol mapping rule is a symbol mapping rule in which one combination of bit values including a bit array of m rows and one column corresponds to one of the modulation symbols subjected to one-dimensional pulse amplitude modulation, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols are adjacent to each other; and the second symbol mapping rule is a symbol mapping rule in which one combination of bit values including a bit array of m rows and one column corresponds to one of the modulation symbols subjected to one-dimensional pulse amplitude modulation, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols have an identical sign and are adjacent to each other, and are identical values between the modulation symbol of which an absolute vale of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are positive and the modulation symbol of which an absolute value of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are negative.

[0325] With this configuration, the error correction encoding device 100 can improve the SNR Thus, the error correction encoding device 100 can improve the accuracy of determination of the bit value in the error correction device 200.

[0326] In addition, as described above, in the above-described configuration, the error correction encoding device 100 is configured so that the encoding unit 120 generates the first input bit array information and the second input bit array information by setting a bit value of a bit other than a bit corresponding to the input information to 0 in the first input bit array information or the second input bit array information when generating the first input bit array information and the second input bit array information on the basis of the input information acquired by the input information acquiring unit 110.

[0327] With this configuration, the error correction encoding device 100 can generate the soft decision error correction frame information for the input information having any number of bits.

[0328] Note that, the error correction encoding device 100 may include the soft decision parity bit generated by the soft decision error correction encoding unit 124 performing the systematic soft decision error correction encoding processing in other soft decision error correction frame information different from the soft decision error correction frame information instead of the soft decision error correction frame information including the inverted first LSB information and the second LSB information used to generate the soft decision parity bit. For example, the other soft decision error correction frame information is soft decision error correction frame information generated by the error correction encoding device 100 next to the soft decision error correction frame information including the inverted first LSB information and the second LSB information used by the error correction encoding device 100 to generate the soft decision parity bit.

[0329] With this configuration, the error correction encoding device 100 can disperse a burst error occurring in the transmission path 30. The burst error mentioned here is an error that occurs in a concentrated manner in a specific portion of a signal due to a change of the transmission path 30 when the signal is transmitted via the

transmission path 30. The error correction encoding device 100 can reduce deterioration of information after the error correction by dispersing the burst error.

[0330] As described above, the error correction device 200 includes: the reception modulation symbol group information generating unit 210 to receive the reception digital baseband modulation signal that is the signal based on the soft decision error correction frame information generated by the error correction encoding device 100 and generate reception modulation symbol group information including N reception modulation symbols on the basis of the reception digital baseband modulation signal; the hard decision candidate generating unit 220 to generate first hard decision candidate bit array information including the bit array of one row and N1 columns, second hard decision candidate bit array information including the bit array of m - 2 rows and N1 columns in the case where m is greater than or equal to 3, and third hard decision candidate bit array information including the bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210 on the basis of the first symbol mapping rule or the second symbol mapping rule; the soft decision information generating unit 230 to generate the first posterior L value sequence including N2 posterior L values corresponding to each columns of the first row of the second bit string group information, the second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and the third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on the basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210; the decoding unit 240 to perform multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230 ; and the information output unit 290 to output information generated by the decoding unit 240 performing the multi-stage error correction processing as output information, in which: in the first decoding processing in the multi-stage error correction processing, the decoding unit 240 generates inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information and second reception LSB information including the bit array of one row and N2 columns corresponding to the second LSB information by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence; in the second decoding processing in the multi-stage error correction processing, the decoding unit 240 generates first reception MSB information including the bit array of one row and N1 columns corresponding to the first MSB information on the basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generates first reception SSB information including the bit array of m - 2 rows and N1 columns corresponding to the first SSB information on the basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generates second reception SSB information including the bit array of m - 2 rows and N2 columns corresponding to the second SSB information on the basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3; in the third decoding processing in the multi-stage error correction processing, the decoding unit 240 generates first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information; in the fourth decoding processing in the multi-stage error correction processing, the decoding unit 240 generates first output bit array information including the bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information; in the fifth decoding processing in the multi-stage error correction processing, the decoding unit 240 generates second output bit array information including the bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of the predetermined area of the first reception MSB information; in the sixth decoding processing in the multi-stage error correction processing, the decoding unit 240 generates the output information corresponding to the input information on the basis of the first output bit array information and the second output bit array information; and the information output unit 290 outputs the output information generated by the decoding unit 240.

[0331] With this configuration, the error correction device 200 can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction device 200 can reduce the amount of calculation of the soft decision error correction decoding processing as compared with the conventional soft decision error correction decoding processing.

[0332] In addition, with this configuration, the error correction device 200 can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction device 200 can make the amount of calculation of the soft decision error correction decoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction device 200 does not need to change the program or the processing circuit for performing the soft decision error correction decoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0333] In addition, as described above, in the above-described configuration, the error correction device 200 is configured to use a symbol mapping rule such as: the first symbol mapping rule is a symbol mapping rule in which one combination of bit values including a bit array of m rows and one column corresponds to one of the modulation symbols subjected to one-dimensional pulse amplitude modulation, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols are adjacent to each other; and the second symbol mapping rule is a symbol mapping rule in which one combination of bit values including a bit array of m rows and one column corresponds to one of the modulation symbols subjected to one-dimensional pulse amplitude modulation, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols have an identical sign and are adjacent to each other, and are identical values between the modulation symbol of which an absolute vale of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are positive and the modulation symbol of which an absolute value of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are negative.

[0334] With this configuration, the error correction device 200 can improve the SNR Thus, the error correction device 200 can improve the accuracy of determination of the bit value.

[0335] As described above, the soft decision error correction frame data structure of the soft decision error correction frame information generated by the error correction encoding device 100 is a soft decision error correction frame data structure used in a communication system in which the transmission device 10 transmits a signal based on input information input to the transmission device 10 to the reception device 20, and the reception device 20 receives the signal transmitted by the transmission device 10 and generates output information corresponding to the input information on the basis of the signal, the soft decision error correction frame data structure including a bit array of m rows and N columns obtained by combining first bit string group information and second bit string group information, the first bit string group information including a bit array of m rows and N1 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol on the basis of a predetermined first symbol mapping rule, the second bit string group information including a bit array of m rows and N2 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol on the basis of a predetermined second symbol mapping rule, in which a soft decision parity bit is stored in a first row in the second bit string group information, the soft decision parity bit being generated by performing systematic soft decision error correction encoding processing using a bit value of each column of the m-th row in the first bit string group information and a bit value of each column of the m-th row in the second bit string group information.

[0336] With such a soft decision error correction frame data structure, the error correction encoding device 100 can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction encoding device 100 can reduce the amount of calculation of the soft decision error correction encoding processing as compared with the conventional soft decision error correction encoding processing.

[0337] In addition, with such a soft decision error correction frame data structure, the error correction encoding device 100 can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction encoding device 100 can make the amount of calculation of the soft decision error correction encoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction encoding device 100 does not need to change the program or the processing circuit for performing the soft decision error correction encoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0338] In addition, with such a soft decision error correction frame data structure, the error correction device 200 can reduce the number of bits to be protected by the soft decision error correction as compared with the con-

ventional soft decision error correction encoding processing. For that reason, the error correction device 200 can reduce the amount of calculation of the soft decision error correction decoding processing as compared with the conventional soft decision error correction decoding processing.

[0339] In addition, with such a soft decision error correction frame data structure, the error correction device 200 can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction device 200 can make the amount of calculation of the soft decision error correction decoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction device 200 does not need to change the program or the processing circuit for performing the soft decision error correction decoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0340] In addition, the soft decision error correction frame data structure of the soft decision error correction frame information generated by the error correction encoding device 100 enables: generation of reception modulation symbol group information including N reception modulation symbols on the basis of a reception digital baseband modulation signal generated from a signal based on soft decision error correction frame information having the soft decision error correction frame data structure; generation of first hard decision candidate bit array information including a bit array of one row and N1 columns, second hard decision candidate bit array information including a bit array of m - 2 rows and N1 columns in the case where m is greater than or equal to 3, and third hard decision candidate bit array information including a bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the first symbol mapping rule or the second symbol mapping rule on the basis of the reception modulation symbol group information generated; generation of the first posterior L value sequence including N2 posterior L values corresponding to each columns of the first row of the second bit string group information, the second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and the third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on the basis of the reception modulation symbol group information generated; and error correction by performing multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, the third hard decision candidate bit array information, the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated.

[0341] In addition, in the soft decision error correction frame data structure of the soft decision error correction frame information generated by the error correction encoding device 100, it is enabled to: generate inverted first reception LSB information including a bit array of one row and N1 columns and second reception LSB information including a bit array of one row and N2 columns by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence, in the first decoding processing in the multi-stage error correction processing; generate first reception MSB information including a bit array of one row and N1 columns on the basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generate first reception SSB information including a bit array of m - 2 rows and N1 columns on the basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generate second reception SSB information including a bit array of m - 2 rows and N2 columns on the basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3, in the second decoding processing in the multi-stage error correction processing; generate first reception LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information, in the third decoding processing in the multi-stage error correction processing; generate first output bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information, in the fourth decoding processing in the multi-stage error correction processing; generate second output bit array information including a bit array of one row and N3 columns by extracting information of a predetermined area of the first reception MSB information, in the fifth decoding processing in the multi-stage error correction processing; and generate the output information corresponding to the input information on the basis of the first output bit array information and the second output bit array information, in the sixth decoding processing in the multi-stage error correction processing.

Modification of First Embodiment.

[0342] A configuration of a main part of a communication system 1c according to a modification of the first embodiment will be described with reference to FIG. 28.

[0343] FIG. 28 is a configuration diagram illustrating an example of the configuration of the main part of the

communication system 1c according to the modification of the first embodiment.

[0344] In the modification of the first embodiment, as an example, the communication system 1c is described as an optical communication system, but the optical communication system is merely an example, and the communication system 1c is not limited to the optical communication system. For example, the communication system 1c may be a communication system by wireless communication, metal communication, or the like.

[0345] The communication system 1c includes a transmission device 10c, the transmission path 30, and a reception device 20c.

[0346] The communication system 1c is obtained by changing the transmission device 10 and the reception device 20 according to the first embodiment to the transmission device 10c and the reception device 20c.

[0347] Note that, in FIG. 28, blocks similar to the blocks illustrated in FIG. 1 are designated by the same reference numerals, and the description thereof will be omitted.

[0348] The transmission device 10c acquires input information and outputs a signal based on the acquired input information. Since the communication system 1c illustrated in FIG. 28 is the optical communication system, the transmission device 10c illustrated in FIG. 28 is an optical transmission device to output an optical signal.

[0349] The transmission device 10c includes an error correction encoding device 100c, the D/A converter 11, the transmission light source 12, and the optical modulator 13.

[0350] The transmission device 10c is obtained by changing the error correction encoding device 100 according to the first embodiment to the error correction encoding device 100c.

[0351] The error correction encoding device 100c acquires the input information input from the outside of the device, and generates a digital baseband modulation signal on the basis of the acquired input information. The error correction encoding device 100c outputs the generated digital baseband modulation signal to the D/A converter 11.

[0352] The reception device 20c receives the signal output by the transmission device 10c via the transmission path 30, generates output information corresponding to the input information on the basis of the signal, and outputs the generated output information. Since the communication system 1c illustrated in FIG. 28 is the optical communication system, the reception device 20c illustrated in FIG. 28 is an optical reception device to receive the optical signal.

[0353] The reception device 20c includes the reception light source 22, the optical receiver 21, the A/D converter 23, and an error correction device 200c.

[0354] The reception device 20c is obtained by changing the error correction device 200 according to the first embodiment to the error correction device 200c.

[0355] The error correction device 200c receives a reception digital baseband modulation signal output by the A/D converter 23, generates the output information corresponding to the input information on the basis of the reception digital baseband modulation signal, and outputs the generated output information.

[0356] A configuration of a main part of the error correction encoding device 100c according to the modification of the first embodiment will be described with reference to FIG. 29.

[0357] FIG. 29 is a configuration diagram illustrating an example of the configuration of the main part of the error correction encoding device 100c according to the modification of the first embodiment.

[0358] The error correction encoding device 100c includes the input information acquiring unit 110, an encoding unit 120c, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140.

[0359] The error correction encoding device 100c is obtained by changing the encoding unit 120 according to the first embodiment to the encoding unit 120c.

[0360] Note that, in FIG. 29, blocks similar to the blocks illustrated in FIG. 2 are designated by the same reference numerals, and the description thereof will be omitted.

[0361] The encoding unit 120c generates soft decision error correction frame information obtained by combining the first bit string group information and the second bit string group information on the basis of the input information acquired by the input information acquiring unit 110.

[0362] A configuration of a main part of the encoding unit 120c according to the modification of the first embodiment will be described with reference to FIG. 30.

[0363] FIG. 30 is a configuration diagram illustrating an example of the configuration of the main part of the encoding unit 120c according to the modification of the first embodiment.

[0364] The encoding unit 120c includes an input bit array information generating unit 121c, the probability distribution shaping encoding unit 122, the bit inversion unit 123, and a soft decision error correction encoding unit 124c.

[0365] The encoding unit 120c is obtained by changing the input bit array information generating unit 121 and the soft decision error correction encoding unit 124 included in the encoding unit 120 according to the first embodiment to the input bit array information generating unit 121c and the soft decision error correction encoding unit 124c.

[0366] The input bit array information generating unit 121 according to the first embodiment generates the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns on the basis of the input information.

[0367] On the other hand, the input bit array information generating unit 121c generates third input bit array information including a bit array of one row and N4 columns (N4 is a natural number of greater than or equal to 1 and less than N2) in addition to the first input bit array

information and the second input bit array information on the basis of the input information.

[0368] The input bit array information generating unit 121c generates the first input bit array information, the second input bit array information, and the third input bit array information including the bit array of one row and N4 columns on the basis of the input information acquired by the input information acquiring unit 110.

[0369] In a case where the input information includes the first input bit array information, the second input bit array information, and the third input bit array information, the input bit array information generating unit 121c generates the first input bit array information, the second input bit array information, and the third input bit array information by extracting each of the first input bit array information, the second input bit array information, and the third input bit array information from the input information, or separating the input information into the first input bit array information, the second input bit array information, and the third input bit array information.

[0370] Similarly to the input bit array information generating unit 121 according to the first embodiment, the input bit array information generating unit 121c stores the generated second input bit array information in the second input bit area of the first bit string group information as a part of the first MSB information including the bit array of one row and N1 columns.

[0371] In addition, the input bit array information generating unit 121c stores the generated third input bit array information in a predetermined area (Hereinafter, the predetermined area is referred to as a "third input bit area".) of the first row in the second bit string group information as a part of the second MSB information including the bit array of one row and N2 columns.

[0372] Specifically, the input bit array information generating unit 121c stores the third input bit array information in the third input bit area of Dv[1][2] that is a bit array space in which the second MSB is stored. Hereinafter, the description will be given assuming that the third input bit area is D[1][2][1 : N4].

[0373] The probability distribution shaping encoding unit 122 generates shaped bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping encoding processing on the first input bit array information generated by the input bit array information generating unit 121c.

[0374] In addition to the inverted first LSB information generated by the bit inversion unit 123 and the second LSB information generated by the probability distribution shaping encoding unit 122, the soft decision error correction encoding unit 124c generates a soft decision parity bit by performing systematic soft decision error correction encoding processing by using the third input bit array information stored in the third input bit area of the second MSB by the input bit array information generating unit 121c. The soft decision error correction encoding unit 124c stores the generated soft decision parity bit in a predetermined area (Hereinafter, the predetermined area is referred to as a "soft decision parity area".) different from the third input bit area in the second MSB information.

[0375] Specifically, the soft decision error correction encoding unit 124c generates the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using B[m][1][1 : N1] that is a bit value of each column in Dv[m][1] storing the inverted first LSB information, B[m][2][1 : N2] that is a bit value of each column in Dv[m][2] storing the second LSB information, and B[1][2][1 : N4] that is a bit value of each column in D[1][2][1 : N4] storing the third input bit array information. The soft decision error correction encoding unit 124c stores the generated soft decision parity bit in the soft decision parity area of Dv[1][2] that is a bit array space in which the second MSB is stored. Hereinafter, the description will be given assuming that the soft decision parity area is D[1][2][N4 + 1 : N2].

[0376] With the above configuration, the encoding unit 120c generates the soft decision error correction frame information by storing the soft decision error correction frame information in Dv[1 : m][1 : 2] that is a bit array space.

[0377] As described above, the encoding unit 120c performs the systematic soft decision error correction encoding processing by using the bit value of each column in Dv[m][1] and the bit value of each column in Dv[m][2]. For that reason, bits to be protected by the soft decision error correction encoding processing are only the least significant bit of each column in Dd[1 : 2] and D[1][2][1 : N4] in which the third input bit array information is stored, in the soft decision error correction frame information.

[0378] Thus, the encoding unit 120c can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing.

[0379] Note that, functions of the input information acquiring unit 110, the encoding unit 120c, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140 included in the error correction encoding device 100c according to the modification of the first embodiment may be implemented by the processor 501 and the memory 502 in the hardware configuration illustrated as an example in FIGS. 5A and 5B in the first embodiment, or may be implemented by the processing circuit 503.

[0380] Operation of the error correction encoding device 100c according to the modification of the first embodiment will be described with reference to FIGS. 31A, 31B, and 31C.

[0381] FIG. 31A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device 100c according to the modification of the first embodiment.

[0382] FIG. 31B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100c according to the modification of the first embodiment.

[0383] FIG. 31C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100c according to the modification of the first embodiment.

[0384] Hereinafter, FIGS. 31A, 31B, and 31C are collectively denoted as FIG. 31.

[0385] The error correction encoding device 100c repeatedly executes the processing of the flowchart illustrated in FIG. 31.

[0386] Note that, the flowchart illustrated in FIG. 31 is obtained by changing step ST610 in the flowchart illustrated in FIG. 6 to step ST3110.

[0387] In FIG. 31, processing steps similar to processing steps of the flowchart illustrated in FIG. 6 are designated by the same reference numerals, and the description thereof will be omitted.

[0388] First, the error correction encoding device 100c performs processing of step ST601.

[0389] Next, in step ST3110, the encoding unit 120c generates the soft decision error correction frame information.

[0390] Specifically, the encoding unit 120c performs processing of step ST3110 by performing processing from step ST3111 to step ST3112, processing from step ST612 to step ST616, and processing from step ST3117 to step ST3118 in processing M below.

[0391] First, in step ST3111, the input bit array information generating unit 120c included in the encoding unit 121c generates the first input bit array information, the second input bit array information, and the third input bit array information.

[0392] Next, in step ST3112, the input bit array information generating unit 121c included in the encoding unit 120c stores the third input bit array information in the third input bit area of Dv[1][2].

[0393] After step ST3112, the encoding unit 120c performs the processing from ST612 to step ST616.

[0394] After step ST616, in step ST3117, the soft decision error correction encoding unit 124c included in the encoding unit 120c generates the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the bit value of each column in Dv[m][1], the bit value of each column in Dv[m][2], and the bit value of each column in D[1][2][1 : N4] that is the third input bit area.

[0395] After step ST3117, in step ST3118, the soft decision error correction encoding unit 124c included in the encoding unit 120c stores the soft decision parity bit in Dv[1][2][N4 + 1] that is the soft decision parity area.

[0396] After step ST3118, the encoding unit 120c ends the processing M. That is, after step ST3118, the encoding unit 120c ends the processing of step ST3110.

[0397] After step ST3110, the error correction encoding device 100c performs processing from step ST620 to step ST630.

[0398] After step ST630, the error correction encoding device 100c ends the processing of the flowchart illustrated in FIG. 31, and the error correction encoding device 100c returns to the processing of step ST601 and repeatedly executes the processing of the flowchart illustrated in FIG. 31.

[0399] A configuration of a main part of the error correction device 200c according to the modification of the first embodiment will be described with reference to FIG. 32.

[0400] FIG. 32 is a configuration diagram illustrating an example of the configuration of the main part of the error correction device 200c according to the modification of the first embodiment.

[0401] The error correction device 200c includes the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, a decoding unit 240c, and the information output unit 290.

[0402] The error correction device 200c is obtained by changing the decoding unit 240 according to the first embodiment to the decoding unit 240c.

[0403] Note that, in FIG. 32, blocks similar to the blocks illustrated in FIG. 7 are designated by the same reference numerals, and the description thereof will be omitted.

[0404] The decoding unit 240c generates the output information by performing the multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230.

[0405] A configuration of a main part of the decoding unit 240c according to the modification of the first embodiment will be described with reference to FIG. 33.

[0406] FIG. 33 is a configuration diagram illustrating an example of the configuration of the main part of the decoding unit 240c according to the modification of the first embodiment.

[0407] The decoding unit 240c includes a soft decision error correction decoding unit 241c, the selection unit 242, the reception side bit inversion unit 243, the probability distribution shaping decoding unit 244, the second output bit array generating unit 245, an output information generating unit 246c, and a third output bit array generating unit 260.

[0408] The decoding unit 240c is obtained by adding the third output bit array generating unit 260 to the configuration of the decoding unit 240 according to the first embodiment, and changing the soft decision error correction decoding unit 241 and the output information generating unit 246 according to the first embodiment to the soft decision error correction decoding unit 241c and the output information generating unit 246c.

[0409] Note that, in FIG. 33, blocks similar to the blocks illustrated in FIG. 8 are designated by the same reference numerals, and the description thereof will be omitted.

[0410] The soft decision error correction decoding unit 241c performs the first decoding processing in the multi-stage error correction processing.

[0411] Specifically, the soft decision error correction decoding unit 241c performs the soft decision error correction processing by using the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence.

[0412] More specifically, the soft decision error correction decoding unit 241c performs the soft decision error correction processing by using L[1][2][1 : N4] that is a posterior L value sequence corresponding to B[1][2][1 : N4] that is the third input bit array information in the second reception MSB information, L[1][2][N4 + 1 : N2] that is a posterior L value sequence corresponding to B[1][2][N4 + 1 : N2] that is a soft decision parity bit in the second reception MSB information, Lv[m][1] that is the second posterior L value sequence, and Lv[m][2] that is the third posterior L value sequence.

[0413] The soft decision error correction decoding unit 241c generates the inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information generated by the bit inversion unit 123 by performing the soft decision error correction processing.

[0414] In addition, the soft decision error correction decoding unit 241c generates the second reception LSB information including the bit array of one row and N2 columns corresponding to the second LSB information generated by the probability distribution shaping encoding unit 122 by performing the soft decision error correction processing.

[0415] In addition, the soft decision error correction decoding unit 241c generates the second reception MSB information including a bit array of one row and N2 columns corresponding to the second MSB information including the third input bit array information generated by the input bit array information generating unit 121c by performing the soft decision error correction processing.

[0416] Since each piece of processing from the second decoding processing to the fifth decoding processing in the multi-stage error correction processing is similar to that of the first embodiment, the description thereof will be omitted.

[0417] The third output bit array generating unit 260 performs eighth decoding processing in the multi-stage error correction processing.

[0418] Specifically, the third output bit array generating unit 260 generates third output bit array information including a bit array of one row and N4 columns corresponding to the third input bit array information by extracting information of an area corresponding to the third input bit area in the second MSB information in the second reception MSB information.

[0419] More specifically, for example, the third output bit array generating unit 260 generates the third output bit array information by extracting bit values from the first column to the N4-th column of the second reception MSB information.

[0420] The output information generating unit 246c performs the sixth decoding processing in the multi-stage error correction processing.

[0421] Specifically, the output information generating unit 246c generates the output information corresponding to the input information on the basis of the third output bit array information in addition to the first output bit array information and the second output bit array information.

[0422] Note that, functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240c, and the information output unit 290 included in the error correction device 200c according to the modification of the first embodiment may be implemented by the processor 901 and the memory 902 in the hardware configuration illustrated as an example in FIGS. 9A and 9B in the first embodiment, or may be implemented by the processing circuit 903.

[0423] Operation of the error correction device 200c according to the modification of the first embodiment will be described with reference to FIGS. 34A, 34B, and 34C.

[0424] FIG. 34A is a part of a flowchart illustrating an example of processing performed by the error correction device 200c according to the modification of the first embodiment.

[0425] FIG. 34B is another part of the flowchart illustrating the example of the processing performed by the error correction device 200c according to the modification of the first embodiment.

[0426] FIG. 34C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device 200c according to the modification of the first embodiment.

[0427] Hereinafter, FIGS. 34A, 34B, and 34C are collectively denoted as FIG. 34.

[0428] The error correction device 200c repeatedly executes the processing of the flowchart illustrated in FIG. 34.

[0429] Note that, the flowchart illustrated in FIG. 34 is obtained by changing step ST1030 in the flowchart illustrated in FIG. 10 to step ST3430.

[0430] In FIG. 34, processing steps similar to processing steps of the flowchart illustrated in FIG. 10 are designated by the same reference numerals, and the description thereof will be omitted.

[0431] First, the error correction device 200c performs processing from step ST1000 to step ST1020.

[0432] After step ST1020, in step ST3430, the decoding unit 240c generates the output information by performing the multi-stage error correction processing.

[0433] Specifically, the decoding unit 240c performs processing of step ST3430 by performing processing of step ST3431, processing from step ST1032 to step ST1036, and processing from step ST3436 to step ST3437 in processing N below.

[0434] First, in step ST3431, the soft decision error cor-

rection decoding unit 241c included in the decoding unit 240c generates the inverted first reception LSB information, the second reception LSB information, and the second reception MSB information by performing the soft decision error correction processing.

[0435] After step ST3431, the decoding unit 240c performs processing from step ST1032 to step ST1035.

[0436] After step ST1035, in step ST3436, the third output bit array generating unit 260 included in the decoding unit 240c generates the third output bit array information.

[0437] After step ST3436, in step ST3437, the output information generating unit 246c included in the decoding unit 240c generates the output information.

[0438] After step ST3437, the decoding unit 240c ends the processing N. That is, after step ST3437, the decoding unit 240c ends the processing of step ST3430.

[0439] After step ST3430, the error correction device 200c performs processing of step ST1050.

[0440] After step ST1050, the error correction device 200c ends the processing of the flowchart illustrated in FIG. 34, and the error correction device 200c returns to the processing of step ST1000 and repeatedly executes the processing of the flowchart illustrated in FIG. 34.

[0441] As described above, the error correction encoding device 100c includes: the input information acquiring unit 110 to acquire the input information; the encoding unit 120c to generate the soft decision error correction frame information including the bit array of m rows and N columns on the basis of the input information acquired by the input information acquiring unit 110, the bit array being obtained by combining the first bit string group information and the second bit string group information, the first bit string group information including the bit array of m rows and N1 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the first bit string group information into the modulation symbol by using the predetermined first symbol mapping rule, the second bit string group information including the bit array of m rows and N2 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the second bit string group information into the modulation symbol by using the predetermined second symbol mapping rule; the modulation symbol conversion unit 130 to generate the modulation symbol group information including N pieces of the modulation symbols by performing the pulse amplitude modulation of the combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit 120c into the modulation symbol for each column of the soft decision error correction frame information by using the first symbol mapping rule or the second symbol mapping rule; and the transmission waveform shaping unit 140 to generate the digital baseband modulation signal on the basis of the modulation symbol group information generated by the modulation symbol conversion unit 130 and output the digital baseband modulation signal generated, in which the encoding unit 120c generates the soft decision error correction frame information by: generating the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit 110; storing the second input bit array information generated as a part of the first MSB information including the bit array of one row and N1 columns in the predetermined area of the first row in the first bit string group information; generating the shaped bit array information including the bit array of m - 1 rows and N columns by performing the probability distribution shaping encoding processing on the first input bit array information generated; generating the first group bit array information including the combination of N1 predetermined columns and the second group bit array information including the combination of N2 predetermined columns by separating the shaped bit array information generated; generating the first LSB information including the bit array of one row and N1 columns by extracting, from the first group bit array information generated, the bit array of the (m - 1)-th row in the first group bit array information, generating the inverted first LSB information including the bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in the information of the first row in the first bit string group information after storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in the m-th row in the first bit string group information; generating the second LSB information including the bit array of one row and N2 columns by extracting the bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated, and storing the second LSB information generated in the m-th row in the second bit string group information; generating the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in the first row in the second bit string group information as the second MSB information including the bit array of one row and N2 columns; in the case where m is greater than or equal to 3, generating the first SSB information including the bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated, the first row to the (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in the second row to the (m - 1)-th row in the first bit string group information; and in the case where m is greater than or equal to 3, generating the second SSB information including the bit array of m - 2 rows and

N2 columns by extracting, from the second group bit array information generated, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the second row to the (m - 1)-th row in the second bit string group information.

[0442] Further, in the above-described configuration, the error correction encoding device 100c is configured so that the encoding unit 120c generates the soft decision error correction frame information by: generating the third input bit array information including the bit array of one row and N4 columns in addition to the first input bit array information and the second input bit array information on the basis of the input information acquired by the input information acquiring unit 110; storing the third input bit array information generated as the part of the second MSB information including the bit array of one row and N2 columns in the predetermined area of the first row in the second bit string group information; and generating the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the third input bit array information stored as the part of the second MSB information in addition to the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in a predetermined area different from an area storing the second bit string group information of the first row of the second bit string group information.

[0443] With this configuration, the error correction encoding device 100c can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction encoding device 100c can reduce the amount of calculation of the soft decision error correction encoding processing as compared with the conventional soft decision error correction encoding processing.

[0444] In addition, with this configuration, the error correction encoding device 100c can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction encoding device 100c can make the amount of calculation of the soft decision error correction encoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction encoding device 100c does not need to change the program or the processing circuit for performing the soft decision error correction encoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0445] Further, with this configuration, the error correction encoding device 100c can transmit the third input bit array information to the error correction device 200c in addition to the first input bit array information and the second input bit array information, so that it is possible to increase the number of pieces of valid information in one piece of soft decision error correction frame information as compared with the error correction encoding device 100 according to the first embodiment. For that reason, the error correction encoding device 100c can efficiently transmit information to the error correction device 200c as compared with the error correction encoding device 100 according to the first embodiment.

[0446] In addition, as described above, the error correction device 200c includes: the reception modulation symbol group information generating unit 210 to receive the reception digital baseband modulation signal that is the signal based on the soft decision error correction frame information generated by the error correction encoding device 100c and generate reception modulation symbol group information including N reception modulation symbols on the basis of the reception digital baseband modulation signal; the hard decision candidate generating unit 220 to generate first hard decision candidate bit array information including the bit array of one row and N1 columns, second hard decision candidate bit array information including the bit array of m - 2 rows and N1 columns in the case where m is greater than or equal to 3, and third hard decision candidate bit array information including the bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210 on the basis of the first symbol mapping rule or the second symbol mapping rule; the soft decision information generating unit 230 to generate the first posterior L value sequence including N2 posterior L values corresponding to each columns of the first row of the second bit string group information, the second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and the third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on the basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210; the decoding unit 240c to perform multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230 ; and the information output unit 290 to output information generated by the decoding unit 240c performing the multi-stage error correction processing as output information, in which: in the first decoding processing in the multi-stage error correction processing, the decoding unit 240c generates inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information and second reception LSB information includ-

ing the bit array of one row and N2 columns corresponding to the second LSB information by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence; in the second decoding processing in the multi-stage error correction processing, the decoding unit 240c generates first reception MSB information including the bit array of one row and N1 columns corresponding to the first MSB information on the basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generates first reception SSB information including the bit array of m - 2 rows and N1 columns corresponding to the first SSB information on the basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generates second reception SSB information including the bit array of m - 2 rows and N2 columns corresponding to the second SSB information on the basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3; in the third decoding processing in the multi-stage error correction processing, the decoding unit 240c generates first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information; in the fourth decoding processing in the multi-stage error correction processing, the decoding unit 240c generates first output bit array information including the bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information; in the fifth decoding processing in the multi-stage error correction processing, the decoding unit 240c generates second output bit array information including the bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of the predetermined area of the first reception MSB information; in the sixth decoding processing in the multi-stage error correction processing, the decoding unit 240c generates the output information corresponding to the input information on the basis of the first output bit array information and the second output bit array information; and the information output unit 290 outputs the output information generated by the decoding unit 240c.

[0447] Further, in the above-described configuration, the error correction device 200c is configured so that the decoding unit 240c: generates the second reception MSB information including the bit array of one row and N2 columns corresponding to the second MSB information, in addition to the inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information and the second reception LSB information including the bit array of one row and N2 columns corresponding to the second LSB information, by performing the soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence, in the first decoding processing in the multi-stage error correction processing; generates the third output bit array information including the bit array of one row and N4 columns corresponding to the third input bit array information by extracting information of a predetermined area of the second reception MSB information in the eighth decoding processing in the multi-stage error correction processing; and generates the output information corresponding to the input information on the basis of the third output bit array information, in addition to the first output bit array information and the second output bit array information, in the sixth decoding processing in the multi-stage error correction processing.

[0448] With this configuration, the error correction device 200c can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction device 200c can reduce the amount of calculation of the soft decision error correction decoding processing as compared with the conventional soft decision error correction decoding processing.

[0449] In addition, with this configuration, the error correction device 200c can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction device 200c can make the amount of calculation of the soft decision error correction decoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction device 200c does not need to change the program or the processing circuit for performing the soft decision error correction decoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0450] Further, with this configuration, the error correction device 200c can restore the third output bit array information corresponding to the third input bit array information by the multi-stage error correction processing in addition to the first output bit array information and the second output bit array information corresponding to the first input bit array information and the second input bit array information.

[0451] Thus, as compared with the error correction device 200 according to the first embodiment, the error correction device 200c can increase the number of pieces of valid information restored from the reception digital baseband modulation signal that is a signal based on one piece of soft decision error correction frame informa-

tion. For that reason, the error correction device 200c can efficiently receive information as compared with the error correction device 200 according to the first embodiment.

Second Embodiment.

[0452] A configuration of a main part of a communication system 1a according to a second embodiment will be described with reference to FIG. 11.

[0453] FIG. 11 is a configuration diagram illustrating an example of the configuration of the main part of the communication system 1a according to the second embodiment.

[0454] In the second embodiment, as an example, the communication system 1a is described as an optical communication system, but the optical communication system is merely an example, and the communication system 1a is not limited to the optical communication system. For example, the communication system 1a may be a communication system by wireless communication, metal communication, or the like.

[0455] The communication system 1a includes a transmission device 10a, the transmission path 30, and a reception device 20a.

[0456] The communication system 1a is obtained by changing the transmission device 10 and the reception device 20 according to the first embodiment to the transmission device 10a and the reception device 20a.

[0457] Note that, in FIG. 11, blocks similar to the blocks illustrated in FIG. 1 are designated by the same reference numerals, and the description thereof will be omitted.

[0458] The transmission device 10a acquires input information and outputs a signal based on the acquired input information. Since the communication system 1a illustrated in FIG. 11 is the optical communication system, the transmission device 10a illustrated in FIG. 11 is an optical transmission device to output an optical signal.

[0459] The transmission device 10a includes an error correction encoding device 100a, the D/A converter 11, the transmission light source 12, and the optical modulator 13.

[0460] The transmission device 10a is obtained by changing the error correction encoding device 100 according to the first embodiment to the error correction encoding device 100a.

[0461] The error correction encoding device 100a acquires the input information input from the outside of the device, and generates a digital baseband modulation signal on the basis of the acquired input information. The error correction encoding device 100a outputs the generated digital baseband modulation signal to the D/A converter 11.

[0462] The reception device 20a receives the signal output by the transmission device 10a via the transmission path 30, generates output information corresponding to the input information on the basis of the signal, and outputs the generated output information. Since the communication system 1a illustrated in FIG. 11 is the optical communication system, the reception device 20a illustrated in FIG. 11 is an optical reception device to receive the optical signal.

[0463] The reception device 20a includes the reception light source 22, the optical receiver 21, the A/D converter 23, and an error correction device 200a.

[0464] The reception device 20a is obtained by changing the error correction device 200 according to the first embodiment to the error correction device 200a.

[0465] The error correction device 200a receives the reception digital baseband modulation signal output by the A/D converter 23, generates the output information corresponding to the input information on the basis of the reception digital baseband modulation signal, and outputs the generated output information.

[0466] A configuration of a main part of the error correction encoding device 100a according to the second embodiment will be described with reference to FIG. 12.

[0467] FIG. 12 is a configuration diagram illustrating an example of the configuration of the main part of the error correction encoding device 100a according to the second embodiment.

[0468] The error correction encoding device 100a includes the input information acquiring unit 110, an encoding unit 120a, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140.

[0469] The error correction encoding device 100a is obtained by changing the encoding unit 120 according to the first embodiment to the encoding unit 120a.

[0470] Note that, in FIG. 12, blocks similar to the blocks illustrated in FIG. 2 are designated by the same reference numerals, and the description thereof will be omitted.

[0471] The encoding unit 120a generates soft decision error correction frame information obtained by combining the first bit string group information and the second bit string group information on the basis of the input information acquired by the input information acquiring unit 110.

[0472] A configuration of a main part of the encoding unit 120a according to the second embodiment will be described with reference to FIG. 13.

[0473] FIG. 13 is a configuration diagram illustrating an example of the main part of the encoding unit 120a according to the second embodiment.

[0474] The encoding unit 120a includes the input bit array information generating unit 121, the probability distribution shaping encoding unit 122, the bit inversion unit 123, the soft decision error correction encoding unit 124, and the hard decision error correction encoding unit 125.

[0475] The encoding unit 120a is obtained by adding the hard decision error correction encoding unit 125 to the configuration of the encoding unit 120 according to the first embodiment.

[0476] Note that, in FIG. 13, blocks similar to the blocks illustrated in FIG. 3 are designated by the same reference numerals, and the description thereof will be omitted.

[0477] The hard decision error correction encoding unit

125 performs systematic hard decision error correction encoding processing by using the first input bit array information generated by the input bit array information generating unit 121 and the second input bit array information generated by the input bit array information generating unit 121.

[0478] The hard decision error correction encoding unit 125 may perform the systematic hard decision error correction encoding processing by using the first input bit array information generated by the input bit array information generating unit 121, and the first SSB information, the second SSB information, the second LSB information, and the first LSB information generated by the probability distribution shaping encoding unit 122.

[0479] In addition, the hard decision error correction encoding unit 125 may perform the systematic hard decision error correction encoding processing by using the first input bit array information generated by the input bit array information generating unit 121, the first SSB information, the second SSB information, and the second LSB information generated by the probability distribution shaping encoding unit 122, and the inverted first LSB information generated by the bit inversion unit 123.

[0480] FIG. 13 is a diagram illustrating a case where the hard decision error correction encoding unit 125 performs the systematic hard decision error correction encoding processing by using the first input bit array information generated by the input bit array information generating unit 121, and the first SSB information, the second SSB information, the second LSB information, and the first LSB information generated by the probability distribution shaping encoding unit 122.

[0481] The hard decision error correction encoding unit 125 generates a hard decision parity bit by performing the systematic hard decision error correction encoding processing, and stores the generated hard decision parity bit as a part of the first MSB information in a predetermined area (Hereinafter, the predetermined area is referred to as a "hard decision parity area".) different from the second input bit area of the first row in the first bit string group information.

[0482] Specifically, the hard decision error correction encoding unit 125 stores the generated hard decision parity bit in the hard decision parity area of Dv[1][1] that is a bit array space in which the first MSB is stored. Hereinafter, the description will be given assuming that the hard decision parity area is D[1][1][N3 + 1 : N1].

[0483] As the systematic hard decision error correction encoding processing, a BCH code, a Reed-Solomon code, or the like is used.

[0484] Note that, functions of the input information acquiring unit 110, the encoding unit 120a, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140 included in the error correction encoding device 100a according to the second embodiment may be implemented by the processor 501 and the memory 502 in the hardware configuration illustrated as an example in FIGS. 5A and 5B in the first embodiment, or may be implemented by the processing circuit 503.

[0485] Operation of the error correction encoding device 100a according to the second embodiment will be described with reference to FIGS. 14A, 14B, and 14C.

[0486] FIG. 14A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device 100a according to the second embodiment.

[0487] FIG. 14B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100a according to the second embodiment.

[0488] FIG. 14C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100a according to the second embodiment.

[0489] Hereinafter, FIGS. 14A, 14B, and 14C are collectively denoted as FIG. 14.

[0490] The error correction encoding device 100a repeatedly executes the processing of the flowchart illustrated in FIG. 14.

[0491] Note that, the flowchart illustrated in FIG. 14 is obtained by changing step ST610 in the flowchart illustrated in FIG. 6 to step ST1410.

[0492] In addition, the flowchart illustrated in FIG. 14 illustrates, as an example, operation in a case where the hard decision error correction encoding unit 125 performs the systematic hard decision error correction encoding processing by using the first input bit array information generated by the input bit array information generating unit 121, and the first SSB information, the second SSB information, the second LSB information, and the first LSB information generated by the probability distribution shaping encoding unit 122.

[0493] In FIG. 14, processing steps similar to processing steps of the flowchart illustrated in FIG. 6 are designated by the same reference numerals, and the description thereof will be omitted.

[0494] First, the error correction encoding device 100a performs processing of step ST601.

[0495] Next, in step ST1410, the encoding unit 120a generates the soft decision error correction frame information.

[0496] Specifically, the encoding unit 120a performs processing of step ST1410 by performing processing from step ST611 to step ST618, and processing from step ST1411 to step ST1412 in processing I below.

[0497] First, the encoding unit 120a performs the processing from step ST611 to step ST614.

[0498] After step ST614, in step ST1411, the hard decision error correction encoding unit 125 included in the encoding unit 120a performs the systematic hard decision error correction encoding processing by using the first input bit array information, the first SSB information, the second SSB information, the second LSB information, and the first LSB information.

[0499] Next, in step ST1412, the hard decision error correction encoding unit 125 included in the encoding

unit 120a stores the hard decision parity bit in the hard decision parity area of Dv[1][1].

[0500] After step ST1412, the encoding unit 120a performs the processing from step ST615 to step ST618.

[0501] After step ST618, the encoding unit 120a ends the processing I. That is, after step ST618, the encoding unit 120a ends the processing of step ST1410.

[0502] After step ST1410, the error correction encoding device 100a performs processing from step ST620 to step ST630.

[0503] After step ST630, the error correction encoding device 100a ends the processing of the flowchart illustrated in FIG. 14, and the error correction encoding device 100a returns to the processing of step ST601 and repeatedly executes the processing of the flowchart illustrated in FIG. 14.

[0504] A configuration of a main part of the error correction device 200a according to the second embodiment will be described with reference to FIG. 15.

[0505] FIG. 15 is a configuration diagram illustrating an example of the main part of the error correction device 200a according to the second embodiment.

[0506] The error correction device 200a includes the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, a decoding unit 240a, and the information output unit 290.

[0507] The error correction device 200a is obtained by changing the decoding unit 240 according to the first embodiment to the decoding unit 240a.

[0508] Note that, in FIG. 15, blocks similar to the blocks illustrated in FIG. 7 are designated by the same reference numerals, and the description thereof will be omitted.

[0509] The decoding unit 240a generates the output information by performing the multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230.

[0510] A configuration of a main part of the decoding unit 240a according to the second embodiment will be described with reference to FIG. 16.

[0511] FIG. 16 is a configuration diagram illustrating an example of the configuration of the main part of the decoding unit 240a according to the second embodiment.

[0512] The decoding unit 240a includes the soft decision error correction decoding unit 241, the selection unit 242, the reception side bit inversion unit 243, the probability distribution shaping decoding unit 244, the second output bit array generating unit 245, the output information generating unit 246, and a hard decision error correction decoding unit 247.

[0513] The decoding unit 240a is obtained by adding the hard decision error correction decoding unit 247 to the configuration of the decoding unit 240 according to the first embodiment.

[0514] Note that, in FIG. 16, blocks similar to the blocks illustrated in FIG. 8 are designated by the same reference numerals, and the description thereof will be omitted.

[0515] The hard decision error correction decoding unit 247 performs seventh decoding processing in the multi-stage error correction processing.

[0516] The hard decision error correction decoding unit 247 performs hard decision error correction processing on information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the inverted first reception LSB information on the basis of information stored in an area (Hereinafter, the area is referred to as a "reception hard decision parity area".) that is a predetermined area of the first reception MSB information and corresponds to the hard decision parity area of the first MSB information.

[0517] The hard decision error correction decoding unit 247 may perform the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information on the basis of the information stored in the reception hard decision parity area of the first reception MSB information.

[0518] In addition, the hard decision error correction decoding unit 247 may perform the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first output bit array information on the basis of the information stored in the reception hard decision parity area of the first reception MSB information.

[0519] FIG. 16 is a diagram illustrating a case where the hard decision error correction decoding unit 247 performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information on the basis of the information stored in the reception hard decision parity area of the first reception MSB information.

[0520] Note that, in a case where the hard decision error correction decoding unit 247 performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the inverted first reception LSB information, the reception side bit inversion unit 243 calculates an exclusive OR by using the

inverted first reception LSB information after the seventh decoding processing and the first reception MSB information in the third decoding processing, and the second output bit array generating unit 245 generates the second output bit array information by extracting information of a predetermined area of the first reception MSB information after the seventh decoding processing in the fifth decoding processing.

[0521] In addition, in a case where the hard decision error correction decoding unit 247 performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information, the probability distribution shaping decoding unit 244 performs the probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information after the seventh decoding processing in the fourth decoding processing, and the second output bit array generating unit 245 generates the second output bit array information by extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing in the fifth decoding processing.

[0522] In addition, in a case where the hard decision error correction decoding unit 247 performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first output bit array information, the second output bit array generating unit 245 generates the second output bit array information by extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing in the fifth decoding processing, and the output information generating unit 246 generates the output information on the basis of the second output bit array information and the first output bit array information after the seventh decoding processing in the sixth decoding processing.

[0523] The error correction device 200a can obtain output information with less residual error by performing error correction by the hard decision error correction processing as compared with a case where the hard decision error correction processing is not performed.

[0524] Note that, functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240a, and the information output unit 290 included in the error correction device 200a according to the second embodiment may be implemented by the processor 901 and the memory 902 in the hardware configuration illustrated as an example in FIGS. 9A and 9B in the first embodiment, or may be implemented by the processing circuit 903.

[0525] Operation of the error correction device 200a according to the second embodiment will be described with reference to FIGS. 17A, 17B, and 17C.

[0526] FIG. 17A is a part of a flowchart illustrating an example of processing performed by the error correction device 200a according to the second embodiment.

[0527] FIG. 17B is another part of the flowchart illustrating the example of the processing performed by the error correction device 200a according to the second embodiment.

[0528] FIG. 17C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device 200a according to the second embodiment.

[0529] Hereinafter, FIGS. 17A, 17B, and 17C are collectively denoted as FIG. 17.

[0530] The error correction device 200a repeatedly executes the processing of the flowchart illustrated in FIG. 17.

[0531] Note that, the flowchart illustrated in FIG. 17 is obtained by changing step ST1030 in the flowchart illustrated in FIG. 10 to step ST1730.

[0532] In addition, the flowchart illustrated in FIG. 17 illustrates, as an example, operation in a case where the hard decision error correction decoding unit 247 performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information on the basis of the information stored in the reception hard decision parity area of the first reception MSB information.

[0533] In FIG. 17, processing steps similar to processing steps of the flowchart illustrated in FIG. 10 are designated by the same reference numerals, and the description thereof will be omitted.

[0534] First, the error correction device 200a performs processing from step ST1000 to step ST1020.

[0535] After step ST1020, in step ST1730, the decoding unit 240a generates the output information by performing the multi-stage error correction processing.

[0536] Specifically, the decoding unit 240a performs processing of step ST1730 by performing processing from step ST1031 to step ST1036 and processing of step ST1731 in processing J below.

[0537] The decoding unit 240a performs processing from step ST1031 to step ST1033.

[0538] After step ST1033, in step ST1731, the hard decision error correction decoding unit 247 included in the decoding unit 240a performs the hard decision error correction processing.

[0539] After step ST1731, the decoding unit 240a performs processing from step ST1034 to step ST1036.

[0540] After step ST1036, the decoding unit 240a ends the processing J. That is, after step ST1036, the decoding unit 240a ends the processing of step ST1730.

[0541] After step ST1730, the error correction device 200a performs processing of step ST1050.

[0542] After step ST1050, the error correction device 200a ends the processing of the flowchart illustrated in FIG. 17, and the error correction device 200a returns to the processing of step ST1000 and repeatedly executes the processing of the flowchart illustrated in FIG. 17.

[0543] As described above, the error correction encoding device 100a includes: the input information acquiring unit 110 to acquire the input information; the encoding unit 120a to generate the soft decision error correction frame information including the bit array of m rows and N columns on the basis of the input information acquired by the input information acquiring unit 110, the bit array being obtained by combining the first bit string group information and the second bit string group information, the first bit string group information including the bit array of m rows and N1 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the first bit string group information into the modulation symbol by using the predetermined first symbol mapping rule, the second bit string group information including the bit array of m rows and N2 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the second bit string group information into the modulation symbol by using the predetermined second symbol mapping rule; the modulation symbol conversion unit 130 to generate the modulation symbol group information including N pieces of the modulation symbols by performing the pulse amplitude modulation of the combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit 120a into the modulation symbol for each column of the soft decision error correction frame information by using the first symbol mapping rule or the second symbol mapping rule; and the transmission waveform shaping unit 140 to generate the digital baseband modulation signal on the basis of the modulation symbol group information generated by the modulation symbol conversion unit 130 and output the digital baseband modulation signal generated, in which the encoding unit 120a generates the soft decision error correction frame information by: generating the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit 110; storing the second input bit array information generated as a part of the first MSB information including the bit array of one row and N1 columns in the predetermined area of the first row in the first bit string group information; generating the shaped bit array information including the bit array of m - 1 rows and N columns by performing the probability distribution shaping encoding processing on the first input bit array information generated; generating the first group bit array information including the combination of N1 predetermined columns and the second group bit array information including the combination of N2 predetermined columns by separating the shaped bit array information generated; generating the first LSB information including the bit array of one row and N1 columns by extracting, from the first group bit array information generated, the bit array of the (m - 1)-th row in the first group bit array information, generating the inverted first LSB information including the bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in the information of the first row in the first bit string group information after storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in the m-th row in the first bit string group information; generating the second LSB information including the bit array of one row and N2 columns by extracting the bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated, and storing the second LSB information generated in the m-th row in the second bit string group information; generating the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in the first row in the second bit string group information as the second MSB information including the bit array of one row and N2 columns; in the case where m is greater than or equal to 3, generating the first SSB information including the bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated, the first row to the (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in the second row to the (m - 1)-th row in the first bit string group information; and in the case where m is greater than or equal to 3, generating the second SSB information including the bit array of m - 2 rows and N2 columns by extracting, from the second group bit array information generated, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the second row to the (m - 1)-th row in the second bit string group information.

[0544] Further, in the above-described configuration, the error correction encoding device 100a is configured so that the encoding unit 120a generates the hard decision parity bit by performing the systematic hard decision error correction encoding processing, by using the first input bit array information and the second input bit array information, or by using the first input bit array information, the first SSB information, the second SSB information, the second LSB information, and the first LSB information or the inverted first LSB information, and stores the hard decision parity bit generated, as the part of the first MSB information in the predetermined area different from the area storing the second input bit array informa-

tion of the first row in the first bit string group information.

[0545] With this configuration, the error correction encoding device 100a can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction encoding device 100a can reduce the amount of calculation of the soft decision error correction encoding processing as compared with the conventional soft decision error correction encoding processing.

[0546] In addition, with this configuration, the error correction encoding device 100a can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction encoding device 100a can make the amount of calculation of the soft decision error correction encoding processing constant in the pulse amplitude modulation of any number of bits. Thus, the error correction encoding device 100a does not need to change the program or the processing circuit for performing the soft decision error correction encoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0547] In addition, with this configuration, it is possible to perform the error correction by the hard decision error correction processing in the error correction device 200a, so that the error correction encoding device 100a can cause the error correction device 200a to output information with less residual error as compared with the case where the hard decision error correction processing is not performed.

[0548] Note that, the hard decision error correction encoding unit 125 included in the encoding unit 120a may store the second MSB information that is the soft decision parity bit generated by the soft decision error correction encoding unit 124 performing the systematic soft decision error correction encoding processing in Dv[1][2] that is the bit array space of the first row in the second bit string group information, and then perform the systematic hard decision error correction encoding processing on the basis of the second input bit array information stored in the second input bit area, the second MSB information stored in Dv[1][2], and the first SSB information, the second SSB information, the inverted first LSB information, and the second LSB information stored in Dv[2 : m][1 : 2].

[0549] With this configuration, the error correction encoding device 100a can reduce a burst error of the second reception MSB information corresponding to the soft decision parity bit that is the second MSB information, in the soft decision error correction decoding processing in the error correction device 200a.

[0550] In addition, as described above, the error correction device 200a includes: the reception modulation symbol group information generating unit 210 to receive the reception digital baseband modulation signal that is the signal based on the soft decision error correction frame information generated by the error correction encoding device 100a and generate reception modulation symbol group information including N reception modulation symbols on the basis of the reception digital baseband modulation signal; the hard decision candidate generating unit 220 to generate first hard decision candidate bit array information including the bit array of one row and N1 columns, second hard decision candidate bit array information including the bit array of m - 2 rows and N1 columns in the case where m is greater than or equal to 3, and third hard decision candidate bit array information including the bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210 on the basis of the first symbol mapping rule or the second symbol mapping rule; the soft decision information generating unit 230 to generate the first posterior L value sequence including N2 posterior L values corresponding to each columns of the first row of the second bit string group information, the second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and the third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on the basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210; the decoding unit 240a to perform multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230 ; and the information output unit 290 to output information generated by the decoding unit 240a performing the multi-stage error correction processing as output information, in which: in the first decoding processing in the multi-stage error correction processing, the decoding unit 240a generates inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information and second reception LSB information including the bit array of one row and N2 columns corresponding to the second LSB information by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence; in the second decoding processing in the multi-stage error correction processing, the decoding unit 240a generates first reception MSB information including the bit array of one row and N1 columns corresponding to the first MSB information on the basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generates first reception

SSB information including the bit array of m - 2 rows and N1 columns corresponding to the first SSB information on the basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generates second reception SSB information including the bit array of m - 2 rows and N2 columns corresponding to the second SSB information on the basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3; in the third decoding processing in the multi-stage error correction processing, the decoding unit 240a generates first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information; in the fourth decoding processing in the multi-stage error correction processing, the decoding unit 240a generates first output bit array information including the bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information; in the fifth decoding processing in the multi-stage error correction processing, the decoding unit 240a generates second output bit array information including the bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of the predetermined area of the first reception MSB information; in the sixth decoding processing in the multi-stage error correction processing, the decoding unit 240a generates the output information corresponding to the input information on the basis of the first output bit array information and the second output bit array information; and the information output unit 290 outputs the output information generated by the decoding unit 240a.

[0551] Further, in the above-described configuration, the error correction device 200a is configured so that: the decoding unit 240a performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information or the inverted first reception LSB information, or on the information corresponding to the second output bit array information of the first reception MSB information and the first output bit array information, on the basis of the information stored in the predetermined area of the first reception MSB information, in the seventh decoding processing in the multi-stage error correction processing; and in a case where the decoding unit 240a performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the inverted first reception LSB information, the decoding unit 240a generates the second output bit array information by calculating the exclusive OR by using the inverted first reception LSB information and the first reception MSB information after the seventh decoding processing, in the third decoding processing, and extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing; and in a case where the decoding unit 240a performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information, the decoding unit 240a generates the second output bit array information by performing the probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information after the seventh decoding processing, in the fourth decoding processing, and extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing; and in a case where the decoding unit 240a performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first output bit array information, the decoding unit 240a generates the second output bit array information by extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing, and generates the output information on the basis of the second output bit array information and the first output bit array information after the seventh decoding processing, in the sixth decoding processing.

[0552] With this configuration, the error correction device 200a can reduce the number of bits to be protected by the soft decision error correction as compared with the conventional soft decision error correction encoding processing. For that reason, the error correction device 200a can reduce the amount of calculation of the soft decision error correction decoding processing as compared with the conventional soft decision error correction decoding processing.

[0553] In addition, with this configuration, the error correction device 200a can make the number of bits to be protected by the soft decision error correction constant even if the number of bits of the pulse amplitude modulation changes. For that reason, the error correction device 200a can make the amount of calculation of the soft decision error correction decoding processing constant

in the pulse amplitude modulation of any number of bits. Thus, the error correction device 200a does not need to change the program or the processing circuit for performing the soft decision error correction decoding processing for each number of bits of the pulse amplitude modulation, in the pulse amplitude modulation of a plurality of number of bits.

[0554] In addition, with this configuration, the error correction device 200a can perform the error correction by the hard decision error correction processing, so that it is possible to output information with less residual error as compared with the case where the hard decision error correction processing is not performed.

Modification of Second Embodiment.

[0555] A modification of the second embodiment is a particularly effective embodiment in a case where the input information is information corresponding to the second input bit array information and the information includes information of the number of bits less than N3, or in a case where the input information does not include information corresponding to the first input bit array information or the second input bit array information.

[0556] Hereinafter, the description will be given assuming that the input information includes the first input bit array information including a bit array of m - 1 rows and N columns and information corresponding to the second input bit array information including N5 (N5 is an integer of greater than or equal to 0 and less than N3.) bits.

[0557] A configuration of a main part of a communication system 1d according to the modification of the second embodiment will be described with reference to FIG. 35.

[0558] FIG. 35 is a configuration diagram illustrating an example of the configuration of the main part of the communication system 1d according to the modification of the second embodiment.

[0559] In the modification of the second embodiment, as an example, the communication system 1d is described as an optical communication system, but the optical communication system is merely an example, and the communication system 1d is not limited to the optical communication system. For example, the communication system 1d may be a communication system by wireless communication, metal communication, or the like.

[0560] The communication system 1d includes a transmission device 10d, the transmission path 30, and a reception device 20d.

[0561] The communication system 1d is obtained by changing the transmission device 10a and the reception device 20a according to the second embodiment to the transmission device 10d and the reception device 20d.

[0562] Note that, in FIG. 35, blocks similar to the blocks illustrated in FIG. 11 are designated by the same reference numerals, and the description thereof will be omitted.

[0563] The transmission device 10d acquires input information and outputs a signal based on the acquired input information. Since the communication system 1d illustrated in FIG. 35 is the optical communication system, the transmission device 10d illustrated in FIG. 35 is an optical transmission device to output an optical signal.

[0564] The transmission device 10d includes an error correction encoding device 100d, the D/A converter 11, the transmission light source 12, and the optical modulator 13.

[0565] The transmission device 10d is obtained by changing the error correction encoding device 100a according to the second embodiment to the error correction encoding device 100d.

[0566] The error correction encoding device 100d acquires the input information input from the outside of the device, and generates a digital baseband modulation signal on the basis of the acquired input information. The error correction encoding device 100d outputs the generated digital baseband modulation signal to the D/A converter 11.

[0567] The reception device 20d receives the signal output by the transmission device 10d via the transmission path 30, generates output information corresponding to the input information on the basis of the signal, and outputs the generated output information. Since the communication system 1d illustrated in FIG. 35 is the optical communication system, the reception device 20d illustrated in FIG. 35 is an optical reception device to receive the optical signal.

[0568] The reception device 20d includes the reception light source 22, the optical receiver 21, the A/D converter 23, and an error correction device 200d.

[0569] The reception device 20d is obtained by changing the error correction device 200a according to the second embodiment to the error correction device 200d.

[0570] The error correction device 200d receives the reception digital baseband modulation signal output by the A/D converter 23, generates the output information corresponding to the input information on the basis of the reception digital baseband modulation signal, and outputs the generated output information.

[0571] A configuration of a main part of the error correction encoding device 100d according to the modification the second embodiment will be described with reference to FIG. 36.

[0572] FIG. 36 is a configuration diagram illustrating an example of the configuration of the main part of the error correction encoding device 100d according to the modification of the second embodiment.

[0573] The error correction encoding device 100d includes the input information acquiring unit 110, an encoding unit 120d, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140.

[0574] The error correction encoding device 100d is obtained by changing the encoding unit 120a according to the second embodiment to the encoding unit 120d.

[0575] Note that, in FIG. 36, blocks similar to the blocks

illustrated in FIG. 12 are designated by the same reference numerals, and the description thereof will be omitted.

[0576] The encoding unit 120d generates soft decision error correction frame information obtained by combining the first bit string group information and the second bit string group information on the basis of the input information acquired by the input information acquiring unit 110.

[0577] A configuration of a main part of the encoding unit 120d according to the modification of the second embodiment will be described with reference to FIG. 37.

[0578] FIG. 37 is a configuration diagram illustrating an example of the configuration of the main part of the encoding unit 120d according to the modification of the second embodiment.

[0579] The encoding unit 120d includes an input bit array information generating unit 121d, the probability distribution shaping encoding unit 122, the bit inversion unit 123, the soft decision error correction encoding unit 124, and a hard decision error correction encoding unit 125d.

[0580] The encoding unit 120d is obtained by changing the input bit array information generating unit 121 and the hard decision error correction encoding unit 125 according to the second embodiment to the input bit array information generating unit 121d and the hard decision error correction encoding unit 125d.

[0581] Note that, in FIG. 37, blocks similar to the blocks illustrated in FIG. 13 are designated by the same reference numerals, and the description thereof will be omitted.

[0582] The input bit array information generating unit 121d generates the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit 110.

[0583] Specifically, for example, the input bit array information generating unit 121d generates the first input bit array information by extracting the first input bit array information including the bit array of m - 1 rows and N columns included in the input information.

[0584] In addition, when generating the second input bit array information on the basis of the input information acquired by the input information acquiring unit 110, the input bit array information generating unit 121d generates the second input bit array information by setting a bit value of a bit other than a bit corresponding to the input information to a predetermined value in the second input bit array information.

[0585] More specifically, for example, the input bit array information generating unit 121d generates the second input bit array information by extracting information corresponding to the second input bit array information including the N5 bits included in the input information, setting a part of the second input bit array information as the information, and setting a remaining part of the second input bit array information to the predetermined value.

[0586] The value to be applied to the remaining part of the second input bit array information is, for example, "0". The value may be "1". In addition, if it is an array of predetermined values, an array of any values using "0" or " 1" for each column in the remaining part of the second input bit array information may be used.

[0587] The input bit array information generating unit 121d stores the generated second input bit array information in the second input bit area, as a part of the first MSB information including a bit array of one row and N1 columns.

[0588] Specifically, the input bit array information generating unit 121d stores the second input bit array information in the second input bit area of Dv[1][1] that is a bit array space in which the first MSB is stored. Hereinafter, the description will be given assuming that the second input bit area is D[1][1][1 : N3].

[0589] In particular, in the modification of the second embodiment, the description will be given assuming that the information including the N5 bits extracted from the input information by the input bit array information generating unit 121d is stored in D[1][1][1 : N5] of D[1][1][1 : N3] that is the second input bit area. In addition, the description will be given assuming that the remaining part of the second input bit array information set to the predetermined value for generating the second input bit array information by the input bit array information generating unit 121d is stored in D[1][1][N5 + 1 : N3] of D[1][1][1 : N3] that is the second input bit area. That is, the predetermined value such as "0" or "1" is stored in D[1][1][N5 + 1 : N3].

[0590] The hard decision error correction encoding unit 125d performs systematic hard decision error correction encoding processing by using the first input bit array information generated by the input bit array information generating unit 121d and the second input bit array information generated by the input bit array information generating unit 121d.

[0591] When performing the systematic hard decision error correction encoding processing, the hard decision error correction encoding unit 125d performs the following processing as preprocessing.

[0592] As first preprocessing, the hard decision error correction encoding unit 125d switches bit values of columns corresponding to each other between a bit value of an area storing the predetermined value, of a predetermined area of the first row in the first bit string group information storing the second input bit array information as the part of the first MSB information, and a bit value of a column corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, of an area of the m-th row in the first bit string group information storing the first LSB information.

[0593] As second preprocessing, the hard decision er-

ror correction encoding unit 125d calculates an exclusive OR for each of the columns corresponding to each other between a bit value after switching the bit value of the area storing the predetermined value, of the predetermined area of the first row in the first bit string group information, and a bit value after switching the bit value of the column corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, of the area of the m-th row in the first bit string group information.

[0594] As third preprocessing, the hard decision error correction encoding unit 125d overwrites the bit value after switching the bit value in the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, by using a calculation result of the exclusive OR in the columns corresponding to each other.

[0595] Specifically, as the first preprocessing, the hard decision error correction encoding unit 125d first switches values of the columns corresponding to each other between B[1][1][N5 + 1 : N3] that are bit values of D[1][1][N5 + 1 : N3] and B[m][1][N5 + 1 : N3] that are bit values of D[m][1][N5 + 1 : N3].

[0596] Next, as the second preprocessing, the hard decision error correction encoding unit 125d calculates the exclusive OR for each of the columns corresponding to each other between B[1][1][N5 + 1 : N3] after switching the values and B[m][1][N5 + 1 : N3] after switching the values.

[0597] Next, as the third preprocessing, the hard decision error correction encoding unit 125d overwrites each of values of B[1][1][N5 + 1 : N3] after switching the values by using a calculation result of the exclusive OR in the columns corresponding to each other.

[0598] After performing the above-described preprocessing, the hard decision error correction encoding unit 125d generates a hard decision parity bit by performing the systematic hard decision error correction encoding processing, and stores the generated hard decision parity bit as a part of the first MSB information in the hard decision parity area.

[0599] Specifically, the hard decision error correction encoding unit 125d stores the generated hard decision parity bit in the hard decision parity area of Dv[1][1] that is a bit array space in which the first MSB is stored. Hereinafter, the description will be given assuming that the hard decision parity area is D[1][1][N3 + 1 : N1].

[0600] Note that, functions of the input information acquiring unit 110, the encoding unit 120d, the modulation symbol conversion unit 130, and the transmission waveform shaping unit 140 included in the error correction encoding device 100d according to the modification of the second embodiment may be implemented by the processor 501 and the memory 502 in the hardware configuration illustrated as an example in FIGS. 5A and 5B in the second embodiment, or may be implemented by the processing circuit 503.

[0601] Operation of the error correction encoding device 100d according to the modification of the second embodiment will be described with reference to FIGS. 38A, 38B, and 38C.

[0602] FIG. 38A is a part of a flowchart illustrating an example of processing performed by the error correction encoding device 100d according to the modification of the second embodiment.

[0603] FIG. 38B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100d according to the modification of the second embodiment.

[0604] FIG. 38C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100d according to the modification of the second embodiment.

[0605] Hereinafter, FIGS. 38A, 38B, and 38C are collectively denoted as FIG. 38.

[0606] The error correction encoding device 100d repeatedly executes the processing of the flowchart illustrated in FIG. 38.

[0607] Note that, the flowchart illustrated in FIG. 38 is obtained by changing step ST1410 in the flowchart illustrated in FIG. 14 to step ST3810.

[0608] In FIG. 38, processing steps similar to processing steps of the flowchart illustrated in FIG. 14 are designated by the same reference numerals, and the description thereof will be omitted.

[0609] First, the error correction encoding device 100d performs processing of step ST601.

[0610] Next, in step ST3810, the encoding unit 120d generates the soft decision error correction frame information.

[0611] Specifically, the encoding unit 120d performs processing of step ST3810 by performing processing from step ST612 to step ST618, processing from step ST1411 to step ST1412, processing of step ST3811, and processing from step ST3815 to step ST3817 in processing O below.

[0612] First, in step ST3811, the input bit array information generating unit 121d included in the encoding unit 120d generates the first input bit array information and the second input bit array information.

[0613] After step ST3811, the encoding unit 120d performs the processing from step ST611 to step ST614.

[0614] After step ST614, in step ST3815, the hard decision error correction encoding unit 125d included in the encoding unit 120d switches the values of B[1][1][N5 + 1 : N3] with the values of B[m][1][N5 + 1 : N3].

[0615] After step ST3815, in step ST3816, the hard decision error correction encoding unit 125d included in the encoding unit 120d calculates exclusive ORs of B[1][1][N5 + 1 : N3] and B[m][1][N5 + 1 : N3].

[0616] After step ST3816, in step ST3817, the hard decision error correction encoding unit 125d included in the encoding unit 120d overwrites the values of B[1][1][N5 + 1 : N3] with calculation results of the exclusive ORs.

[0617] After step ST3817, the encoding unit 120d performs the processing from step ST1411 to step ST1412.

[0618] After step ST1412, the encoding unit 120d performs the processing from step ST615 to step ST618.

[0619] After step ST618, the encoding unit 120d ends the processing O. That is, after step ST618, the encoding unit 120d ends the processing of step ST3810.

[0620] After step ST3810, the error correction encoding device 100d performs processing from step ST620 to step ST630.

[0621] After step ST630, the error correction encoding device 100d ends the processing of the flowchart illustrated in FIG. 38, and the error correction encoding device 100d returns to the processing of step ST601 and repeatedly executes the processing of the flowchart illustrated in FIG. 38.

[0622] A configuration of a main part of the error correction device 200d according to the modification of the second embodiment will be described with reference to FIG. 39.

[0623] FIG. 39 is a configuration diagram illustrating an example of the configuration of the main part of the error correction device 200d according to the modification of the second embodiment.

[0624] The error correction device 200d includes the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, a decoding unit 240d, and the information output unit 290.

[0625] The error correction device 200d is obtained by changing the decoding unit 240a according to the second embodiment to the decoding unit 240d.

[0626] Note that, in FIG. 39, blocks similar to the blocks illustrated in FIG. 15 are designated by the same reference numerals, and the description thereof will be omitted.

[0627] The decoding unit 240d generates the output information by performing the multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230.

[0628] A configuration of a main part of the decoding unit 240d according to the modification of the second embodiment will be described with reference to FIG. 40.

[0629] FIG. 40 is a configuration diagram illustrating an example of the configuration of the main part of the decoding unit 240d according to the modification of the second embodiment.

[0630] The decoding unit 240d includes the soft decision error correction decoding unit 241, the selection unit 242, the reception side bit inversion unit 243, the probability distribution shaping decoding unit 244, a second output bit array generating unit 245d, the output information generating unit 246, and a hard decision error correction decoding unit 247d.

[0631] The decoding unit 240d is obtained by changing the second output bit array generating unit 245 and the hard decision error correction decoding unit 247 according to the second embodiment to the second output bit array generating unit 245d and the hard decision error correction decoding unit 247d.

[0632] Note that, in FIG. 40, blocks similar to the blocks illustrated in FIG. 16 are designated by the same reference numerals, and the description thereof will be omitted.

[0633] The hard decision error correction decoding unit 247d performs seventh decoding processing in the multi-stage error correction processing.

[0634] The hard decision error correction decoding unit 247d performs hard decision error correction processing on information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the inverted first reception LSB information on the basis of information stored in the reception hard decision parity area corresponding to the hard decision parity area of the first MSB information, which is a predetermined area of the first reception MSB information.

[0635] After performing the hard decision error correction processing, the hard decision error correction decoding unit 247d performs processing below as post-processing, in the seventh decoding processing in the multi-stage error correction processing.

[0636] First, as first post-processing, the hard decision error correction decoding unit 247d calculates an exclusive OR for each of columns corresponding to each other between a bit value of a column in the first reception MSB information corresponding to one of the columns of an area storing a predetermined value in a predetermined area of the first row in the first bit string group information storing the second input bit array information as a part of the first MSB information, and a bit value of a column in the first reception LSB information corresponding to one of the columns of the area storing the predetermined value in the predetermined area of the first row in the first bit string group information storing the second input bit array information as the part of the first MSB information.

[0637] Next, as second post-processing, the hard decision error correction decoding unit 247d overwrites the bit value of the column in the first reception MSB information corresponding to one of the columns of the area storing the predetermined value in the predetermined area of the first row in the first bit string group information, by using a calculation result of the exclusive OR in the columns corresponding to each other.

[0638] Specifically, first, as the first post-processing, the hard decision error correction decoding unit 247d calculates the exclusive OR for each of the columns corre-

sponding to each other between values from the (N5 + 1)-th column to the N3-th column of the first reception MSB information corresponding to B[1][1][N5 + 1 : N3] that are bit values of D[1][1][N5 + 1 : N3] that is a bit array space in which the first MSB information is stored, and values from the (N5 + 1)-th column to the N3-th column of the first reception LSB information corresponding to B[m][1][N5 + 1 : N3] that are bit values of D[m][1][N5+ 1 : N3] that is a bit array space in which the first LSB information is stored. When performing the first post-processing, the hard decision error correction decoding unit 247d may use N3 - N5 predetermined fixed values stored in D[1][1][N5 + 1 : N3] when the input bit array information generating unit 121d included in the encoding unit 120d of the error correction encoding device 100d generates the second input bit array information, instead of the values from the (N5 + 1)-th column to the N3-th column of the first reception LSB information, and calculate the exclusive OR for each of the columns corresponding to each other between the values from the (N5 + 1)-th column to the N3-th column of the first reception MSB information and the N3 -N5 predetermined fixed values. Hereinafter, the description will be given assuming that, as the first post-processing, the hard decision error correction decoding unit 247d calculates the exclusive OR for each of the columns corresponding to each other between the values from the (N5 + 1)-th column to the N3-th column of the first reception MSB information and the values from the (N5 + 1)-th column to the N3-th column of the first reception LSB information.

[0639] Next, as the second post-processing, the hard decision error correction decoding unit 247d overwrites each of the values from the (N5 + 1)-th column to the N3-th column of the first reception LSB information by using the calculation result of the exclusive OR in the columns corresponding to each other.

[0640] The second output bit array generating unit 245d performs the fifth decoding processing in the multi-stage error correction processing.

[0641] Specifically, the second output bit array generating unit 245d generates the second output bit array information including a bit array of one row and N5 columns corresponding to the information including the N5 bits included in the input information by extracting information in an area of the first reception MSB information corresponding to an area storing the information corresponding to the second input bit array information including the N5 bits included in the input information, of an area in which the error correction encoding device 100d stores the first MSB information.

[0642] More specifically, for example, the second output bit array generating unit 245d generates the second output bit array information by extracting bit values from the first column to the N5-th column of the area in which the error correction encoding device 100d stores the first MSB information.

[0643] The error correction device 200d can obtain output information with less residual error by performing error correction by the hard decision error correction processing as compared with the case where the hard decision error correction processing is not performed.

[0644] In particular, the error correction device 200d can perform the error correction with higher performance as compared with the error correction in the error correction device 200a according to the second embodiment, by performing the multi-stage error correction processing on the basis of the reception digital baseband modulation signal that is a signal based on the soft decision error correction frame information generated by the error correction encoding device 100d described above.

[0645] Note that, functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240d, and the information output unit 290 included in the error correction device 200d according to the modification of the second embodiment may be implemented by the processor 901 and the memory 902 in the hardware configuration illustrated as an example in FIGS. 9A and 9B in the second embodiment, or may be implemented by the processing circuit 903.

[0646] Operation of the error correction device 200d according to the modification of the second embodiment will be described with reference to FIGS. 41A, 41B, and 41C.

[0647] FIG. 41Ais a part of a flowchart illustrating an example of processing performed by the error correction device 200d according to the modification of the second embodiment.

[0648] FIG. 41B is another part of the flowchart illustrating the example of the processing performed by the error correction device 200d according to the modification of the second embodiment.

[0649] FIG. 41C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device 200d according to the modification of the second embodiment.

[0650] Hereinafter, FIGS. 41A, 41B, and 41C are collectively denoted as FIG. 41.

[0651] The error correction device 200d repeatedly executes the processing of the flowchart illustrated in FIG. 41.

[0652] Note that, the flowchart illustrated in FIG. 41 is obtained by changing step ST1730 in the flowchart illustrated in FIG. 17 to step ST4130.

[0653] In FIG. 41, processing steps similar to processing steps of the flowchart illustrated in FIG. 17 are designated by the same reference numerals, and the description thereof will be omitted.

[0654] First, the error correction device 200d performs processing from step ST1000 to step ST1020.

[0655] After step ST1020, in step ST4130, the decoding unit 240d generates the output information by performing the multi-stage error correction processing.

[0656] Specifically, the decoding unit 240d performs processing of step ST4130 by performing processing

from step ST1031 to step ST1034 and step ST1036, processing of step ST1731, and processing from step ST4132 to step ST4133 and step ST4135 in processing P below.

[0657] More specifically, first, the decoding unit 240d performs the processing from step ST1031 to step ST1033.

[0658] After step ST1033, the decoding unit 240d performs the processing of step ST1731.

[0659] After step ST1731, in step ST4132, the hard decision error correction decoding unit 247d included in the decoding unit 240d calculates exclusive ORs of the values from the (N5 + 1)-th column to the N3-th column of the first reception MSB information and the values from the (N5 + 1)-th column to the N3-th column of the first reception LSB information.

[0660] After step ST4132, in step ST4133, the hard decision error correction decoding unit 247d included in the decoding unit 240d overwrites the values from the (N5 + 1)-th column to the N3-th column of the first reception LSB information with the calculation results of the exclusive OR in the columns corresponding to each other.

[0661] After step ST4133, the decoding unit 240d performs the processing of step ST1034.

[0662] After step ST1034, in step ST4135, the second output bit array generating unit 245d included in the decoding unit 240d generates the second output bit array information including the bit array of one row and N5 columns.

[0663] After step ST4135, the decoding unit 240d performs the processing of step ST1036.

[0664] After step ST1036, the decoding unit 240d ends the processing P. That is, after step ST1036, the decoding unit 240d ends the processing of step ST4130.

[0665] After step ST4130, the error correction device 200d performs processing of step ST1050.

[0666] After step ST1050, the error correction device 200d ends the processing of the flowchart illustrated in FIG. 41, and the error correction device 200d returns to the processing of step ST1000 and repeatedly executes the processing of the flowchart illustrated in FIG. 41.

[0667] As described above, the error correction encoding device 100d includes: the input information acquiring unit 110 to acquire the input information; the encoding unit 120d to generate the soft decision error correction frame information including the bit array of m rows and N columns on the basis of the input information acquired by the input information acquiring unit 110, the bit array being obtained by combining the first bit string group information and the second bit string group information, the first bit string group information including the bit array of m rows and N1 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the first bit string group information into the modulation symbol by using the predetermined first symbol mapping rule, the second bit string group information including the bit array of m rows and N2 columns in which it is enabled to perform the pulse amplitude modulation of the combination of bit values of each column of the second bit string group information into the modulation symbol by using the predetermined second symbol mapping rule; the modulation symbol conversion unit 130 to generate the modulation symbol group information including N pieces of the modulation symbols by performing the pulse amplitude modulation of the combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit 120d into the modulation symbol for each column of the soft decision error correction frame information by using the first symbol mapping rule or the second symbol mapping rule; and the transmission waveform shaping unit 140 to generate the digital baseband modulation signal on the basis of the modulation symbol group information generated by the modulation symbol conversion unit 130 and output the digital baseband modulation signal generated, in which the encoding unit 120d generates the soft decision error correction frame information by: generating the first input bit array information including the bit array of m - 1 rows and N columns and the second input bit array information including the bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit 110; storing the second input bit array information generated as a part of the first MSB information including the bit array of one row and N1 columns in the predetermined area of the first row in the first bit string group information; generating the shaped bit array information including the bit array of m - 1 rows and N columns by performing the probability distribution shaping encoding processing on the first input bit array information generated; generating the first group bit array information including the combination of N1 predetermined columns and the second group bit array information including the combination of N2 predetermined columns by separating the shaped bit array information generated; generating the first LSB information including the bit array of one row and N1 columns by extracting, from the first group bit array information generated, the bit array of the (m - 1)-th row in the first group bit array information, generating the inverted first LSB information including the bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in the information of the first row in the first bit string group information after storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in the m-th row in the first bit string group information; generating the second LSB information including the bit array of one row and N2 columns by extracting the bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated, and storing the second LSB information gen-

erated in the m-th row in the second bit string group information; generating the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in the first row in the second bit string group information as the second MSB information including the bit array of one row and N2 columns; in the case where m is greater than or equal to 3, generating the first SSB information including the bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated, the first row to the (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in the second row to the (m - 1)-th row in the first bit string group information; and in the case where m is greater than or equal to 3, generating the second SSB information including the bit array of m - 2 rows and N2 columns by extracting, from the second group bit array information generated, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the second row to the (m - 1)-th row in the second bit string group information.

[0668] Further, in the above-described configuration, the error correction encoding device 100d is configured so that the encoding unit 120d generates the hard decision parity bit by performing the systematic hard decision error correction encoding processing, by using the first input bit array information and the second input bit array information, or by using the first input bit array information, the first SSB information, the second SSB information, the second LSB information, and the first LSB information or the inverted first LSB information, and stores the hard decision parity bit generated, as the part of the first MSB information in the predetermined area different from the area storing the second input bit array information of the first row in the first bit string group information.

[0669] Further, in the above-described configuration, the error correction encoding device 100d is configured so that: the encoding unit 120d generates the second input bit array information by setting the bit value of the bit other than the bit corresponding to the input information to the predetermined value in the second input bit array information when generating the second input bit array information on the basis of the input information acquired by the input information acquiring unit 110; and the encoding unit 120d, when performing the systematic hard decision error correction encoding processing, as the first preprocessing, switches the bit values of the columns corresponding to each other between the bit value of the area storing the predetermined value, of the predetermined area of the first row in the first bit string group information storing the second input bit array information as the part of the first MSB information, and the bit value of the column corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, of the area of the m-th row in the first bit string group information storing the first LSB information, and as the second preprocessing, calculates the exclusive OR for each of the columns corresponding to each other between the bit value after switching the bit value of the area storing the predetermined value, of the predetermined area of the first row in the first bit string group information, and the bit value after switching the bit value of the column corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, of the area of the m-th row in the first bit string group information, and as the third preprocessing, overwrites the bit value after switching the bit value of the area storing the predetermined value, of the predetermined area of the first row in the first bit string group information, by using the calculation result of the exclusive OR in the columns corresponding to each other.

[0670] With this configuration, the error correction device 200d can perform the error correction with higher performance as compared with the error correction device 200a according to the second embodiment that performs the error correction by the hard decision error correction processing, so that the error correction encoding device 100d can cause the error correction device 200d to output the output information with less residual error as compared with the case where the hard decision error correction processing is not performed.

[0671] In addition, as described above, the error correction device 200d includes: the reception modulation symbol group information generating unit 210 to receive the reception digital baseband modulation signal that is the signal based on the soft decision error correction frame information generated by the error correction encoding device 100d and generate reception modulation symbol group information including N reception modulation symbols on the basis of the reception digital baseband modulation signal; the hard decision candidate generating unit 220 to generate first hard decision candidate bit array information including the bit array of one row and N1 columns, second hard decision candidate bit array information including the bit array of m - 2 rows and N1 columns in the case where m is greater than or equal to 3, and third hard decision candidate bit array information including the bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210 on the basis of the first symbol mapping rule or the second symbol mapping rule; the soft decision information generating unit 230 to generate the first posterior L value sequence including N2 posterior L values corresponding to each columns of the first row of the second bit string group information, the second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and the third posterior L value sequence including N2 posterior L values corre-

sponding to each columns of the m-th row of the second bit string group information on the basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit 210; the decoding unit 240d to perform multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230 ; and the information output unit 290 to output information generated by the decoding unit 240d performing the multi-stage error correction processing as output information, in which: in the first decoding processing in the multi-stage error correction processing, the decoding unit 240d generates inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information and second reception LSB information including the bit array of one row and N2 columns corresponding to the second LSB information by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence; in the second decoding processing in the multi-stage error correction processing, the decoding unit 240d generates first reception MSB information including the bit array of one row and N1 columns corresponding to the first MSB information on the basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generates first reception SSB information including the bit array of m - 2 rows and N1 columns corresponding to the first SSB information on the basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generates second reception SSB information including the bit array of m - 2 rows and N2 columns corresponding to the second SSB information on the basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3; in the third decoding processing in the multi-stage error correction processing, the decoding unit 240d generates first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information; in the fourth decoding processing in the multi-stage error correction processing, the decoding unit 240d generates first output bit array information including the bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information; in the fifth decoding processing in the multi-stage error correction processing, the decoding unit 240d generates second output bit array information including the bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of the predetermined area of the first reception MSB information; in the sixth decoding processing in the multi-stage error correction processing, the decoding unit 240d generates the output information corresponding to the input information on the basis of the first output bit array information and the second output bit array information; and the information output unit 290 outputs the output information generated by the decoding unit 240d.

[0672] Further, in the above-described configuration, the error correction device 200d is configured so that: the decoding unit 240d performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information or the inverted first reception LSB information, or on the information corresponding to the second output bit array information of the first reception MSB information and the first output bit array information, on the basis of the information stored in the predetermined area of the first reception MSB information, in the seventh decoding processing in the multi-stage error correction processing; and in a case where the decoding unit 240d performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the inverted first reception LSB information, the decoding unit 240d generates the second output bit array information by calculating the exclusive OR by using the inverted first reception LSB information and the first reception MSB information after the seventh decoding processing, in the third decoding processing, and extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing; and in a case where the decoding unit 240d performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information, the decoding unit 240d generates the second output bit array information by performing the probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception

LSB information, and the second reception LSB information after the seventh decoding processing, in the fourth decoding processing, and extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing; and in a case where the decoding unit 240d performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first output bit array information, the decoding unit 240d generates the second output bit array information by extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing, and generates the output information on the basis of the second output bit array information and the first output bit array information after the seventh decoding processing, in the sixth decoding processing.

[0673] Further, in the above-described configuration, the error correction device 200d is configured so that the decoding unit 240d performs the hard decision error correction processing, and then, in the seventh decoding processing in the multi-stage error correction processing, as the first post-processing, calculates the exclusive OR for each of columns corresponding to each other between the bit value of the column in the first reception MSB information corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information storing the second input bit array information as the part of the first MSB information, and the bit value of the column in the first reception LSB information corresponding to one of the columns of the area storing the predetermined value in the predetermined area in the first row in the first bit string group information storing the second input bit array information as the part of the first MSB information, and as the second post-processing, overwrites the bit value of the column in the first reception MSB information corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, by using the calculation result of the exclusive OR in the columns corresponding to each other.

[0674] With this configuration, the error correction device 200d can perform the error correction with higher performance as compared with the error correction device 200a according to the second embodiment that performs the error correction by the hard decision error correction processing.

Third Embodiment.

[0675] A configuration of a main part of a communication system 1b according to a third embodiment will be described with reference to FIG. 18.

[0676] FIG. 18 is a configuration diagram illustrating an example of the configuration of the main part of the communication system 1b according to the third embodiment.

[0677] In the third embodiment, as an example, the communication system 1b is described as an optical communication system, but the optical communication system is merely an example, and the communication system 1b is not limited to the optical communication system. For example, the communication system 1b may be a communication system by wireless communication, metal communication, or the like.

[0678] The communication system 1b includes a transmission device 10b, the transmission path 30, and a reception device 20b.

[0679] The communication system 1b is obtained by changing the transmission device 10 and the reception device 20 according to the first embodiment to the transmission device 10b and the reception device 20b.

[0680] Note that, in FIG. 18, blocks similar to the blocks illustrated in FIG. 1 are designated by the same reference numerals, and the description thereof will be omitted.

[0681] The transmission device 10b acquires input information and outputs a signal based on the acquired input information. Since the communication system 1b illustrated in FIG. 18 is the optical communication system, the transmission device 10b illustrated in FIG. 18 is an optical transmission device to output an optical signal.

[0682] The transmission device 10b includes an error correction encoding device 100b, the D/A converter 11, the transmission light source 12, and the optical modulator 13.

[0683] The transmission device 10b is obtained by changing the error correction encoding device 100 according to the first embodiment to the error correction encoding device 100b.

[0684] The error correction encoding device 100b acquires the input information input from the outside of the device, and generates a digital baseband modulation signal on the basis of the acquired input information. The error correction encoding device 100b outputs the generated digital baseband modulation signal to the D/A converter 11.

[0685] The reception device 20b receives the signal output by the transmission device 10b via the transmission path 30, generates output information corresponding to the input information on the basis of the signal, and outputs the generated output information. Since the communication system 1b illustrated in FIG. 18 is the optical communication system, the reception device 20b illustrated in FIG. 18 is an optical reception device to receive the optical signal.

[0686] The reception device 20b includes the reception light source 22, the optical receiver 21, the A/D converter 23, and an error correction device 200b.

[0687] The reception device 20b is obtained by changing the error correction device 200 according to the first embodiment to the error correction device 200b.

[0688] The error correction device 200b receives the reception digital baseband modulation signal output by the A/D converter 23, generates the output information

corresponding to the input information on the basis of the reception digital baseband modulation signal, and outputs the generated output information.

[0689] A configuration of a main part of the error correction encoding device 100b according to the third embodiment will be described with reference to FIG. 19.

[0690] FIG. 19 is a configuration diagram illustrating an example of the configuration of the main part of the error correction encoding device 100b according to the third embodiment.

[0691] The error correction encoding device 100b includes the input information acquiring unit 110, an encoding unit 120b, the modulation symbol conversion unit 130, the transmission waveform shaping unit 140, and an interleaving unit 150.

[0692] The error correction encoding device 100b is obtained by adding the interleaving unit 150 to the configuration of the error correction encoding device 100 according to the first embodiment, and changing the encoding unit 120 according to the first embodiment to the encoding unit 120b.

[0693] Note that, in FIG. 19, blocks similar to the blocks illustrated in FIG. 2 are designated by the same reference numerals, and the description thereof will be omitted.

[0694] The encoding unit 120b generates soft decision error correction frame information obtained by combining the first bit string group information and the second bit string group information on the basis of the input information acquired by the input information acquiring unit 110.

[0695] Details of the encoding unit 120b will be described later.

[0696] The interleaving unit 150 switches information of any column with information of any other column, in the soft decision error correction frame information generated by the encoding unit 120b, on the basis of a predetermined switching rule (Hereinafter, it is referred to as a "first switching rule".).

[0697] A bit array space in which the soft decision error correction frame information is stored will be described with reference to FIG. 25.

[0698] Note that, D that is a bit array space in which the soft decision error correction frame information illustrated in FIG. 25 is stored, illustrates, as an example, a case where N1 and N2 are equal.

[0699] FIG. 25A is an explanatory diagram illustrating an example of the bit array space in which soft decision error correction frame information before the interleaving unit 150 performs switching is stored.

[0700] As illustrated in FIG. 25A, in D that is a bit array space in which the soft decision error correction frame information before the interleaving unit 150 performs switching is stored, Dd[1] that is a bit array space of m rows and N1 columns in which the first bit string group information is stored and Dd[1] that is a bit array space of m rows and N2 columns in which the second bit string group information is stored are arranged in one bit array space.

[0701] The interleaving unit 150 switches information of any column with information of any other column, in D that is the bit array space illustrated in FIG. 25A, on the basis of the first switching rule.

[0702] FIG. 25B is an explanatory diagram illustrating an example of the bit array space in which soft decision error correction frame information after the interleaving unit 150 performs switching is stored.

[0703] For example, as illustrated in FIG. 25B, the interleaving unit 150 switches arrangements of columns in the soft decision error correction frame information so that D[1 : m][2][k] that is a bit array space storing information of the k-th column of the second bit string group information is disposed between D[1 : m][1][k] that is a bit array space storing information of the k-th column of the first bit string group information and D[1 : m][1][k + 1].

[0704] The bit array space illustrated in FIG. 25B is merely an example, and as long as the interleaving unit 150 performs switching on the basis of the first switching rule, the mode of the bit array space after performing switching is not limited to the bit array space illustrated in FIG. 25B.

[0705] The modulation symbol conversion unit 130 performs pulse amplitude modulation on the basis of the soft decision error correction frame information after performing switching of the interleaving unit 150 columns.

[0706] The modulation symbol group information stored in the bit array space in which the modulation symbol group information generated by the modulation symbol conversion unit 130 is stored will be described with reference to FIG. 26.

[0707] FIG. 26A is an explanatory diagram illustrating an example of the modulation symbol group information in a case where the error correction encoding device 100b does not include the interleaving unit 150.

[0708] As illustrated in FIG. 26A, in the modulation symbol group information in the case where the error correction encoding device 100b does not include the interleaving unit 150, Xv[1] that is the first modulation symbol group information and Xv[2] that is the second modulation symbol group information are arranged in one bit array space.

[0709] FIG. 26B is an explanatory diagram illustrating an example of the modulation symbol group information in a case where the error correction encoding device 100b includes the interleaving unit 150.

[0710] As illustrated in FIG. 26B, in the modulation symbol group information in the case where the error correction encoding device 100b includes the interleaving unit 150, X[2][k] that is a PAM symbol belonging to Xv[2] that is the second modulation symbol group information is disposed between X[1][k] and X[1][k + 1] that are PAM symbols belonging to Xv[1] that is the first modulation symbol group information so that the modulation symbol group information corresponds to the soft decision error correction frame information after the interleaving unit 150 performs the switching as illustrated as an example in FIG. 25B.

[0711] Note that, the interleaving unit 150 may switch information of any column with information of any other column, in the modulation symbol group information generated by the modulation symbol conversion unit 130, on the basis of the first switching rule.

[0712] Hereinafter, the description will be given assuming that the interleaving unit 150 switches information of any column with information of any other column, in the soft decision error correction frame information generated by the encoding unit 120b, on the basis of the first permutation rule.

[0713] A configuration of a main part of the encoding unit 120b according to the third embodiment will be described with reference to FIG. 20.

[0714] FIG. 20 is a configuration diagram illustrating an example of the main part of the encoding unit 120b according to the third embodiment.

[0715] The encoding unit 120b includes the input bit array information generating unit 121, the probability distribution shaping encoding unit 122, the bit inversion unit 123, the soft decision error correction encoding unit 124, an LSB interleaving unit 126, and an LSB deinterleaving unit 127.

[0716] The encoding unit 120b is obtained by adding the LSB interleaving unit 126 and the LSB deinterleaving unit 127 to the configuration of the encoding unit 120 according to the first embodiment.

[0717] Note that, in FIG. 20, blocks similar to the blocks illustrated in FIG. 3 are designated by the same reference numerals, and the description thereof will be omitted.

[0718] The LSB interleaving unit 126 switches information of any column in the inverted first LSB information generated by the bit inversion unit 123 with information of any other column in the inverted first LSB information, on the basis of a predetermined switching rule (Hereinafter, it is referred to as a "second switching rule".).

[0719] In addition, the LSB interleaving unit 126 switches information of any column in the second LSB information generated by the probability distribution shaping encoding unit 122 with information of any other column in the second LSB information, on the basis of the second switching rule.

[0720] A bit array space in which the inverted first LSB information and the second LSB information are stored will be described with reference to FIG. 27.

[0721] FIG. 27A is an explanatory diagram illustrating an example of a bit array space in which soft decision error correction frame information before the LSB interleaving unit 126 performs switching is stored.

[0722] As illustrated in FIG. 27A, in the inverted first LSB information before the LSB interleaving unit 126 performs switching, D[1 : m - 1][1][k] in which the k-th information in the first MSB information and the second SSB information is stored and D[m][1][k] in which the k-th information in the inverted first LSB information is stored are arranged in one column in Dd[1] that is a bit array space in which the first bit string group information is stored.

[0723] In addition, as illustrated in FIG. 27A, in the second LSB information before the LSB interleaving unit 126 performs switching, D[1 : m - 1][2][k] in which the k-th information in the second MSB information and the second SSB information is stored and D[m][2][k] in which the k-th information in the second LSB information is stored are arranged in one column in Dd[2] that is a bit array space in which the second bit string group information is stored.

[0724] The LSB interleaving unit 126 switches information of any column with information of any other column, in Dv[m][1] in which the inverted first LSB information illustrated in FIG. 27A is stored, on the basis of the second switching rule.

[0725] In addition, the LSB interleaving unit 126 switches information of any column with information of any other column, in Dv[m][2] in which the second LSB information illustrated in FIG. 27A is stored, on the basis of the second switching rule.

[0726] FIG. 27B is an explanatory diagram illustrating an example of the bit array space in which soft decision error correction frame information after the LSB interleaving unit 126 performs switching is stored.

[0727] For example, as illustrated in FIG. 27B, the LSB interleaving unit 126 switches arrangements of columns in the inverted first LSB information so that pieces of information of odd-numbered columns in the inverted first LSB information are adjacent to each other, and pieces of information of even-numbered columns in the inverted first LSB information are adjacent to each other, in Dv[m][1] in which the inverted first LSB information is stored.

[0728] In addition, for example, as illustrated in FIG. 27B, the LSB interleaving unit 126 switches arrangements of columns in the second LSB information so that pieces of information of odd-numbered columns in the second LSB information are adjacent to each other, and pieces of information of even-numbered columns in the second LSB information are adjacent to each other, in Dv[m][2] in which the second LSB information is stored.

[0729] Note that, the function f() illustrated in FIG. 27B is a ceiling function.

[0730] The bit array space illustrated in FIG. 27B is merely an example, and as long as the LSB interleaving unit 126 performs switching on the basis of the second switching rule, the mode of the bit array space after performing switching is not limited to the bit array space illustrated in FIG. 27B.

[0731] The modulation symbol conversion unit 130 performs pulse amplitude modulation on the basis of the soft decision error correction frame information after performing switching of the interleaving unit 150 columns.

[0732] The soft decision error correction encoding unit 124 generates a soft decision parity bit by performing systematic soft decision error correction encoding processing by using the inverted first LSB information and the second LSB information after the LSB interleaving unit 126 performs switching. The soft decision error

correction encoding unit 124 stores the generated soft decision parity bit as the second MSB information in Dv[1][2] that is a bit array space.

[0733] On the basis of the second switching rule, the LSB deinterleaving unit 127 restores the arrangements of the columns in the inverted first LSB information after the soft decision error correction encoding unit 124 generates the soft decision parity bit, to a state before the LSB interleaving unit 126 switches the arrangements of the columns.

[0734] In addition, on the basis of the second switching rule, the LSB deinterleaving unit 127 restores the arrangements of the columns in the second LSB information after the soft decision error correction encoding unit 124 generates the soft decision parity bit, to a state before the LSB interleaving unit 126 switches the arrangements of the columns.

[0735] In addition, the LSB deinterleaving unit 127 switches the arrangements of the columns of the soft decision parity bit stored as the second MSB information in Dv[1][2] that is the bit array space on the basis of the second switching rule, to cause an arrangement of a column of the soft decision parity bit stored in Dv[1][2] to be an arrangement of a column similar to a case where the encoding unit 120b does not include the LSB interleaving unit 126.

[0736] Note that, functions of the input information acquiring unit 110, the encoding unit 120b, the modulation symbol conversion unit 130, the transmission waveform shaping unit 140, and the interleaving unit 150 included in the error correction encoding device 100b according to the third embodiment may be implemented by the processor 501 and the memory 502 in the hardware configuration illustrated as an example in FIGS. 5A and 5B in the first embodiment, or may be implemented by the processing circuit 503.

[0737] Operation of the error correction encoding device 100b according to the third embodiment will be described with reference to FIGS. 21A, 21B, and 21C.

[0738] FIG. 21Ais a part of a flowchart illustrating an example of processing performed by the error correction encoding device 100b according to the third embodiment.

[0739] FIG. 21B is another part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100b according to the third embodiment.

[0740] FIG. 21C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction encoding device 100b according to the third embodiment.

[0741] Hereinafter, FIGS. 21A, 21B, and 21C are collectively denoted as FIG. 21.

[0742] The error correction encoding device 100b repeatedly executes the processing of the flowchart illustrated in FIG. 21.

[0743] Note that, the flowchart illustrated in FIG. 21 is obtained by changing step ST610 in the flowchart illustrated in FIG. 6 to step ST2110, and adding step ST2120 between step ST610 and step ST620.

[0744] In FIG. 21, processing steps similar to processing steps of the flowchart illustrated in FIG. 6 are designated by the same reference numerals, and the description thereof will be omitted.

[0745] First, the error correction encoding device 100b performs processing of step ST601.

[0746] Next, in step ST2110, the encoding unit 120b generates the soft decision error correction frame information.

[0747] Specifically, the encoding unit 120b performs processing of step ST2110 by performing processing from step ST611 to step ST618, and processing from step ST2111 to step ST2115 in processing K below.

[0748] First, the encoding unit 120b performs the processing from step ST611 to step ST616.

[0749] After step ST616, in step ST2111, the LSB interleaving unit 126 included in the encoding unit 120b switches the arrangements of the columns in the inverted first LSB information.

[0750] Next, in step ST2112, the LSB interleaving unit 126 included in the encoding unit 120b switches the arrangements of the columns in the second LSB information.

[0751] After step ST2112, the encoding unit 120b performs the processing of step ST617 and step ST618.

[0752] After step ST618, in step ST2113, the LSB deinterleaving unit 127 included in the encoding unit 120b restores the arrangements of the columns in the inverted first LSB information to the state before the LSB interleaving unit 126 switches the arrangements of the columns.

[0753] Next, in step ST2114, the LSB deinterleaving unit 127 included in the encoding unit 120b restores the arrangements of the columns in the second LSB information to the state before the LSB interleaving unit 126 switches the arrangements of the columns.

[0754] Next, in step ST2115, the LSB deinterleaving unit 127 included in the encoding unit 120b switches the arrangements of the column of the soft decision parity bit.

[0755] After step ST2115, the encoding unit 120b ends the processing K. That is, after step ST2115, the encoding unit 120b ends the processing of step ST2110.

[0756] Note that, the order of the processing of step ST2111 and step ST2112 is any order, and the order of the processing from step ST2113 to ST2115 is any order.

[0757] After step ST2110, in step ST2120, the interleaving unit 150 switches information of any column with information of any other column, in the soft decision error correction frame information.

[0758] After step ST2120, the error correction encoding device 100b performs processing from step ST620 to step ST630.

[0759] After step ST630, the error correction encoding device 100b ends the processing of the flowchart illustrated in FIG. 21, and the error correction encoding device 100b returns to the processing of step ST601 and repeatedly executes the processing of the flowchart illustrated

in FIG. 21.

[0760] A configuration of a main part of the error correction device 200b according to the third embodiment will be described with reference to FIG. 22. FIG. 22 is a configuration diagram illustrating an example of the main part of the error correction device 200b according to the third embodiment.

[0761] The error correction device 200b includes the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, a decoding unit 240b, a deinterleaving unit 250, and the information output unit 290.

[0762] The error correction device 200b is obtained by adding the deinterleaving unit 250 to the configuration of the error correction device 200 according to the first embodiment, and changing the decoding unit 240 according to the first embodiment to the decoding unit 240b.

[0763] Note that, in FIG. 22, blocks similar to the blocks illustrated in FIG. 7 are designated by the same reference numerals, and the description thereof will be omitted.

[0764] The deinterleaving unit 250 switches the arrangements of the columns of each of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230, on the basis of the first switching rule, thereby restoring the arrangements of the columns of each of the first hard decision candidate bit array information, the second hard decision candidate bit array information, the third hard decision candidate bit array information, the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence to cause them to be the arrangements equivalent to the arrangements of the columns of each of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230 in the case where the error correction encoding device 100b does not include the interleaving unit 150.

[0765] Note that, the deinterleaving unit 250 may switch the arrangements of the reception PAM symbols in the reception modulation symbol group information generated by the reception modulation symbol generating unit 212 on the basis of the first switching rule, thereby restoring the arrangements of the reception PAM symbols to cause them to be the arrangements equivalent to the arrangements of the reception PAM symbols in the reception modulation symbol group information generated by the reception modulation symbol generating unit 212 in the case where the error correction encoding device 100b does not include the interleaving unit 150.

[0766] Hereinafter, the description will be given assuming that the deinterleaving unit 250 switches the arrangements of the columns of each of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit 220, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit 230.

[0767] The decoding unit 240b generates the output information by performing the multi-stage error correction processing on the basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, the third hard decision candidate bit array information, the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence.

[0768] A configuration of a main part of the decoding unit 240b according to the third embodiment will be described with reference to FIG. 23.

[0769] FIG. 23 is a configuration diagram illustrating an example of the configuration of the main part of the decoding unit 240b according to the third embodiment.

[0770] The decoding unit 240b includes the soft decision error correction decoding unit 241, the selection unit 242, the reception side bit inversion unit 243, the probability distribution shaping decoding unit 244, the second output bit array generating unit 245, the output information generating unit 246, a reception LSB interleaving unit 248, and a reception LSB deinterleaving unit 249.

[0771] The decoding unit 240b is obtained by adding the reception LSB interleaving unit 248 and the reception LSB deinterleaving unit 249 to the configuration of the decoding unit 240 according to the first embodiment. is added.

[0772] Note that, in FIG. 23, blocks similar to the blocks illustrated in FIG. 8 are designated by the same reference numerals, and the description thereof will be omitted.

[0773] The reception LSB interleaving unit 248 switches the arrangements of the columns in the second posterior L value sequence by switching information of any column in the second posterior L value sequence with information of any other column in the second posterior L value sequence on the basis of the second switching rule.

[0774] In addition, the reception LSB interleaving unit 248 switches the arrangements of the columns in the third posterior L value sequence by switching information of any column in the third posterior L value sequence with information of any other column in the third posterior L value sequence on the basis of the second switching rule.

[0775] The soft decision error correction decoding unit

241 performs the soft decision error correction processing by using the first posterior L value sequence, the second posterior L value sequence after the reception LSB interleaving unit 248 performs the switching, and the third posterior L value sequence after the reception LSB interleaving unit 248 performs the switching.

[0776] The reception LSB deinterleaving unit 249 switches the arrangements of the columns in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241, on the basis of the second switching rule, thereby switching the arrangements of the columns in the inverted first reception LSB information to cause them to be equivalent to the arrangements of the columns in the inverted first reception LSB information generated by the soft decision error correction decoding unit 241 in a case where the decoding unit 240b does not include the reception LSB interleaving unit 248.

[0777] In addition, the reception LSB deinterleaving unit 249 switches the arrangements of the columns in the second reception LSB information generated by the soft decision error correction decoding unit 241, on the basis of the second switching rule, thereby switching the arrangements of the columns in the second reception LSB information to cause them to be equivalent to the arrangements of the columns in the second reception LSB information generated by the soft decision error correction decoding unit 241 in the case where the decoding unit 240b does not include the reception LSB interleaving unit 248.

[0778] Note that, functions of the reception modulation symbol group information generating unit 210, the hard decision candidate generating unit 220, the soft decision information generating unit 230, the decoding unit 240b, the deinterleaving unit 250, and the information output unit 290 included in the error correction device 200b according to the third embodiment may be implemented by the processor 901 and the memory 902 in the hardware configuration illustrated as an example in FIGS. 9A and 9B in the first embodiment, or may be implemented by the processing circuit 903.

[0779] Operation of the error correction device 200b according to the third embodiment will be described with reference to FIGS. 24A, 24B, and 24C.

[0780] FIG. 24A is a part of a flowchart illustrating an example of processing performed by the error correction device 200b according to the third embodiment.

[0781] FIG. 24B is another part of the flowchart illustrating the example of the processing performed by the error correction device 200b according to the third embodiment.

[0782] FIG. 24C is a remaining part of the flowchart illustrating the example of the processing performed by the error correction device 200b according to the third embodiment.

[0783] Hereinafter, FIGS. 24A, 24B, and 24C are collectively denoted as FIG. 24.

[0784] The error correction device 200b repeatedly executes the processing of the flowchart illustrated in FIG. 24.

[0785] Note that, the flowchart illustrated in FIG. 24 is obtained by adding step ST2420 between processing steps of step ST1020 and step ST1030 in the flowchart illustrated in FIG. 10, and changing step ST1030 to ST2430.

[0786] In FIG. 24, processing steps similar to processing steps of the flowchart illustrated in FIG. 10 are designated by the same reference numerals, and the description thereof will be omitted.

[0787] First, the error correction device 200b performs processing from step ST1000 to step ST1020.

[0788] After step ST1020, in step ST2420, the deinterleaving unit 250 switches the arrangements of the columns of each of the first hard decision candidate bit array information, the second hard decision candidate bit array information, the third hard decision candidate bit array information, the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence.

[0789] After step ST2420, in step ST2430, the decoding unit 240b generates the output information by performing the multi-stage error correction processing.

[0790] Specifically, the decoding unit 240b performs processing of step ST2430 by performing processing from step ST1031 to step ST1036, and processing from step ST2431 to step ST2433 in processing L below.

[0791] In step ST2431, the reception LSB interleaving unit 248 included in the decoding unit 240b switches the arrangements of the columns of each of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence.

[0792] After step ST2431, the decoding unit 240b performs the processing of step ST1031.

[0793] After step ST1031, in step ST2432, the reception LSB deinterleaving unit 249 included in the decoding unit 240b switches the arrangements of the columns of the inverted first reception LSB information.

[0794] Next, in step ST2433, the reception LSB deinterleaving unit 249 included in the decoding unit 240b switches the arrangements of the columns of the second reception LSB information.

[0795] After step ST2433, the decoding unit 240b performs the processing from step ST1032 to step ST1036.

[0796] After step ST1036, the decoding unit 240b ends the processing L. That is, after step ST1036, the decoding unit 240b ends the processing of step ST2430.

[0797] After step ST2430, the error correction device 200b performs processing of step ST1050.

[0798] After step ST1050, the error correction device 200b ends the processing of the flowchart illustrated in FIG. 24, and the error correction device 200b returns to the processing of step ST1000 and repeatedly executes the processing of the flowchart illustrated in FIG. 24.

[0799] With this configuration, the error correction encoding device 100b can disperse a burst error occurring in the transmission path 30. For that reason, the error

correction encoding device 100b can suppress performance degradation of the soft decision error correction decoding processing in the error correction device 200b.

[0800] Note that, in the above description, the error correction encoding device 100b has been described as including the interleaving unit 150, the LSB interleaving unit 126, and the LSB deinterleaving unit 127, but it is not limited thereto.

[0801] For example, the error correction encoding device 100b may be one including the interleaving unit 150 and neither the LSB interleaving unit 126 nor the LSB deinterleaving unit 127.

[0802] In addition, the error correction encoding device 100b may be one including the LSB interleaving unit 126 and the LSB deinterleaving unit 127 and not including the interleaving unit 150.

[0803] In addition, in the above description, the error correction device 200b has been described as including the deinterleaving unit 250, the reception LSB interleaving unit 248, and the reception LSB deinterleaving unit 249, but it is not limited thereto.

[0804] For example, in a case where the error correction encoding device 100b includes the interleaving unit 150 and includes neither the LSB interleaving unit 126 nor the LSB deinterleaving unit 127, the error correction encoding device 100b is one including the deinterleaving unit 250 and neither the reception LSB interleaving unit 248 nor the reception LSB deinterleaving unit 249.

[0805] In addition, in a case where the error correction encoding device 100b includes the LSB interleaving unit 126 and the LSB deinterleaving unit 127 and does not include the interleaving unit 150, the error correction encoding device 100b is one including the reception LSB interleaving unit 248 and the reception LSB deinterleaving unit 249 and not including the deinterleaving unit 250.

[0806] Note that, in the present disclosure, within the scope of the invention, free combination of embodiments, a modification of any component of each embodiment, or omission of any component in each embodiment is possible.

INDUSTRIAL APPLICABILITY

[0807] The present disclosure is suitable for a communication system in which, when information is transmitted from a transmission device to a reception device, the transmission device performs error correction encoding on the information to be transmitted, and the reception device performs error correction on the information received.

REFERENCE SIGNS LIST

[0808] 1, 1a, 1b, 1c, 1d: communication system, 30: transmission path, 10, 10a, 10b, 10c, 10d: transmission device, 11: D/A converter, 12: transmission light source, 13: optical modulator, 100, 100a, 100b, 100c, 100d: error correction encoding device, 110: input information acquiring unit, 120, 120a, 120b, 120c, 120d: encoding unit, 121, 121c, 121d: input bit array information generating unit, 122: probability distribution shaping encoding unit, 123: bit inversion unit, 124, 124c: soft decision error correction encoding unit, 125, 125d: hard decision error correction encoding unit, 126: LSB interleaving unit, 127: LSB deinterleaving unit, 130: modulation symbol conversion unit, 131: first symbol mapping unit, 132: second symbol mapping unit, 140: transmission waveform shaping unit, 141: polarization multiplexing unit, 142: transmission digital signal generating unit, 150: interleaving unit, 20, 20a, 20b, 20c, 20d: reception device, 21: optical receiver, 22: reception light source, 23: A/D converter, 200, 200a, 200b, 200c, 200d: error correction device, 210: reception modulation symbol group information generating unit, 211: reception polarization multiplexing symbol generating unit, 212: reception modulation symbol generating unit, 220: hard decision candidate generating unit, 221: first hard decision candidate generating unit, 222: second hard decision candidate generating unit, 223: third hard decision candidate generating unit, 230: soft decision information generating unit, 231: first soft decision information generating unit, 232: second soft decision information generating unit, 233: third soft decision information generating unit, 240, 240a, 240b, 240c, 240d: decoding unit, 241, 241c: soft decision error correction decoding unit, 242: selection unit, 2421: first selection unit, 2422: second selection unit, 2423: third selection unit, 243: reception side bit inversion unit, 244: probability distribution shaping decoding unit, 245, 245d: second output bit array generating unit, 246, 246c: output information generating unit, 247, 247d: hard decision error correction decoding unit, 248: reception LSB interleaving unit, 249: reception LSB deinterleaving unit, 250: deinterleaving unit, 260: third output bit array generating unit, 290: information output unit, 501, 901: processor, 502, 902: memory, 503, 903: processing circuit.

Claims

1. An error correction encoding device comprising:

an input information acquiring unit to acquire input information;

an encoding unit to generate soft decision error correction frame information including a bit array of m rows and N columns on a basis of the input information acquired by the input information acquiring unit, the bit array being obtained by combining first bit string group information and second bit string group information, the first bit string group information including a bit array of m rows and N1 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol by using a predetermined first symbol mapping

rule, the second bit string group information including a bit array of m rows and N2 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol by using a predetermined second symbol mapping rule, where m is a natural number of greater than or equal to 2, N1 is a natural number of greater than or equal to 2, N2 is a natural number of greater than or equal to 1, and N is a number obtained by adding N1 and N2 together;

a modulation symbol conversion unit to generate modulation symbol group information including N pieces of the modulation symbols by performing pulse amplitude modulation of a combination of bit values of each column of the soft decision error correction frame information generated by the encoding unit into the modulation symbol for each column of the soft decision error correction frame information by using the first symbol mapping rule or the second symbol mapping rule; and

a transmission waveform shaping unit to generate a digital baseband modulation signal on a basis of the modulation symbol group information generated by the modulation symbol conversion unit and output the digital baseband modulation signal generated,

wherein

the encoding unit

generates the soft decision error correction frame information by:

generating first input bit array information including a bit array of m - 1 rows and N columns and second input bit array information including a bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit, where N3 is a natural number of greater than or equal to 1 and less than N1;

storing the second input bit array information generated as a part of first MSB information including a bit array of one row and N1 columns in a predetermined area of a first row in the first bit string group information;

generating shaped bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping encoding processing on the first input bit array information generated;

generating first group bit array information including a combination of N1 predetermined columns and second group bit array information including a combination of N2 predetermined columns by separating the shaped bit array information generated;

generating first LSB information including a bit array of one row and N1 columns by extracting, from the first group bit array information generated, a bit array of an (m - 1)-th row in the first group bit array information, generating inverted first LSB information including a bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in information of the first row in the first bit string group information after storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in an m-th row in the first bit string group information;

generating second LSB information including a bit array of one row and N2 columns by extracting a bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated, and storing the second LSB information generated in the m-th row in the second bit string group information;

generating a soft decision parity bit by performing systematic soft decision error correction encoding processing by using the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in the first row in the second bit string group information as second MSB information including a bit array of one row and N2 columns;

in a case where m is greater than or equal to 3, generating first SSB information including a bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated, the first row to an (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in a second row to the (m - 1)-th row in the first bit string group information; and

in the case where m is greater than or equal to 3, generating second SSB information including a bit array of m - 2 rows and N2 columns by extracting, from the second group bit array information generated, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the

second row to the (m - 1)-th row in the second bit string group information.

2. The error correction encoding device according to claim 1, wherein

the first symbol mapping rule is a symbol mapping rule in which one combination of bit values including a bit array of m rows and one column corresponds to one of the modulation symbols subjected to one-dimensional pulse amplitude modulation, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols are adjacent to each other, and
the second symbol mapping rule is a symbol mapping rule in which one combination of bit values including a bit array of m rows and one column corresponds to one of the modulation symbols subjected to one-dimensional pulse amplitude modulation, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols have an identical sign and are adjacent to each other, and are identical values between the modulation symbol of which an absolute value of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are positive and the modulation symbol of which an absolute value of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are negative.

3. The error correction encoding device according to claim 1, wherein
the encoding unit generates the first input bit array information and the second input bit array information by setting a bit value of a bit other than a bit corresponding to the input information to 0 in the first input bit array information or the second input bit array information when generating the first input bit array information and the second input bit array information on the basis of the input information acquired by the input information acquiring unit.

4. The error correction encoding device according to claim 1, wherein

the encoding unit generates a hard decision parity bit by performing systematic hard decision error correction encoding processing, by using the first input bit array information and the second input bit array information, or by using the first input bit array information, the first SSB information, the second SSB information, the second LSB information, and the first LSB information or the inverted first LSB information, and
stores the hard decision parity bit generated, as a part of the first MSB information in a predetermined area different from an area storing the second input bit array information of the first row in the first bit string group information.

5. The error correction encoding device according to claim 4, wherein

the encoding unit generates the second input bit array information by setting a bit value of a bit other than a bit corresponding to the input information to a predetermined value in the second input bit array information when generating the second input bit array information on the basis of the input information acquired by the input information acquiring unit, and
the encoding unit, when performing the systematic hard decision error correction encoding processing,
as first preprocessing, switches bit values of columns corresponding to each other between a bit value of an area storing the predetermined value, of a predetermined area of the first row in the first bit string group information storing the second input bit array information as a part of the first MSB information, and a bit value of a column corresponding to one of the columns of an area storing the predetermined value of a predetermined area of the first row in the first bit string group information, of an area of the m-th row in the first bit string group information storing the first LSB information, and
as second preprocessing, calculates an exclusive OR for each of the columns corresponding to each other between a bit value after switching the bit value of the area storing the predetermined value, of the predetermined area of the first row in the first bit string group information, and a bit value after switching the bit value of the column corresponding to one of the columns of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, of the area of the m-th row in the first bit string group information, and
as third preprocessing, overwrites the bit value

after switching the bit value of the area storing the predetermined value, of the predetermined area of the first row in the first bit string group information, by using a calculation result of the exclusive OR in the columns corresponding to each other.

6. The error correction encoding device according to claim 1, wherein
the encoding unit generates the soft decision error correction frame information by:

generating third input bit array information including a bit array of one row and N4 columns in addition to the first input bit array information and the second input bit array information on the basis of the input information acquired by the input information acquiring unit, where N4 is a natural number of greater than or equal to 1 and less than N2;
storing the third input bit array information generated as a part of the second MSB information including the bit array of one row and N2 columns in a predetermined area of the first row in the second bit string group information; and
generating the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the third input bit array information stored as the part of the second MSB information in addition to the inverted first LSB information generated and the second LSB information generated, and storing the soft decision parity bit generated, in a predetermined area different from an area storing the second bit string group information of the first row of the second bit string group information.

7. An error correction encoding method comprising:

an input information acquiring step of acquiring, by an input information acquiring unit, input information; and
an encoding step of generating, by an encoding unit, soft decision error correction frame information including a bit array of m rows and N columns on a basis of the input information acquired by the input information acquiring unit, the bit array being obtained by combining first bit string group information and second bit string group information, the first bit string group information including a bit array of m rows and N1 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol by using a predetermined first symbol mapping rule, the second bit string group information including a bit array of m rows and N2 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol by using a predetermined second symbol mapping rule, where m is a natural number of greater than or equal to 2, N1 is a natural number of greater than or equal to 2, N2 is a natural number of greater than or equal to 1, and N is a number obtained by adding N1 and N2 together,
wherein
the encoding step
includes:

a first encoding step of generating first input bit array information including a bit array of m - 1 rows and N columns and second input bit array information including a bit array of one row and N3 columns on the basis of the input information acquired by the input information acquiring unit, where N3 is a natural number of greater than or equal to 1 and less than N1;
a second encoding step of storing the second input bit array information generated by the first encoding step as a part of first MSB information including a bit array of one row and N1 columns in a predetermined area of a first row in the first bit string group information;
a third encoding step of generating shaped bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping encoding processing on the first input bit array information generated by the first encoding step;
a fourth encoding step of generating first group bit array information including a combination of N1 predetermined columns and second group bit array information including a combination of N2 predetermined columns by separating the shaped bit array information generated by the third encoding step;
a fifth encoding step of generating first LSB information including a bit array of one row and N1 columns by extracting, from the first group bit array information generated by the fourth encoding step, a bit array of an (m - 1)-th row in the first group bit array information, generating inverted first LSB information including a bit array of one row and N1 columns by calculating exclusive ORs of bit values of each columns in the first LSB information generated and each bit values of each columns in information of the first row in the first bit string group information after

storing the second input bit array information, the columns in the information of the first row in the first bit string group information each corresponding to the columns in the first LSB information, and storing the inverted first LSB information generated in an m-th row in the first bit string group information;

a sixth encoding step of generating second LSB information including a bit array of one row and N2 columns by extracting a bit array of the (m - 1)-th row in the second group bit array information from the second group bit array information generated by the fourth encoding step, and storing the second LSB information generated in the m-th row in the second bit string group information;

a seventh encoding step of generating a soft decision parity bit by performing systematic soft decision error correction encoding processing by using the inverted first LSB information generated by the fifth encoding step and the second LSB information generated by the sixth encoding step, and storing the soft decision parity bit generated, in the first row in the second bit string group information as second MSB information including a bit array of one row and N2 columns;

an eighth encoding step of generating first SSB information including a bit array of m - 2 rows and N1 columns by extracting, from the first group bit array information generated by the fourth encoding step, the first row to an (m - 2)-th row in the first group bit array information, and storing the first SSB information generated, in a second row to the (m - 1)-th row in the first bit string group information, in a case where m is greater than or equal to 3; and

a ninth encoding step of generating second SSB information including a bit array of m - 2 rows and N2 columns by extracting, from the second group bit array information generated by the fourth encoding step, the first row to the (m - 2)-th row in the second group bit array information, and storing the second SSB information generated, in the second row to the (m - 1)-th row in the second bit string group information, in the case where m is greater than or equal to 3.

8. An error correction device comprising:

a reception modulation symbol group information generating unit to receive a reception digital baseband modulation signal that is a signal based on the soft decision error correction frame information generated by the error correction encoding method according to claim 7 and generate reception modulation symbol group information including N reception modulation symbols on a basis of the reception digital baseband modulation signal;

a hard decision candidate generating unit to generate first hard decision candidate bit array information including a bit array of one row and N1 columns, second hard decision candidate bit array information including a bit array of m - 2 rows and N1 columns in a case where m is greater than or equal to 3, and third hard decision candidate bit array information including a bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the reception modulation symbol group information generated by the reception modulation symbol group information generating unit on a basis of the first symbol mapping rule or the second symbol mapping rule;

a soft decision information generating unit to generate a first posterior L value sequence including N2 posterior L values corresponding to each columns of a first row of the second bit string group information, a second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and a third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on a basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit;

a decoding unit to perform multi-stage error correction processing on a basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit; and

an information output unit to output information generated by the decoding unit performing the multi-stage error correction processing as output information,

wherein

in first decoding processing in the multi-stage error correction processing, the decoding unit generates inverted first reception LSB information including a bit array of one row and N1 columns corresponding to the inverted first LSB information and second reception LSB informa-

tion including a bit array of one row and N2 columns corresponding to the second LSB information by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence,

in second decoding processing in the multi-stage error correction processing, the decoding unit generates first reception MSB information including a bit array of one row and N1 columns corresponding to the first MSB information on a basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generates first reception SSB information including a bit array of m - 2 rows and N1 columns corresponding to the first SSB information on a basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generates second reception SSB information including a bit array of m - 2 rows and N2 columns corresponding to the second SSB information on a basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3,

in third decoding processing in the multi-stage error correction processing, the decoding unit generates first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information,

in fourth decoding processing in the multi-stage error correction processing, the decoding unit generates first output bit array information including a bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information,

in fifth decoding processing in the multi-stage error correction processing, the decoding unit generates second output bit array information including a bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of a predetermined area of the first reception MSB information,

in sixth decoding processing in the multi-stage error correction processing, the decoding unit generates the output information corresponding to the input information on a basis of the first output bit array information and the second output bit array information, and

the information output unit outputs the output information generated by the decoding unit.

9. The error correction device according to claim 8, wherein

the first symbol mapping rule is a symbol mapping rule in which one of the modulation symbols subjected to one-dimensional pulse amplitude modulation corresponds to one combination of bit values including a bit array of m rows and one column, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols are adjacent to each other, and

the second symbol mapping rule is a symbol mapping rule in which one of the modulation symbols subjected to one-dimensional pulse amplitude modulation corresponds to one combination of bit values including a bit array of m rows and one column, and is the symbol mapping rule in which a combination of the bit values from the first row to the (m - 1)-th row of the bit array of m rows and one column is a combination corresponding to a binary reflected Gray code, and bit values of the m-th row are values different from each other in the modulation symbols in which amplitude values of the modulation symbols have an identical sign and are adjacent to each other, and are identical values between the modulation symbol of which an absolute vale of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are positive and the modulation symbol of which an absolute value of an amplitude value of the modulation symbol is minimum among the modulation symbols in which the amplitude values of the modulation symbols are negative.

10. The error correction device according to claim 8, wherein

the decoding unit performs hard decision error correction processing on information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second recep-

tion LSB information, and the first reception LSB information or the inverted first reception LSB information, or on the information corresponding to the second output bit array information of the first reception MSB information and the first output bit array information, on a basis of information stored in a predetermined area of the first reception MSB information, in seventh decoding processing in the multi-stage error correction processing, and

in a case where the decoding unit performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the inverted first reception LSB information, the decoding unit generates the second output bit array information by calculating an exclusive OR by using the inverted first reception LSB information and the first reception MSB information after the seventh decoding processing, in the third decoding processing, and extracting information of a predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing, and

in a case where the decoding unit performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first reception SSB information, the second reception SSB information, the second reception LSB information, and the first reception LSB information, the decoding unit generates the second output bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information after the seventh decoding processing, in the fourth decoding processing, and extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing, and

in a case where the decoding unit performs the hard decision error correction processing on the information corresponding to the second output bit array information of the first reception MSB information, and the first output bit array information, the decoding unit generates the second output bit array information by extracting the information of the predetermined area of the first reception MSB information after the seventh decoding processing, in the fifth decoding processing, and generates the output information on a basis of the second output bit array information and the first output bit array information after the seventh decoding processing, in the sixth decoding processing.

11. The error correction device according to claim 10, wherein

the decoding unit performs the hard decision error correction processing, and then, in the seventh decoding processing in the multi-stage error correction processing,

as first post-processing, calculates an exclusive OR for each of columns corresponding to each other between a bit value of a column in the first reception MSB information corresponding to each column of an area storing a predetermined value of a predetermined area of the first row in the first bit string group information storing the second input bit array information as a part of the first MSB information, and a bit value of a column in the first reception LSB information corresponding to each column of the area storing the predetermined value in the predetermined area in the first row in the first bit string group information storing the second input bit array information as the part of the first MSB information, and

as second post-processing, overwrites the bit value of the column in the first reception MSB information corresponding to each column of the area storing the predetermined value of the predetermined area of the first row in the first bit string group information, by using a calculation result of the exclusive OR in the columns corresponding to each other.

12. The error correction device according to claim 8, wherein

the first encoding step generates third input bit array information including a bit array of one row and N4 columns in addition to the first input bit array information and the second input bit array information on the basis of the input information acquired by the input information acquiring unit, where N4 is a natural number of greater than or equal to 1 and less than N2,

the second encoding step stores the second input bit array information generated by the first encoding step as a part of the first MSB information in a predetermined area of the first row in the first bit string group information, and stores the third input bit array information generated by the first encoding step as a part of the second MSB information in a predetermined area of the first row in the second bit string group informa-

tion,
the seventh encoding step generates the soft decision parity bit by performing the systematic soft decision error correction encoding processing by using the third input bit array information generated by the first encoding step in addition to the inverted first LSB information generated by the fifth encoding step and the second LSB information generated by the sixth encoding step, and stores the soft decision parity bit generated, in an area different from the area in which the third input bit array information is stored of the second MSB information, and
the decoding unit generates second reception MSB information including a bit array of one row and N2 columns corresponding to the second MSB information, in addition to the inverted first reception LSB information including the bit array of one row and N1 columns corresponding to the inverted first LSB information and the second reception LSB information including the bit array of one row and N2 columns corresponding to the second LSB information, by performing soft decision error correction processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence, in the first decoding processing in the multi-stage error correction processing,
generates third output bit array information including a bit array of one row and N4 columns corresponding to the third input bit array information by extracting information of a predetermined area of the second reception MSB information in eighth decoding processing in the multi-stage error correction processing, and
generates the output information corresponding to the input information on a basis of the third output bit array information, in addition to the first output bit array information and the second output bit array information, in the sixth decoding processing in the multi-stage error correction processing.

13. An error correction method comprising:

a reception modulation symbol group information generating step of receiving a reception digital baseband modulation signal that is a signal based on the soft decision error correction frame information generated by the error correction encoding method according to claim 7 and generating reception modulation symbol group information including N reception modulation symbols on a basis of the reception digital baseband modulation signal, by a reception modulation symbol group information generating unit;
a hard decision candidate generating step of generating, by a hard decision candidate generating unit, first hard decision candidate bit array information including a bit array of one row and N1 columns, second hard decision candidate bit array information including a bit array of m - 2 rows and N1 columns in a case where m is greater than or equal to 3, and third hard decision candidate bit array information including a bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the first symbol mapping rule or the second symbol mapping rule, on a basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit;
a soft decision information generating step of generating, by a soft decision information generating unit, a first posterior L value sequence including N2 posterior L values corresponding to each columns of a first row of the second bit string group information, a second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and a third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on a basis of the reception modulation symbol group information generated by the reception modulation symbol group information generating unit;
a decoding step of performing, by a decoding unit, multi-stage error correction processing on a basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, and the third hard decision candidate bit array information generated by the hard decision candidate generating unit, and the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated by the soft decision information generating unit; and
an information output step of outputting, by an information output unit, information generated by the decoding unit performing the multi-stage error correction processing as output information,
wherein
in first decoding processing in the multi-stage error correction processing, the decoding unit generates inverted first reception LSB information including a bit array of one row and N1 columns corresponding to the inverted first LSB information and second reception LSB information including a bit array of one row and N2 columns corresponding to the second LSB information by performing soft decision error correc-

tion processing on the basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence,
in second decoding processing in the multi-stage error correction processing, the decoding unit generates first reception MSB information including a bit array of one row and N1 columns corresponding to the first MSB information on a basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generates first reception SSB information including a bit array of m - 2 rows and N1 columns corresponding to the first SSB information on a basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generates second reception SSB information including a bit array of m - 2 rows and N2 columns corresponding to the second SSB information on a basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3,
in third decoding processing in the multi-stage error correction processing, the decoding unit generates first reception LSB information corresponding to the first LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information,
in fourth decoding processing in the multi-stage error correction processing, the decoding unit generates first output bit array information including a bit array of m - 1 rows and N columns corresponding to the first input bit array information by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information,
in fifth decoding processing in the multi-stage error correction processing, the decoding unit generates second output bit array information including a bit array of one row and N3 columns corresponding to the second input bit array information by extracting information of a predetermined area of the first reception MSB information,
in sixth decoding processing in the multi-stage error correction processing, the decoding unit generates the output information corresponding to the input information on a basis of the first output bit array information and the second output bit array information, and
the information output unit outputs the output information generated by the decoding unit.

14. A communication method comprising:

an error correction encoding step of generating the soft decision error correction frame information based on the input information by the error correction encoding method according to claim 7;
a modulation symbol conversion step of generating, by a modulation symbol conversion unit, modulation symbol group information including N pieces of the modulation symbols by performing pulse amplitude modulation on a combination of bit values of each column of the soft decision error correction frame information generated by the error correction encoding step into the modulation symbol for each column of the soft decision error correction frame information on a basis of the first symbol mapping rule or the second symbol mapping rule;
a transmission waveform shaping step, by a transmission waveform shaping unit, of generating a digital baseband modulation signal on a basis of the modulation symbol group information generated by the modulation symbol conversion unit, and outputting the digital baseband modulation signal generated;
a transmission step, by a transmission unit, of receiving the digital baseband modulation signal output by the transmission waveform shaping unit and transmitting a signal based on the digital baseband modulation signal;
a reception step, by a reception unit, of receiving the signal transmitted by the transmission unit and generating a reception digital baseband modulation signal from the signal; and
an error correction step of generating and outputting output information corresponding to the input information by the error correction method according to claim 13 on a basis of the reception digital baseband modulation signal generated by the reception unit.

15. An optical communication system comprising: an optical transmission path to transmit an optical signal; a transmission device; and a reception device, wherein

the transmission device includes:

the error correction encoding device according to claim 1;
a D/A converter to receive the digital base-

band modulation signal output by the error correction encoding device, convert the digital baseband modulation signal into a transmission electrical signal that is an analog baseband modulation signal, and output the transmission electrical signal after conversion;
a transmission light source to output unmodulated light having a single wavelength; and
an optical modulator to receive the transmission electrical signal output by the D/A converter and the unmodulated light output by the transmission light source, modulate the unmodulated light with the transmission electrical signal to generate modulated light, and output the modulated light generated as a modulated optical signal to the optical transmission path, and
the reception device
includes:

a reception light source to output unmodulated light having a single wavelength corresponding to a center wavelength of the modulated light that is a modulated optical signal output to the optical transmission path by the transmission device;
an optical receiver to receive the modulated optical signal output to the optical transmission path by the transmission device and the unmodulated light output by the reception light source, generate a reception electrical signal that is a reception analog baseband modulation signal by performing coherent detection using the modulated light that is the modulated optical signal and the unmodulated light, and output the reception electrical signal generated;
an A/D converter to receive the reception electrical signal output by the optical receiver, convert the reception electrical signal into a reception digital baseband modulation signal, and output the reception digital baseband modulation signal after conversion; and
the error correction device according to claim 8.

16. A soft decision error correction frame data structure used in a communication system in which a transmission device transmits a signal based on input information input to the transmission device to a reception device, and the reception device receives the signal transmitted by the transmission device and generates output information corresponding to the input information on a basis of the signal,

the soft decision error correction frame data structure comprising
a bit array of m rows and N columns obtained by combining first bit string group information and second bit string group information, the first bit string group information including a bit array of m rows and N1 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the first bit string group information into a modulation symbol on a basis of a predetermined first symbol mapping rule, the second bit string group information including a bit array of m rows and N2 columns in which it is enabled to perform pulse amplitude modulation of a combination of bit values of each column of the second bit string group information into a modulation symbol on a basis of a predetermined second symbol mapping rule, where m is a natural number of greater than or equal to 2, N1 is a natural number of greater than or equal to 2, N2 is a natural number of greater than or equal to 1, and N is a number obtained by adding N1 and N2 together, wherein a soft decision parity bit is stored in a first row in the second bit string group information, the soft decision parity bit being generated by performing systematic soft decision error correction encoding processing using a bit value of each column of an m-th row in the first bit string group information and a bit value of each column of the m-th row in the second bit string group information.

17. A soft decision error correction frame data structure to enable

generation of reception modulation symbol group information including N reception modulation symbols on a basis of a reception digital baseband modulation signal generated from a signal based on soft decision error correction frame information having the soft decision error correction frame data structure according to claim 16,
generation of first hard decision candidate bit array information including a bit array of one row and N1 columns, second hard decision candidate bit array information including a bit array of m - 2 rows and N1 columns in a case where m is greater than or equal to 3, and third hard decision candidate bit array information including a bit array of m - 2 rows and N2 columns in the case where m is greater than or equal to 3, by using the first symbol mapping rule or the second symbol mapping rule on a basis of the reception modulation symbol group information

generated,
generation of a first posterior L value sequence including N2 posterior L values corresponding to each columns of the first row of the second bit string group information, a second posterior L value sequence including N1 posterior L values corresponding to each columns of the m-th row of the first bit string group information, and a third posterior L value sequence including N2 posterior L values corresponding to each columns of the m-th row of the second bit string group information on the basis of the reception modulation symbol group information generated, and
error correction by performing multi-stage error correction processing on a basis of the first hard decision candidate bit array information, the second hard decision candidate bit array information, the third hard decision candidate bit array information, the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence generated.

18. The soft decision error correction frame data structure according to claim 17, wherein it is enabled to

generate inverted first reception LSB information including a bit array of one row and N1 columns and second reception LSB information including a bit array of one row and N2 columns by performing soft decision error correction processing on a basis of the first posterior L value sequence, the second posterior L value sequence, and the third posterior L value sequence, in first decoding processing in the multi-stage error correction processing,
generate first reception MSB information including a bit array of one row and N1 columns on a basis of the first hard decision candidate bit array information and the inverted first reception LSB information, generate first reception SSB information including a bit array of m - 2 rows and N1 columns on a basis of the second hard decision candidate bit array information and the inverted first reception LSB information in the case where m is greater than or equal to 3, and generate second reception SSB information including a bit array of m - 2 rows and N2 columns on a basis of the third hard decision candidate bit array information and the second reception LSB information in the case where m is greater than or equal to 3, in second decoding processing in the multi-stage error correction processing,
generate first reception LSB information by calculating exclusive ORs of bit values of each columns in the inverted first reception LSB information and each bit values of each columns in the first reception MSB information each corresponding to the columns in the inverted first reception LSB information, in third decoding processing in the multi-stage error correction processing,
generate first output bit array information including a bit array of m - 1 rows and N columns by performing probability distribution shaping decoding processing on the first reception SSB information, the second reception SSB information, the first reception LSB information, and the second reception LSB information, in fourth decoding processing in the multi-stage error correction processing,
generate second output bit array information including a bit array of one row and N3 columns by extracting information of a predetermined area of the first reception MSB information, in fifth decoding processing in the multi-stage error correction processing, and
generate the output information corresponding to the input information on a basis of the first output bit array information and the second output bit array information, in sixth decoding processing in the multi-stage error correction processing.

FIG. 1

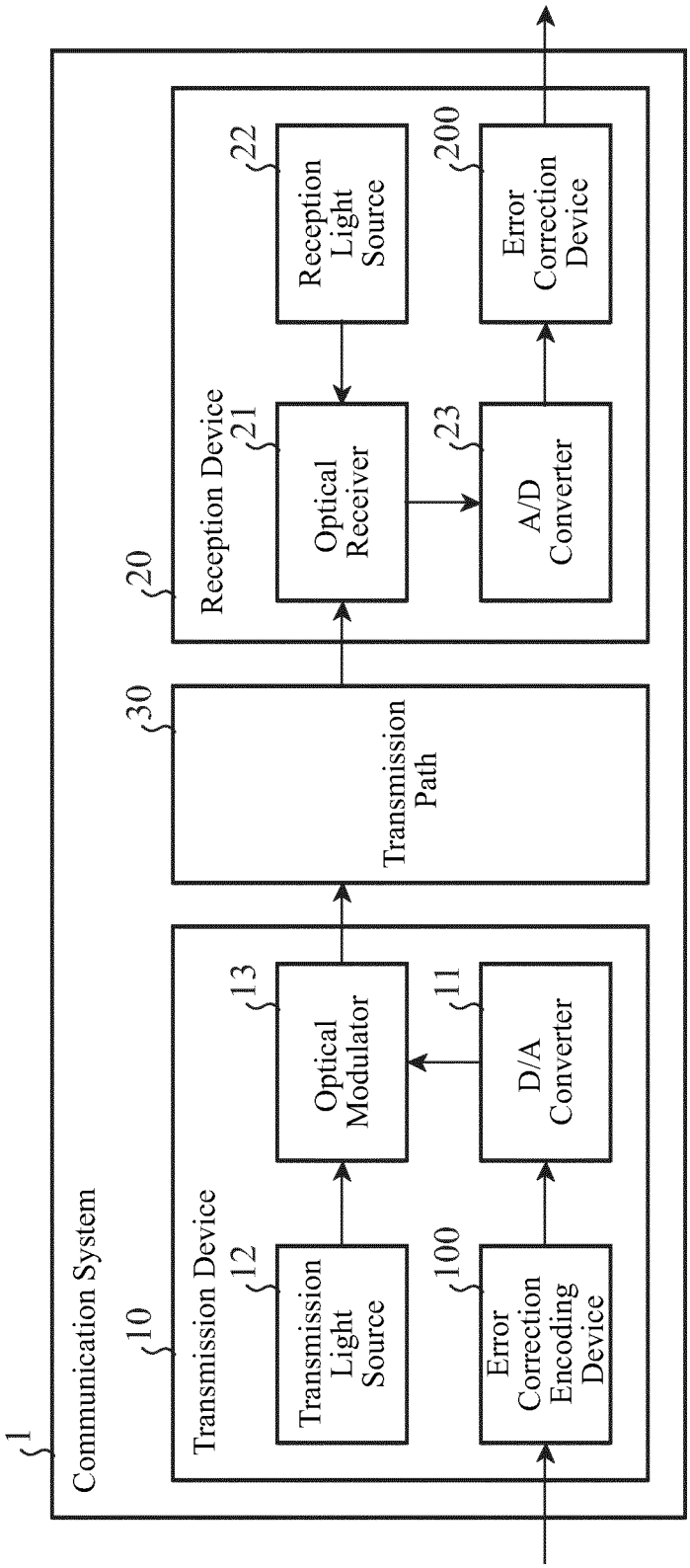

1
Communication System
10
Transmission Device
12
Transmission Light Source
100
Error Correction Encoding Device
13
Optical Modulator
11
D/A Converter
30
Transmission Path
20
Reception Device
21
Optical Receiver
23
A/D Converter
22
Reception Light Source
200
Error Correction Device

FIG. 2

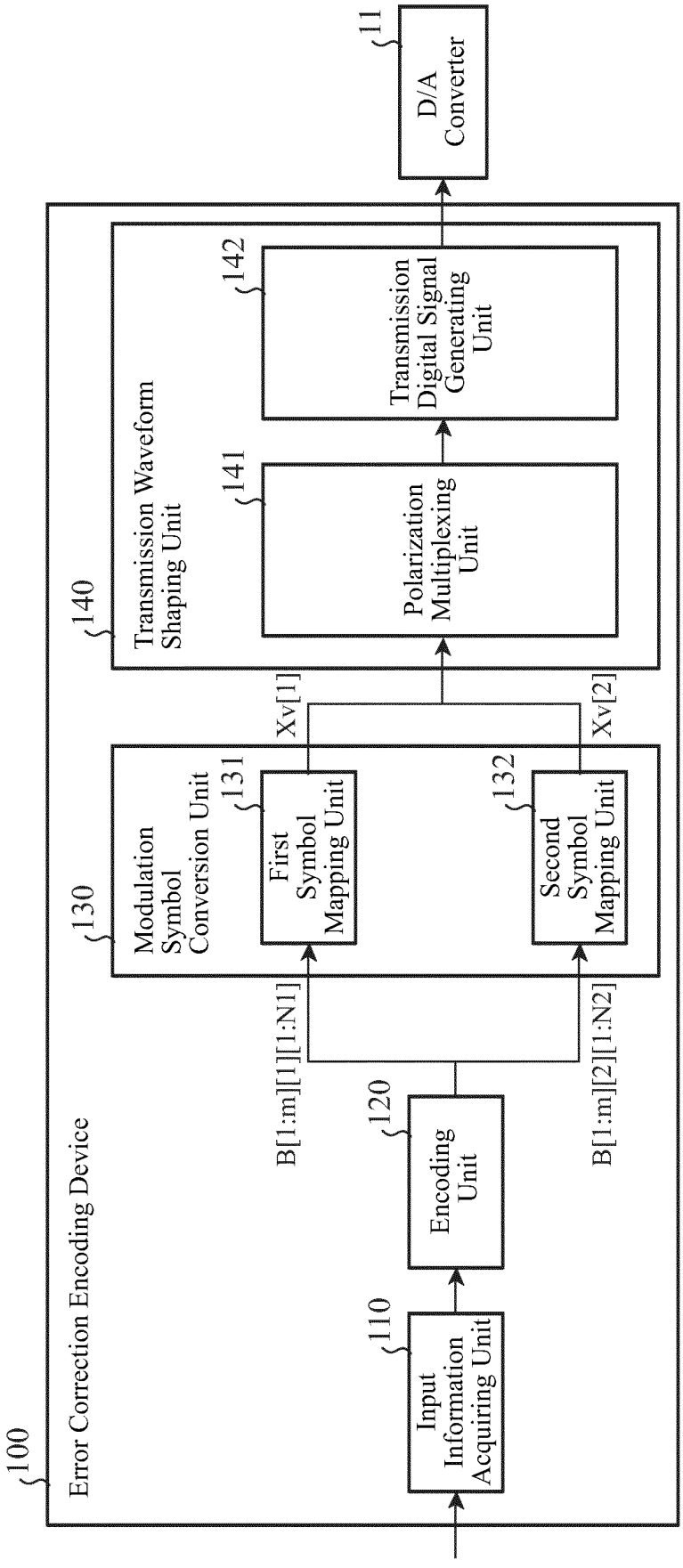

100
Error Correction Encoding Device
110
Input Information Acquiring Unit
120
Encoding Unit
B[1:m][1][1:N1]
B[1:m][2][1:N2]
130
Modulation Symbol Conversion Unit
131
First Symbol Mapping Unit
132
Second Symbol Mapping Unit
Xv[1]
Xv[2]
140
Transmission Waveform Shaping Unit
141
Polarization Multiplexing Unit
142
Transmission Digital Signal Generating Unit
11
D/A Converter

FIG. 3

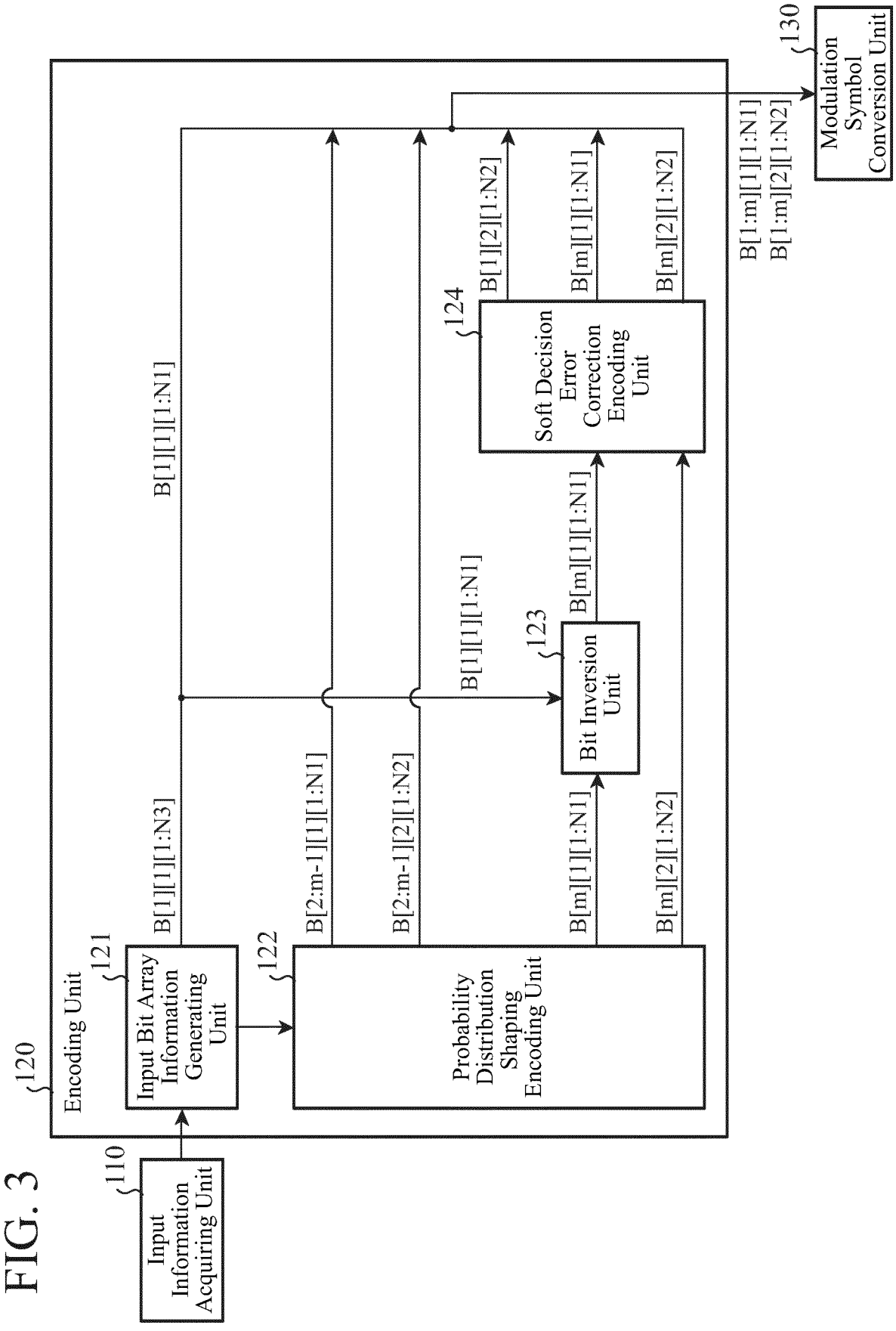

Input Information Acquiring Unit
110
Encoding Unit
120
Input Bit Array Information Generating Unit
121
Probability Distribution Shaping Encoding Unit
122
Bit Inversion Unit
123
Soft Decision Error Correction Encoding Unit
124
Modulation Symbol Conversion Unit
130
B[1][1][1:N3]
B[1][1][1:N1]
B[2:m-1][1][1:N1]
B[2:m-1][2][1:N2]
B[1][1][1:N1]
B[m][1][1:N1]
B[m][2][1:N2]
B[m][1][1:N1]
B[m][2][1:N2]
B[1][2][1:N2]
B[m][1][1:N1]
B[m][2][1:N2]
B[1:m][1][1:N1]
B[1:m][2][1:N2]

FIG. 4A

First Symbol Mapping Rule

PAM Symbol X[1][k]	Combination of Bits B[1:m][1][k]
15	0101
13	0100
11	0111
9	0110
7	0011
5	0010
3	0001
1	0000
-1	1001
-3	1000
-5	1011
-7	1010
-9	1111
-11	1110
-13	1101
-15	1100

FIG. 4B

Second Symbol Mapping Rule

PAM Symbol X[2][k]	Combination of Bits B[1:m][2][k]
15	0101
13	0100
11	0111
9	0110
7	0011
5	0010
3	0001
1	0000
-1	1000
-3	1001
-5	1010
-7	1011
-9	1110
-11	1111
-13	1100
-15	1101

FIG. 5A

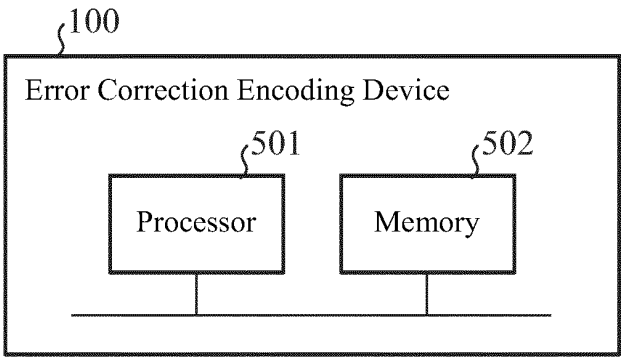


FIG. 5B

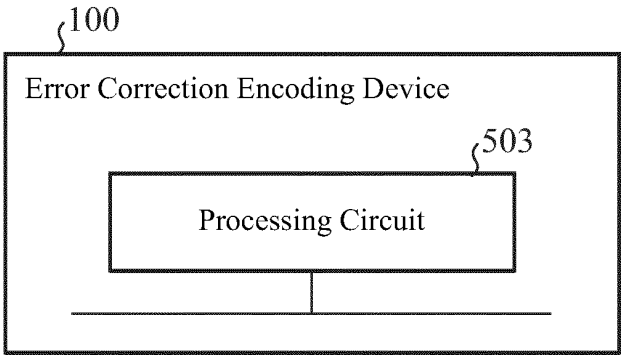


FIG. 6A

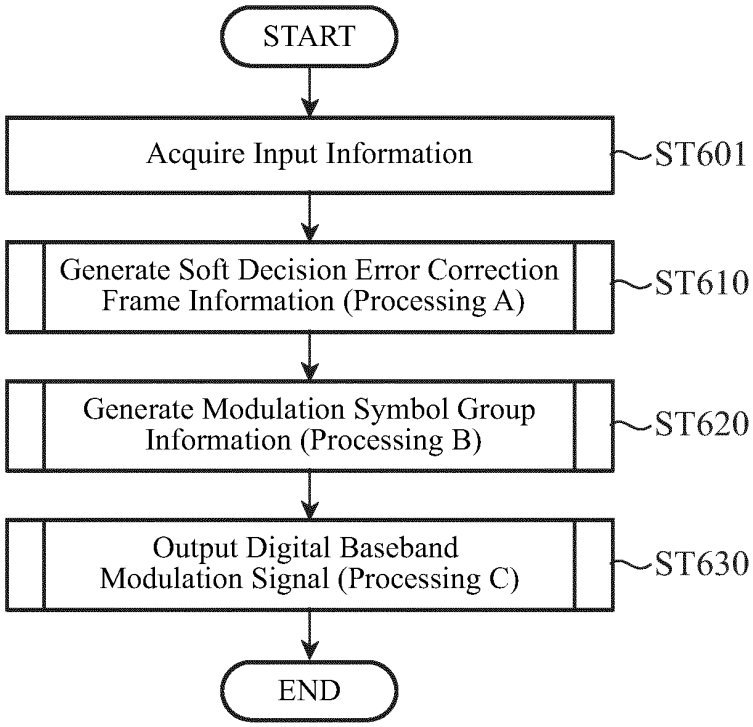


FIG. 6B

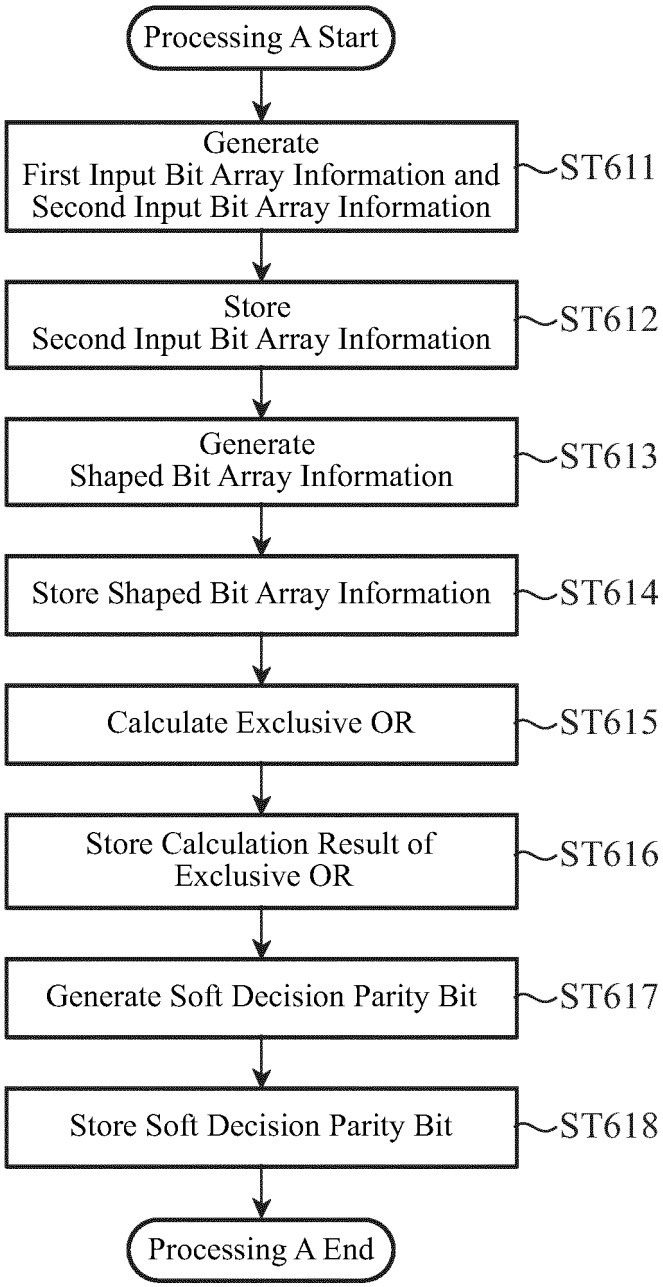
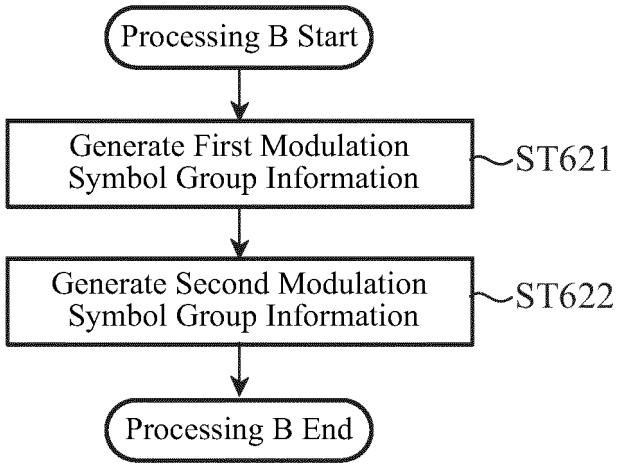

Processing A Start
Generate First Input Bit Array Information and Second Input Bit Array Information
ST611
Store Second Input Bit Array Information
ST612
Generate Shaped Bit Array Information
ST613
Store Shaped Bit Array Information
ST614
Calculate Exclusive OR
ST615
Store Calculation Result of Exclusive OR
ST616
Generate Soft Decision Parity Bit
ST617
Store Soft Decision Parity Bit
ST618
Processing A End

FIG. 6C


Processing B Start
Generate First Modulation Symbol Group Information
ST621
Generate Second Modulation Symbol Group Information
ST622
Processing B End

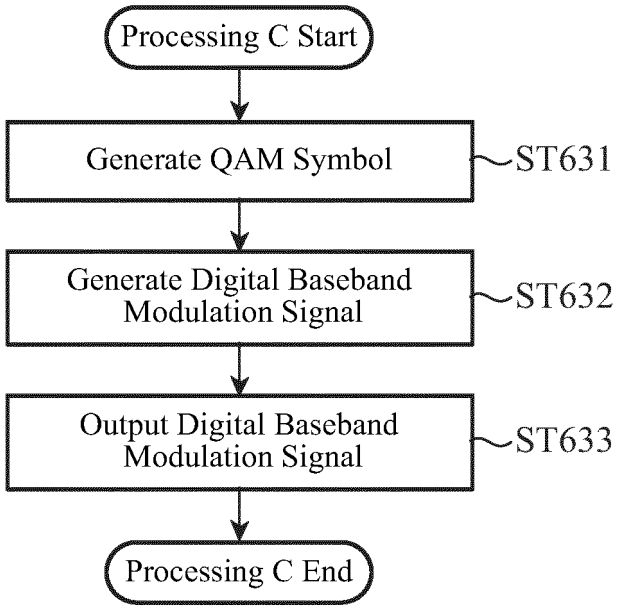

Processing C Start
Generate QAM Symbol
ST631
Generate Digital Baseband Modulation Signal
ST632
Output Digital Baseband Modulation Signal
ST633
Processing C End

FIG. 7

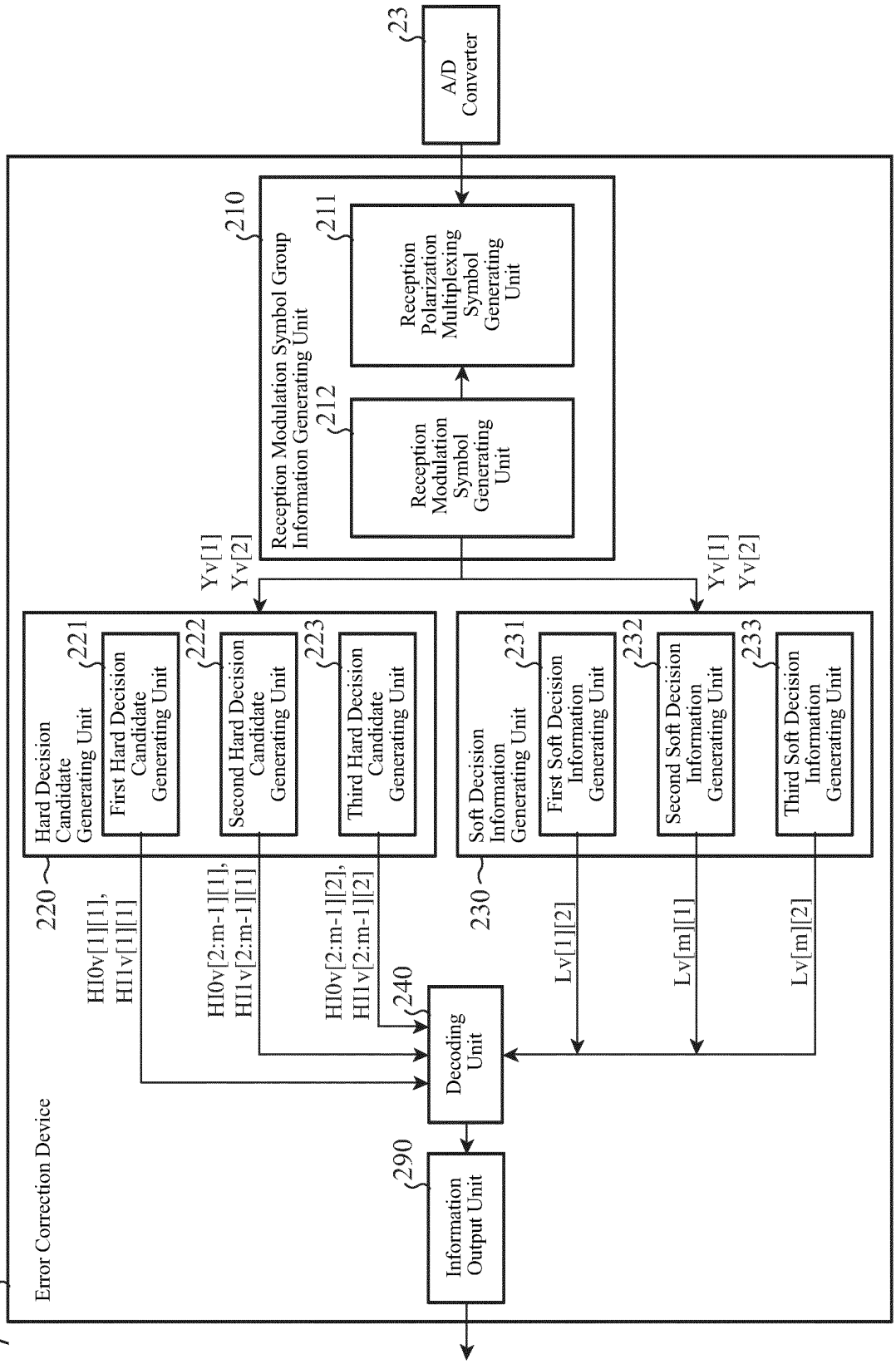

200
Error Correction Device
23
A/D Converter
210
Reception Modulation Symbol Group Information Generating Unit
211
Reception Polarization Multiplexing Symbol Generating Unit
212
Reception Modulation Symbol Generating Unit
Yv[1]
Yv[2]
Yv[1]
Yv[2]
220
Hard Decision Candidate Generating Unit
221
First Hard Decision Candidate Generating Unit
222
Second Hard Decision Candidate Generating Unit
223
Third Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
231
First Soft Decision Information Generating Unit
232
Second Soft Decision Information Generating Unit
233
Third Soft Decision Information Generating Unit
HI0v[1][1], HI1v[1][1]
HI0v[2:m-1][1], HI1v[2:m-1][1]
HI0v[2:m-1][2], HI1v[2:m-1][2]
Lv[1][2]
Lv[m][1]
Lv[m][2]
240
Decoding Unit
290
Information Output Unit

FIG. 8

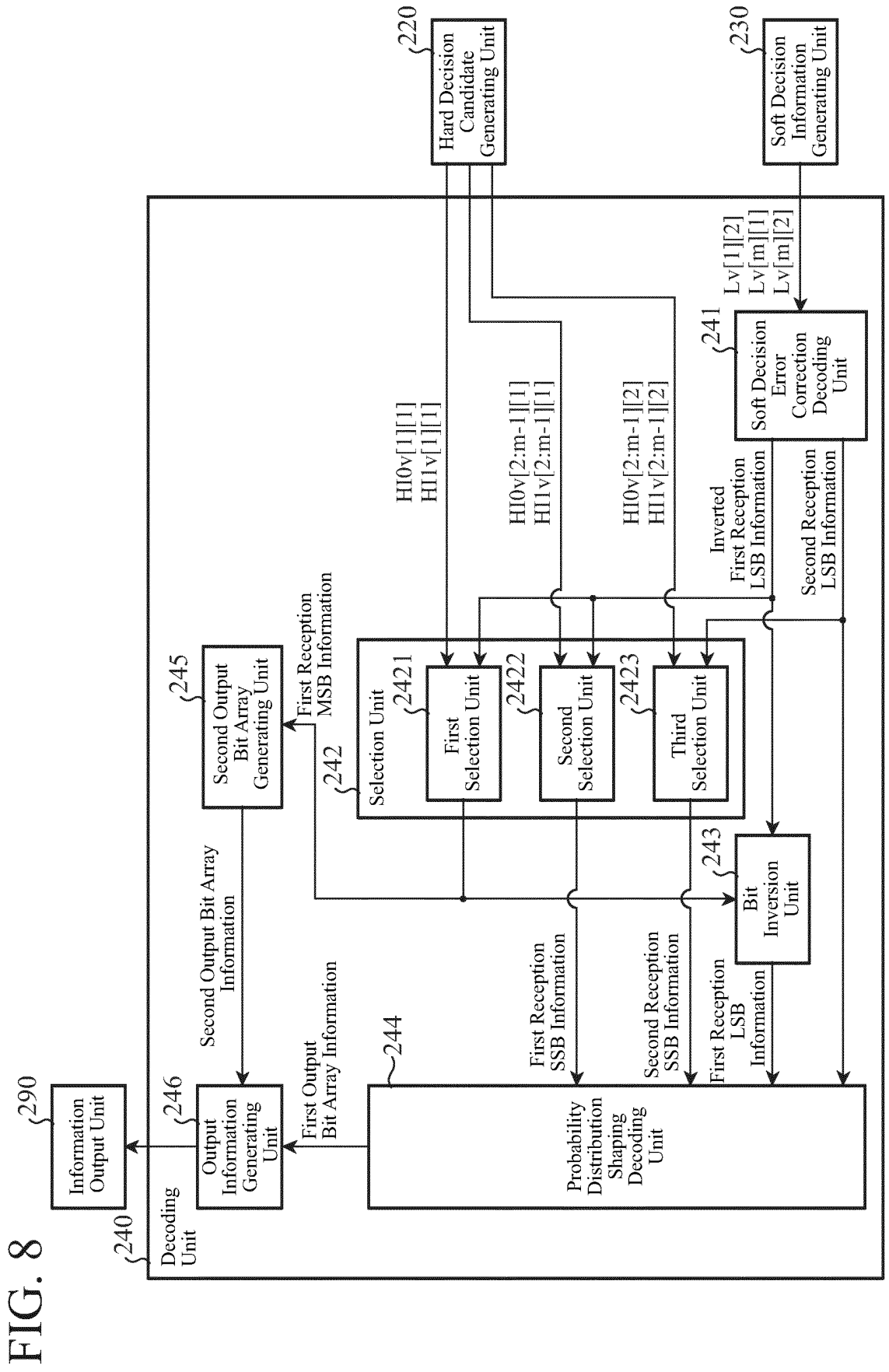

240
Decoding Unit
290
Information Output Unit
246
Output Information Generating Unit
245
Second Output Bit Array Generating Unit
242
Selection Unit
2421
First Selection Unit
2422
Second Selection Unit
2423
Third Selection Unit
243
Bit Inversion Unit
244
Probability Distribution Shaping Decoding Unit
220
Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
241
Soft Decision Error Correction Decoding Unit
First Reception MSB Information
Second Output Bit Array Information
First Output Bit Array Information
HI0v[1][1]
HI1v[1][1]
HI0v[2:m-1][1]
HI1v[2:m-1][1]
HI0v[2:m-1][2]
HI1v[2:m-1][2]
Lv[1][2]
Lv[m][1]
Lv[m][2]
Inverted First Reception LSB Information
Second Reception LSB Information
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information

FIG. 9A

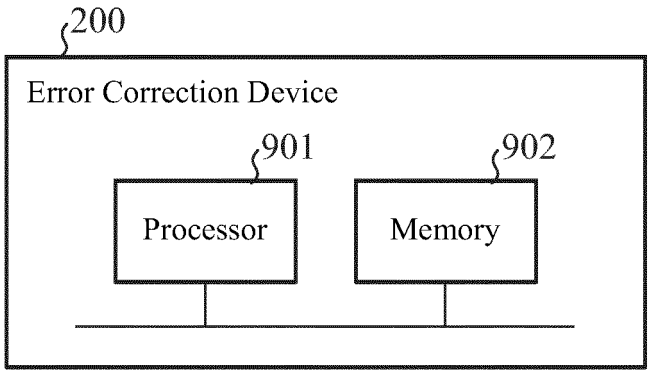

200
Error Correction Device
901
902
Processor
Memory

FIG. 9B

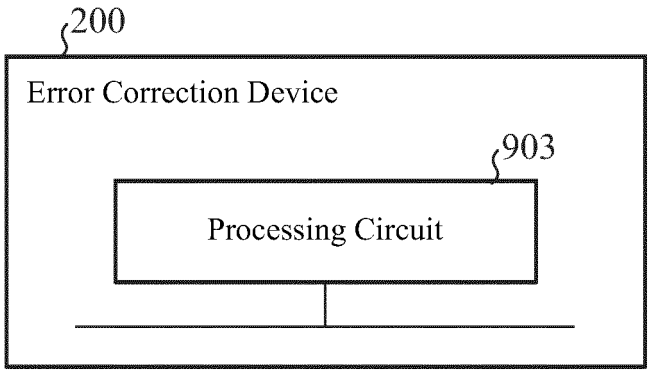

200
Error Correction Device
903
Processing Circuit

FIG. 10A

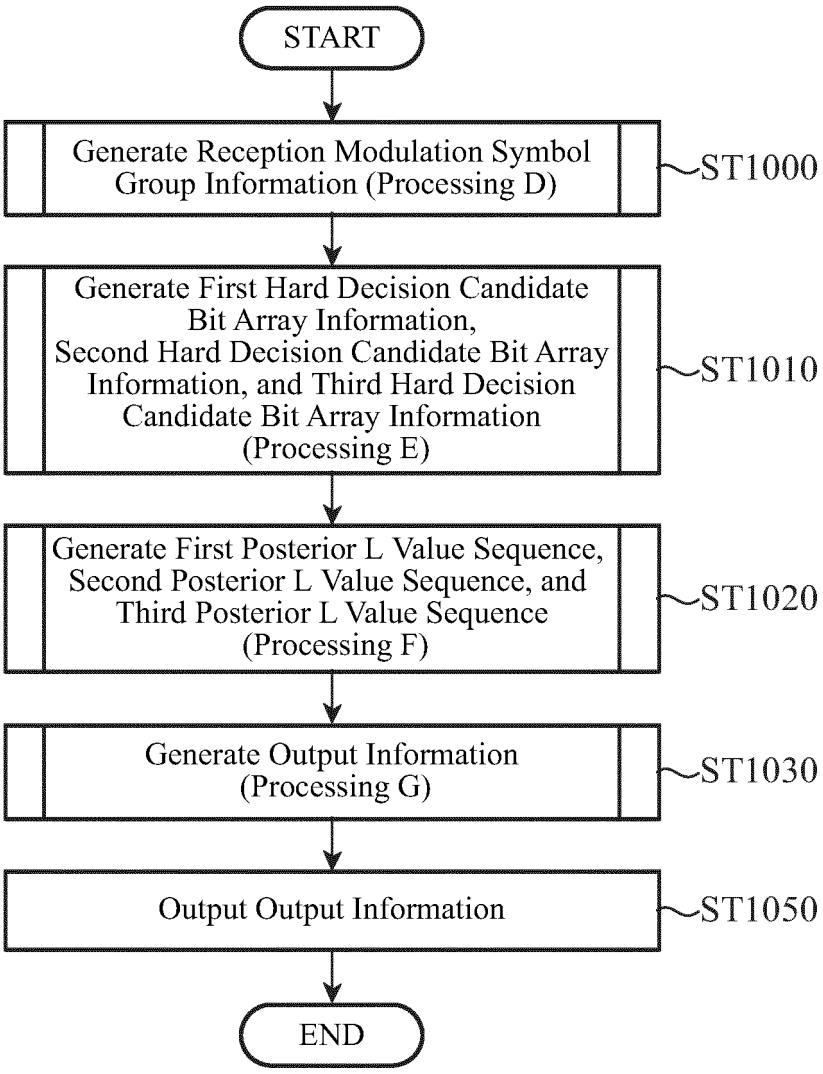

START
Generate Reception Modulation Symbol Group Information (Processing D)
ST1000
Generate First Hard Decision Candidate Bit Array Information, Second Hard Decision Candidate Bit Array Information, and Third Hard Decision Candidate Bit Array Information (Processing E)
ST1010
Generate First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence (Processing F)
ST1020
Generate Output Information (Processing G)
ST1030
Output Output Information
ST1050
END

FIG. 10B

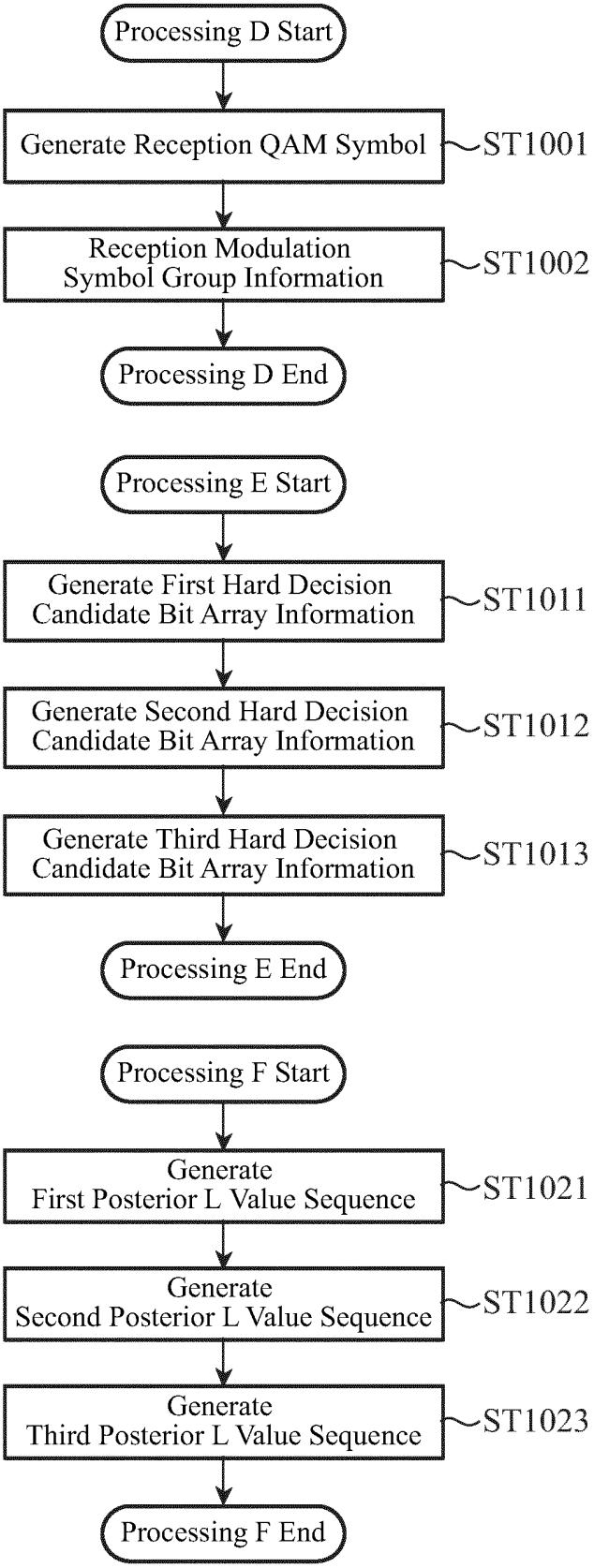

Processing D Start
Generate Reception QAM Symbol
ST1001
Reception Modulation Symbol Group Information
ST1002
Processing D End
Processing E Start
Generate First Hard Decision Candidate Bit Array Information
ST1011
Generate Second Hard Decision Candidate Bit Array Information
ST1012
Generate Third Hard Decision Candidate Bit Array Information
ST1013
Processing E End
Processing F Start
Generate First Posterior L Value Sequence
ST1021
Generate Second Posterior L Value Sequence
ST1022
Generate Third Posterior L Value Sequence
ST1023
Processing F End

FIG. 10C

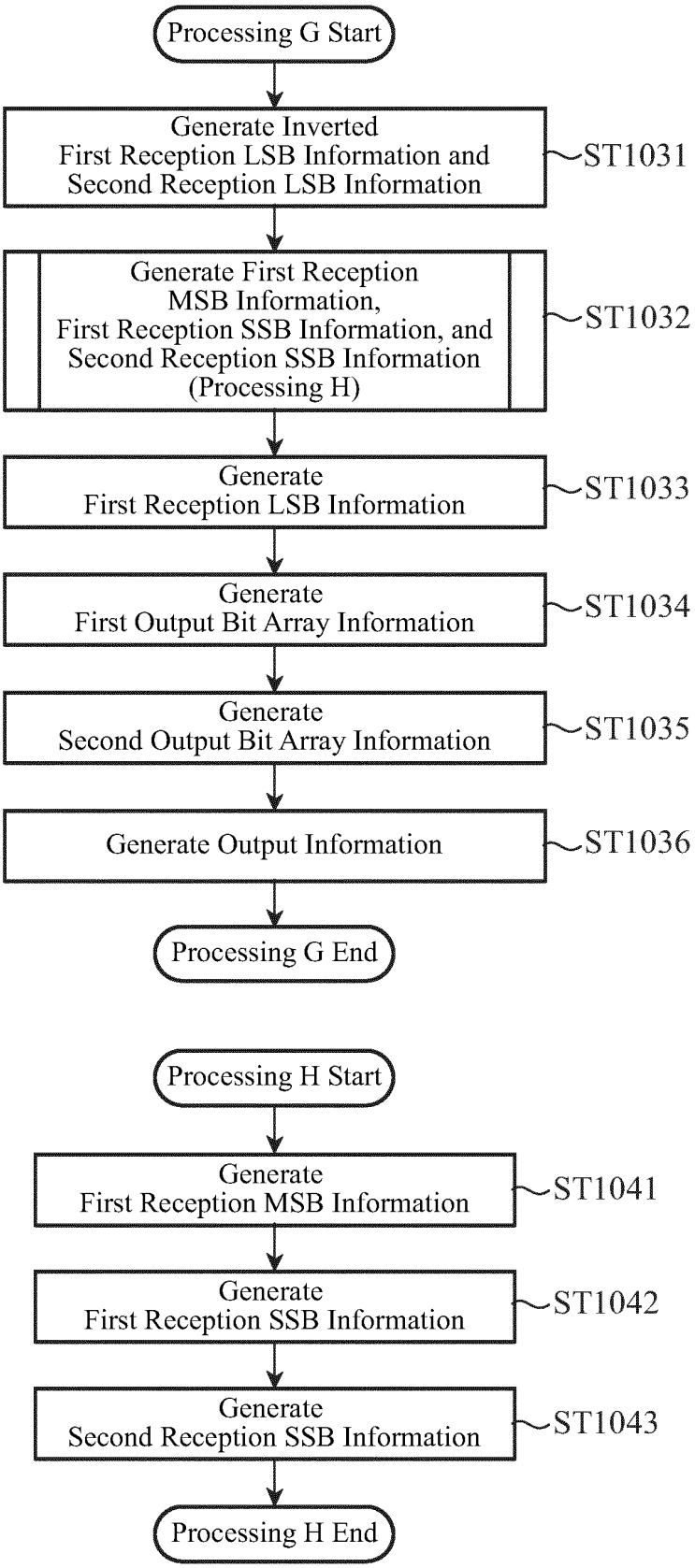

Processing G Start
Generate Inverted First Reception LSB Information and Second Reception LSB Information
ST1031
Generate First Reception MSB Information, First Reception SSB Information, and Second Reception SSB Information (Processing H)
ST1032
Generate First Reception LSB Information
ST1033
Generate First Output Bit Array Information
ST1034
Generate Second Output Bit Array Information
ST1035
Generate Output Information
ST1036
Processing G End
Processing H Start
Generate First Reception MSB Information
ST1041
Generate First Reception SSB Information
ST1042
Generate Second Reception SSB Information
ST1043
Processing H End

FIG. 11

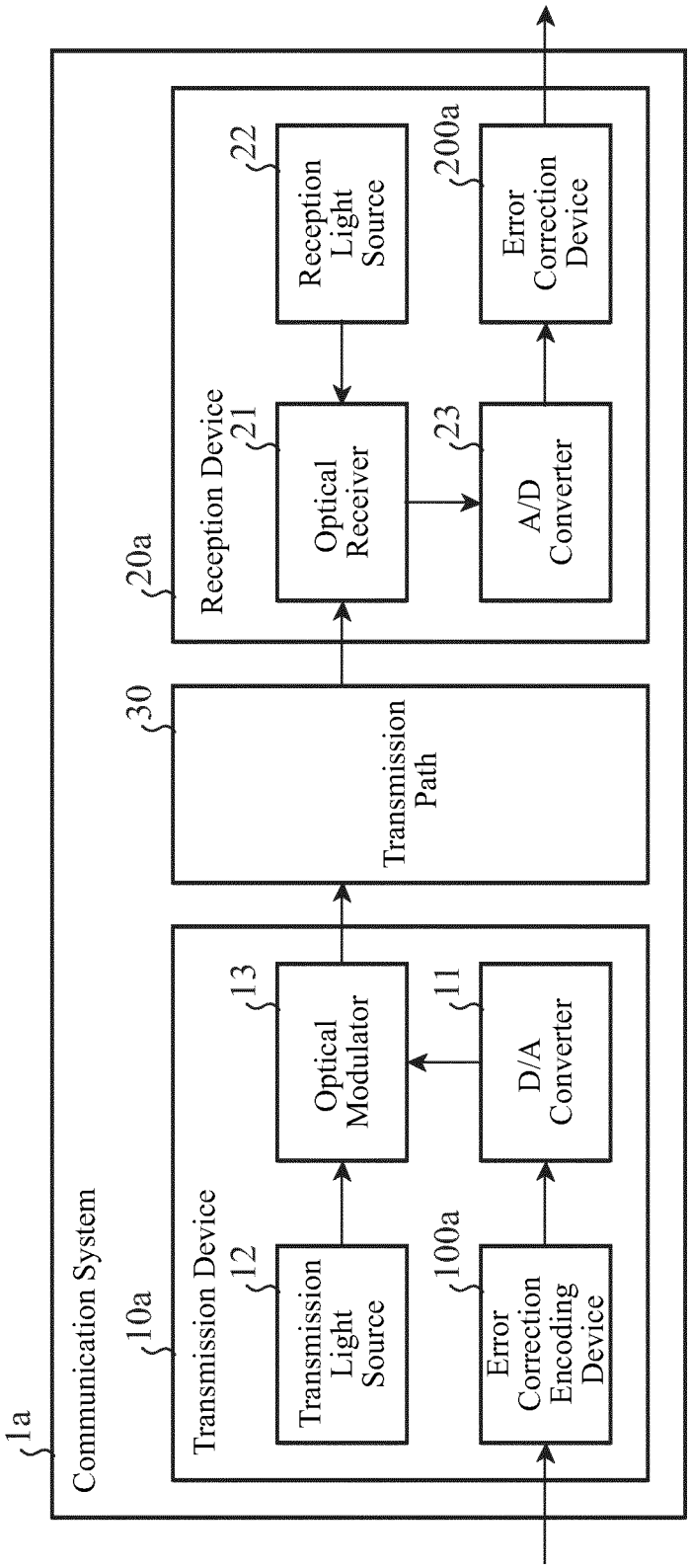

1a
Communication System
10a
Transmission Device
12
Transmission Light Source
13
Optical Modulator
100a
11
D/A Converter
Error Correction Encoding Device
30
Transmission Path
20a
Reception Device
21
Optical Receiver
22
Reception Light Source
23
A/D Converter
200a
Error Correction Device

FIG. 12

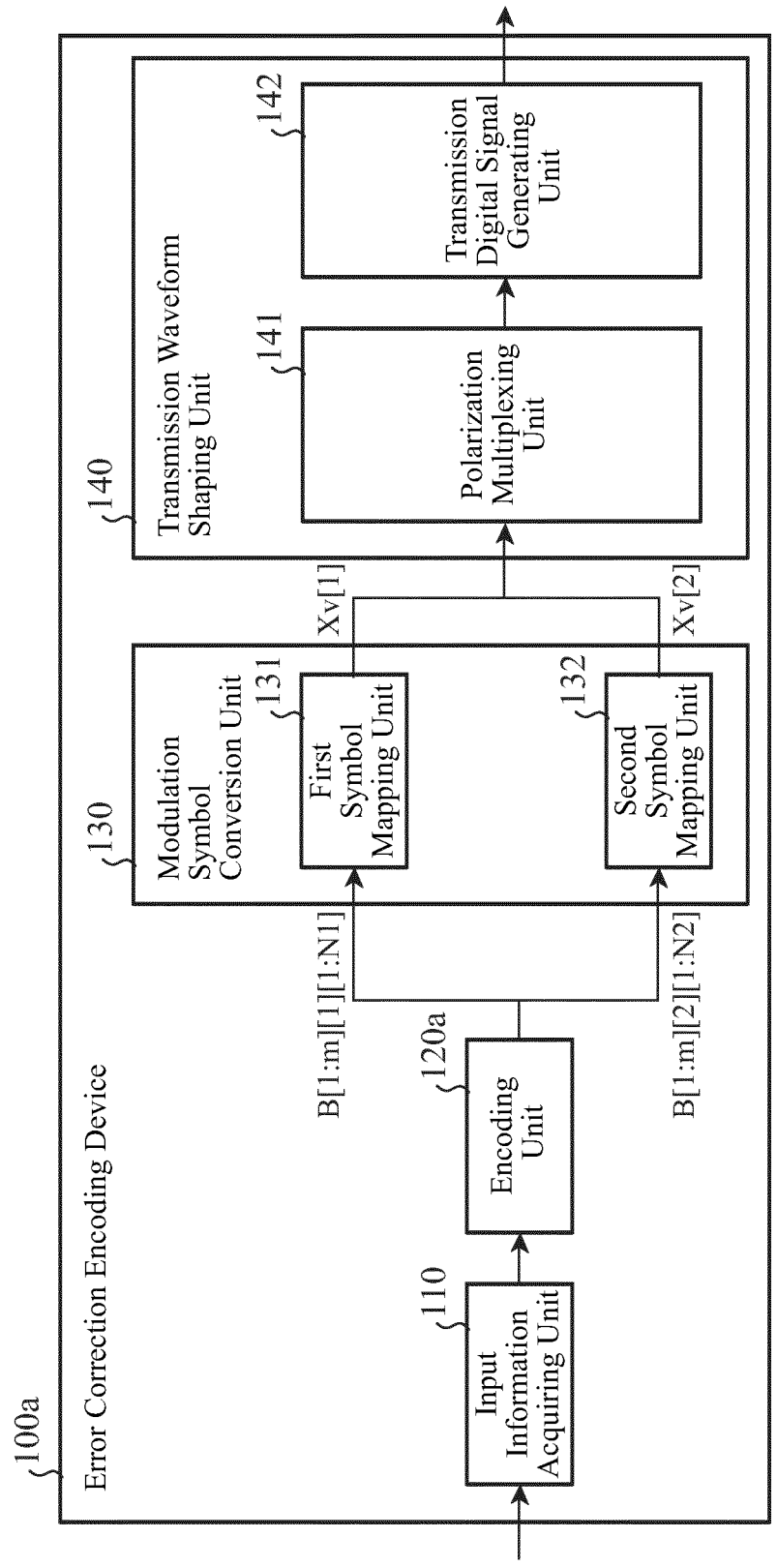

100a
Error Correction Encoding Device
110
Input Information Acquiring Unit
120a
Encoding Unit
B[1:m][1][1:N1]
B[1:m][2][1:N2]
130
Modulation Symbol Conversion Unit
131
First Symbol Mapping Unit
132
Second Symbol Mapping Unit
Xv[1]
Xv[2]
140
Transmission Waveform Shaping Unit
141
Polarization Multiplexing Unit
142
Transmission Digital Signal Generating Unit

FIG. 13

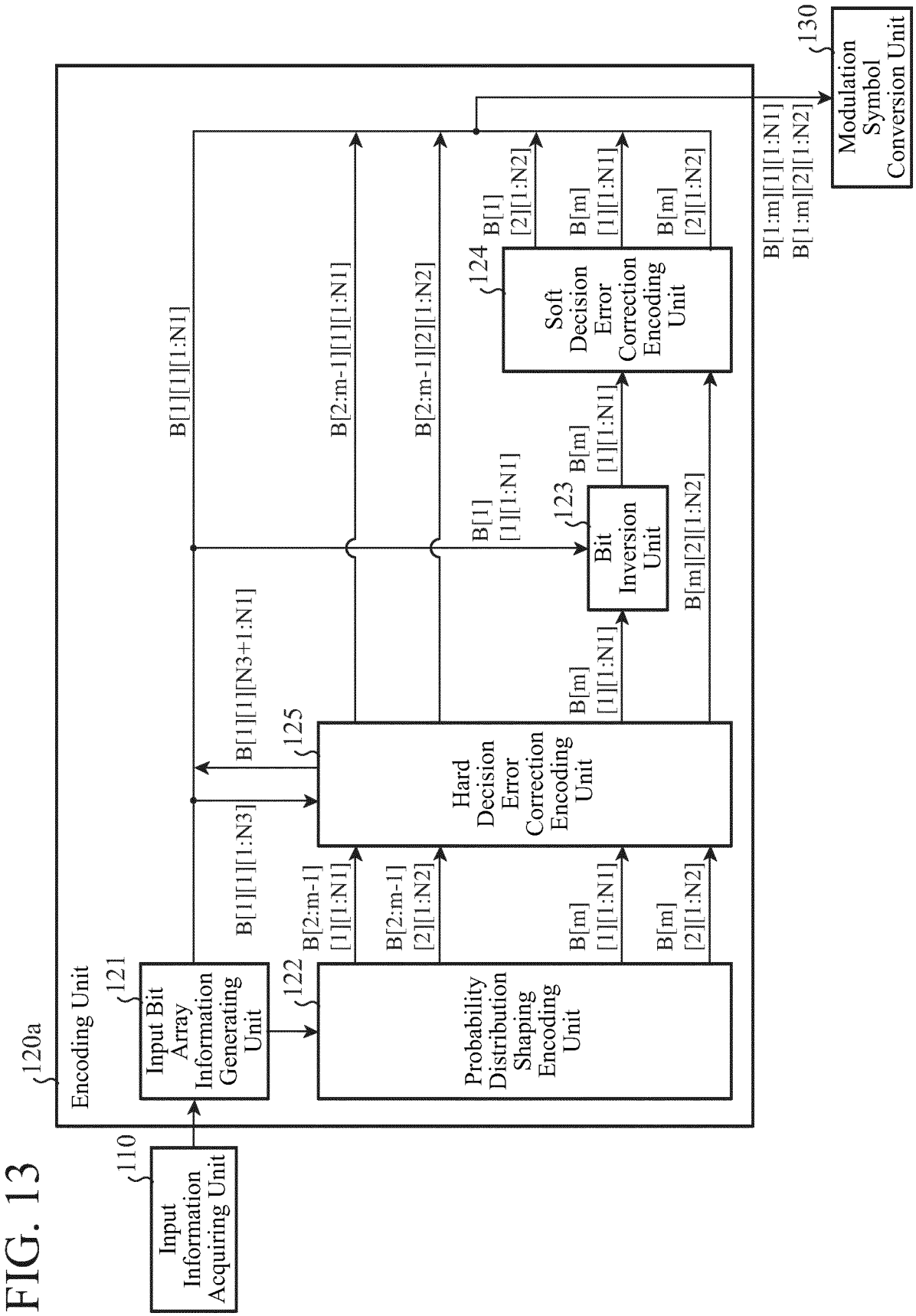

Input Information Acquiring Unit
110
Encoding Unit
120a
Input Bit Array Information Generating Unit
121
Probability Distribution Shaping Encoding Unit
122
Hard Decision Error Correction Encoding Unit
125
Bit Inversion Unit
123
Soft Decision Error Correction Encoding Unit
124
Modulation Symbol Conversion Unit
130
B[1][1][1:N1]
B[1][1][1:N3]
B[1][1][N3+1:N1]
B[2:m-1][1][1:N1]
B[2:m-1][2][1:N2]
B[2:m-1] [1][1:N1]
B[2:m-1] [2][1:N2]
B[m] [1][1:N1]
B[m] [2][1:N2]
B[1] [1][1:N1]
B[m][2][1:N2]
B[1] [2][1:N2]
B[m] [1][1:N1]
B[m] [2][1:N2]
B[1:m][1][1:N1]
B[1:m][2][1:N2]

FIG. 14A

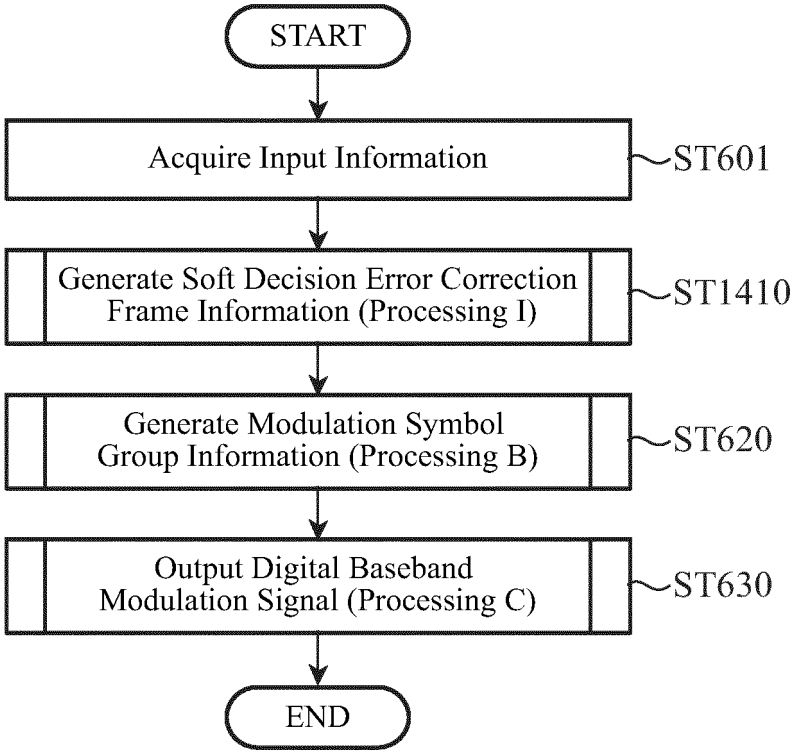

START
Acquire Input Information
ST601
Generate Soft Decision Error Correction Frame Information (Processing I)
ST1410
Generate Modulation Symbol Group Information (Processing B)
ST620
Output Digital Baseband Modulation Signal (Processing C)
ST630
END

FIG. 14B

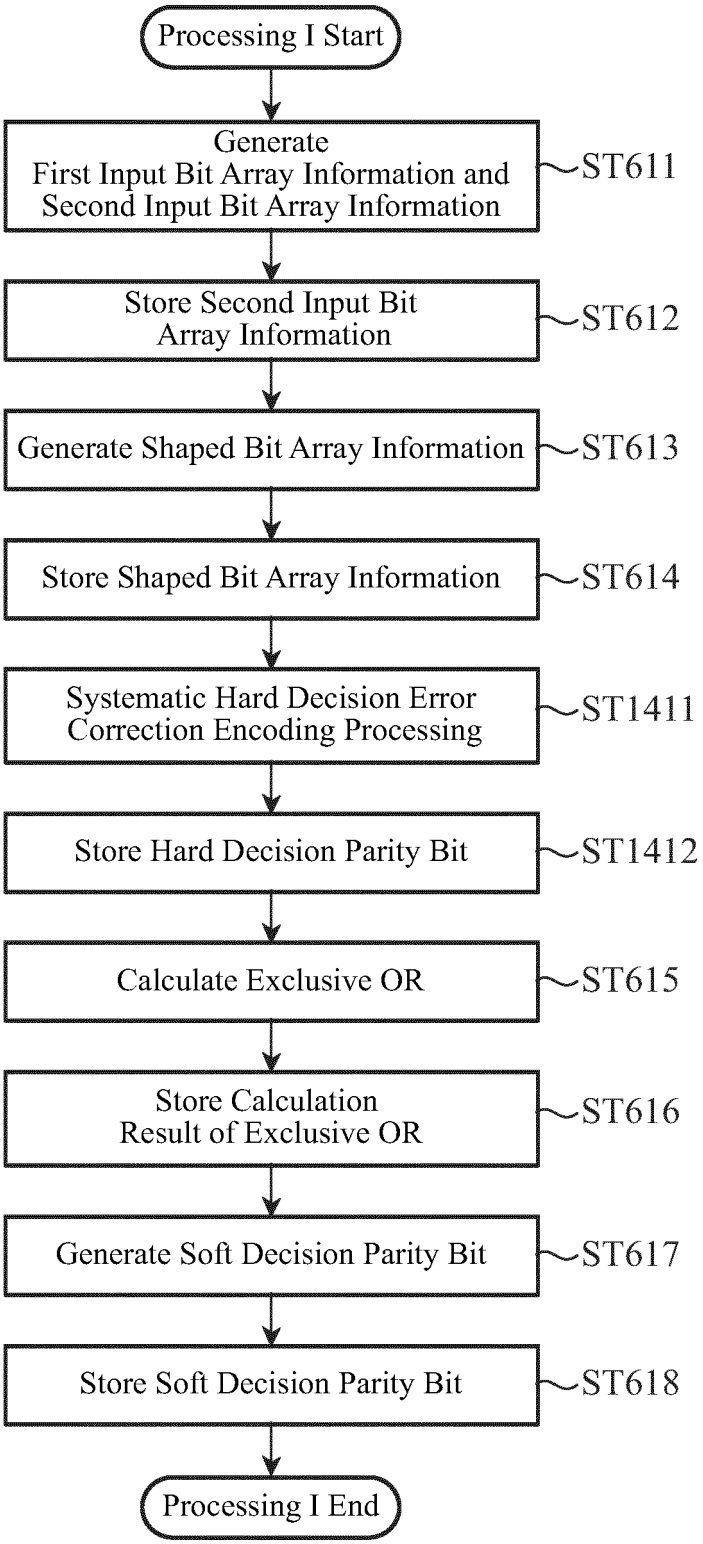
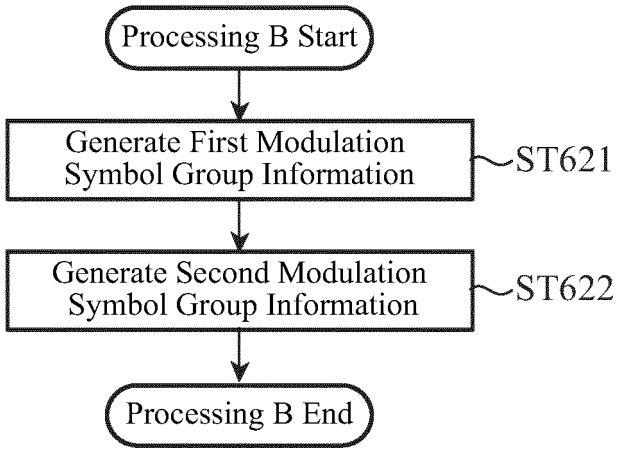

Processing I Start
Generate First Input Bit Array Information and Second Input Bit Array Information
ST611
Store Second Input Bit Array Information
ST612
Generate Shaped Bit Array Information
ST613
Store Shaped Bit Array Information
ST614
Systematic Hard Decision Error Correction Encoding Processing
ST1411
Store Hard Decision Parity Bit
ST1412
Calculate Exclusive OR
ST615
Store Calculation Result of Exclusive OR
ST616
Generate Soft Decision Parity Bit
ST617
Store Soft Decision Parity Bit
ST618
Processing I End

FIG. 14C


Processing B Start
Generate First Modulation Symbol Group Information
ST621
Generate Second Modulation Symbol Group Information
ST622
Processing B End

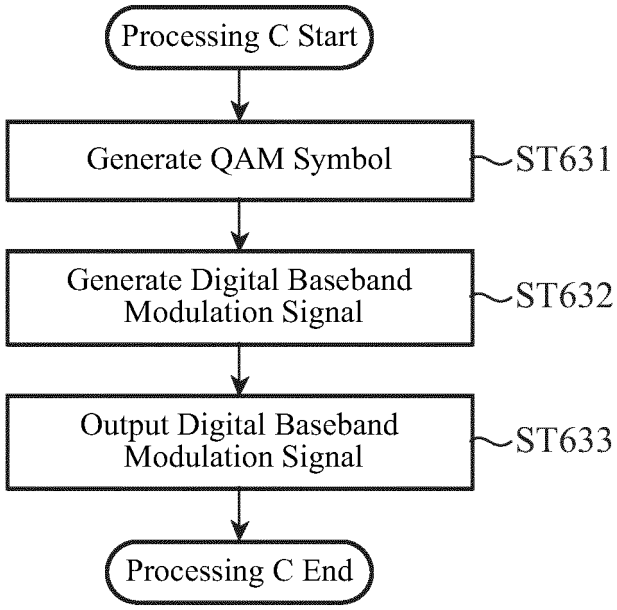

Processing C Start
Generate QAM Symbol
ST631
Generate Digital Baseband Modulation Signal
ST632
Output Digital Baseband Modulation Signal
ST633
Processing C End

FIG. 15

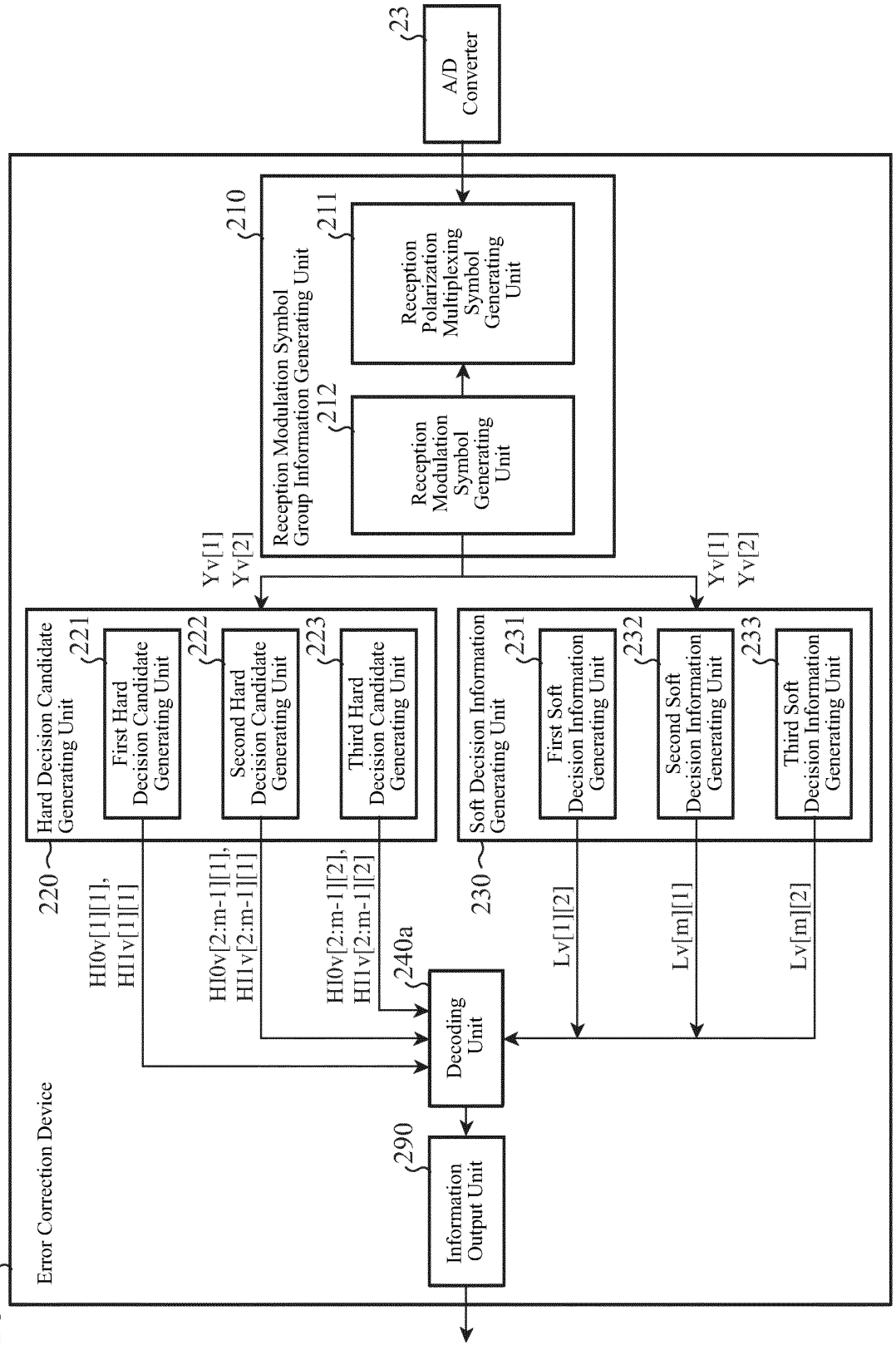

200a
Error Correction Device
23
A/D Converter
210
Reception Modulation Symbol Group Information Generating Unit
211
Reception Polarization Multiplexing Symbol Generating Unit
212
Reception Modulation Symbol Generating Unit
Yv[1]
Yv[2]
220
Hard Decision Candidate Generating Unit
221
First Hard Decision Candidate Generating Unit
222
Second Hard Decision Candidate Generating Unit
223
Third Hard Decision Candidate Generating Unit
HI0v[1][1], HI1v[1][1]
HI0v[2:m-1][1], HI1v[2:m-1][1]
HI0v[2:m-1][2], HI1v[2:m-1][2]
230
Soft Decision Information Generating Unit
231
First Soft Decision Information Generating Unit
232
Second Soft Decision Information Generating Unit
233
Third Soft Decision Information Generating Unit
Lv[1][2]
Lv[m][1]
Lv[m][2]
240a
Decoding Unit
290
Information Output Unit

FIG. 16

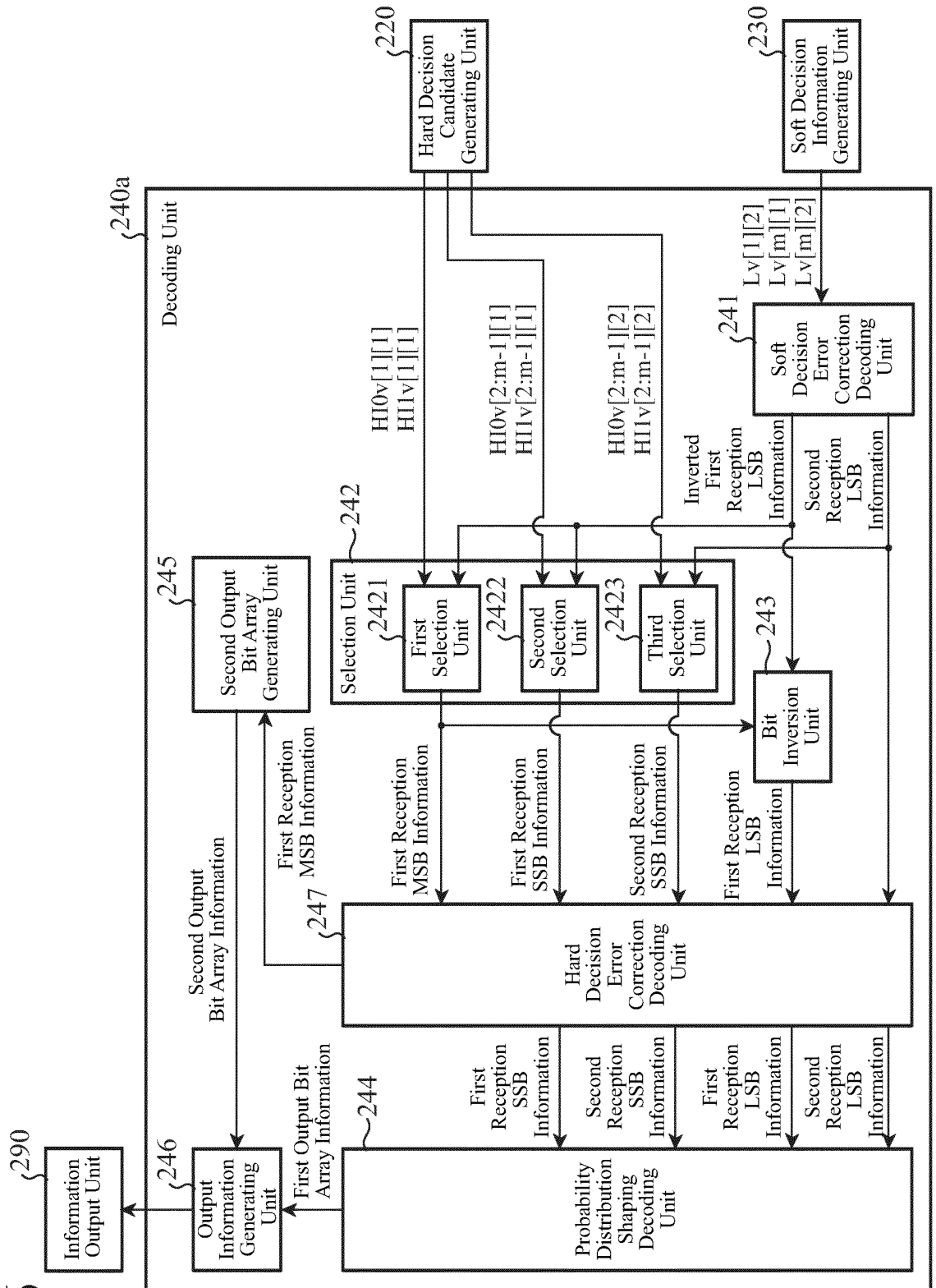

240a
Decoding Unit
220
Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
241
Soft Decision Error Correction Decoding Unit
242
Selection Unit
2421
First Selection Unit
2422
Second Selection Unit
2423
Third Selection Unit
243
Bit Inversion Unit
245
Second Output Bit Array Generating Unit
246
Output Information Generating Unit
247
Hard Decision Error Correction Decoding Unit
244
Probability Distribution Shaping Decoding Unit
290
Information Output Unit
HI0v[1][1]
HI1v[1][1]
HI0v[2:m-1][1]
HI1v[2:m-1][1]
HI0v[2:m-1][2]
HI1v[2:m-1][2]
Lv[1][2]
Lv[m][1]
Lv[m][2]
Inverted First Reception LSB Information
Second Reception LSB Information
First Reception MSB Information
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information
Second Output Bit Array Information
First Output Bit Array Information
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information
Second Reception LSB Information

FIG. 17A

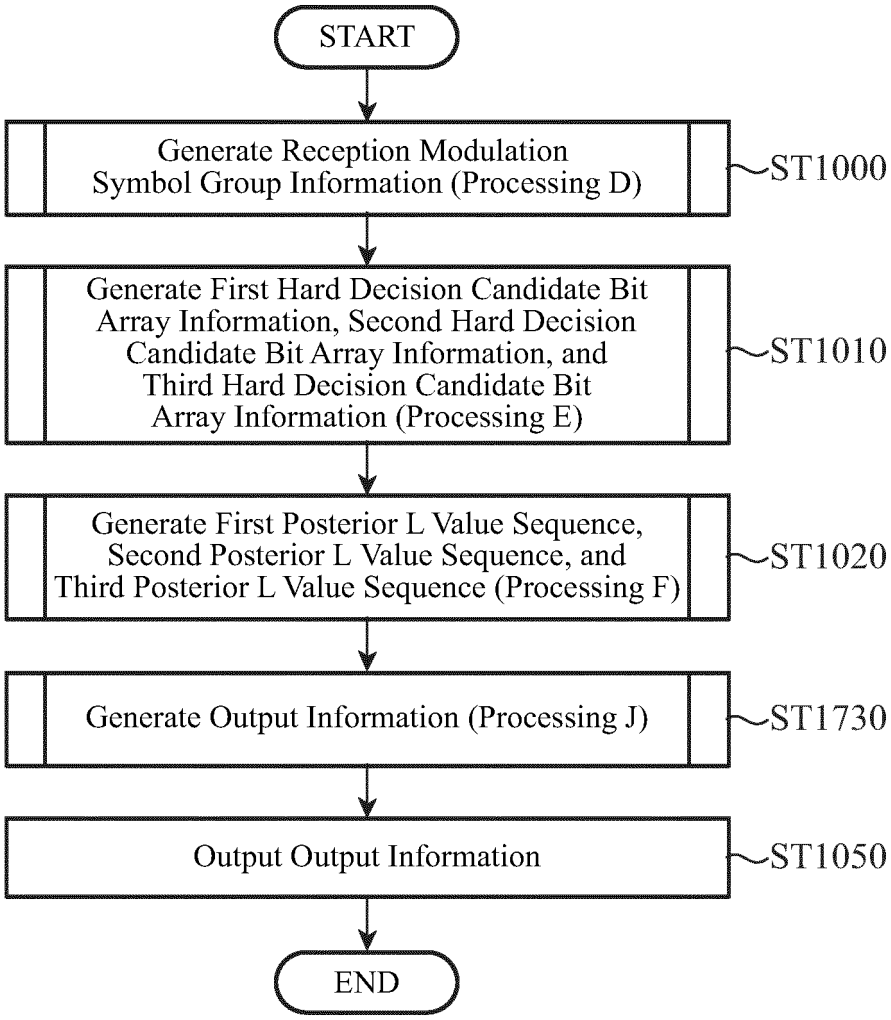

START
Generate Reception Modulation Symbol Group Information (Processing D)
ST1000
Generate First Hard Decision Candidate Bit Array Information, Second Hard Decision Candidate Bit Array Information, and Third Hard Decision Candidate Bit Array Information (Processing E)
ST1010
Generate First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence (Processing F)
ST1020
Generate Output Information (Processing J)
ST1730
Output Output Information
ST1050
END

FIG. 17B

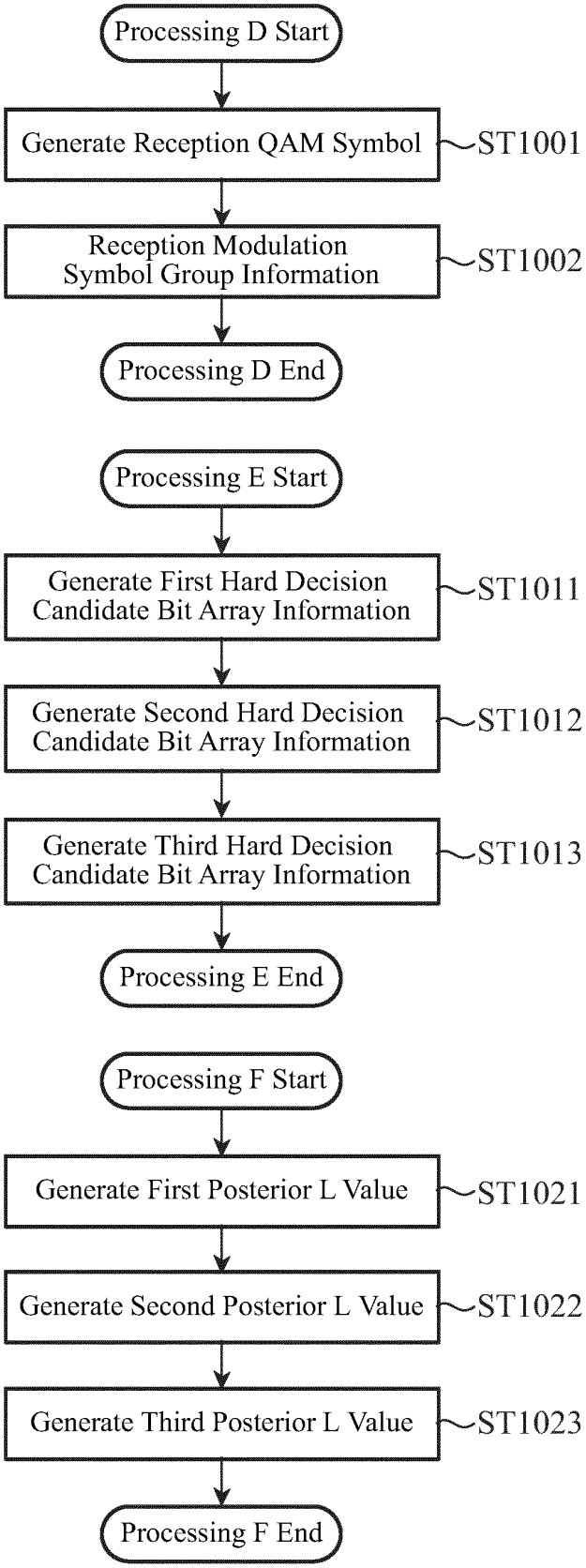

Processing D Start
Generate Reception QAM Symbol
ST1001
Reception Modulation Symbol Group Information
ST1002
Processing D End
Processing E Start
Generate First Hard Decision Candidate Bit Array Information
ST1011
Generate Second Hard Decision Candidate Bit Array Information
ST1012
Generate Third Hard Decision Candidate Bit Array Information
ST1013
Processing E End
Processing F Start
Generate First Posterior L Value
ST1021
Generate Second Posterior L Value
ST1022
Generate Third Posterior L Value
ST1023
Processing F End

FIG. 17C

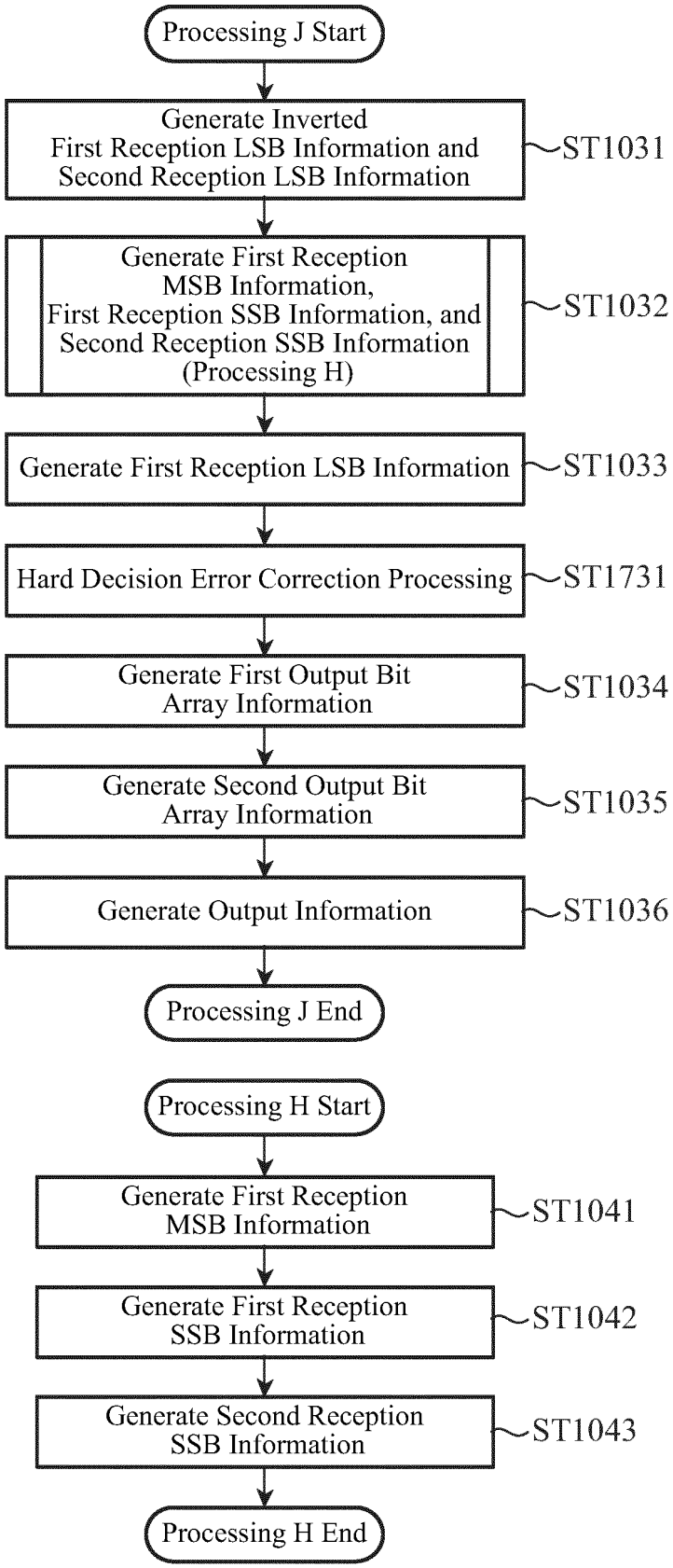

Processing J Start
Generate Inverted First Reception LSB Information and Second Reception LSB Information
ST1031
Generate First Reception MSB Information, First Reception SSB Information, and Second Reception SSB Information (Processing H)
ST1032
Generate First Reception LSB Information
ST1033
Hard Decision Error Correction Processing
ST1731
Generate First Output Bit Array Information
ST1034
Generate Second Output Bit Array Information
ST1035
Generate Output Information
ST1036
Processing J End
Processing H Start
Generate First Reception MSB Information
ST1041
Generate First Reception SSB Information
ST1042
Generate Second Reception SSB Information
ST1043
Processing H End

FIG. 18

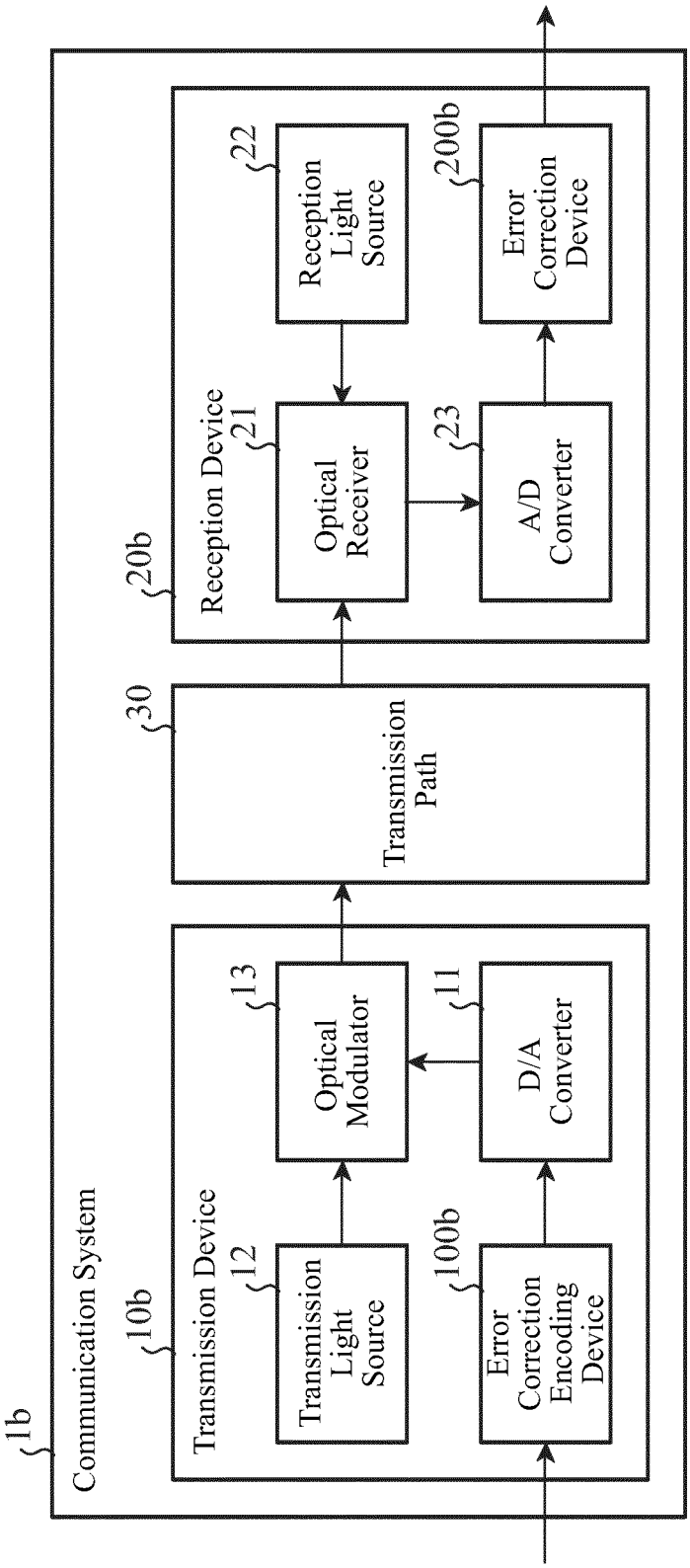

1b
Communication System
10b
Transmission Device
12
Transmission Light Source
100b
Error Correction Encoding Device
13
Optical Modulator
11
D/A Converter
30
Transmission Path
20b
Reception Device
21
Optical Receiver
22
Reception Light Source
23
A/D Converter
200b
Error Correction Device

FIG. 19

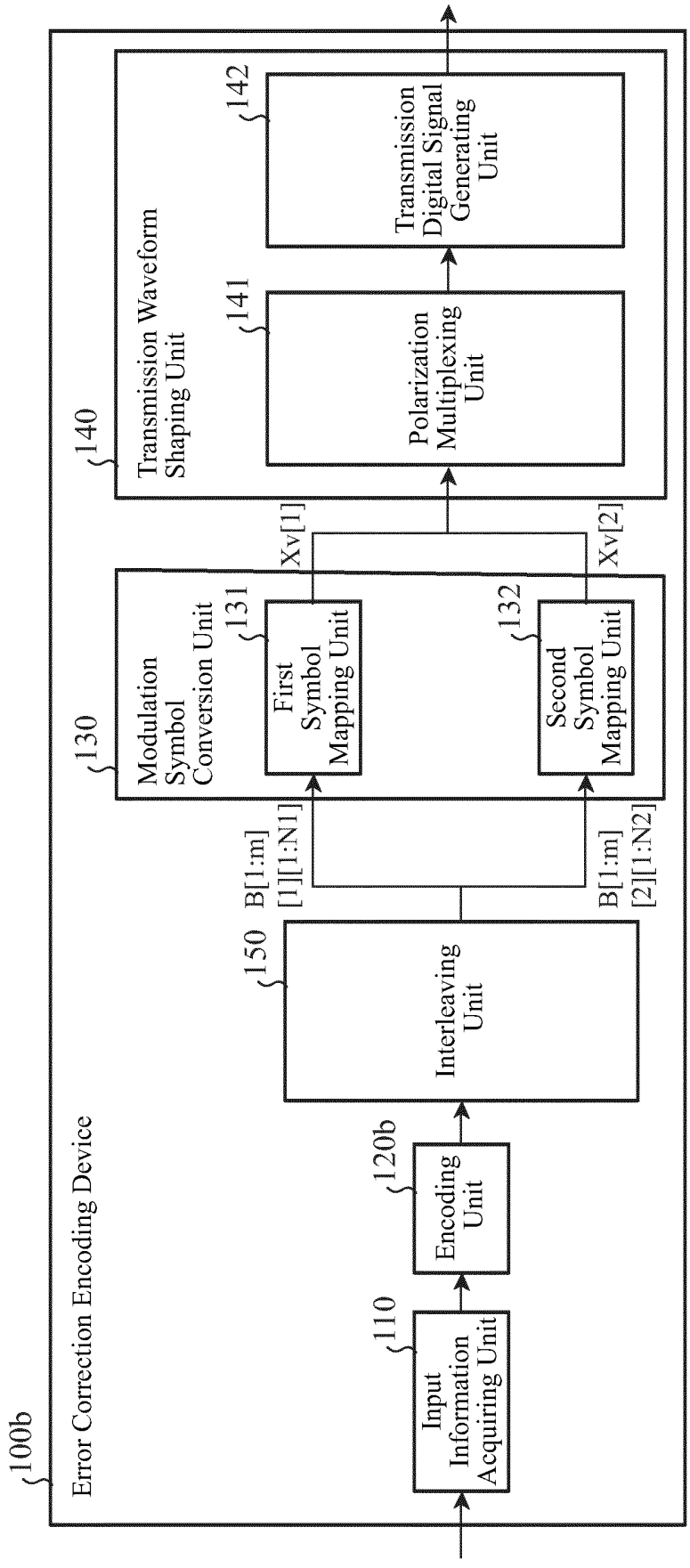

100b
Error Correction Encoding Device
110
Input Information Acquiring Unit
120b
Encoding Unit
150
Interleaving Unit
B[1:m] [1][1:N1]
B[1:m] [2][1:N2]
130
Modulation Symbol Conversion Unit
131
First Symbol Mapping Unit
132
Second Symbol Mapping Unit
Xv[1]
Xv[2]
140
Transmission Waveform Shaping Unit
141
Polarization Multiplexing Unit
142
Transmission Digital Signal Generating Unit

FIG. 20

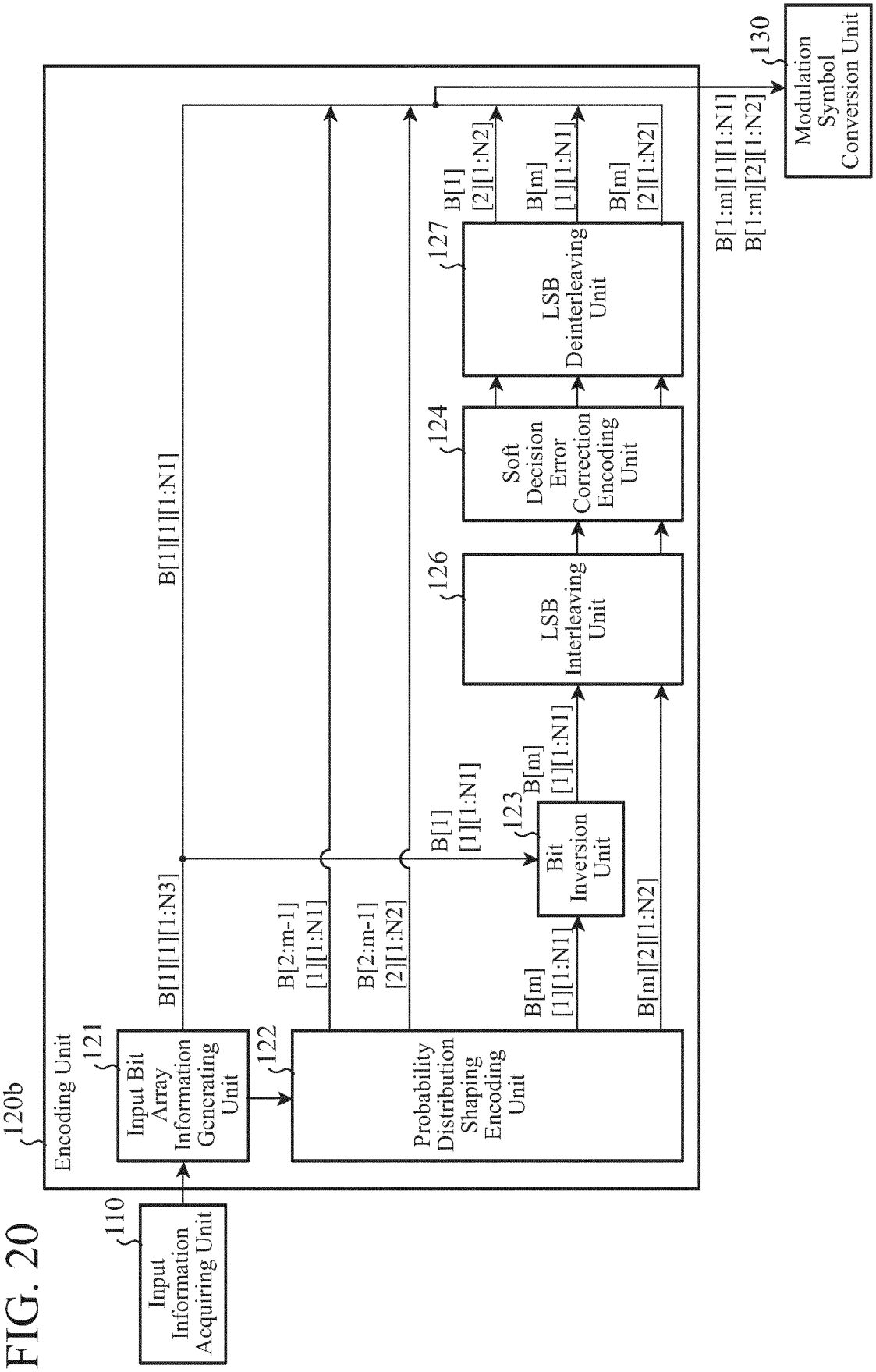

110
Input Information Acquiring Unit
120b
Encoding Unit
121
Input Bit Array Information Generating Unit
122
Probability Distribution Shaping Encoding Unit
123
Bit Inversion Unit
124
Soft Decision Error Correction Encoding Unit
126
LSB Interleaving Unit
127
LSB Deinterleaving Unit
130
Modulation Symbol Conversion Unit
B[1][1][1:N3]
B[1][1][1:N1]
B[2:m-1][1][1:N1]
B[2:m-1][2][1:N2]
B[1][1][1:N1]
B[m][1][1:N1]
B[m][2][1:N2]
B[1][2][1:N2]
B[m][1][1:N1]
B[m][2][1:N2]
B[1:m][1][1:N1]
B[1:m][2][1:N2]

FIG. 21A

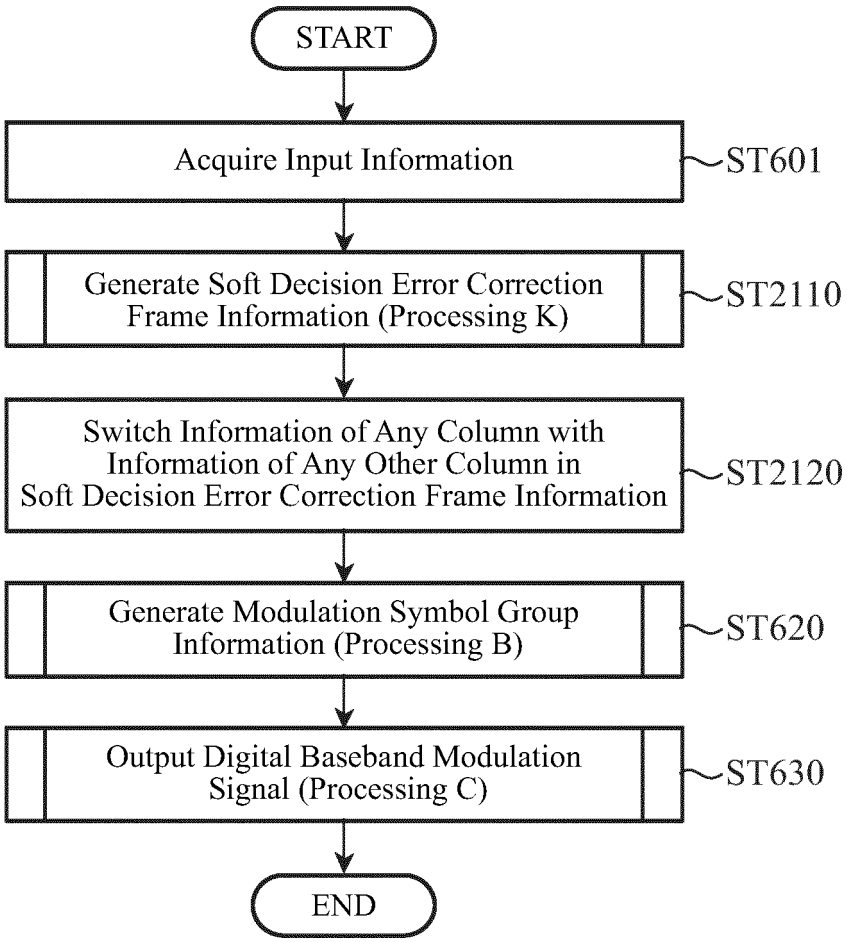

START
Acquire Input Information
ST601
Generate Soft Decision Error Correction Frame Information (Processing K)
ST2110
Switch Information of Any Column with Information of Any Other Column in Soft Decision Error Correction Frame Information
ST2120
Generate Modulation Symbol Group Information (Processing B)
ST620
Output Digital Baseband Modulation Signal (Processing C)
ST630
END

FIG. 21B

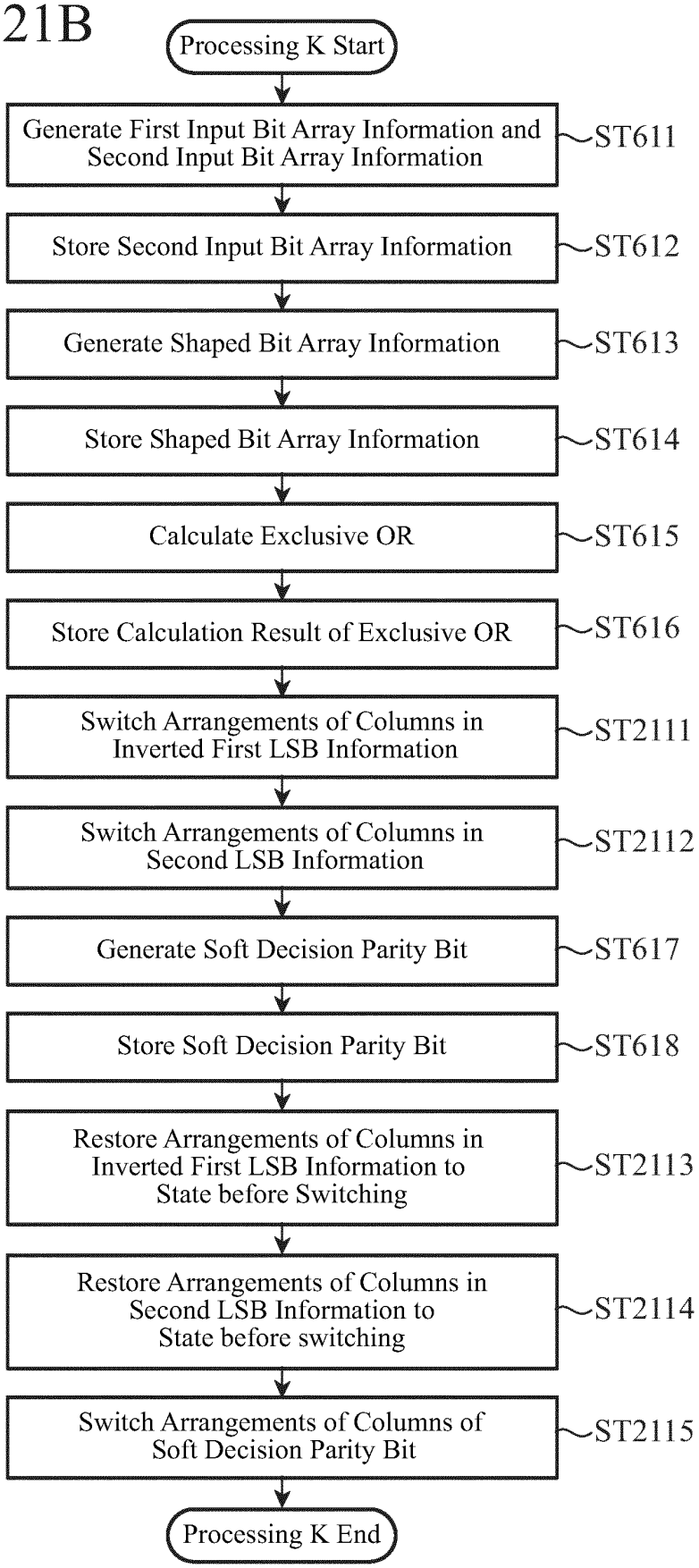
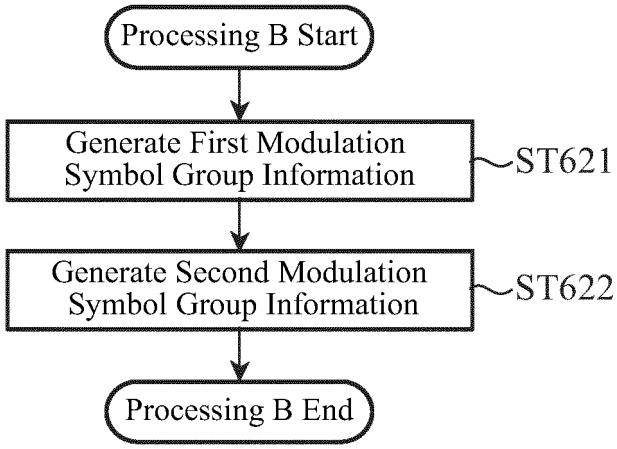

Processing K Start
Generate First Input Bit Array Information and Second Input Bit Array Information
ST611
Store Second Input Bit Array Information
ST612
Generate Shaped Bit Array Information
ST613
Store Shaped Bit Array Information
ST614
Calculate Exclusive OR
ST615
Store Calculation Result of Exclusive OR
ST616
Switch Arrangements of Columns in Inverted First LSB Information
ST2111
Switch Arrangements of Columns in Second LSB Information
ST2112
Generate Soft Decision Parity Bit
ST617
Store Soft Decision Parity Bit
ST618
Restore Arrangements of Columns in Inverted First LSB Information to State before Switching
ST2113
Restore Arrangements of Columns in Second LSB Information to State before switching
ST2114
Switch Arrangements of Columns of Soft Decision Parity Bit
ST2115
Processing K End

FIG. 21C


Processing B Start
Generate First Modulation Symbol Group Information
ST621
Generate Second Modulation Symbol Group Information
ST622
Processing B End

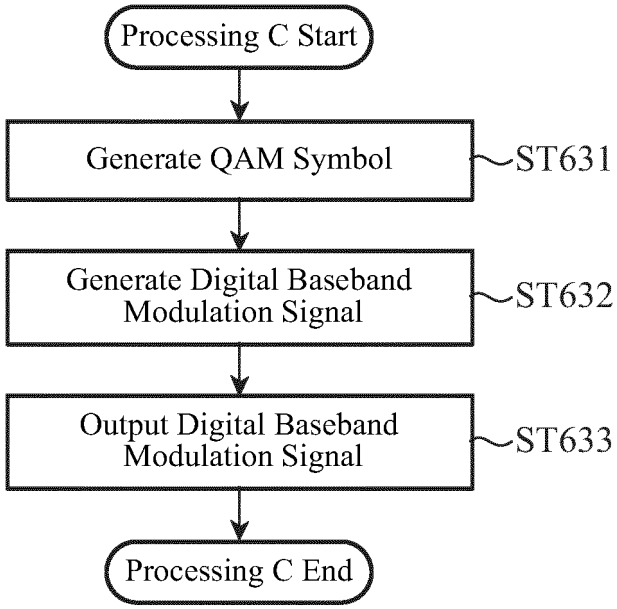

Processing C Start
Generate QAM Symbol
ST631
Generate Digital Baseband Modulation Signal
ST632
Output Digital Baseband Modulation Signal
ST633
Processing C End

FIG. 22

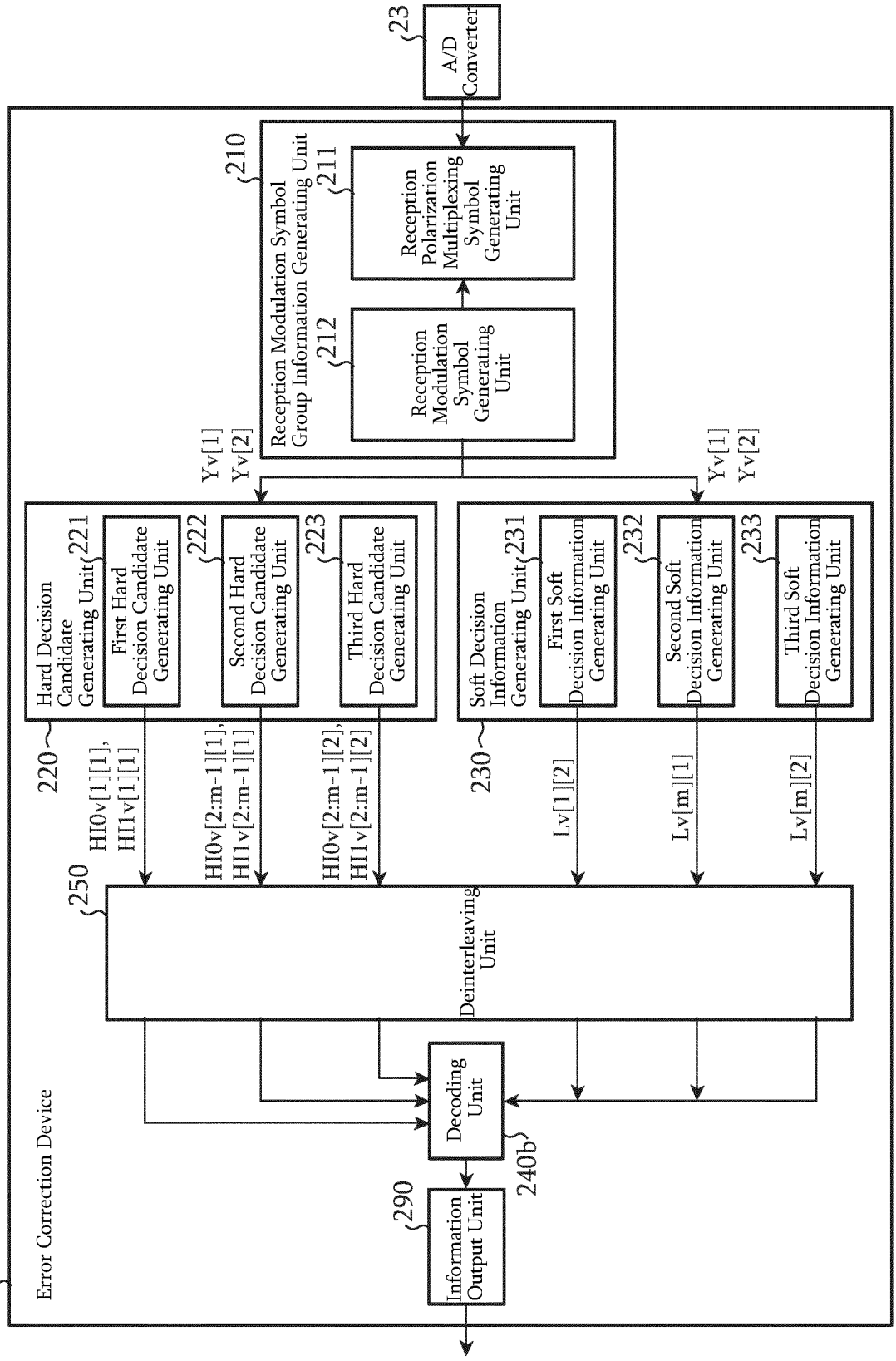

200b
Error Correction Device
23
A/D Converter
210
Reception Modulation Symbol Group Information Generating Unit
211
Reception Polarization Multiplexing Symbol Generating Unit
212
Reception Modulation Symbol Generating Unit
Yv[1] Yv[2]
Yv[1] Yv[2]
220
Hard Decision Candidate Generating Unit
221
First Hard Decision Candidate Generating Unit
222
Second Hard Decision Candidate Generating Unit
223
Third Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
231
First Soft Decision Information Generating Unit
232
Second Soft Decision Information Generating Unit
233
Third Soft Decision Information Generating Unit
HI0v[1][1], HI1v[1][1]
HI0v[2:m-1][1], HI1v[2:m-1][1]
HI0v[2:m-1][2], HI1v[2:m-1][2]
Lv[1][2]
Lv[m][1]
Lv[m][2]
250
Deinterleaving Unit
Decoding Unit
240b
290
Information Output Unit

FIG. 23

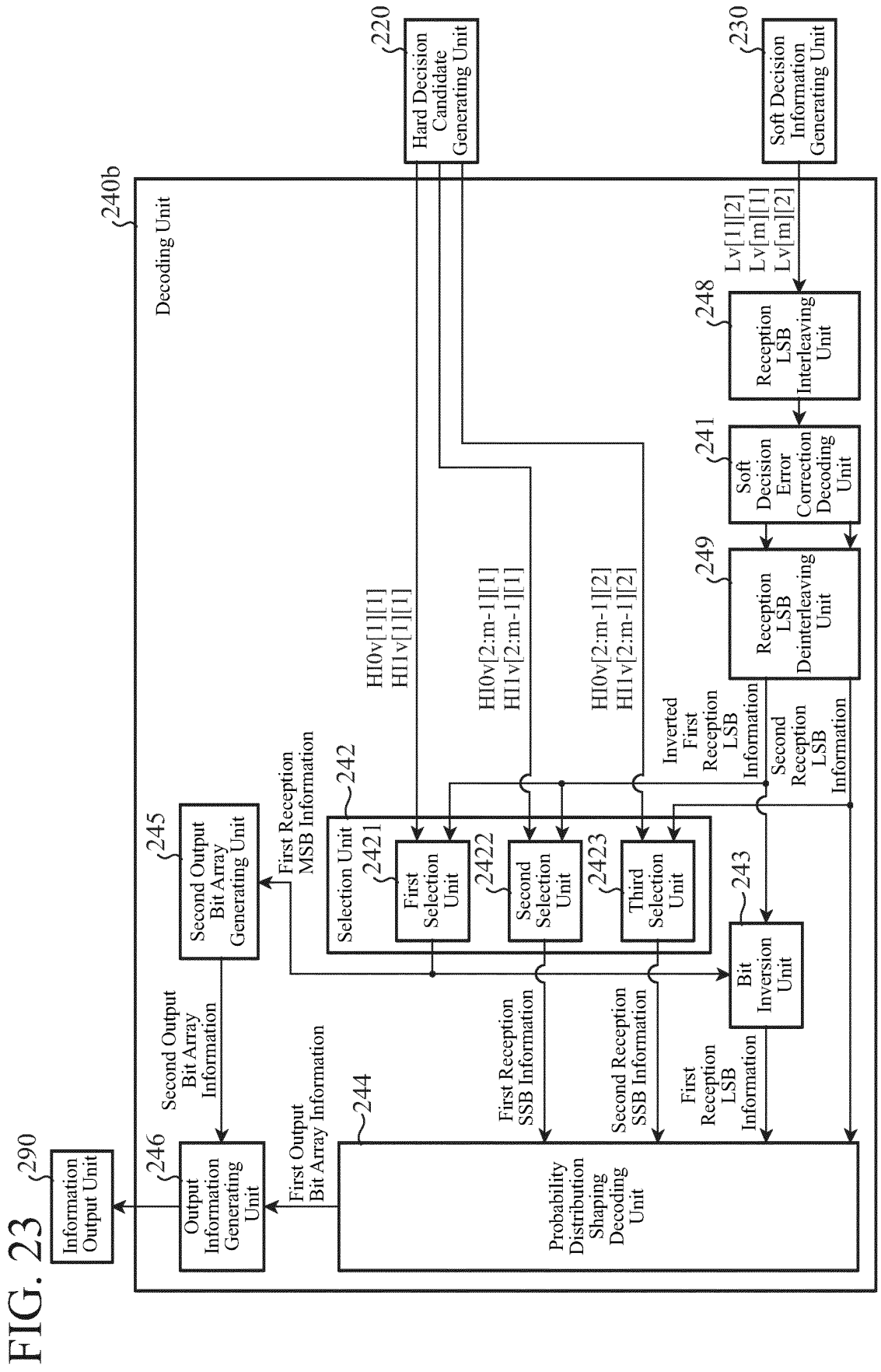

290
Information Output Unit
240b
Decoding Unit
220
Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
Lv[1][2]
Lv[m][1]
Lv[m][2]
248
Reception LSB Interleaving Unit
241
Soft Decision Error Correction Decoding Unit
249
Reception LSB Deinterleaving Unit
HI0v[1][1]
HI1v[1][1]
HI0v[2:m-1][1]
HI1v[2:m-1][1]
HI0v[2:m-1][2]
HI1v[2:m-1][2]
Inverted First Reception LSB Information
Second Reception LSB Information
First Reception MSB Information
242
Selection Unit
2421
First Selection Unit
2422
Second Selection Unit
2423
Third Selection Unit
245
Second Output Bit Array Generating Unit
243
Bit Inversion Unit
Second Output Bit Array Information
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information
First Output Bit Array Information
244
246
Output Information Generating Unit
Probability Distribution Shaping Decoding Unit

FIG. 24A

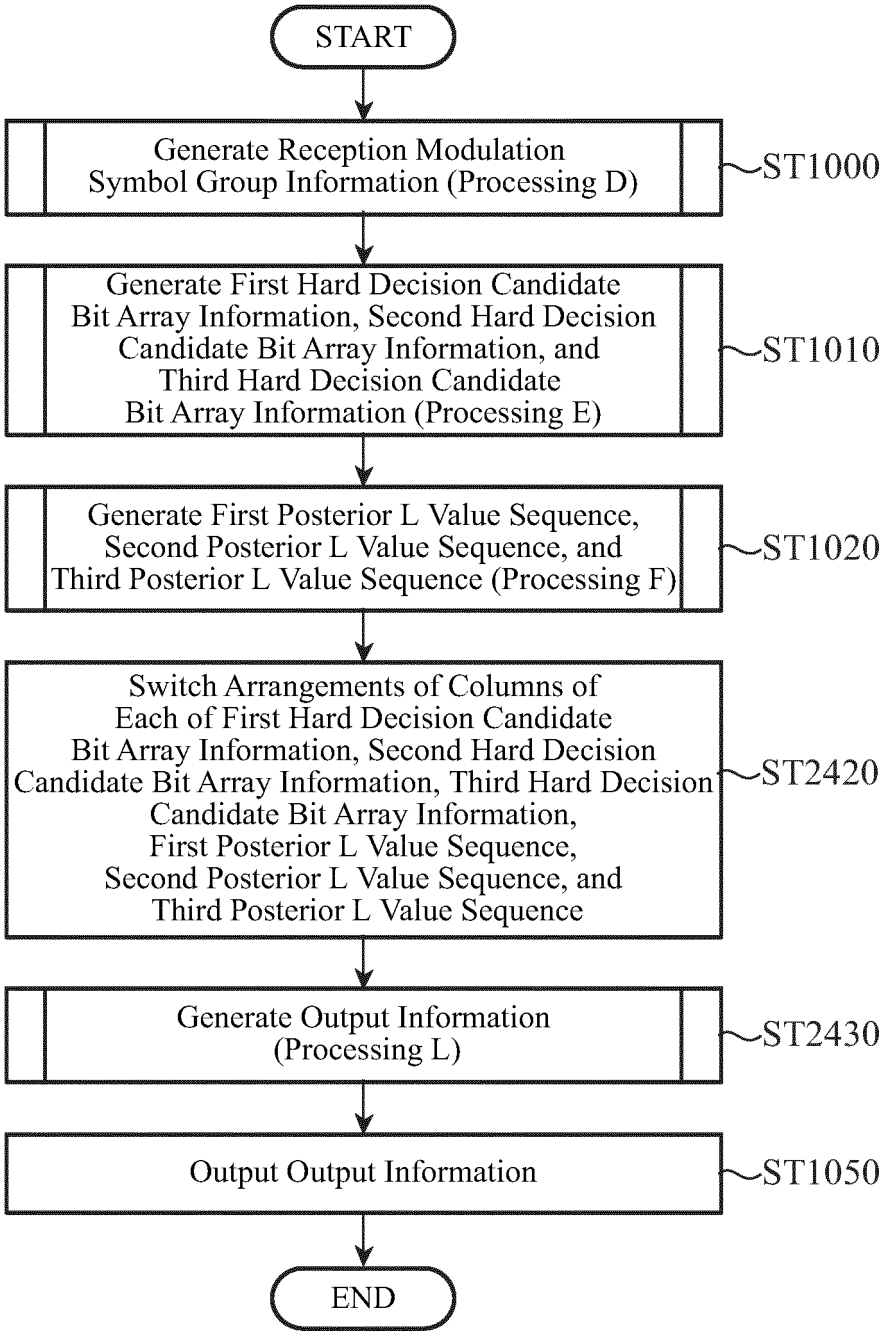

START
Generate Reception Modulation Symbol Group Information (Processing D)
ST1000
Generate First Hard Decision Candidate Bit Array Information, Second Hard Decision Candidate Bit Array Information, and Third Hard Decision Candidate Bit Array Information (Processing E)
ST1010
Generate First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence (Processing F)
ST1020
Switch Arrangements of Columns of Each of First Hard Decision Candidate Bit Array Information, Second Hard Decision Candidate Bit Array Information, Third Hard Decision Candidate Bit Array Information, First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence
ST2420
Generate Output Information (Processing L)
ST2430
Output Output Information
ST1050
END

FIG. 24B

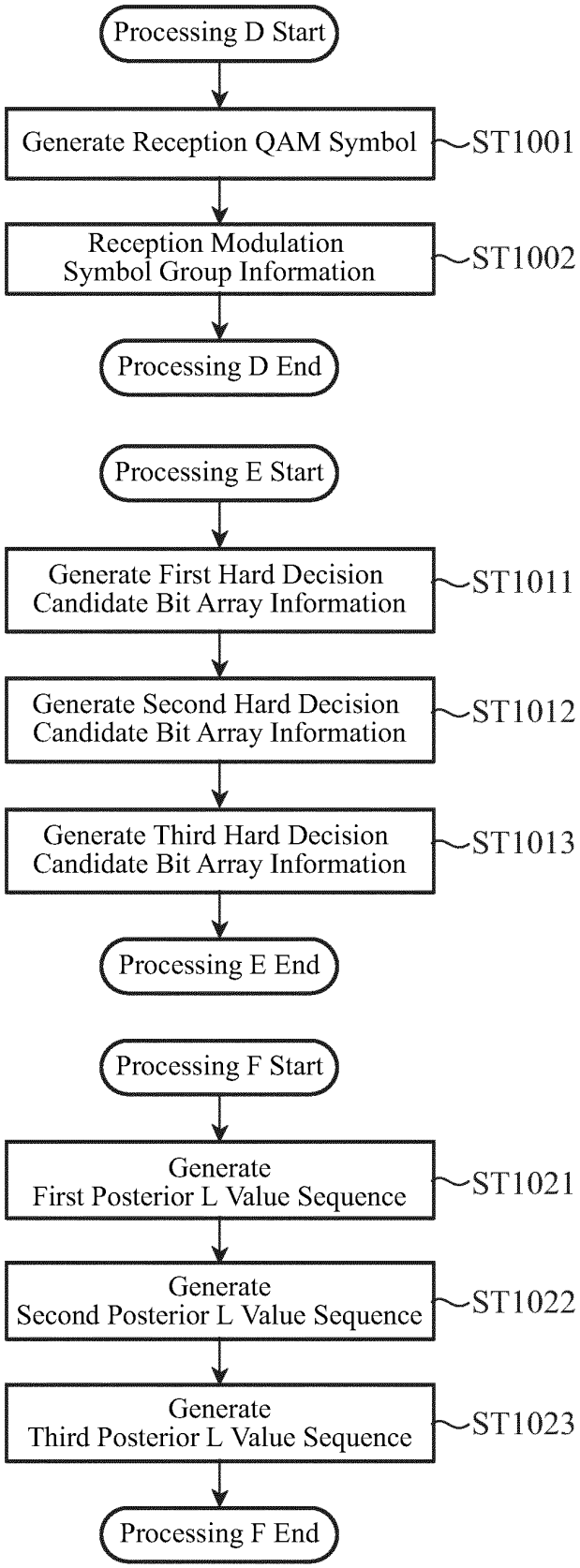

Processing D Start
Generate Reception QAM Symbol
ST1001
Reception Modulation Symbol Group Information
ST1002
Processing D End
Processing E Start
Generate First Hard Decision Candidate Bit Array Information
ST1011
Generate Second Hard Decision Candidate Bit Array Information
ST1012
Generate Third Hard Decision Candidate Bit Array Information
ST1013
Processing E End
Processing F Start
Generate First Posterior L Value Sequence
ST1021
Generate Second Posterior L Value Sequence
ST1022
Generate Third Posterior L Value Sequence
ST1023
Processing F End

FIG. 24C

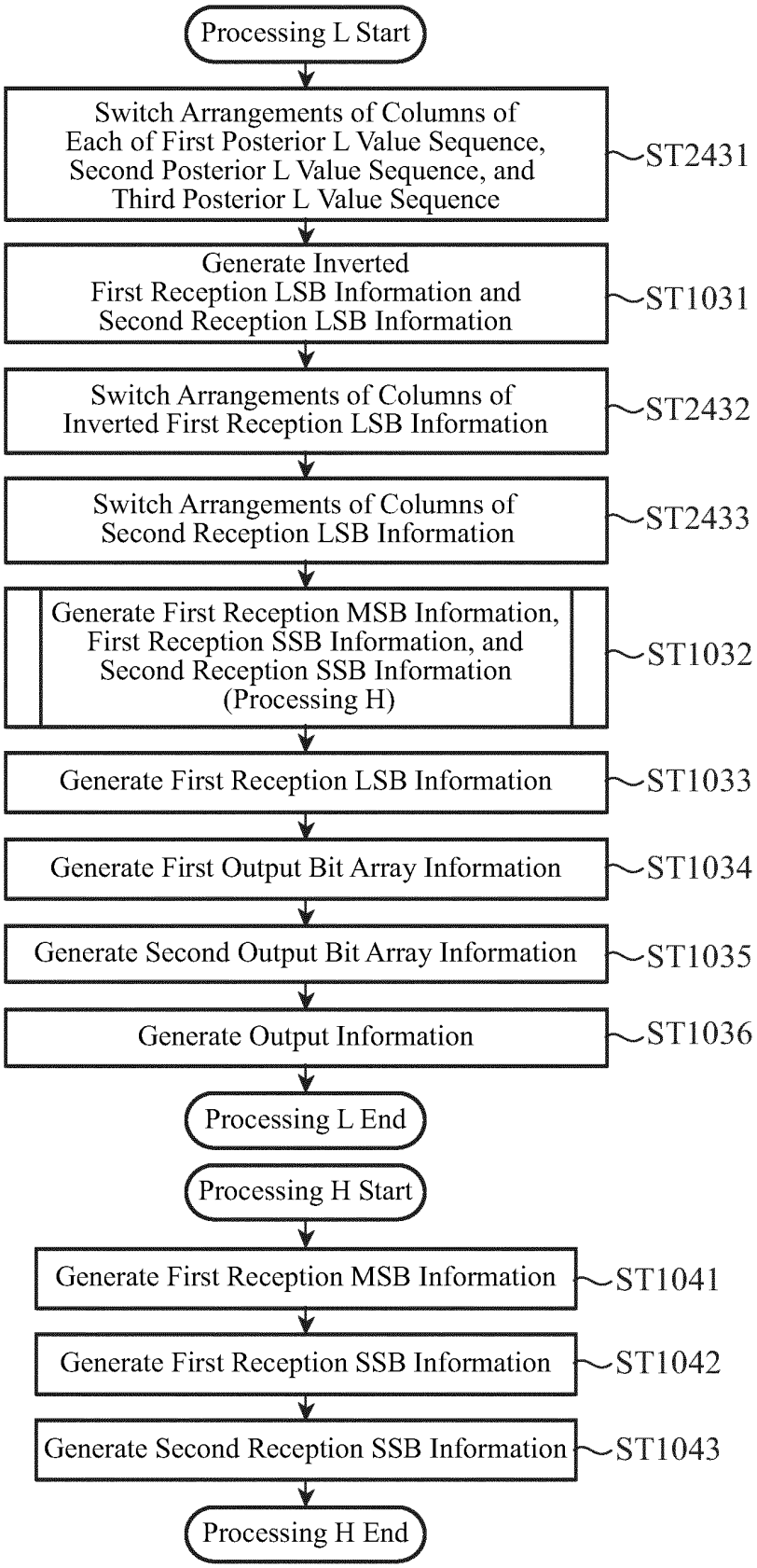

Processing L Start
Switch Arrangements of Columns of Each of First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence
ST2431
Generate Inverted First Reception LSB Information and Second Reception LSB Information
ST1031
Switch Arrangements of Columns of Inverted First Reception LSB Information
ST2432
Switch Arrangements of Columns of Second Reception LSB Information
ST2433
Generate First Reception MSB Information, First Reception SSB Information, and Second Reception SSB Information (Processing H)
ST1032
Generate First Reception LSB Information
ST1033
Generate First Output Bit Array Information
ST1034
Generate Second Output Bit Array Information
ST1035
Generate Output Information
ST1036
Processing L End
Processing H Start
Generate First Reception MSB Information
ST1041
Generate First Reception SSB Information
ST1042
Generate Second Reception SSB Information
ST1043
Processing H End

FIG. 25A

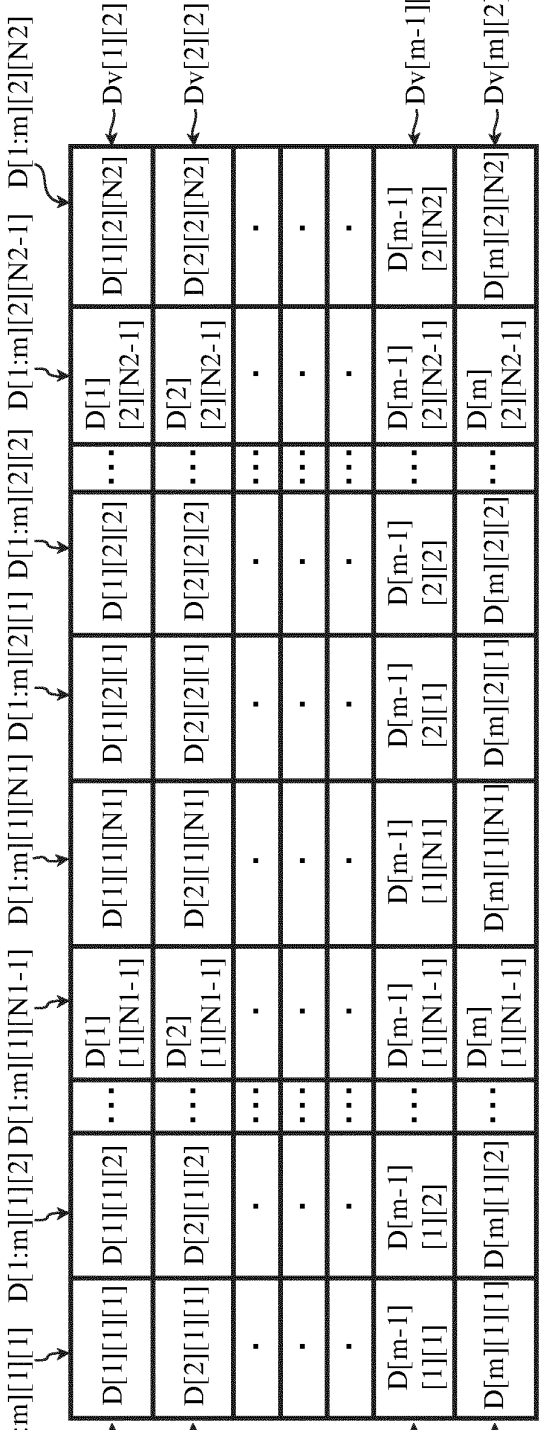
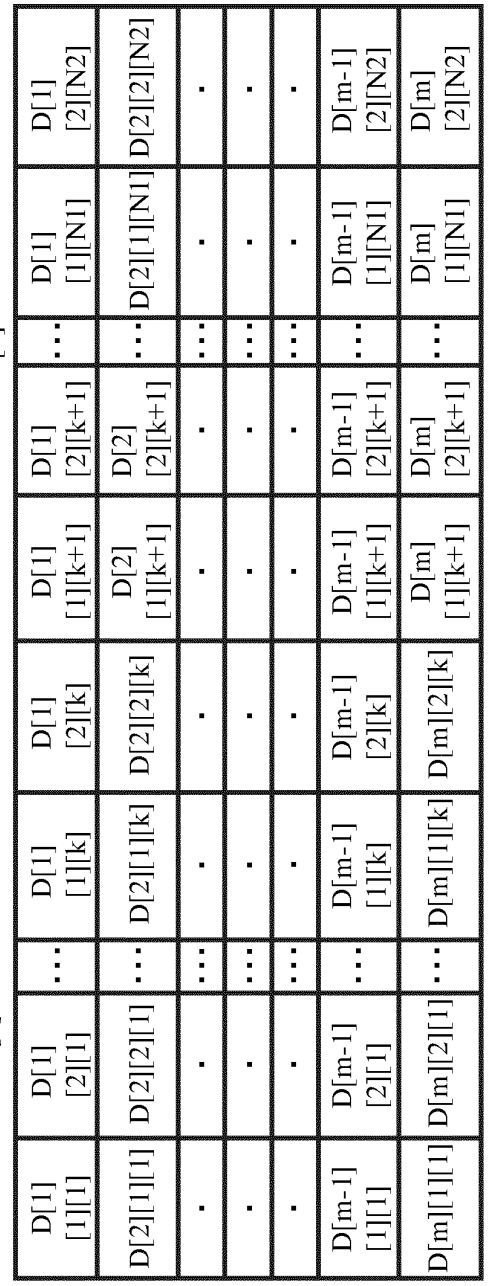


FIG. 25B



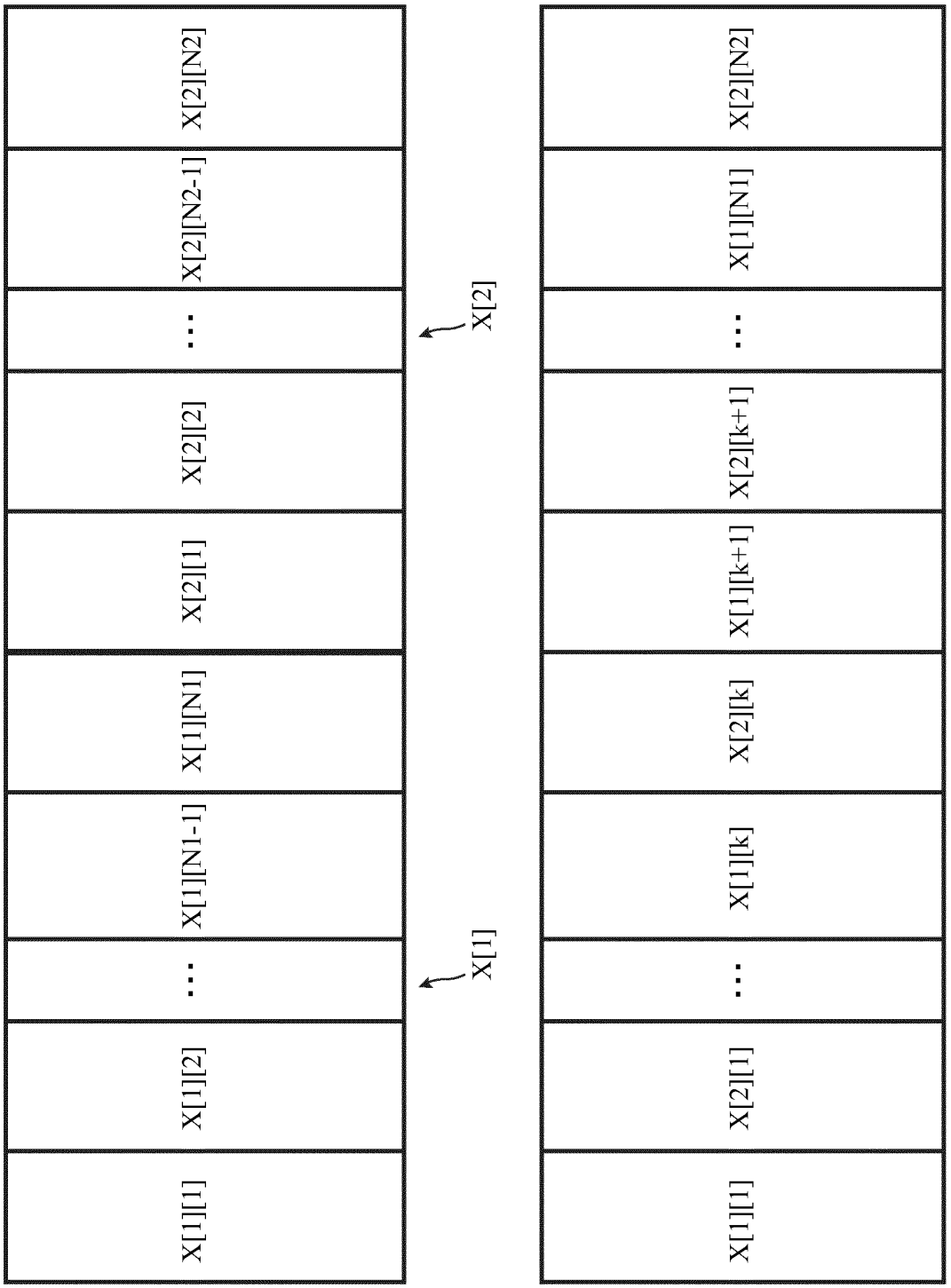


FIG. 26A

FIG. 26B

FIG. 27A

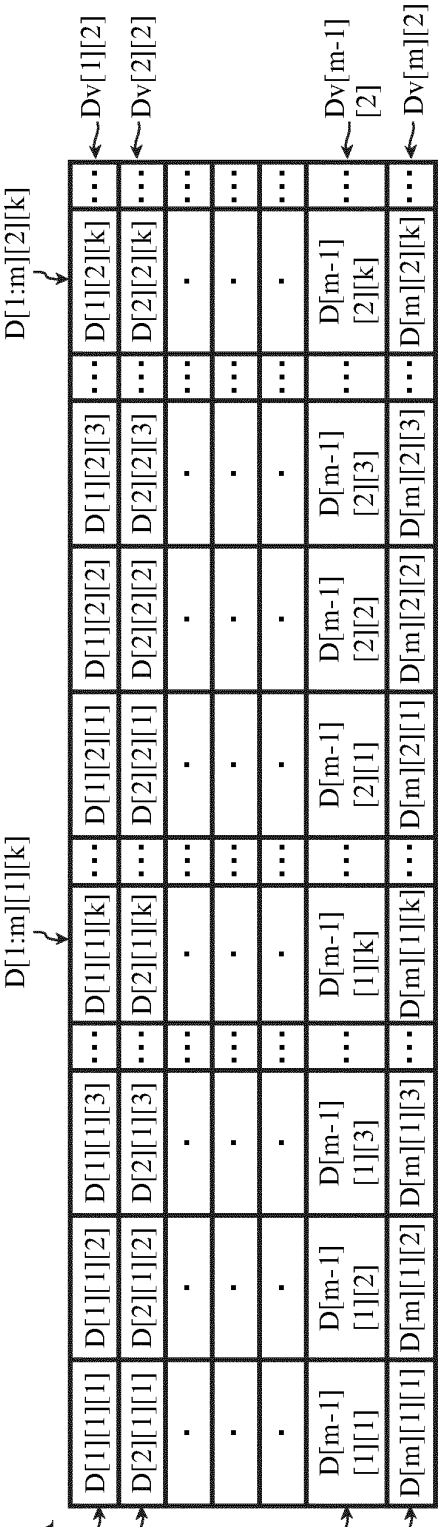


FIG. 27B

FIG. 28

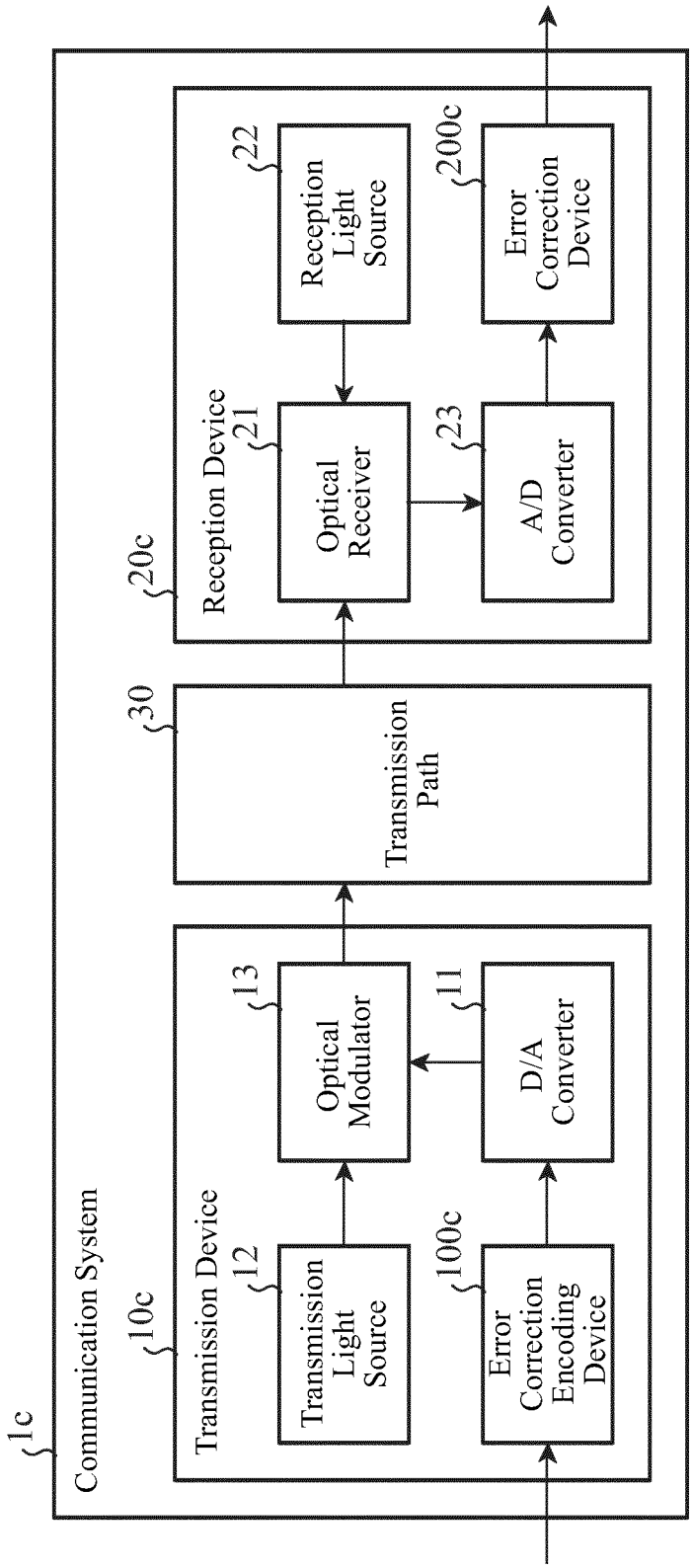

1c
Communication System
10c
Transmission Device
12
Transmission Light Source
13
Optical Modulator
100c
Error Correction Encoding Device
11
D/A Converter
30
Transmission Path
20c
Reception Device
21
Optical Receiver
22
Reception Light Source
23
A/D Converter
200c
Error Correction Device

FIG. 29

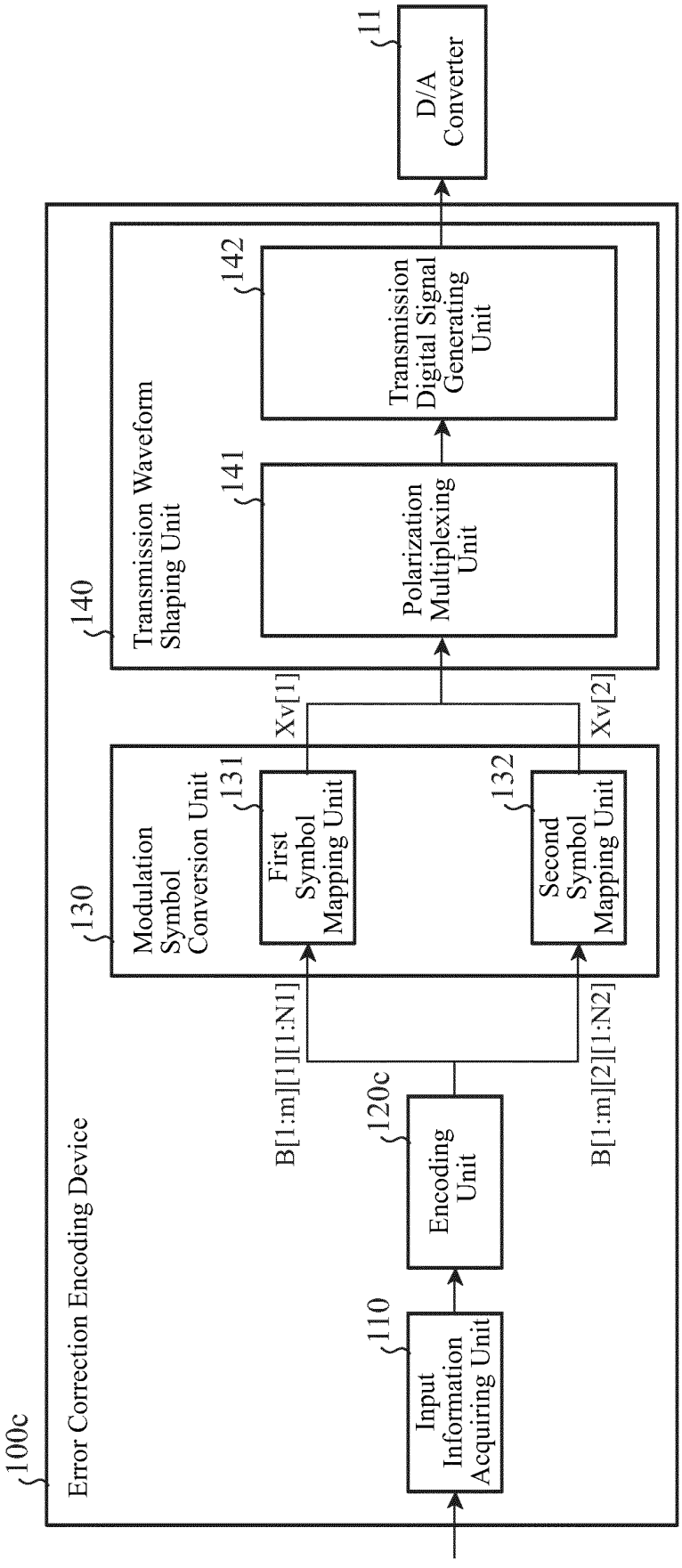

100c
Error Correction Encoding Device
110
Input Information Acquiring Unit
120c
Encoding Unit
B[1:m][1][1:N1]
B[1:m][2][1:N2]
130
Modulation Symbol Conversion Unit
131
First Symbol Mapping Unit
132
Second Symbol Mapping Unit
Xv[1]
Xv[2]
140
Transmission Waveform Shaping Unit
141
Polarization Multiplexing Unit
142
Transmission Digital Signal Generating Unit
11
D/A Converter

FIG. 30

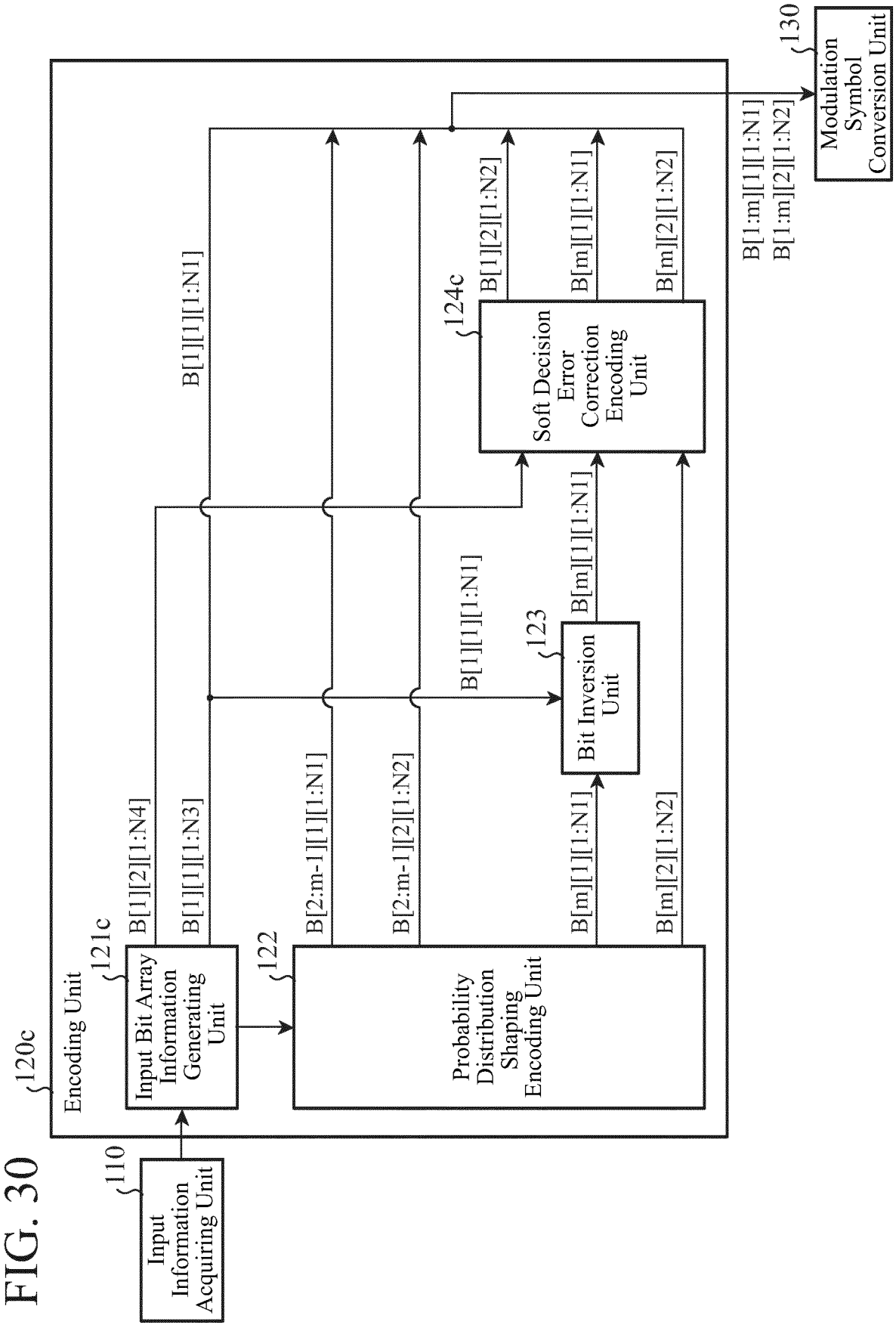

Input Information Acquiring Unit
110
120c
Encoding Unit
Input Bit Array Information Generating Unit
121c
Probability Distribution Shaping Encoding Unit
122
Bit Inversion Unit
123
Soft Decision Error Correction Encoding Unit
124c
Modulation Symbol Conversion Unit
130
B[1][1][1:N1]
B[1][1][1:N3]
B[1][2][1:N4]
B[2:m-1][1][1:N1]
B[2:m-1][2][1:N2]
B[1][1][1:N1]
B[m][1][1:N1]
B[m][2][1:N2]
B[1][2][1:N2]
B[m][1][1:N1]
B[m][2][1:N2]
B[1:m][1][1:N1]
B[1:m][2][1:N2]

FIG. 31A

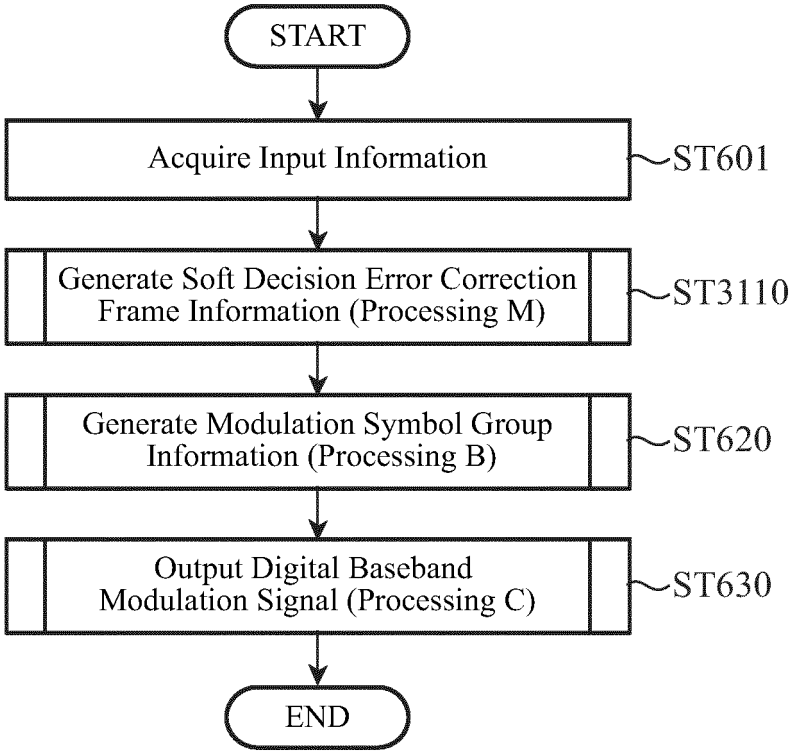

START
Acquire Input Information
ST601
Generate Soft Decision Error Correction Frame Information (Processing M)
ST3110
Generate Modulation Symbol Group Information (Processing B)
ST620
Output Digital Baseband Modulation Signal (Processing C)
ST630
END

FIG. 31B

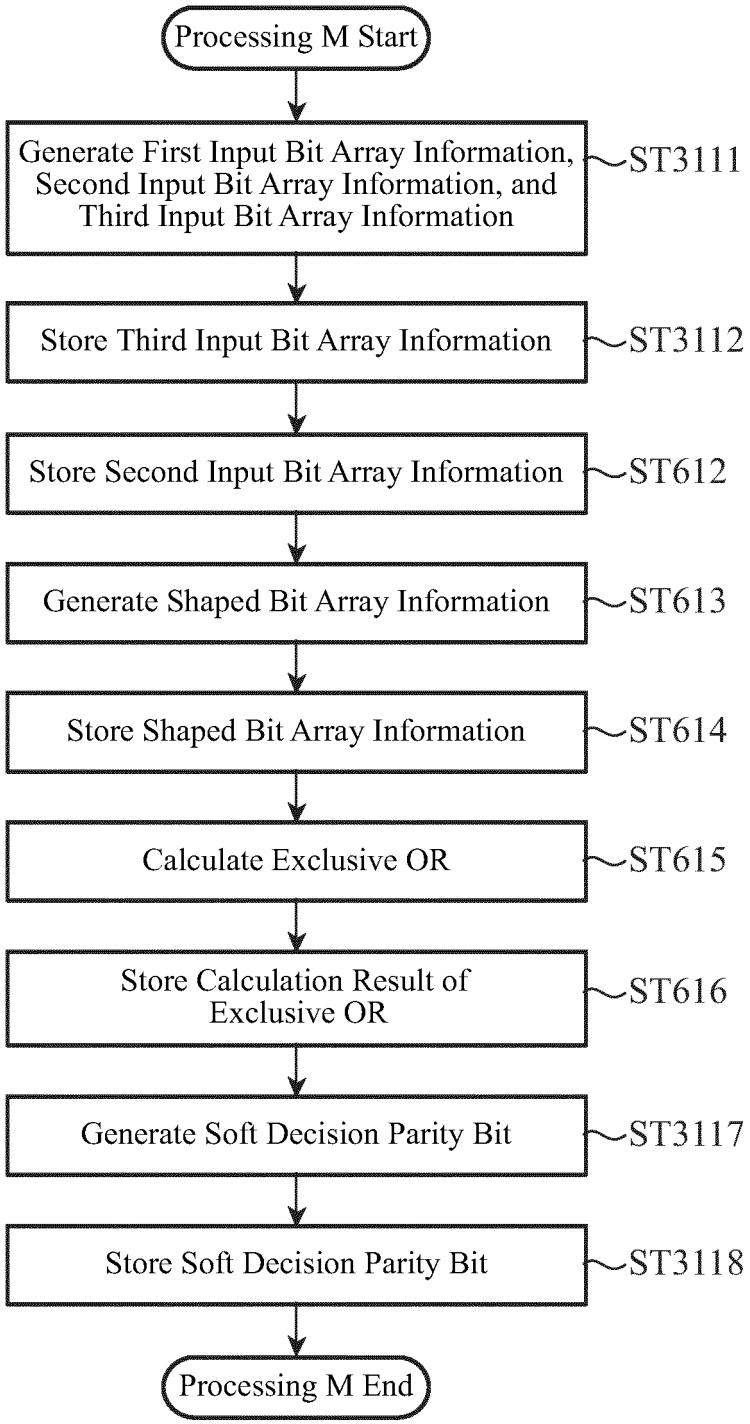
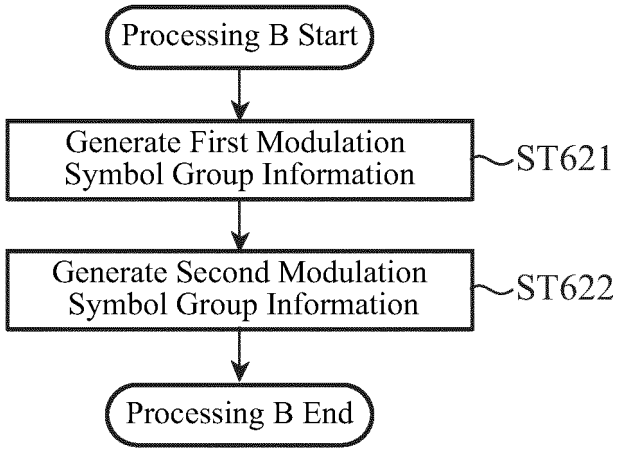

Processing M Start
Generate First Input Bit Array Information, Second Input Bit Array Information, and Third Input Bit Array Information
ST3111
Store Third Input Bit Array Information
ST3112
Store Second Input Bit Array Information
ST612
Generate Shaped Bit Array Information
ST613
Store Shaped Bit Array Information
ST614
Calculate Exclusive OR
ST615
Store Calculation Result of Exclusive OR
ST616
Generate Soft Decision Parity Bit
ST3117
Store Soft Decision Parity Bit
ST3118
Processing M End

FIG. 31C


Processing B Start
Generate First Modulation Symbol Group Information
ST621
Generate Second Modulation Symbol Group Information
ST622
Processing B End

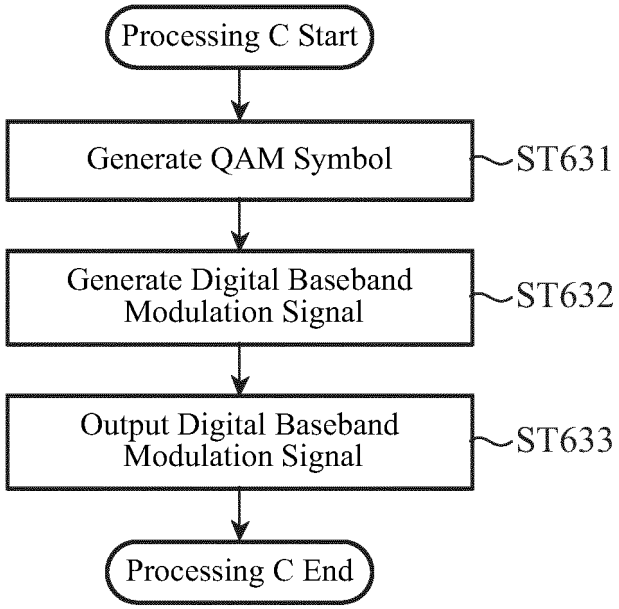

Processing C Start
Generate QAM Symbol
ST631
Generate Digital Baseband Modulation Signal
ST632
Output Digital Baseband Modulation Signal
ST633
Processing C End

FIG. 32

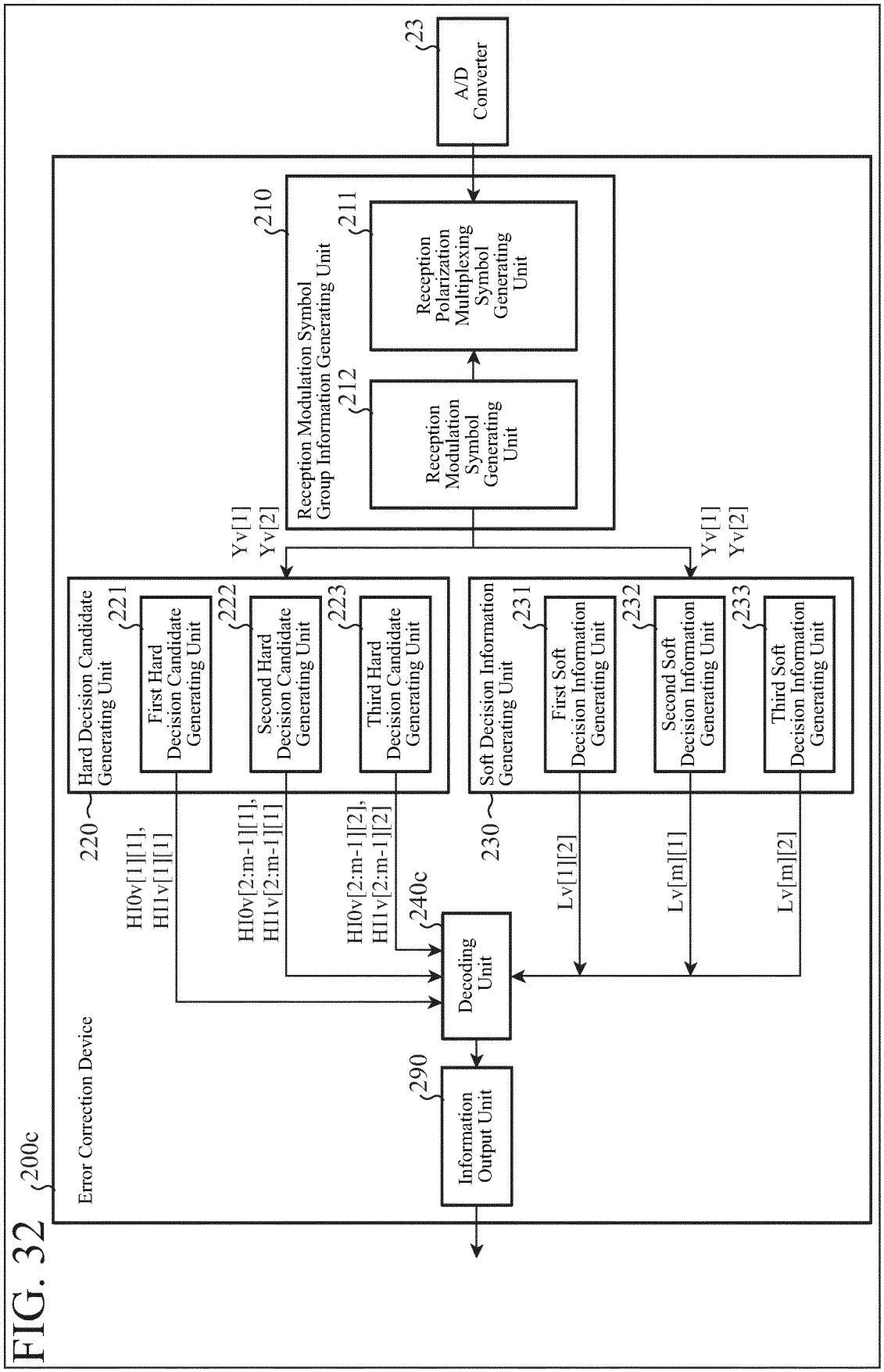

200c
Error Correction Device
23
A/D Converter
210
Reception Modulation Symbol Group Information Generating Unit
211
Reception Polarization Multiplexing Symbol Generating Unit
212
Reception Modulation Symbol Generating Unit
Yv[1]
Yv[2]
220
Hard Decision Candidate Generating Unit
221
First Hard Decision Candidate Generating Unit
222
Second Hard Decision Candidate Generating Unit
223
Third Hard Decision Candidate Generating Unit
HI0v[1][1], HI1v[1][1]
HI0v[2:m-1][1], HI1v[2:m-1][1]
HI0v[2:m-1][2], HI1v[2:m-1][2]
230
Soft Decision Information Generating Unit
231
First Soft Decision Information Generating Unit
232
Second Soft Decision Information Generating Unit
233
Third Soft Decision Information Generating Unit
Lv[1][2]
Lv[m][1]
Lv[m][2]
240c
Decoding Unit
290
Information Output Unit

FIG. 33

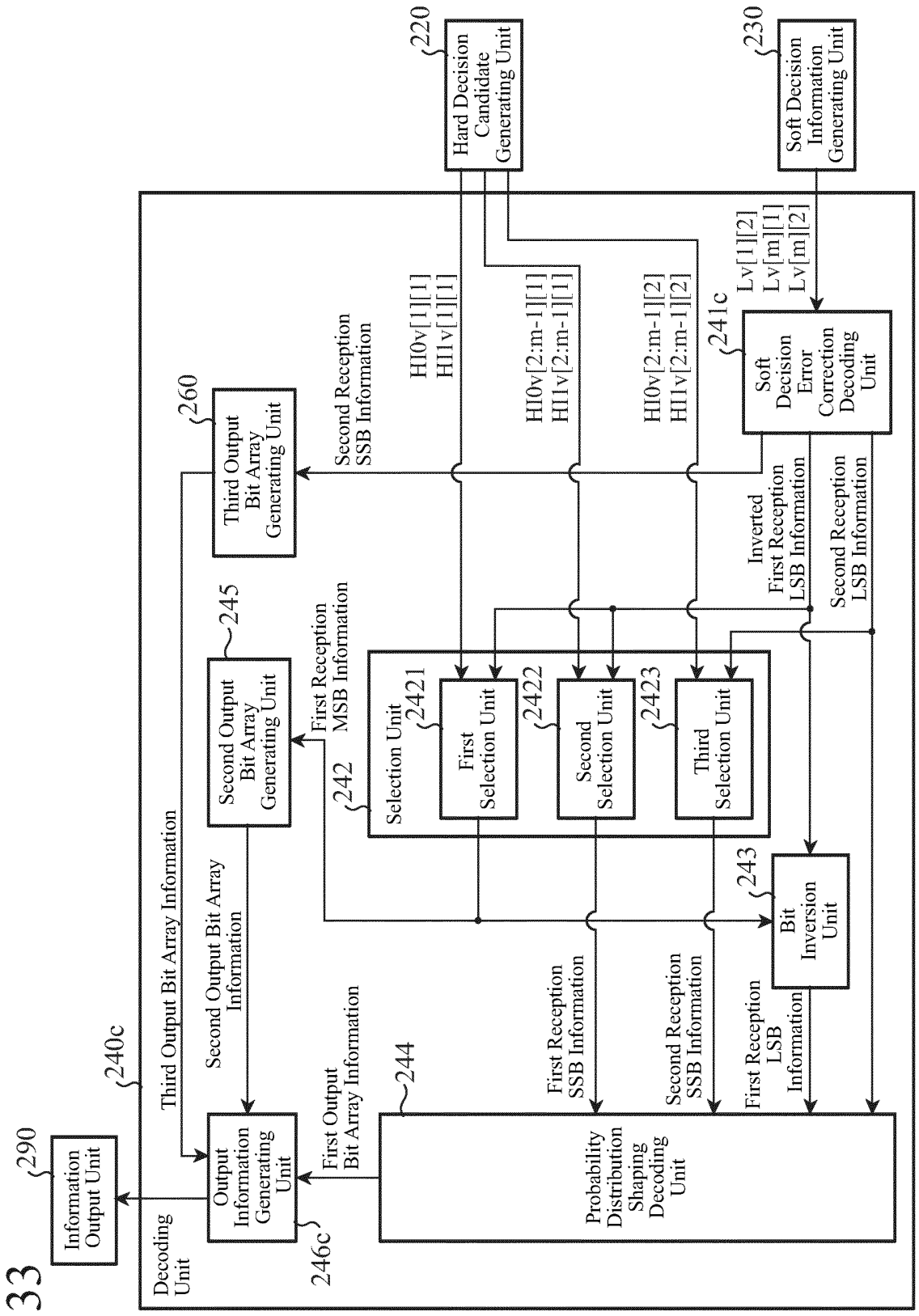

290
Information Output Unit
240c
Decoding Unit
Third Output Bit Array Information
Second Output Bit Array Information
First Output Bit Array Information
Output Information Generating Unit
246c
244
Probability Distribution Shaping Decoding Unit
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information
243
Bit Inversion Unit
Inverted First Reception LSB Information
Second Reception LSB Information
242
Selection Unit
2421
First Selection Unit
2422
Second Selection Unit
2423
Third Selection Unit
First Reception MSB Information
245
Second Output Bit Array Generating Unit
260
Third Output Bit Array Generating Unit
Second Reception SSB Information
HI0v[1][1]
HI1v[1][1]
HI0v[2:m-1][1]
HI1v[2:m-1][1]
HI0v[2:m-1][2]
HI1v[2:m-1][2]
220
Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
Lv[1][2]
Lv[m][1]
Lv[m][2]
241c
Soft Decision Error Correction Decoding Unit

FIG. 34A

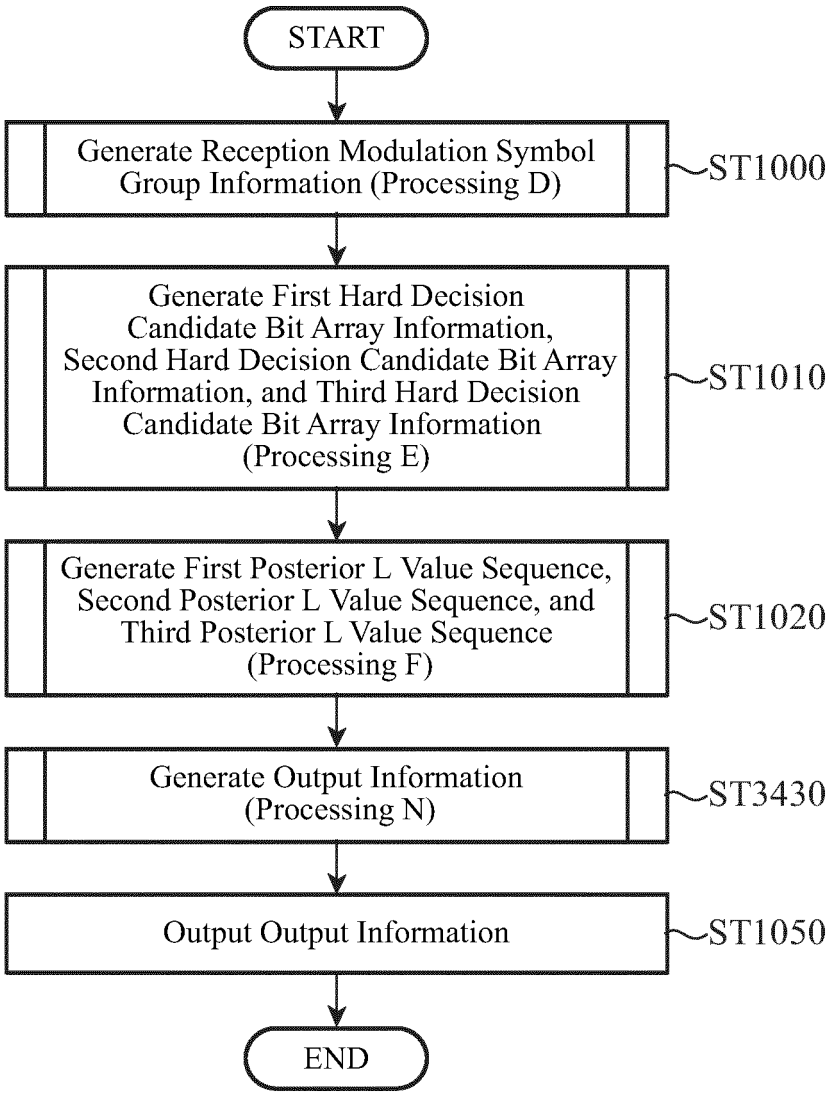

START
Generate Reception Modulation Symbol Group Information (Processing D)
ST1000
Generate First Hard Decision Candidate Bit Array Information, Second Hard Decision Candidate Bit Array Information, and Third Hard Decision Candidate Bit Array Information (Processing E)
ST1010
Generate First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence (Processing F)
ST1020
Generate Output Information (Processing N)
ST3430
Output Output Information
ST1050
END

FIG. 34B

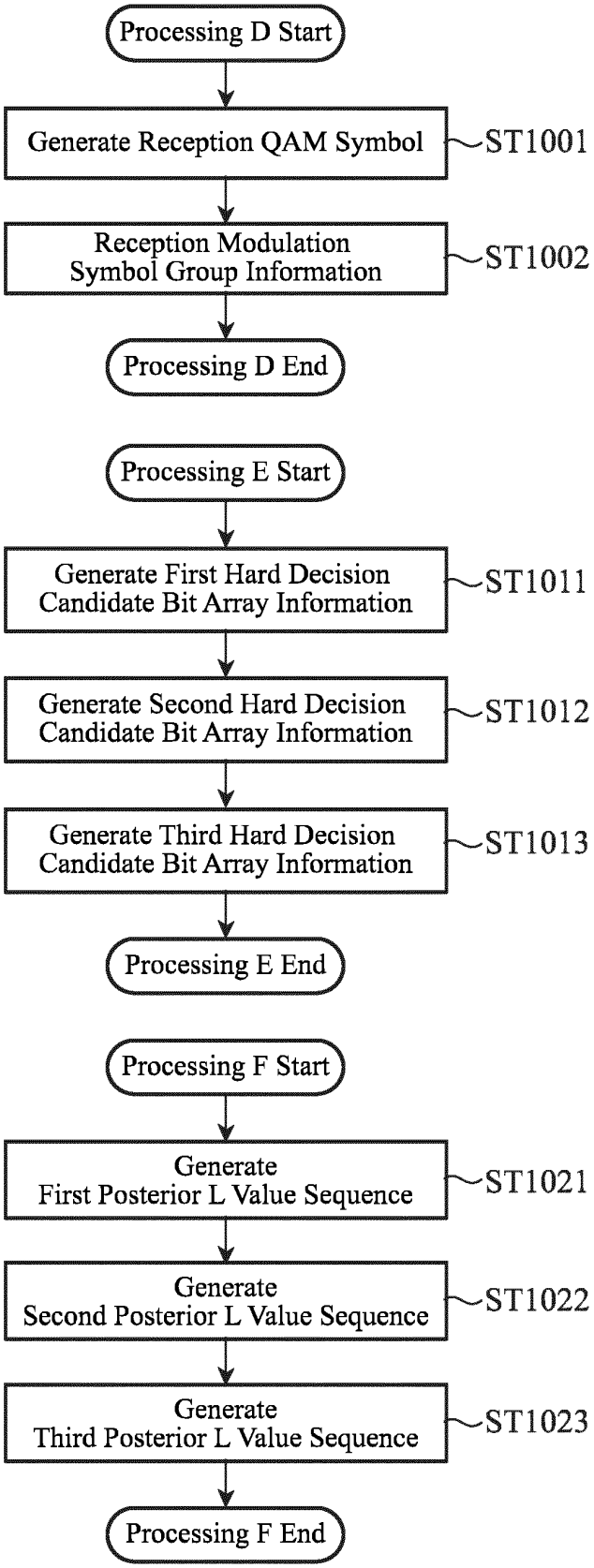

Processing D Start
Generate Reception QAM Symbol
ST1001
Reception Modulation Symbol Group Information
ST1002
Processing D End
Processing E Start
Generate First Hard Decision Candidate Bit Array Information
ST1011
Generate Second Hard Decision Candidate Bit Array Information
ST1012
Generate Third Hard Decision Candidate Bit Array Information
ST1013
Processing E End
Processing F Start
Generate First Posterior L Value Sequence
ST1021
Generate Second Posterior L Value Sequence
ST1022
Generate Third Posterior L Value Sequence
ST1023
Processing F End

FIG. 34C

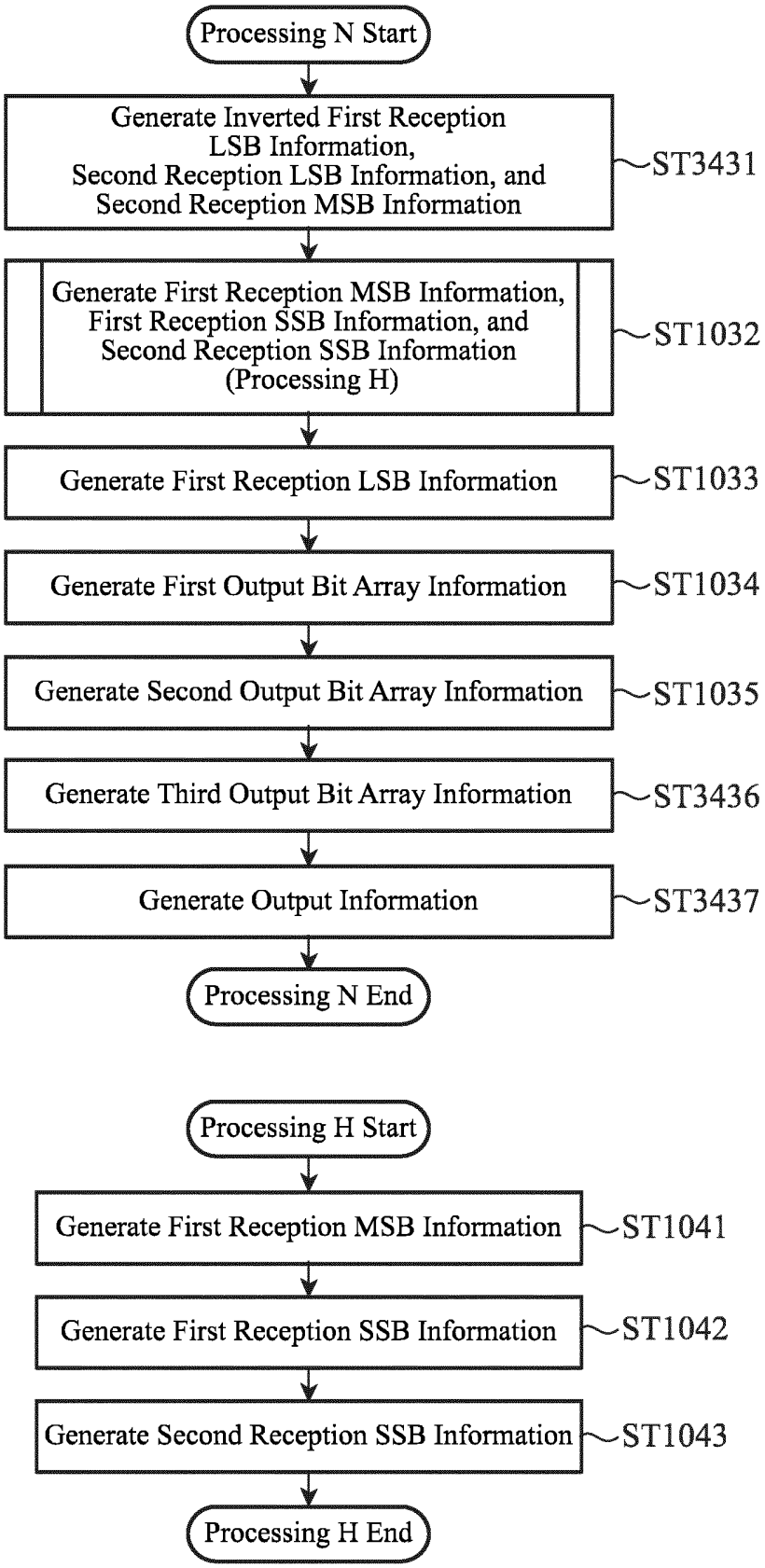

Processing N Start
Generate Inverted First Reception LSB Information, Second Reception LSB Information, and Second Reception MSB Information
ST3431
Generate First Reception MSB Information, First Reception SSB Information, and Second Reception SSB Information (Processing H)
ST1032
Generate First Reception LSB Information
ST1033
Generate First Output Bit Array Information
ST1034
Generate Second Output Bit Array Information
ST1035
Generate Third Output Bit Array Information
ST3436
Generate Output Information
ST3437
Processing N End
Processing H Start
Generate First Reception MSB Information
ST1041
Generate First Reception SSB Information
ST1042
Generate Second Reception SSB Information
ST1043
Processing H End

FIG. 35

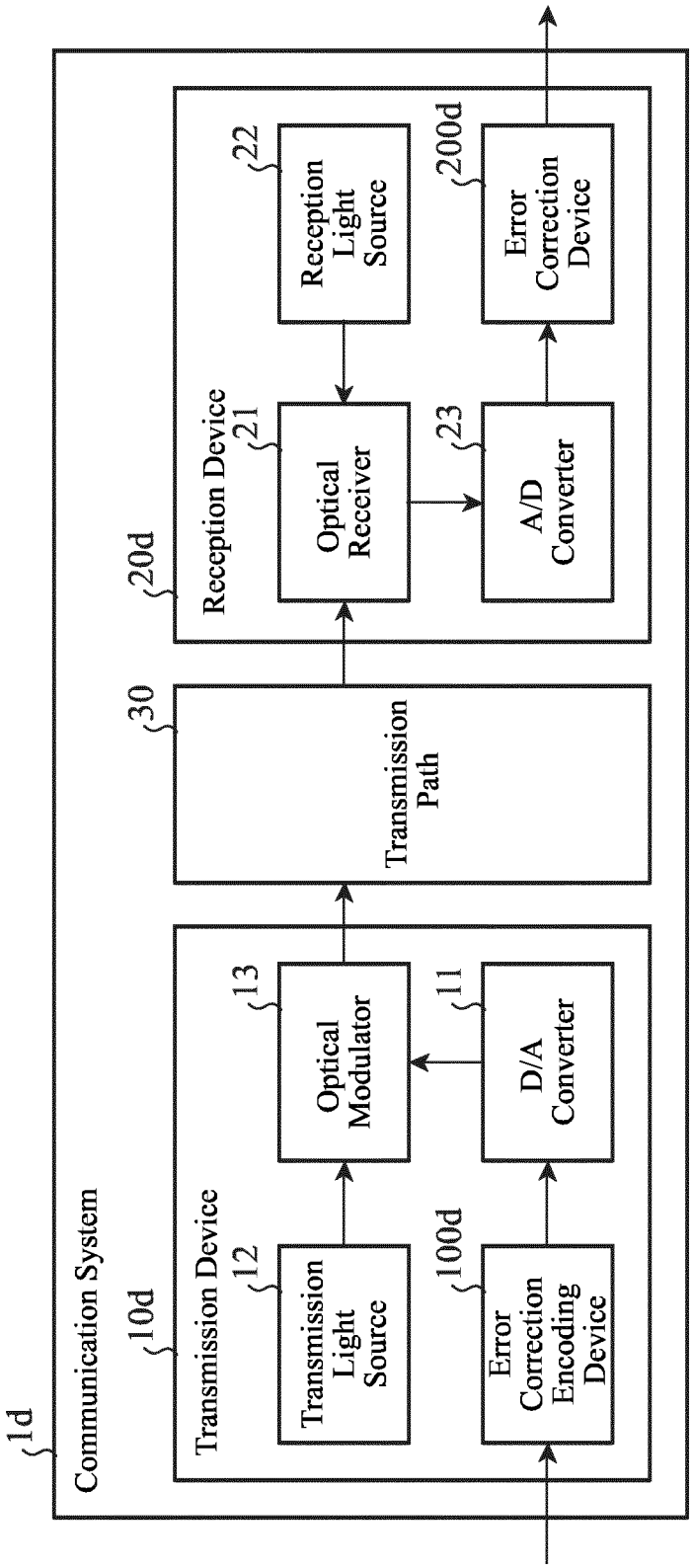

1d
Communication System
10d
Transmission Device
12
Transmission Light Source
100d
Error Correction Encoding Device
13
Optical Modulator
11
D/A Converter
30
Transmission Path
20d
Reception Device
21
Optical Receiver
23
A/D Converter
22
Reception Light Source
200d
Error Correction Device

FIG. 36

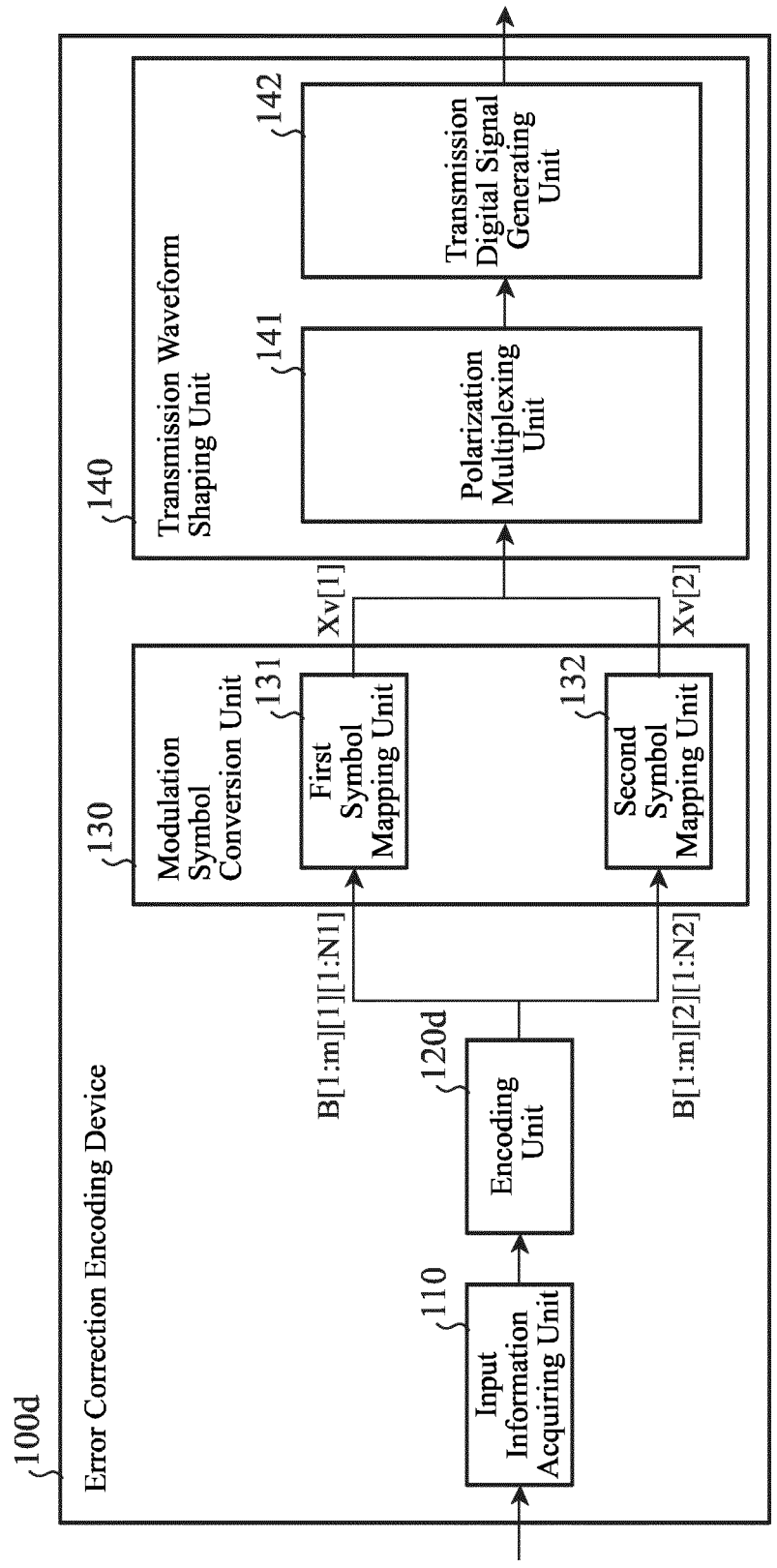

100d
Error Correction Encoding Device
110
Input Information Acquiring Unit
120d
Encoding Unit
B[1:m][1][1:N1]
B[1:m][2][1:N2]
130
Modulation Symbol Conversion Unit
131
First Symbol Mapping Unit
132
Second Symbol Mapping Unit
Xv[1]
Xv[2]
140
Transmission Waveform Shaping Unit
141
Polarization Multiplexing Unit
142
Transmission Digital Signal Generating Unit

FIG. 37

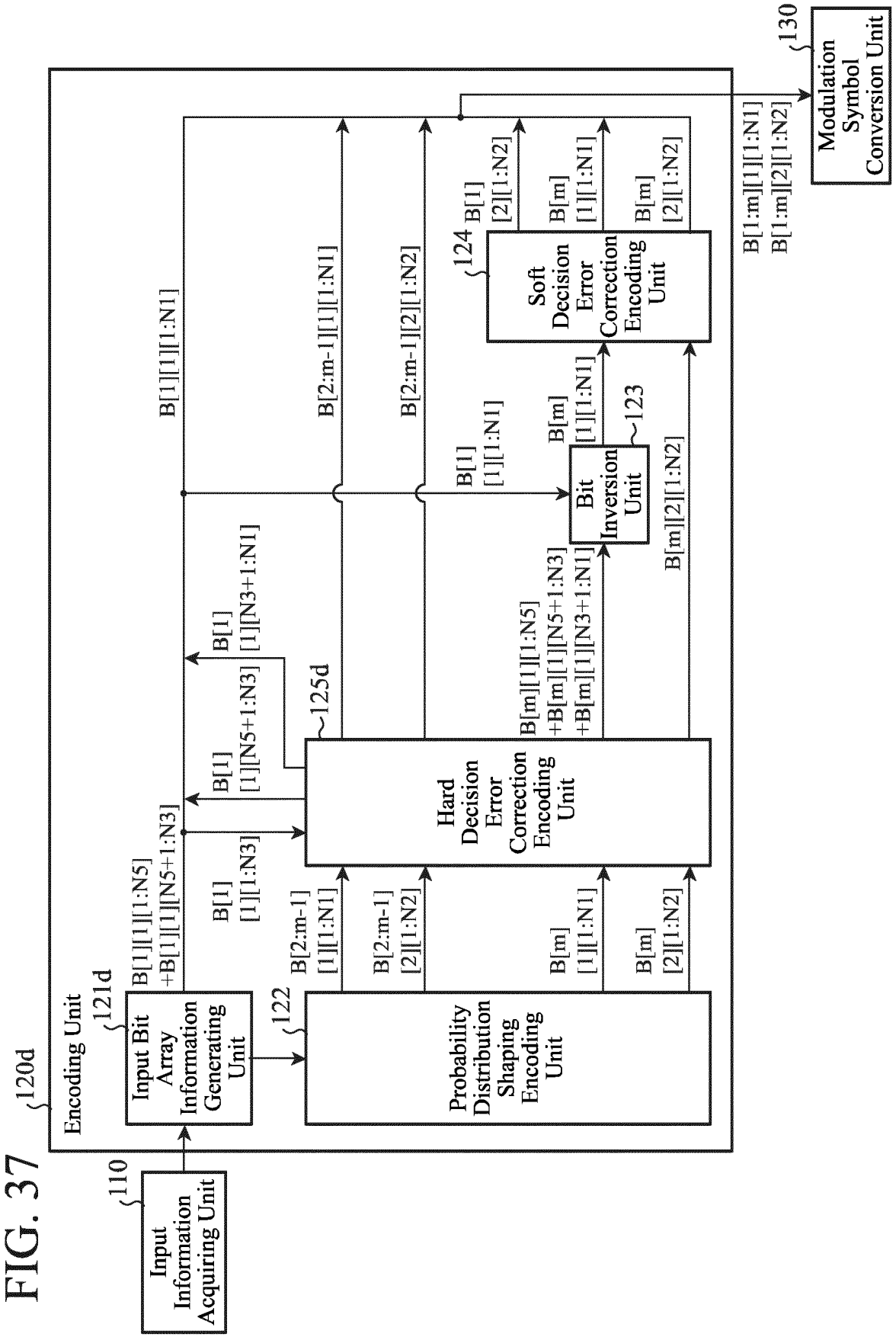

Input Information Acquiring Unit
110
Encoding Unit
120d
Input Bit Array Information Generating Unit
121d
Probability Distribution Shaping Encoding Unit
122
Hard Decision Error Correction Encoding Unit
125d
Bit Inversion Unit
123
Soft Decision Error Correction Encoding Unit
124
Modulation Symbol Conversion Unit
130
B[1][1][1:N5] +B[1][1][N5+1:N3]
B[1] [1][1:N3]
B[1] [1][N5+1:N3]
B[1] [1][N3+1:N1]
B[2:m-1] [1][1:N1]
B[2:m-1] [2][1:N2]
B[m] [1][1:N1]
B[m] [2][1:N2]
B[1][1][1:N1]
B[2:m-1][1][1:N1]
B[2:m-1][2][1:N2]
B[m][1][1:N5] +B[m][1][N5+1:N3] +B[m][1][N3+1:N1]
B[m][2][1:N2]
B[1] [1][1:N1]
B[m] [1][1:N1]
B[1] [2][1:N2]
B[m] [1][1:N1]
B[m] [2][1:N2]
B[1:m][1][1:N1]
B[1:m][2][1:N2]

FIG. 38A

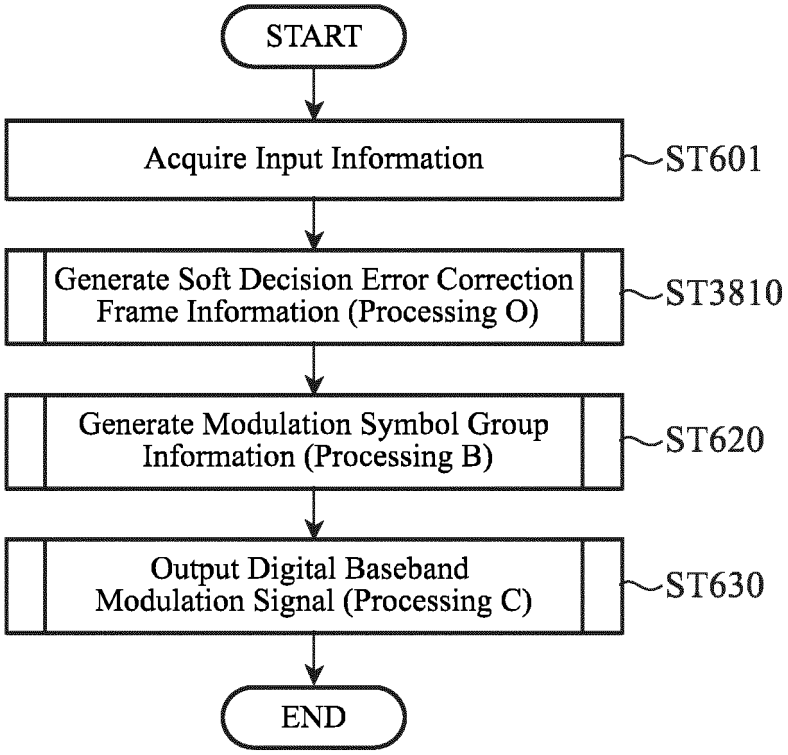

START
Acquire Input Information
ST601
Generate Soft Decision Error Correction Frame Information (Processing O)
ST3810
Generate Modulation Symbol Group Information (Processing B)
ST620
Output Digital Baseband Modulation Signal (Processing C)
ST630
END

FIG. 38B

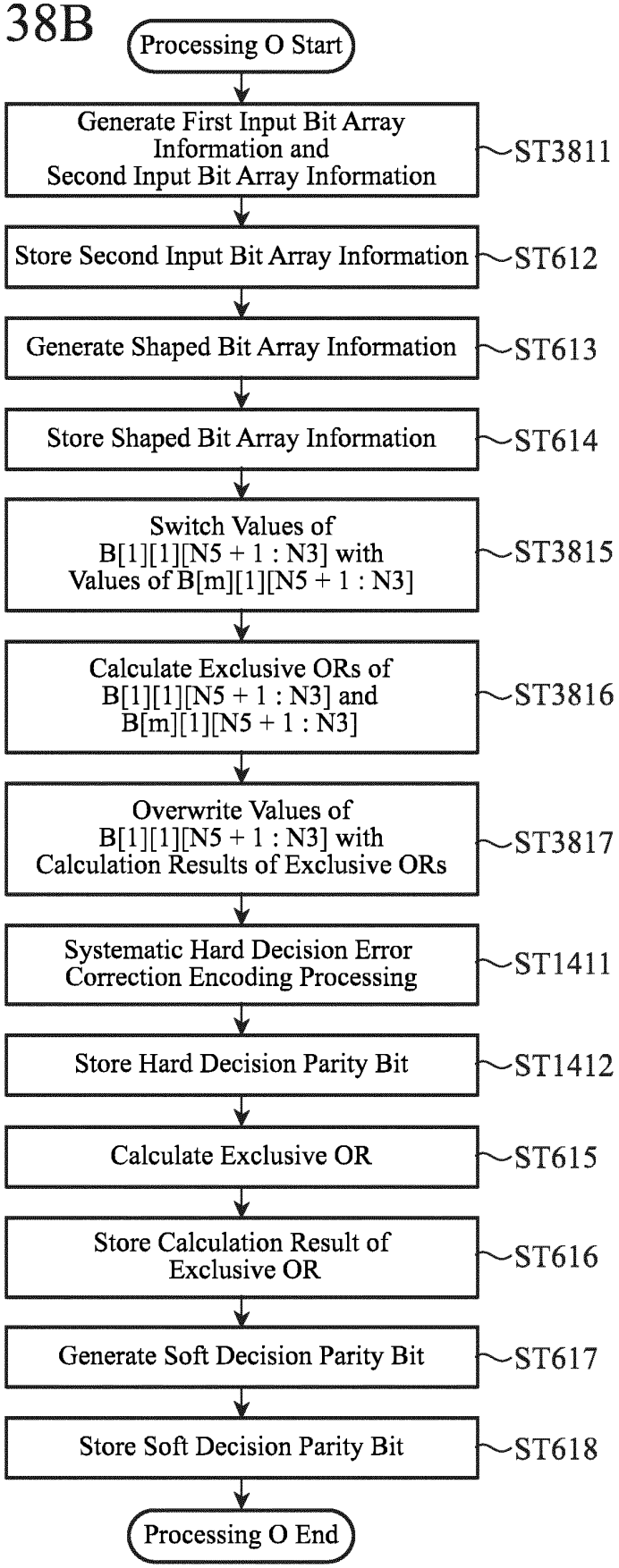
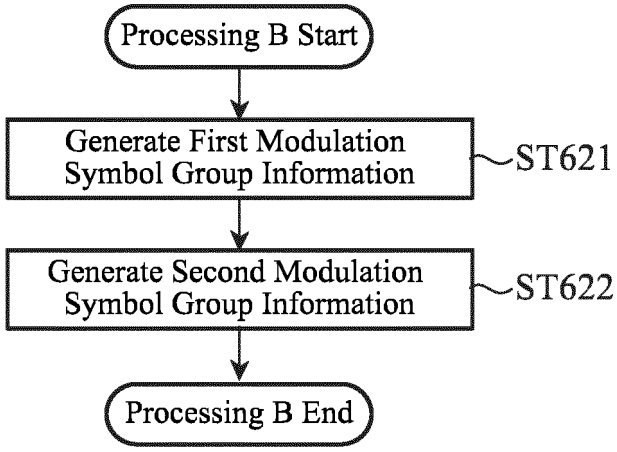

Processing O Start
Generate First Input Bit Array Information and Second Input Bit Array Information
ST3811
Store Second Input Bit Array Information
ST612
Generate Shaped Bit Array Information
ST613
Store Shaped Bit Array Information
ST614
Switch Values of B[1][1][N5 + 1 : N3] with Values of B[m][1][N5 + 1 : N3]
ST3815
Calculate Exclusive ORs of B[1][1][N5 + 1 : N3] and B[m][1][N5 + 1 : N3]
ST3816
Overwrite Values of B[1][1][N5 + 1 : N3] with Calculation Results of Exclusive ORs
ST3817
Systematic Hard Decision Error Correction Encoding Processing
ST1411
Store Hard Decision Parity Bit
ST1412
Calculate Exclusive OR
ST615
Store Calculation Result of Exclusive OR
ST616
Generate Soft Decision Parity Bit
ST617
Store Soft Decision Parity Bit
ST618
Processing O End

FIG. 38C


Processing B Start
Generate First Modulation Symbol Group Information
ST621
Generate Second Modulation Symbol Group Information
ST622
Processing B End

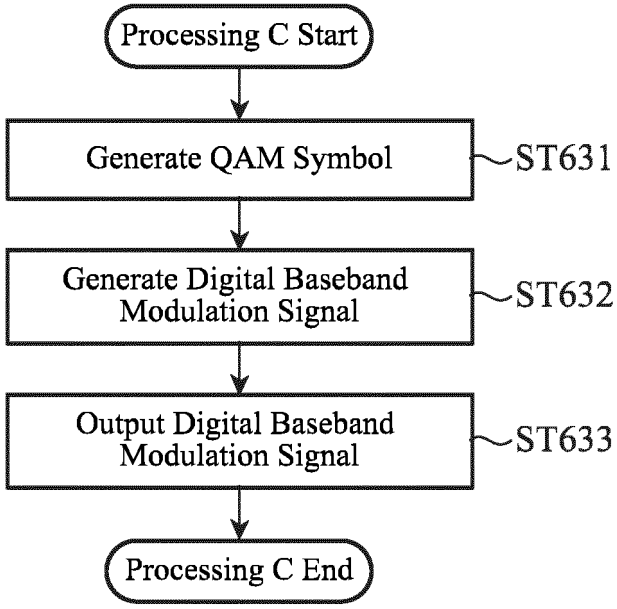

Processing C Start
Generate QAM Symbol
ST631
Generate Digital Baseband Modulation Signal
ST632
Output Digital Baseband Modulation Signal
ST633
Processing C End

FIG. 39

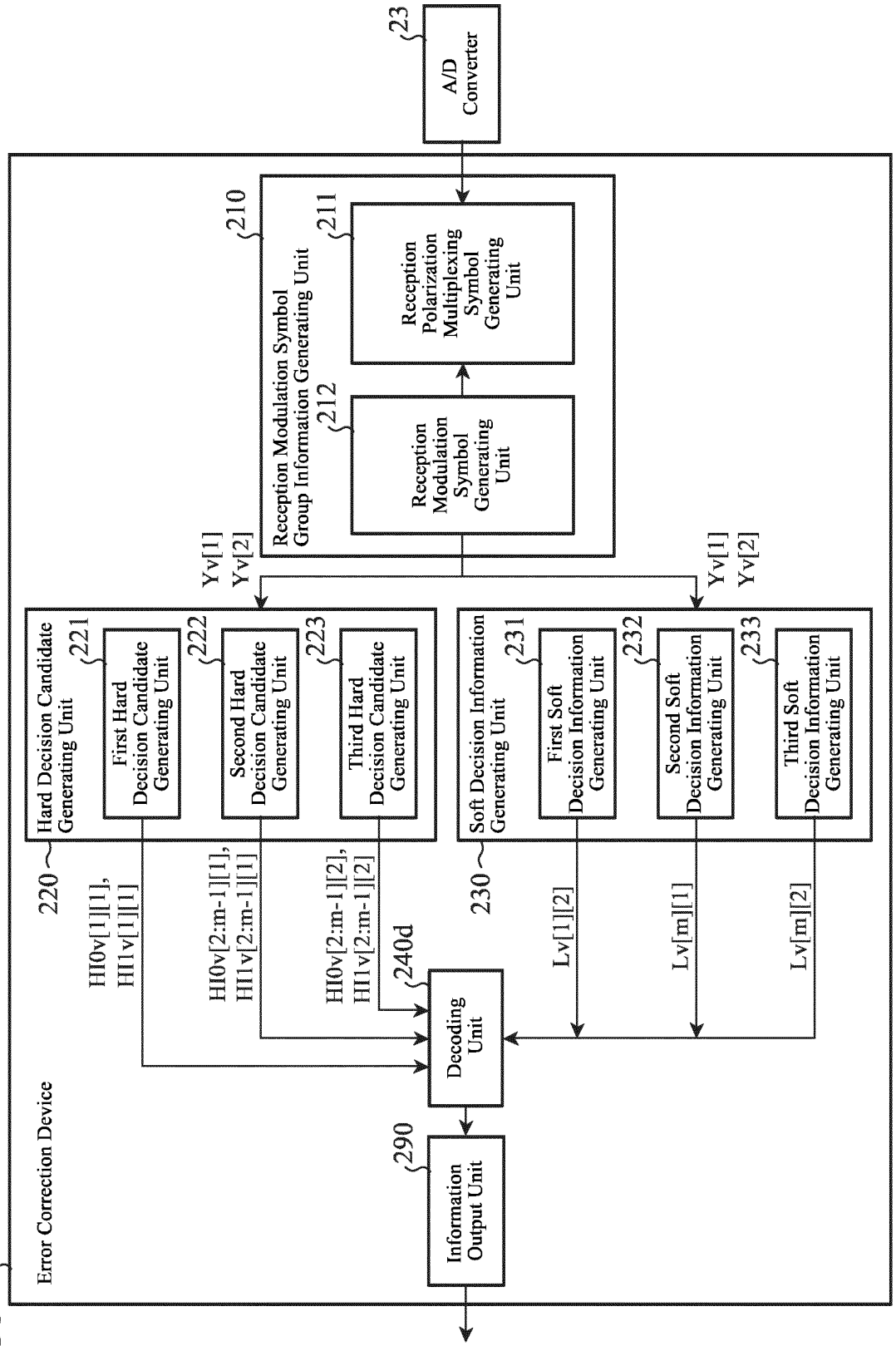

200d
Error Correction Device
23
A/D Converter
210
Reception Modulation Symbol Group Information Generating Unit
211
Reception Polarization Multiplexing Symbol Generating Unit
212
Reception Modulation Symbol Generating Unit
Yv[1]
Yv[2]
220
Hard Decision Candidate Generating Unit
221
First Hard Decision Candidate Generating Unit
222
Second Hard Decision Candidate Generating Unit
223
Third Hard Decision Candidate Generating Unit
HI0v[1][1], HI1v[1][1]
HI0v[2:m-1][1], HI1v[2:m-1][1]
HI0v[2:m-1][2], HI1v[2:m-1][2]
230
Soft Decision Information Generating Unit
231
First Soft Decision Information Generating Unit
232
Second Soft Decision Information Generating Unit
233
Third Soft Decision Information Generating Unit
Lv[1][2]
Lv[m][1]
Lv[m][2]
240d
Decoding Unit
290
Information Output Unit

FIG. 40

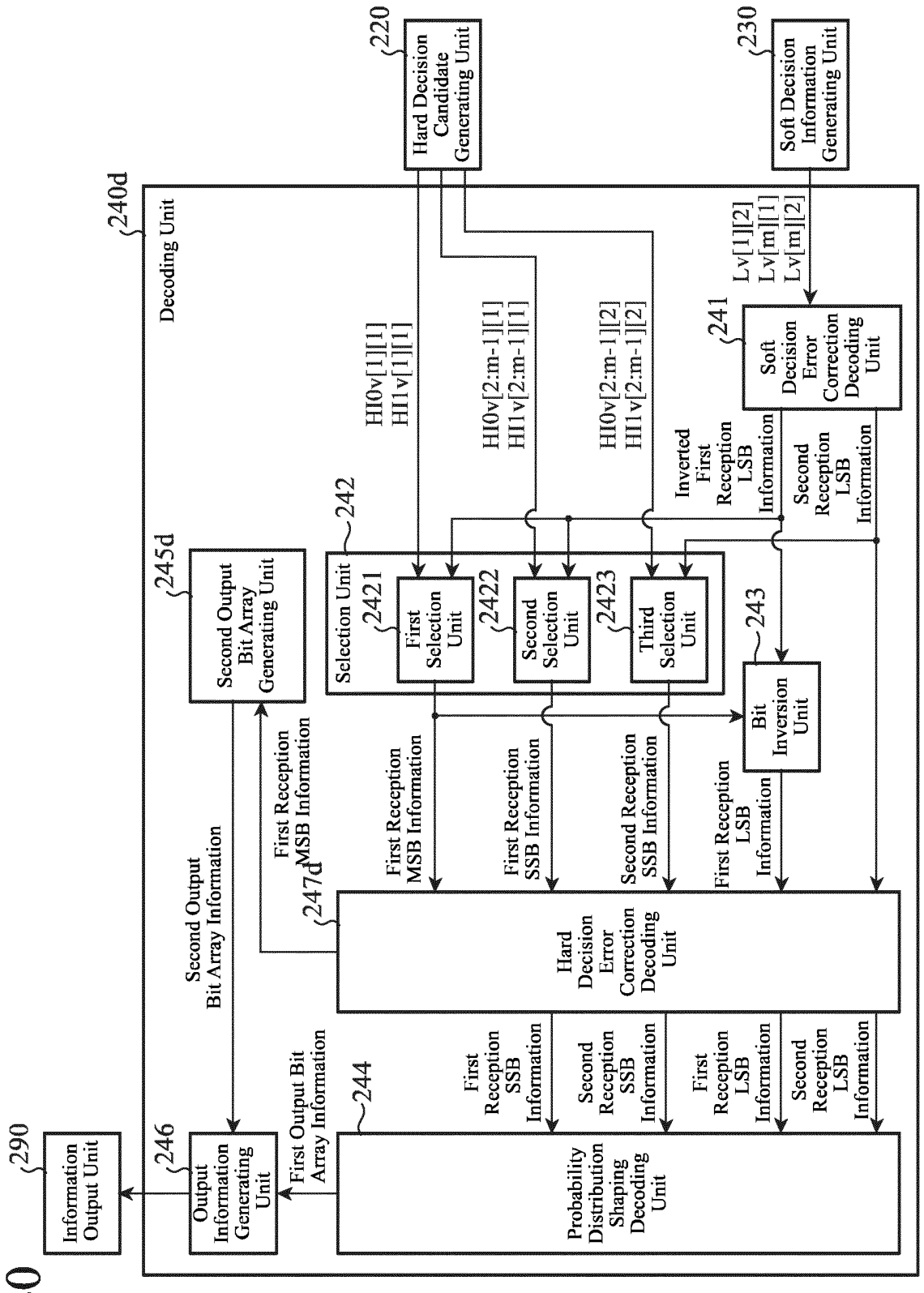

290
Information Output Unit
246
Output Information Generating Unit
240d
Decoding Unit
220
Hard Decision Candidate Generating Unit
230
Soft Decision Information Generating Unit
245d
Second Output Bit Array Generating Unit
242
Selection Unit
2421
First Selection Unit
2422
Second Selection Unit
2423
Third Selection Unit
241
Soft Decision Error Correction Decoding Unit
243
Bit Inversion Unit
247d
Hard Decision Error Correction Decoding Unit
244
Probability Distribution Shaping Decoding Unit
HI0v[1][1]
HI1v[1][1]
HI0v[2:m-1][1]
HI1v[2:m-1][1]
HI0v[2:m-1][2]
HI1v[2:m-1][2]
Lv[1][2]
Lv[m][1]
Lv[m][2]
Inverted First Reception LSB Information
Second Reception LSB Information
First Reception MSB Information
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information
Second Output Bit Array Information
First Output Bit Array Information
First Reception MSB Information
First Reception SSB Information
Second Reception SSB Information
First Reception LSB Information
Second Reception LSB Information

FIG. 41A

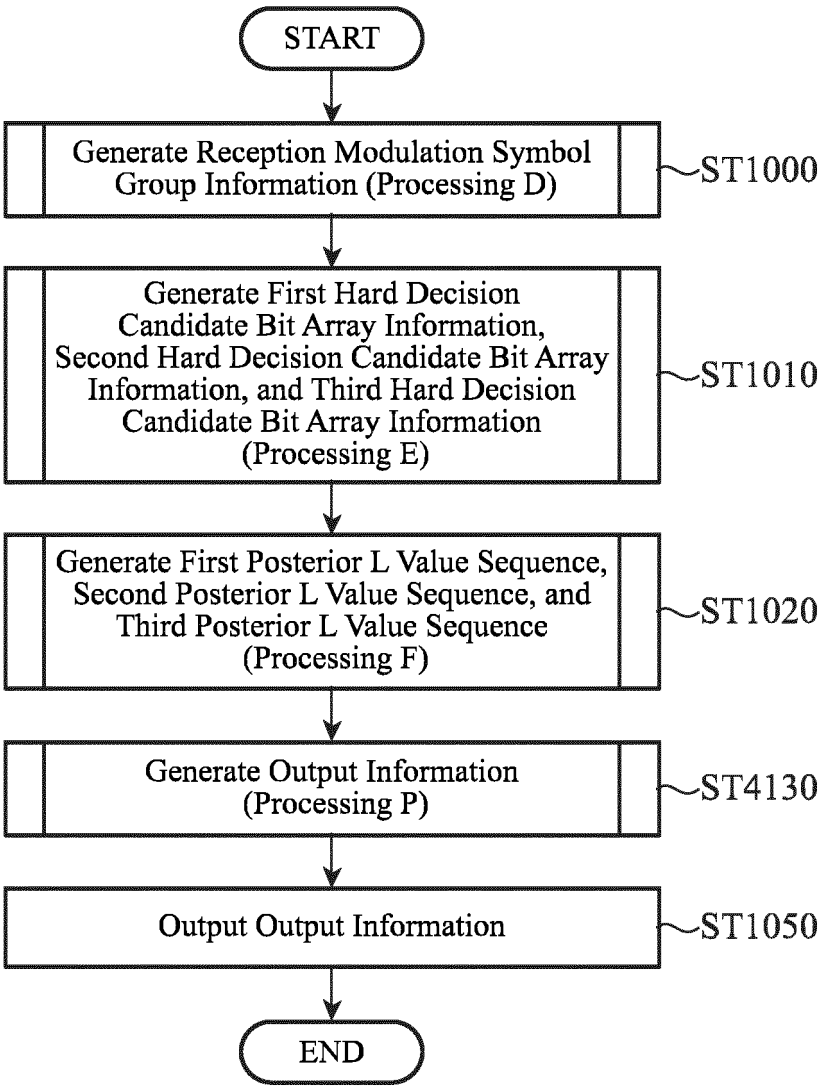

START
Generate Reception Modulation Symbol Group Information (Processing D)
ST1000
Generate First Hard Decision Candidate Bit Array Information, Second Hard Decision Candidate Bit Array Information, and Third Hard Decision Candidate Bit Array Information (Processing E)
ST1010
Generate First Posterior L Value Sequence, Second Posterior L Value Sequence, and Third Posterior L Value Sequence (Processing F)
ST1020
Generate Output Information (Processing P)
ST4130
Output Output Information
ST1050
END

FIG. 41B

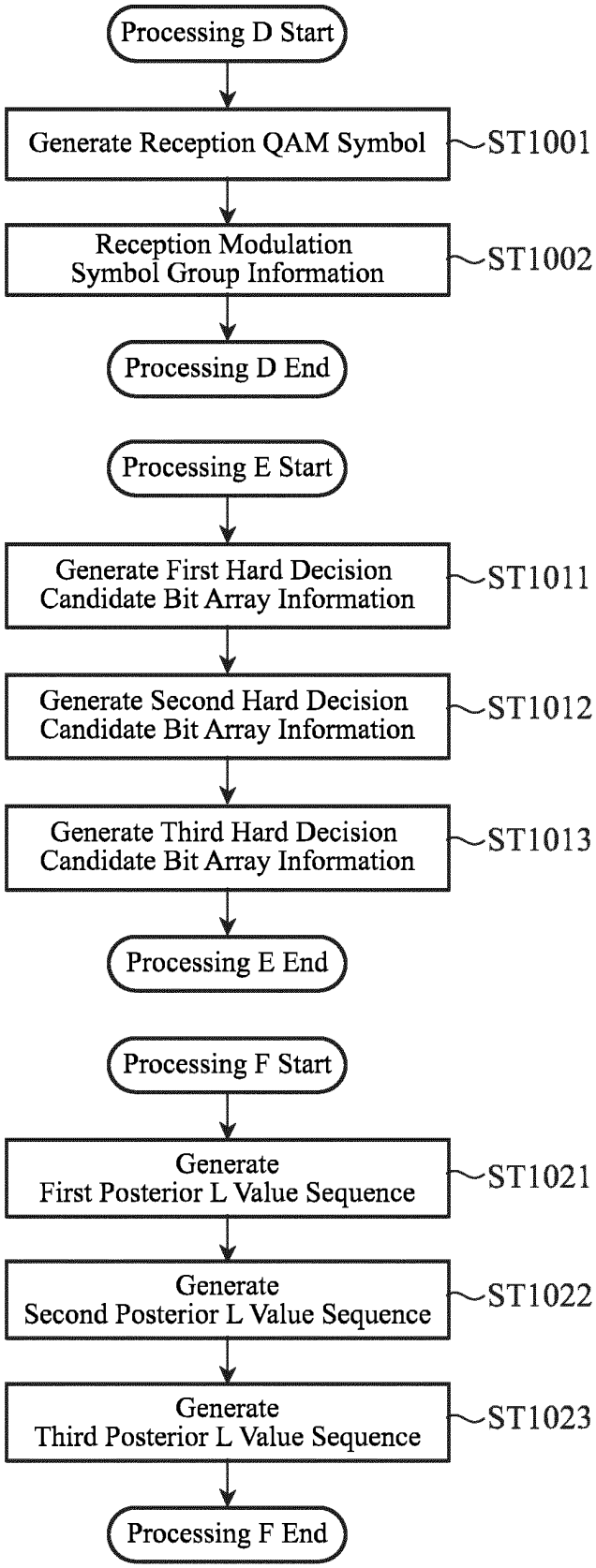
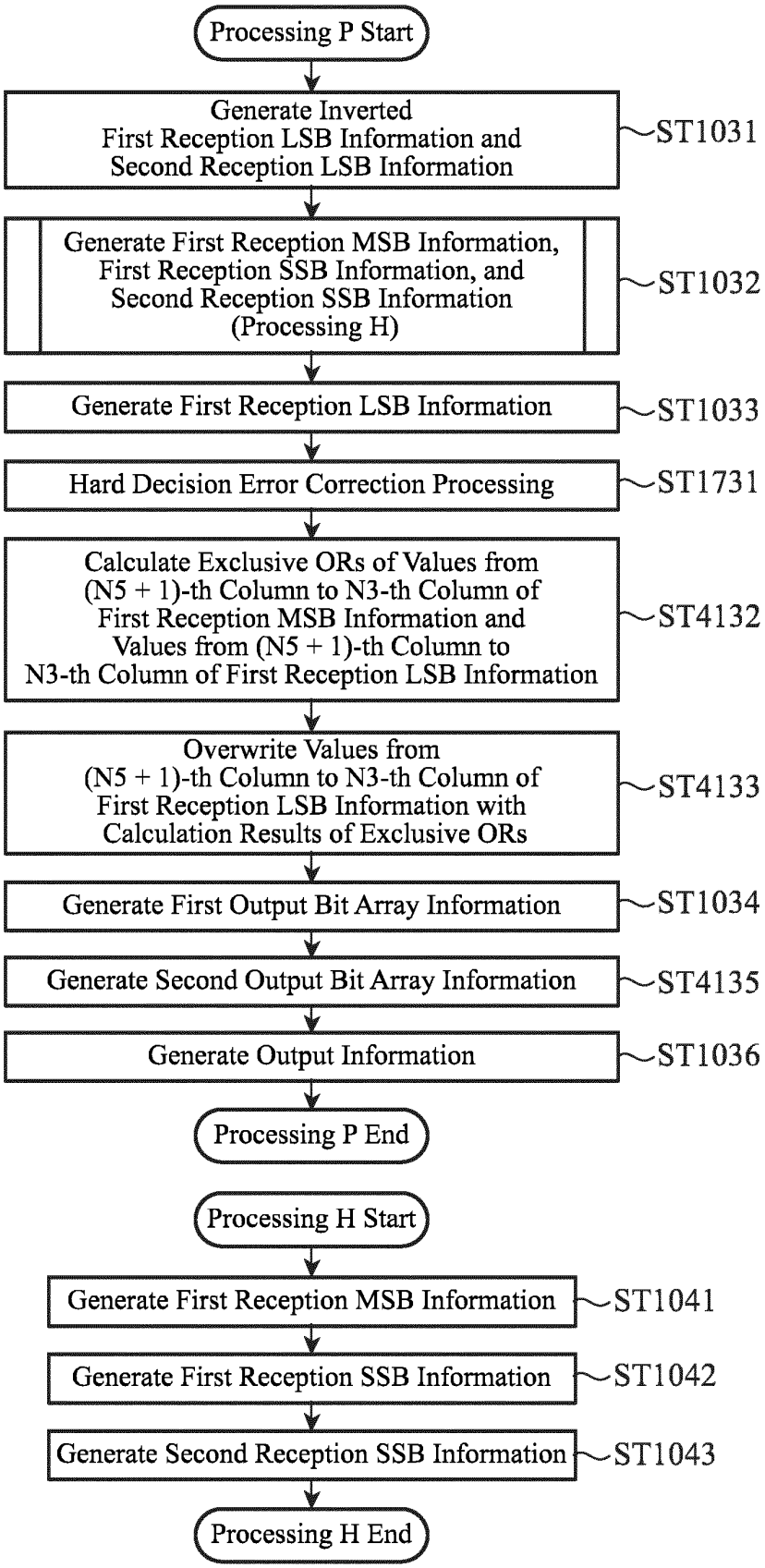

Processing D Start
Generate Reception QAM Symbol
ST1001
Reception Modulation Symbol Group Information
ST1002
Processing D End
Processing E Start
Generate First Hard Decision Candidate Bit Array Information
ST1011
Generate Second Hard Decision Candidate Bit Array Information
ST1012
Generate Third Hard Decision Candidate Bit Array Information
ST1013
Processing E End
Processing F Start
Generate First Posterior L Value Sequence
ST1021
Generate Second Posterior L Value Sequence
ST1022
Generate Third Posterior L Value Sequence
ST1023
Processing F End

FIG. 41C


Processing P Start
Generate Inverted First Reception LSB Information and Second Reception LSB Information
ST1031
Generate First Reception MSB Information, First Reception SSB Information, and Second Reception SSB Information (Processing H)
ST1032
Generate First Reception LSB Information
ST1033
Hard Decision Error Correction Processing
ST1731
Calculate Exclusive ORs of Values from (N5 + 1)-th Column to N3-th Column of First Reception MSB Information and Values from (N5 + 1)-th Column to N3-th Column of First Reception LSB Information
ST4132
Overwrite Values from (N5 + 1)-th Column to N3-th Column of First Reception LSB Information with Calculation Results of Exclusive ORs
ST4133
Generate First Output Bit Array Information
ST1034
Generate Second Output Bit Array Information
ST4135
Generate Output Information
ST1036
Processing P End
Processing H Start
Generate First Reception MSB Information
ST1041
Generate First Reception SSB Information
ST1042
Generate Second Reception SSB Information
ST1043
Processing H End

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2020/006955

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl. H03M13/25(2006.01)i, H03M13/45(2006.01)i
FI: H03M13/25, H03M13/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int. Cl. H03M13/25, H03M13/45

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan	1922-1996
Published unexamined utility model applications of Japan	1971-2020
Registered utility model specifications of Japan	1996-2020
Published registered utility model applications of Japan	1994-2020

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	SUGITANI, Kiichi et al., Partial Multilevel Coding with Probabilistic Shaping for Low-power Optical Transmission, 2019, 24th OptoElectronics and Communications Conference (OECC) and 2019 International Conference on Photonics in Switching and Computing (PSC), 2019 (accession date), sections I, II	16, 17 1-15, 18
A	BISPLINGHOFF Andreas, et al. Low-Power, Phase-Slip Tolerant, Multilevel Coding for M-QAM, Journal of Lightwave Technology, vol. 35, no. 4, 2017, pp. 1006-1014, section III, section III	1-18
A	WO 2018/167920 A1 (MITSUBISHI ELECTRIC CORP.) 20 September 2018	1-18

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31.03.2020	07.04.2020
Name and mailing address of the ISA/ Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2020/006955

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2018/116411 A1 (NEC CORP.) 28 June 2018	1-18
A	US 10091046 B1 (NOKIA TECHNOLOGIES OY) 02 October 2018	1-18

Form PCT/ISA/210 (continuation of second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/JP2020/006955

Patent Documents referred to in the Report	Publication Date	Patent Family	Publication Date
WO 2018/167920 A1	20.09.2018	CN 110402565 A	
WO 2018/116411 A1	28.06.2018	(Family: none)	
US 10091046 B1	02.10.2018	WO 2019/096895 A1	

Form PCT/ISA/210 (patent family annex) (January 2015)

REFERENCES CITED IN THE DESCRIPTION

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Non-patent literature cited in the description

- **K. SUGITANI et al.** Partial multilevel coding with probabilistic shaping for low-power optical transmission. *Proc. OECC/PSC,* 2019 **[0006]**
- **T. YOSHIDA.** Hierarchical Distribution Matching for Probabilistically Shaped Coded Modulation. *Journal of Lightwave Technology,* March 2019, vol. 37 (6), 1579-1589 **[0088]**