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(54) **FPCB AND MANUFACTURING METHOD THEREFOR**

FPCB UND HERSTELLUNGSVERFAHREN DAFÜR

CARTE DE CIRCUIT IMPRIMÉ FLEXIBLE ET SON PROCÉDÉ DE FABRICATION

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(56) References cited:

JP-A- 2007 018 774 JP-A- H0 845 413

KR-A- 20060 068 964 US-A- 4 388 603

US-A- 5 099 219

US-A1- 2002 101 323

US-A1- 2019 006 141

US-B1- 9 854 671

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Description**CROSS-REFERENCE TO RELATED APPLICATION**

[0001] The present application claims the benefit of the priority of Korean Patent Application No. 10-2020-0094041, filed on July 28, 2020.

TECHNICAL FIELD

[0002] The present invention relates to an FPCB and a method for manufacturing the same, and more specifically, to an FPCB which does not require a fuse to be mounted thereon, thereby reducing the total volume and saving costs, and a method for manufacturing the same.

BACKGROUND ART

[0003] A printed circuit board (PCB) is widely used in various electronic products such as TVs, computers, mobile phones, displays, communication networks, and semiconductor modules. As a type of such PCB, a flexible printed circuit board (FPCB) with flexibility in particular has recently been widely used.

[0004] In general, an FPCB is manufactured by laminating a copper foil on a polyimide film to form a copper clad laminate, laminating a dry film thereon to form a conductor pattern through exposure, development, and etching processes, and then attach a cover layer on the outermost copper foil. The FPCB is installed in a bent state inside a complex product case by utilizing the flexibility of raw materials or is used at a repeatedly moving portion, and due to the properties thereof, is used in various manners in miniaturization (digital cameras, camcorders, etc.), flexibility (printer heads, hard disks, etc.), high-density wires (precision instruments such as medical devices), and rationalization of assembly (measuring instruments, vehicle electronics, battery modules, etc.).

[0005] The FPCB is formed by etching and the like, and thus, does not occupy a large volume, and does not frequently cause problems such as disconnection due to an external impact. However, elements such as a fuse are mounted on the FPCB separately through a mounting process after the FPCB is completely manufactured. Therefore, there have been problems in that the total volume of the FPCB increases, and costs also increase.

[Prior Art Document]

[0006]

(Patent Document 1) Korean Patent Publication No. 1845714.

US5099219 and US2019006141 disclose a flexible printed circuit board, wherein the pattern circuit layer comprises a pattern fuse. US9854671 discloses a circuit board comprising an inductive coil with a double helical structure.

DISCLOSURE OF THE INVENTION**TECHNICAL PROBLEM**

[0007] An object of the present invention for solving the above problems is to provide an FPCB which does not require a fuse to be mounted thereon, thereby reducing the total volume and saving costs, and a method for manufacturing the same.

[0008] Problems to be solved by the present invention are not limited to the above-mentioned problem, and other problems that are not mentioned may be apparent to those skilled in the art from the following description.

15 TECHNICAL SOLUTION

[0009] In an FPCB including a pattern circuit layer according to an embodiment of the present invention for achieving the above objects, the pattern circuit layer has a pattern fuse embedded therein, and the pattern fuse includes: a first conductive wire made of a metal and having a spiral structure; and a second conductive wire made of a metal and having a spiral structure, wherein the first conductive wire and the second conductive wire have a double helix structure.

[0010] In addition, the first conductive wire may include: a first lower conductive wire formed on a bottom surface of the pattern circuit layer; a first upper conductive wire formed on a top surface of the pattern circuit layer; and a first via conductive wire configured to connect the first lower conductive wire and the first upper conductive wire to each other, and the second conductive wire may include: a second lower conductive wire formed on the bottom surface of the pattern circuit layer; a second upper conductive wire formed on the top surface of the pattern circuit layer; and a second via conductive wire configured to connect the second lower conductive wire and the second upper conductive wire to each other.

[0011] In addition, the first conductive wire and the second conductive wire may have a quadrangular shape and a double helix structure.

[0012] In addition, each of the first lower conductive wire, the second lower conductive wire, the first upper conductive wire, and the second upper conductive wire may be formed to have a linear shape.

[0013] In addition, each of the first via conductive wire and the second via conductive wire may be formed to have a linear shape in a thickness direction on the pattern circuit layer.

[0014] In addition, each of the first conductive wire and the second conductive wire may have a start terminal and an end terminal, which are exposed on only one of the top surface or the bottom surface of the pattern circuit layer.

[0015] In addition, the start terminal of the first conductive wire and the start terminal of the second conductive wire may be separately formed, and the end terminal of the first conductive wire and the end terminal of the second

ond conductive wire may also be separately formed.

[0016] In addition, the start terminal of the first conductive wire and the start terminal of the second conductive wire may be formed connected to each other, and the end terminal of the first conductive wire and the end terminal of the second conductive wire may be formed connected to each other.

[0017] In addition, each of the first conductive wire and the second conductive wire may have the start terminal connected to a power bus bar and the end terminal connected to a sensing bus bar.

[0018] In addition, the end terminal of the first conductive wire may be connected to a first sensing bus bar, and the end terminal of the second conductive wire may be connected to a second bus bar.

[0019] In addition, the metal may include at least one of silver, copper, gold, or aluminum.

[0020] In addition, a cover lay may be further laminated on the top surface of the pattern circuit layer.

[0021] A method for manufacturing an FPCB according to the present invention for achieving the above objects is defined in claim 13. The method includes: forming a first lower conductive wire and a second lower conductive wire on an top surface of a base film; exposing both ends of the first lower conductive wire and the second lower conductive wire, and laminating a micro-pillar on the top surface of the base film; forming a first via conductive wire and a second via conductive wire on both the ends of the first lower conductive wire and the second lower conductive wire, respectively; injecting a filler into an empty space in which the micro-pillar is not filled on the top surface of the base film; and forming a first upper conductive wire connecting the first via conductive wires to each other and a second upper conductive wire connecting the second via conductive wires to each other on an top surface of the micro-pillar.

[0022] In addition, in the forming of the first lower conductive wire and the second lower conductive wire, the first lower conductive wire and the second lower conductive wire may be formed parallel to a first direction.

[0023] In addition, in the forming of the first upper conductive wire and the second upper conductive wire, the first upper conductive wire and the second upper conductive wire may be formed parallel to a second direction.

[0024] In addition, the first direction and the second direction may be directions different from each other.

[0025] In addition, in the forming of the first lower conductive wire and the second lower conductive wire, the first lower conductive wire and the second lower conductive wire may be formed on the top surface of the base film by at least one of an etching or printing method.

[0026] In addition, in the forming of the first upper conductive wire and the second upper conductive wire, the first upper conductive wire and the second upper conductive wire may be formed on the top surface of the micro-pillar by at least one of an etching or printing method.

[0027] In addition, after the forming of the first upper

conductive wire and the second upper conductive wire, a first conductive wire including the first lower conductive wire, the first via conductive wire, and the first upper conductive wire, and a second conductive wire including the second lower conductor, the second via conductor, and the second upper conductor may each have a start terminal formed at a start portion, and an end terminal formed at an end portion.

[0028] In addition, the first conductive wire and the second conductive wire may have the start terminal and the end terminal, which are exposed only on one of an top surface or a bottom surface of a pattern circuit layer.

[0029] Other specific details of the present invention are included in the detailed description and drawings.

ADVANTAGEOUS EFFECTS

[0030] According to the embodiments of the present invention, there are at least the following effects.

[0031] Since the pattern fuse having the double helix structure is formed on the FPCB using the through polymer via (TPV) method rather than the mounting method and the like, it is possible to reduce the total volume of the FPCB and save the costs.

[0032] Effects according to the present invention are not limited by the contents exemplified above, and more various effects are included herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033]

FIG. 1 is a perspective view of a FPCB 1 which has a pattern fuse 100 embedded therein according to an embodiment of the present invention.

FIG. 2 is a flowchart illustrating a method for manufacturing the FPCB 1 which has the pattern fuse 100 embedded therein according to an embodiment of the present invention.

FIG. 3 is a schematic side view illustrating a state in which a first lower conductive wire 1011 and a second lower conductive wire 1021 are formed on a base film 11 according to an embodiment of the present invention.

FIG. 4 is a schematic top view illustrating the state in which the first lower conductive wire 1011 and the second lower conductive wire 1021 are formed on the base film 11 according to an embodiment of the present invention.

FIG. 5 is a schematic side view illustrating a state in which a micro-pillar 103 is formed on the base film 11 according to an embodiment of the present invention.

FIG. 6 is a schematic top view illustrating the state in which the micro-pillar 103 is formed on the base film 11 according to an embodiment of the present invention.

FIG. 7 is a schematic side view illustrating a state in

which a first via conductive wire 1012 and a second via conductive wire 1022 are formed on the base film 11 according to an embodiment of the present invention.

FIG. 8 is a schematic side view illustrating a state in which a filler 104 is injected into the base film 11 according to an embodiment of the present invention.

FIG. 9 is a schematic top view illustrating the state in which the filler 104 is injected into the base film 11 according to an embodiment of the present invention.

FIG. 10 is a schematic top view illustrating a state in which a first upper conductive wire 1013 and a second upper conductive wire 1023 are formed according to an embodiment of the present invention.

FIG. 11 is a perspective view illustrating a state in which start terminals 1014 and 1024 and end terminals 1015 and 1025 are formed on a first conductive wire 101 and a second conductive wire 102 according to an embodiment of the present invention.

FIG. 12 is a schematic view illustrating a state in which bus bars 21 and 22 are connected to the pattern fuse 100 according to an embodiment of the present invention.

FIG. 13 is a perspective view illustrating the state in which a start terminal 105 and an end terminal 106 are formed on the first conductive wire 101 and the second conductive wire 102 according to another embodiment of the present invention.

FIG. 14 is a schematic view illustrating a state in which bus bars 21a and 22a are connected to a pattern fuse 100a according to another embodiment of the present invention.

MODE FOR CARRYING OUT THE INVENTION

[0034] Advantages and features of the inventive concept and methods of accomplishing the same may be understood more readily by reference to the following detailed description of exemplary embodiments and the accompanying drawings. The inventive concept may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the inventive concept to those skilled in the art to which the inventive concept pertains. The inventive concept will only be defined by the appended claims. The same reference numerals refer to like elements throughout the specification.

[0035] Unless otherwise defined, all the terms used herein (including technical and scientific terms) will be used in a sense that can be commonly understood to those of ordinary skill in the art to which the inventive concept pertains. In addition, the terms that are defined in a commonly used dictionary are not interpreted ideally or excessively unless specifically defined.

[0036] The terms used herein are for the purpose of describing embodiments and are not intended to be limiting of the present invention. In the present disclosure, singular forms include plural forms unless the context clearly indicates otherwise. As used herein, the terms "comprises" and/or "comprising" are intended to be inclusive of the stated elements, and do not exclude the possibility of the presence or the addition of one or more other elements.

[0037] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0038] FIG. 1 is a perspective view of a FPCB 1 which has a pattern fuse 100 embedded therein according to an embodiment of the present invention.

[0039] According to an embodiment of the present invention, since the pattern fuse 100 having a double helix structure is formed on the FPCB 1 using a through polymer via (TPV) method rather than a mounting method and the like, it is possible to reduce the total volume of the FPCB 1 and save costs.

[0040] To this end, in the FPCB 1 including a pattern circuit layer 10 according to an embodiment of the present invention, the pattern circuit layer 10 has the pattern fuse 100 embedded therein, and the pattern fuse 100 includes a first conductive wire 101 made of a metal and spirally formed, and a second conductive wire 102 made of a metal and spirally formed. The first conductive wire 101 and the second conductive wire 102 have a double helix structure.

[0041] As illustrated in FIG. 1, the pattern fuse 100 according to an embodiment of the present invention includes the first conductive wire 101 and the second conductive wire 102. The first conductive wire 101 is made of a metal, and is embedded in the pattern circuit layer 10 of the FPCB 1. In addition, the second conductive wire 102 is also made of a metal, and is embedded in the pattern circuit layer 10 of the FPCB 1. Both the first conductive wire 101 and the second conductive wire 102 have spiral structures, and particularly, a double helix structure.

[0042] Specifically, the first conductive wire 101 includes a first lower conductive wire 1011, a first upper conductive wire 1013, and a first via conductive wire 1012. The first lower conductive wire 1011 is formed to have a linear shape on a bottom surface of the pattern circuit layer 10, and the first upper conductive wire 1013 is formed to have a linear shape on a top surface of the pattern circuit layer 10. In addition, the first via conductive wire 1012 connects the first lower conductive wire 1011 and the first upper conductive wire 1013 to each other, and is formed to have a linear shape in a thickness direction on the pattern circuit layer 10. Since the first lower conductive wire 1011, the first upper conductive wire 1013, and the first via conductive wire 1012 each have the linear shape as described above, the first conductive wire 101 may have a quadrangular shape. In addition, since the first lower conductive wire 1011, the first via

conductive wire 1012, and the first upper conductive wire 1013 are sequentially connected and repeatedly formed, the first conductive wire 101 may have the spiral structure.

[0043] In the same manner, the second conductive wire 102 includes a second lower conductive wire 1021, a second upper conductive wire 1023, and a second via conductive wire 1022. The second lower conductive wire 1021 is formed to have a linear shape on the bottom surface of the pattern circuit layer 10, and the second upper conductive wire 1023 is formed to have a linear shape on the top surface of the pattern circuit layer 10. In addition, the second via conductive wire 1022 connects the second lower conductive wire 1021 and the second upper conductive wire 1023 to each other, and is formed to have a linear shape in the thickness direction on the pattern circuit layer 10. Since the second lower conductive wire 1021, the second upper conductive wire 1023, and the second via conductive wire 1022 each have the linear shape as described above, the second conductive wire 102 may have a quadrangular shape. In addition, since the second lower conductive wire 1021, the second via conductive wire 1022, and the second upper conductive wire 1023 are sequentially connected and repeatedly formed, the second conductive wire 102 may have the spiral structure.

[0044] The first conductive wire 101 and the second conductive wire 102 are not separately formed, but rather spirally formed in the state of overlapping each other, that is, have the double helix structure. In addition, the metal for forming the first conductive wire 101 and the second conductive wire 102 may include at least one of silver, copper, gold, or aluminum which has high electrical conductivity, and particularly, may preferably include copper, which is easy to be molded, has a low price, and is economical.

[0045] FIG. 2 is a flowchart illustrating a method for manufacturing the FPCB 1 which has the pattern fuse 100 embedded therein according to an embodiment of the present invention.

[0046] A method for manufacturing the FPCB 1 according to an embodiment of the present invention includes a process of forming a first lower conductive wire 1011 and a second lower conductive wire 1021 on a top surface of a base film 11; a process of exposing both ends of the first lower conductive wire 1011 and the second lower conductive wire 1021, and laminating a micro-pillar 103 on the top surface of the base film 11; a process of forming the first via conductive wire 1012 and the second via conductive wire 1022 on both the ends of the first lower conductive wire 1011 and the second lower conductive wire 1021, respectively; a process of injecting a filler 104 into an empty space in which the micro-pillar 103 is not filled on the top surface of the base film 11, and a process of forming the first upper conductive wire 1013 connecting the first via conductive wires 1012 to each other and the second upper conductive wire 1023 connecting the second via conductive wires 1022 to each other on a top

surface of the micro-pillar 103.

[0047] Hereinafter, each step illustrated in the flow chart of FIG. 2 will be described in detail with reference to FIG. 3 to FIG. 10.

[0048] FIG. 3 is a schematic side view illustrating a state in which a first lower conductive wire 1011 and a second lower conductive wire 1021 are formed on a base film 11 according to an embodiment of the present invention, and FIG. 4 is a schematic top view illustrating the state in which the first lower conductive wire 1011 and the second lower conductive wire 1021 are formed on the base film 11 according to an embodiment of the present invention.

[0049] First, the base film 11 is prepared, and as illustrated in FIG. 3, the first lower conductive wire 1011 and the second lower conductive wire 1021 are formed on an top surface of the base film 11 (S201). The base film 11 may be a film containing silicon. In addition, the first lower conductive wire 1011 and the second lower conductive wire 1021 may be formed on the top surface of the base film 11 by at least one of an etching or printing method.

[0050] The first lower conductive wire 1011 and the second lower conductive wire 1021 are each provided in plurality, and may be formed parallel to a first direction. In addition, the first direction may have, for example, as illustrated in FIG. 4, a predetermined inclination with respect to the base film 11. In addition, the first lower conductive wire 1011 and the second lower conductive wire 1021 may be alternately formed with each other. Therefore, later, the first conductive wire 101 and the second conductive wire 102 may have the double helix structure.

[0051] FIG. 5 is a schematic side view illustrating a state in which a micro-pillar 103 is formed on the base film 11 according to an embodiment of the present invention, and FIG. 6 is a schematic top view illustrating the state in which the micro-pillar 103 is formed on the base film 11 according to an embodiment of the present invention.

[0052] When the first lower conductive wire 1011 and the second lower conductive wire 1021 are formed, both the ends of the first lower conductive wire 1011 and the second lower conductive wire 1021 are exposed as illustrated in FIG. 5, and the micro-pillar 103 is laminated on the top surface of the base film 11 (S202). At this time, the micro-pillar 103 are provided in plurality, and as illustrated in FIG. 6, and may be formed parallel to a second direction which is different from the first direction. In addition, later, the first upper conductive wire 1013 and the second upper conductive wire 1023 are formed along the micro-pillar 103. Therefore, ends of different first lower conductive wires 1011 may be disposed on both the ends of one micro-pillar 103, respectively, or ends of different second lower conductive wires 1021 may be disposed on both the ends of one micro-pillar 103, respectively.

[0053] In order to laminate the micro-pillar 103, a thick photoresist may be first laminated and then patterned. The micro-pillar 103 may be an epoxy-based SU-8 negative photoresist which is crosslinked by ultraviolet rays

and of which remaining portions are washed to facilitate the patterning.

[0054] Meanwhile, although not shown in the drawings, after the micro-pillar 103 is laminated, a separate seed layer may be formed to activate the micro-pillar 103. In order to form the seed layer, a physical vapor deposition (PVD) method may be used, or an atomic layer deposition (ALD) method may be used. In addition, the seed layer may include nitride titanium (TiN) having electrical conductivity, good adhesion to a metal, and a low processing temperature.

[0055] FIG. 7 is a schematic side view illustrating a state in which a first via conductive wire 1012 and a second via conductive wire 1022 are formed on the base film 11 according to an embodiment of the present invention.

[0056] After the micro-pillar 103 is laminated, the first via conductive wire 1012 and the second via conductive wire 1022 may be respectively formed at both the ends of the first lower conductive wire 1011 and the second lower conductive wire 1021 S203. As described above, ends of different first lower conductive wires 1011 may be disposed on both the ends of the micro-pillar 103, respectively, or ends of different second lower conductive wire 1021 may be disposed on both the ends of the micro-pillar 103, respectively. Therefore, when the first via conductive wire 1012 and the second via conductive wire 1022 are formed, as illustrated in FIG. 7, the first via conductive wire 1012 and the second via conductive wire 1022 may be formed along sidewalls of both the ends of the micro-pillar 103.

[0057] In order to form the first via conductive wire 1012 and the second via conductive wire 1022, the micro-pillar 103 may be subjected to electroless plating with a metal such as copper. In addition, in order to prevent corrosion of the metal, electrolytic plating may be additionally performed with a metal having low ionization tendency.

[0058] Each of the first via conductive wire 1012 and the second via conductive wire 1022 is also made of a metal, and when the first conductive wire 1013 and the second conductive wire 1023 are formed later, the first via conductive wire 1012 and the second via conductive wire 1022 respectively connect the lower conductive wires 1011 and 1021 and the upper conductive wires 1021 and 1022, and thus, serve as a through electrode configured to electrically connect the bottom surface and the top surface of the pattern circuit layer 10 to each other.

[0059] FIG. 8 is a schematic side view illustrating a state in which a filler 104 is injected into the base film 11 according to an embodiment of the present invention, and FIG. 9 is a schematic top view illustrating the state in which the filler 104 is injected into the base film 11 according to an embodiment of the present invention.

[0060] As illustrated in FIGS. 8 and 9, on the top surface of the base film 11, the filler 104 is injected into an empty space in which the micro-pillar 103 is not filled (S204). The filler 104 may be an epoxy molding composition (EMC) having electrical insulation. Thereby, the micro-pillar 103 may be encapsulated inside the insula-

tor.

[0061] FIG. 10 is a schematic top view illustrating a state in which a first upper conductive wire 1013 and a second upper conductive wire 1023 are formed according to an embodiment of the present invention.

[0062] On the top surface of the micro-pillar 103, the first upper conductive wire 1013 connecting the first via conductive wires 1012 to each other and the second upper conductive wire 1023 connecting the second via conductive wires 1022 to each other are formed S205. In addition, the first upper conductive wire 1021 and the second upper conductive wire 1023 may be formed on the top surface of the base film 103 by at least one of an etching or printing method.

[0063] The first upper conductive wire 1013 and the second upper conductive wire 1023 are all formed along the micro-pillar 103. That is, the first upper conductive wire 1013 may be formed on the top surface of the micro-pillar 103 on which the first via conductive wire 1012 is formed, while connecting the first via conductive wires 1012 to each other, the second upper conductive wire 1023 may be formed on the top surface of the micro-pillar 103 on which the second via conductive wire 1022 is formed, while connecting the first via conductive wires 1012 to each other. At this time, the first upper conductive wire 1013 and the second upper conductive wire 1023 may be formed to be wider than the first via conductive wire 1012 and the second via conductive wire 1022 to be connected to the first via conductive wire 1012 and the second via conductive wire 1022, respectively.

[0064] As described above, ends of different first lower wires 1011 may be disposed on both the ends of one micro-pillar 103, respectively, or ends of different second lower wires 1021 may be disposed on both the ends of one micro-pillar 103, respectively. Therefore, the first upper conductive wire 1013 is connected to each of the different first lower conductive wires 1011 through the first via conductive wire 1012, and the second upper conductive wire 1023 is connected to each of the different second lower conductive wires 1021 through the second via conductive wire 1012, so that the first conductive wire 101 and the second conductive wire 102 may be spirally formed.

[0065] The first upper conductive wire 1013 and the second upper conductive wire 1023 are each provided in plurality, and are all formed along the micro-pillar 103, and thus, may be formed parallel to the second direction. It is preferable that the second direction is a direction different from the first direction. For example, as illustrated in FIG. 10, the second direction may have a predetermined inclination with respect to the first direction. In addition the first upper conductive wire 1013 and the second upper conductive wire 1023 may be alternately formed with each other. Therefore, in the pattern circuit layer 10 of the FPCB 1, the pattern fuse 100 including the first conductive wire 101 and the second lead 102 having a double helix structure may be formed embedded. Furthermore, after the pattern fuse 100 is formed,

the base film 11 may be removed.

[0066] Meanwhile, although not illustrated in the drawings, in order to protect a circuit pattern of the FPCB 1, a cover lay may be laminated on the top surface of the micro-pillar 103. The cover lay may be a film of a polyimide-based material.

[0067] FIG. 11 is a perspective view illustrating a state in which start terminals 1014 and 1024 and end terminals 1015 and 1025 are formed on a first conductive wire 101 and a second conductive wire 102 according to an embodiment of the present invention.

[0068] After the first upper conductive wire 1013 and the second upper conductive wire 1023 are formed, the start terminals 1014 and 1024 are formed at start portions of the first conductive wire 101 and the second conductive wire 102, and the end terminals 1015 and 1025 are formed at end portions thereof. At this time, the first conductive wire 101 and the second conductive wire 102 may have the start terminals 1014 and 1024 and the end terminals 1015 and 1025 all exposed only on one of the top surface or the bottom surface of the pattern circuit layer 10.

[0069] In addition, according to an embodiment of the present invention, the first conductive wire 101 and the second conductive wire 102 have the start terminals 1014 and 1024 and the end terminals 1015 and 1025 all separately formed. That is, as illustrated in FIG. 11, at the start portion of the first conductive wire 101, a first start terminal 1014 is formed, and at the start portion of the second conductive wire 102, a second start terminal 1024 is separately formed. In addition, at the end portion of the first conductive wire 101, a first end terminal 1015 is formed, and at the end portion of the second conductive wire 102, a second end terminal 1025 is separately formed.

[0070] FIG. 12 is a schematic view illustrating a state in which bus bars 21 and 22 are connected to the pattern fuse 100 according to an embodiment of the present invention.

[0071] If at least one of the first start terminal 1014, the second start terminal 1024, the first end terminal 1015, or the second end terminal 1025 is exposed on another surface of the pattern circuit layer 10, in order to be connected to the bus bars 21 and 22, the upper and bottom surfaces of the FPCB 1 should be bent to be inverted from each other. Then, a process of bending the FPCB 1 should be further added, and there is also a problem in that the durability of a bent portion is degraded to cause lifespan to be shortened.

[0072] The first start terminal 1014 of the first conductive wire 101 and the second start terminal 1024 of the second conductive wire 102 are, as illustrated in FIG. 12, connected to one power bus bar 21. However, according to an embodiment of the present invention, the first start terminal 1014 and the second start terminal 1024 are all exposed on the same surface of the pattern circuit layer 10, so that when connected to the power bus bar 21, the top surface and the bottom surface of the FPCB 1 are

not required to be bent to be inverted from each other.

[0073] In addition, the first end terminal 1015 of the first conductive wire 101 and the second end terminal 1025 of the second conductive wire 102 are connected to different sensing bus bars 221 and 222, respectively. However, the first end terminal 1015 and the second end terminal 1025 are all exposed on the same surface of the pattern circuit layer 10, so that when connected to the sensing bus bar 22, the top surface and the bottom surface of the FPCB 1 are not required to be bent to be inverted from each other.

[0074] FIG. 13 is a perspective view illustrating the state in which a start terminal 105 and an end terminal 106 are formed on the first conductive wire 101 and the second conductive wire 102 according to another embodiment of the present invention.

[0075] According to another embodiment of the present invention, the first conductive wire 101 and the second conductive wire 102 have the start terminal 105 and the end terminal 106 formed respectively connected to each other. That is, as illustrated in FIG. 13, a first start terminal formed in a start portion of the first conductive wire 101 and a second start terminal formed in a start portion of the second conductive wire 102 are formed connected to each other. In addition, a first end terminal formed in an end portion of the first conductive wire 101 and a second end terminal formed in an end portion of the second conductive wire 102 are formed connected to each other. Particularly, as illustrated in FIG. 13, the first start terminal and the second start terminal may be integrally formed as one start terminal 105, and the first end terminal and the second end terminal may be integrally formed as one end terminal 106. However, the present invention is not limited thereto. The first start terminal and the second start terminal and the first end terminal and the second end terminal may be separately formed and then bonded to each other through a separate bonding part (not shown), or may be connected to each other through welding or an adhesive. In addition, the first conductive wire 101 and the second conductive wire 102 may have the start terminal 105 and the end terminal 106 all exposed only on one of the top surface or the bottom surface of the pattern circuit layer 10.

[0076] FIG. 14 is a schematic view illustrating a state in which bus bars 21a and 22a are connected to a pattern fuse 100a according to another embodiment of the present invention.

[0077] The start terminals 105 of the first conductive wire 101 and the second conductive wire 102 are formed connected to each other, and thus, are connected to one power bus bar 21a as illustrated in FIG. 14. However, the first start terminal and the second start terminal are all exposed on the same surface of the pattern circuit layer 10 and then connected to each other, so that when connected to the power bus bar 21a, a top surface and a bottom surface of an FPCB 1a are not required to be bent to be inverted from each other.

[0078] In addition, the end terminals 106 of the first

conductive wire 101 and the second conductive wire 102 are also formed connected to each other, and thus, are connected to one sensing bus bar 22a. However, the first end terminal and the second end terminal are all exposed on the same surface of the pattern circuit layer 10, so that when connected to the sensing bus bar 22a, the top surface and the bottom surface of the FPCB 1a are not required to be bent to be inverted from each other.

[Description of the Reference Numerals or Symbols]

[0079]

1: FPCB 2: Bus bar
10: Pattern circuit layer 11: Base film
21: Power bus bar 22: Sensing bus bar
100: Pattern fuse 101: First conductive wire
102: Second conductive wire 103: Micro-pillar
104: Filler 1011: First lower conductive wire
1012: First via conductive wire 1013: First upper conductive wire
1014: First start terminal 1015: First end terminal
1021: Second lower conductive wire 1022: Second via conductive wire
1023: Second upper conductive wire 1024: Second start terminal
1025: Second end terminal

Claims

1. An flexible printed circuit board FPCB (1) comprising a pattern circuit layer (10),

wherein the pattern circuit layer (10) has a pattern fuse (100) embedded therein,
characterised in that
the pattern fuse (100) comprises:

a first conductive wire (101) made of a metal and having a spiral structure; and
a second conductive wire (102) made of a metal and having a spiral structure,
wherein the first conductive wire (101) and the second conductive wire (102) have a double helix structure.

2. The FPCB of claim 1, wherein the first conductive wire comprises:

a first lower conductive wire (1011) formed on a bottom surface of the pattern circuit layer (10);
a first upper conductive wire (1013) formed on a top surface of the pattern circuit layer (10); and
a first via conductive wire (1012) configured to connect the first lower conductive wire (1011) and the first upper conductive wire (1013) to each other, and

the second conductive wire (102) comprises:

a second lower conductive wire (1021) formed on the bottom surface of the pattern circuit layer (10);
a second upper conductive wire (1023) formed on the top surface of the pattern circuit layer (10); and
a second via conductive wire (1022) configured to connect the second lower conductive wire (1021) and the second upper conductive wire (1023) to each other.

3. The FPCB of claim 2, wherein the first conductive wire (101) and the second conductive wire (102) have a quadrangular shape and a double helix structure.

4. The FPCB of claim 3, wherein each of the first lower conductive wire (1011), the second lower conductive wire (1021), the first upper conductive wire (1013), and the second upper conductive wire (1023) is formed to have a linear shape.

5. The FPCB of claim 3, wherein each of the first via conductive wire (1012) and the second via conductive wire (1022) is formed to have a linear shape in a thickness direction on the pattern circuit layer (10).

6. The FPCB of claim 1, wherein each of the first conductive wire (101) and the second conductive wire (102) has a start terminal (1014, 1024) and an end terminal (1015, 1025), which are exposed on only one of the top surface or the bottom surface of the pattern circuit layer (10).

7. The FPCB of claim 6, wherein the start terminal (1014) of the first conductive wire (101) and the start terminal (1024) of the second conductive wire (102) are separately formed, and the end terminal (1015) of the first conductive wire (101) and the end terminal (1025) of the second conductive wire (102) are also separately formed.

8. The FPCB of claim 6, wherein the start terminal (1014) of the first conductive wire (101) and the start terminal (1024) of the second conductive wire (102) are formed connected to each other, and the end terminal (1015) of the first conductive wire (101) and the end terminal (1025) of the second conductive wire (102) are formed connected to each other.

9. The FPCB of claim 6, wherein each of the first conductive wire (101) and the second conductive wire (102) has the start terminal (1015, 1024) connected to a power bus bar (21) and the end terminal (1015, 1025) connected to a sensing bus bar (22).

10. The FPCB of claim 9, wherein the end terminal (1015) of the first conductive wire (101) is connected to a first sensing bus bar, and the end terminal (1025) of the second conductive wire (102) is connected to a second sensing bus bar. 5
11. The FPCB of claim 1, wherein the metal comprises at least one of silver, copper, gold, or aluminum.
12. The FPCB of claim 1, wherein a cover lay is further laminated on the top surface of the pattern circuit layer (10). 10
13. A method for manufacturing an FPCB (1) according to one of the claims 1 to 12, the method comprising: 15
- forming a first lower conductive wire (1011) and a second lower conductive wire (1021) on a top surface of a base film (11);
- exposing both ends of the first lower conductive wire (1011) and the second lower conductive wire (1021), and laminating a micro-pillar (103) on the top surface of the base film (11); 20
- forming a first via conductive wire (1012) and a second via conductive wire (1022) on both the ends of the first lower conductive wire (1011) and the second lower conductive wire (1021), respectively; 25
- injecting a filler (104) into an empty space in which the micro-pillar (103) is not filled on the top surface of the base film (11); and 30
- forming a first upper conductive wire (1013) connecting the first via conductive wires (1012) to each other and a second upper conductive wire (1023) connecting the second via conductive wires (1022) to each other on a top surface of the micro-pillar (103). 35
14. The method of claim 13, wherein, in the forming of the first lower conductive wire (1011) and the second lower conductive wire (1021), the first lower conductive wire (1011) and the second lower conductive wire (1021) are formed parallel to a first direction. 40
15. The method of claim 14, wherein, in the forming of the first upper conductive wire (1013) and the second upper conductive wire (1023), the first upper conductive wire (1013) and the second upper conductive wire (1023) are formed parallel to a second direction. 45

Patentansprüche

1. Flexible gedruckte Schaltungsplatte FPCB (1), die eine Musterschaltungsschicht (10) umfasst, wobei die Musterschaltungsschicht (10) eine darin eingebettete Mustersicherung (100) aufweist, **dadurch gekennzeichnet, dass** die Mustersiche- 55

rung (100) umfasst:

einen ersten leitenden Draht (101), der aus einem Metall hergestellt ist und eine Spiralstruktur aufweist; und

einen zweiten leitenden Draht (102), der aus einem Metall hergestellt ist und eine Spiralstruktur aufweist,

wobei der erste leitende Draht (101) und der zweite leitende Draht (102) eine Doppelhelixstruktur aufweisen.

2. FPCB nach Anspruch 1, wobei der erste leitende Draht umfasst:

einen ersten unteren leitenden Draht (1011), der auf einer unteren Oberfläche der Musterschaltungsschicht (10) ausgebildet ist;

einen ersten oberen leitenden Draht (1013), der auf einer oberen Oberfläche der Musterschaltungsschicht (10) ausgebildet ist; und

einen ersten durchgehenden leitenden Draht (1012), der so konfiguriert ist, dass er den ersten unteren leitenden Draht (1011) und den ersten oberen leitenden Draht (1013) miteinander verbindet, und

der zweite leitende Draht (102) umfasst:

einen zweiten unteren leitenden Draht (1021), der auf der unteren Oberfläche der Musterschaltungsschicht (10) ausgebildet ist;

einen zweiten oberen leitenden Draht (1023), der auf der oberen Oberfläche der Musterschaltungsschicht (10) ausgebildet ist; und

einen zweiten durchgehenden leitenden Draht (1022), der so konfiguriert ist, dass er den zweiten unteren leitenden Draht (1021) und den zweiten oberen leitenden Draht (1023) miteinander verbindet.

3. FPCB nach Anspruch 2, wobei der erste leitende Draht (101) und der zweite leitende Draht (102) eine viereckige Form und eine Doppelhelixstruktur aufweisen.
4. FPCB nach Anspruch 3, wobei der erste untere leitende Draht (1011), der zweite untere leitende Draht (1021), der erste obere leitende Draht (1013) und der zweite obere leitende Draht (1023) jeweils so geformt sind, dass sie eine lineare Form aufweisen.

5. FPCB nach Anspruch 3, wobei der erste durchgehende leitende Draht (1012) und der zweite durchgehende leitende Draht (1022) jeweils so geformt sind, dass sie eine lineare Form in einer Dickenrichtung auf der Musterschaltungsschicht (10) aufwei-

sen.

6. FPCB nach Anspruch 1, wobei sowohl der erste leitende Draht (101) als auch der zweite leitende Draht (102) einen Anfangsanschluss (1014, 1024) und einen Endanschluss (1015, 1025) aufweisen, die nur entweder auf der oberen Oberfläche oder der unteren Oberfläche der Musterschaltungsschicht (10) freiliegen. 5
7. FPCB nach Anspruch 6, wobei der Anfangsanschluss (1014) des ersten leitenden Drahtes (101) und der Anfangsanschluss (1024) des zweiten leitenden Drahtes (102) separat ausgebildet sind, und der Endanschluss (1015) des ersten leitenden Drahtes (101) und der Endanschluss (1025) des zweiten leitenden Drahtes (102) ebenfalls separat ausgebildet sind. 10
8. FPCB nach Anspruch 6, wobei der Anfangsanschluss (1014) des ersten leitenden Drahtes (101) und der Anfangsanschluss (1024) des zweiten leitenden Drahtes (102) miteinander verbunden ausgebildet sind, und der Endanschluss (1015) des ersten leitenden Drahtes (101) und der Endanschluss (1025) des zweiten leitenden Drahtes (102) miteinander verbunden ausgebildet sind. 15
9. FPCB nach Anspruch 6, wobei sowohl der erste leitende Draht (101) als auch der zweite leitende Draht (102) mit dem Anfangsanschluss (1015, 1024) an eine Stromsammelschiene (21) und mit dem Endanschluss (1015, 1025) an eine Abtast-Sammelschiene (22) angeschlossen ist. 20
10. FPCB nach Anspruch 9, wobei der Endanschluss (1015) des ersten leitenden Drahtes (101) mit einer ersten Abtast-Sammelschiene verbunden ist und der Endanschluss (1025) des zweiten leitenden Drahtes (102) mit einer zweiten Abtast-Sammelschiene verbunden ist. 25
11. FPCB nach Anspruch 1, wobei das Metall mindestens eines von Silber, Kupfer, Gold oder Aluminium umfasst. 30
12. FPCB nach Anspruch 1, wobei auf die obere Oberfläche der Musterschaltungsschicht (10) außerdem eine Abdecklage laminiert ist. 35
13. Verfahren zur Herstellung einer FPCB (1) nach einem der Ansprüche 1 bis 12, wobei das Verfahren umfasst: 40

Bilden eines ersten unteren leitenden Drahtes (1011) und eines zweiten unteren leitenden Drahtes (1021) auf einer oberen Oberfläche ei-

ner Basisfolie (10);

Freilegen beider Enden des ersten unteren leitenden Drahtes (1011) und des zweiten unteren leitenden Drahtes (1021) und Laminieren einer Mikrosäule (103) auf die obere Oberfläche der Basisfolie (11);

Bilden eines ersten durchgehenden leitenden Drahtes (1012) und eines zweiten durchgehenden leitenden Drahtes (1022) an den beiden Enden des ersten unteren leitenden Drahtes (1011) bzw. des zweiten unteren leitenden Drahtes (1021);

Einspritzen eines Füllstoffs (104) in einen leeren Raum, in dem die Mikrosäule (103) nicht gefüllt ist, auf der oberen Oberfläche der Basisfolie (11); und

Bilden eines ersten oberen leitenden Drahtes (1013), der die ersten durchgehenden leitenden Drähte (1012) miteinander verbindet, und eines zweiten oberen leitenden Drahtes (1023), der die zweiten durchgehenden leitenden Drähte (1022) miteinander verbindet, auf einer oberen Oberfläche der Mikrosäule (103).

14. Verfahren nach Anspruch 13, wobei bei der Bildung des ersten unteren leitenden Drahtes (1011) und des zweiten unteren leitenden Drahtes (1021) der erste untere leitende Draht (1011) und der zweite untere leitende Draht (1021) parallel zu einer ersten Richtung ausgebildet werden. 25
15. Verfahren nach Anspruch 14, wobei bei der Bildung des ersten oberen leitenden Drahtes (1013) und des zweiten oberen leitenden Drahtes (1023) der erste obere leitende Draht (1013) und der zweite obere leitende Draht (1023) parallel zu einer zweiten Richtung ausgebildet werden. 30

Revendications 40

1. Carte de circuit imprimé souple FPCB (1) comprenant une couche de circuit à motif (10), 45

dans laquelle la couche de circuit à motif (10) a un fusible à motif (100) intégré dans celle-ci,

caractérisée en ce que

le fusible à motif (100) comprend :

un premier fil conducteur (101) constitué d'un métal et ayant une structure en spirale ; et

un deuxième fil conducteur (102) constitué d'un métal et ayant une structure en spirale ; dans laquelle le premier fil conducteur (101) et le deuxième fil conducteur (102) ont une structure en double hélice. 50

2. FPCB selon la revendication 1, dans laquelle le premier fil conducteur comprend :

un premier fil conducteur inférieur (1011) formé sur une surface inférieure de la couche de circuit à motif (10) ;
 un premier fil conducteur supérieur (1013) formé sur une surface supérieure de la couche de circuit à motif (10) ; et
 un premier fil conducteur traversant (1012) configuré pour connecter le premier fil conducteur inférieur (1011) et le premier fil conducteur supérieur (1013) l'un à l'autre, et
 le deuxième fil conducteur (102) comprend :

un deuxième fil conducteur inférieur (1021) formé sur la surface inférieure de la couche de circuit à motif (10) ;
 un deuxième fil conducteur supérieur (1023) formé sur la surface supérieure de la couche de circuit à motif (10) ; et
 un deuxième fil conducteur traversant (1022) configuré pour connecter le deuxième fil conducteur inférieur (1021) et le deuxième fil conducteur supérieur (1023) l'un à l'autre.

3. FPCB selon la revendication 2, dans laquelle le premier fil conducteur (101) et le deuxième fil conducteur (102) ont une forme quadrangulaire et une structure en double hélice.

4. FPCB selon la revendication 3, dans laquelle chacun du premier fil conducteur inférieur (1011), du deuxième fil conducteur inférieur (1021), du premier fil conducteur supérieur (1013) et du deuxième fil conducteur supérieur (1023) est formé de façon à avoir une forme linéaire.

5. FPCB selon la revendication 3, dans laquelle chacun du premier fil conducteur traversant (1012) et du deuxième fil conducteur traversant (1022) est formé de façon à avoir une forme linéaire dans une direction d'épaisseur sur la couche de circuit à motif (10).

6. FPCB selon la revendication 1, dans laquelle chacun du premier fil conducteur (101) et du deuxième fil conducteur (102) a une borne de début (1014, 1024) et une borne de fin (1015, 1025), qui sont exposées sur une seule de la surface supérieure ou de la surface inférieure de la couche de circuit à motif (10).

7. FPCB selon la revendication 6, dans laquelle la borne de début (1014) du premier fil conducteur (101) et la borne de début (1024) du deuxième fil conducteur (102) sont formées séparément, et la borne de fin (1015) du premier fil conducteur (101) et la borne de fin (1025) du deuxième fil conducteur

(102) sont également formées séparément.

8. FPCB selon la revendication 6, dans laquelle la borne de début (1014) du premier fil conducteur (101) et la borne de début (1024) du deuxième fil conducteur (102) sont formées de façon à être connectées l'une à l'autre, et la borne de fin (1015) du premier fil conducteur (101) et la borne de fin (1025) du deuxième fil conducteur (102) sont formées de façon à être connectées l'une à l'autre.

9. FPCB selon la revendication 6, dans laquelle chacun du premier fil conducteur (101) et du deuxième fil conducteur (102) a la borne de début (1015, 1024) connectée à une barre omnibus de puissance (21) et la borne de fin (1015, 1025) connectée à une barre omnibus de détection (22).

10. FPCB selon la revendication 9, dans laquelle la borne de fin (1015) du premier fil conducteur (101) est connectée à une première barre omnibus de détection, et la borne de fin (1025) du deuxième fil conducteur (102) est connectée à une deuxième barre omnibus de détection.

11. FPCB selon la revendication 1, dans laquelle le métal comprend au moins un parmi l'argent, le cuivre, l'or ou l'aluminium.

12. FPCB selon la revendication 1, dans laquelle une couche de recouvrement est en outre stratifiée sur la surface supérieure de la couche de circuit à motif (10).

13. Procédé de fabrication d'une FPCB (1) selon l'une des revendications 1 à 12, le procédé comprenant :

la formation d'un premier fil conducteur inférieur (1011) et d'un deuxième fil conducteur inférieur (1021) sur une surface supérieure d'un film de base (11) ;

l'exposition des deux extrémités du premier fil conducteur inférieur (1011) et du deuxième fil conducteur inférieur (1021), et la stratification d'un micropilier (103) sur la surface supérieure du film de base (11) ;

la formation d'un premier fil conducteur traversant (1012) et d'un deuxième fil conducteur traversant (1022) sur les deux extrémités du premier fil conducteur inférieur (1011) et du deuxième fil conducteur inférieur (1021), respectivement ;

l'injection d'une charge (104) dans un espace vide qui n'est pas rempli par le micropilier (103) sur la surface supérieure du film de base (11) ; et la formation d'un premier fil conducteur supérieur (1013) connectant les premiers fils conduc-

teurs traversants (1012) l'un à l'autre et d'un deuxième fil conducteur supérieur (1023) connectant les deuxièmes fils conducteurs traversants (1022) l'un à l'autre sur une surface supérieure du micropilier (103).

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14. Procédé selon la revendication 13, dans lequel, lors de la formation du premier fil conducteur inférieur (1011) et du deuxième fil conducteur inférieur (1021), le premier fil conducteur inférieur (1011) et le deuxième fil conducteur inférieur (1021) sont formés parallèlement à une première direction.

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15. Procédé selon la revendication 14, dans lequel, lors de la formation du premier fil conducteur supérieur (1013) et du deuxième fil conducteur supérieur (1023), le premier fil conducteur supérieur (1013) et le deuxième fil conducteur supérieur (1023) sont formés parallèlement à une deuxième direction.

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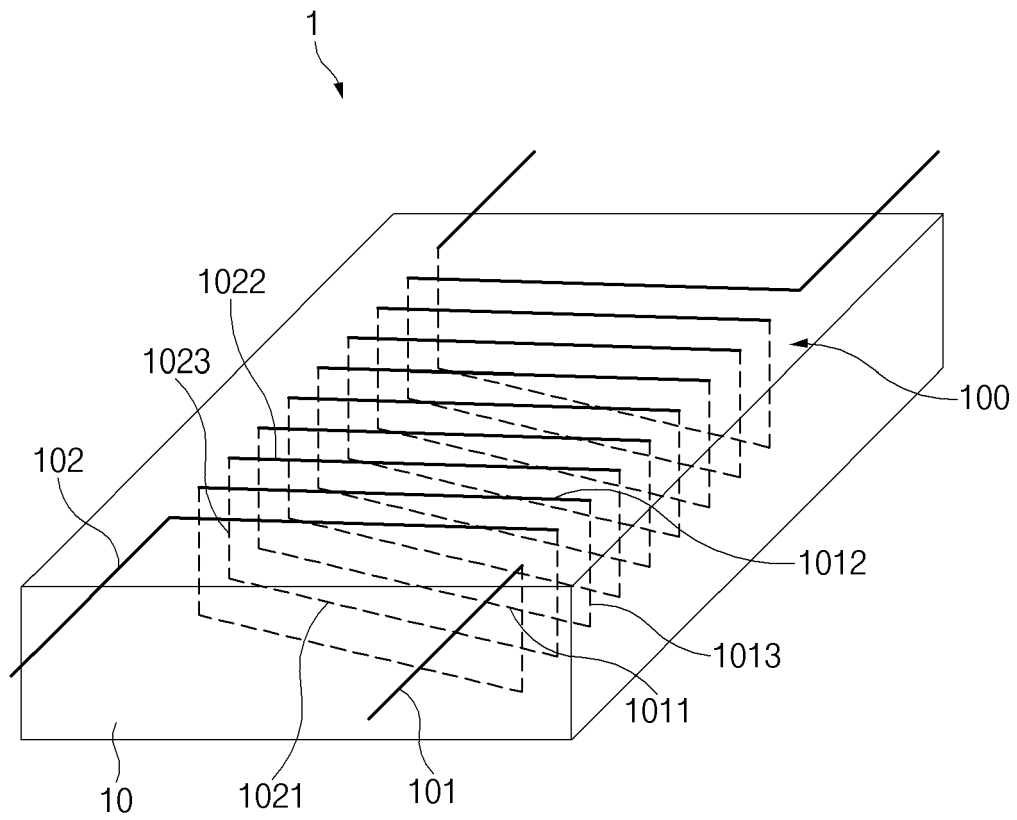


FIG.1

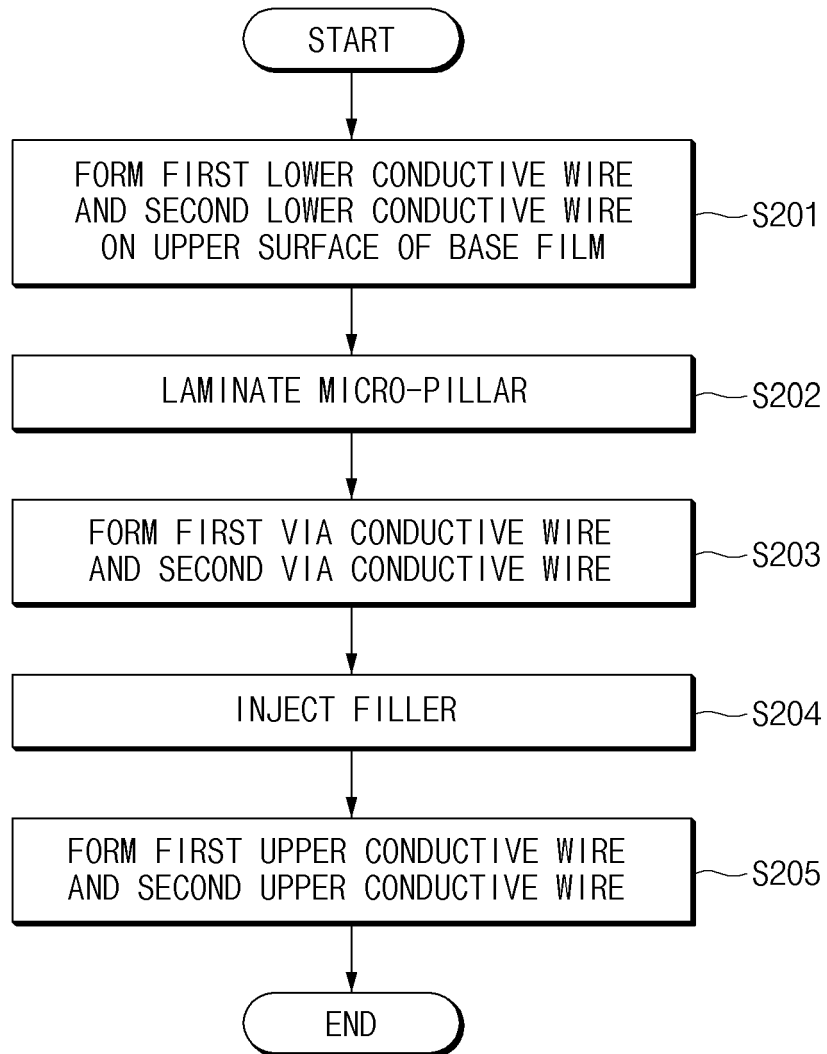


FIG.2

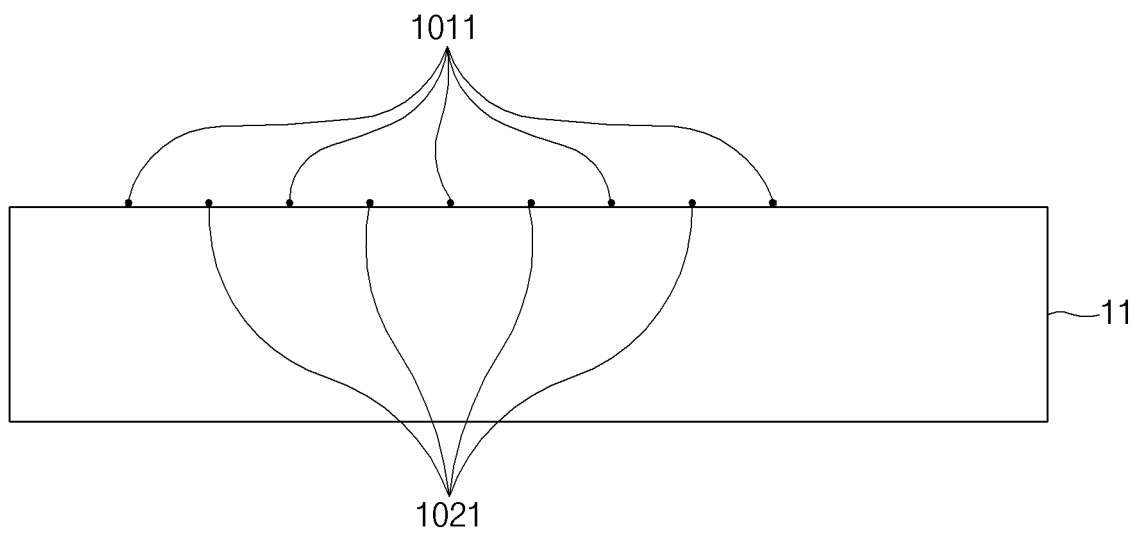


FIG.3

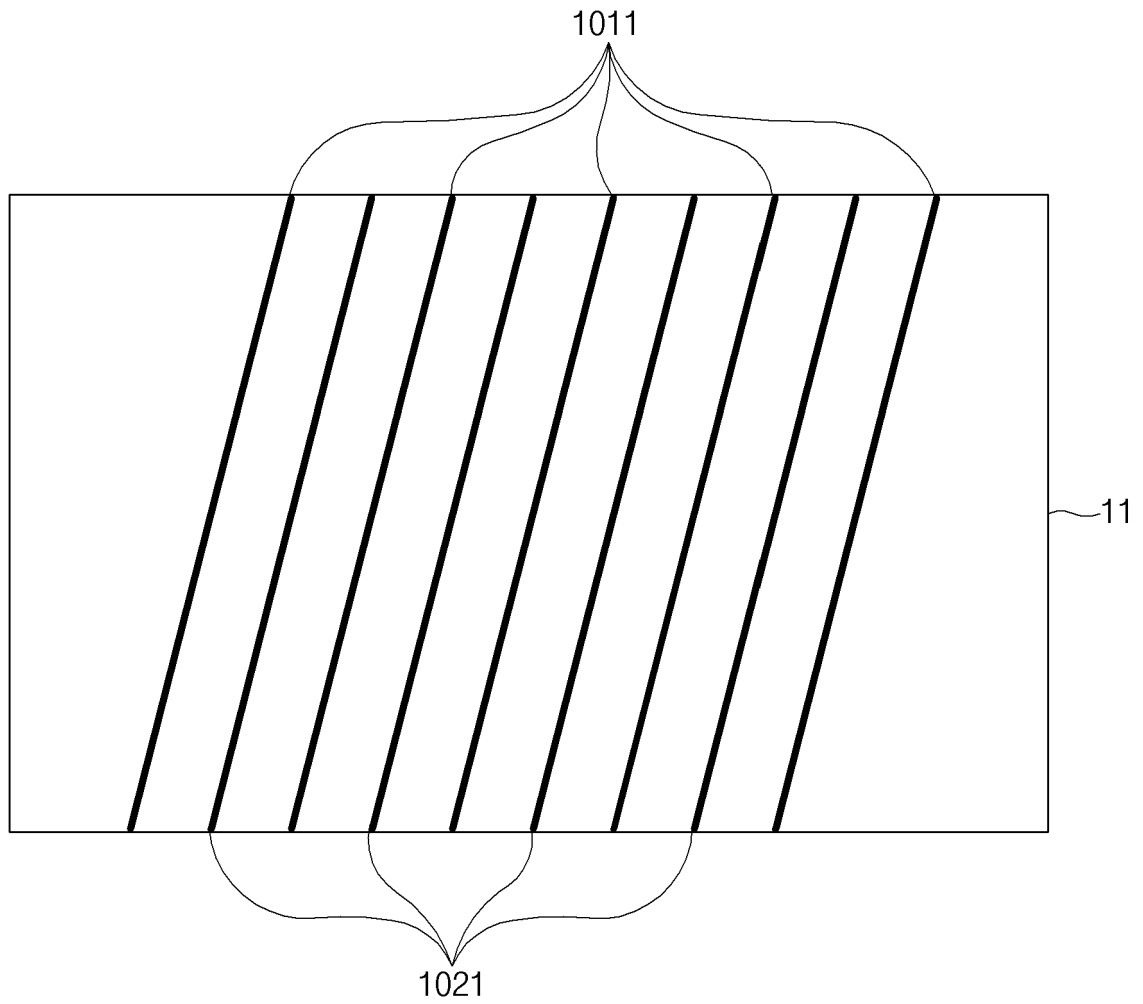


FIG.4

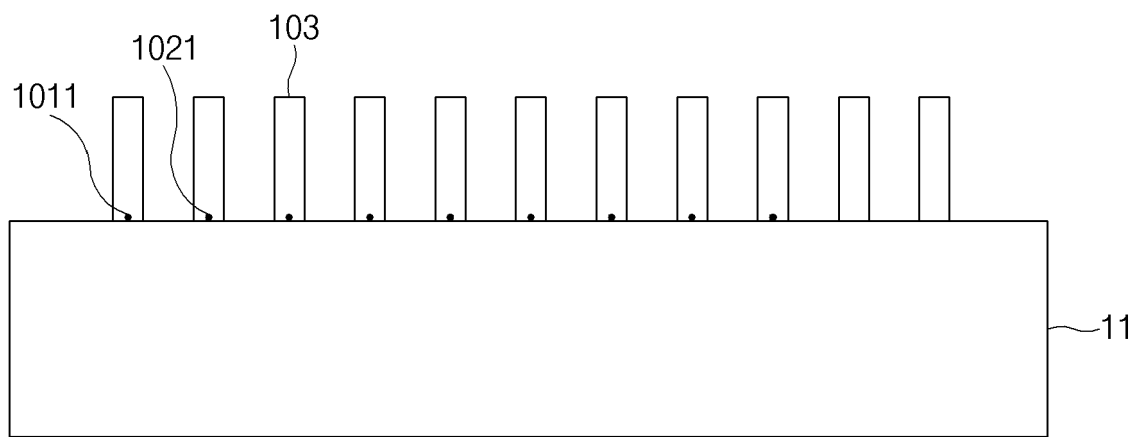


FIG.5

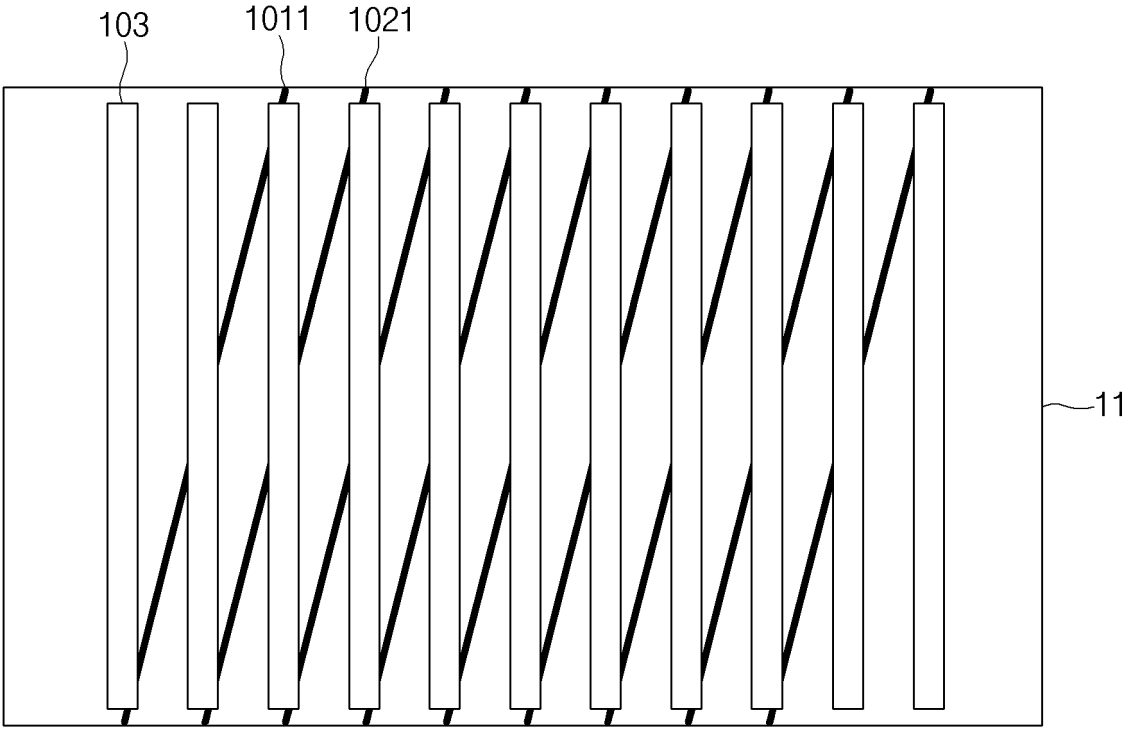


FIG.6

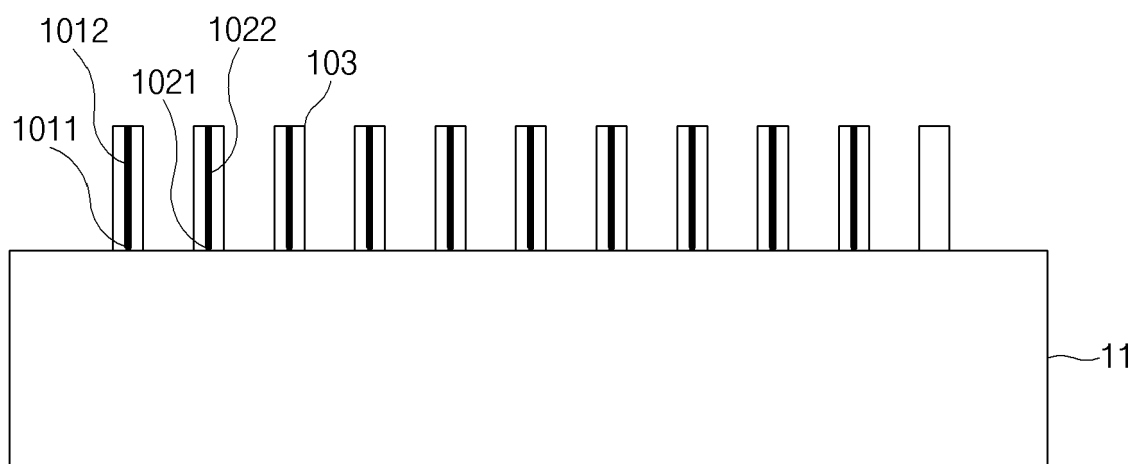


FIG.7

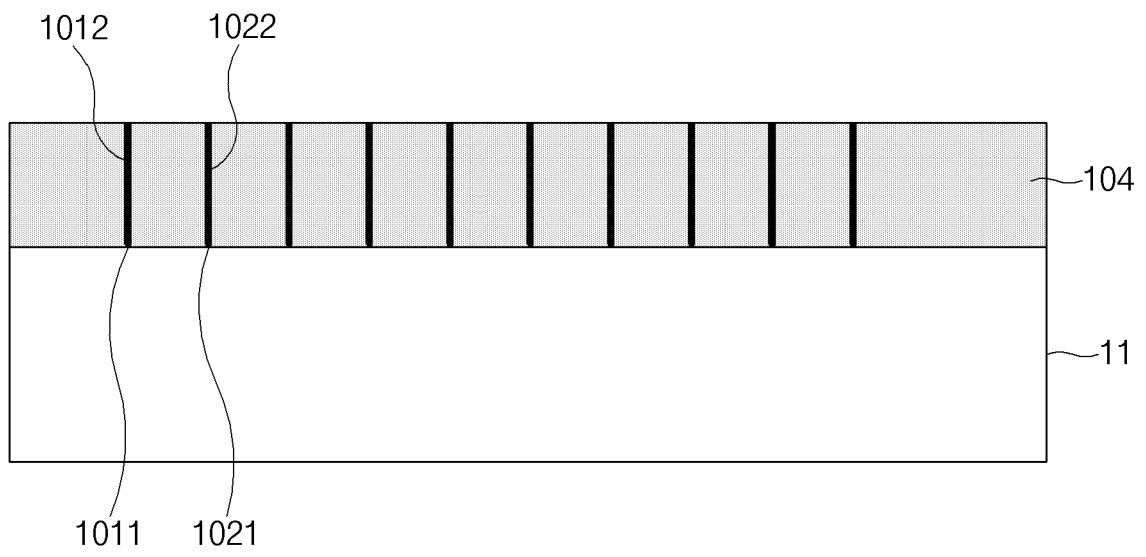


FIG.8

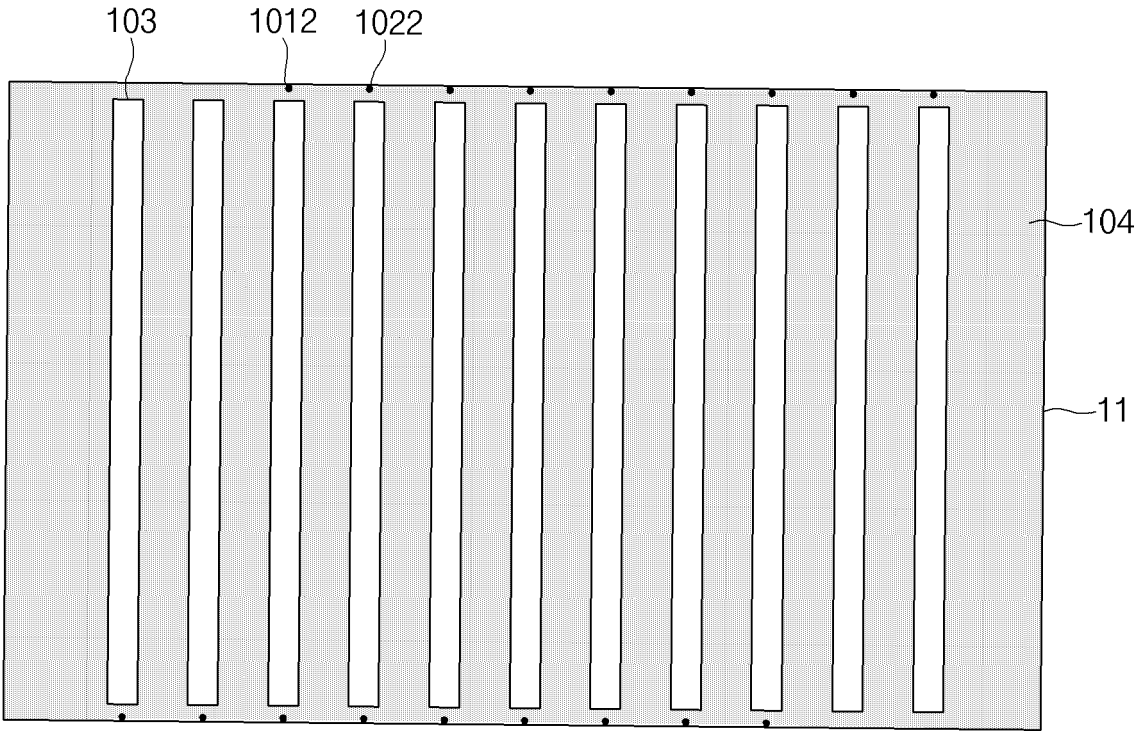


FIG.9

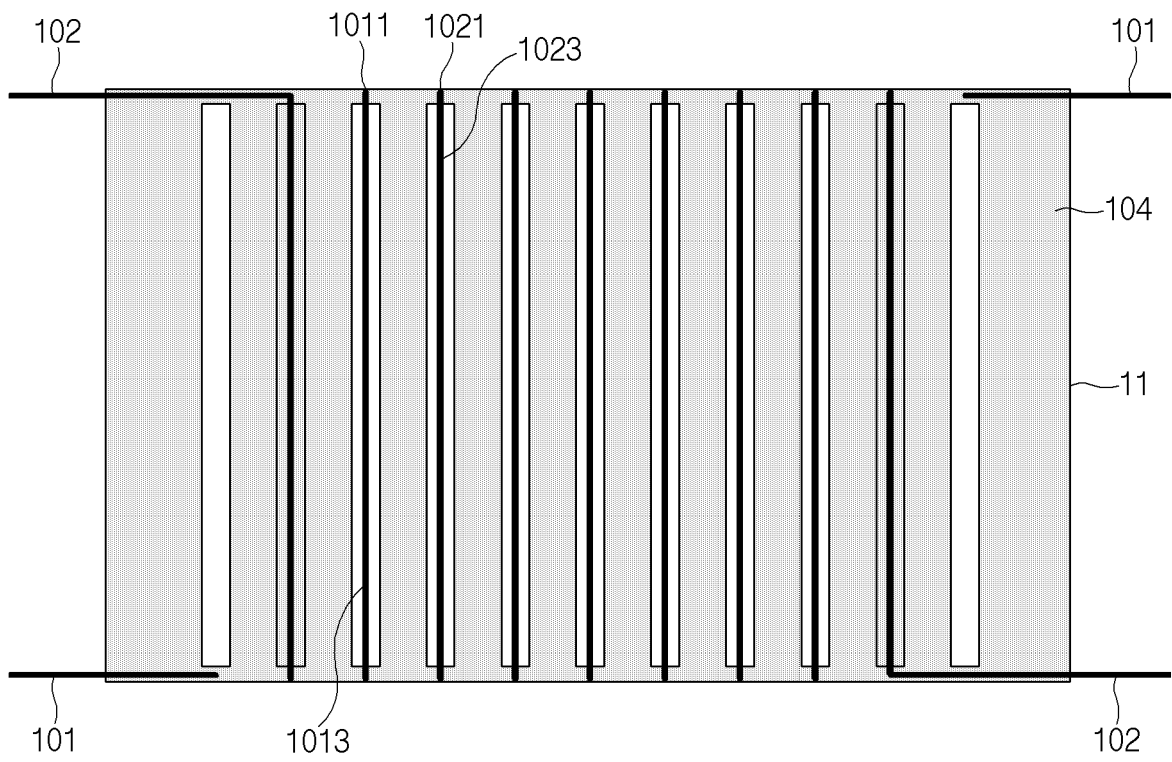


FIG.10

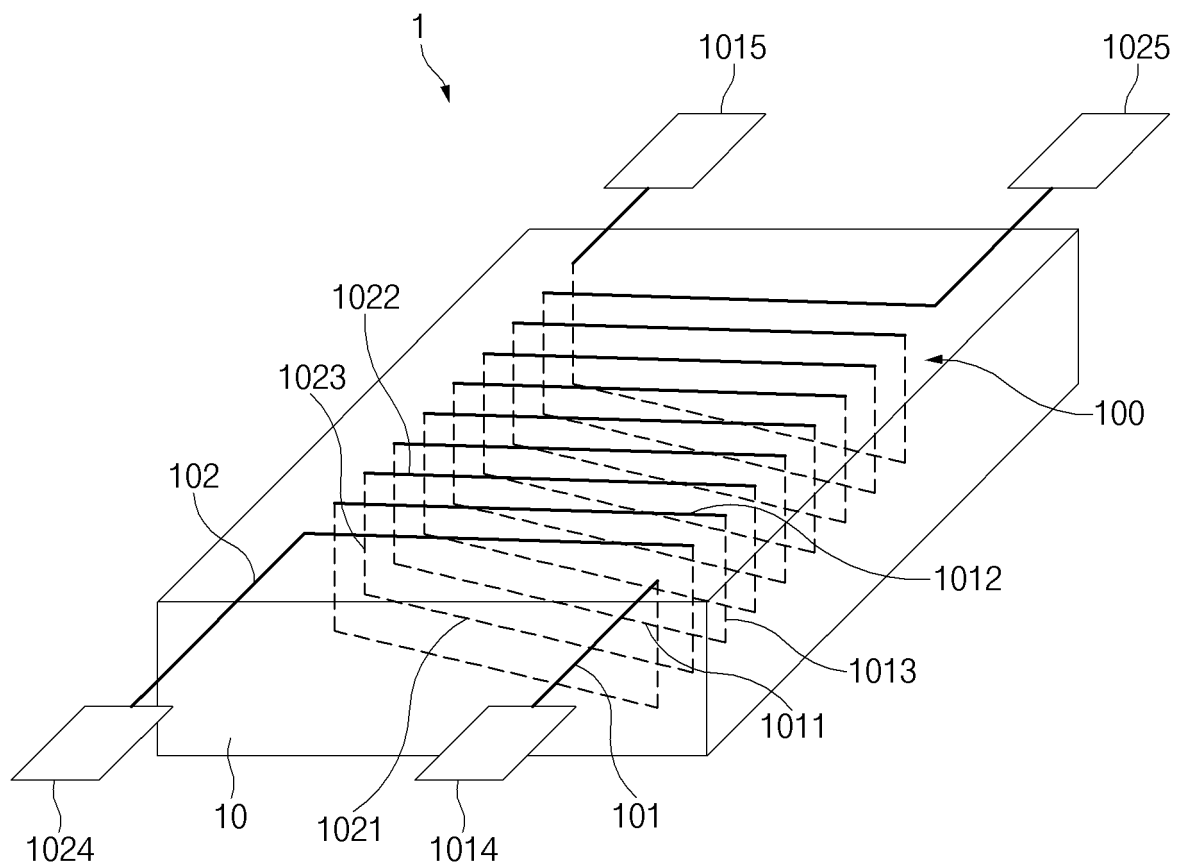


FIG.11

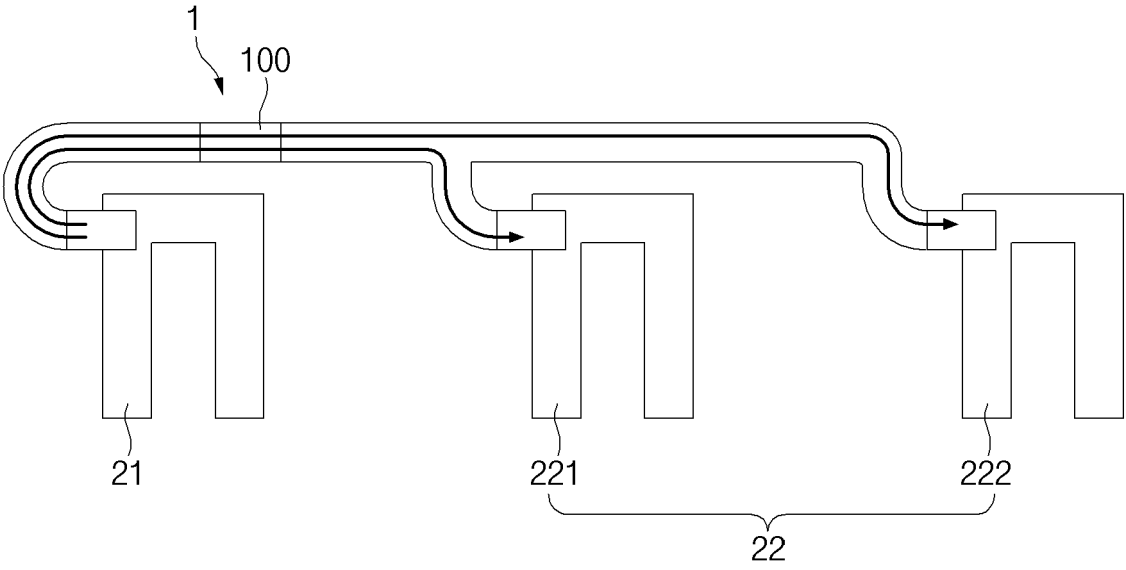


FIG.12

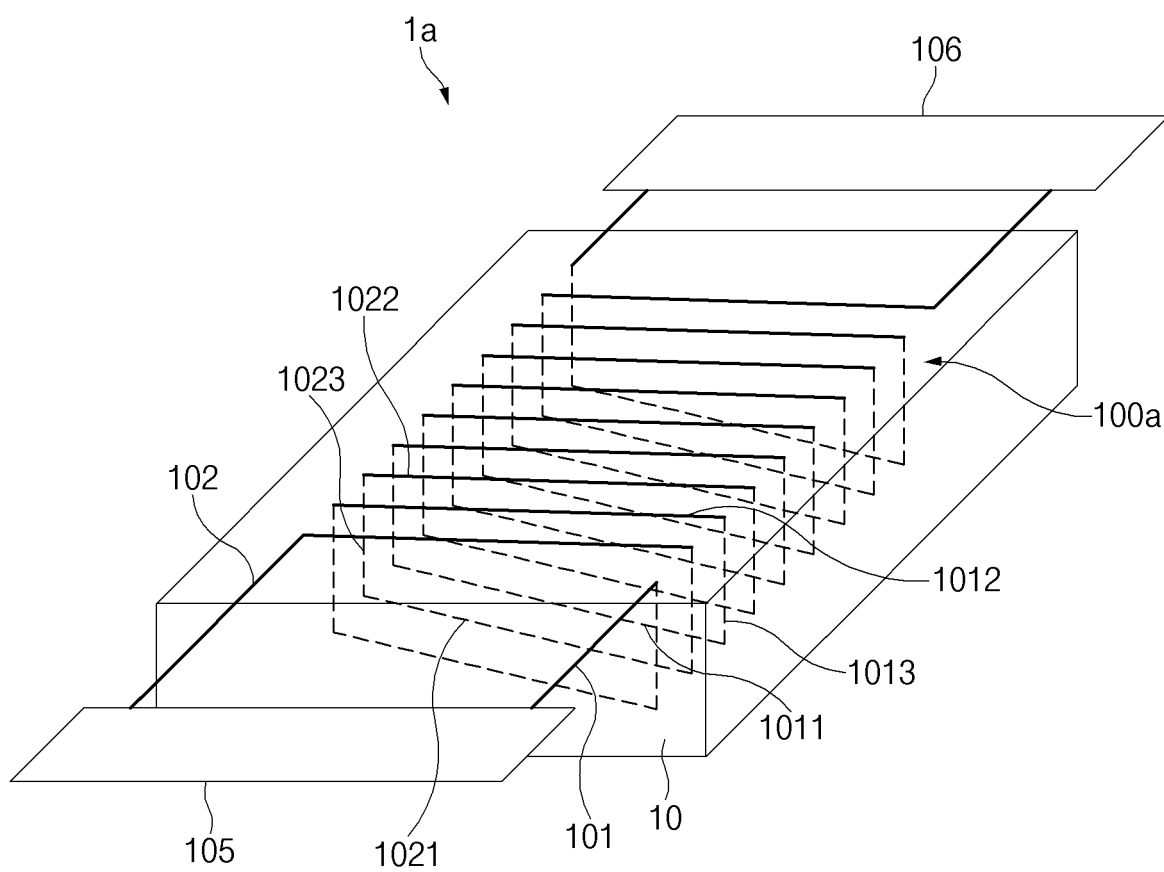


FIG. 13

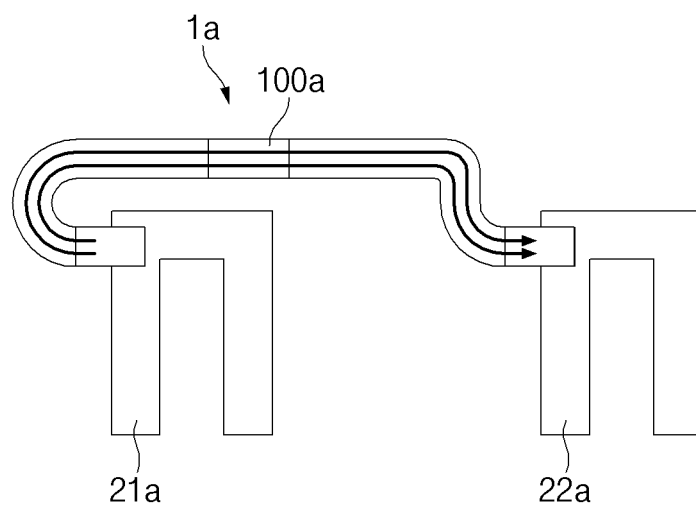


FIG.14

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020200094041 [0001]
- KR 1845714 [0006]
- US 5099219 A [0006]
- US 2019006141 A [0006]
- US 9854671 B [0006]