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(54) ELECTRONIC DEVICE

(57) An electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) is provided. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) includes a tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220) and a first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1111_2, 1211). The tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220) is electrically connected to a circuit node (N1, N2). The

first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1111_2, 1211) is electrically connected to the circuit node (N1, N2). The first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1111_2, 1211) includes a first control terminal and a first terminal. The first control terminal is electrically connected to the first terminal.

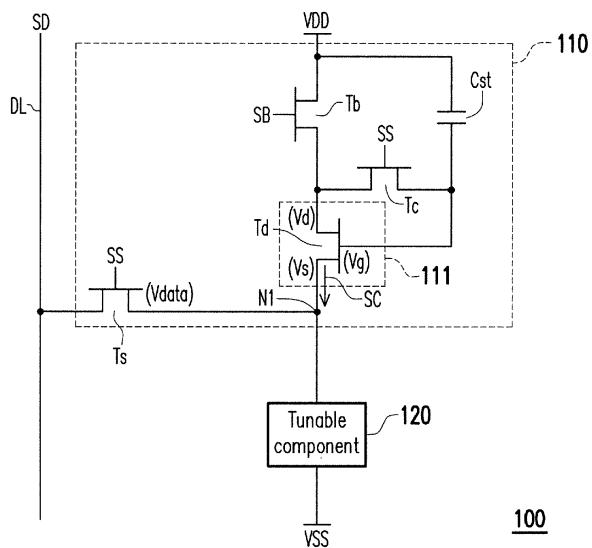


FIG. 1

Description**BACKGROUND**

Technical Field

[0001] The disclosure relates a device, particularly, the disclosure relates to an electronic device.

Description of Related Art

[0002] Antenna pixel circuit supplies a bias voltage to a varactor to control its permittivity with a storage capacitor (Cst). To keep the bias voltage within a specific range, the voltage needs to be restored (refresh) by data scan to compensate voltage drop by a leakage current of the varactor. However, there is a problem that higher leakage current requires higher refresh rates and/or larger storage capacitors to keep the bias voltage within a specific range, but which would be obstacles for commercialization.

SUMMARY

[0003] The electronic device of the disclosure includes a tunable component and a first source follower circuit. The tunable component is electrically connected to a circuit node. The first source follower circuit is electrically connected to the circuit node. The first source follower circuit includes a first control terminal and a first terminal. The first control terminal is electrically connected to the first terminal.

[0004] Based on the above, according to the electronic device of the disclosure, the electronic device can effectively compensate the leakage current of the tunable component.

[0005] To make the aforementioned more comprehensible, several embodiments accompanied with drawings are described in detail as follows.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The accompanying drawings are included to provide a further understanding of the disclosure, and are incorporated in and constitute a part of this specification. The drawings illustrate exemplary embodiments of the disclosure and, together with the description, serve to explain the principles of the disclosure.

FIG. 1 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 2 is a timing diagram of related voltages and signals according to the embodiment of FIG. 1 of the disclosure.

FIG. 3 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 4 is a timing diagram of related voltages and signals according to the embodiment of FIG. 3 of the disclosure.

FIG. 5 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 6 is a timing diagram of related voltages and signals according to the embodiment of FIG. 5 of the disclosure.

FIG. 7 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 8 is a timing diagram of related voltages and signals according to the embodiment of FIG. 7 of the disclosure.

FIG. 9 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 10 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 11 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 12 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

FIG. 13 is a timing diagram of related voltages and signals according to the embodiment of FIG. 12 of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

[0007] Reference will now be made in detail to the exemplary embodiments of the disclosure, examples of which are illustrated in the accompanying drawings.

40 Whenever possible, the same reference numbers are used in the drawings and the description to refer to the same or like components.

[0008] Certain terms are used throughout the specification and appended claims of the disclosure to refer to

45 specific components. Those skilled in the art should understand that electronic device manufacturers may refer to the same components by different names. This article does not intend to distinguish those components with the same function but different names.

In the following description and rights request, the words such as "comprise" and "include" are open-ended terms, and should be explained as "including but not limited to...".

[0009] The term "coupling (or electrically connection)" used throughout the whole specification of the present application (including the appended claims) may refer to any direct or indirect connection means. For example, if the text describes that a first device is coupled (or connected) to a second device, it should be interpreted that

the first device may be directly connected to the second device, or the first device may be indirectly connected through other devices or certain connection means to be connected to the second device. The terms "first", "second", and similar terms mentioned throughout the whole specification of the present application (including the appended claims) are merely used to name discrete elements or to differentiate among different embodiments or ranges. Therefore, the terms should not be regarded as limiting an upper limit or a lower limit of the quantity of the elements and should not be used to limit the arrangement sequence of elements. In addition, wherever possible, elements/components/steps using the same reference numerals in the drawings and the embodiments represent the same or similar parts. Reference may be mutually made to related descriptions of elements/components/steps using the same reference numerals or using the same terms in different embodiments.

[0010] The electronic device of the disclosure may include, for example, an antenna pixel circuit, and the tunable component may correspond to an antenna unit of one pixel of the antenna pixel. The tunable component of the disclosure may be a voltage-controlled device, and the voltage-controlled device may include, for example, a varactor, a resistor, an inductor or a capacitor. In the embodiment of the disclosure, the constant voltage source circuit of the disclosure may provide a voltage that can be efficiently restored (refreshed) through data scanning to compensate for the voltage drop caused by the leakage current of the varactor of the tunable component.

[0011] It should be noted that in the following embodiments, the technical features of several different embodiments may be replaced, recombined, and mixed without departing from the spirit of the disclosure to complete other embodiments. As long as the features of each embodiment do not violate the spirit of the disclosure or conflict with each other, they may be mixed and used together arbitrarily.

[0012] FIG. 1 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 1, the electronic device 100 includes a constant voltage source circuit 110, a tunable component 120 and a data line DL. The constant voltage source circuit 110 is electrically connected to the tunable component 120 and the data line DL. In the embodiment of the disclosure, the constant voltage source circuit 110 includes a source follower circuit 111, a compensation transistor Tc, a bias transistor Tb, a scan transistor Ts and a storage capacitor Cst, and the source follower circuit 111 includes a drive transistor Td. In the embodiment of the disclosure, the drive transistor Td, the compensation transistor Tc, the bias transistor Tb and the scan transistor Ts are N-type transistors, such as a N-type metal oxide semiconductor (NMOS). In the embodiment of the disclosure, a first terminal of the drive transistor Td is electrically connected to a first terminal of the compensation transistor Tc. A control terminal of the drive trans-

sistor Td is electrically connected to a second terminal of the compensation transistor Tc. A second terminal of the drive transistor Td is electrically connected to a circuit node N1. A first terminal of the bias transistor Tb is electrically connected to an operation voltage VDD. A second terminal of the bias transistor Tb is electrically connected to the first terminal of the drive transistor Td. A first terminal of the storage capacitor Cst is electrically connected to the operation voltage VDD, and a second terminal

5 of the storage capacitor Cst is electrically connected to the second terminal of the compensation transistor Tc and the control terminal of the drive transistor Td. In one embodiment of the disclosure, the second terminal of the storage capacitor Cst may electrically connected to a reference voltage. A first terminal of the scan transistor Ts is electrically connected to the data line DL. A second terminal of the scan transistor Ts is electrically connected to the circuit node N1. The tunable component 120 is electrically connected between the circuit node N1 and 10 the voltage VSS. In the embodiment of the disclosure, the voltage VDD may greater than the voltage VSS.

[0013] In the embodiment of the disclosure, the drive transistor Td may be operated as a source follower amplifier. The compensation transistor Tc is configured to 15 let the drive transistor Td to form a diode unit when the compensation transistor Tc is turned on. The bias transistor Tb is configured to provide the driving voltage (e.g., the operation voltage VDD) to the drive transistor Td when the bias transistor Tb is turned on. The storage capacitor Cst is configured to hold the voltage for the 20 control terminal of the drive transistor Td. In the embodiment of the disclosure, a control terminal of the compensation transistor Tc and a control terminal of the scan transistor Ts may receive a scan signal SS. A control 25 terminal of the bias transistor Tb may receive a bias signal SB. The data line DL may transmit a data signal SD. In the embodiment of the disclosure, the first terminal of the drive transistor Td may be, for example, a drain electrode of the transistor. The second terminal of the drive transistor Td may be, for example, a source electrode of the 30 transistor. The control terminal of each transistor in the embodiment may be, for example, a gate electrode of the transistor.

[0014] In the embodiment of the disclosure, the constant voltage source circuit 110 may effectively and automatically compensate the leakage current of the tunable component 120, and at the same time, the threshold voltage Vth of the driving transistor Td may also be compensated, so that the bias voltage (Vbias) of the tunable component 120 may be effectively maintained.

[0015] FIG. 2 is a timing diagram of related voltages and signals according to the embodiment of FIG. 1 of the disclosure. Referring to FIG. 1 and FIG. 2, during a reset period PR from time t1 to time t2, the bias transistor Tb, the scan transistor Ts and the compensation transistor Tc are turned on by the bias signal SB and the scan signal SS with a high voltage level, so that the first terminal and the control terminal of the drive transistor Td receive the

operation voltage VDD. The voltage V_d of the first terminal and the voltage V_g of the control terminal of the drive transistor T_d may be the operation voltage VDD. Thus, the drive transistor T_d is operated in a conducting state like a diode unit, so that the voltage V_s of the second terminal of the drive transistor T_d may equal to the operation voltage VDD minus the threshold voltage $|V_{th}|$ of the drive transistor T_d .

[0016] During a scan period PS from time t_2 to time t_3 , the bias transistor T_b is turned off by the bias signal S_B with a low voltage level, and the scan transistor T_s and the compensation transistor T_c are turned on by the scan signal S_S with the high voltage level, so that the drive transistor T_d is operated as a diode unit. The data line D_L may provide the data signal S_D to the scan transistor T_s which is turned on, so the voltage V_s of the second terminal of the drive transistor T_d may be a data voltage V_{data} . At the same time, due to the operation voltage VDD is higher than the data voltage V_{data} ($VDD > V_{data} > V_{SS}$), a current may be transmitted from the control terminal of the drive transistor T_d to the second terminal of the drive transistor T_d through the compensation transistor T_c . Thus, the drive transistor T_d is operated in a conducting state like a diode unit, so that the voltage V_g of control terminal of the drive transistor T_d may be a voltage of $V_{data} + |V_{th}|$, where V_{th} is a threshold voltage of the drive transistor T_d . Moreover, the voltage V_d of the first terminal of the drive transistor T_d may also be the voltage of $V_{data} + |V_{th}|$.

[0017] During a bias period P_B from time t_4 to time t_5 , the bias transistor T_b is turned on by the bias signal S_B with the high voltage level, and the scan transistor T_s and the compensation transistor T_c are turned off by the scan signal S_S with a low voltage level. Since the bias transistor T_b is turned on, the voltage V_d of the first terminal of the drive transistor T_d may be the operation voltage VDD. The voltage V_g of control terminal of the drive transistor T_d may be maintained the voltage of $V_{data} + |V_{th}|$. The voltage V_s of the second terminal of the drive transistor T_d may be the data voltage V_{data} . At the same time, the tunable component 120 is operated in a working state, and the second terminal of the drive transistor T_d provides a source current S_C to the tunable component 120 according to the operation voltage VDD. It should be noted that, when the tunable component 120 occurs a leakage current, a bias voltage (V_{bias}) of the tunable component 120 may drop ($V_{bias}-dV$), and the voltage V_s of the second terminal of the drive transistor T_d may also drop, where the symbol "dV" means a delta voltage. Therefore, the drive transistor T_d may provide more current to the tunable component 120 to compensate the leakage current of the tunable component 120, and at the same time, the threshold voltage V_{th} of the driving transistor T_d can be compensated, so that the bias voltage (V_{bias}) of the tunable component 120 may be effectively maintained during the bias period P_B .

[0018] FIG. 3 is a schematic diagram of an electronic device according to an embodiment of the disclosure.

Referring to FIG. 3, the electronic device 300 includes a constant voltage source circuit 310, a tunable component 320 and a data line D_L . The constant voltage source circuit 310 is electrically connected to the tunable component 320 and the data line D_L . In the embodiment of the disclosure, the constant voltage source circuit 310 includes a source follower circuit 311, a compensation transistor T_c , a bias transistor T_b , a scan transistor T_s , a reset transistor T_r and a storage capacitor C_{st} , and the source follower circuit 311 includes a drive transistor T_d . In the embodiment of the disclosure, the drive transistor T_d , the compensation transistor T_c , the bias transistor T_b , the scan transistor T_s and the reset transistor T_r are N-type transistors, such as a NMOS. In the embodiment of the disclosure, a first terminal of the drive transistor T_d is electrically connected to a first terminal of the compensation transistor T_c . A control terminal of the drive transistor T_d is electrically connected to a second terminal of the compensation transistor T_c . A second terminal of the drive transistor T_d is electrically connected to a circuit node N_1 . A first terminal of the bias transistor T_b is electrically connected to an operation voltage VDD. A second terminal of the bias transistor T_b is electrically connected to the first terminal of the drive transistor T_d . A first terminal of the storage capacitor C_{st} is electrically connected to the operation voltage VDD, and a second terminal of the storage capacitor C_{st} is electrically connected to the second terminal of the compensation transistor T_c and the control terminal of the drive transistor T_d . In one embodiment of the disclosure, the second terminal of the storage capacitor C_{st} may electrically connected to a reference voltage. A first terminal of the scan transistor T_s is electrically connected to the data line D_L . A second terminal of the scan transistor T_s is electrically connected to the circuit node N_1 . A first terminal of the reset transistor T_r is electrically connected to the operation voltage VDD. A second terminal of the reset transistor T_r is electrically connected to the control terminal of the drive transistor T_d . The tunable component 120 is electrically connected between the circuit node N_1 and the voltage V_{SS} .

[0019] In the embodiment of the disclosure, the drive transistor T_d may be operated as a source follower amplifier. The compensation transistor T_c is configured to let the drive transistor T_d to form a diode unit when the compensation transistor T_c is turned on. The bias transistor T_b is configured to provide a first operation voltage (e.g., the operation voltage VDD) to the drive transistor T_d when the bias transistor T_b is turned on. The storage capacitor C_{st} is configured to hold the voltage for the control terminal of the drive transistor T_d . The reset transistor T_r is configured to reset the voltage of the control terminal of the drive transistor T_d . In the embodiment of the disclosure, a control terminal of the compensation transistor T_c and a control terminal of the scan transistor T_s may receive a scan signal S_S . A control terminal of the bias transistor T_b may receive a bias signal S_B . A control terminal of the reset transistor T_r may receive a

reset signal SR. The data line DL may transmit a data signal SD.

[0020] In the embodiment of the disclosure, the constant voltage source circuit 310 may effectively and automatically compensate the leakage current of the tunable component 320, and at the same time, the threshold voltage V_{th} of the driving transistor T_d may also be compensated, so that the bias voltage (V_{bias}) of the tunable component 320 may be effectively maintained.

[0021] FIG. 4 is a timing diagram of related voltages and signals according to the embodiment of FIG. 3 of the disclosure. Referring to FIG. 3 and FIG. 4, during a reset period PR from time t_2 to time t_3 , the reset transistor T_r is turned on by the reset signal SR with a high voltage level, and the bias transistor T_b , the scan transistor T_s and the compensation transistor T_c are turned off by the bias signal SB and the scan signal SS with a low voltage level, so that the control terminal of the drive transistor T_d receive the operation voltage VDD, and the voltage V_d of the first terminal of the drive transistor T_d may be maintained at the operation voltage VDD from the previous bias period PB before the time t_1 . Moreover, the voltage V_s of the second terminal of the drive transistor T_d may be maintained at a voltage from the previous bias period PB before the time t_1 such as a data voltage V_{data} .

[0022] During a scan period PS from time t_4 to time t_5 , the reset transistor T_r and the bias transistor T_b are turned off by the bias signal SB and the reset signal SR with the low voltage level, and the scan transistor T_s and the compensation transistor T_c are turned on by the scan signal SS with the high voltage level, so that the drive transistor T_d is operated as a diode unit. The data line DL may provide the data signal SD to the scan transistor T_s which is turned on, so the voltage V_s of the second terminal of the drive transistor T_d may be the data voltage V_{data} . At the same time, due to the operation voltage VDD is higher than the data voltage V_{data} ($VDD > V_{data} > VSS$), a current may be transmitted from the control terminal of the drive transistor T_d to the second terminal of the drive transistor T_d through the compensation transistor T_c . Thus, the drive transistor T_d is operated in a conducting state like a diode unit, so that the voltage V_g of control terminal of the drive transistor T_d may be a voltage of $V_{data} + |V_{th}|$, where V_{th} is a threshold voltage of the drive transistor T_d . Moreover, the voltage V_d of the first terminal of the drive transistor T_d may also be the voltage of $V_{data} + |V_{th}|$.

[0023] During a bias period PB from time t_6 to time t_7 , the bias transistor T_b is turned on by the bias signal SB with the high voltage level, and the reset transistor T_r , the scan transistor T_s and the compensation transistor T_c are turned off by the reset signal SR and the scan signal SS with a low voltage level. Since the bias transistor T_b is turned on, the voltage V_d of the first terminal of the drive transistor T_d may be the operation voltage VDD. The voltage V_g of control terminal of the drive transistor T_d may be maintained the voltage of $V_{data} + |V_{th}|$. The voltage V_s of the second terminal of the drive trans-

sistor T_d may be the data voltage V_{data} . At the same time, the tunable component 320 is operated in a working state, and the second terminal of the drive transistor T_d provides a source current SC to the tunable component 320 according to the operation voltage VDD. It should be noted that, when the tunable component 320 occurs a leakage current, a bias voltage (V_{bias}) of the tunable component 120 may drop ($V_{bias}-dV$), and the voltage V_s of the second terminal of the drive transistor T_d may also drop. Therefore, the drive transistor T_d may provide more current to the tunable component 320 to compensate the leakage current of the tunable component 320, and at the same time, the threshold voltage V_{th} of the driving transistor T_d can be compensated, so that the bias voltage (V_{bias}) of the tunable component 320 may be effectively maintained during the bias period PB.

[0024] FIG. 5 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 5, the electronic device 500 includes a constant voltage source circuit 510, a tunable component 520 and a data line DL. The constant voltage source circuit 510 is electrically connected to the tunable component 520 and the data line DL. In the embodiment of the disclosure, the constant voltage source circuit 510 includes a source follower circuit 511, a compensation transistor T_c , a bias transistor T_b , a scan transistor T_s and a storage capacitor C_{st} , and the source follower circuit 511 includes a drive transistor T_d . In the embodiment of the disclosure, the drive transistor T_d , the compensation transistor T_c , the bias transistor T_b and the scan transistor T_s are P-type transistors, such as a P-type metal oxide semiconductor (PMOS). In the embodiment of the disclosure, a first terminal of the drive transistor T_d is electrically connected to a circuit node N2. A second terminal of the drive transistor T_d is electrically connected to a first terminal of the bias transistor T_b and a first terminal of the compensation transistor T_c . A control terminal of the drive transistor T_d is electrically connected to a second terminal of the compensation transistor T_c . A first terminal of the bias transistor T_b is electrically connected to the second terminal of the drive transistor T_d . A second terminal of the bias transistor T_b is electrically connected to a voltage VSS. A first terminal of the storage capacitor C_{st} is electrically connected to the control terminal of the drive transistor T_d and a second terminal of the compensation transistor T_c , and a second terminal of the storage capacitor C_{st} is electrically connected to the voltage VSS. In one embodiment of the disclosure, the second terminal of the storage capacitor C_{st} may be electrically connected to a reference voltage. A first terminal of the scan transistor T_s is electrically connected to the data line DL. A second terminal of the scan transistor T_s is electrically connected to the circuit node N2. The tunable component 120 is electrically connected between the circuit node N2 and the operation voltage VDD.

[0025] In the embodiment of the disclosure, the drive transistor T_d may be operated as a source follower amplifier. The compensation transistor T_c is configured to

let the drive transistor T_d to form a diode unit when the compensation transistor T_c is turned on. The bias transistor T_b is configured to provide a second operation voltage (e.g., voltage V_{SS}) to the drive transistor T_d when the bias transistor T_b is turned on. In the embodiment of the disclosure, the storage capacitor C_{st} is configured to hold the voltage for the control terminal of the drive transistor T_d . In the embodiment of the disclosure, a control terminal of the compensation transistor T_c and a control terminal of the scan transistor T_s may receive a scan signal $/SS$. A control terminal of the bias transistor T_b may receive a bias signal $/SB$. The data line DL may transmit a data signal SD . In the embodiment of the disclosure, the first terminal of the drive transistor T_d may be, for example, a source electrode of the transistor. The second terminal of the drive transistor T_d may be, for example, a drain electrode of the transistor. The control terminal of each transistor in the embodiment may be, for example, a gate electrode of the transistor.

[0026] In the embodiment of the disclosure, the constant voltage source circuit 510 may effectively and automatically compensate the leakage current of the tunable component 520 , and at the same time, the threshold voltage V_{th} of the driving transistor T_d may also be compensated, so that the bias voltage (V_{bias}) of the tunable component 520 may be effectively maintained.

[0027] FIG. 6 is a timing diagram of related voltages and signals according to the embodiment of FIG. 5 of the disclosure. Referring to FIG. 5 and FIG. 6, during a reset period PR from time t_1 to time t_2 , the bias transistor T_b , the scan transistor T_s and the compensation transistor T_c are turned on by the bias signal $/SB$ and the scan signal $/SS$ with a low voltage level, so that the second terminal and the control terminal of the drive transistor T_d receive the voltage V_{SS} . The voltage V_d of the second terminal and the voltage V_g of the control terminal of the drive transistor T_d may be the voltage V_{SS} . Thus, the drive transistor T_d is operated in a conducting state like a diode unit, so that the voltage V_s of the first terminal of the drive transistor T_d may equal to the voltage V_{SS} plus an absolute value of a threshold voltage ($|V_{th}|$) of the drive transistor T_d .

[0028] During a scan period PS from time t_2 to time t_3 , the bias transistor T_b is turned off by the bias signal $/SB$ with a high voltage level, and the scan transistor T_s and the compensation transistor T_c are turned on by the scan signal $/SS$ with the low voltage level, so that the drive transistor T_d is operated as a diode unit. The data line DL may provide the data signal SD to the scan transistor T_s which is turned on, so the voltage V_s of the first terminal of the drive transistor T_d may be a data voltage V_{data} . At the same time, due to the data voltage V_{data} is higher than ($V_{DD} > V_{data} > V_{SS}$) the voltage V_{SS} , a current may be transmitted from the first terminal of the drive transistor T_d to the control terminal of the drive transistor T_d through the compensation transistor T_c . Thus, the drive transistor T_d is operated in a conducting state like a diode unit, so that the voltage V_g of control terminal

of the drive transistor T_d may be a voltage of $V_{data} - |V_{th}|$, where V_{th} is a threshold voltage of the drive transistor T_d . Moreover, the voltage V_d of the second terminal of the drive transistor T_d may also be the voltage of $V_{data} - |V_{th}|$.

[0029] During a bias period PB from time t_4 to time t_5 , the bias transistor T_b is turned on by the bias signal $/SB$ with the low voltage level, and the scan transistor T_s and the compensation transistor T_c are turned off by the scan signal $/SS$ with a high voltage level. Since the bias transistor T_b is turned on, the voltage V_d of the second terminal of the drive transistor T_d may be the voltage V_{SS} . The voltage V_g of control terminal of the drive transistor T_d may be maintained the voltage of $V_{data} - |V_{th}|$. The voltage V_s of the second terminal of the drive transistor T_d may be the data voltage V_{data} . At the same time, the tunable component 520 is operated in a working state, and the first terminal of the drive transistor T_d generates a sink current SC from the tunable component 520 . It should be noted that, when the tunable component 520 occurs a leakage current, a bias voltage (V_{bias}) of the tunable component 520 may increase ($V_{bias}+dV$), and the voltage V_s of the second terminal of the drive transistor T_d may also increase. Therefore, the drive transistor T_d may generate more current to the voltage V_{SS} through the bias transistor T_b , so that the leakage current of the tunable component 520 may be compensate automatically. At the same time, the threshold voltage V_{th} of the driving transistor T_d can be compensated, so that the bias voltage (V_{bias}) of the tunable component 520 may be effectively maintained during the bias period PB .

[0030] FIG. 7 is a schematic diagram of an electronic device according to an embodiment of the disclosure. FIG. 7 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 7, the electronic device 700 includes a constant voltage source circuit 710 , a tunable component 720 and a data line DL . The constant voltage source circuit 710 is electrically connected to the tunable component 720 and the data line DL . In the embodiment of the disclosure, the constant voltage source circuit 710 includes a source follower circuit 711 , a compensation transistor T_c , a bias transistor T_b , a scan transistor T_s , a reset transistor T_r and a storage capacitor C_{st} , and the source follower circuit 711 includes a drive transistor T_d . In the embodiment of the disclosure, the drive transistor T_d , the compensation transistor T_c , the bias transistor T_b , the scan transistor T_s and the reset transistor T_r are P-type transistors, such as a PMOS. In the embodiment of the disclosure, a first terminal of the drive transistor T_d is electrically connected to a circuit node $N2$. A second terminal of the drive transistor T_d is electrically connected to a first terminal of the bias transistor T_b and the first terminal of compensation transistor T_r . A control terminal of the drive transistor T_d is electrically connected to a second terminal of the compensation transistor T_c . A first terminal of the bias transistor T_b is electrically connected to the second terminal of the drive transistor T_d . A second terminal

of the bias transistor Tb is electrically connected to a voltage VSS. A first terminal of the storage capacitor Cst is electrically connected to the control terminal of the drive transistor Td and a second terminal of the compensation transistor Tc, and a second terminal of the storage capacitor Cst is electrically connected to the voltage VSS. In one embodiment of the disclosure, the second terminal of the storage capacitor Cst may electrically connected to a reference voltage. A first terminal of the scan transistor Ts is electrically connected to the data line DL. A second terminal of the scan transistor Ts is electrically connected to the circuit node N2. A first terminal of the reset transistor Tr is electrically connected to control terminal of the drive transistor Td. A second terminal of the reset transistor Tr is electrically connected to the voltage VSS and the second terminal of the bias transistor Tb. The tunable component 720 is electrically connected between the circuit node N2 and the operation voltage VDD.

[0031] In the embodiment of the disclosure, the drive transistor Td may be operated as a source follower amplifier. The compensation transistor Tc is configured to let the drive transistor Td to form a diode unit when the compensation transistor Tc is turned on. The bias transistor Tb is configured to provide a second operation voltage (e.g., the voltage VSS) to the drive transistor Td when the bias transistor Tb is turned on. The storage capacitor Cst is configured to hold the voltage for the control terminal of the drive transistor Td. The reset transistor Tr is configured to reset the voltage of the control terminal of the driver transistor Td. In the embodiment of the disclosure, a control terminal of the compensation transistor Tc and a control terminal of the scan transistor Ts may receive a scan signal /SS. A control terminal of the bias transistor Tb may receive a bias signal /SB. A control terminal of the reset transistor Tr may receive a reset signal /SR. The data line DL may transmit a data signal SD.

[0032] In the embodiment of the disclosure, the constant voltage source circuit 710 may effectively and automatically compensate the leakage current of the tunable component 720, and at the same time, the threshold voltage Vth of the driving transistor Td may also be compensated, so that the bias voltage (Vbias) of the tunable component 720 may be effectively maintained.

[0033] FIG. 8 is a timing diagram of related voltages and signals according to the embodiment of FIG. 7 of the disclosure. Referring to FIG. 7 and FIG. 8, during a reset period PR from time t2 to time t3, the reset transistor Tr is turned on by the reset signal /SR with a low voltage level, and the bias transistor Tb, the scan transistor Ts and the compensation transistor Tc are turned off by the bias signal /SB and the scan signal /SS with a high voltage level, so that the control terminal of the drive transistor Td receive the voltage VSS., and the voltage Vd of the first terminal of the drive transistor Td may be maintained at the voltage VSS from the previous bias period PB before the time t1. Moreover, the voltage Vs of the first terminal of the drive transistor Td may be maintained at a

voltage from the previous bias period PB before the time t1 such as a data voltage Vdata.

[0034] During a scan period PS from time t4 to time t5, the reset transistor Tr and the bias transistor Tb are turned off by the bias signal /SB and the reset signal /SR with the high voltage level, and the scan transistor Ts and the compensation transistor Tc are turned on by the scan signal /SS with the low voltage level, so that the drive transistor Td is operated as a diode unit. The data line DL may provide the data signal SD to the scan transistor Ts which is turned on, so the voltage Vs of the second terminal of the drive transistor Td may be a data voltage Vdata. At the same time, due to the data voltage Vdata is higher than the ground voltage VSS ($VDD > Vdata > VSS$), a current may be transmitted from the first terminal of the drive transistor Td to the control terminal of the drive transistor Td through the compensation transistor Tc. Thus, the drive transistor Td is operated in a conducting state like a diode unit, so that the voltage Vg of control terminal of the drive transistor Td may be a voltage of $Vdata - |Vth|$, where Vth is a threshold voltage of the drive transistor Td. Moreover, the voltage Vd of the first terminal of the drive transistor Td may also be the voltage of $Vdata - |Vth|$.

[0035] During a bias period PB from time t6 to time t7, the bias transistor Tb is turned on by the bias signal /SB with the low voltage level, and the reset transistor Tr, the scan transistor Ts and the compensation transistor Tc are turned off by the reset signal SR and the scan signal SS with the high voltage level. Since the bias transistor Tb is turned on, the voltage Vd of the first terminal of the drive transistor Td may be the voltage VSS. The voltage Vg of control terminal of the drive transistor Td may be maintained the voltage of $Vdata - |Vth|$. The voltage Vs of the first terminal of the drive transistor Td may be the data voltage Vdata. At the same time, the tunable component 720 is operated in a working state, and the first terminal of the drive transistor Td generates a sink current SC from the tunable component 720. It should be noted that, when the tunable component 720 occurs a leakage current, a bias voltage (Vbias) of the tunable component 720 may increase ($Vbias + dV$), and the voltage Vs of the first terminal of the drive transistor Td may also increase. Therefore, the drive transistor Td may generate more current to the voltage VSS through the bias transistor Tb, so that the leakage current of the tunable component 720 may be compensate automatically. At the same time, the threshold voltage Vth of the driving transistor Td can be compensated, so that the bias voltage (Vbias) of the tunable component 720 may be effectively maintained during the bias period PB.

[0036] FIG. 9 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 9, the electronic device 900 includes a constant voltage source circuit 910, a tunable component 920 and a data line DL. The constant voltage source circuit 910 is electrically connected to the tunable component 920 and the data line DL. In the embodiment of the

disclosure, the constant voltage source circuit 910 includes a source follower circuit 911, a compensation transistor Tc, a bias transistor Tb, a scan transistor Ts, a storage capacitor Cst and an input capacitor Cin, and the source follower circuit 911 includes a drive transistor Td. In the embodiment of the disclosure, the drive transistor Td, the compensation transistor Tc, the bias transistor Tb and the scan transistor Ts are N-type transistors, such as a NMOS. In the embodiment of the disclosure, a first terminal of the drive transistor Td is electrically connected to a first terminal of the compensation transistor Tc. A control terminal of the drive transistor Td is electrically connected to a second terminal of the compensation transistor Tc. A second terminal of the drive transistor Td is electrically connected to a circuit node N1. A first terminal of the bias transistor Tb is electrically connected to an operation voltage VDD. A second terminal of the bias transistor Tb is electrically connected to the first terminal of the drive transistor Td. A first terminal of the storage capacitor Cst is electrically connected to the operation voltage VDD, and a second terminal of the storage capacitor Cst is electrically connected to the second terminal of the compensation transistor Tc and the control terminal of the drive transistor Td. In one embodiment of the disclosure, the second terminal of the storage capacitor Cst may electrically connected to a reference voltage. A first terminal of the scan transistor Ts is electrically connected to the data line DL. A second terminal of the scan transistor Ts is electrically connected to the circuit node N1. The tunable component 920 is electrically connected between the circuit node N1 and the voltage VSS. A first terminal of the input capacitor Cin is electrically connected to the circuit node N1. A second terminal of the input capacitor Cin is electrically connected to a radio frequency input node N3.

[0037] In the embodiment of the disclosure, the drive transistor Td may be operated as a source follower amplifier. The compensation transistor Tc is configured to let the drive transistor Td to form a diode unit when the compensation transistor Tc is turned on. The bias transistor Tb is configured to provide a first operation voltage (e.g., the operation voltage VDD) to the drive transistor Td when the bias transistor Tb is turned on. In the embodiment of the disclosure, the storage capacitor Cst is configured to hold the voltage for the control terminal of the drive transistor Td. In the embodiment of the disclosure, a control terminal of the compensation transistor Tc and a control terminal of the scan transistor Ts may receive a scan signal SS. A control terminal of the bias transistor Tb may receive a bias signal SB. A radio frequency signal RF-in is transmitted from the radio frequency input node N3 to the circuit node N1.

[0038] In the embodiment of the disclosure, the transistors of the electronic device 900 may operate according to the embodiment of FIG. 2. In the embodiment of the disclosure, the input node N3 may receive the radio frequency signal RF-in (AC signal) during the bias period PB, so that the radio frequency signal RF-in may be mod-

ulated with the voltage Vdata (DC bias voltage) of the circuit node N1 with capacitive coupling with the input capacitor Cin to generate a modulated signal (DC+AC) to the tunable component 920. In the embodiment of the disclosure, the constant voltage source circuit 910 may effectively and automatically compensate the leakage current of the tunable component 920, and at the same time, the threshold voltage Vth of the driving transistor Td may also be compensated, so that the bias voltage (Vbias) of the tunable component 920 may be effectively maintained.

[0039] FIG. 10 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 10, the electronic device 1000 includes a constant voltage source circuit 1010, a tunable component 1020, a bias transistor TbB, a smoothing capacitor Cs, a reset transistor TrB and a data line DL. The constant voltage source circuit 1010 is electrically connected to the tunable component 1020 and the data line DL. In the embodiment of the disclosure, the constant voltage source circuit 1010 includes a source follower circuit 1011, a compensation transistor Tc, a bias transistor TbA, a scan transistor Ts, a reset transistor TrA and a storage capacitor Cst, and the source follower circuit 1011 includes a drive transistor Td. In the embodiment of the disclosure, the drive transistor Td, the compensation transistor Tc, the bias transistor TbA, the bias transistor TbB, the scan transistor Ts, the reset transistor TrA and the reset transistor TrB are N-type transistors, such as a NMOS. In the embodiment of the disclosure, a first terminal of the drive transistor Td is electrically connected to a first terminal of the compensation transistor Tc. A control terminal of the drive transistor Td is electrically connected to a second terminal of the compensation transistor Tc. A second terminal of the drive transistor Td is electrically connected to a circuit node N1. A first terminal of the bias transistor TbA is electrically connected to an operation voltage VDD. A second terminal of the bias transistor TbA is electrically connected to the first terminal of the drive transistor Td. A first terminal of the storage capacitor Cst is electrically connected to the operation voltage VDD, and a second terminal of the storage capacitor Cst is electrically connected to the second terminal of the compensation transistor Tc and the control terminal of the drive transistor Td. In one embodiment of the disclosure, the second terminal of the storage capacitor Cst may electrically connected to a reference voltage. A first terminal of the scan transistor Ts is electrically connected to the data line DL. A second terminal of the scan transistor Ts is electrically connected to the circuit node N1. A first terminal of the reset transistor TrA is electrically connected to the operation voltage VDD. A second terminal of the reset transistor TrA is electrically connected to the control terminal of the drive transistor Td. A first terminal of the bias transistor TbB is electrically connected to the circuit node N1. The second terminal of the bias transistor TbB is electrically connected to the tunable component 1020. The tunable compo-

ment 1020 is electrically connected between the second terminal of the bias transistor TbB and the voltage VSS. The smoothing capacitor Cs is electrically connected to the tunable component 1020 in parallel. The reset transistor TrB is electrically connected to the tunable component 1020 in parallel.

[0040] In the embodiment of the disclosure, the drive transistor Td may be operated as a source follower amplifier. The compensation transistor Tc is configured to let the drive transistor Td to form a diode unit when the compensation transistor Tc is turned on. The bias transistor TbA and the bias transistor TbB are configured to provide a first operation voltage (e.g., the operation voltage VDD) to the tunable component 1020 through the drive transistor Td when the bias transistor TbA and the bias transistor TbB are turned on. The reset transistor TrA is configured to reset the voltage of the control terminal of the drive transistor Td. The reset transistor TrB is configured to reset the tunable component 1020. In the embodiment of the disclosure, the storage capacitor Cst is configured to hold the voltage for the control terminal of the drive transistor Td. In the embodiment of the disclosure, a control terminal of the compensation transistor Tc and a control terminal of the scan transistor Ts may receive a scan signal SS. A control terminal of the bias transistor TbA and a control terminal of the bias transistor TbB may receive a bias signal SB. A control terminal of the reset transistor TrA and a control terminal of the reset transistor TrB may receive a reset signal SR. The data line DL may transmit a data signal SD.

[0041] In the embodiment of the disclosure, the transistors of the electronic device 1000 may operate according to the embodiment of FIG. 4. In the embodiment of the disclosure, the bias transistor TbB may be adapted to cut off the leakage current from the tunable component 1020 during the reset period PR and the scan period PS. The reset transistor TrB may be adapted to reset the bias voltage of the tunable component 1020 during the reset period PR. The smoothing capacitor Cs may be adapted to suppress voltage fluctuation caused by fast leakage current changes and during reset and scan operation.

[0042] In the embodiment of the disclosure, the constant voltage source circuit 1010 may effectively and automatically compensate the leakage current of the tunable component 1020, and at the same time, the threshold voltage Vth of the driving transistor Td may also be compensated, so that the bias voltage (Vbias) of the tunable component 1020 may be effectively maintained.

[0043] FIG. 11 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 11, the electronic device 1100 includes a constant voltage source circuit 1110, a tunable component 1120 and a data line DL. The constant voltage source circuit 1110 is electrically connected to the tunable component 1120 and the data line DL. In the embodiment of the disclosure, the constant voltage source circuit 1110 includes a first source follower circuit 1111_1, a second source follower circuit 1111_2, a first compen-

sation transistor Tc1, a second compensation transistor Tc2, a first bias transistor Tb1, a second bias transistor Tb2, a scan transistor Ts, a first storage capacitor Cst1 and a second storage capacitor Cst2. The first source

5 follower circuit 1111_1 includes a first drive transistor Td1. The second source follower circuit 1111_2 includes a second drive transistor Td2. In the embodiment of the disclosure, the first drive transistor Td1, the first compensation transistor Tc1, the first bias transistor Tb1, the scan 10 transistor Ts, the second compensation transistor Tc2 and the second bias transistor Tb2 are N-type transistors, such as a NMOS. In the embodiment of the disclosure, the second drive transistor Td2 is a P-type transistor, such as a PMOS.

[0044] In the embodiment of the disclosure, a first terminal of the first drive transistor Td1 is electrically connected to a first terminal of the first compensation transistor Tc1. A control terminal of the first drive transistor Td is electrically connected to a second terminal of the

20 first compensation transistor Tc1. A second terminal of the first drive transistor Td1 is electrically connected to a circuit node N1. A first terminal of the first bias transistor Tb1 is electrically connected to an operation voltage VDD. A second terminal of the first bias transistor Tb1 is electrically connected to the first terminal of the first drive

25 transistor Td1. A first terminal of the first storage capacitor Cst1 is electrically connected to the operation voltage VDD, and a second terminal of the first storage capacitor Cst1 is electrically connected to the second terminal of

30 the first compensation transistor Tc1 and the control terminal of the first drive transistor Td1. A first terminal of the scan transistor Ts is electrically connected to the data line DL. A second terminal of the scan transistor Ts is electrically connected to the circuit node N1.

[0045] In the embodiment of the disclosure, a first terminal of the second drive transistor Td2 is electrically connected to the circuit node N1. A second terminal of the second drive transistor Td2 is electrically connected to a first terminal of the second bias transistor Tb2, and

40 a first terminal of the second compensation transistor Tc2. A control terminal of the second drive transistor Td2 is electrically connected to a second terminal of the second compensation transistor Tc2. A first terminal of the second bias transistor Tb2 is electrically connected to

45 the second terminal of the second drive transistor Td2. A second terminal of the second bias transistor Tb2 is electrically connected to a voltage VSS. A first terminal of the second storage capacitor Cst2 is electrically connected to the control terminal of the second drive transistor Td2 and a second terminal of the second compensation transistor Tc2, and a second terminal of the second storage capacitor Cst2 is electrically connected to the voltage VSS. In the embodiment of the disclosure, the tunable component 1120 is electrically connected between the circuit node N1 and a radio frequency input node N3. An input capacitor Cin is electrically connected to the tunable component 1120 in parallel, or equivalent to parasitic capacitance of the tunable component 1120.

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In the embodiment of the disclosure, a radio frequency signal RF-in is transmitted from a radio frequency input node N3 to the tunable component 1120.

[0046] In the embodiment of the disclosure, the first drive transistor Td1 may be operated as a source follower amplifier. The first compensation transistor Tc1 is configured to let the first drive transistor Td1 to form a diode unit when the first compensation transistor Tc1 is turned on. The first bias transistor Tb1 is configured to provide a first operation voltage (e.g., the operation voltage VDD) to the first drive transistor Td1 when the bias transistor Tb1 is turned on. In the embodiment of the disclosure, the first storage capacitor Cst1 is configured to hold the voltage for the control terminal of the first drive transistor Td1. In the embodiment of the disclosure, the second drive transistor Td2 may be operated as another source follower amplifier. The second compensation transistor Tc2 is configured to let the second drive transistor Td2 to form a diode unit when the second compensation transistor Tc2 is turned on. The second bias transistor Tb2 is configured to provide a second operation voltage (e.g., the voltage VSS) to the second drive transistor Td2 when the second bias transistor Tb2 is turned on. In the embodiment of the disclosure, the second storage capacitor Cst2 is configured to hold the voltage for the control terminal of the second drive transistor Td2. In the embodiment of the disclosure, a control terminal of the first compensation transistor Tc1 and a control terminal of the scan transistor Ts may receive a scan signal SS. A control terminal of the first bias transistor Tb1 may receive a bias signal SB. A control terminal of the second compensation transistor Tc2 may receive a scan signal SS. A control terminal of the second bias transistor Tb2 may receive a bias signal SB. In the embodiment of the disclosure, the data line DL may transmit a data signal SD.

[0047] In the embodiment of the disclosure, the operation manner of the electronic device 1100 can be inferred from the description of the above-mentioned embodiments. In the embodiment of the disclosure, the tunable component 1120 may alternately receive the source current SC1 and the sink current SC2 in an oscillating manner, and the input node N3 may receive the radio frequency signal RF-in (AC signal) during the bias period PB, so that the radio frequency signal RF-in may be modulated with the voltage Vdata (DC bias voltage) of the circuit node N1 with capacitive coupling with the input capacitor Cin (AC coupling) to generate a modulated signal (DC+AC) to the tunable component 1120. In the embodiment of the disclosure, the voltage Vdata may higher than the voltage of the radio frequency signal RF-in, and the first drive transistor Td1 may compensate the leakage current of the tunable component 1120 by automatically adjusting the source current SC1 accordingly. The current direction of the leakage current may toward to output to the input node N3. In one embodiment of the disclosure, the voltage of the radio frequency signal RF-in may higher than the voltage Vdata, and the second drive transistor Td2 may compensate the leakage current of the

tunable component 1120 by automatically adjusting the source current SC2 accordingly. The current direction of the leakage current may toward to output to the circuit node N1.

[0048] In the embodiment of the disclosure, the constant voltage source circuit 1110 may effectively and automatically compensate the leakage current of the tunable component 1120, and at the same time, the threshold voltages Vth of the first driving transistor Td1 and the second driving transistor Td2 may also be compensated, so that the bias voltage (Vbias) of the tunable component 1120 may be effectively maintained.

[0049] In addition, in other embodiments of the disclosure, the radio frequency signal RF-in may be replaced by a direct current signal (DC-in). The direct current signal (DC-in) may be transmitted from the input node N3 to the tunable component 1120. Thus, in other embodiments of the disclosure, when the voltage Vdata is higher than the voltage of the direct current signal (DC-in), the first drive transistor Td1 may compensate the leakage current of the tunable component 1120 by automatically adjusting the source current SC1 accordingly. The current direction of the leakage current may toward to output to the input node N3. Moreover, in other embodiments of the disclosure, when the voltage of the direct current signal (DC-in) is higher than the voltage Vdata, the second drive transistor Td2 may compensate the leakage current of the tunable component 1120 by automatically adjusting the source current SC2 accordingly. The current direction of the leakage current may toward to output to the circuit node N1.

[0050] FIG. 12 is a schematic diagram of an electronic device according to an embodiment of the disclosure. Referring to FIG. 12, the electronic device 1200 includes a constant voltage source circuit 1210, a tunable component 1220, smoothing capacitor Cs and a data line DL. The constant voltage source circuit 1210 is electrically connected to the tunable component 1220 and the data line DL. In the embodiment of the disclosure, the constant voltage source circuit 1210 includes a source follower circuit 1211, a compensation transistor Tc, a bias transistor Tb, a scan transistor Ts, a reset transistor Tr and a storage capacitor Cst, and the source follower circuit 1211 includes a drive transistor Td. In the embodiment of the disclosure, the drive transistor Td, the compensation transistor Tc, the bias transistor Tb, the scan transistor Ts and the reset transistor Tr are N-type transistors, such as a NMOS. In the embodiment of the disclosure, a first terminal of the drive transistor Td is electrically connected to a first terminal of the compensation transistor Tc. A control terminal of the drive transistor Td is electrically connected to a second terminal of the compensation transistor Tc. A second terminal of the drive transistor Td is electrically connected to a circuit node N1. A first terminal of the bias transistor Tb is electrically connected to an operation voltage VDD. A second terminal of the bias transistor Tb is electrically connected to the first terminal of the drive transistor Td. A first ter-

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min of the storage capacitor C_{st} is electrically connected to the operation voltage VDD , and a second terminal of the storage capacitor C_{st} is electrically connected to the second terminal of the compensation transistor T_c and the control terminal of the drive transistor T_d . In one embodiment of the disclosure, the second terminal of the storage capacitor C_{st} may electrically connected to a reference voltage. A first terminal of the scan transistor T_s is electrically connected to the data line DL . A second terminal of the scan transistor T_s is electrically connected to the circuit node $N1$. The tunable component 1220 is electrically connected between the circuit node $N1$ and the ground voltage VSS . The smoothing capacitor C_s is electrically connected to the tunable component 1220 in parallel.

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[0051] In the embodiment of the disclosure, the drive transistor T_d may be operated as a source follower amplifier. The compensation transistor T_c is configured to let the drive transistor T_d to form a diode unit when the compensation transistor T_c is turned on. The bias transistor T_b is configured to provide a first operation voltage (e.g., the operation voltage VDD) to the drive transistor T_d when the bias transistor T_b is turned on. The storage capacitor C_{st} is configured to hold the voltage for the control terminal of the drive transistor T_d . The reset transistor T_r is configured to reset the voltage of a control terminal of the drive transistor T_d . In the embodiment of the disclosure, a control terminal of the compensation transistor T_c and a control terminal of the scan transistor T_s may receive a scan signal SS . A control terminal of the bias transistor T_b may receive a bias signal SB . A control terminal of the reset transistor T_r may receive a reset signal SR . The data line DL may transmit a data signal SD .

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[0052] In the embodiment of the disclosure, the constant voltage source circuit 1210 may effectively and automatically compensate the leakage current of the tunable component 1220, and at the same time, the threshold voltage Vth of the driving transistor T_d may also be compensated, so that the bias voltage (V_{bias}) of the tunable component 1220 may be effectively maintained.

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[0053] FIG. 13 is a timing diagram of related voltages and signals according to the embodiment of FIG. 12 of the disclosure. In the embodiment of the disclosure, the operation manner of the electronic device 1100 in the reset periods $PR1$, $PR2$, the scan periods $PS1$, $PS2$ and the bias periods PB_1 to $PB_{(K+2)}$ can be inferred from the description of the above-mentioned embodiment of the FIG. 2, where K is a positive integer. In the embodiment of the disclosure, a whole frame period, for example from time $t1$ to time $t(n+2)$, may have multiple bias periods PB_1 to $PB_{(K+1)}$ and multiple hold periods PH_1 to PH_K that are alternately performed, where n is a positive integer. During the hold periods PH_1 to PH_K , respectively, the bias transistor T_b , the scan transistor T_s and the compensation transistor T_c are turned off by the bias signal SB and the scan signal SS with a low voltage level. In other words, the bias transistor T_b may be turned off

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periodically to reduce stress of the bias transistor T_b and the drive transistor T_d . Moreover, the smoothing capacitor C_s may be adapted to suppress the bias voltage drop during the hold periods PH_1 to PH_K respectively. Besides, the smoothing capacitor C_s may also be applied to each of the constant voltage source circuits of the above-mentioned embodiments.

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[0054] In summary, the electronic device of the disclosure is capable of effectively compensating the leakage current of the tunable component without requiring the electronic device to operate at a higher refresh rate nor use a larger storage capacitor. Furthermore, in some embodiments of the disclosure, the electronic device also has the advantage that the stress of the transistor can be effectively relieved.

Claims

- 20
1. An electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200), comprising:
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a tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220), electrically connected to a circuit node (N1, N2); and
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a first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211), electrically connected to the circuit node (N1, N2), and comprising a first control terminal and a first terminal, wherein the first control terminal is electrically connected to the first terminal.
2. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
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a first reset transistor (T_r , TrA), electrically connected to the first control terminal of the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211).
3. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, wherein a current is transmitted from the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211) to the tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220).
4. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, wherein a current is transmitted from the tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220) to the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211).
5. The electronic device according to the claim 1, wherein the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211) comprises a first drive transistor (T_d , $Td1$).

6. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a smoothing capacitor (Cs), electrically connected to the tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220) in parallel. 5

7. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a first compensation transistor (Tc, Tc1), electrically connected to the first control terminal and the first terminal of the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211). 10

8. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a first bias transistor (Tb, Tb 1, TbA), electrically connected to the first terminal of the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211) and a first operation voltage. 15

9. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a first storage capacitor (Cst, Cst1), electrically connected to the first control terminal of the first source follower circuit (111, 311, 511, 711, 911, 1011, 1111_1, 1211). 20

10. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a second source follower circuit (1111_2), electrically connected to the circuit node (N1), wherein the second source follower circuit (1111_2) comprises a second control terminal and a second terminal, and the second control terminal is electrically connected to the second terminal. 25

11. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 10, wherein the second source follower circuit (1111_2) comprises a second drive transistor (Td2), wherein the second drive transistor is a N-type transistor or a P-type transistor. 30

12. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 10, further comprising:
a second compensation transistor (Tc2), electrically connected to the second control terminal and the second terminal of the second source follower circuit (1111_2). 35

13. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 10, further comprising:
a second bias transistor (Tb2), electrically connected to the second terminal of the second source follower circuit (1111_2) and a second operation voltage;
a second storage capacitor (Cst2), electrically connected to the second control terminal of the second source follower circuit (1111_2); and
a second reset transistor (Tr2), electrically connected to the second control terminal of the second source follower circuit (1111_2). 40

14. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a scan transistor (Ts), electrically connected to the circuit node (N1, N2), wherein the scan transistor (Ts) is further electrically connected to a data line (DL). 45

15. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 1, further comprising:
a third reset transistor (TrB), electrically connected to the tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220) in parallel; and
a third bias transistor (TbB), electrically connected between the circuit node (N1, N2) and the tunable component (120, 320, 520, 720, 920, 1020, 1120, 1220). 50

16. The electronic device (100, 300, 500, 700, 900, 1000, 1100, 1200) according to the claim 10, further comprising:
a second compensation transistor (Tc2), electrically connected to the second control terminal and the second terminal of the second source follower circuit (1111_2). 55

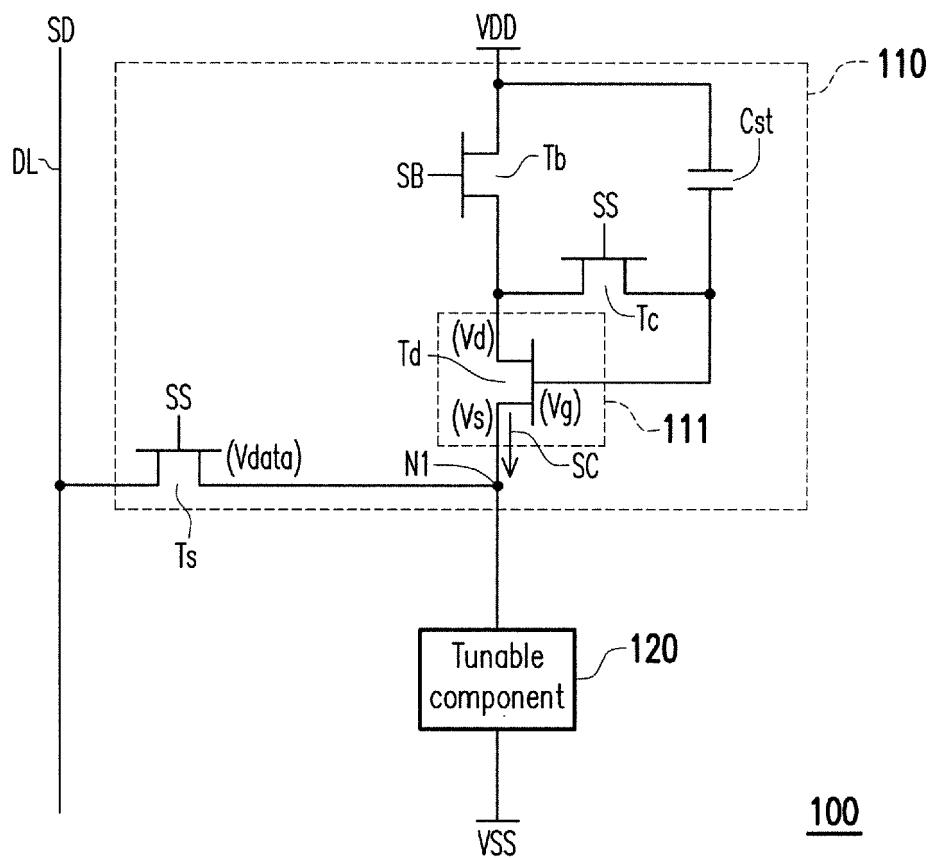


FIG. 1

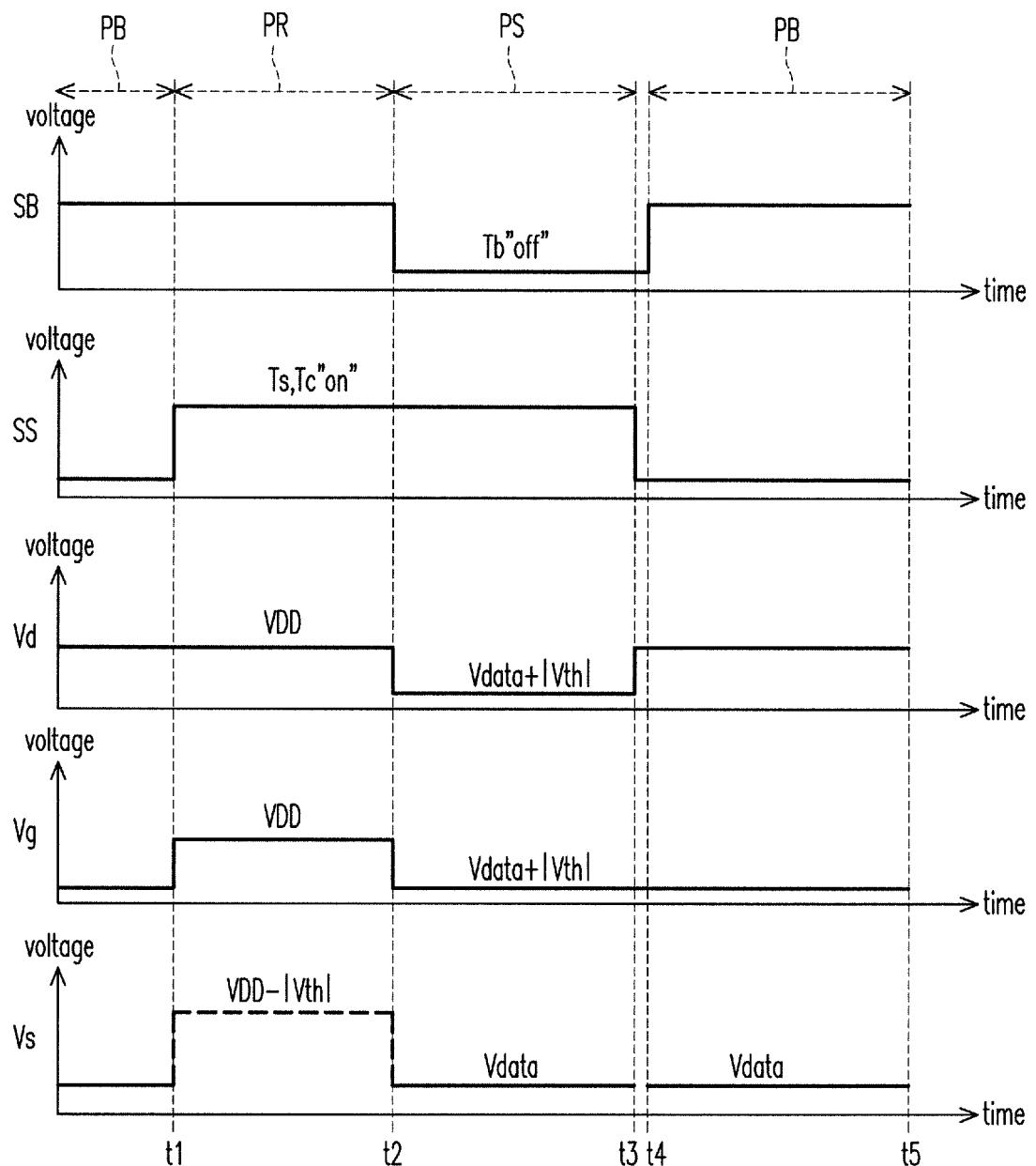


FIG. 2

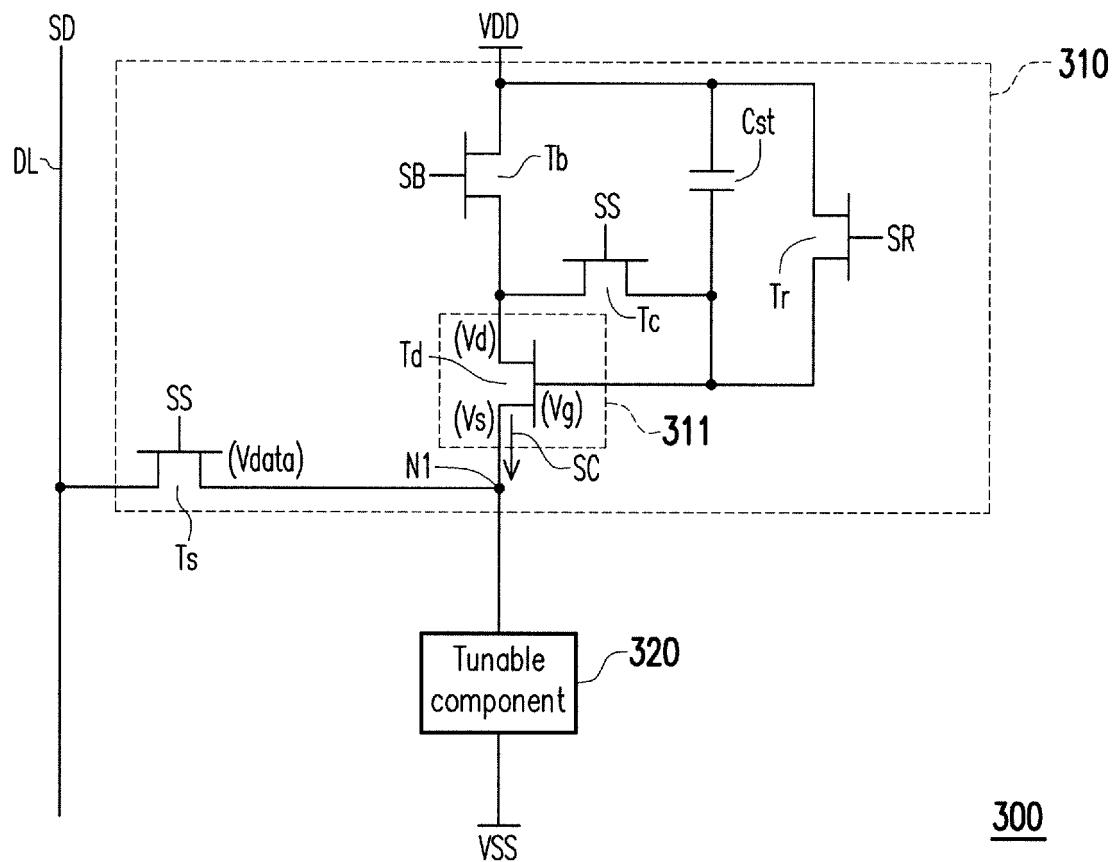


FIG. 3

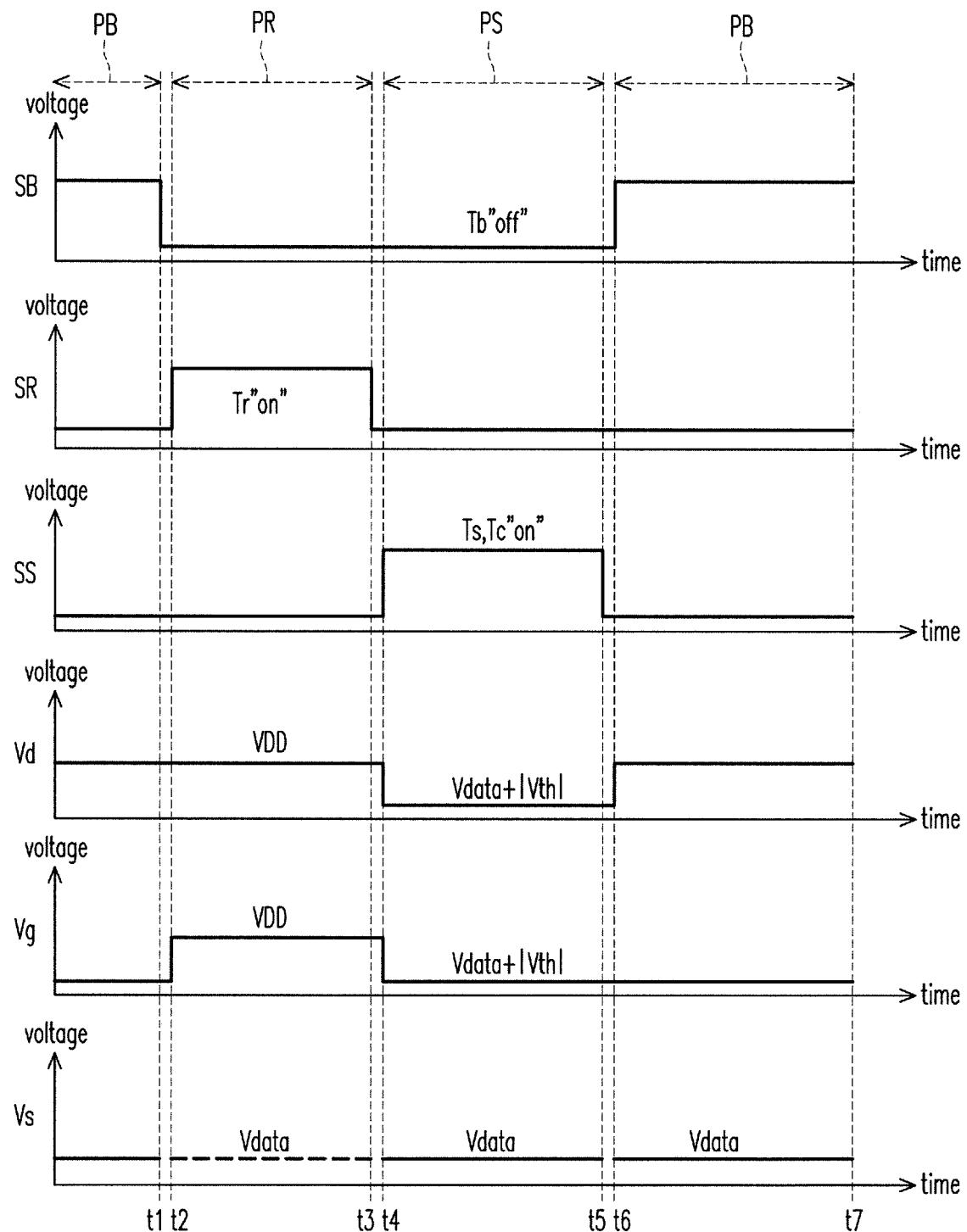


FIG. 4

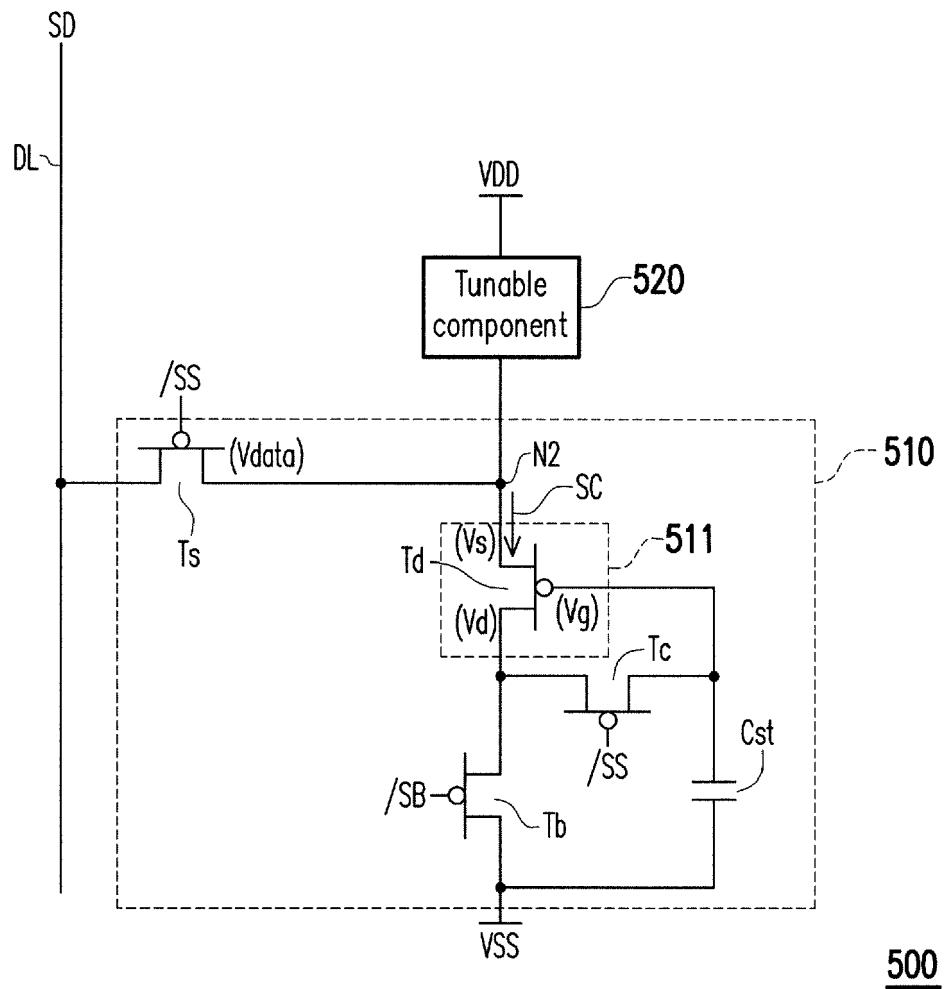


FIG. 5

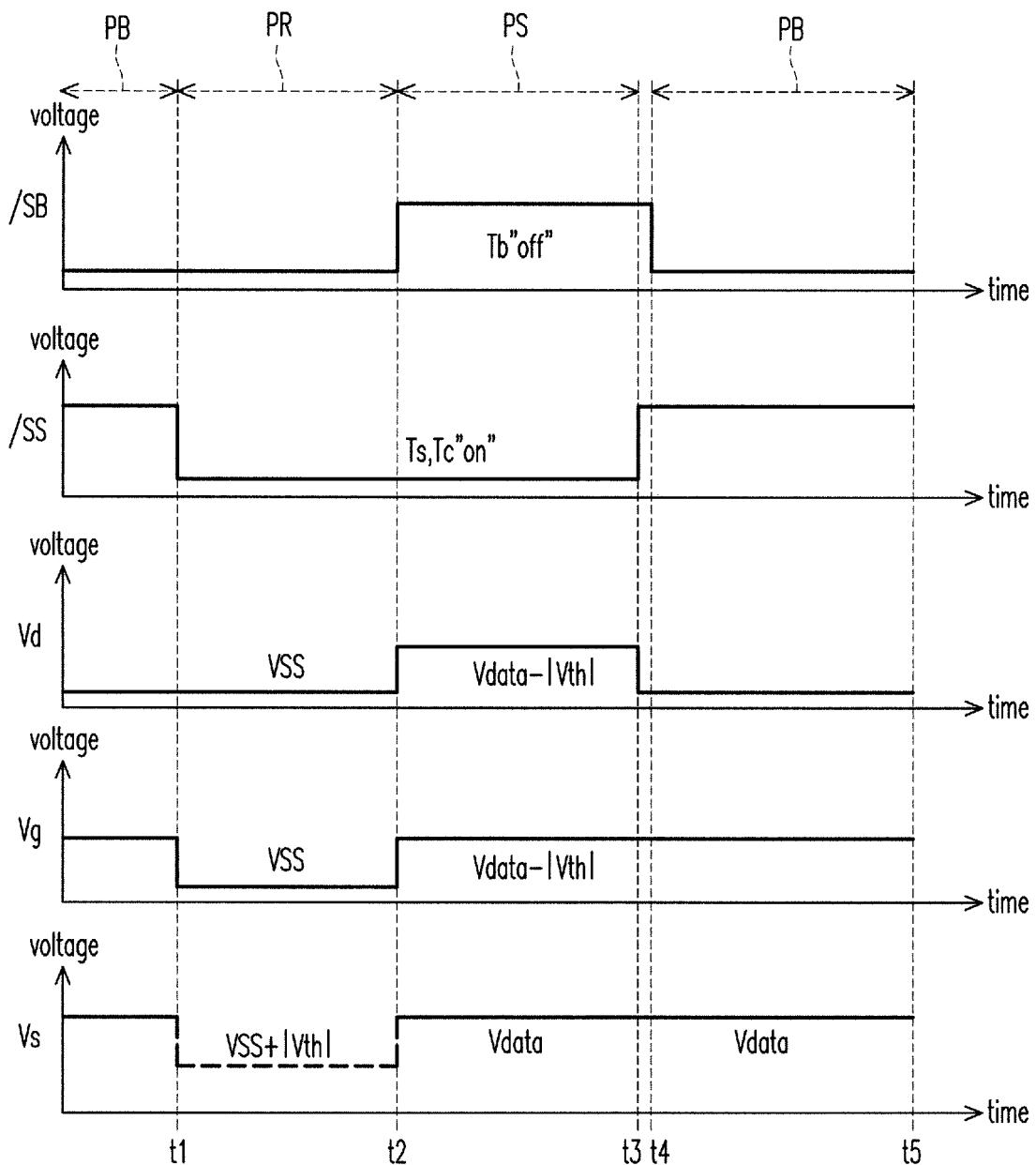


FIG. 6

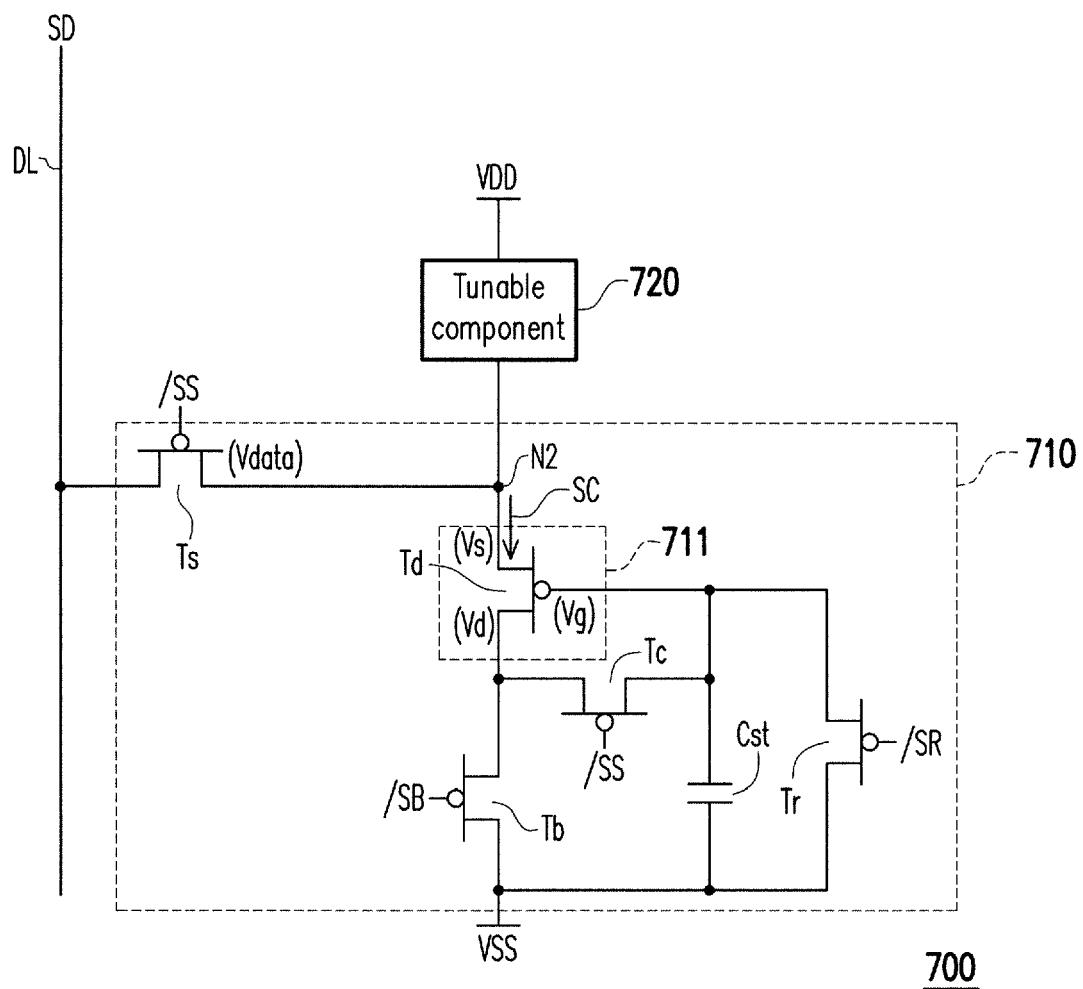


FIG. 7

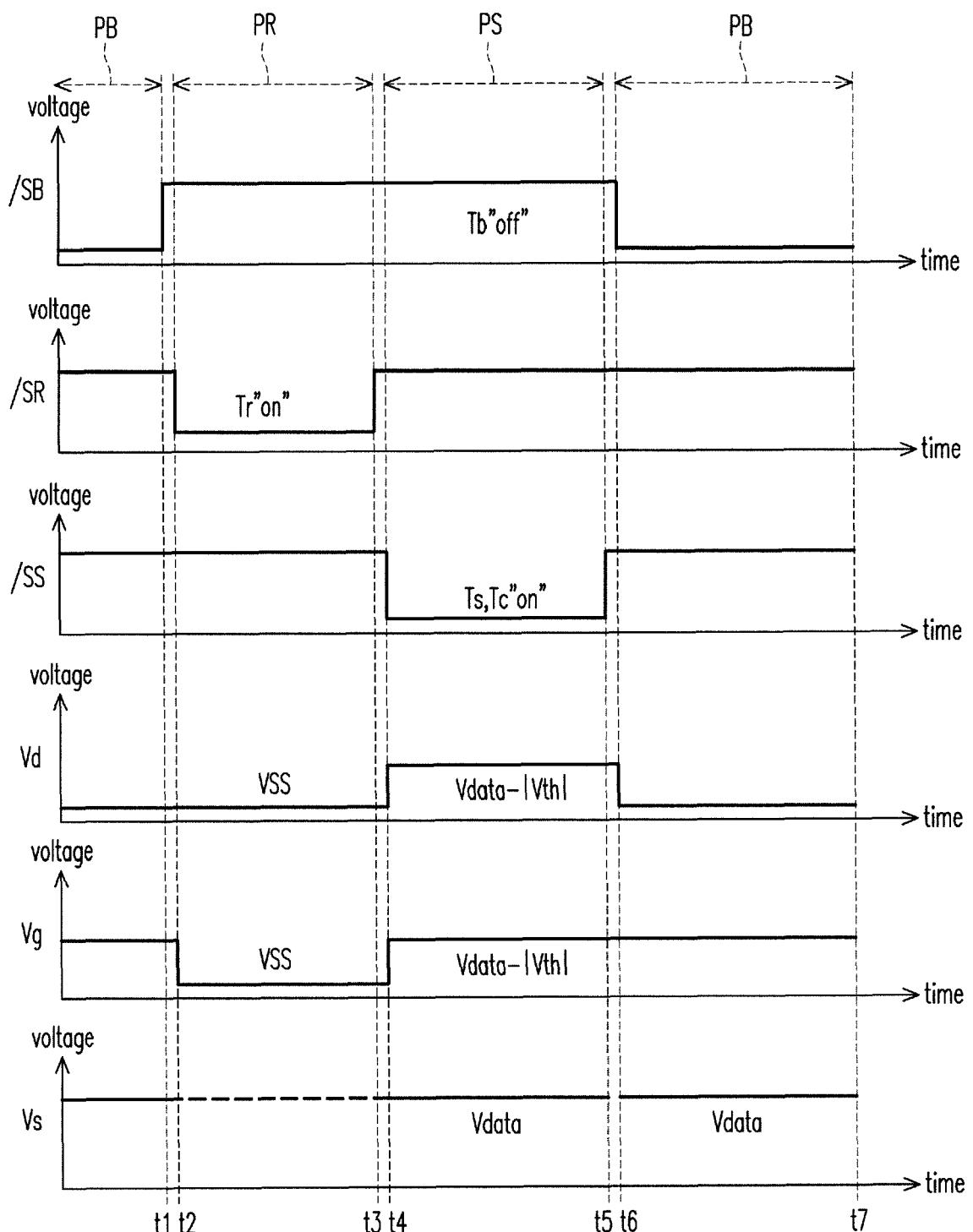


FIG. 8

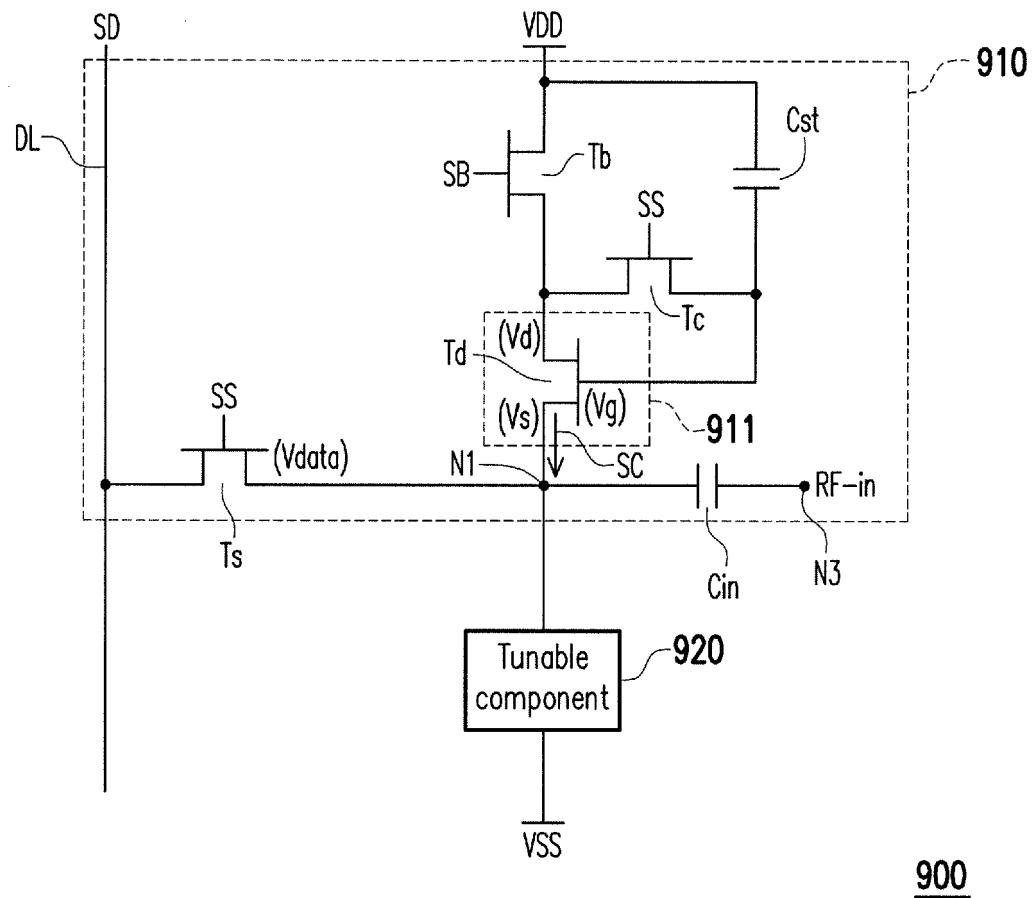


FIG. 9

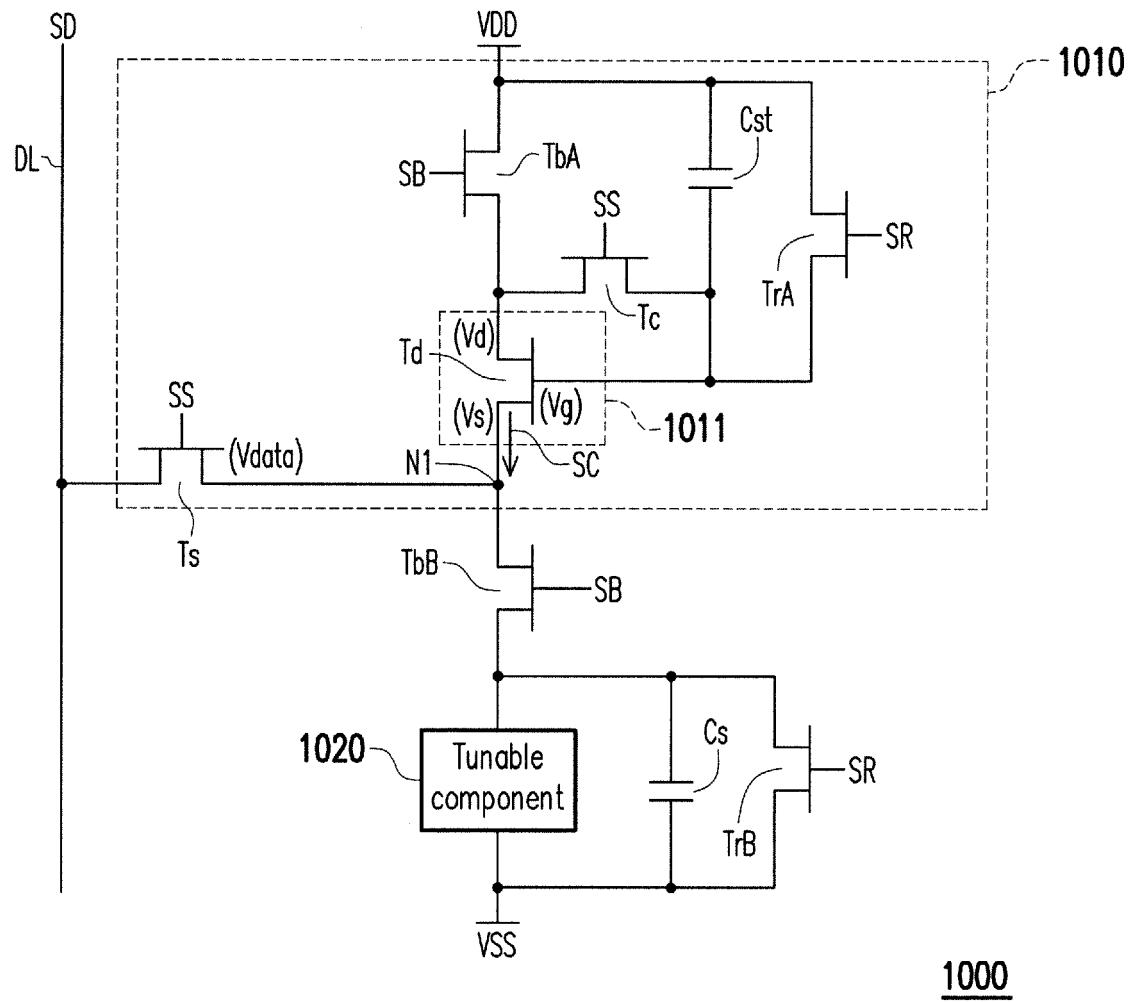


FIG. 10

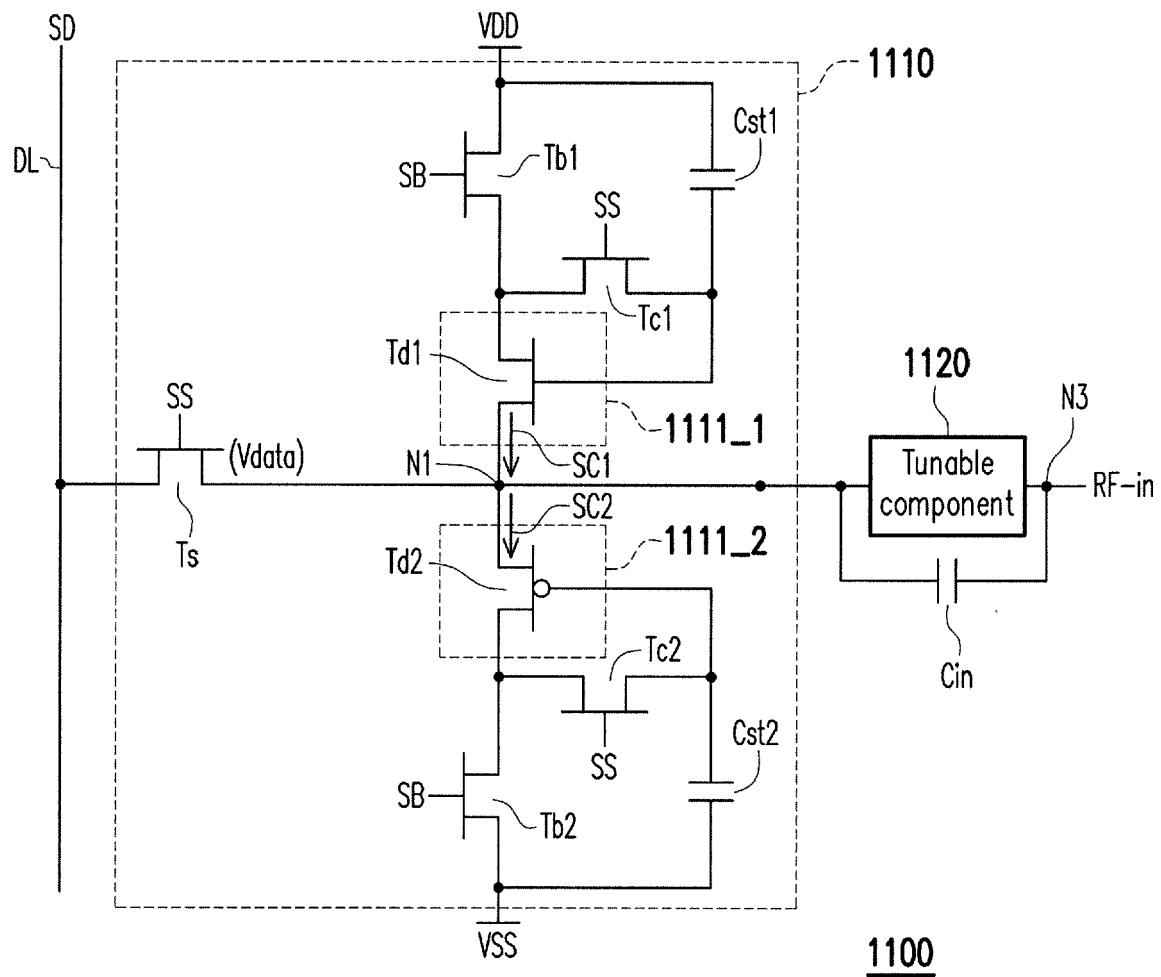


FIG. 11

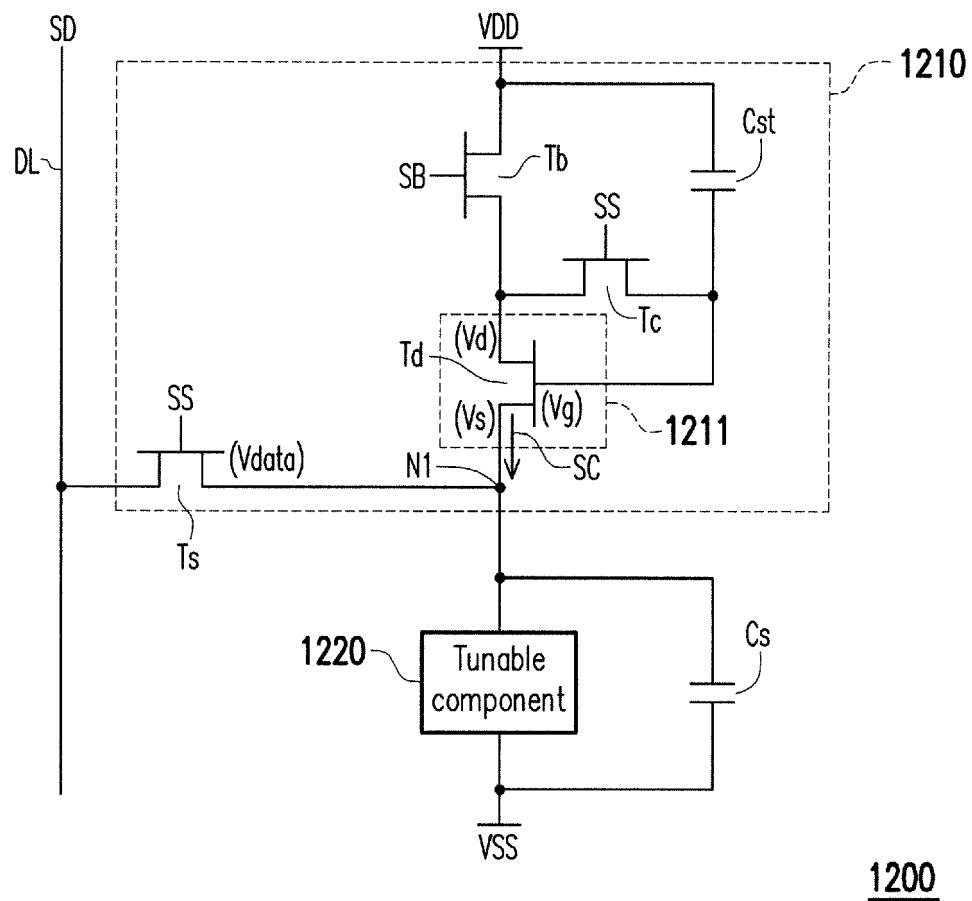


FIG. 12

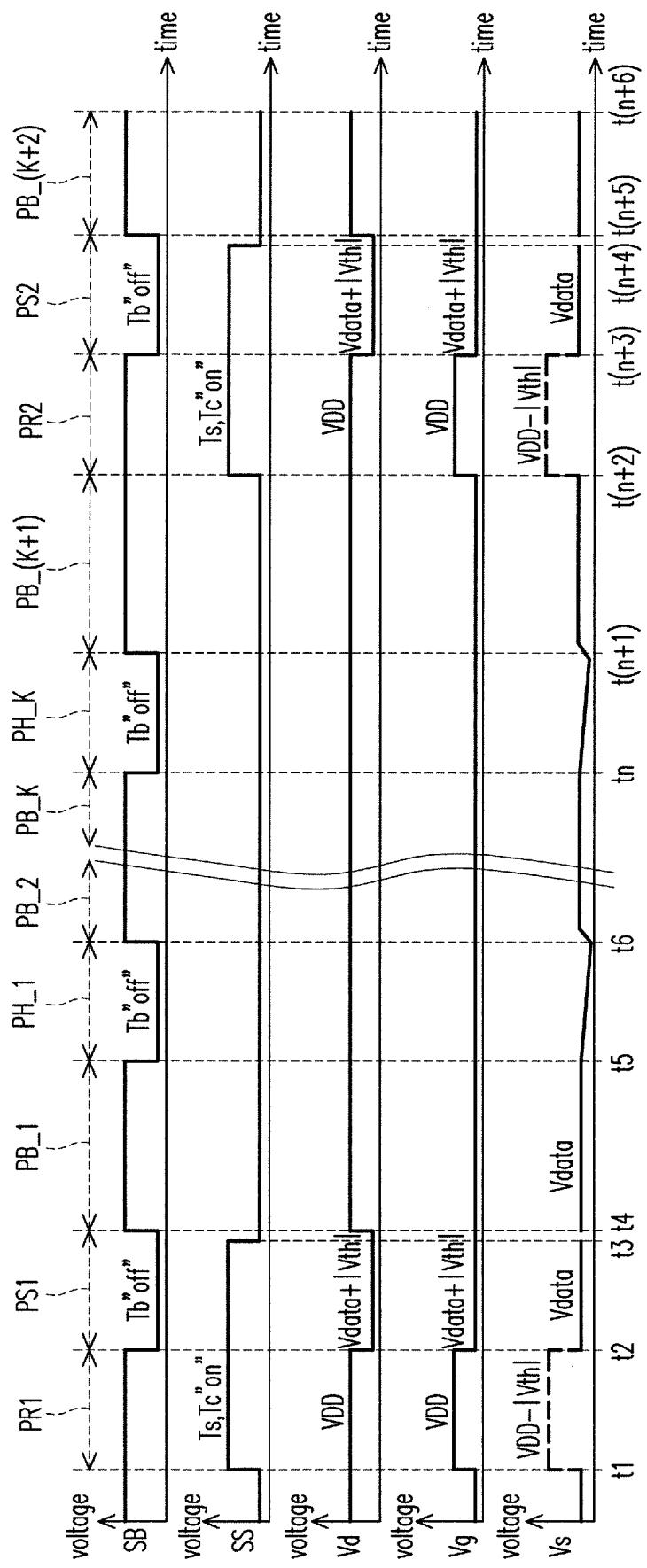


FIG. 13



EUROPEAN SEARCH REPORT

Application Number

EP 22 19 0691

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The present search report has been drawn up for all claims			
1	Place of search The Hague	Date of completion of the search 16 January 2023	Examiner João Carlos Silva
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