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(54) **PIXEL DRIVER CIRCUIT**

(57) An embodiment of this application provides a pixel drive circuit that can be used for a micro LED, including a first switch and a second switch that are cascaded between a cathode of a light emitting diode and the ground, and a charge absorption circuit. The first switch is controlled by a PWM signal to control the light emitting diode to be turned on or off, a control end of the second switch receives a bias voltage, and the charge absorption circuit is connected to a connection point of the first switch and the second switch, to absorb a charge on the connection point. This can accelerate establishment of a signal of the light emitting diode, and improve display performance of the pixel light emitting diode.

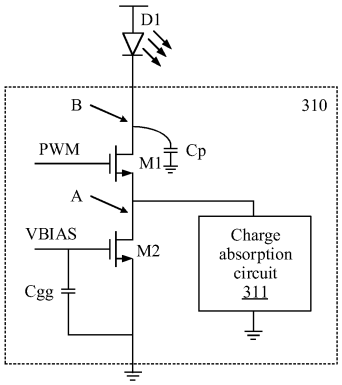

FIG. 3

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Description

TECHNICAL FIELD

[0001] This application relates to circuit technologies, and in particular, to a pixel drive circuit.

BACKGROUND

[0002] An light emitting diode (LED) display panel implements pixel display by using an LED, and in terms of display performance, the LED has higher contrast and higher luminance than a conventional liquid crystal display (LCD).

[0003] In the LED display panel, an LED pixel array is driven by a pixel drive circuit. The pixel drive circuit is selected based on a row selection signal and a column drive signal, to drive the LED to emit light. An anode of the LED is connected to a power supply, and a cathode is connected to the pixel drive circuit. Because there are a parasitic capacitor and a parasitic resistor on the cathode of the LED, when the LED is frequently switched between an on state and an off state, the pixel drive circuit needs to charge or discharge the cathode of the LED at a high speed, and charging/discharging time affects switching time of the LED, and consequently, a switching speed of the LED is limited. When the switching speed of the LED is relatively slow, a ghost phenomenon is easily observed by a human eye, and user experience is affected.

SUMMARY

[0004] Embodiments of this application provide a pixel drive circuit, to accelerate absorption of a charge in a parasitic capacitor by using a charge absorption circuit, so that a switching frequency of a light emitting diode is improved.

[0005] According to a first aspect, an embodiment of this application provides a pixel drive circuit, including a first switch and a second switch that are cascaded between a cathode of a light emitting diode and the ground, and a charge absorption circuit. An anode of the light emitting diode is electrically connected to a voltage source, one end of the charge absorption circuit is electrically connected to a connection point (a first node) of the first switch and the second switch, and the other end is connected to the ground. A first end of the first switch is electrically connected to the cathode of the light emitting diode, and a control end of the first switch receives a control signal, so that the first switch is closed or opened based on the control signal, to control the light emitting diode to be turned on or off. A first end of the second switch is electrically connected to a second end of the first switch, a second end of the second switch is grounded, a control end of the second switch receives a bias voltage, and the second switch is closed in a working state. The charge absorption circuit is configured to absorb a charge from the first node. When the first switch is opened and the light emitting diode is off, a parasitic capacitor on the cathode (a second node) of the light emitting diode D1 accumulates charges. When the first switch is closed, the charge in the parasitic capacitor is discharged by using the first switch and the second switch, and may also be discharged by using the charge absorption circuit.

[0006] The charge absorption circuit electrically connected to the first node can accelerate release of the charge on the first node, so that the charge in the parasitic capacitor can be released more quickly. When a charge release speed in the parasitic capacitor is accelerated, current signal establishment time of the light emitting diode is shortened, and a refresh frequency of the light emitting diode is increased, so that time experienced by the light emitting diode in a process from an extinct state to a lighted state is shortened, a ghost phenomenon caused when a human eye observes the light emitting diode can be improved, display precision of the light emitting diode is improved, and user experience is improved.

[0007] In a possible implementation, both the first switch and the second switch may be NMOS transistors. A source of a first NMOS transistor used as the first switch is electrically connected to the ground, a drain of the first NMOS transistor and a source of a second NMOS transistor used as the second switch are electrically connected to the first node, and a drain of the second NMOS transistor is electrically connected to the cathode of the light emitting diode.

[0008] In a possible implementation, the charge absorption circuit includes a first capacitor, one end of the first capacitor is electrically connected to the first node, and the other end is grounded. The capacitor used as the charge absorption circuit occupies a relatively small area resource, so that display performance of the light emitting diode can be significantly improved at the extremely low cost of hardware resources.

[0009] In a possible implementation, the first capacitor is a metal-insulator-metal MIM capacitor, a metal-oxide-metal MOM capacitor, or a metal-oxide-semiconductor MOS capacitor.

[0010] In a possible implementation, the charge absorption circuit includes a diode-connected MOS transistor; in other words, two MOS transistors are connected to form a two-end component to be used as a diode. The diode-connected MOS transistor can better improve display performance of the light emitting diode.

[0011] In a possible implementation, the diode-connected MOS transistor includes a third NMOS transistor and a fourth NMOS transistor. A drain and a gate of the third NMOS transistor are electrically connected to the first node, a drain of the fourth NMOS transistor is electrically connected to a source of the third NMOS transistor, a source of the fourth NMOS transistor is grounded, and a gate of the fourth NMOS transistor is electrically connected to the first node.

[0012] In a possible implementation, the charge ab-

sorption circuit includes a Schottky diode, a cathode of the Schottky diode is electrically connected to the first node, and an anode is grounded. The Schottky diode used as the charge absorption circuit occupies a relatively small area resource, so that display performance of the light emitting diode can be significantly improved at the extremely low cost of hardware resources.

[0013] In a possible implementation, the pixel drive circuit further includes a second capacitor, one end of the second capacitor is electrically connected to the control end of the second switch, and the other end is grounded.

[0014] In a possible implementation, the control signal that is input to the first switch is a pulse width modulation PWM signal.

[0015] In a possible implementation, the foregoing plurality of light emitting diodes may include a plurality of RGB pixels, and each RGB pixel includes three types of pixels: R, G, and B.

[0016] In a possible implementation, the foregoing plurality of pixel drive circuits are separately disposed in a plurality of chips, and each pixel drive circuit drives a corresponding light emitting diode.

[0017] According to a second aspect, an embodiment of this application provides a pixel drive circuit, including a first switch and a second switch that are cascaded between a cathode of a light emitting diode and the ground, a charge absorption circuit, and a ninth switch. An anode of the light emitting diode is electrically connected to a voltage source, one end of the charge absorption circuit is electrically connected to the cathode of the light emitting diode by using the ninth switch, and the other end is connected to the ground. A first end of the first switch is electrically connected to the cathode of the light emitting diode, and a control end of the first switch and a control end of the ninth switch receive a same control signal, so that the first switch and the ninth switch are closed or opened based on the control signal, to control the light emitting diode to be turned on or off. A first end of the second switch is electrically connected to a second end of the first switch, a second end of the second switch is grounded, a control end of the second switch receives a bias voltage, and the second switch is closed in a working state. The charge absorption circuit is configured to absorb a charge from the cathode of the light emitting diode. When the first switch is opened and the light emitting diode is off, a parasitic capacitor on the cathode (a second node) of the light emitting diode D1 accumulates charges. When the first switch is closed, the charge in the parasitic capacitor is discharged by using the first switch and the second switch, and may also be discharged by using the charge absorption circuit.

[0018] The charge absorption circuit electrically connected to the cathode of the light emitting diode can accelerate release of a charge on the cathode of the light emitting diode, so that the charge in the parasitic capacitor can be released more quickly. When a charge release speed in the parasitic capacitor is accelerated, current signal establishment time of the light emitting diode is shortened, and a refresh frequency of the light emitting diode is increased, so that time experienced by the light emitting diode in a process from an extinct state to a lighted state is shortened, a ghost phenomenon caused when a human eye observes the light emitting diode can be improved, display precision of the light emitting diode is improved, and user experience is improved.

[0019] In a possible implementation, both the first switch and the second switch may be NMOS transistors. A source of a first NMOS transistor used as the first switch is electrically connected to the ground, a drain of the first NMOS transistor and a source of a second NMOS transistor used as the second switch are electrically connected to the cathode of the light emitting diode, and a drain of the second NMOS transistor is electrically connected to the cathode of the light emitting diode.

[0020] In a possible implementation, the charge absorption circuit includes a first capacitor, one end of the first capacitor is electrically connected to the cathode of the light emitting diode, and the other end is grounded. The capacitor used as the charge absorption circuit occupies a relatively small area resource, so that display performance of the light emitting diode can be significantly improved at the extremely low cost of hardware resources.

[0021] In a possible implementation, the first capacitor is a metal-insulator-metal MIM capacitor, a metal-oxide-metal MOM capacitor, or a metal-oxide-semiconductor MOS capacitor.

[0022] In a possible implementation, the charge absorption circuit includes a diode-connected MOS transistor; in other words, two MOS transistors are connected to form a two-end component to be used as a diode. The diode-connected MOS transistor can better improve display performance of the light emitting diode.

[0023] In a possible implementation, the diode-connected MOS transistor includes a third NMOS transistor and a fourth NMOS transistor. A drain and a gate of the third NMOS transistor are electrically connected to the cathode of the light emitting diode, a drain of the fourth NMOS transistor is electrically connected to a source of the third NMOS transistor, a source of the fourth NMOS transistor is grounded, and a gate of the fourth NMOS transistor is electrically connected to the cathode of the light emitting diode.

[0024] In a possible implementation, the charge absorption circuit includes a Schottky diode, a cathode of the Schottky diode is electrically connected to the cathode of the light emitting diode, and an anode is grounded. The Schottky diode used as the charge absorption circuit occupies a relatively small area resource, so that display performance of the light emitting diode can be significantly improved at the extremely low cost of hardware resources.

[0025] In a possible implementation, the pixel drive circuit further includes a second capacitor, one end of the second capacitor is electrically connected to the control end of the second switch, and the other end is grounded.

[0026] In a possible implementation, the control signal that is input to the first switch is a pulse width modulation PWM signal.

[0027] According to a third aspect, an embodiment of this application provides a display circuit, including a plurality of pixel drive circuits in the first aspect and any possible implementation, and a plurality of light emitting diodes. The plurality of light emitting diodes are separately electrically connected to the plurality of pixel drive circuits, and the plurality of pixel drive circuits are configured to separately drive the plurality of light emitting diodes.

[0028] According to a fourth aspect, an embodiment of this application provides a display circuit, including a plurality of pixel drive circuits in the second aspect and any possible implementation, and a plurality of light emitting diodes. The plurality of light emitting diodes are separately electrically connected to the plurality of pixel drive circuits, and the plurality of pixel drive circuits are configured to separately drive the plurality of light emitting diodes.

[0029] According to a fifth aspect, an embodiment of this application provides a terminal device, including a rear cover, a bezel, and the display circuit in the third aspect or the fourth aspect. The rear cover and the display circuit are disposed opposite to each other and are connected by using the bezel.

[0030] The pixel drive circuit in the second aspect, the display circuits in the third aspect and the fourth aspect, and the terminal device in the fifth aspect have a similar effect to the pixel drive circuit in the first aspect, and can all improve the ghost phenomenon caused when the human eye observes the light emitting diode, and improve display precision of the light emitting diode. Details are not described herein again.

BRIEF DESCRIPTION OF DRAWINGS

[0031]

FIG. 1 is a schematic diagram of a sectional structure of a terminal device according to an embodiment of this application;

FIG. 2 is a schematic diagram of a display circuit according to an embodiment of this application;

FIG. 3 is a diagram of a circuit structure of a pixel drive circuit according to an embodiment of this application;

FIG. 4a is a waveform diagram of a PWM signal in a pixel drive circuit according to an embodiment of this application;

FIG. 4b is a waveform diagram of a current in a light emitting diode;

FIG. 4c is a waveform diagram of a node A in a conventional circuit;

FIG. 4d is a waveform diagram of a node A in a pixel drive circuit according to an embodiment of this application;

FIG. 5 shows a more specific pixel drive circuit according to an embodiment of this application;

FIG. 6 shows another more specific pixel drive circuit according to an embodiment of this application;

FIG. 7 shows still another more specific pixel drive circuit according to an embodiment of this application;

FIG. 8 shows yet another more specific pixel drive circuit according to an embodiment of this application; and

FIG. 9 is a diagram of another pixel drive circuit according to an embodiment of this application.

DESCRIPTION OF EMBODIMENTS

[0032] The following clearly and completely describes the technical solutions in embodiments of this application with reference to the accompanying drawings in embodiments of this application.

[0033] The terms "first" and "second" in this application are merely intended for a purpose of description, and shall not be understood as an indication or implication of relative importance or implicit indication of a quantity of indicated technical features. In addition, the term "electrical connection" needs to be understood in a broad sense. For example, "electrical connection" may be a physical direction connection, or may be an electrical connection implemented by using an intermediary medium, for example, a connection implemented by using a resistor, an inductor, or another electrical element.

[0034] When being used to describe a three-end switch element, a "first end" and a " second end" may separately be connection ends of the three-end switch element, and a "control end" may be a control end of the three-end switch element. For example, for a metal-oxide-semiconductor (MOS) transistor switch, a control end may be a gate of the MOS transistor, a first end may be a source of the MOS transistor, and a second end is a drain of the MOS transistor; or the first end may be a drain of the MOS transistor, and the second end is a source of the MOS transistor.

[0035] FIG. 1 is a schematic diagram of a sectional structure of a terminal device 200 according to an embodiment of this application. The terminal device 200 may be a smartphone, a portable computer, a tablet computer, an electronic band, or the like, or a super small display. The terminal device 200 includes a screen 210, a bezel 220, and a rear cover 230. The screen 210 and the rear cover 230 are disposed opposite to each other, and are connected by using the bezel 220, to form a cavity between the screen 210 and the rear cover 230. A substrate 240 is disposed in the cavity, and a plurality of drive circuits 250 are disposed on the substrate 240. An LED array 260 is further disposed on the substrate 240. One drive circuit 250 may be connected to one or more LED arrays 260, and drive a corresponding LED array 260 to emit light. The substrate 240 may be a printed circuit board (PCB). The terminal device 200 may further in-

clude a touch panel, configured to sense a touch signal and convert the touch signal into an electrical signal. The terminal device 200 may further include another chip such as a processor chip, a storage chip, or a baseband chip. The chip may be disposed on the substrate 240, or may be disposed on another PCB in the terminal device 200, and is electrically connected to the drive circuit 250, to control the drive circuit 250 to drive the LED array 260.

[0036] FIG. 2 is a schematic diagram of a display circuit 300 according to an embodiment of this application. The display circuit 300 may be a micro light emitting diode (micro LED) display circuit. The display circuit 300 includes a plurality of pixel drive circuits 310 arranged in an array and a plurality of RGB pixels corresponding to the pixel drive circuits 310. The pixel drive circuit 310 may be the drive circuit 250 shown in FIG. 1, and the RGB pixel may be the LED array 260 shown in FIG. 1. Each pixel drive circuit 310 may drive four RGB pixels in a connection relationship shown in FIG. 2, drive more RGB pixels, or drive only one RGB pixel. Each RGB pixel includes R (red), G (green), and B (blue). The plurality of pixel drive circuits 310 may be separately disposed on a plurality of chips, or may be fabricated on the substrate 240 in a form of a thin film transistor (TFT). For example, one pixel drive circuit 310 drives four RGB pixels. For a 2K screen whose resolution is 2560*1440, the display circuit 300 may include 2560*1440/4=921600 pixel drive circuits 310, and each pixel drive circuit 310 is disposed on one chip and drives four RGB pixels. Specifically, each pixel drive circuit includes 12 current sources to drive 12 light emitting diodes in the four RGB pixels. In another implementation, a plurality of pixel drive circuits may alternatively be integrated into one chip.

[0037] FIG. 3 is a diagram of a circuit structure of a pixel drive circuit 310 according to an embodiment of this application. The pixel drive circuit 310 includes a first switch M1 and a second switch M2 that are cascaded, and a charge absorption circuit 311. A first end of the first switch M1 is electrically connected to a cathode of a light emitting diode D1, a second end of the first switch M1 is electrically connected to a first end of the second switch M2, and a control end of the first switch M1 is configured to receive a switch control signal. In an implementation, the switch control signal may be a pulse width modulation (PWM) signal. A second end of the second switch M2 is grounded, and is electrically connected to one end of a second capacitor Cgg. A control end of the second switch M2 is configured to receive a bias voltage VBIAS. In addition, an anode of the light emitting diode D1 is connected to a power supply, to provide a voltage difference applied to two ends of the light emitting diode D1. The charge absorption circuit 311 is electrically connected to a node A (that is, a connection point of the first switch M1 and the second switch M2), to absorb a charge on the node A. Some charges on the node A flow to the ground through the second switch M2, and other charges are absorbed by the charge absorption circuit 311. The pixel drive circuit 310 may further include the second capacitor Cgg that is electrically connected to the control end and the second end of the second switch M2.

[0038] In a working state, the first switch M1 is closed or opened by using the received switch control signal, and the second switch M2 is kept closed by using the received bias voltage VBIAS. When the switch control signal controls the first switch M1 to be opened, a voltage of a node B (that is, the cathode of the light emitting diode D1) increases, a current in the light emitting diode D1 is 0, and a parasitic capacitor Cp on the node B accumulates charges. When the switch control signal controls the first switch M1 to be closed, the parasitic capacitor Cp performs discharging by using the first switch M1 and the second switch M2. The light emitting diode D1 is turned on when a voltage of the node B is lower than a specific threshold (depending on characteristics of the light emitting diode D1). After the first switch M1 is closed, the charge absorption circuit 311 may absorb the charge on the node A. Therefore, charges accumulated in the parasitic capacitor Cp may be first discharged by using the first switch M1, and then by using the second switch M2, and discharged by using the charge absorption circuit 311, to accelerate discharging of the parasitic capacitor Cp on the node B, prolong current signal establishment time of the light emitting diode D1, and improve a refresh frequency of the light emitting diode D1. In a non-working state, the bias voltage VBIAS controls the second switch M2 to be opened.

[0039] When the voltage of the node B is less than a specific threshold, the light emitting diode D1 is turned on. The threshold is mainly related to a forward conduction voltage of the light emitting diode D1. For example, a forward conduction voltage of a silicon (Si) transistor is approximately 0.7 V, and a forward conduction voltage of a germanium (Ge) transistor is approximately 0.3 V

[0040] In an implementation, both the first switch M1 and the second switch M2 are NMOS transistors. The control end of the first switch M1 is a gate, the first end of the first switch M1 is a drain, and the second end is a source. The control end of the second switch M2 is a gate, the first end of the second switch M2 is a drain, and the second end is a source.

[0041] The switch control signal is generated by a control signal generator and output to the control end of the first switch M1 in the pixel drive circuit 310. In an implementation, the control signal generator and the pixel drive circuit 310 may be separately disposed on different chips. For example, one pixel drive circuit 310 is disposed on a corresponding drive IC, and the control signal generator is disposed on another chip. A control signal such as a PWM signal generated by one control signal generator may control on and off of the first switch M1 in the plurality of pixel drive circuits 310.

[0042] In a same charging/discharging periodicity, FIG. 4a is a waveform diagram of a PWM signal in the pixel drive circuit 310, FIG. 4b is a waveform diagram of a current I_{D1} in the light emitting diode D 1, FIG. 4c is a waveform diagram of a node A in a conventional circuit,

and FIG. 4d shows an optimized circuit, that is, a waveform diagram of the node A in the pixel drive circuit 310 provided in this embodiment of this application. In this embodiment of this application, as an example for description, the switch control signal is a PWM signal, and both the first switch M1 and the second switch M2 are NMOS transistors.

[0043] When the pixel drive circuit 310 works normally, the second switch M2 is closed. From a moment 0 to a moment t_1, the PWM signal is at a low level, and in this case, the first switch M1 is in an open state. Therefore, the voltage of the node B is higher than the foregoing threshold voltage, the current I_{D1} in the light emitting diode D1 is 0, and the light emitting diode D1 is in an off state. At the moment t_1, the PWM signal changes from the low level to a high level, and in this case, the first switch M1 switches from the open state to a closed state. Because both the first switch M1 and the second switch M2 are in a closed state, a voltage of the node B in an ideal state rapidly decreases to 0, and the current I_{D1} in the light emitting diode D1 rapidly increases to a relatively large value, as shown by an "ideal current" curve in FIG. 4b. In actual operation, as shown by a "conventional circuit" curve in FIG. 4b, because there is a parasitic capacitor Cp on a node B in a conventional circuit in a conventional technology, when the first switch M1 switches from the open state to the closed state, the parasitic capacitor Cp first needs to perform discharging by using the first switch M1 and the second switch M2 from the moment t_1 to a moment t_4, until a voltage of the node B is lower than the foregoing threshold voltage. At the moment t_4, the current I_{D1} in the light emitting diode D1 starts to increase, reaches a maximum value at a moment t_3, and then keeps the maximum value until a moment t_2, and the light emitting diode D1 is in an on state. At the moment t_2, the PWM signal changes from the high level to the low level, and the current I_{D1} in the light emitting diode D1 decreases. Correspondingly, as shown in FIG. 4c, because discharging is slow, after the first switch M1 is closed, a node A in the conventional circuit in the conventional technology requires time T1 to complete signal establishment. It can be learned from FIG. 4a to FIG. 4c that, from the moment t_1 to the moment t_4, the parasitic capacitor Cp is in a discharging process, and consequently, a process in which the light emitting diode D 1 changes from off to on experiences a relatively long time. A larger parasitic capacitor Cp leads to longer time from t_1 to t_4, and a ghost phenomenon is more easily observed by a human eye. This affects user experience.

[0044] In the pixel drive circuit 310 provided in this embodiment of this application, the charge absorption circuit 311 connected to the node A may absorb the charge on the node A when the parasitic capacitor Cp performs discharging, to accelerate a discharging process and accelerate a refresh frequency of the light emitting diode D1. As shown by an "optimized circuit" curve in FIG. 4b, because the charge absorption circuit 311 accelerates the discharging process, the current I_{D1} in the light emitting diode D1 can reach the maximum value more quickly and can be stable, so that the light emitting diode D1 can normally emit light. As shown in FIG. 4d, a voltage of the node A in the pixel drive circuit 310 decreases and approaches a normal working voltage after time T2 elapses, and then reaches the normal working voltage after time T3 elapses. Compared with the time T3, the pixel driver circuit 310 provided in this embodiment of this application can reduce the voltage of the node B to the normal working voltage in shorter time, to accelerate signal establishment time of the light emitting diode D 1, and increase a switching frequency of the light emitting diode D1, so that ghost is eliminated, display precision is improved, and user experience is improved.

[0045] FIG. 5 shows a more specific pixel drive circuit 310 according to an embodiment of this application. The charge absorption circuit 311 includes a capacitor Ca. In the foregoing discharging process, charges in the parasitic capacitor Cp may be absorbed by the capacitor Ca by using the first switch M1 and the node A, and this is equivalent to redistributing charges in the capacitor Ca and the parasitic capacitor Cp, so that the discharging process of the node B is accelerated. A capacitance value of the capacitor Ca is related to a capacitance value of the parasitic capacitor Cp. When the capacitance value of the parasitic capacitor Cp is relatively large, the capacitor Ca also requires a relatively large capacitance value. In addition, when the first switch M1 is opened, a larger voltage difference between the node B and the node A indicates a larger capacitance value required by the capacitor Ca.

[0046] The capacitor Ca may be a metal-insulator-metal (MIM) capacitor, a metal-oxide-metal (MOM) capacitor, or a metal-oxide-semiconductor (MOS) capacitor

[0047] FIG. 6 shows another more specific pixel drive circuit 310 according to an embodiment of this application. The charge absorption circuit 311 includes a diode-connected MOS transistor. Specifically, the diode-connected MOS transistor includes an NMOS transistor M3 and an NMOS transistor M4. A drain and a gate of the NMOS transistor M3 are connected to the node A, a drain of the NMOS transistor M4 is connected to a source of the NMOS transistor M3, a source of the NMOS transistor M4 is grounded, and a gate of the NMOS transistor M4 is also connected to the node A.

[0048] In the foregoing discharging process, charges in the parasitic capacitor Cp may flow to the ground by using the conductive NMOS transistor M3 and the conductive NMOS transistor M4. Specifically, after the first switch M1 is closed, the voltage of the node A increases. In this case, the NMOS transistor M3 and the NMOS transistor M4 are turned on, and both the voltage of the node A and the voltage of the node B rapidly decrease. When the voltage of the node A decreases and approaches the normal working voltage, the NMOS transistor M3 and the NMOS transistor M4 are cut off. After the NMOS transistor M3 and the NMOS transistor M4 are cut off, the second switch M2 continues to perform discharging

for the node A and the node B, so that the node B reaches a voltage at which the light emitting diode D1 works normally.

[0049] FIG. 7 shows still another more specific pixel drive circuit 310 according to an embodiment of this application. The charge absorption circuit 311 includes a Schottky diode D2. A cathode of the Schottky diode D2 is electrically connected to the node A, and the anode is grounded. The Schottky diode D2 may also accelerate absorption of the charge on the node A, so that the pixel driver 310 can reduce the node B to the normal working voltage in shorter time, to accelerate signal establishment time of the light emitting diode D 1, and increase a switching frequency of the light emitting diode D1, so that ghost is eliminated, display precision is improved, and user experience is improved.

[0050] FIG. 8 shows yet another more specific pixel drive circuit 310 according to an embodiment of this application. The pixel drive circuit 310 shown in FIG. 8 further includes a fifth switch M5 connected between the second switch M2 and the ground. The fifth switch M5 may be an NMOS transistor. In an implementation, a drain of the fifth switch M5 is connected to a source of the second switch M2, a source of the fifth switch M5 is grounded and connected to one end of the capacitor Cgg, and a gate of the fifth switch M5 is connected to a gate of the second switch M2 and the other end of the capacitor Cgg, to receive a bias voltage VBIAS. The charge absorption circuit 311 in FIG. 8 may be any charge absorption circuit provided in embodiments of this application.

[0051] As shown in FIG. 8, an embodiment of this application further provides a bias circuit 320. The bias circuit 320 includes a sixth switch M6, a seventh switch M7, and an eighth switch M8. In an implementation, the sixth switch M6 and the seventh switch M7 are NMOS transistors, and the eighth switch M8 is a PMOS transistor. A source of the sixth switch M6 is grounded, a gate is connected to a gate of the seventh switch M7, and a bias voltage VBIAS is generated. A drain of the sixth switch M6 is connected to a source of the seventh switch M7. A drain of the seventh switch M7 is separately connected to the gate of the seventh switch M7 and a drain of the eighth switch M8, and a source of the eighth switch M8 is connected to a power supply. The bias circuit 320 may provide a bias voltage for any pixel drive circuit provided in embodiments of this application.

[0052] In an implementation, one bias circuit 320 and the pixel drive circuit 310 may be separately disposed on different chips. The bias circuit 320 may provide a bias voltage VBIAS for a plurality of pixel drive circuits 310. In another implementation, the bias circuit 320 and one or more pixel drive circuits 310 may alternatively be integrated into a same chip.

[0053] As shown in FIG. 9, an embodiment of this application further provides a pixel drive circuit 900. A circuit structure of the pixel drive circuit 900 is similar to a structure of the pixel drive circuit 310, and a difference is that a charge absorption circuit 310 in the pixel drive circuit 900 is connected to a cathode of a light emitting diode D1 by using a ninth switch M9. The charge absorption circuit 310 in the pixel drive circuit 900 may be any charge absorption circuit in embodiments of this application. One end of the ninth switch M9 is connected to one end of the charge absorption circuit 310, the other end is connected to the cathode of the light emitting diode D1, and a PWM signal received by a gate of the ninth switch M9 is the same as a PWM signal received by the first switch M1. In normal operation, because the PWM signal controls on and off of both the first switch M1 and the ninth switch M9, after the two switches are closed, the charge absorption circuit 310 starts to absorb a charge on the light emitting diode D1, to accelerate release of a charge on the cathode of the light emitting diode D1, so that the charge in a parasitic capacitor can be released more quickly. When a charge release speed in the parasitic capacitor is accelerated, current signal establishment time of the light emitting diode is shortened, and a refresh frequency of the light emitting diode is increased, so that time experienced by the light emitting diode in a process from an extinct state to a lighted state is shortened, a ghost phenomenon caused when a human eye observes the light emitting diode can be improved, display precision of the light emitting diode is improved, and user experience is improved.

[0054] In addition to the foregoing terminal device mentioned in embodiments of this application, the pixel drive circuit provided in embodiments of this application may be further used by another device, such as an ultra-large indoor display screen, a helmet-mounted display (helmet-mounted displays, HMD), a head up display (HUD), Light Fidelity (Li-Fi), augmented reality (AR), and virtual reality (VR).

[0055] The foregoing descriptions are merely specific implementations of this application, but are not intended to limit the protection scope of this application. Any variation or replacement readily figured out by a person skilled in the art within the technical scope disclosed in this application shall fall within the protection scope of this application. Therefore, the protection scope of this application shall be subject to the protection scope of the claims.

Claims

1. A pixel drive circuit, wherein the pixel drive circuit comprises:

a first switch and a second switch that are cascaded between a cathode of a light emitting diode and the ground, wherein a control end of the first switch receives a control signal, a control end of the second switch receives a bias voltage, and an anode of the light emitting diode is electrically connected to a power supply; and
and a charge absorption circuit, electrically con-

nected between the ground and a first node, wherein the first node is a connection point of the first switch and the second switch, and the charge absorption circuit is configured to absorb a charge from the first node.

2. The pixel drive circuit according to claim 1, wherein the charge absorption circuit comprises a first capacitor, wherein one end of the first capacitor is electrically connected to the first node, and the other end is electrically connected to the ground.

3. The pixel drive circuit according to claim 2, wherein the first capacitor is a metal-insulator metal, MIM, capacitor, a metal-oxide-metal, MOM, capacitor, or a metal-oxide-semiconductor, MOS, capacitor.

4. The pixel drive circuit according to claim 1, wherein the charge absorption circuit comprises a diode-connected MOS transistor

5. The pixel drive circuit according to claim 4, wherein the diode-connected MOS transistor comprises:

a third NMOS transistor, wherein a drain and a gate of the third NMOS transistor are electrically connected to the first node; and
and a fourth NMOS transistor, wherein a drain of the fourth NMOS transistor is electrically connected to a source of the third NMOS transistor, a source of the fourth NMOS transistor is grounded, and a gate of the fourth NMOS transistor is electrically connected to the first node.

6. The pixel drive circuit according to claim 1, wherein the charge absorption circuit comprises a Schottky diode, a cathode of the Schottky diode is electrically connected to the first node, and an anode of the Schottky diode is grounded.

7. The pixel drive circuit according to any one of claims 1 to 6, wherein the first switch is a first NMOS transistor, the second switch is a second NMOS transistor, wherein a source of the first NMOS transistor is electrically connected to the ground, a drain of the first NMOS transistor and a source of the second NMOS transistor are electrically connected to the first node, and a drain of the second NMOS transistor is electrically connected to the cathode of the light emitting diode.

8. The pixel drive circuit according to any one of claims 1 to 7, wherein the pixel drive circuit further comprises a second capacitor, wherein one end of the second capacitor is electrically connected to the control end of the second switch, and the other end is grounded.

9. The pixel drive circuit according to any one of claims 1 to 8, wherein the control signal is a pulse width modulation, PWM, signal.

10. A display circuit, wherein the display circuit comprises:

a plurality of pixel drive circuits according to any one of claims 1 to 9; and
a plurality of light emitting diodes, separately electrically connected to the plurality of pixel drive circuits, wherein the plurality of pixel drive circuits are configured to separately drive the plurality of light emitting diodes.

11. A terminal device, comprising a rear cover, a bezel, and the display circuit according to claim 10, wherein the rear cover and the display circuit are disposed opposite to each other and are connected by using the bezel.

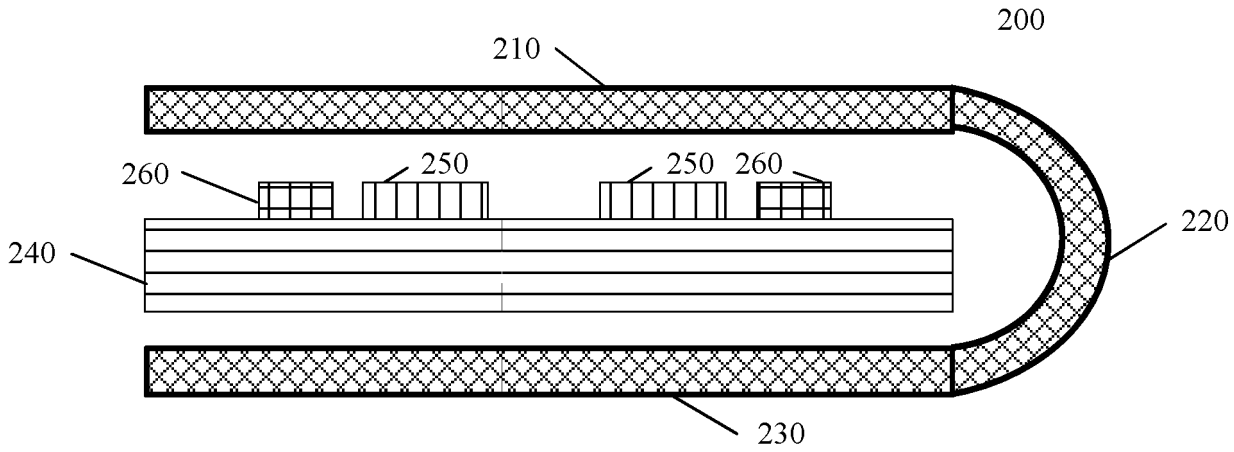

FIG. 1

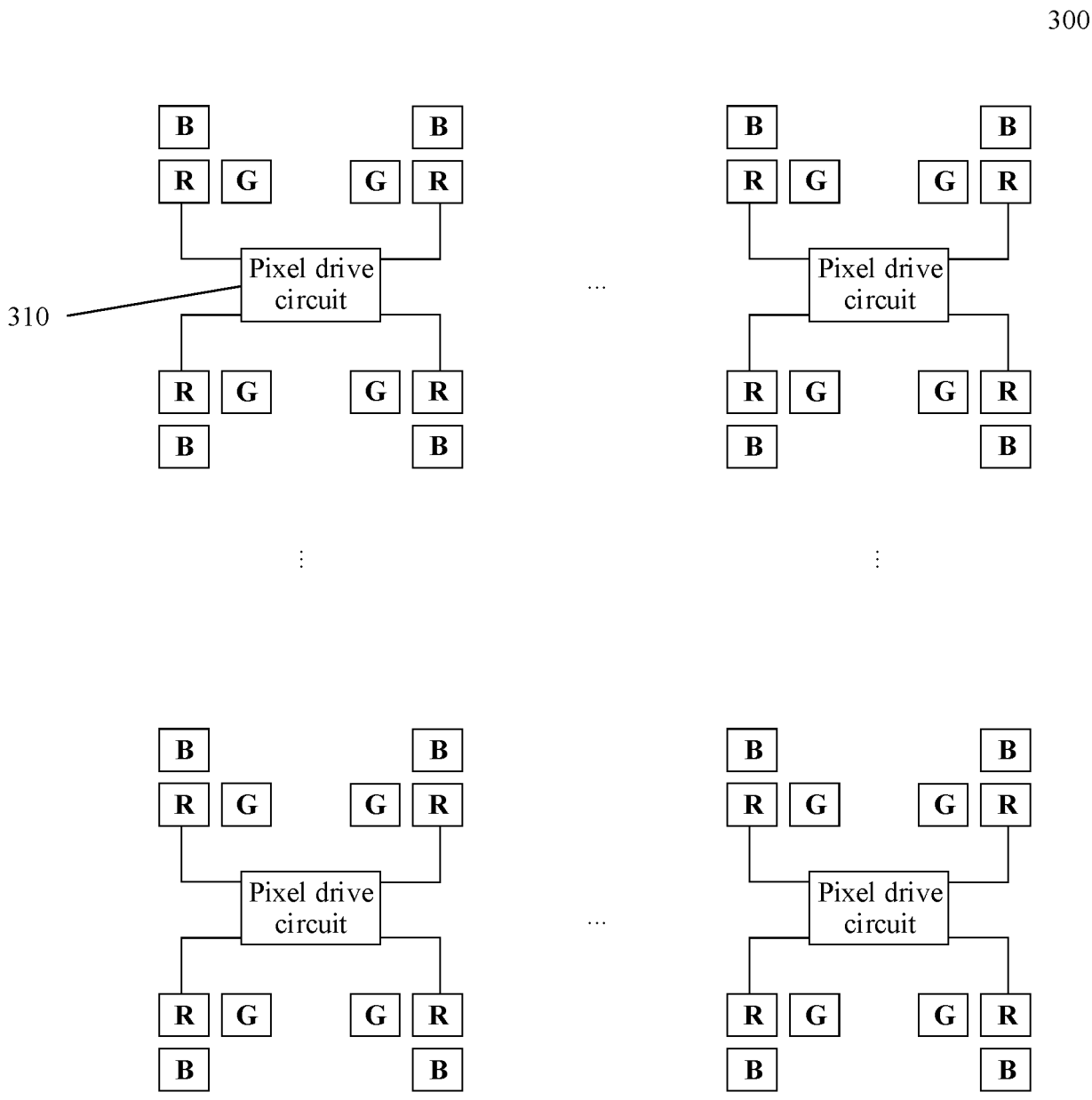

FIG. 2

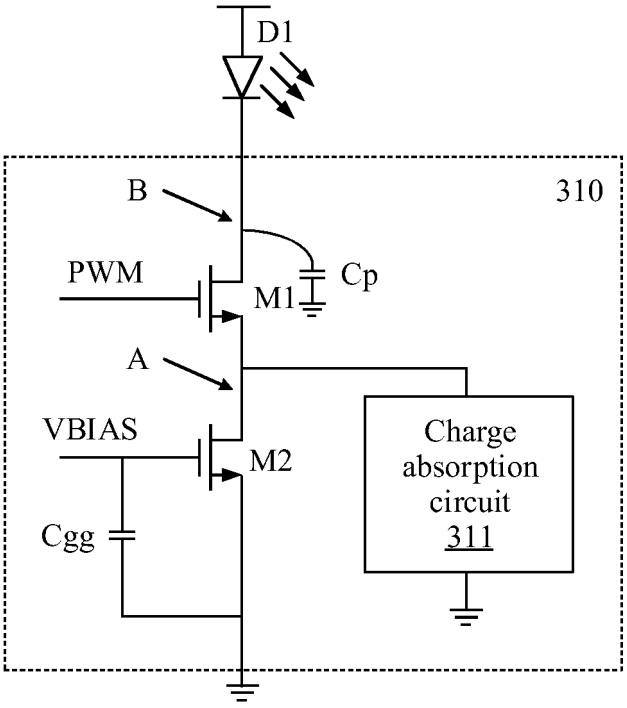
D1
B
310
PWM
M1
Cp
A
VBIAS
M2
Cgg
Charge
absorption
circuit
311

FIG. 3

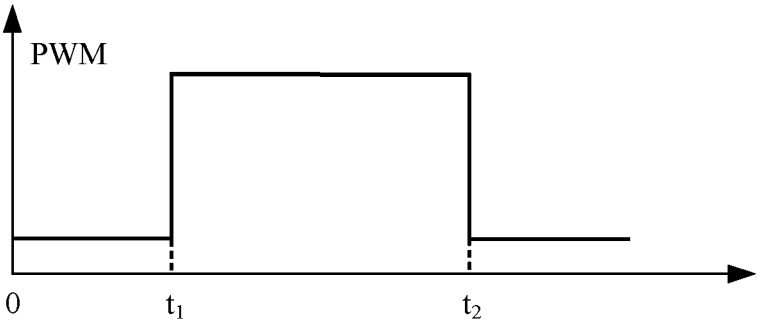

FIG. 4a

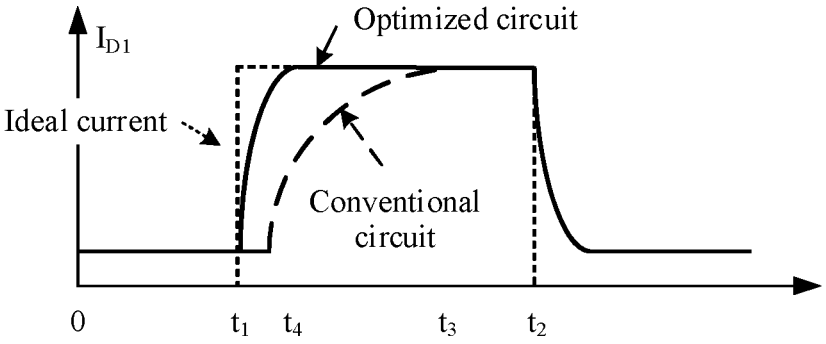

FIG. 4b

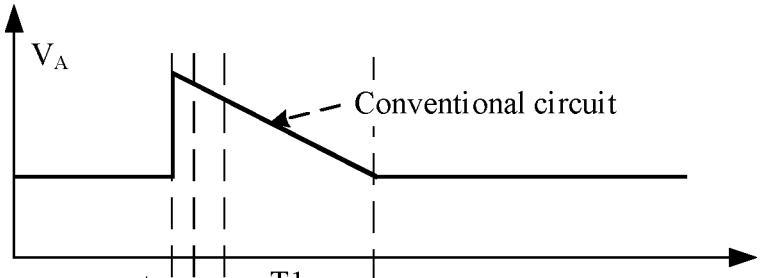

FIG. 4c

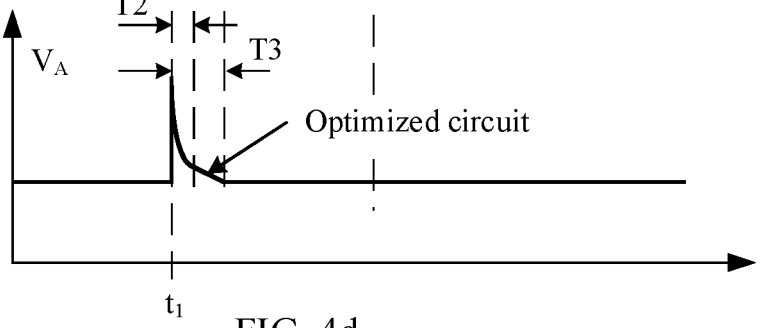

FIG. 4d

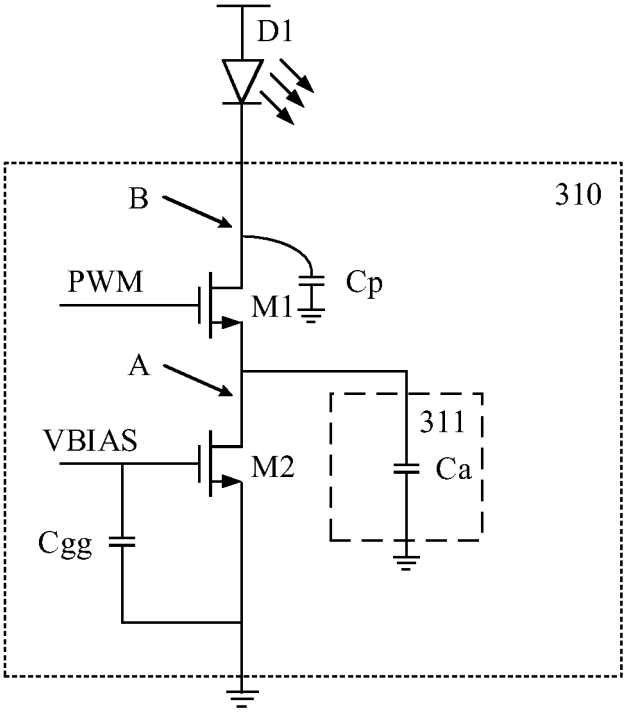
D1
310
B
PWM
M1
Cp
A
311
VBIAS
M2
Ca
Cgg

FIG. 5

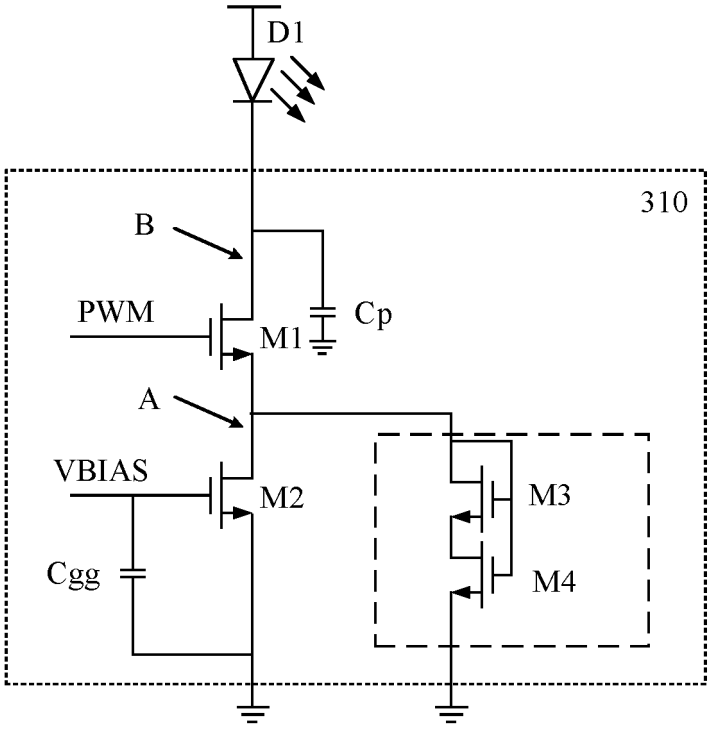
D1
310
B
PWM
M1
Cp
A
VBIAS
M2
M3
M4
Cgg

FIG. 6

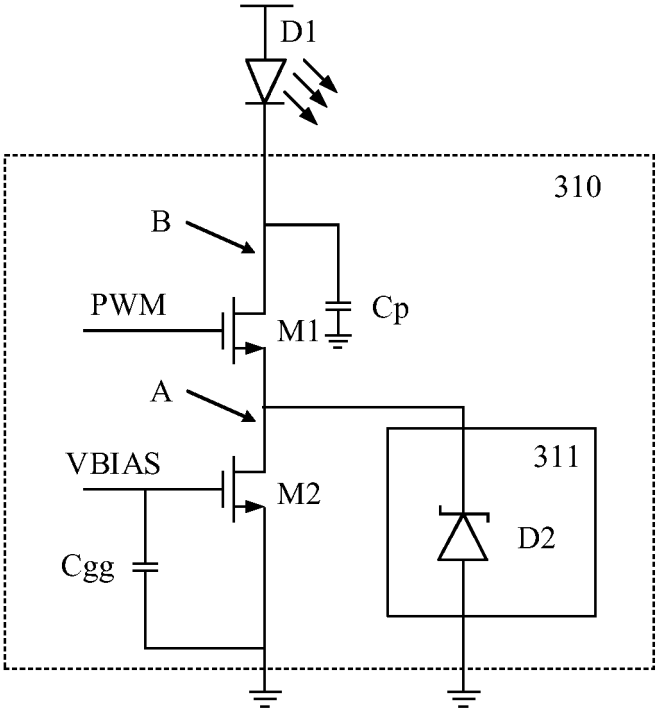

FIG. 7

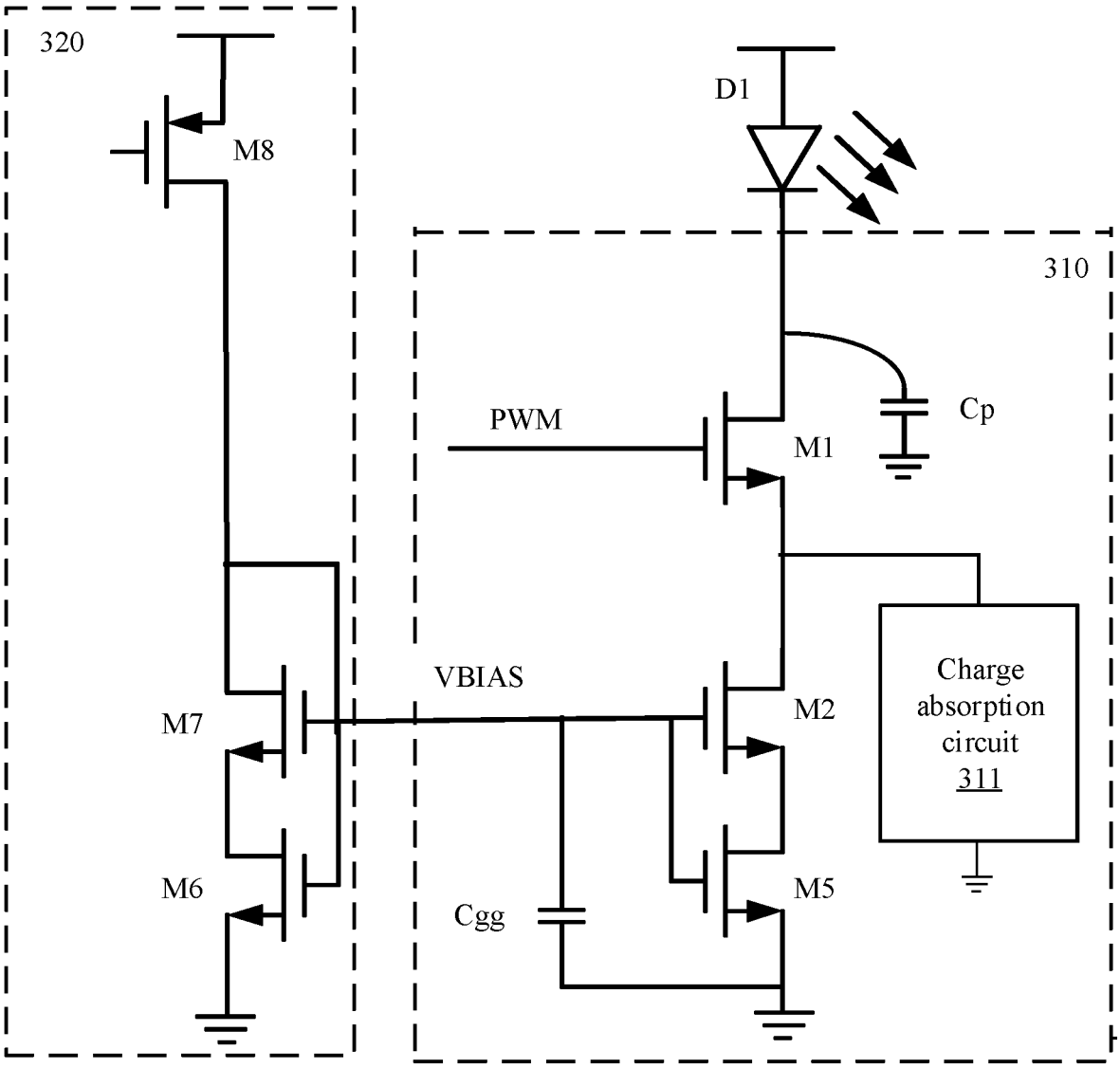
320
M8
D1
310
PWM
M1
Cp
VBIAS
M2
Charge
absorption
circuit
311
M7
M6
Cgg
M5

FIG. 8

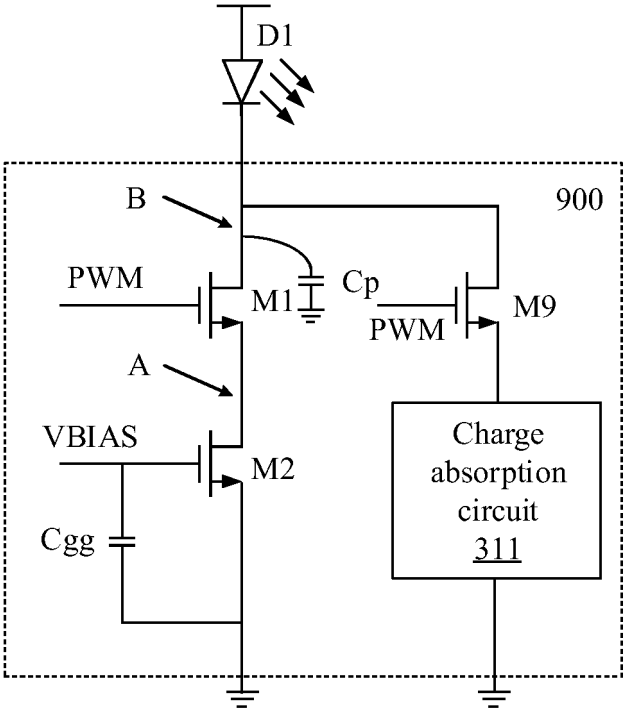
D1
B
900
PWM
M1
Cp
PWM
M9
A
VBIAS
M2
Cgg
Charge absorption circuit 311

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/099448

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS; CNTXT; CNKI; VEN; USTXT; EPTXT; WOTXT: 华星光电, 华为, 残影, 放电, 电容, 微, 重影, 二极管, 寄生, 残像, 鬼影, 肖特基, 电荷吸收, LED, Vbias, PWM, capacit+, ghost+, micro, discharge

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 110930936 A (NOVATEK MICROELECTRONICS CORP.) 27 March 2020 (2020-03-27) description, paragraphs [0075]-[0110], and figures 1-10	1-11
Y	WO 2019108553 A1 (PLANAR SYSTEMS, INC.) 06 June 2019 (2019-06-06) description, paragraphs [0015]-[0034], and figures 1-5	1-11
Y	CN 103426396 A (MACROBLOCK, INC.) 04 December 2013 (2013-12-04) description paragraph [0009], figures 3, 4	4, 5, 7-11
A	CN 103258499 A (GUANGZHOU GUIXIN ELECTRONIC TECHNOLOGY CO., LTD.) 21 August 2013 (2013-08-21) entire document	1-11
A	CN 106952610 A (SHENZHEN SUNMOON MICROELECTRONICS CO., LTD.) 14 July 2017 (2017-07-14) entire document	1-11

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2021	**18 March 2021**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088** **China**	Authorized officer
Facsimile No. **(86-10)62019451**	Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2020/099448

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	110930936	A	27 March 2020	US	2020090578	A1	19 March 2020
WO	2019108553	A1	06 June 2019	CN	111373468	A	03 July 2020
CN	103426396	A	04 December 2013	TW	201349206	A	01 December 2013
				TW	I459351	B	01 November 2014
				US	2013314307	A1	28 November 2013
				KR	101435718	B1	01 September 2014
				KR	20130131203	A	03 December 2013
				EP	2667375	A1	27 November 2013
				JP	2013246430	A	09 December 2013
CN	103258499	A	21 August 2013	CN	103258499	B	17 August 2016
				US	9047810	B2	02 June 2015
				US	2012206430	A1	16 August 2012
CN	106952610	A	14 July 2017	CN	207115972	U	16 March 2018

Form PCT/ISA/210 (patent family annex) (January 2015)