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(54) **MEMORY AND MANUFACTURING METHOD THEREFOR**

(57) A memory and a method for manufacturing the same are provided. The memory includes: a substrate (20) including an isolation structure (21) and an active area (22) between adjacent isolation structures (21); a first gate structure, the first gate structure locates in a first groove (213) of the isolation structure (21), includes a first gate filled in the first groove (213), and the first gate includes a first conductive layer (23) filled at the bottom of the first groove (213) and a second conductive layer (24), the second conductive layer locates above the first conductive layer (23), and the work function of the material of the first conductive layer (23) is greater than that of the material of the second conductive layer (24); a second gate structure, located in the second groove of the active area, includes a second gate filled in the second groove, and the material of the second gate is the same as that of the second conductive layer.

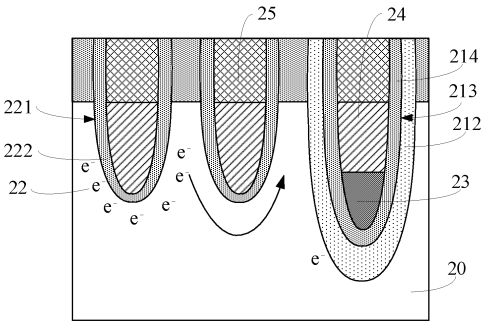

FIG. 17

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Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to the Chinese Patent Application No. 202010802218.4, filed on August 11, 2020, entitled "MEMORY AND METHOD FOR MANUFACTURING SAME", which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The disclosure relates to the field of semiconductors, in particular to a memory and a method for manufacturing the same.

BACKGROUND

[0003] The memory is a memory component for storing programs and various data information, and can be classified into a read-only memory and a random access memory according to the types of the memory used. The memory typically includes a capacitor and a transistor connected with the capacitor. The capacitor is configured to store a charge representative of the stored information and the transistor is a switch for controlling the inflow and discharge of the charge of the capacitor. The transistor has a source, a drain, and a gate, and the gate is connected to the word line.

[0004] However, with the increasing miniaturization of process nodes, the problem of memory signal interference becomes increasingly serious, and how to solve this problem has become an important issue of memory process optimization.

SUMMARY

[0005] The disclosure provides a memory and a method for manufacturing the same, which facilitate the reduction of signal interference between active areas on both sides of an isolation structure.

[0006] To address the above problem, the disclosure provides a memory including: a substrate, the substrate includes an isolation structure and an active area between adjacent isolation structures; a first gate structure, the first gate structure locates in a first groove of the isolation structure, and includes a first gate filled in the first groove, and the first gate includes a first conductive layer filled at the bottom of the first groove and a second conductive layer located above the first conductive layer, and the work function of the material of the first conductive layer is greater than that of the material of the second conductive layer; a second gate structure, the second gate structure located in a second groove of the active area, and includes a second gate filled in the second groove, and the material of the second gate is the same as that of the second conductive layer.

[0007] Furthermore, the first gate structure includes a first gate dielectric layer covering the bottom surface and sidewalls of the first groove, and the second gate structure includes a second gate dielectric layer covering the bottom surface and sidewalls of the second groove. The material of the first gate dielectric layer is the same as that of the second gate dielectric layer.

[0008] Furthermore, the thickness of the first gate dielectric layer in the direction perpendicular to the surface of the substrate is greater than the thickness of the first gate dielectric layer in the direction parallel to the surface of the substrate.

[0009] Furthermore, the first gate structure further includes a first blocking layer covering the surface of the first gate dielectric layer, and the first blocking layer is configured to block the migration of metal ions in the first gate towards the first gate dielectric layer.

[0010] Furthermore, the second gate structure further includes a second blocking layer covering the surface of the second gate dielectric layer, and the second blocking layer is configured to block the migration of metal ions in the second gate towards the second gate dielectric layer.

[0011] Furthermore, the material of the first blocking layer is the same as that of the second blocking layer.

[0012] Furthermore, the depth of the first gate in the substrate is greater than that of the second gate in the substrate.

[0013] Furthermore, the first groove has a first depth in the substrate, and the second groove has a second depth in the substrate, and the difference between the first depth and the second depth is 10% to 50% of the first depth.

[0014] Furthermore, the isolation structure further includes a third groove that has an opening width less than that of the first groove in the direction parallel to the surface of the substrate, and the third groove is filled with a third gate structure which has a material same as that of the second gate structure.

[0015] Furthermore, the isolation structure further includes a third groove that has an opening width less than that of the first groove in the direction parallel to the surface of the substrate, and third groove is filled with a third gate structure which has a material same as that of the first gate structure.

[0016] Furthermore, in the direction perpendicular to the surface of the substrate, the top surface of the first conductive layer is lower than or flush with the bottom surface of the second gate.

[0017] Furthermore, in the direction perpendicular to the surface of the substrate, the thickness of the first conductive layer is in a range of 1 nm to 5 nm.

[0018] Furthermore, the material of the first conductive layer includes at least one of titanium nitride, tungsten, nickel or cobalt.

[0019] Furthermore, the material of the first conductive layer includes tungsten, and the crystal orientations of the tungsten in the first conductive layer include [100] and [110].

[0020] Furthermore, the material of the second con-

ductive layer includes tungsten, and the crystal orientation of the tungsten in the second conductive layer includes [111], [113], or [116],

[0021] Correspondingly, the disclosure further provides a method for manufacturing a memory, the method includes following acts. A substrate is provided. The substrate includes an isolation structure and an active area between adjacent isolation structures. An etching process is performed to form a first groove in the isolation structure and a second groove in the active area. A first deposition process is performed to form a first conductive layer filled at the bottom of the first groove. A second deposition process is performed to form a second conductive layer filled above the first conductive layer and in the second groove. The work function of the first conductive layer is greater than that of the second conductive layer. The first conductive layer and the second conductive layer filled in the first groove form a first gate. The second conductive layer filled in the second groove forms a second gate.

[0022] Furthermore, before performing the first deposition process, the method further includes the following acts. A first gate dielectric layer covering the bottom surface and the sidewalls of the first groove and a second gate dielectric layer covering the bottom surface and the sidewalls of the second groove are formed. The material of the first gate dielectric layer is the same as that of the second gate dielectric layer.

[0023] Furthermore, before performing the first deposition process, the method further includes following acts. A first blocking layer covering the surface of the first gate dielectric layer is formed. The first blocking layer is configured to block the migration of metal ions in the first gate towards the first gate dielectric layer.

[0024] Furthermore, the first blocking layer and a second blocking layer covering the surface of the second gate dielectric layer are formed in the same process. The second blocking layer is configured to block the migration of metal ions in the second gate towards the second gate dielectric layer.

[0025] Furthermore, in the direction perpendicular to the surface of the substrate, the depth of the first groove of the isolation structure is greater than that of the second groove of the active area.

[0026] As compared to the related art, the disclosure has the following advantages:

[0027] In the above-described technical solutions, as compared to the second gate, the first gate further has a first conductive layer with a greater work function of material, so that the first gate structure has a higher threshold voltage than the second gate structure. In the case that the operating voltage applied to the first gate remains unchanged, the higher the threshold voltage of the first gate structure is, and the less electrons are capable of being actuated by the operating voltage, so that the number of electrons gathered in the channel region below the isolation structure decreases, and it is difficult to form a channel. In this way, it is difficult for the electrons to transition from one active area to another through the channel region, thereby reducing the signal interference between active areas on both sides of an isolation structure.

[0028] In addition, the depth of the first gate in the substrate is greater than that of the second gate in the substrate. In this way, it is advantageous to reduce the resistance of the portion of the word line in the isolation structure, thus improving the capability of the signal transmission of the word line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] One or more examples are illustrated by the figures of the appended drawings, which are not to be construed as a limitation of the examples, and elements in the drawings have the same reference numerals are represented as similar elements. Unless otherwise indicated, the figures in the drawings do not constitute a limitation in scale.

FIGs. 1 to 3 are schematic structural diagrams of a memory;

FIGs. 4 to 17 are schematic cross-sectional structure diagrams corresponding to each step of a method for manufacturing a memory according to an example of the disclosure.

DETAILED DESCRIPTION

[0030] Referring to FIG. 1, a memory includes an active area 12 and an isolation structure 13 located between adjacent active areas 12; and bit lines are located above the active area 12 and the isolation structure 13, and word lines 11 are located in the active area 12 and the isolation structure 13. FIG. 2 is a schematic cross-sectional diagram in the first cross-sectional direction of the memory shown in FIG. 1. FIG. 3 is a cross-sectional diagram in the second cross-sectional direction of the memory shown in FIG. 1.

[0031] As the word line 11 is located in both the active area 12 and the isolation structure 13, in the process of etching to form the word line 11, the gate structure 133 is also formed in the isolation structure 13 besides that the gate structure 133 formed in the active area 12. The gate structure 133 consists of the gate 135 and the gate dielectric layer 134.

[0032] As the gate structure 133 is provided in the isolation structure 13, when an operating voltage is applied to the word line 11, the gate 135 in the isolation structure 13 actuates electrons in the active areas 12 located at both sides of the isolation structure 13, and the actuated electrons will gather in the channel region located below the isolation structure 13, thereby forming a channel. The electrons can transition between adjacent active areas 12 through the channel, thereby causing signal interference. The number of actuated electrons is associated

with the threshold voltage of the gate structure 133. Under the same operating voltage, the higher the threshold voltage is, the less electrons actuated by the gate 135.

[0033] The value of the threshold voltage is associated with the width L of the gate 135 in the first cross-sectional direction AA. The greater the width L is, the larger the electric field of the gate 135 is at an operating voltage, and the less the threshold voltage is; In addition, the threshold voltage is also related to the depth d of the gate 134 in the substrate 10. The greater the depth d is, the stronger the electric field the gate 135 has in a working voltage, and thus the threshold voltage is lower.

[0034] According to the width L in the first cross-sectional direction AA, the isolation structure 13 may be divided into two kinds, i.e., the first isolation structure 131 and the second isolation structure 132. The width L of the first isolation structure 131 is less than the width L of the second isolation structure 132. As the width L of the second isolation structure 132 is greater, the intensity of electric field of the gate 135 in the second isolation structure 132 is relatively high, and the threshold voltage is relatively low, so that the electrons in the active area 12 located at both sides of the second isolation structure 132 are more likely to be actuated to transition, thereby causing signal interference.

[0035] On the contrary, as the width L of the first isolation structure 131 is relatively narrow, the intensity of electric field of the gate 135 in the first isolation structure 131 is relatively low, and the threshold voltage is relatively high, so that the electrons in the active area 12 located at both sides of the first isolation structure 131 are not likely to be actuated to transition, and thus signal interference problem is relatively unserious.

[0036] In order to solve the above problem, the disclosure provides a memory and a method for manufacturing the same. By providing a first conductive layer located at the bottom of a first groove in addition to a second conductive layer, the first gate structure has a relatively high threshold voltage and a second gate structure has a relatively low threshold voltage. Under the condition that the operating voltage applied to the first gate remains unchanged, the threshold voltage of the first gate structure is relatively high, and the number of actuated electrons is less, and the number of electrons gathered in a channel region below the isolation structure is less, so that it is difficult to form a channel. In this way, it is difficult for the electrons to transition from one active area to another through the channel region, thereby reducing signal interference between the active areas at both sides of the isolation structure.

[0037] In order to make the purposes, technical solutions, and advantages of the examples of the disclosure clearer, each example of the disclosure will be described in detail with reference to the appended drawings. However, it will be appreciated by those skilled in the art that in various examples of the disclosure, numerous technical details are set forth in order to enable the reader to better understand the disclosure, but the technical solution of disclosure can also be achieved without these technical details and various changes and modifications based on the following examples.

[0038] FIGs. 4 to 17 are schematic cross-sectional structures corresponding to each step of a method for manufacturing a memory according to an example of the disclosure. For ease of understanding, schematic cross-sectional structures of the first cross-sectional direction AA and the second cross-sectional direction BB are provided for each of manufacturing steps.

[0039] Referring to FIGs. 4 and 5, a substrate 20 is provided. The substrate 20 includes an isolation structure 21 and an active area 22 located between adjacent isolation structures 21.

[0040] In this example, in the first cross-sectional direction AA, the isolation structure 21 includes a first isolation structure 211 and a second isolation structure 212 with different widths. The width of the second isolation structure 212 is greater than that of the first isolation structure 211. The depth of the second isolation structure 212 in the substrate 20 is greater than that of the first isolation structure 211 in the substrate 20 due to an etch loading effect.

[0041] "Etching loading effect" means that under the same etching process, the depth of the groove formed by etching is related to the width of the opening of at the top of the groove. The wider the opening at the top is, the more plasma gas acting on the etching is, so that the depth of the groove is deeper.

[0042] In this example, a dielectric layer 20a is further provided at the top of the substrate 20, and can be used to protect the substrate 20 or to support other structures. For concision of illustration, the dielectric layer 20a is not shown in a schematic cross-sectional structure diagram in the first cross-sectional direction AA.

[0043] Referring to FIGs. 6 and 7, an etching process is performed to form a first groove 213 in the isolation structure 21 and a second groove 221 in the active area 22.

[0044] In this example, the depth of the first groove 213 in the substrate 20 is greater than that of the second groove 221 in the substrate 20, so that a thicker gate in the direction perpendicular to the surface of the substrate 20 can be formed by subsequent filling, thereby reducing the resistance of the word line in the second isolation structure 212. In other examples, the depth of the first groove in the substrate is equal to or less than that of the second groove in the substrate.

[0045] In this example, with the depth of the first groove 213 being greater than that of the second groove 221, it is also advantageous for the first conductive layer subsequently filled at the bottom of the first groove 213 to be staggered from the second gate subsequently filled in the second groove 221 in the direction perpendicular to the surface of the substrate 20, so that the presence of the first conductive layer does not affect the performance of the second gate.

[0046] The depth of the first groove 213 in the substrate

20 is associated with the resistance of the first gate subsequently formed in the first groove 213 and the threshold voltage of the first gate structure. Specifically, the first gate structure includes a first gate and a first gate dielectric layer. Where the thickness of the first gate dielectric layer is same, the deeper the depth of the first groove 213 is, the larger the cross-sectional area of the first gate subsequently formed is in the direction perpendicular to the substrate 20, so that the resistance of the first gate is less in the extending direction of the word line. In addition, where the same conductive material is filled, the deeper the depth of the first groove 213 is, the lager the size of the first gate is, the greater the intensity of the electric field of the first gate is, so that the threshold voltage of the first gate structure is lower.

[0047] In this example, the first groove 213 has a first depth in the substrate 20, and the second groove 221 has a second depth in the substrate 20. There is a first depth difference between the first depth and the second depth. The first depth difference d1 is 10% to 50%, for example, 20%, 30% or 40% of the depth of the first groove 213. When the first depth difference d1 is too small, it is not advantageous to reduce the resistance of the word line in the second isolation structure 212, and it is prone for the first conductive layer subsequently formed to overlap with the front projection of the second gate filled in the second groove 221 in the direction parallel to the surface of the substrate, thereby affecting the performance of the second gate. When the first depth difference d1 is too large, it is prone to cause etching defects due to the overlarge width-depth ratio.

[0048] In this example, in the etching process, a third groove 215 is formed in the first isolation structure 211, and a first groove 213 is formed in the second isolation structure 212. The width of the opening of the third groove 215 is less than the width of the opening of the first groove 213 in the direction parallel to the surface of the substrate 20. The depth of the third groove 215 is less than that of the first groove 213 due to the etch loading effect. As the width of the opening of the third groove 215 is less than that of the first groove 213, and the depth of the third groove 215 is less than that of the first groove 213, under the same thickness of the gate dielectric layers and the same conductive material of the gate, the threshold voltage of the gate structure in the third groove 215 is lower than that of the gate structure in the first groove 213, so that electrons of the active areas 22 at both sides of the second isolation structure 212 are prone to be actuated to gather in the channel region below the second isolation structure 212, thereby causing electronic transitions and signal interference.

[0049] As an illustrative example, the gate in the second isolation structure 212 is adjusted to increase the gate threshold voltage, that is, the gate structure in the second isolation structure 212 is different from that in the first isolation structure 211, and only the first conductive layer is formed subsequently in the second isolation structure 212. In fact, the first conductive layer may also be filled in the third groove 215. In other words, the material of the gate structure in the third groove 215 is the same as that of the gate structure in the first groove 213.

[0050] In this example, the gate structure in the first groove 213 is referred to as a first gate structure, the gate structure in the active area 22 is referred to as a second gate structure, and the gate structure in the third groove 215 is referred to as a third gate structure. The material of the third gate structure is the same as that of the second gate structure.

[0051] Referring to FIGs. 8 and 9, a first gate dielectric layer 214 covering the bottom surface and sidewalls of the first groove 213 and a second gate dielectric layer 222 covering the bottom surface and sidewalls of the second groove 221 are formed.

[0052] In this example, in the same deposition process, the first gate dielectric layer 214 and the second gate dielectric layer 222 are formed. The material of the first gate dielectric layer 214 is the same as that of the second gate dielectric layer 222. In addition, the first gate dielectric layer 214 is also located above the active area 22.

[0053] The thickness of the first gate dielectric layer 214 is associated with the threshold voltage of the first gate structure and the resistance of the word line in the second isolation structure 212. Specifically, the thicker the first gate dielectric layer 214 is, the greater the isolation effect of the first gate dielectric layer 214 on the electric field of the first gate is. In addition, the first gate dielectric layer 214 is relatively thick, the reserved space of the first gate is less, the size of the first gate is smaller, the intensity of electric field of the first gate is less, and the threshold voltage of the first gate structure is higher. In addition, the less the size of the first gate is, the less the resistance of the word line in the second isolation structure 212 is.

[0054] To reach both a higher threshold voltage of the first gate structure and a lower resistance of the word lines in the second isolation structure 212, the first gate dielectric layer 214 can be provided so that its first thickness d2 in the direction perpendicular to the surface of the substrate 20 is thicker than its second thickness d3 in the direction parallel to the surface of the substrate 20.

[0055] In this example, referring to FIGs. 10 to 13, a first deposition process is performed to form a first conductive layer 23 filled at the bottom of the first groove 213.

[0056] The first deposition process includes the following acts. A first conductive film 231 filled up in the first groove 213 and the second groove 221 is formed. The first conductive film 231 is etched to form a first conductive layer 23 filled only at the bottom of the first groove 213.

[0057] In this example, the work function of the material of the first conductive layer 23 is greater than that of the material of the second conductive layer subsequently formed. In this way, it is advantageous to increase the work function of the first gate in the second isolation structure 212, thereby increasing the threshold voltage of the first gate structure. The higher the threshold voltage of

the first gate structure is, the more difficult it is to form a channel under the same operating voltage, that is, the more difficult it is for electrons to transition from the active area 22 on one side of the second isolation structure 212 towards the other active area 22 on the other side of the second isolation structure 212. By doing so, it is advantageous to reduce signal interference between the active areas 22 at two adjacent sides of the second isolation structure 212.

[0058] In this example, the material of the first conductive layer 23 includes at least one of titanium nitride, tungsten, nickel, or cobalt. The material of the first conductive layer 23 includes tungsten, and the crystal orientations of the tungsten of the first conductive layer 23 include [100] and [110]. It is noted that in the case that the material of the second conductive layer subsequently formed is also tungsten, the crystal orientation of the tungsten of the second conductive layer includes [111], [113] or [116], that is, the work function of the tungsten of the second conductive layer is less than that of the tungsten of the first conductive layer 23.

[0059] In this example, in the direction perpendicular to the surface of the substrate 20, the thickness of the first conductive layer 23 is in a range of 1 nm to 5 nm, for example, 2 nm, 3 nm, or 4 nm. In the case that the thickness of the first conductive layer 23 is too thin, the increase of the threshold voltage is less, so that the suppression of signal interference is weaker. In the case that thickness of the first conductive layer 23 is too thick, the performance of the second gate structure in the active area 22 may be affected.

[0060] In this example, before forming the first conductive layer 23, a first blocking layer (not shown) covering the bottom surface and sidewalls of the first gate dielectric layer 214 and a second blocking layer (not shown) covering the bottom surface and sidewalls of the second gate dielectric layer 222 are also formed. The material of the first blocking layer may be the same as that of the second blocking layer. The blocking layer is configured to block the migration of metal ions in the gate towards the gate dielectric layer and the substrate 20. The first blocking layer and the second blocking layer may be formed in the same process.

[0061] Referring to FIGs. 14 and 15, a second deposition process is performed to form a second conductive layer 24. The second conductive layer fills on the first conductive layer 23 and in the second groove 221.

[0062] In this example, the first conductive layer 23 and the second conductive layer 24 filled in the first groove 213 form a first gate; and the first gate and the first gate dielectric layer 214 form a first gate structure. The second conductive layer 24 filled in the second groove 221 forms a second gate; and the second gate and the second gate dielectric layer 222 form a second gate structure.

[0063] Referring to FIGs. 16 and 17, an isolation layer 25 is formed.

[0064] The isolation layer 25 is configured for electrical isolation. The material of the isolation layer 25 includes silicon nitride.

[0065] In this example, as compared to the second gate, the first gate further has a first conductive layer with a greater work function of material, so that the first gate structure has a higher threshold voltage than the second gate structure. In the case that the operating voltage applied to the first gate remains unchanged, as the threshold voltage of the first gate structure increases, the number of actuated electrons decreases, then the number of electrons gathered in the channel region below the isolation structure decreases, so that it is difficult to form the channel. In this way, it is difficult for the electrons to transition from one active area to another through the channel region, thereby reducing signal interference between the active areas at both sides of the isolation structure.

[0066] Correspondingly, an example of the disclosure further provides a memory which may be formed by the method for manufacturing a memory described above.

[0067] Referring to FIGs. 16 and 17, the memory includes: a substrate 20 including an isolation structure 21 and an active area 22 located between adjacent isolation structures 21; a first gate structure (not shown) located in a first groove 213 in the isolation structure 21, in which the first gate structure includes a first gate (not shown) filled in the first groove 213, and the first gate includes a first conductive layer 23 filled at the bottom of the first groove 213 and a second conductive layer 24 located above the first conductive layer 23, and the work function of the material of the first conductive layer 23 is greater than that of the material of the second conductive layer 24; a second gate structure (not shown), in which the second gate structure is located in the second groove 221 of the active area 22, and the second gate structure includes a second gate (not shown) filled in the second groove 221, and the material of the second gate is the same as that of the second conductive layer.

[0068] In this example, the first gate structure includes a first gate dielectric layer 214 covering the bottom surface and sidewalls of the first groove 213, and the second gate structure includes a second gate dielectric layer 222 covering the bottom surface and sidewalls of the second groove 221. The material of the first gate dielectric layer 214 is the same as that of the second gate dielectric layer 222.

[0069] In this example, the depth of the first gate in the substrate 20 is greater than that of the second gate in the substrate 20.

[0070] In this example, the isolation structure 21 further includes a third groove (not shown). In the direction parallel to the surface of the substrate 20, the width of the opening the first groove 213 is greater than that of the third groove. The third groove is filled with the third gate structure whose material is the same as that of the second gate structure.

[0071] In this example, in the direction perpendicular to the surface of the substrate 20, the top surface of the first conductive layer 23 is lower than or flush with the

bottom surface of the second gate.

[0072] In this example, the first gate structure further includes a first blocking layer located between the first gate and the first gate dielectric layer 214, and the second gate structure further includes a second blocking layer located between the second gate and the second gate dielectric layer 222. The material of the first blocking layer is the same as that of the second blocking layer.

[0073] In this example, in the direction perpendicular to the surface of the substrate 20, the thickness of the first conductive layer 23 is in a range of 1 nm to 5 nm, for example, 2 nm, 3 nm, or 4nm.

[0074] In this example, the material of the first conductive layer 23 includes at least one of titanium nitride, tungsten, nickel or cobalt. The material of the first conductive layer 23 comprises tungsten, and the crystal orientations of the tungsten of the first conductive layer 23 include [100] and [110]. It is noted that in the case that the material of the second conductive layer subsequently formed is also tungsten, and the crystal orientation of the tungsten of the second conductive layer includes [111], [113] or [116], that is, the work function of the tungsten of the second conductive layer is less than that of the tungsten of the first conductive layer 23.

[0075] In this example, as compared to the second gate, the first gate further has a first conductive layer with a greater work function of material, so that the first gate structure has a higher threshold voltage than the second gate structure. In the case that the operating voltage applied to the first gate remains unchanged, the threshold voltage of the first gate structure increases, the number of electrons capable of being actuated by the operating voltage decreases, and the number of electrons gathered in the channel region below the isolation structure decreases, so that it is more difficult to form the channel. In this way, it is difficult for electrons to transition from one active area to another through the channel region, thereby reducing signal interference between the active areas at both sides of the second isolation structure.

[0076] It will be appreciated by those of ordinary skill in the art that the above-described examples are specific examples for achieving the disclosure, and that various modifications may be made in form and detail in practical applications without departing from the spirit and scope of the disclosure. Any person skilled in the art may make respective changes and modifications without departing from the spirit and scope of the disclosure, and therefore the scope of protection of the disclosure should be limited by the scope defined by the claims.

Claims

1. A memory, comprising,

a substrate, wherein the substrate comprises an isolation structure and an active area between adjacent isolation structures;

a first gate structure, wherein the first gate structure locates in a first groove of the isolation structure, and comprises a first gate filled in the first groove, and the first gate comprises a first conductive layer filled at a bottom of the first groove and a second conductive layer located above the first conductive layer, and a work function of a material of the first conductive layer is greater than a work function of a material of the second conductive layer; and

a second gate structure, wherein the second gate structure locates in a second groove of the active area, and comprises a second gate filled in the second groove, and a material of the second gate is same as the material of the second conductive layer.

2. The memory of claim 1, wherein the first gate structure comprises a first gate dielectric layer covering a bottom surface and sidewalls of the first groove, and the second gate structure comprises a second gate dielectric layer covering a bottom surface and sidewalls of the second groove, and a material of the first gate dielectric layer is same as a material of the second gate dielectric layer.

3. The memory of claim 2, wherein a thickness of the first gate dielectric layer in a direction perpendicular to a surface of the substrate is greater than a thickness of the first gate dielectric layer in a direction parallel to the surface of the substrate.

4. The memory of claim 2, wherein the first gate structure further comprises a first blocking layer covering a surface of the first gate dielectric layer, and the first blocking layer is configured to block a migration of metal ions in the first gate towards the first gate dielectric layer.

5. The memory of claim 4, wherein the second gate structure further comprises a second blocking layer covering a surface of the second gate dielectric layer, and the second blocking layer is configured to block a migration of metal ions in the second gate towards the second gate dielectric layer.

6. The memory of claim 5, wherein a material of the first blocking layer is same as a material of the second blocking layer.

7. The memory of claim 1, wherein a depth of the first gate in the substrate is greater than a depth of the second gate in the substrate.

8. The memory of claim 7, wherein the first groove has a first depth in the substrate, the second groove has a second depth in the substrate, and a difference between the first depth and the second depth is 10%

to 50% of the first depth.

9. The memory of claim 1, wherein the isolation structure further comprises a third groove that has an opening width less than an opening width of the first groove in a direction parallel to a surface of the substrate, the third groove is filled with a third gate structure, and the third gate structure has a material same as a material of the second gate structure.

10. The memory of claim 1, wherein the isolation structure further comprises a third groove that has an opening width less than an opening width of the first groove in a direction parallel to a surface of the substrate, and the third groove is filled with a third gate structure, and the third gate structure has a material same as a material of the first gate structure.

11. The memory of claim 1 wherein in a direction perpendicular to a surface of the substrate, a top surface of the first conductive layer is lower than or flush with a bottom surface of the second gate.

12. The memory of claim 1, wherein in a direction perpendicular to a surface of the substrate, a thickness of the first conductive layer is in a range of 1 nm to 5 nm.

13. The memory of claim 1 or 12, wherein the material of the first conductive layer comprises at least one of titanium nitride, tungsten, nickel or cobalt.

14. The memory of claim 13, wherein the material of the first conductive layer comprises tungsten, crystal orientations of the tungsten in the first conductive layer comprise [100] and [110].

15. The memory of claim 14, wherein the material of the second conductive layer comprises tungsten, and a crystal orientation of the tungsten of the second conductive layer comprises [111], [113], or [116].

16. A method for manufacturing a memory, comprising,

providing a substrate, the substrate comprising an isolation structure and an active area between adjacent isolation structures;
performing an etching process to form a first groove in the isolation structure and a second groove in the active area;
performing a first deposition process to form a first conductive layer filled at bottom of the first groove; and
performing a second deposition process to form a second conductive layer filled above the first conductive layer and in the second groove, the first conductive layer having a work function greater than a work function of the second conductive layer, the first conductive layer filled in the first groove and the second conductive layer forming a first gate, and the second conductive layer filled in the second groove forming a second gate.

17. The method of claim 16, further comprising: before performing the first deposition process, forming a first gate dielectric layer covering a bottom surface and sidewalls of the first groove and a second gate dielectric layer covering a bottom surface and sidewalls of the second groove, and a material of the first gate dielectric layer is same as a material of the second gate dielectric layer.

18. The method of claim 17, further comprising: before performing the first deposition process, forming a first blocking layer covering a surface of the first gate dielectric layer, the first blocking layer being configured to block a migration of metal ions in the first gate towards the first gate dielectric layer.

19. The method of claim 18, wherein the first blocking layer and a second blocking layer covering a surface of the second gate dielectric layer are formed in same process, and the second blocking layer is configured to block a migration of metal ions in the second gate towards the second gate dielectric layer.

20. The method of claim 16, wherein in a direction perpendicular to a surface of the substrate, a depth of the first groove of the isolation structure is greater than a depth of the second groove of the active area.

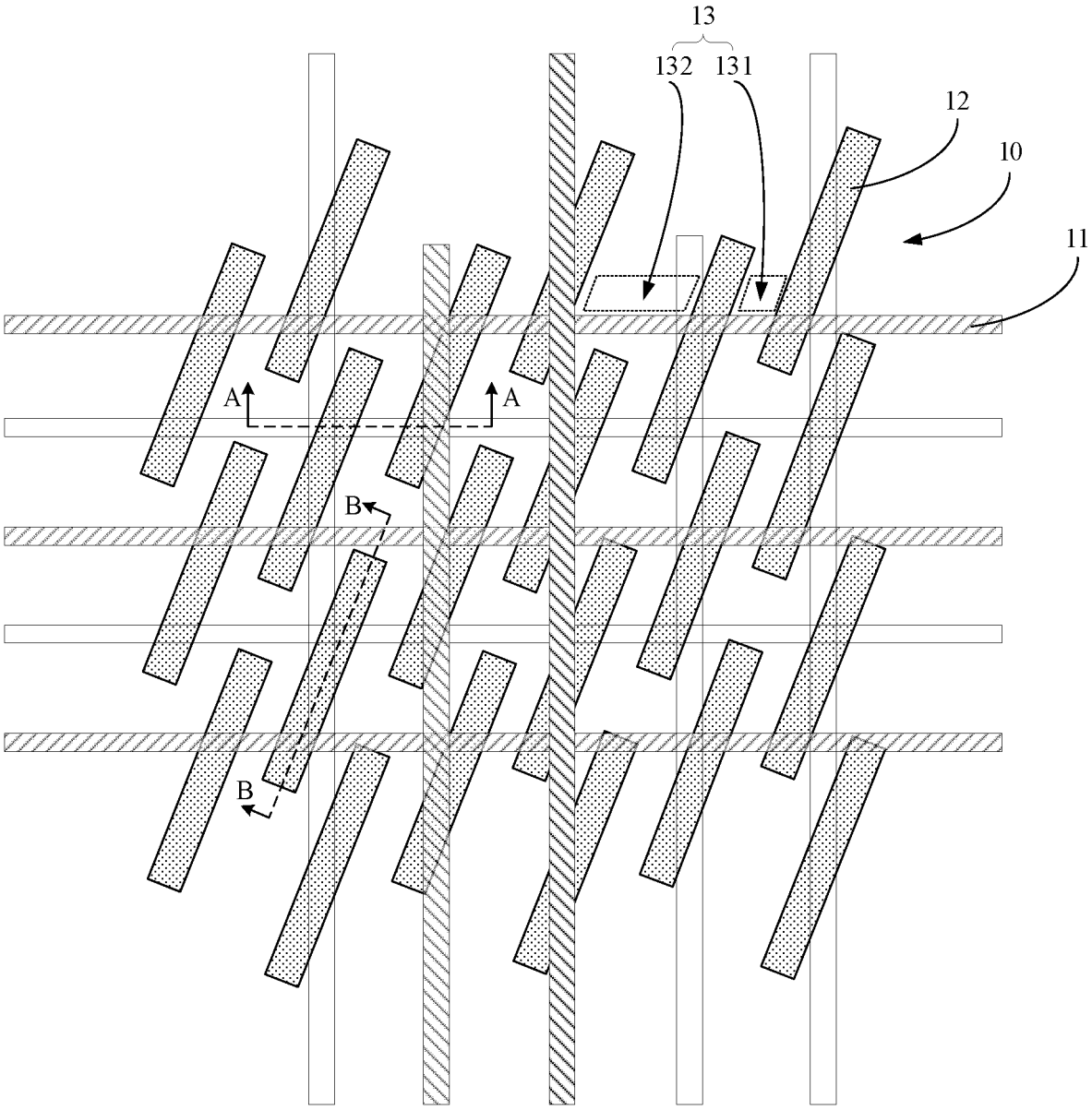

FIG. 1

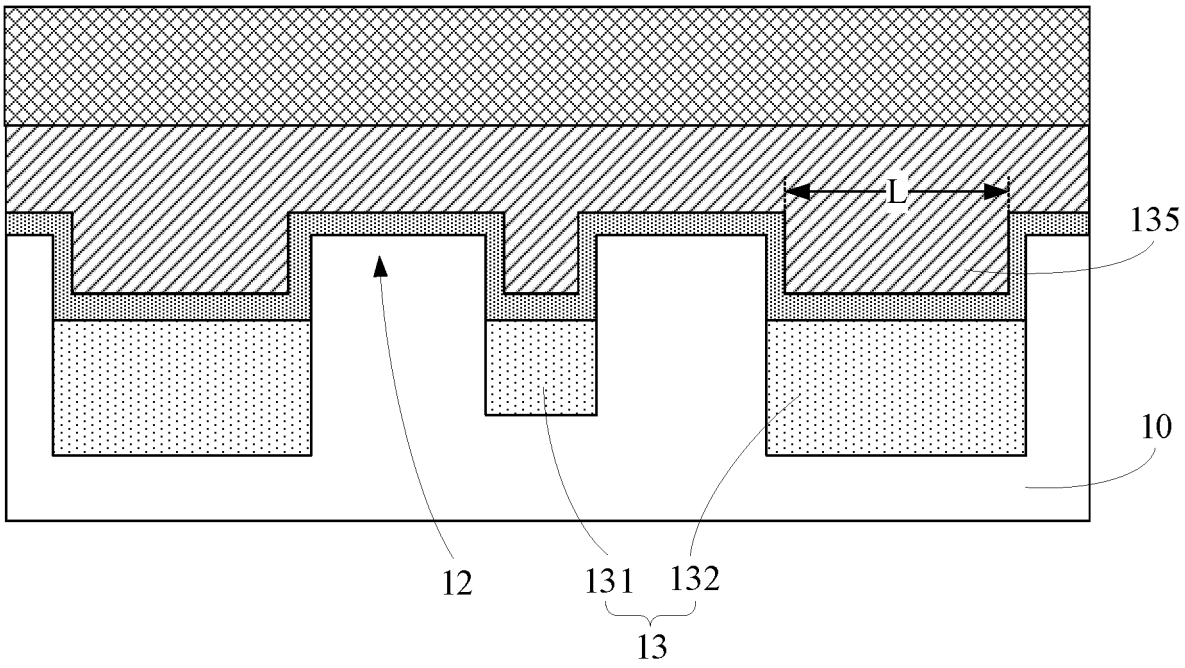

FIG. 2

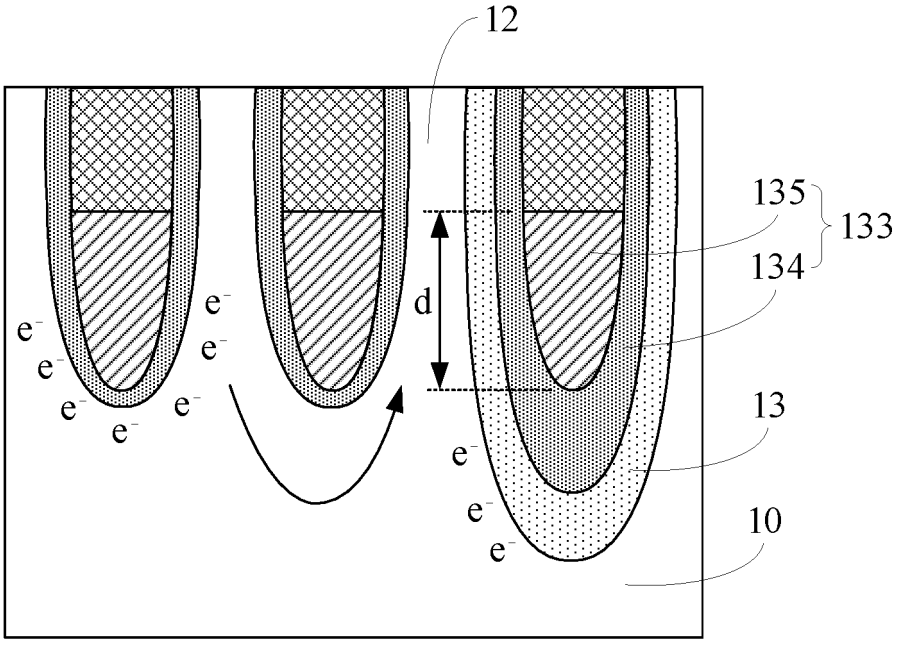

FIG. 3

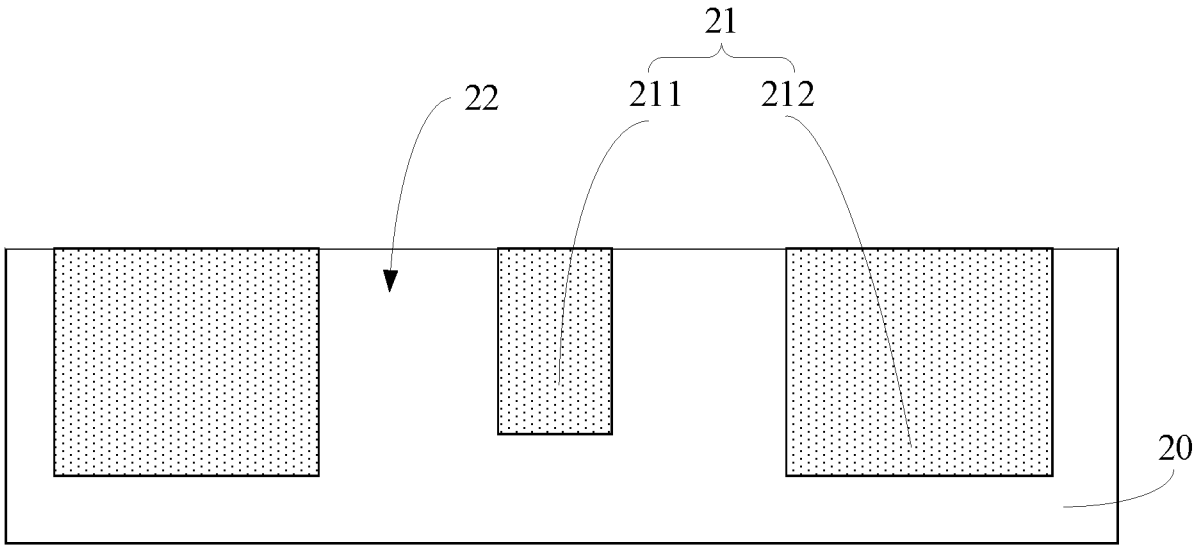

FIG. 4

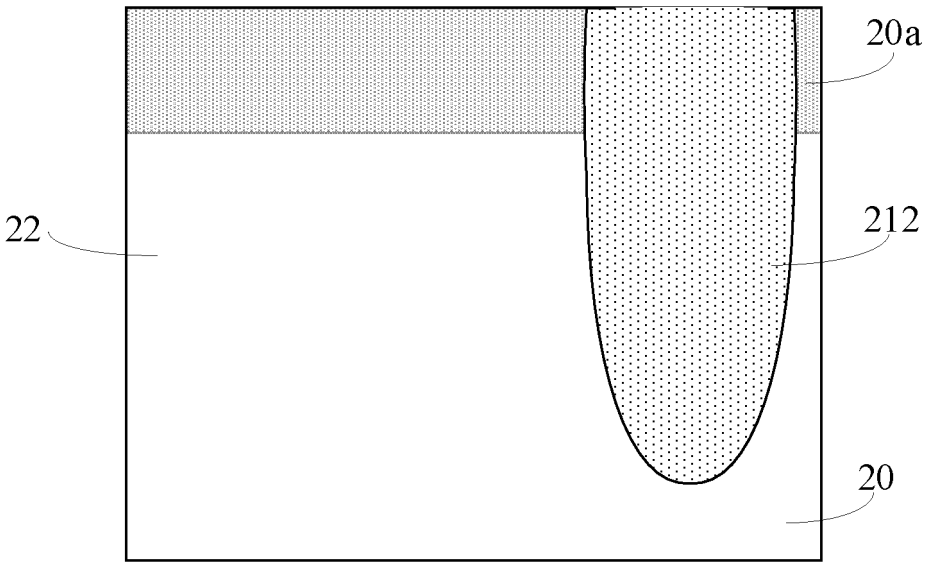

FIG. 5

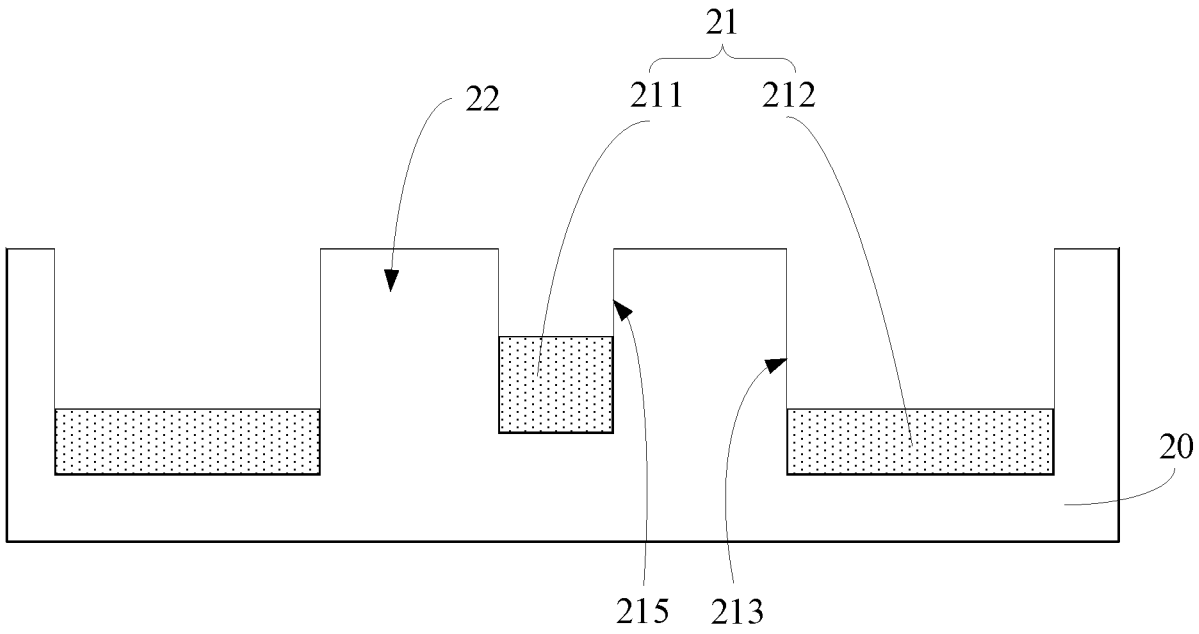

FIG. 6

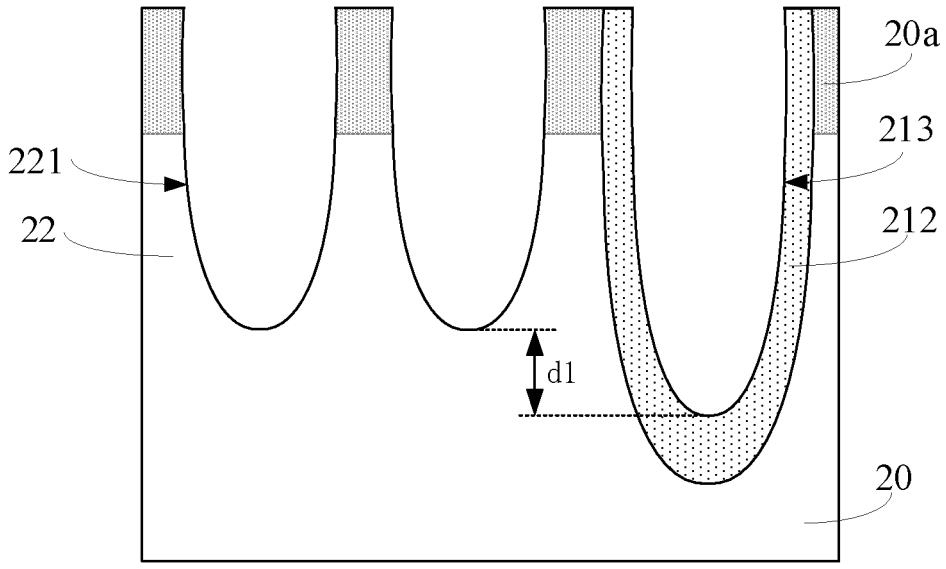

FIG. 7

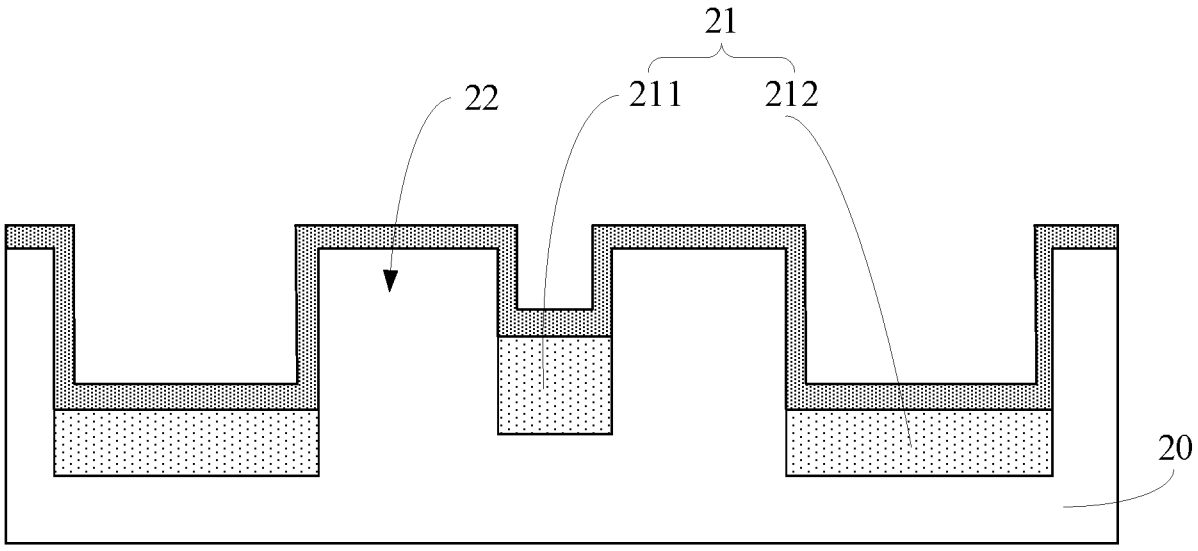

FIG. 8

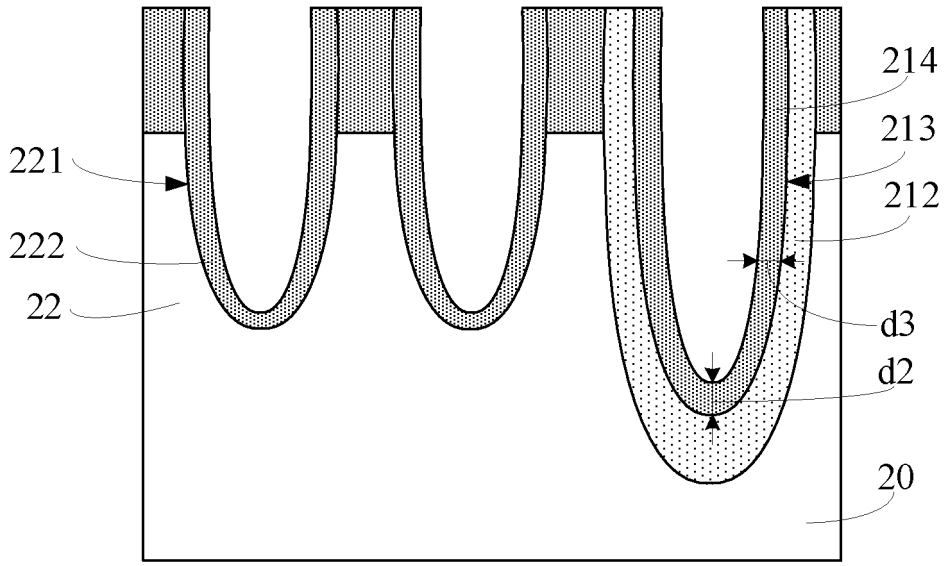

FIG. 9

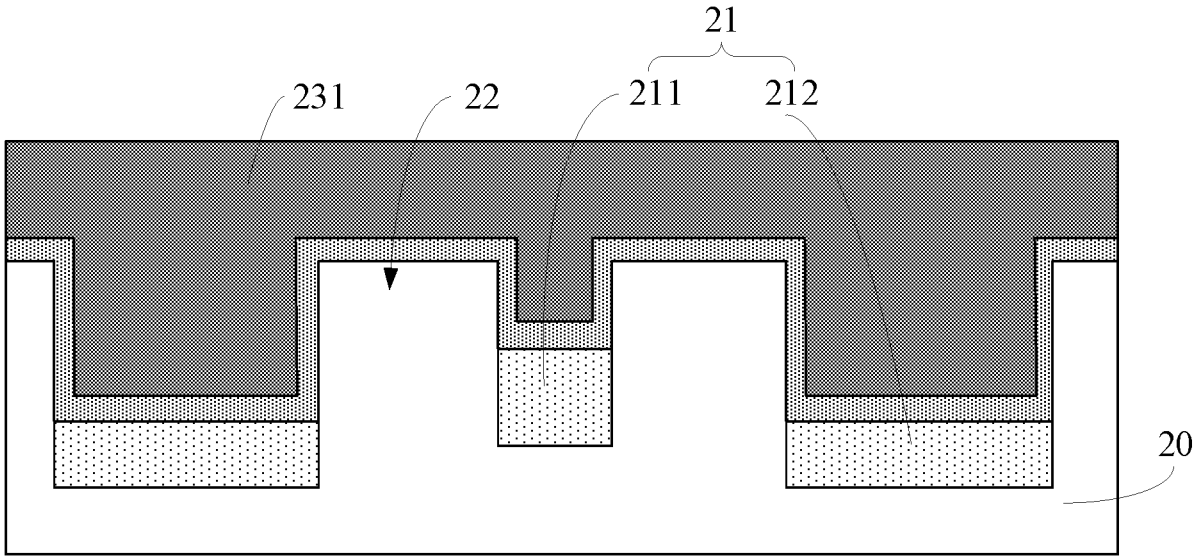

FIG. 10

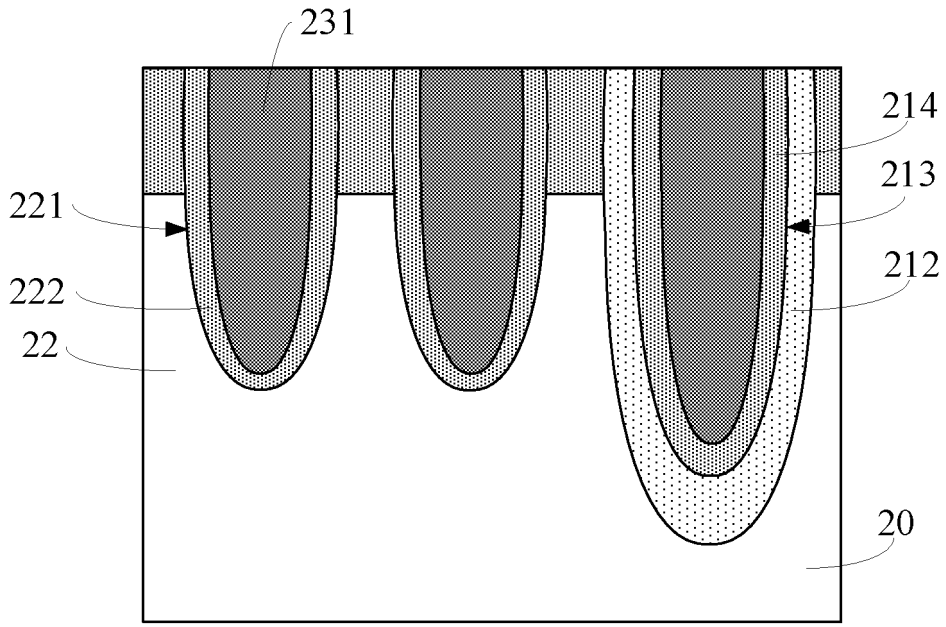

FIG. 11

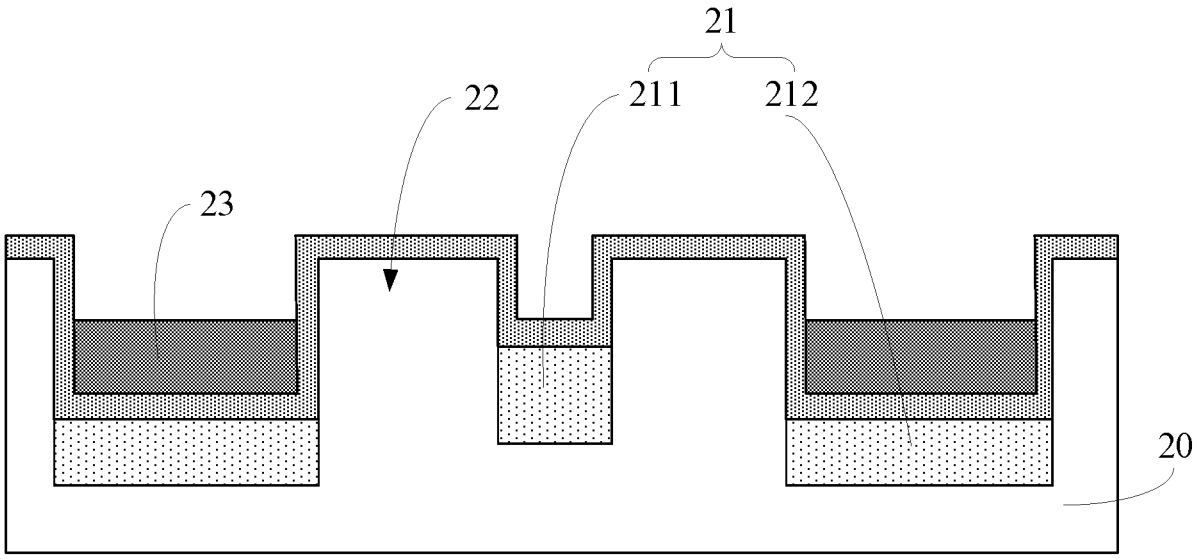

FIG. 12

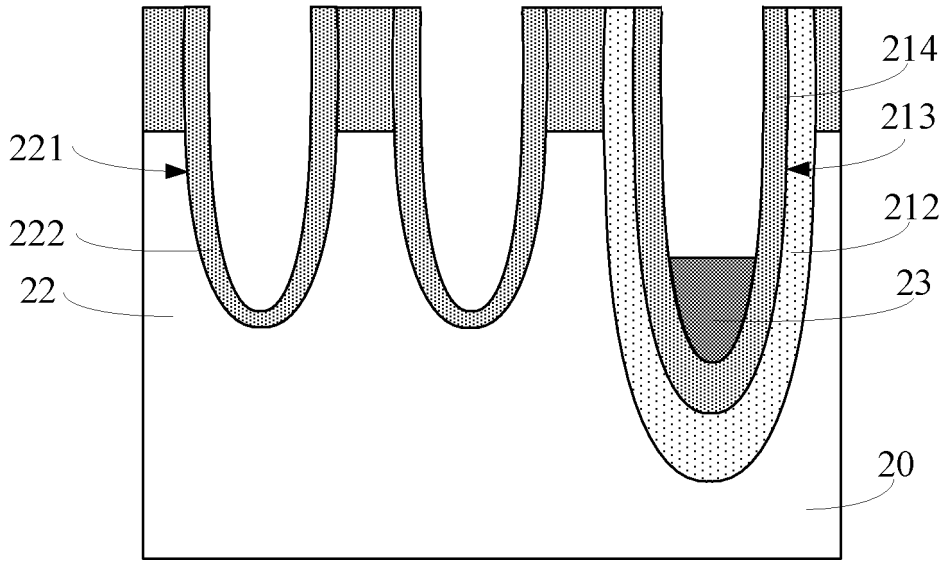

FIG. 13

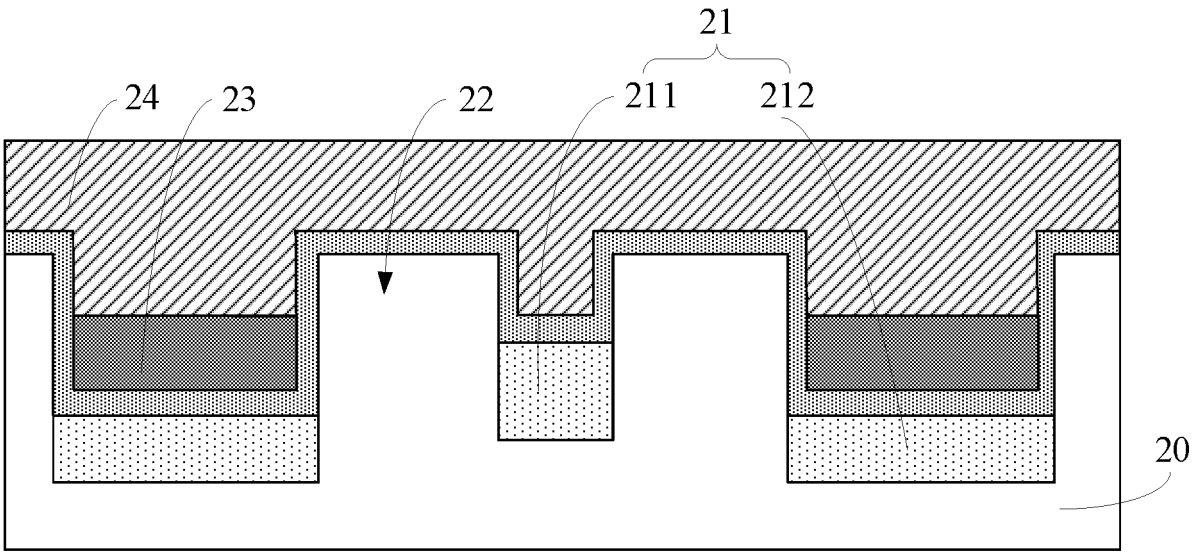

FIG. 14

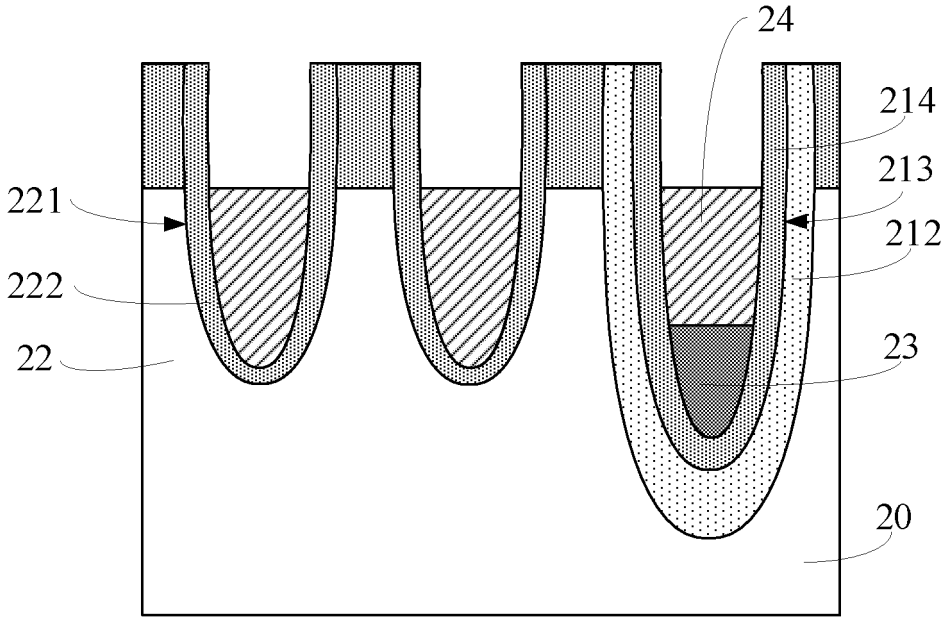

FIG. 15

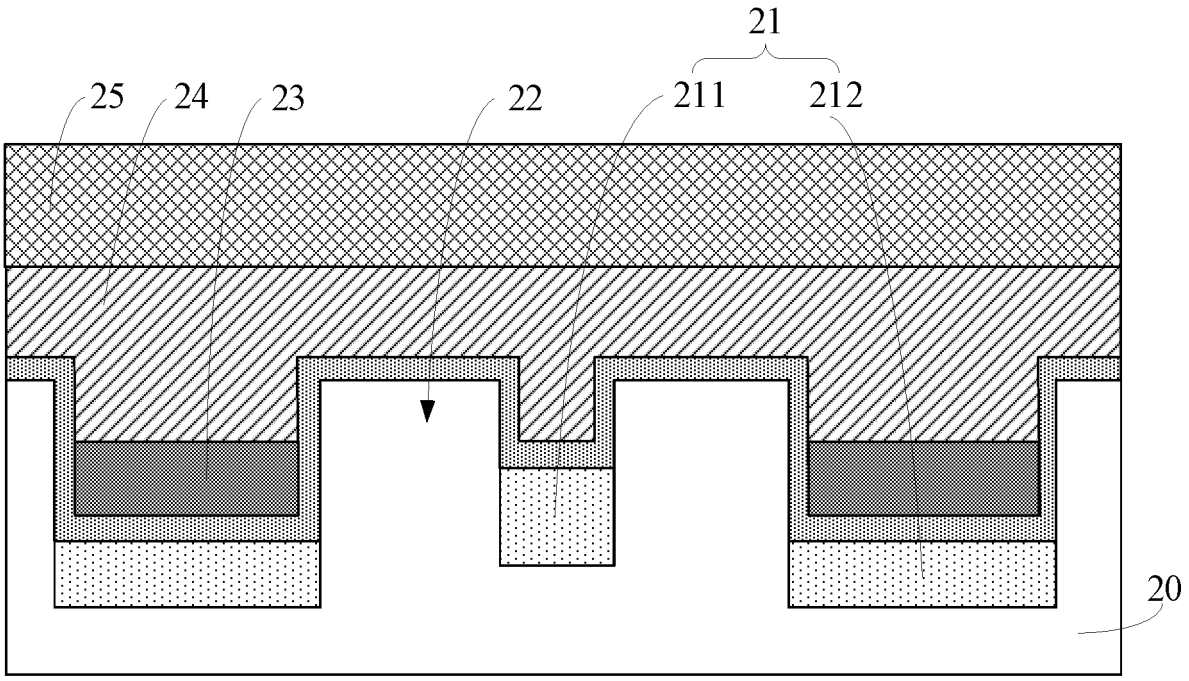

FIG. 16

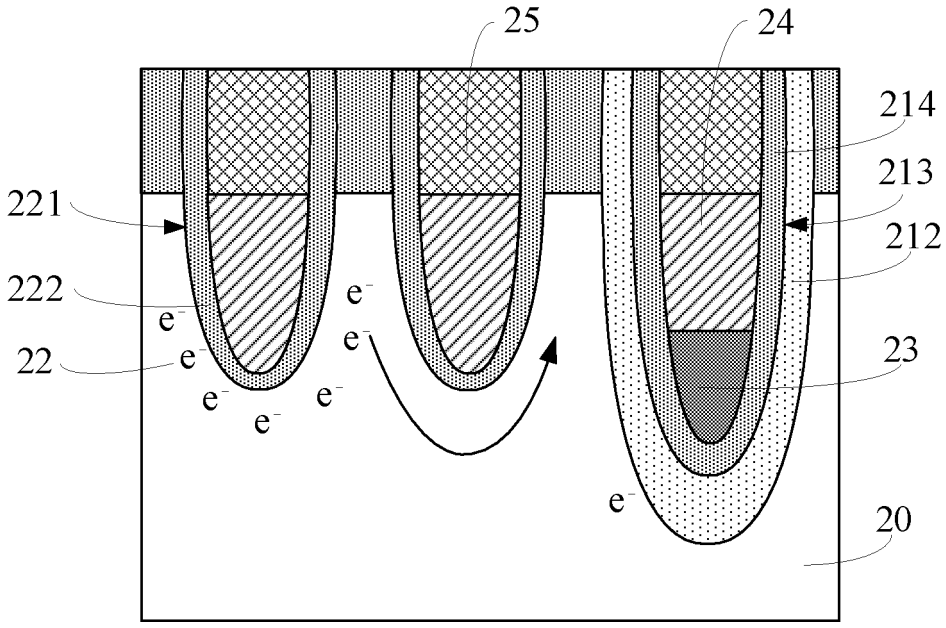

FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/138090

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/108(2006.01)i; H01L 29/423(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI: 存储器, NAND, 电极, 栅, 导电, 功函数, 沟, 槽, 有源, 隔离, 信号, 干扰, memory, electrode?, gate, conduct+, channel?, groove?, active, isolat+, signal, interfere, function

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 210156376 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 17 March 2020 (2020-03-17) description, paragraphs [0100]-[0124], and figures 11-12	1-20
A	CN 108364937 A (SAMSUNG ELECTRONICS CO., LTD.) 03 August 2018 (2018-08-03) entire document	1-20
A	CN 110896053 A (SEMICONDUCTOR MANUFACTURING ELECTRONICS (SHAOXING) CORPORATION) 20 March 2020 (2020-03-20) entire document	1-20
A	CN 210245492 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 03 April 2020 (2020-04-03) entire document	1-20
A	US 2016240665 A1 (SANDISK 3D L.L.C.) 18 August 2016 (2016-08-18) entire document	1-20
A	US 2019103489 A1 (SUPER GROUP SEMICONDUCTOR CO., LTD.) 04 April 2019 (2019-04-04) entire document	1-20

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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 April 2021	**10 May 2021**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2020/138090

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
CN 210156376 U	17 March 2020	None	
CN 108364937 A	03 August 2018	KR 20180088187 A	03 August 2018
		US 2018211952 A1	26 July 2018
		US 10381345 B2	13 August 2019
CN 110896053 A	20 March 2020	None	
CN 210245492 U	03 April 2020	None	
US 2016240665 A1	18 August 2016	US 9583615 B2	28 February 2017
		WO 2016133569 A1	25 August 2016
US 2019103489 A1	04 April 2019	TW 201916372 A	16 April 2019
		US 10529847 B2	07 January 2020
		TW I629795 B	11 July 2018

Form PCT/ISA/210 (patent family annex) (January 2015)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 202010802218 **[0001]**