



(12) **EUROPEAN PATENT APPLICATION**  
published in accordance with Art. 153(4) EPC

(43) Date of publication:  
**07.06.2023 Bulletin 2023/23**

(51) International Patent Classification (IPC):  
**H02M 7/49 (2007.01)**

(21) Application number: **20946645.7**

(52) Cooperative Patent Classification (CPC):  
**H02M 7/49**

(22) Date of filing: **28.07.2020**

(86) International application number:  
**PCT/JP2020/028887**

(87) International publication number:  
**WO 2022/024218 (03.02.2022 Gazette 2022/05)**

(84) Designated Contracting States:  
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR**  
Designated Extension States:  
**BA ME**  
Designated Validation States:  
**KH MA MD TN**

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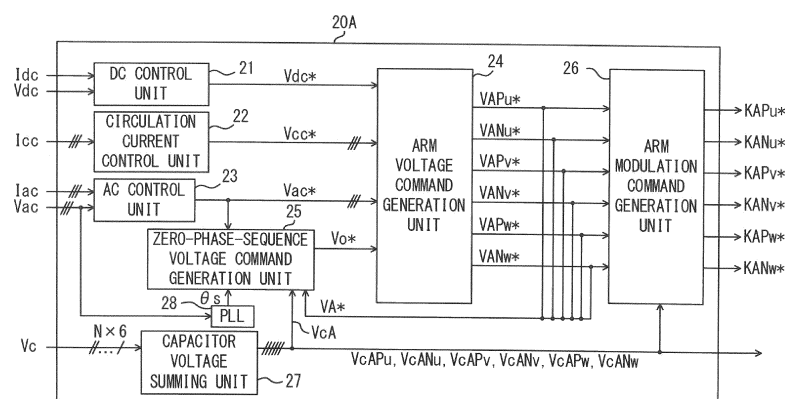
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(54) **POWER CONVERSION DEVICE**

(57) A power converter (10) includes two arms for each phase between DC terminals (5P, 5N), and each arm is formed by connecting a plurality of converter cells (11) in series. A control device (20) includes an arm voltage command generation unit (24) which generates, for each arm, an arm voltage command ( $V_A^*$ ) for the plurality of converter cells (11). The arm voltage command ( $V_A^*$ )

is generated by superimposing a zero-phase-sequence voltage command ( $V_o^*$ ) having a frequency component that is three times an AC fundamental frequency. Phase adjustment of the zero-phase-sequence voltage command ( $V_o^*$ ) is performed on the basis of voltage of a DC capacitor (13) in the converter cell (11) and the arm voltage command ( $V_A^*$ ).

FIG. 4



**Description**TECHNICAL FIELD

5 **[0001]** The present invention relates to a power conversion device.

BACKGROUND ART

10 **[0002]** In recent years, in power conversion devices used for high-voltage application such as a power grid, a multilevel converter in which a plurality of converter cells each including an energy storage element are connected in series in a multiplexed manner, has been put into practice. Such a converter is called a modular multilevel converter (MMC) type, a cascaded multilevel converter (CMC) type, or the like.

15 **[0003]** In a conventional power conversion device that converts three-phase AC power using a general inverter/converter as described in, for example, Patent Document 1, when imbalance of a power grid is detected, a sinusoidal base signal is generated for each phase, and a third-order harmonic is superimposed on each base signal, to generate a voltage command signal for each phase. Thus, the peak of the voltage command is reduced, whereby utilization of DC voltage can be improved.

20 **[0004]** Meanwhile, a conventional power conversion device described in Patent Document 2 is a power conversion device of the MMC type and outputs zero-phase-sequence voltage with a third-order harmonic of a fundamental wave superimposed thereon to an AC circuit as in the control described in Patent Document 1.

CITATION LISTPATENT DOCUMENT

25 **[0005]**

Patent Document 1: Japanese Laid-Open Patent Publication JP 2018- 14 860 A

Patent Document 2: WO 2017/046908 A1

SUMMARY OF THE INVENTIONPROBLEMS TO BE SOLVED BY THE INVENTION

35 **[0006]** In the above conventional power conversion device of the MMC type, a different capacitor is provided for each arm, and power pulsation of each arm flows in/out to/from each capacitor. Therefore, depending on the capacitances of the capacitors or the operation condition, voltage pulsation might occur in the capacitors of each arm, thus hampering improvement in utilization of DC voltage.

40 **[0007]** The present invention has been made to solve the above problem, and an object of the present invention is to provide a power conversion device of the MMC type that can assuredly improve utilization of DC voltage.

SOLUTION TO THE PROBLEMS

45 **[0008]** A power conversion device according to the present invention includes: a power converter for performing power conversion between a DC circuit and a three-phase AC circuit; and a control device for performing output control of the power converter. The power converter includes, for each phase of the three-phase AC circuit, two arms provided between common DC terminals and connected to each other, a connection portion therebetween being connected to the corresponding phase of the three-phase AC circuit, each of the arms being formed by connecting, in series, a plurality of converter cells each composed of a plurality of semiconductor switching elements and a DC capacitor.

50 **[0009]** The control device includes a voltage command generation unit which generates, for each of the arms of the power converter, an output voltage command for the plurality of converter cells, and the control device generates, for each of the arms, a base command for output voltage of the plurality of converter cells, performs phase adjustment of a zero-phase-sequence voltage command having a frequency component that is three times a fundamental frequency of the three-phase AC circuit on the basis of voltage of the DC capacitor and the output voltage command, and superimposes the phase-adjusted zero-phase-sequence voltage command on the base command, thus generating the output voltage command.

EFFECT OF THE INVENTION

**[0010]** The power conversion device according to the present invention makes it possible to provide a power conversion device of the MMC type that can assuredly improve utilization of DC voltage.

BRIEF DESCRIPTION OF THE DRAWINGS**[0011]**

FIG. 1 shows a schematic configuration of a power conversion device according to Embodiment 1.  
 FIG. 2 shows a configuration example of a converter cell according to Embodiment 1.  
 FIG. 3 shows a configuration example of a converter cell according to Embodiment 1.  
 FIG. 4 is a block diagram showing a main control unit of a control device according to Embodiment 1.  
 FIG. 5 is a block diagram showing an arm control unit of the control device according to Embodiment 1.  
 FIG. 6 is a block diagram showing a zero-phase-sequence voltage command generation unit according to Embodiment 1.  
 FIG. 7 is a waveform diagram showing the relationship between a capacitor voltage sum for an arm and an arm voltage command in a first comparative example.  
 FIG. 8 is a waveform diagram showing the relationship between a capacitor voltage sum for an arm and an arm voltage command in a second comparative example.  
 FIG. 9 is a waveform diagram at various parts, for illustrating operation of the power conversion device according to Embodiment 1.  
 FIG. 10 is a waveform diagram at various parts, for illustrating operation of the power conversion device according to Embodiment 1.  
 FIG. 11 is a waveform diagram at various parts, for illustrating operation of the power conversion device according to Embodiment 1.  
 FIG. 12 is a waveform diagram at various parts, for illustrating operation of the power conversion device according to Embodiment 1.  
 FIG. 13 is a waveform diagram showing an arm voltage command and a control margin according to Embodiment 1.  
 FIG. 14 is a waveform diagram showing detection sections and phase update of a zero-phase-sequence voltage command in a power conversion device according to Embodiment 3.  
 FIG. 15 is a waveform diagram showing an arm voltage command and a control margin for each arm in the power conversion device according to Embodiment 3.  
 FIG. 16 shows detection arms set for each detection section in the power conversion device according to Embodiment 3.  
 FIG. 17 is a flowchart illustrating operation of the power conversion device according to Embodiment 3.  
 FIG. 18 is a flowchart illustrating operation of the power conversion device according to Embodiment 3.  
 FIG. 19 is a waveform diagram showing phase update of a zero-phase-sequence voltage command in the power conversion device according to Embodiment 3.  
 FIG. 20 is a waveform diagram showing phase update of a zero-phase-sequence voltage command in a power conversion device according to Embodiment 4.  
 FIG. 21 is a flowchart illustrating operation of the power conversion device according to Embodiment 4.

DESCRIPTION OF EMBODIMENTSEmbodiment 1

**[0012]** FIG. 1 shows a schematic configuration of a power conversion device according to Embodiment 1.

**[0013]** As shown in FIG. 1, a power conversion device 1 includes a power converter 10 which is a main circuit and a control device 20 for performing output control of the power converter 10, and is connected between an AC grid 2 as a three-phase AC circuit and a DC circuit 4.

**[0014]** The power converter 10 includes a plurality of leg circuits 100u, 100v, 100w (referred to as leg circuit(s) 100 when mentioning them collectively or any of them) connected in parallel to each other, between a positive DC terminal 5P and a negative DC terminal 5N which are common DC terminals.

**[0015]** The leg circuit 100 is provided for each of a plurality of phases (in this case, three phases U, V, W) forming AC. The leg circuits 100 are connected between the AC grid 2 and the DC circuit 4 and perform power conversion between AC and DC. AC input terminals 6 respectively provided to the leg circuits 100u, 100v, 100w are connected to the AC grid 2 via a transformer 3.

**[0016]** The positive DC terminal 5P and the negative DC terminal 5N connected in common to the leg circuits 100 are connected to the DC circuit 4. The DC circuit 4 is, for example, a DC power grid including a DC power transmission network and the like, or another power conversion device. In the former case, a high-voltage DC power transmission (HVDC) system is formed. In the latter case, two power conversion devices are connected, thus forming a back-to-back (BTB) system for connecting two AC grids different in rated frequency or the like.

**[0017]** The leg circuit 100u includes a U-phase upper arm Pu from the positive DC terminal 5P to the AC input terminal 6, and a U-phase lower arm Nu from the negative DC terminal 5N to the AC input terminal 6. The leg circuit 100v includes a V-phase upper arm Pv from the positive DC terminal 5P to the AC input terminal 6, and a V-phase lower arm Nv from the negative DC terminal 5N to the AC input terminal 6. The leg circuit 100w includes a W-phase upper arm Pw from the positive DC terminal 5P to the AC input terminal 6, and a W-phase lower arm Nw from the negative DC terminal 5N to the AC input terminal 6.

**[0018]** That is, the upper arms Pu, Pv, Pw for the respective phases and the lower arms Nu, Nv, Nw for the respective phases are connected in series to each other, and the connection points therebetween serve as the AC input terminals 6 for the respective phases.

**[0019]** The leg circuits 100u, 100v, 100w have the same configuration. Therefore, hereinafter, the leg circuit 100u for U phase will be described as a representative.

**[0020]** The arm Pu is formed by connecting a plurality of (N) converter cells 11 and a reactor 12P in series. Similarly, the arm Nu is formed by connecting a plurality of (N) converter cells 11 and a reactor 12N in series.

**[0021]** The position where the reactor 12P is provided may be any position in the arm Pu, and the position where the reactor 12N is provided may be any position in the arm Nu.

**[0022]** As each of the reactors 12P, 12N, a plurality of reactors may be provided, and the inductance values of the reactors may be different from each other. Only one of the reactors 12P, 12N may be provided and another one may be omitted.

**[0023]** Although the case where the AC input terminals 6 are connected to the AC grid 2 via the transformer 3 is shown here, a configuration in which the AC input terminals 6 are connected to the AC grid 2 via an interconnection reactor instead of the transformer 3, may be adopted.

**[0024]** Instead of the AC input terminals 6 for the respective phases, primary windings may be provided to the leg circuits 100u, 100v, 100w and the leg circuits 100u, 100v, 100w may be electrically connected to the transformer 3 via secondary windings magnetically coupled with the primary windings. In this case, the reactors 12P, 12N may be used as the primary winding for each phase.

**[0025]** That is, the upper arms Pu, Pv, Pw for the respective phases and the lower arms Nu, Nv, Nw for the respective phases are connected to each other by connection portions such as the AC input terminals 6 or the primary windings, and are electrically connected to the AC grid 2 via the connection portions.

**[0026]** The power conversion device 1 further includes DC voltage detectors 7P, 7N, an arm current detector 8 provided to each of the arms Pu, Nu, Pv, Nv, Pw, Nw, an AC voltage detector 9A, and an AC current detector 9B, as detectors for measuring electric quantities (current, voltage, etc.) used for control. Signals from these detectors are inputted to the control device 20 via signal lines.

**[0027]** The signal lines are formed by optical fibers, for example. In FIG. 1, for simplification, some of the signal lines for signals to be inputted from the detectors to the control device 20 are collectively shown. Similarly, some of signal lines for signals to be inputted/outputted between the control device 20 and the converter cells 11 are collectively shown. The signal lines between the converter cells 11 and the control device 20 may be separately provided as the ones for transmission and the ones for reception.

**[0028]** Hereinafter, each detector will be specifically described.

**[0029]** The DC voltage detector 7P detects DC voltage VdcP of the positive DC terminal 5P. The DC voltage detector 7N detects DC voltage VdcN of the negative DC terminal 5N. A difference between the DC voltage VdcP and the DC voltage VdcN is defined as DC voltage Vdc.

**[0030]** The arm current detectors 8 provided to the arms Pu, Nu, Pv, Nv, Pw, Nw respectively detect arm currents IPu, INu, IPv, INv, IPw, INw flowing through the arms Pu, Nu, Pv, Nv, Pw, Nw. In the following description, the arm currents IPu, IPv, IPw are collectively referred to as upper arm currents IAP, the arm currents INu, INv, INw are collectively referred to as lower arm currents IAN, and the upper arm current IAP and the lower arm current IAN are collectively referred to as arm currents IA.

**[0031]** The AC voltage detector 9A detects AC voltage Vacu for U phase, AC voltage Vacv for V phase, and AC voltage Vacw for W phase of the AC grid 2. In the following description, Vacu, Vacv, and Vacw are collectively referred to as Vac.

**[0032]** The AC current detector 9B detects AC current Iacu for U phase, AC current Iacv for V phase, and AC current Iacw for W phase of the AC grid. In the following description, Iacu, Iacv, and Iacw are collectively referred to as Iac.

**[0033]** FIG. 2 and FIG. 3 show configuration examples of each converter cell 11 in the power converter 10.

**[0034]** The converter cell 11 shown in FIG. 2 has a circuit configuration called a half-bridge configuration.

**[0035]** This converter cell 11 includes a series unit formed by connecting, in series, two switching elements Q1, Q2

to which diodes D are connected in antiparallel, a DC capacitor 13, a voltage detector 14, and a bypass switch 15. The series unit of the switching elements Q1, Q2 and the DC capacitor 13 are connected in parallel.

[0036] In this case, both terminals of the switching element Q2 serve as input/output terminals 11A, 11B of the converter cell 11. Through switching operations of the switching elements Q1, Q2, voltage Vc across the DC capacitor 13 or zero voltage is outputted. For example, when the switching element Q1 is ON and the switching element Q2 is OFF, the voltage Vc across the DC capacitor 13 is outputted. When the switching element Q1 is OFF and the switching element Q2 is ON, zero voltage is outputted.

[0037] The voltage detector 14 detects the voltage Vc across the DC capacitor 13. The bypass switch 15 is connected between the input/output terminals 11A, 11B. For example, by turning on the bypass switch 15 when the AC grid 2 is abnormal, the converter cell 11 is short-circuited, whereby the switching elements Q1, Q2 in the converter cell 11 are protected from overcurrent.

[0038] The converter cell 11 shown in FIG. 3 has a circuit configuration called a full-bridge configuration. This converter cell 11 includes a first series unit formed by connecting, in series, two switching elements Q3, Q4 to which diodes D are connected in antiparallel, a second series unit similarly formed by connecting, in series, two switching elements Q5, Q6 to which diodes D are connected in antiparallel, a DC capacitor 13, a voltage detector 14, and a bypass switch 15. The first series unit of the switching elements Q3, Q4, the second series unit of the switching elements Q5, Q6, and the DC capacitor 13 are connected in parallel.

[0039] In this case, the middle point in the first series unit of the switching elements Q3, Q4 and the middle point in the second series unit of the switching elements Q5, Q6 serve as input/output terminals 11A, 11B of the converter cell 11. Through switching operations of the switching elements Q3 to Q6, positive/negative voltage Vc across the DC capacitor 13 or zero voltage is outputted.

[0040] Similarly to the converter cell 11 shown in FIG. 2, the voltage detector 14 detects the voltage Vc across the DC capacitor 13. The bypass switch 15 is connected between the input/output terminals 11A, 11B.

[0041] As the switching elements Q1 to Q6 in the converter cell 11 shown in FIG. 2 and FIG. 3, for example, self-turn-off semiconductor switching elements such as an insulated gate bipolar transistor (IGBT), a gate commutated turn-off (GCT), or a thyristor are used. As the DC capacitor 13, a film capacitor is mainly used.

[0042] In the following description, the converter cell 11 having the half-bridge configuration shown in FIG. 2 is used.

[0043] The converter cell 11 may have a configuration other than the above-described ones, and for example, a circuit configuration called a clamped double cell may be used. Also, the switching elements Q1 to Q6 and the DC capacitor 13 are not limited to the above-described ones.

[0044] Next, the configuration of the control device 20 will be described.

[0045] As described above, the control device 20 receives the DC voltages VdcP, VdcN, the arm currents IA of the arms Pu, Nu, Pv, Nv, Pw, Nw, the AC voltage Vac for each phase, the AC current Iac for each phase, and the capacitor voltage Vc of each converter cell 11, which are detected values. Then, on the basis of the above received information, the control device 20 generates and outputs gate signals gs1, gs2 for driving the switching elements Q1, Q2 of each converter cell 11.

[0046] In the control device 20, from the above received information, the DC voltage Vdc and DC current Idc are calculated, and further, circulation currents Iccu, Iccv, Iccw for the respective phases are calculated. In the following description, Iccu, Iccv, and Iccw are collectively referred to as Icc.

[0047] The circulation current Icc for each phase is current circulating in the power converter 10 without flowing to the AC side and the DC side, and is represented as follows.

$$I_{cc} = (I_{AP} + I_{AN})/2 - I_{dc}/3$$

[0048] FIG. 4 is a block diagram showing a main control unit 20A of the control device 20, and FIG. 5 is a block diagram showing an arm control unit 20B of the control device 20.

[0049] The control device 20 includes the main control unit 20A, and the arm control units 20B provided for the respective arms Pu, Nu, Pv, Nv, Pw, Nw. In FIG. 5, the arm control unit 20B for the arm Nu is shown.

[0050] As shown in FIG. 4, the main control unit 20A includes a DC control unit 21, a circulation current control unit 22, an AC control unit 23, an arm voltage command generation unit 24, a zero-phase-sequence voltage command generation unit 25, and an arm modulation command generation unit 26. Further, the main control unit 20A includes a capacitor voltage summing unit 27 and a phase locked loop (PLL) unit 28.

[0051] The DC control unit 21 receives the DC voltage Vdc and the DC current Idc, and on the basis of these, generates a DC voltage command Vdc\*. The generated DC voltage command Vdc\* is inputted to the arm voltage command generation unit 24.

[0052] The circulation current control unit 22 receives the circulation currents Icc for the respective phases, and on the basis of the circulation currents Icc, generates circulation voltage commands Vccu\*, Vccv\*, Vccw\* for the respective

phases. In the following description,  $V_{ccu}^*$ ,  $V_{ccv}^*$ , and  $V_{ccw}^*$  are collectively referred to as  $V_{cc}^*$ . The generated circulation voltage commands  $V_{cc}^*$  for the respective phases are inputted to the arm voltage command generation unit 24.

**[0053]** The AC control unit 23 receives the AC voltages  $V_{ac}$  for the respective phases and the AC currents  $I_{ac}$  for the respective phases, and on the basis of these, generates AC voltage commands  $V_{acu}^*$ ,  $V_{acv}^*$ ,  $V_{acw}^*$  for the respective phases. In the following description,  $V_{acu}^*$ ,  $V_{acv}^*$ , and  $V_{acw}^*$  are collectively referred to as  $V_{ac}^*$ . The generated AC voltage commands  $V_{ac}^*$  for the respective phases are inputted to the arm voltage command generation unit 24.

**[0054]** The arm voltage command generation unit 24 receives the DC voltage command  $V_{dc}^*$ , the AC voltage commands  $V_{ac}^*$  for the respective phases, and the circulation voltage commands  $V_{cc}^*$  for the respective phases, and further receives a zero-phase-sequence voltage command  $V_o^*$  generated by the zero-phase-sequence voltage command generation unit 25. Then, the arm voltage command generation unit 24 generates arm voltage commands  $V_{APu}^*$ ,  $V_{ANu}^*$ ,  $V_{APv}^*$ ,  $V_{ANv}^*$ ,  $V_{APw}^*$ ,  $V_{ANw}^*$  (referred to as arm voltage commands  $V_A^*$  when mentioning them collectively) as output voltage commands for the respective arms Pu, Nu, Pv, Nv, Pw, Nw.

**[0055]** First, a base command based on the DC voltage command  $V_{dc}^*$ , the AC voltage command  $V_{ac}^*$  for each phase, and the circulation voltage command  $V_{cc}^*$  for each phase is generated, and the zero-phase-sequence voltage command  $V_o^*$  is superimposed on the base command, whereby the arm voltage command  $V_A^*$  is generated.

**[0056]** For example, the arm voltage commands  $V_{APu}^*$ ,  $V_{ANu}^*$  for U phase are represented by the following Expressions (1) and (2). The same applies to V phase and W phase.

$$V_{APu}^* = V_{dc}^* - V_{acu}^* + V_{ccu}^* - V_o^* \quad \dots (1)$$

$$V_{ANu}^* = V_{dc}^* + V_{acu}^* + V_{ccu}^* + V_o^* \quad \dots (2)$$

**[0057]** The capacitor voltage summing unit 27 obtains the capacitor voltages  $V_c$  of the respective converter cells 11 and calculates capacitor voltage sums  $V_{cAPu}$ ,  $V_{cANu}$ ,  $V_{cAPv}$ ,  $V_{cANv}$ ,  $V_{cAPw}$ ,  $V_{cANw}$  (referred to as capacitor voltage sums  $V_{cA}$  when mentioning them collectively) for the respective arms Pu, Nu, Pv, Nv, Pw, Nw. The arm control unit 20B for each arm Pu, Nu, Pv, Nv, Pw, Nw collects N capacitor voltages  $V_c$  of the converter cells 11.

**[0058]** The PLL unit 28 extracts a phase  $\theta_s$  from the AC voltage  $V_{ac}$  for each phase. For example, the AC voltage  $V_{acu}$  for U phase is represented as  $V_{acu} = V_p \sin \theta_s$ , using an amplitude  $V_p$ .

**[0059]** The zero-phase-sequence voltage command generation unit 25 receives the AC voltage commands  $V_{ac}^*$  for the respective phases, the respective arm voltage commands  $V_A^*$ , the capacitor voltage sums  $V_{cA}$  for the respective arms, and the phase  $\theta_s$ , and generates the zero-phase-sequence voltage command  $V_o^*$ . The details of the zero-phase-sequence voltage command generation unit 25 will be described later.

**[0060]** The arm modulation command generation unit 26 receives the respective arm voltage commands  $V_A^*$  and the capacitor voltage sums  $V_{cA}$  for the respective arms Pu, Nu, Pv, Nv, Pw, Nw, and generates arm modulation commands  $K_{APu}^*$ ,  $K_{ANu}^*$ ,  $K_{APv}^*$ ,  $K_{ANv}^*$ ,  $K_{APw}^*$ ,  $K_{ANw}^*$  (referred to as arm modulation commands  $K_A^*$  when mentioning them collectively) for the respective arms Pu, Nu, Pv, Nv, Pw, Nw.

**[0061]** As described above, the control device 20 includes similar arm control units 20B for the respective arms Pu, Nu, Pv, Nv, Pw, Nw. Hereinafter, the arm control unit 20B for the arm Nu will be described.

**[0062]** As shown in FIG. 5, the arm control unit 20B includes, for each converter cell 11 in the arm Nu, a cell control unit 29 for controlling the converter cell 11 individually. The arm control unit 20B receives the arm modulation command  $K_{ANu}^*$  from the arm modulation command generation unit 26, the capacitor voltage sum  $V_{cANu}$  from the capacitor voltage summing unit 27, and the detected arm current  $I_{Nu}$ , as information about the arm Nu. The above received information is also inputted to each of the cell control units 29 for controlling the respective converter cells 11.

**[0063]** Each cell control unit 29 operates as follows.

**[0064]** In the converter cell 11 that is a control target of the cell control unit 29, the capacitor voltage  $V_c$  is detected by the voltage detector 14, and the capacitor voltage  $V_c$  is inputted to the cell control unit 29. In addition, the detected capacitor voltage  $V_c$  is also outputted from the cell control unit 29 to the capacitor voltage summing unit 27 of the main control unit 20A.

**[0065]** The cell control unit 29 controls the converter cell 11 so that the capacitor voltage  $V_c$  of the converter cell 11 that is the control target approaches an average value ( $V_{cANu}/N$ ) of the capacitor voltages in the arm Nu.

**[0066]** More specifically, the cell control unit 29 calculates a control quantity from the arm current  $I_{Nu}$  and a deviation between the average value ( $V_{cANu}/N$ ) of the capacitor voltages and the corresponding capacitor voltage  $V_c$ , and superimposes the control quantity on the arm modulation command  $K_{ANu}^*$ , to correct the arm modulation command  $K_{ANu}^*$ . Then, on the basis of the corrected arm modulation command  $K_{ANu}^*$ , the cell control unit 29 generates and outputs gate signals  $gs1$ ,  $gs2$  for driving the switching elements Q1, Q2 of the corresponding converter cell 11.

**[0067]** In the above description of the control device 20, for simplification, the case where control for balancing the

capacitor voltage sums  $V_{cA}$  for the respective arms Pu, Nu, Pv, Nv, Pw, Nw is omitted has been shown. However, control for balancing the DC voltages between phases or between arms may be added.

[0068] FIG. 6 is a block diagram showing the zero-phase-sequence voltage command generation unit 25.

[0069] As shown in FIG. 6, the zero-phase-sequence voltage command generation unit 25 receives the AC voltage commands  $V_{ac}^*$  for the respective phases, the respective arm voltage commands  $V_A^*$ , the capacitor voltage sums  $V_{cA}$  for the respective arms, and the phase  $\theta_s$ , and generates the zero-phase-sequence voltage command  $V_o^*$ .

[0070] In this case, the zero-phase-sequence voltage command  $V_o^*$  having a frequency component that is three times the fundamental frequency of AC voltage is generated with the phase thereof adjusted. Then, as described above, the zero-phase-sequence voltage command  $V_o^*$  is superimposed on the base command, whereby the arm voltage command  $V_A^*$  is generated.

[0071] The zero-phase-sequence voltage command  $V_o^*$  has a common value among U phase, V phase, and W phase, and theoretically, does not influence outputted AC voltage between phases. In addition, since the zero-phase-sequence voltage command  $V_o^*$  has a frequency component that is three times the fundamental frequency of the AC voltage, when the AC voltage  $V_{ac}$  is balanced and the numbers of normal converter cells 11 (the numbers of operating converter cells 11) included in the respective arms Pu, Nu, Pv, Nv, Pw, Nw are equal, instantaneous power for each phase is balanced.

[0072] The AC voltage command  $V_{ac}^*$  inputted to the zero-phase-sequence voltage command generation unit 25 is inputted to a zero-phase-sequence voltage generation unit 30 and a reference phase generation unit 31 in the zero-phase-sequence voltage command generation unit 25.

[0073] The reference phase generation unit 31 detects phase shift  $\theta_v$  of AC voltage due to voltage drop by the transformer 3 and the reactor 12P (or 12N) (hereinafter, may be simply referred to as phase  $\theta_v$ ), and the phase shift  $\theta_v$  is inputted to a phase adjustment unit 32. On the basis of the phase  $\theta_v$  outputted from the reference phase generation unit 31, the reference phase of the AC voltage command  $V_{ac}^*$  becomes  $(\theta_s + \theta_v)$ .

[0074] The phase adjustment unit 32 further receives the respective arm voltage commands  $V_A^*$ , the capacitor voltage sums  $V_{cA}$  for the respective arms, and the phase  $\theta_s$ , and determines an adjustment phase  $\theta_o$  for adjusting the phase of the zero-phase-sequence voltage command  $V_o^*$  (hereinafter, may be simply referred to as phase  $\theta_o$ ).

[0075] The zero-phase-sequence voltage generation unit 30 generates the zero-phase-sequence voltage command  $V_o^*$  on the basis of the AC voltage command  $V_{ac}^*$  and the phases  $\theta_s$ ,  $\theta_v$ ,  $\theta_o$ .

[0076] When the circulation current  $I_{cc}$  is 0, the arm voltage command  $V_{ANu}^*$  for the U-phase lower arm Nu is represented by the following Expression (3), on the basis of the above Expression (2).

$$V_{ANu}^* = V_{dc}^* + V_{acu}^* + V_o^* \quad \dots (3)$$

[0077] Here,  $V_{dc}^*$  and  $V_{acu}^*$  are represented as  $V_{dc}^* = V_{dc}/2$  and  $V_{acu}^* = V_p \cdot \sin(\theta_s + \theta_v)$ , and the zero-phase-sequence voltage command  $V_o^*$  is represented by the following Expression (4), using a constant  $a$ .

$$V_o^* = a \cdot V_p \cdot \sin 3(\theta_s + \theta_v + \theta_o) \quad \dots (4)$$

[0078] Then, the above Expression (3) can be deformed into the following Expression (5).

$$V_{ANu}^* = (V_{dc}/2) + V_p \cdot \sin(\theta_s + \theta_v) + a \cdot V_p \cdot \sin 3(\theta_s + \theta_v + \theta_o) \quad \dots (5)$$

[0079] In a general 2-level three-phase power conversion device not having a MMC configuration, a common DC capacitor is connected for three phases collectively. Therefore, power pulsations occurring in the respective phases are canceled out and the voltage of the DC capacitor is constant while hardly pulsating. In such a case, phase adjustment for the zero-phase-sequence voltage command to be superimposed is not needed, that is, with the adjustment phase  $\theta_o = 0$ , the peak of the AC output voltage can be reduced. Here, power flows in/out to/from the DC capacitor due to switching, but is negligible because the switching frequency is a high frequency.

[0080] Also in a power conversion device having a MMC configuration, the same applies if voltage of the DC capacitor is almost constant without pulsating. This will be shown as a first comparative example below.

[0081] FIG. 7 is a waveform diagram showing the relationship between a capacitor voltage sum for an arm and an arm voltage command in the first comparative example. The first comparative example is an example in which voltage of the DC capacitor is almost constant without pulsating under the same configuration as that of the power conversion device 1 according to Embodiment 1.

[0082] As shown in FIG. 7, a capacitor voltage sum  $V_{cA\alpha}$  for an arm is constant. For controlling the output voltage of

the arm, a zero-phase-sequence voltage command is superimposed on a base command  $VA_{\alpha}^*$ , whereby an arm voltage command  $VA_{\beta}^*$  is generated. In this case, phase adjustment for the zero-phase-sequence voltage command is not needed, and the zero-phase-sequence voltage command  $Vo^*$  and the arm voltage command  $VANu^*$  ( $VA_{\beta}^*$ ) obtained when  $\theta_0$  is 0 in the above Expressions (4) and (5) are used.

**[0083]** In the first comparative example, it is found that the peak of the arm voltage command  $VA_{\beta}^*$  on which the zero-phase-sequence voltage command with no phase adjustment has been superimposed is reduced. In this case, by setting the constant  $a$  to  $1/6$ , a necessary output voltage range can be reduced by about 13%.

**[0084]** The power conversion device 1 having the MMC configuration according to Embodiment 1 is used in a HVDC system or a BTB system, and in actuality, power pulsation occurring in each arm directly flows in/out to/from the DC capacitor 13 of each converter cell 11. For example, the arm current  $INu$  of the arm  $Nu$  which is the U-phase lower arm is represented by the following Expression (6). Here,  $I_p$  is an amplitude and  $\varphi$  is a power factor.

$$INu = -Idc/3 + I_p \cdot \sin(\theta_s + \varphi) \quad \dots (6)$$

**[0085]** Instantaneous power  $pNu$  flowing in/out to/from the arm  $Nu$  is calculated as a product of the arm voltage command  $VANu^*$  shown by the above Expression (5) and the arm current  $INu$  shown by the above Expression (6), and is represented by the following Expression (7). Here, the influence on the instantaneous power  $pNu$  due to superimposition of the zero-phase-sequence voltage command  $Vo^*$  in Expression (5) is small and therefore is regarded as 0, for simplification.

$$pNu = (Vdc \cdot I_p/2) \cdot \sin(\theta_s + \varphi) - (V_p \cdot Idc/3) \cdot \sin(\theta_s + \theta_v) - (V_p \cdot I_p/2) \cdot \cos(2\theta_s + \theta_v + \varphi) \quad \dots (7)$$

**[0086]** From the above Expression (7), it is found that power pulsation having a frequency that is equal to or two times the fundamental frequency of the AC grid 2 flows in/out to/from the arm  $Nu$ . Power pulsation  $\Delta WNu$  at  $t = 0$  in the DC capacitor 13 in the arm  $Nu$  is represented by the following Expression (8). Here,  $\theta_s = \omega t$  is satisfied.

$$\Delta WNu = -(Vdc \cdot I_p/2\omega) \cdot \cos(\theta_s + \varphi) + (V_p \cdot Idc/3\omega) \cdot \cos(\theta_s + \theta_v) - (V_p \cdot I_p/4\omega) \cdot \sin(2\theta_s + \theta_v + \varphi) \quad \dots (8)$$

**[0087]** With the power pulsation  $\Delta WNu$ , the capacitor voltage sum  $VcANu$  for the arm  $Nu$  pulsates, and voltage that can be outputted by the arm  $Nu$  also varies with time. The pulsation of the capacitor voltage sum  $VcA$  increases as the capacitance of the DC capacitor 13 becomes smaller.

**[0088]** A case where, while the capacitor voltage sum  $VcA$  varies with time, the arm voltage command  $VA_{\beta}^*$  on which the zero-phase-sequence voltage command with no phase adjustment has been superimposed is used as in the first comparative example, will be shown as a second comparative example below.

**[0089]** FIG. 8 is a waveform diagram showing the relationship between a capacitor voltage sum for an arm and an arm voltage command in the second comparative example. The second comparative example is an example in which, under the same configuration as that of the power conversion device 1 according to Embodiment 1, voltage of the DC capacitor 13 pulsates and the same zero-phase-sequence voltage command as used in the above first comparative example, i.e., the zero-phase-sequence voltage command with no phase adjustment is used. The base command  $VA_{\alpha}^*$  and the arm voltage command  $VA_{\beta}^*$  are the same as in the first comparative example shown in FIG. 7, while the capacitor voltage sum  $VcA$  for the arm is pulsating.

**[0090]** In the second comparative example, the arm voltage command  $VA_{\beta}^*$  does not fall within an output voltage range between the value of the capacitor voltage sum  $VcA$  and 0, and as a result, there is a region where voltage cannot be outputted.

**[0091]** In addition, each converter cell 11 is individually controlled and the output voltage thereof might increase/decrease more or less. Further, pulsation due to switching is superimposed on the capacitor voltage  $Vc$  of each converter cell 11, so that the range of voltage that can be outputted might change more or less.

**[0092]** From the above, it is desirable that the arm voltage command falls within the output voltage range with a margin provided.

**[0093]** In the present embodiment, by performing phase adjustment of the zero-phase-sequence voltage command  $Vo^*$ , the arm voltage command  $VA^*$  is caused to fall within the output voltage range between the value of the capacitor voltage sum  $VcA$  and 0 with a margin provided. In this case, the control device 20 changes the adjustment phase  $\theta_0$  for the zero-phase-sequence voltage command  $Vo^*$  so that a margin of the arm voltage command  $VA^*$  with respect to the

output voltage range increases.

**[0094]** Phase adjustment of the zero-phase-sequence voltage command  $V_o^*$  will be described in detail below.

**[0095]** As the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range (0 to  $V_{cA}$ ) of the arm, there are an upper margin  $\sigma_U$  to an upper limit value  $V_{cA}$  and a lower margin  $\sigma_L$  to a lower limit value 0. The upper margin  $\sigma_U$  is a control margin in the present invention. Both margins are instantaneous values. The upper margin  $\sigma_U$  is a value obtained by subtracting the arm voltage command  $V_A^*$  from the capacitor voltage sum  $V_{cA}$  and the lower margin  $\sigma_L$  is equal to the arm voltage command  $V_A^*$ .

**[0096]** In order to increase the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range (0 to  $V_{cA}$ ) of the arm, both of a minimum value  $\sigma_{Umin}$  of the upper margin  $\sigma_U$  and a minimum value  $\sigma_{Lmin}$  of the lower margin  $\sigma_L$  need to be made as great as possible in one cycle of the AC voltage. Therefore, the adjustment phase  $\theta_o$  for the zero-phase-sequence voltage command  $V_o^*$  is changed so that the smaller one of the two minimum values  $\sigma_{Umin}$ ,  $\sigma_{Lmin}$  in one cycle of the AC voltage increases.

**[0097]** FIG. 9 is a waveform diagram at various parts, for illustrating operation of the power conversion device. In FIG. 9, the capacitor voltage sum  $V_{cA}$ , the arm voltage command  $V_A^*$ , the upper margin  $\sigma_U$ , the lower margin  $\sigma_L$ , and the zero-phase-sequence voltage command  $V_o^*$  are shown. Here, a case where the adjustment phase  $\theta_o$  for the zero-phase-sequence voltage command  $V_o^*$  is increased is shown, and a zero-phase-sequence voltage command  $V_o^{*a}$ , an arm voltage command  $V_A^{*a}$ , an upper margin  $\sigma_{Ua}$ , and a lower margin  $\sigma_{La}$  are waveforms before phase adjustment.

**[0098]** Here, waveforms for the arm Nu are shown. The capacitor voltage sum  $V_{cA}$ , the arm voltage command  $V_A^*$ , the upper margin  $\sigma_U$ , and the lower margin  $\sigma_L$  may be read as being replaced with a capacitor voltage sum  $V_{cANu}$ , an arm voltage command  $V_{ANu}^*$ , an upper margin  $\sigma_{UNu}$ , and a lower margin  $\sigma_{LNU}$ .

**[0099]** In a case where positive power is transmitted from the AC grid 2 to the DC circuit 4, the capacitor voltage sum  $V_{cANu}$  for the arm Nu pulsates as follows, in accordance with the above Expression (8). That is, on the capacitor voltage sum  $V_{cANu}$ , negative-direction pulsation is superimposed in a range of  $0 \leq \theta_s \leq \pi/2$ , and positive-direction pulsation is superimposed in a range of  $\pi/2 \leq \theta_s \leq \pi$ .

**[0100]** If the adjustment phase  $\theta_o$  for the zero-phase-sequence voltage command  $V_o^*$  is 0, the arm voltage command  $V_{ANu}^*$  has local maximum values at  $\theta_s = \pi/3$  and  $2\pi/3$ . Therefore, around  $\theta_s = \pi/3$ , the capacitor voltage sum  $V_{cANu}$  is small and the range of voltage that can be outputted is small, so that the upper margin  $\sigma_{UNu}$  also becomes small. Around  $\theta_s = 2\pi/3$ , the capacitor voltage sum  $V_{cANu}$  is great and the range of voltage that can be outputted is great, so that the upper margin  $\sigma_{UNu}$  also becomes great.

**[0101]** It is known that, in the arm voltage command  $V_{ANu}^*$  shown by the above Expression (5), the necessary output voltage range can be effectively reduced in a case of  $a = 1/6$ , and the arm voltage command  $V_{ANu}^*$  can be represented by the following Expression (9).

$$V_{ANu}^* = (V_{dc}/2) + V_p \cdot \sin(\theta_s + \theta_v) + (1/6) \cdot V_p \cdot \sin 3(\theta_s + \theta_v + \theta_o) \quad \dots (9)$$

**[0102]** On the basis of the above Expression (9), the upper margin  $\sigma_{UNu}$  and the lower margin  $\sigma_{LNU}$  for the arm Nu are calculated so as to be represented by the following Expression (10) and Expression (11).

$$\sigma_{UNu} = V_{cANu} - ((V_{dc}/2) + V_p \cdot \sin(\theta_s + \theta_v) + (1/6) \cdot V_p \cdot \sin 3(\theta_s + \theta_v + \theta_o)) \quad \dots (10)$$

$$\sigma_{LNU} = (V_{dc}/2) + V_p \cdot \sin(\theta_s + \theta_v) + (1/6) \cdot V_p \cdot \sin 3(\theta_s + \theta_v + \theta_o) \quad \dots (11)$$

**[0103]** The adjustment phase  $\theta_o (= \omega t)$  for the zero-phase-sequence voltage command  $V_o^*$  changes, and if the above Expression (10) and Expression (11) are differentiated with respect to the adjustment phase  $\theta_o$ , the following Expression (12) and Expression (13) are obtained. Here,  $V_{cANu}$  in Expression (10) is hardly influenced by the zero-phase-sequence voltage command  $V_o^*$  and therefore is neglected.

$$\sigma_{UNu}/dt = -(1/2) \cdot V_p \cdot \cos 3(\theta_s + \theta_v + \theta_o) \quad \dots (12)$$

$$\sigma_{LNU}/dt = (1/2) \cdot V_p \cdot \cos 3(\theta_s + \theta_v + \theta_o) \quad \dots (13)$$

**[0104]** From Expression (12) and Expression (13), as shown in FIG. 9, when the adjustment phase  $\theta_o$  is increased, the upper margin  $\sigma_{UNu}$  around  $\theta_s + \theta_v = \pi/3$  (region X1) increases, and the upper margin  $\sigma_{UNu}$  around  $\theta_s + \theta_v = 2\pi/3$

(region X2) decreases. In addition, the lower margin  $\sigma_{LNU}$  around  $\theta_s + \theta_v = 4\pi/3$  (region X3) increases, and the lower margin  $\sigma_{LNU}$  around  $\theta_s + \theta_v = 5\pi/3$  (region X4) decreases.

**[0105]** Conversely, when the adjustment phase  $\theta_o$  is decreased, the upper margin  $\sigma_{UNu}$  around  $\theta_s + \theta_v = \pi/3$  (region X1) decreases, and the upper margin  $\sigma_{UNu}$  around  $\theta_s + \theta_v = 2\pi/3$  (region X2) increases. In addition, the lower margin  $\sigma_{LNU}$  around  $\theta_s + \theta_v = 4\pi/3$  (region X3) decreases, and the lower margin  $\sigma_{LNU}$  around  $\theta_s + \theta_v = 5\pi/3$  (region X4) increases.

**[0106]** As described above, through phase adjustment of the zero-phase-sequence voltage command  $V_o^*$ , the minimum value  $\sigma_{Umin}$  of the upper margin  $\sigma_U$  obtained in the region X1 or the region X2 based on the reference phase ( $\theta_s + \theta_v$ ) and the minimum value  $\sigma_{Lmin}$  of the lower margin  $\sigma_L$  obtained in the region X3 or the region X4 are changed. At this time, by changing the adjustment phase  $\theta_o$  so that the smaller one of the two minimum values  $\sigma_{Umin}$ ,  $\sigma_{Lmin}$  increases, the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range is increased.

**[0107]** In the case shown in FIG. 9, before the phase adjustment, the minimum value  $\sigma_{Umin}$  of the upper margin  $\sigma_{Ua}$  obtained in the region X1 is smaller than the minimum value  $\sigma_{Lmin}$  of the lower margin  $\sigma_{La}$  obtained in the region X4, and therefore the adjustment phase  $\theta_o$  is increased to increase the minimum value  $\sigma_{Umin}$  of the upper margin  $\sigma_{Ua}$ .

**[0108]** In the region X1 and the region X3, the margin (upper margin  $\sigma_U$  or lower margin  $\sigma_L$ ) increases with increase in the adjustment phase  $\theta_o$ , and in the regions X2 and X4, the margin (upper margin  $\sigma_U$  or lower margin  $\sigma_L$ ) decreases with increase in the adjustment phase  $\theta_o$ . Therefore, a case where the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range becomes greatest is when the smaller one of the minimum value of the upper margin  $\sigma_U$  in the region X1 and the minimum value of the lower margin  $\sigma_L$  in the region X3 coincides with the smaller one of the minimum value of the upper margin  $\sigma_U$  in the region X2 and the minimum value of the lower margin  $\sigma_L$  in the region X4.

**[0109]** FIG. 10 to FIG. 12 are waveform diagrams at various parts, for illustrating operation of the power conversion device, and show cases where the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range becomes greatest. In FIG. 10 to FIG. 12, as in FIG. 9, the capacitor voltage sum  $V_{cA}$ , the arm voltage command  $V_A^*$ , the upper margin  $\sigma_U$ , the lower margin  $\sigma_L$ , and the zero-phase-sequence voltage command  $V_o^*$  are shown.

**[0110]** FIG. 10 and FIG. 11 show cases where the adjustment phase  $\theta_o$  for the zero-phase-sequence voltage command  $V_o^*$  is increased, and the zero-phase-sequence voltage command  $V_o^*a$ , the arm voltage command  $V_A^*a$ , the upper margin  $\sigma_{Ua}$ , and the lower margin  $\sigma_{La}$  are waveforms before phase adjustment. FIG. 12 shows a case where the adjustment phase  $\theta_o$  is kept without being changed, and the zero-phase-sequence voltage command  $V_o^*a$  before phase adjustment overlaps the zero-phase-sequence voltage command  $V_o^*$ .

**[0111]** Also in FIG. 10 to FIG. 12, waveforms for the arm Nu are shown, and the capacitor voltage sum  $V_{cA}$ , the arm voltage command  $V_A^*$ , the upper margin  $\sigma_U$ , and the lower margin  $\sigma_L$  may be read as being replaced with the capacitor voltage sum  $V_{cANu}$ , the arm voltage command  $V_{ANu}^*$ , the upper margin  $\sigma_{UNu}$ , and the lower margin  $\sigma_{LNU}$ . Although not shown, as in FIG. 9, regions of the reference phase ( $\theta_s + \theta_v$ ) around  $\pi/3$ , around  $2\pi/3$ , around  $4\pi/3$ , and around  $5\pi/3$  are defined as a region X1, a region X2, a region X3, and a region X4, respectively.

**[0112]** In the case shown in FIG. 10, the adjustment phase  $\theta_o$  is increased so that the minimum value  $\sigma_{Umin}$  of the upper margin  $\sigma_U$  obtained in the region X1 and the minimum value  $\sigma_{Lmin}$  of the lower margin  $\sigma_L$  obtained in the region X4 become equal to each other. In this case, the minimum value of the upper margin  $\sigma_U$  in the region X1 is smaller than the minimum value of the lower margin  $\sigma_L$  in the region X3, and the minimum value of the lower margin  $\sigma_L$  in the region X4 is smaller than the minimum value of the upper margin  $\sigma_U$  in the region X2.

**[0113]** Then, the minimum value ( $\sigma_{Umin}$ ) of the upper margin  $\sigma_U$  in the region X1 and the minimum value ( $\sigma_{Lmin}$ ) of the lower margin  $\sigma_L$  in the region X4 are compared with each other, and in this case, the adjustment phase  $\theta_o$  is increased. Thus,  $\sigma_{Umin}$  is increased and  $\sigma_{Lmin}$  is decreased so as to make  $\sigma_{Umin}$  and  $\sigma_{Lmin}$  equal to each other.

**[0114]** In the case shown in FIG. 11, the adjustment phase  $\theta_o$  is increased so that the minimum value of the upper margin  $\sigma_U$  in the region X1 and the minimum value of the upper margin  $\sigma_U$  in the region X2 become an equal minimum value  $\sigma_{Umin}$ . In this case, the minimum value of the upper margin  $\sigma_U$  in the region X1 is smaller than the minimum value of the lower margin  $\sigma_L$  in the region X3, and the minimum value of the upper margin  $\sigma_U$  in the region X2 is smaller than the minimum value ( $\sigma_{Lmin}$ ) of the lower margin  $\sigma_L$  in the region X4.

**[0115]** Then, the minimum value of the upper margin  $\sigma_U$  in the region X1 and the minimum value of the upper margin  $\sigma_U$  in the region X2 are compared with each other, and in this case, the adjustment phase  $\theta_o$  is increased. Thus, the minimum value of the upper margin  $\sigma_U$  in the region X1 is increased and the minimum value of the upper margin  $\sigma_U$  in the region X2 is decreased so that both values become an equal minimum value  $\sigma_{Umin}$ .

**[0116]** In the case shown in FIG. 12, the minimum value of the lower margin  $\sigma_L$  in the region X3 and the minimum value of the lower margin  $\sigma_L$  in the region X4 become an equal minimum value  $\sigma_{Lmin}$ . In this case, the minimum value of the lower margin  $\sigma_L$  in the region X3 is smaller than the minimum value ( $\sigma_{Umin}$ ) of the upper margin  $\sigma_U$  in the region X1, and the minimum value of the lower margin  $\sigma_L$  in the region X4 is smaller than the minimum value of the upper margin  $\sigma_U$  in the region X2. Then, the minimum value of the lower margin  $\sigma_L$  in the region X3 and the minimum value of the lower margin  $\sigma_L$  in the region X4 are compared with each other, and in this case, both values are an equal minimum value  $\sigma_{Lmin}$ . Therefore, the adjustment phase  $\theta_o$  is not changed.

**[0117]** In the control device 20, in accordance with the capacitance of the DC capacitor 13, the AC voltage  $V_{ac}$ , the

DC voltage  $V_{dc}$ , or the like in the power converter 10, a circuit constant, and the operation state of the power converter 10, the above-described method is applied, thereby changing the adjustment phase  $\theta_0$  so as to maximize the margin of the arm voltage command  $VA^*$  with respect to the output voltage range.

**[0118]** Hereinafter, a specific adjustment method for the adjustment phase  $\theta_0$  will be described with reference to FIG. 13.

**[0119]** FIG. 13 is a waveform diagram showing the arm voltage command (lower margin  $\sigma_L$ ) and the control margin (upper margin  $\sigma_U$ ) for the arm  $N_u$ .

**[0120]** As shown in FIG. 13, for the arm  $N_u$ , in one cycle of the AC voltage, the upper margin  $\sigma_U$  has one or two first local minimum values  $\sigma_{U\alpha}$ ,  $\sigma_{U\beta}$  which can become the minimum value thereof, in a first half cycle range of  $0 \leq \theta_s + \theta_v < \pi$ . In addition, the lower margin  $\sigma_L$  has one or two second local minimum values  $\sigma_{L\alpha}$ ,  $\sigma_{L\beta}$  which can become the minimum value thereof, in a second half cycle range of  $\pi \leq \theta_s + \theta_v < 2\pi$ . Here, a case where there are two first local minimum values  $\sigma_{U\alpha}$ ,  $\sigma_{U\beta}$  in the first half cycle range and there are two second local minimum values  $\sigma_{L\alpha}$ ,  $\sigma_{L\beta}$  in the second half cycle range, is shown.

**[0121]** Here, the first local minimum value  $\sigma_{U\alpha}$  is a value (magnitude:  $U_1$ ) around  $\theta_s + \theta_v = \pi/3$  (region X1) in the first half ( $0 \leq \theta_s + \theta_v < \pi/2$ ) of the first half cycle, and the first local minimum value  $\sigma_{U\beta}$  is a value (magnitude:  $U_2$ ) around  $\theta_s + \theta_v = 2\pi/3$  (region X2) in the second half ( $\pi/2 \leq \theta_s + \theta_v < \pi$ ) of the first half cycle. In addition, the second local minimum value  $\sigma_{L\alpha}$  is a value (magnitude:  $L_1$ ) around  $\theta_s + \theta_v = 4\pi/3$  (region X3) in the first half ( $\pi \leq \theta_s + \theta_v < 3\pi/2$ ) of the second half cycle, and the second local minimum value  $\sigma_{L\beta}$  is a value (magnitude:  $L_2$ ) around  $\theta_s + \theta_v = 5\pi/3$  (region X4) in the second half ( $3\pi/2 \leq \theta_s + \theta_v < 2\pi$ ) of the second half cycle.

**[0122]** In the control device 20, first, the phase adjustment unit 32 of the zero-phase-sequence voltage command generation unit 25 monitors the upper margin  $\sigma_U$  and the lower margin  $\sigma_L$ , and detects the first local minimum values  $\sigma_{U\alpha}$ ,  $\sigma_{U\beta}$  and the second local minimum values  $\sigma_{L\alpha}$ ,  $\sigma_{L\beta}$  in one cycle of the AC voltage. As an example of the detection method, detection is performed when the upper margin  $\sigma_U$  or the lower margin  $\sigma_L$  has become greater than the value in the previous cycle through consecutive three sampling cycles.

**[0123]** Next, from the detected first local minimum values  $\sigma_{U\alpha}$ ,  $\sigma_{U\beta}$  and second local minimum values  $\sigma_{L\alpha}$ ,  $\sigma_{L\beta}$ , a third local minimum value which is smallest in a range of the first half of the first half cycle and the first half of the second half cycle, is extracted. That is, the first local minimum value  $\sigma_{U\alpha}$  and the second local minimum value  $\sigma_{L\alpha}$  are compared with each other, and the smaller one is extracted as the third local minimum value.

**[0124]** Similarly, a fourth local minimum value which is smallest in a range of the second half of the first half cycle and the second half of the second half cycle, is extracted. That is, the first local minimum value  $\sigma_{U\beta}$  and the second local minimum value  $\sigma_{L\beta}$  are compared with each other, and the smaller one is extracted as the fourth local minimum value.

**[0125]** In a case where one of the two local minimum values (first local minimum value  $\sigma_{U\alpha}$  and second local minimum value  $\sigma_{L\alpha}$ ) to be used for extracting the third local minimum value is absent, the detected other local minimum value is used as the third local minimum value. Similarly, in a case where one of the two local minimum values (first local minimum value  $\sigma_{U\beta}$  and second local minimum value  $\sigma_{L\beta}$ ) to be used for extracting the fourth local minimum value is absent, the detected other local minimum value is used as the fourth local minimum value.

**[0126]** Then, the third local minimum value is subtracted from the fourth local minimum value, to calculate a deviation. When the deviation is positive, the adjustment phase  $\theta_0$  for the zero-phase-sequence voltage command  $Vo^*$  is increased, and when the deviation is negative, the adjustment phase  $\theta_0$  is decreased.

**[0127]** Here, in a case of  $U_1 < L_2 < U_2 < L_1$ , the third local minimum value is  $U_1$  (first local minimum value  $\sigma_{U\alpha}$ ) and the fourth local minimum value is  $L_2$  (second local minimum value  $\sigma_{L\beta}$ ), and the deviation is positive. Thus, the adjustment phase  $\theta_0$  is increased.

**[0128]** Regarding increase/decrease of the adjustment phase  $\theta_0$ , the adjustment phase  $\theta_0$  may be changed on a certain value basis, or integral control or the like may be used. In addition, with a set value provided in advance, if the deviation obtained by subtracting the third local minimum value from the fourth local minimum value is smaller than the set value, the adjustment phase  $\theta_0$  may be fixed without being changed. This can prevent the adjustment phase  $\theta_0$  from being frequently changed every time the arm voltage command  $VA^*$  or the capacitor voltage sum  $V_{cA}$  for the arm is slightly changed due to disturbance or the like. Therefore, a phenomenon in which new disturbance occurs due to frequent change of the adjustment phase  $\theta_0$  so that the adjustment phase  $\theta_0$  cannot converge, does not happen, and thus the adjustment phase  $\theta_0$  can be reliably controlled.

**[0129]** In the present embodiment, as described above, by performing adjustment to increase/decrease the adjustment phase  $\theta_0$ , phase adjustment of the zero-phase-sequence voltage command  $Vo^*$  is performed. Thus, even if the capacitor voltage sum  $V_{cA}$  pulsates, the margin of the arm voltage command  $VA^*$  with respect to the output voltage range based on the capacitor voltage sum  $V_{cA}$  can be increased, whereby utilization of DC voltage can be assuredly improved.

**[0130]** In the above phase adjustment, the case of adjusting the adjustment phase  $\theta_0$  for the arm voltage command  $VA^*$  for the U-phase lower arm  $N_u$  has been shown, and the zero-phase-sequence voltage command  $Vo^*$  thus obtained is used in common for all the arms  $P_u$ ,  $N_u$ ,  $P_v$ ,  $N_v$ ,  $P_w$ ,  $N_w$ . Under the assumption that the AC grid 2 is in a three-phase balanced state, calculation of the adjustment phase  $\theta_0$  may be performed for at least one of the six arms  $P_u$ ,  $N_u$ ,  $P_v$ ,  $N_v$ ,  $P_w$ ,  $N_w$ , whereby the margin of the arm voltage command  $VA^*$  with respect to the output voltage range can be

increased for all the arms and thus utilization of DC voltage can be assuredly improved.

#### Embodiment 2

**[0131]** In the above Embodiment 1, the case where calculation of phase adjustment for the zero-phase-sequence voltage command  $V_o^*$  is performed for one arm has been shown.

**[0132]** In Embodiment 2, for all the six arms Pu, Nu, Pv, Nv, Pw, Nw included in the power converter 10, six values of each of the first local minimum values  $\sigma U_\alpha$ ,  $\sigma U_\beta$  and the second local minimum values  $\sigma L_\alpha$ ,  $\sigma L_\beta$  of the upper margin  $\sigma U$  and the lower margin  $\sigma L$  are detected per one cycle of the AC voltage. Then, among the six detected values of each local minimum value, the smallest first local minimum values  $\sigma U_{\alpha min}$ ,  $\sigma U_{\beta min}$  and second local minimum values  $\sigma L_{\alpha min}$ ,  $\sigma L_{\beta min}$  are extracted.

**[0133]** The subsequent method is the same as in the above Embodiment 1. That is, among the first local minimum values  $\sigma U_{\alpha min}$ ,  $\sigma U_{\beta min}$  and the second local minimum values  $\sigma L_{\alpha min}$ ,  $\sigma L_{\beta min}$ , the first local minimum value  $\sigma U_{\alpha min}$  and the second local minimum value  $\sigma L_{\alpha min}$  are compared with each other, and the smaller one is extracted as the third local minimum value. Similarly, the first local minimum value  $\sigma U_{\beta min}$  and the second local minimum value  $\sigma L_{\beta min}$  are compared with each other, and the smaller one is extracted as the fourth local minimum value.

**[0134]** Then, the third local minimum value is subtracted from the fourth local minimum value, to calculate a deviation. When the deviation is positive, the adjustment phase  $\theta_o$  for the zero-phase-sequence voltage command  $V_o^*$  is increased, and when the deviation is negative, the adjustment phase  $\theta_o$  is decreased.

**[0135]** As described above, by performing adjustment to increase/decrease the adjustment phase  $\theta_o$ , phase adjustment of the zero-phase-sequence voltage command  $V_o^*$  is performed. Thus, even if the capacitor voltage sum  $V_{cA}$  pulsates, the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range based on the capacitor voltage sum  $V_{cA}$  can be increased, whereby utilization of DC voltage can be assuredly improved.

**[0136]** The AC grid 1 is basically in a three-phase balanced state, but in actuality, there is a case of not being in a three-phase balanced state. In addition, in a case where one of the converter cells 11 in any arm of the power converter 10 has failed, operation is performed by bypassing the failed converter cell 11 via the bypass switch 15. In this case, the number of the converter cells 11 that can perform output becomes smaller in the arm than in the other normal arms, so that the voltage that can be outputted decreases, and also, since the number of the DC capacitors 13 becomes small, pulsation of the capacitor voltage sum  $V_{cA}$  also increases. Therefore, for the arm including the failed converter cell 11, the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range tends to be smaller as compared to the other normal arms.

**[0137]** In the present embodiment, as described above, the upper margins  $\sigma U$  and the lower margins  $\sigma L$  for all the arms are monitored, and calculation of phase adjustment is performed on the basis of the first local minimum values  $\sigma U_\alpha$ ,  $\sigma U_\beta$  and the second local minimum values  $\sigma L_\alpha$ ,  $\sigma L_\beta$  for all the arms.

**[0138]** Thus, even in a case where the three-phase balance of the AC grid 2 is lost or a case where there are variations in the main circuit constants for the arms or there are variations in the numbers of normal converter cells 11 in the arms of the power converter 10, the margins of the arm voltage commands  $V_A^*$  with respect to the output voltage range can be increased in the entire power conversion device 1. That is, while the margin for one arm is improved, a problem such as deterioration in the margins for the other arms does not occur, and for all the arms, the arm voltage commands  $V_A^*$  can fall within the output voltage range with margins provided, whereby utilization of DC voltage can be assuredly improved with high reliability.

#### Embodiment 3

**[0139]** In the above embodiments 1 and 2, for phase adjustment of the zero-phase-sequence voltage command  $V_o^*$ , the upper margin  $\sigma U$  and the lower margin  $\sigma L$  for the arm are monitored and the first local minimum values  $\sigma U_\alpha$ ,  $\sigma U_\beta$  and the second local minimum values  $\sigma L_\alpha$ ,  $\sigma L_\beta$  are detected in one cycle of the AC voltage.

**[0140]** In the present embodiment, extrema of the upper margin  $\sigma U$  and the lower margin  $\sigma L$  are not detected and the minimum value within a divided section is used. Matters other than phase adjustment of the zero-phase-sequence voltage command  $V_o^*$  are the same as in the above Embodiment 1.

**[0141]** FIG. 14 is a waveform diagram showing respective detection sections and phase update of the zero-phase-sequence voltage command in the power conversion device. As shown in FIG. 14, one cycle of the AC grid 2 is divided into six PH sections which are detection sections at  $PH = 0$  to 5, and the adjustment phase  $\theta_o$  is updated at a timing T of a set phase  $\theta_s + \theta_v + \theta_o = \pi/2 + 2m\pi$  ( $m$  is an integer), as a phase adjustment time point. In FIG. 14,  $\theta_s + \theta_v + \theta_o$  ( $\theta_o = \theta_1$ ) before update of the adjustment phase  $\theta_o$  and  $\theta_s + \theta_v + \theta_o$  ( $\theta_o = \theta_1 + \Delta\theta_o$ ) after the update, are shown.

**[0142]** In the control device 20, the phase adjustment unit 32 of the zero-phase-sequence voltage command generation unit 25 monitors the upper margin  $\sigma U$  and the lower margin  $\sigma L$  for the set arm in each PH section ( $PH = 0$  to 5), to detect the upper margin minimum value and the lower margin minimum value, and calculates and updates the adjustment

phase  $\theta_0$  at the timing T.

[0143] Hereinafter, an adjustment method for the adjustment phase  $\theta_0$  according to the present embodiment will be described in detail with reference to FIG. 15 to FIG. 18.

[0144] FIG. 15 is a waveform diagram showing the arm voltage command (lower margin  $\sigma_L$ ) and the control margin (upper margin  $\sigma_U$ ) for each arm in the power conversion device.

[0145] In FIG. 15, waveforms of the upper margin  $\sigma_U$  and the lower margin  $\sigma_L$  for each arm Pu, Nu, Pv, Nv, Pw, Nw in a range of  $0 \leq \theta_s + \theta_v + \theta_0 \leq 2\pi$  are shown. In FIG. 15, for simplification,  $\theta_0$  is not changed at the update timing T ( $\theta_s + \theta_v + \theta_0 = \pi/2$ ).

[0146] A timing at  $\theta_s + \theta_v + \theta_0 = \pi/2$  is a start point of the PH section at PH = 0. For the arm Nu, a first instantaneous value  $\sigma_{U1}$  and a second instantaneous value  $\sigma_{U2}$  where the upper margin  $\sigma_U$  can become the minimum value are in the PH sections at PH = 5 and PH = 0, respectively, and a first instantaneous value  $\sigma_{L1}$  and a second instantaneous value  $\sigma_{L2}$  where the lower margin  $\sigma_L$  can become the minimum value are in the PH sections at PH = 2 and PH = 3, respectively. In the other PH sections at PH = 1 and PH = 4, the AC component of the arm voltage command  $VA^*$  (lower margin  $\sigma_L$ ) passes 0.

[0147] As described above, for each arm, the PH sections corresponding to the first instantaneous value  $\sigma_{U1}$  and the second instantaneous value  $\sigma_{U2}$  where the upper margin  $\sigma_U$  can become the minimum value, and the PH sections corresponding to the first instantaneous value  $\sigma_{L1}$  and the second instantaneous value  $\sigma_{L2}$  where the lower margin  $\sigma_L$  can become the minimum value, are present.

[0148] From the above Expression (12) and Expression (13), when the adjustment phase  $\theta_0$  is increased, the first instantaneous value  $\sigma_{U1}$  of the upper margin  $\sigma_U$  increases and the second instantaneous value  $\sigma_{U2}$  decreases. In addition, the first instantaneous value  $\sigma_{L1}$  of the lower margin  $\sigma_L$  increases and the second instantaneous value  $\sigma_{L2}$  decreases.

[0149] Conversely, when the adjustment phase  $\theta_0$  is decreased, the first instantaneous value  $\sigma_{U1}$  of the upper margin  $\sigma_U$  decreases and the second instantaneous value  $\sigma_{U2}$  increases. In addition, the first instantaneous value  $\sigma_{L1}$  of the lower margin  $\sigma_L$  decreases and the second instantaneous value  $\sigma_{L2}$  increases.

[0150] In each of the PH sections at PH = 0 to 5, four instantaneous values, i.e., the first instantaneous value  $\sigma_{U1}$  and the second instantaneous value  $\sigma_{U2}$  of the upper margins  $\sigma_U$  and the first instantaneous value  $\sigma_{L1}$  and the second instantaneous value  $\sigma_{L2}$  of the lower margins  $\sigma_L$  are each detected for different arms. With reference to FIG. 15, for example, in the PH section at PH = 0, the second instantaneous value  $\sigma_{L2}$  of the lower margin  $\sigma_L$  is detected for the arm Pu, the second instantaneous value  $\sigma_{U2}$  of the upper margin  $\sigma_U$  is detected for the arm Nu, the first instantaneous value  $\sigma_{U1}$  of the upper margin  $\sigma_U$  is detected for the arm Pw, and the first instantaneous value  $\sigma_{L1}$  of the lower margin  $\sigma_L$  is detected for the arm Pv.

[0151] As described above, in each PH section, first to fourth arms which are arms for which the four instantaneous values, i.e., the first instantaneous value  $\sigma_{U1}$  and the second instantaneous value  $\sigma_{U2}$  of the upper margins  $\sigma_U$  and the first instantaneous value  $\sigma_{L1}$  and the second instantaneous value  $\sigma_{L2}$  of the lower margins  $\sigma_L$  are detected, are determined.

[0152] FIG. 16 shows detection arms set for each detection section in the power conversion device. In the control device 20, the phase adjustment unit 32 of the zero-phase-sequence voltage command generation unit 25 stores information in which the first to fourth arms corresponding to the above four instantaneous values  $\sigma_{U1}$ ,  $\sigma_{U2}$ ,  $\sigma_{L1}$ ,  $\sigma_{L2}$  are set in advance in each PH section, as a table as shown in FIG. 16, for example. Then, in accordance with the stored information, the instantaneous values  $\sigma_{U1}$ ,  $\sigma_{U2}$ ,  $\sigma_{L1}$ ,  $\sigma_{L2}$  for the set first to fourth arms are detected in each PH section.

[0153] FIG. 17 and FIG. 18 are flowcharts illustrating operation of the power conversion device. In this case, operation for phase adjustment of the zero-phase-sequence voltage command  $Vo^*$ , i.e., calculation and update of the adjustment phase  $\theta_0$ , by the phase adjustment unit 32 of the zero-phase-sequence voltage command generation unit 25 in the control device 20, will be described.

[0154] First, the phase adjustment unit 32 recognizes the PH section at PH = 0, using the phase  $\theta_s (= \omega t)$  of the AC voltage  $V_{ac}$  from the AC grid 2, phase shift  $\theta_v$  between the AC voltage  $V_{ac}$  and the AC component of the arm voltage command  $VA^*$ , and the adjustment phase  $\theta_0$  (step S00).

[0155] Next, by referring to the stored information in which the first to fourth arms are set, the instantaneous values (first instantaneous value  $\sigma_{U1}$  and second instantaneous value  $\sigma_{U2}$ ) of the upper margins  $\sigma_U$  for the first arm and the second arm and the instantaneous values (first instantaneous value  $\sigma_{L1}$  and second instantaneous value  $\sigma_{L2}$ ) of the lower margins  $\sigma_L$  for the third arm and the fourth arm are detected in the PH section at PH = 0 (step S01).

[0156] Next, for  $\theta^* = \theta_s + \theta_v + \theta_0$ , whether PH = 0 and  $\theta^* \geq 5\pi/6$  are satisfied is determined, and in a case of No, the process returns to step S01 (step S02).

[0157] In a case of Yes in step S02, minimum values  $\sigma_{U1min}$ ,  $\sigma_{U2min}$ ,  $\sigma_{L1min}$ ,  $\sigma_{L2min}$  of the instantaneous values  $\sigma_{U1}$ ,  $\sigma_{U2}$ ,  $\sigma_{L1}$ ,  $\sigma_{L2}$  in the PH section (PH = 0) detected in step S01 are stored as a first value, a second value, a third value, and a fourth value (step S03). Then, the PH section is set to the section at PH = 1 (step S04).

[0158] Next, by referring to the stored information in which the first to fourth arms are set, the instantaneous values

(first instantaneous value  $\sigma U1$  and second instantaneous value  $\sigma U2$ ) of the upper margins  $\sigma U$  for the first arm and the second arm and the instantaneous values (first instantaneous value  $\sigma L1$  and second instantaneous value  $\sigma L2$ ) of the lower margins  $\sigma L$  for the third arm and the fourth arm are detected in the PH section at  $PH = 1$  (step S05).

**[0159]** Next, for  $\theta^* = \theta_s + \theta_v + \theta_o$ , whether  $PH = 1$  and  $\theta^* \geq 7\pi/6$  are satisfied is determined, and in a case of No, the process returns to step S05 (step S06).

**[0160]** In a case of Yes in step S06, minimum values  $\sigma U1min$ ,  $\sigma U2min$ ,  $\sigma L1min$ ,  $\sigma L2min$  of the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  in the PH section ( $PH = 1$ ) detected in step S05 are stored as a first value, a second value, a third value, and a fourth value (step S07). Then, the PH section is set to the section at  $PH = 2$  (step S08).

**[0161]** Next, the above four steps from step 04 to step 08 are repeated while PH is increased by 1 for each time and the range of  $\theta^*$  is also increased by  $\pi/3$  for each time, until the PH section is set to the section at  $PH = 5$  (step S20). Then, in the PH section at  $PH = 5$ , similarly, the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  are detected (step S21).

**[0162]** Next, for  $\theta^* = \theta_s + \theta_v + \theta_o$ , whether  $PH = 5$  and  $\theta^* \geq \pi/2$  are satisfied is determined, and in a case of No, the process returns to step S21 (step S22).

**[0163]** In a case of Yes in step S22, minimum values  $\sigma U1min$ ,  $\sigma U2min$ ,  $\sigma L1min$ ,  $\sigma L2min$  of the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  in the PH section ( $PH = 5$ ) detected in step S21 are detected and stored as a first value, a second value, a third value, and a fourth value (step S23). Then, the adjustment phase  $\theta_o$  is calculated and updated on the basis of the minimum values  $\sigma U1min$ ,  $\sigma U2min$ ,  $\sigma L1min$ ,  $\sigma L2min$  stored in the respective PH sections (step S24), and the process returns to step S00 to set the PH section to the section at  $PH = 0$ .

**[0164]** The calculation of the adjustment phase  $\theta_o$  in step S24 is performed as follows. Each minimum value of six data of each of  $\sigma U1min$ ,  $\sigma U2min$ ,  $\sigma L1min$ ,  $\sigma L2min$  in all the PH sections at  $PH = 0$  to 5 is defined as a first minimum value  $\sigma U1m$ , a second minimum value  $\sigma U2m$ , a third minimum value  $\sigma L1m$ , and a fourth minimum value  $\sigma L2m$ , respectively. Then, the first minimum value  $\sigma U1m$  and the third minimum value  $\sigma L1m$  are compared with each other and the smaller one is extracted as  $\sigma UL1$ , and similarly, the second minimum value  $\sigma U2m$  and the fourth minimum value  $\sigma L2m$  are compared with each other and the smaller one is extracted as  $\sigma UL2$ .

**[0165]** Then, the extracted  $\sigma UL1$  is subtracted from the extracted  $\sigma UL2$ , to calculate a deviation. When the deviation is positive, the adjustment phase  $\theta_o$  for the zero-phase-sequence voltage command  $V_o^*$  is increased, and when the deviation is negative, the adjustment phase  $\theta_o$  is decreased.

**[0166]** Regarding increase/decrease of the adjustment phase  $\theta_o$ , the adjustment phase  $\theta_o$  may be changed on a certain value basis, or integral control or the like may be used.

**[0167]** Here, with a set value provided in advance, if the deviation obtained by subtracting the extracted  $\sigma UL1$  from the extracted  $\sigma UL2$  is smaller than the set value, the adjustment phase  $\theta_o$  may be fixed without being changed. This can prevent the adjustment phase  $\theta_o$  from being frequently changed every time the arm voltage command  $V_A^*$  or the capacitor voltage sum  $V_{cA}$  for the arm is slightly changed due to disturbance or the like, whereby the adjustment phase  $\theta_o$  can be reliably controlled.

**[0168]** In the present embodiment, as described above, by performing adjustment to increase/decrease the adjustment phase  $\theta_o$ , phase adjustment of the zero-phase-sequence voltage command  $V_o^*$  is performed. Thus, even if the capacitor voltage sum  $V_{cA}$  pulsates, the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range based on the capacitor voltage sum  $V_{cA}$  can be increased, whereby utilization of DC voltage can be assuredly improved.

**[0169]** In addition, using instantaneous value information of the upper margins  $\sigma U$  and the lower margins  $\sigma L$  for all the arms, the adjustment phase  $\theta_o$  is adjusted to be increased/decreased so that the smallest margin ( $\sigma U$ ,  $\sigma L$ ) increases. Thus, even in a case where the three-phase balance of the AC grid 2 is lost or a case where there are variations in the main circuit constants for the arms or there are variations in the numbers of normal converter cells 11 in the arms of the power converter 10, the margins of the arm voltage commands  $V_A^*$  with respect to the output voltage range can be increased in the entire power conversion device 1.

**[0170]** In addition, in the present embodiment, on the basis of information of the first to fourth arms set in advance for each PH section, the first minimum value  $\sigma U1m$  and the second minimum value  $\sigma U2m$  of the upper margins  $\sigma U$  and the third minimum value  $\sigma L1m$  and the fourth minimum value  $\sigma L2m$  of the lower margins  $\sigma L$  are detected, and phase adjustment of the zero-phase-sequence voltage command  $V_o^*$  is performed so as to increase the margin of the arm voltage command  $V_A^*$  with respect to the output voltage range.

**[0171]** Therefore, it is not necessary to detect the local minimum values  $\sigma U\alpha$ ,  $\sigma U\beta$ ,  $\sigma L\alpha$ ,  $\sigma L\beta$  of the upper margin  $\sigma U$  and the lower margin  $\sigma L$  as shown in the above embodiments 1 and 2. Presence/absence or the number of the local minimum values of each of the upper margin  $\sigma U$  and the lower margin  $\sigma L$  in a range of interest is not constant, and detection for the local minimum values is performed by recognizing the crests and the troughs of the waveforms of the upper margin  $\sigma U$  and the lower margin  $\sigma L$  and therefore is complicated.

**[0172]** In the present embodiment, without using the local minimum values of the upper margin  $\sigma U$  and the lower margin  $\sigma L$ , phase adjustment of the zero-phase-sequence voltage command  $V_o^*$  can be performed easily and reliably.

## Embodiment 4

**[0173]** In the present embodiment, as in the above Embodiment 3, on the basis of information of the first to fourth arms set in advance for each PH section, the first minimum value  $\sigma U1m$  and the second minimum value  $\sigma U2m$  of the upper margins  $\sigma U$  and the third minimum value  $\sigma L1m$  and the fourth minimum value  $\sigma L2m$  of the lower margins  $\sigma L$  are detected to perform adjustment to increase/decrease the adjustment phase  $\theta o$ .

**[0174]** In the above Embodiment 3, the adjustment phase  $\theta o$  is updated at the timing T for every cycle of the AC grid 2, whereas in the present embodiment, a period in which detection for the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  of the upper margins  $\sigma U$  and the lower margins  $\sigma L$  is stopped is provided and the update interval for the adjustment phase  $\theta o$  is expanded.

**[0175]** Hereinafter, update of the adjustment phase  $\theta o$  in Embodiment 4 will be described on the basis of comparison with the above Embodiment 3.

**[0176]** FIG. 19 is a waveform diagram showing phase update of the zero-phase-sequence voltage command in the power conversion device according to the above Embodiment 3. FIG. 20 is a waveform diagram showing phase update of the zero-phase-sequence voltage command in the power conversion device according to Embodiment 4.

**[0177]** The first update timing T is  $\theta s + \theta v + \theta o = \pi/2$ , and in the graphs,  $\theta s + \theta v + \theta o$  ( $\theta o = \theta 1$ ) before update of the adjustment phase  $\theta o$  and  $\theta s + \theta v + \theta o$  ( $\theta o = \theta 1 + \Delta\theta o$ ) after the update are shown.

**[0178]** In the above Embodiment 3 shown in FIG. 19, the next update timing T is a timing at  $\theta s + \theta v + \theta 1 + \Delta\theta o = \pi/2 + 2\pi$ . That is, the next update timing T is a timing at  $\theta s + \theta v + \theta 1 = \pi/2 - \Delta\theta o + 2\pi$ . In a case where  $\Delta\theta o$  is positive, in a period 40 of  $\pi/2 - \Delta\theta o \leq \theta s + \theta v + \theta 1 < \pi/2$ , the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  cannot be detected, and as a result, reliability of the first minimum value  $\sigma U1m$  and the second minimum value  $\sigma U2m$  of the upper margins  $\sigma U$  and the third minimum value  $\sigma L1m$  and the fourth minimum value  $\sigma L2m$  of the lower margins  $\sigma L$  is deteriorated.

**[0179]** On the other hand, in Embodiment 4 shown in FIG. 20, a period 41 in which the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  are continuously detected, and a period 42 in which detection for the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  is stopped, are provided. At the timing T ( $\theta s + \theta v + \theta o = \pi/2$ ) when the continuous detection period 41 is finished, the adjustment phase  $\theta o$  is updated from  $\theta 1$  to  $\theta 1 + \Delta\theta o$ . Then, the detection stop period 42 of  $\pi/2 \leq \theta s + \theta v + \theta 1 < \pi/2 - \Delta\theta o + 2\pi$  passes, and in the subsequent continuous detection period 41, the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  are continuously detected over one cycle until the next update timing T ( $\theta s + \theta v + \theta 1 = \pi/2 - \Delta\theta o + 4\pi$ ). Then, at the next update timing T, the adjustment phase  $\theta o$  is updated from  $\theta 1 + \Delta\theta o$  to  $\theta 1 + \Delta\theta o + \Delta\theta oA$ , thus shifting to the detection stop period 42.

**[0180]** FIG. 21 is a flowchart illustrating operation of the power conversion device according to Embodiment 4. In this case, operation for phase adjustment of the zero-phase-sequence voltage command  $Vo^*$ , i.e., calculation and update of the adjustment phase  $\theta o$ , by the phase adjustment unit 32 of the zero-phase-sequence voltage command generation unit 25 in the control device 20, will be described.

**[0181]** First, a determination signal Cal which is 0 or 1 is set to an initial value 1 (step S100).

**[0182]** Next, whether the determination signal Cal is 0 or 1 is determined (step S101). If the determination signal Cal is 1, the processing from step S00 to step S24 shown in the above Embodiment 3 is performed to calculate and update the adjustment phase  $\theta o$  on the basis of the minimum values  $\sigma U1min$ ,  $\sigma U2min$ ,  $\sigma L1min$ ,  $\sigma L2min$  stored in the respective PH sections (step S102), and the determination signal Cal is set to 0 (step S103), to return to step S101.

**[0183]** In step S101, if the determination signal Cal is 0, the PH section is set to the section at  $PH = 0$  (step S 104). Then, for  $\theta^* = \theta s + \theta v + \theta o$ , whether  $PH = 0$  and  $\theta^* \geq 5\pi/6$  are satisfied is determined, and this determination processing is repeated until the determination indicates Yes (step S105). In a case of Yes, the PH section is set to the section at  $PH = 1$  (step S106).

**[0184]** Then, for  $\theta^* = \theta s + \theta v + \theta o$ , whether  $PH = 1$  and  $\theta^* \geq 7\pi/6$  are satisfied is determined, and this determination processing is repeated until the determination indicates Yes (step S 107). In a case of Yes, the PH section is set to the section at  $PH = 2$  (step S108).

**[0185]** The above two steps of step 107 and step 108 are repeated while PH is increased by 1 for each time and the range of  $\theta^*$  is also increased by  $\pi/3$  for each time, until the PH section is set to the section at  $PH = 5$  (step S120). Then, for  $\theta^* = \theta s + \theta v + \theta o$ , whether  $PH = 5$  and  $\theta^* \geq \pi/2$  is satisfied is determined, and this determination process is repeated until the determination indicates Yes (step S121). In a case of Yes, the determination signal Cal is set to 1 (step S122), to return to step S101.

**[0186]** As described above, using the determination signal Cal, if the determination signal Cal is 1, the continuous detection period 41 is set, and if the determination signal Cal is 0, the detection stop period 42 is set. Thus, the continuous detection period 41 for the instantaneous values  $\sigma U1$ ,  $\sigma U2$ ,  $\sigma L1$ ,  $\sigma L2$  can be a period that continues over one cycle, whereby the first minimum value  $\sigma U1m$  and the second minimum value  $\sigma U2m$  of the upper margins  $\sigma U$  and the third minimum value  $\sigma L1m$  and the fourth minimum value  $\sigma L2m$  of the lower margins  $\sigma L$  are reliably acquired and reliability of phase adjustment is improved.

**[0187]** In the above description, the continuous detection period 41 is set as one cycle of the AC voltage. However,

the continuous detection period 41 may be a cycle that is an integer multiple of the AC voltage cycle.

**[0188]** If the continuous detection period 41 is present at least over one cycle of the AC voltage, the detection stop period 42 may not necessarily be provided.

**[0189]** Although the invention is described above in terms of various exemplary embodiments and implementations, it should be understood that the various features, aspects, and functionality described in one or more of the individual embodiments are not limited in their applicability to the particular embodiment with which they are described, but instead can be applied, alone or in various combinations to one or more of the embodiments of the invention.

**[0190]** It is therefore understood that numerous modifications which have not been exemplified can be devised without departing from the scope of the present invention. For example, at least one of the constituent components may be modified, added, or eliminated. At least one of the constituent components mentioned in at least one of the preferred embodiments may be selected and combined with the constituent components mentioned in another preferred embodiment.

#### DESCRIPTION OF THE REFERENCE CHARACTERS

##### **[0191]**

|                                               |                                                     |
|-----------------------------------------------|-----------------------------------------------------|
| 1                                             | power conversion device                             |
| 2                                             | AC grid                                             |
| 4                                             | DC circuit                                          |
| 5P, 5N                                        | DC terminal                                         |
| 6                                             | AC input terminal                                   |
| 10                                            | power converter                                     |
| 11                                            | converter cell                                      |
| 24                                            | arm voltage command generation unit                 |
| 13                                            | DC capacitor                                        |
| 20                                            | control device                                      |
| 25                                            | zero-phase-sequence voltage command generation unit |
| 32                                            | phase adjustment unit                               |
| 41                                            | continuous detection period                         |
| 42                                            | detection stop period                               |
| Pu, Nu, Pv, Nv, Pw, Nw                        | arm                                                 |
| VA*, VAPu*, VANu*, VAPv*, VANv*, VAPw*, VANw* | arm voltage command                                 |
| Vo*                                           | zero-phase-sequence voltage command                 |
| VcA, VcAPu, VcANu, VcAPv, VcANv, VcAPw, VcANw | capacitor voltage sum                               |
| $\sigma U$                                    | upper margin                                        |
| $\sigma L$                                    | lower margin                                        |
| $\sigma U_{min}$                              | minimum value of upper margin                       |
| $\sigma L_{min}$                              | minimum value of lower margin                       |
| $\sigma U_{\alpha}, \sigma U_{\beta}$         | first local minimum value                           |
| $\sigma L_{\alpha}, \sigma L_{\beta}$         | second local minimum value                          |
| $\sigma U_1, \sigma U_2$                      | instantaneous value of upper margin                 |
| $\sigma L_1, \sigma L_2$                      | instantaneous value of lower margin                 |
| $\sigma U_{1min}$                             | first value                                         |
| $\sigma U_{2min}$                             | second value                                        |
| $\sigma L_{1min}$                             | third value                                         |
| $\sigma L_{2min}$                             | fourth value                                        |
| $\sigma U_{1m}$                               | first minimum value                                 |
| $\sigma U_{2m}$                               | second minimum value                                |
| $\sigma L_{1m}$                               | third minimum value                                 |
| $\sigma L_{2m}$                               | fourth minimum value                                |
| $\theta_o$                                    | adjustment phase                                    |
| T                                             | timing of phase adjustment                          |

#### Claims

1. A power conversion device comprising:

a power converter for performing power conversion between a DC circuit and a three-phase AC circuit; and a control device for performing output control of the power converter, wherein the power converter includes, for each phase of the three-phase AC circuit, two arms provided between common DC terminals and connected to each other, a connection portion therebetween being connected to the corresponding phase of the three-phase AC circuit, each of the arms being formed by connecting, in series, a plurality of converter cells each composed of a plurality of semiconductor switching elements and a DC capacitor, and wherein the control device includes a voltage command generation unit which generates, for each of the arms of the power converter, an output voltage command for the plurality of converter cells, and the control device generates, for each of the arms, a base command for output voltage of the plurality of converter cells, performs phase adjustment of a zero-phase-sequence voltage command having a frequency component that is three times a fundamental frequency of the three-phase AC circuit on the basis of voltage of the DC capacitor and the output voltage command, and superimposes the phase-adjusted zero-phase-sequence voltage command on the base command, thus generating the output voltage command.

2. The power conversion device according to claim 1, wherein the control device calculates a control margin by subtracting the output voltage command for the arm from a voltage sum of a plurality of the DC capacitors in the arm, compares a minimum value of the control margin and a minimum value of the output voltage command in one cycle of AC voltage, and performs phase adjustment of the zero-phase-sequence voltage command so that a smaller one of the minimum values increases.

3. The power conversion device according to claim 2, wherein the control device detects, in one cycle of the AC voltage, a first local minimum value that can become the minimum value of the control margin for the arm and a second local minimum value that can become the minimum value of the output voltage command, and performs phase adjustment of the zero-phase-sequence voltage command on the basis of the detected first local minimum value and the detected second local minimum value.

4. The power conversion device according to claim 3,

wherein in one cycle of the AC voltage, there is at least one first local minimum value in a first half cycle and there is at least one second local minimum value in a second half cycle, and the control device extracts, from the first local minimum value and the second local minimum value, a third local minimum value that is smallest in a range of a first half of the first half cycle and a first half of the second half cycle, and a fourth local minimum value that is smallest in a range of a second half of the first half cycle and a second half of the second half cycle, and performs phase adjustment of the zero-phase-sequence voltage command on the basis of a deviation between the third local minimum value and the fourth local minimum value.

5. The power conversion device according to claim 4, wherein the control device detects the first local minimum values and the second local minimum values for all the arms, respectively, and extracts one said third local minimum value and one said fourth local minimum value from the detected first local minimum values and the detected second local minimum values.

6. The power conversion device according to claim 4 or 5, wherein the third local minimum value increases with increase in a phase of the zero-phase-sequence voltage command, and the fourth local minimum value increases with decrease in the phase of the zero-phase-sequence voltage command.

7. The power conversion device according to any one of claims 4 to 6, wherein the control device does not change a phase of the zero-phase-sequence voltage command when the deviation between the third local minimum value and the fourth local minimum value is smaller than a set value.

8. The power conversion device according to claim 2, wherein the control device

calculates the control margin for each of the arms, in each of six sections obtained by dividing one cycle of the AC voltage, sets, in advance, a first arm and a second arm for which the control margin can become the minimum value in the one cycle of the AC voltage, and a third arm and a fourth arm for which the output voltage command can become the minimum value in the one cycle of the AC voltage, among the plurality of arms,

in each of the sections, detects the control margin for the first arm and defines the minimum value thereof as a first value, detects the control margin for the second arm and defines the minimum value thereof as the second value, detects the output voltage command for the third arm and defines the minimum value thereof as a third value, and detects the output voltage command for the fourth arm and defines the minimum value thereof as a fourth value, and  
 at a set phase of the AC voltage, performs phase adjustment of the zero-phase-sequence voltage command on the basis of the first to fourth values.

9. The power conversion device according to claim 8,  
 wherein among the first to fourth arms set in each of the sections,

for the first arm, the control margin in the section increases with increase in a phase of the zero-phase-sequence voltage command,  
 for the second arm, the control margin in the section increases with decrease in the phase of the zero-phase-sequence voltage command,  
 for the third arm, the output voltage command in the section increases with increase in the phase of the zero-phase-sequence voltage command, and  
 for the fourth arm, the output voltage command in the section increases with decrease in the phase of the zero-phase-sequence voltage command, and the control device  
 defines respective minimum values of the first values, the second values, the third values, and the fourth values in all the six divided sections, as a first minimum value, a second minimum value, a third minimum value, and a fourth minimum value, and  
 extracts a smaller one of the first minimum value and the third minimum value, and a smaller one of the second minimum value and the fourth minimum value, and performs phase adjustment of the zero-phase-sequence voltage command on the basis of a deviation between the two extracted values.

10. The power conversion device according to claim 9,  
 wherein the control device does not change the phase of the zero-phase-sequence voltage command when the deviation is smaller than a set value.

11. The power conversion device according to any one of claims 8 to 10,

wherein in a continuous detection period until a phase adjustment time point, the control device detects the control margins for the first and second arms and the output voltage commands for the third and fourth arms, and the continuous detection period is at least one cycle of the AC voltage.

12. The power conversion device according to claim 11,  
 wherein the control device sets the continuous detection period to be an integer multiple of a cycle of the AC voltage, and provides a period in which detection for the control margins for the first and second arms and the output voltage commands for the third and fourth arms is stopped from a previous phase adjustment time point until a start time point of the continuous detection period.

FIG. 1

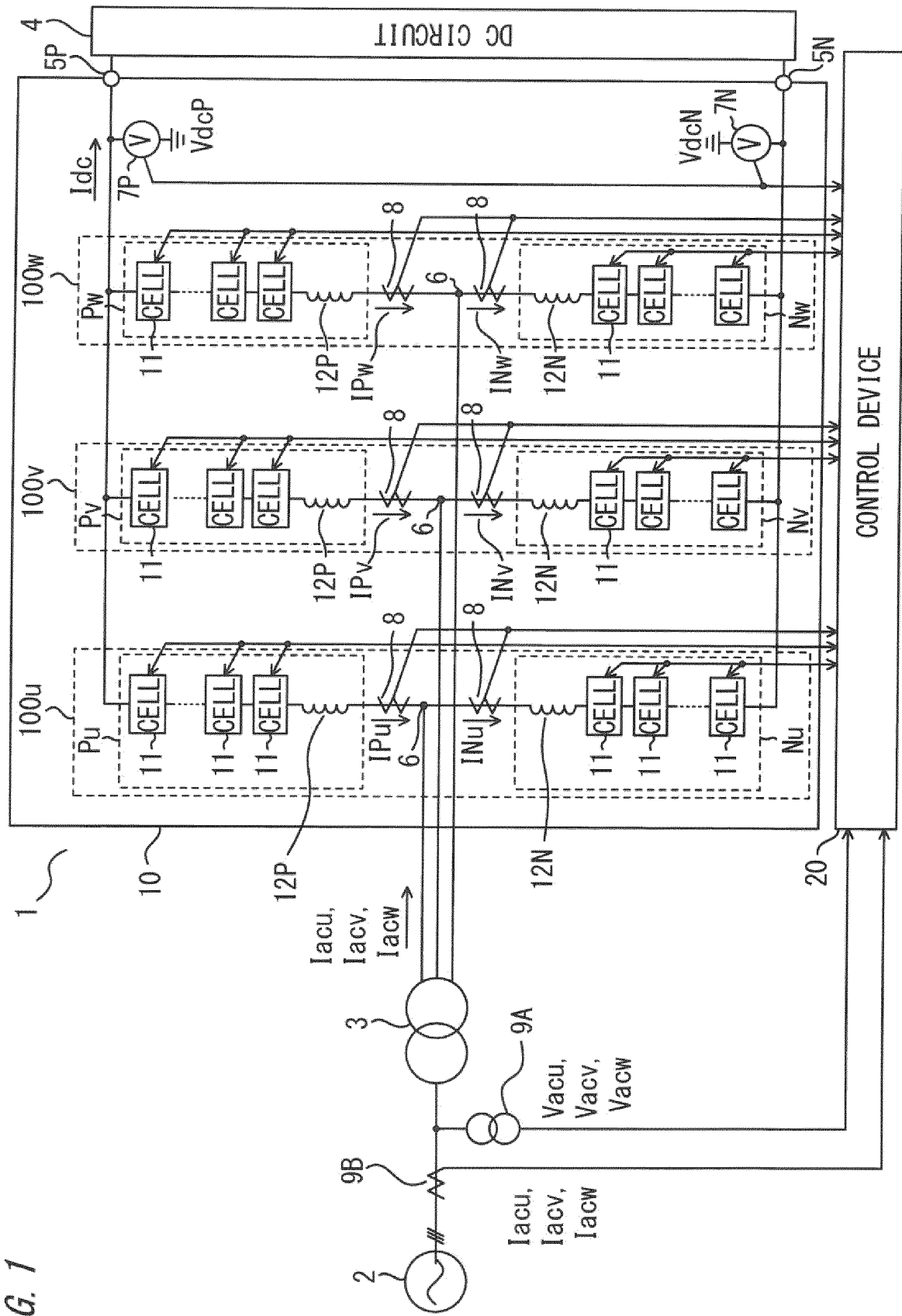


FIG. 2

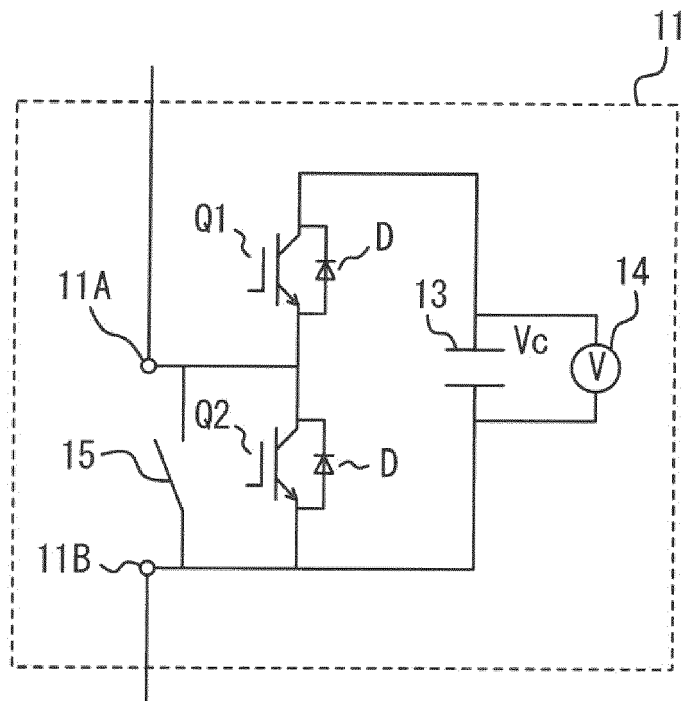


FIG. 3

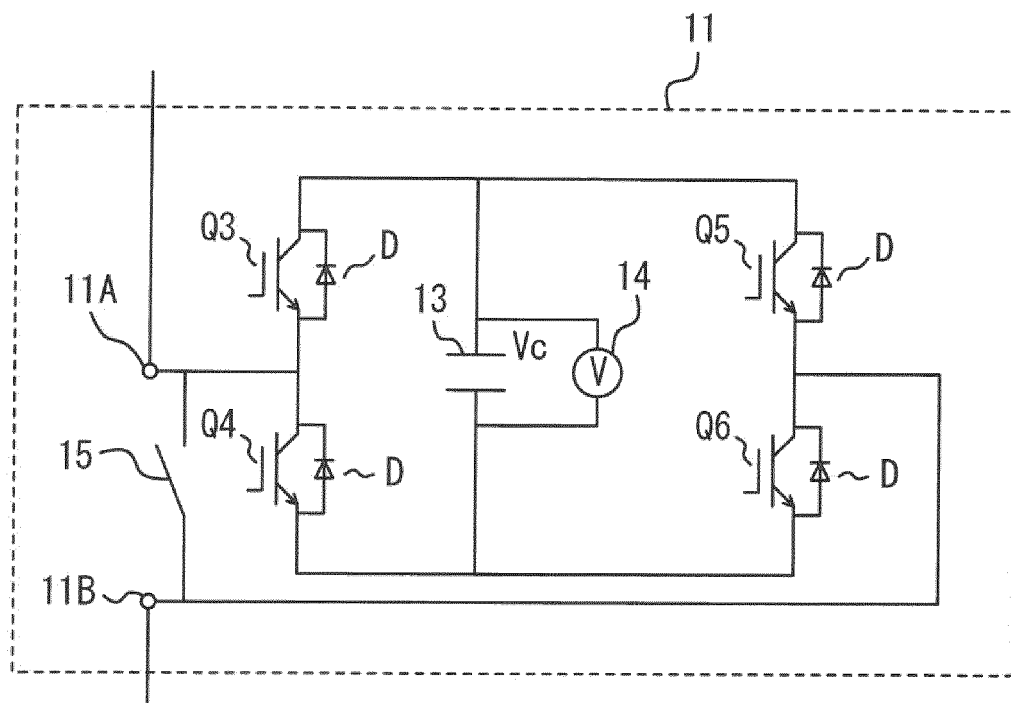


FIG. 4

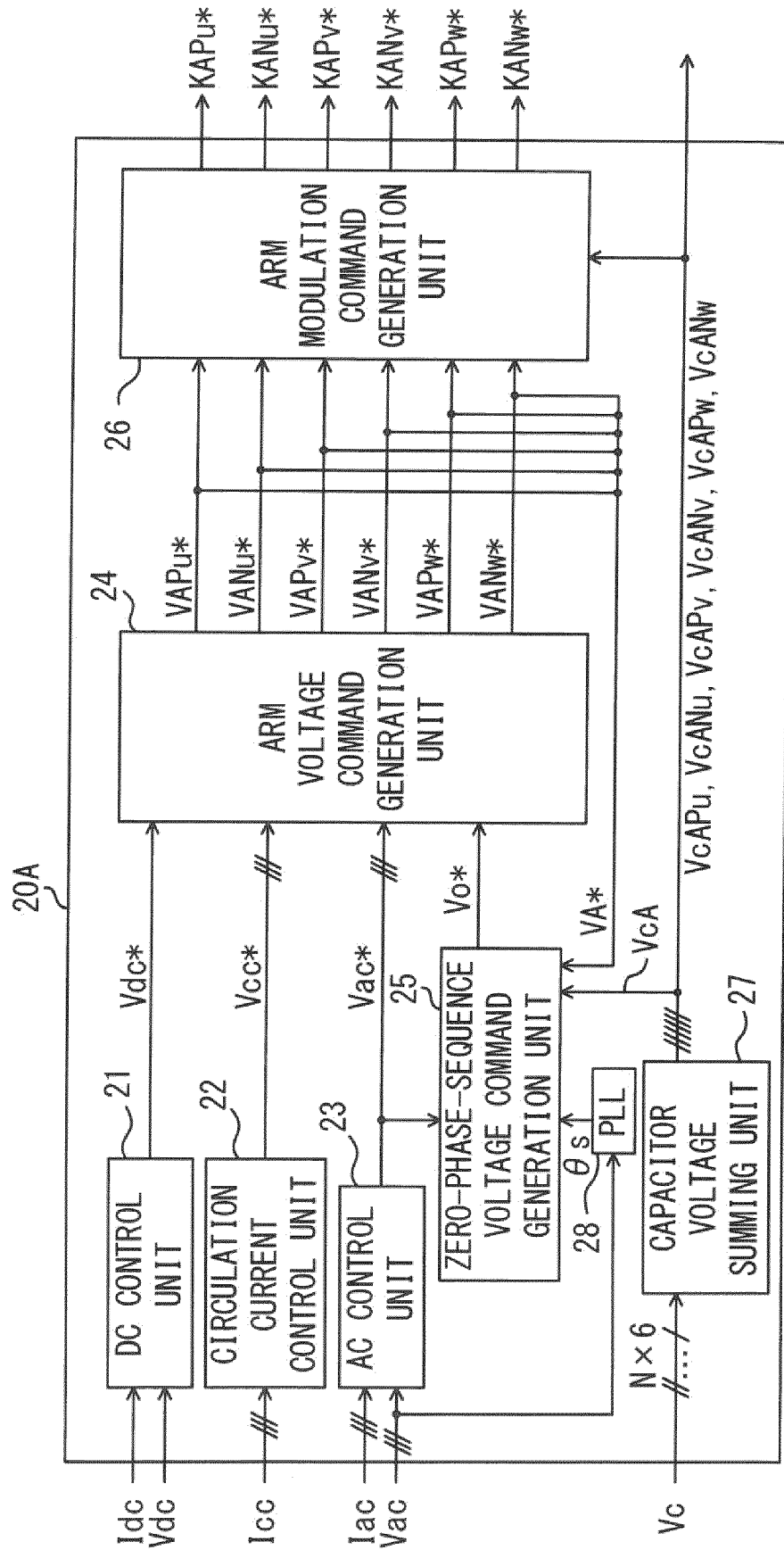


FIG. 5

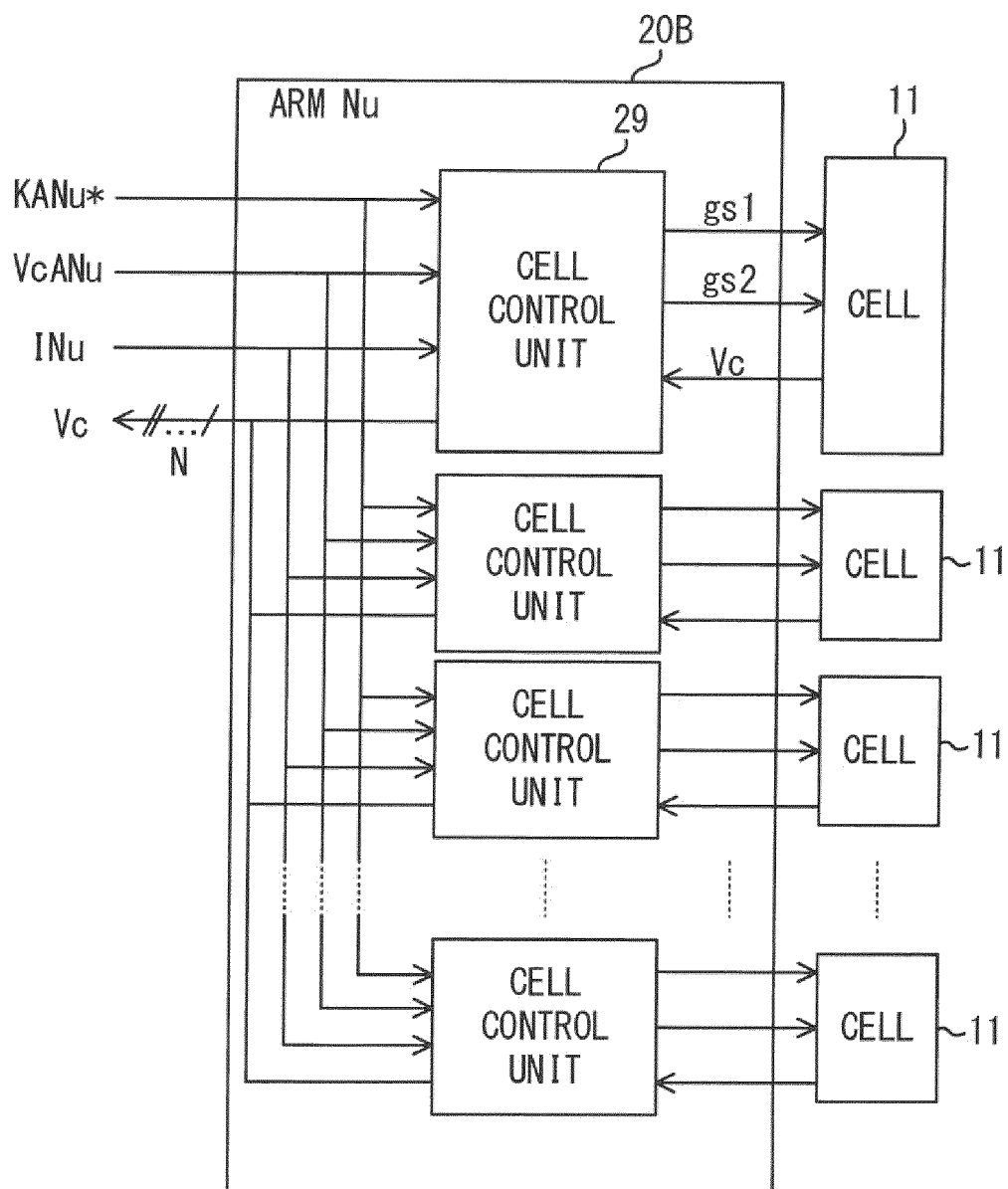


FIG. 6

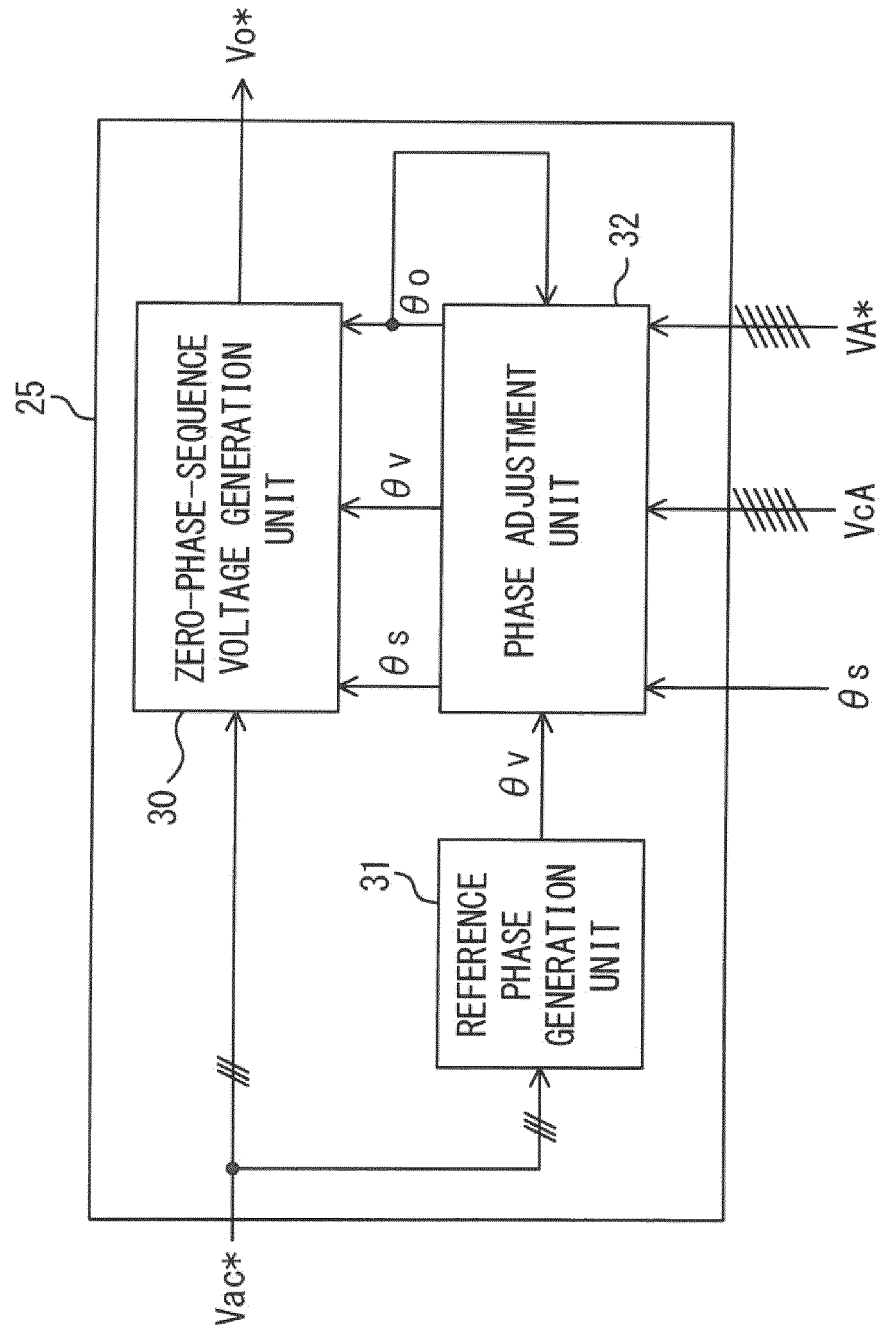


FIG. 7

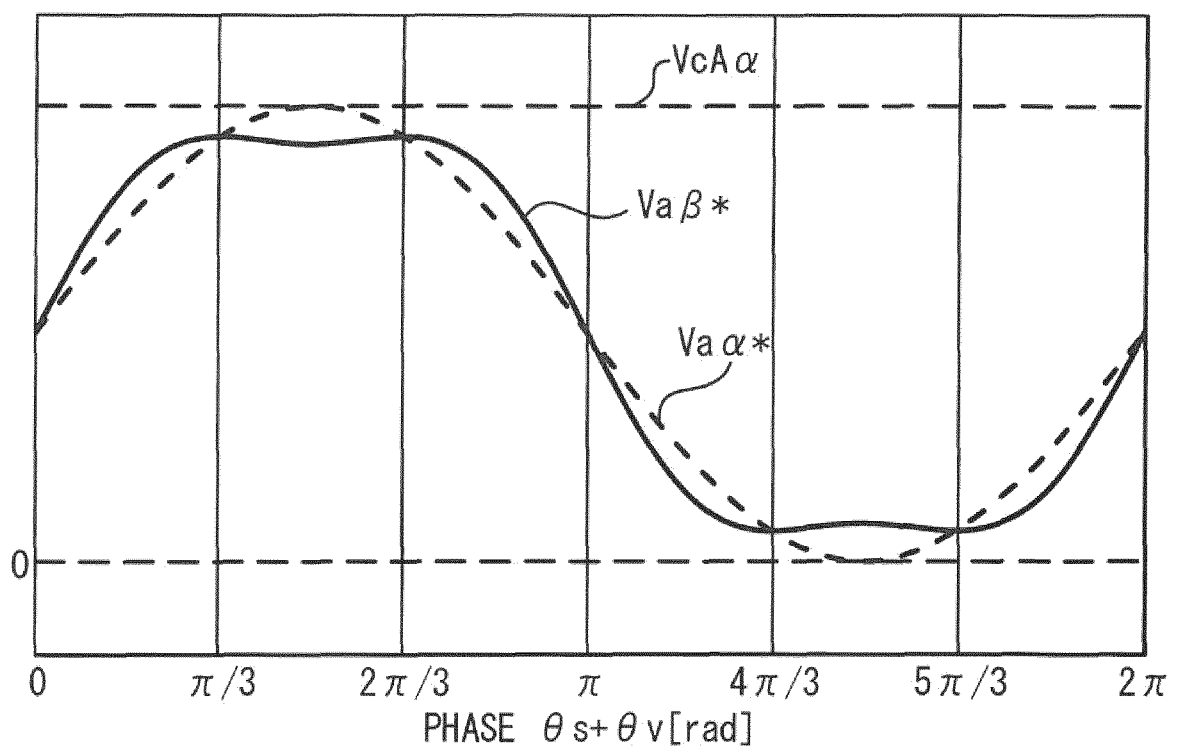


FIG. 8

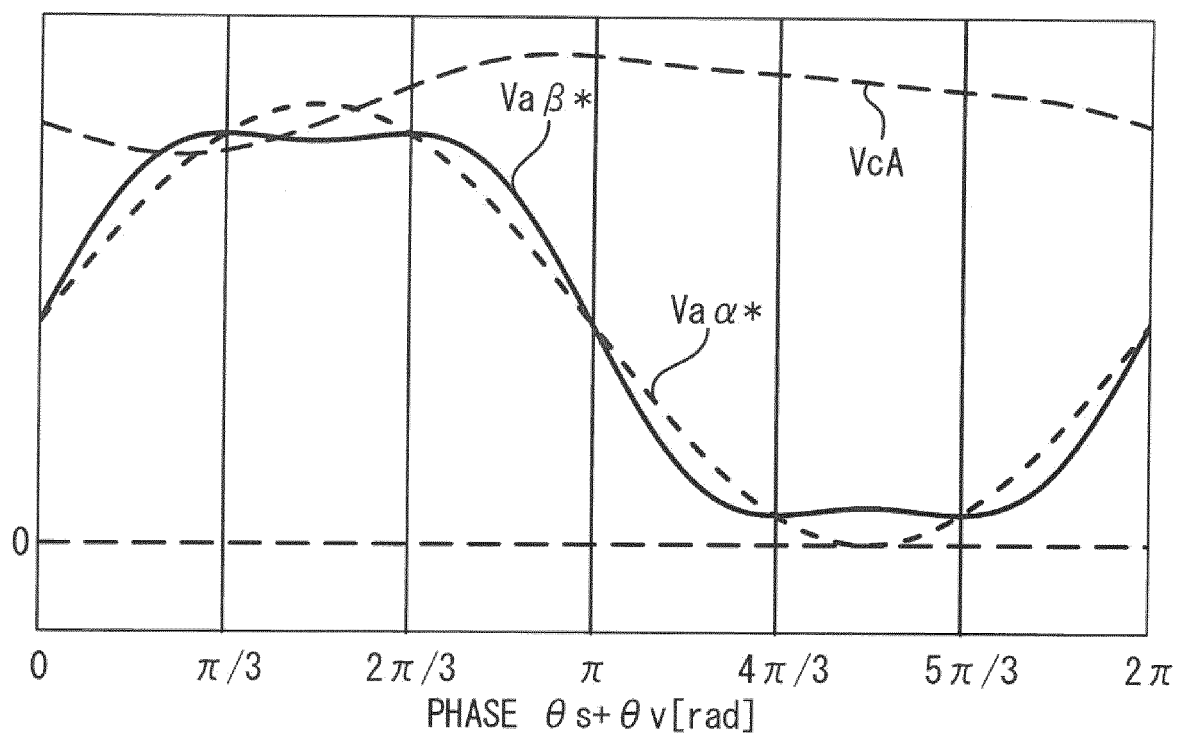


FIG. 9

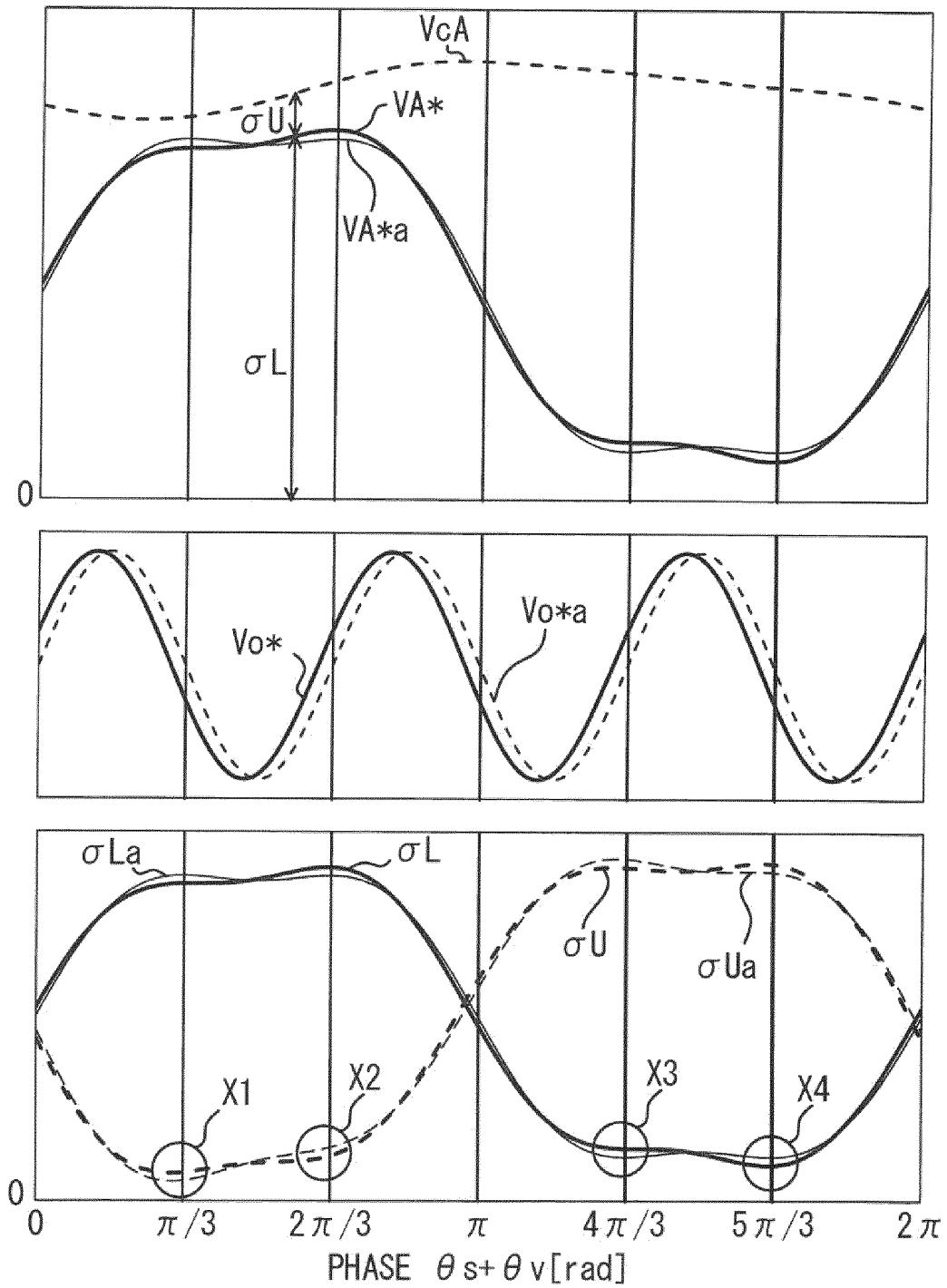


FIG. 10

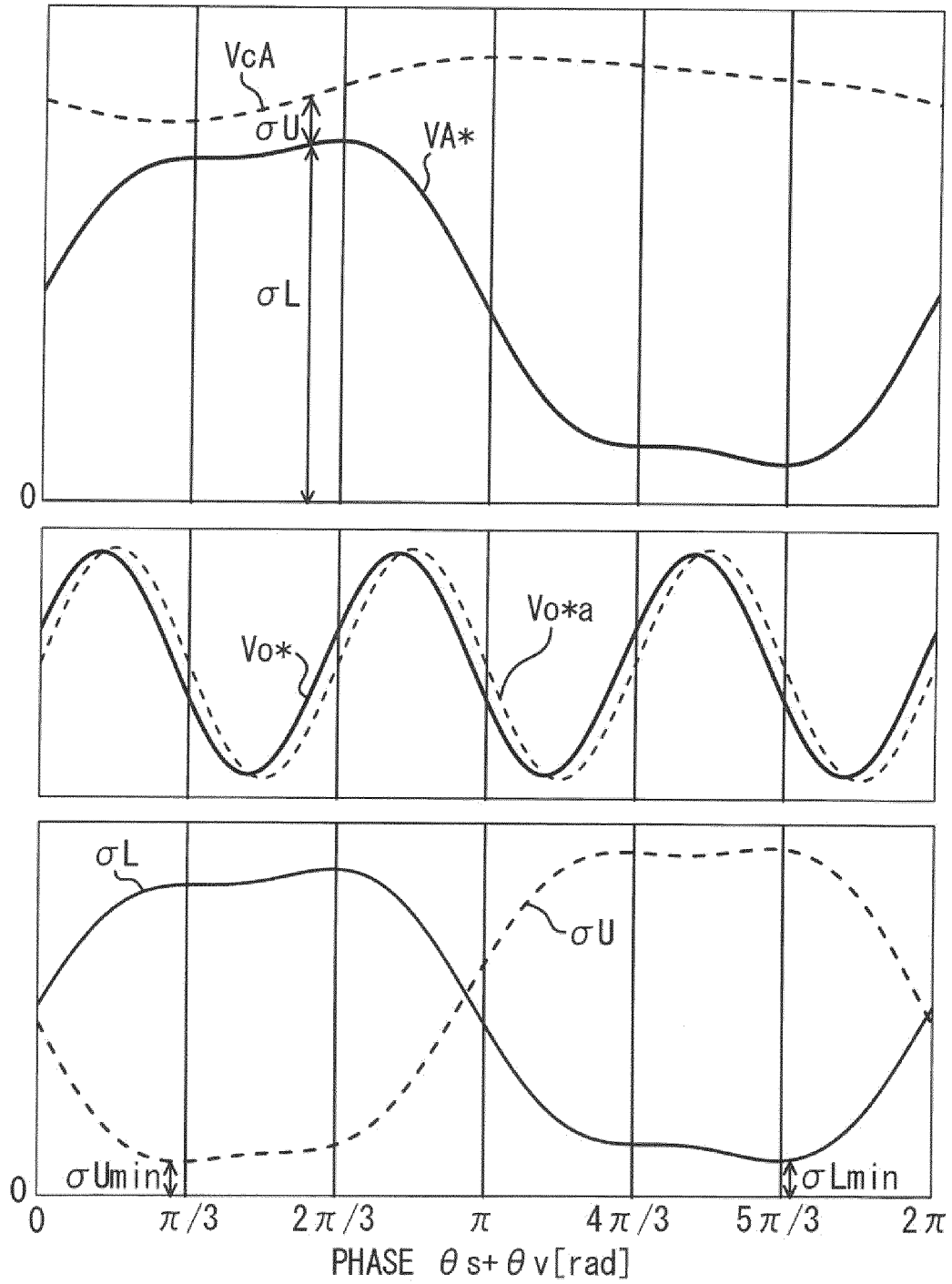


FIG. 11

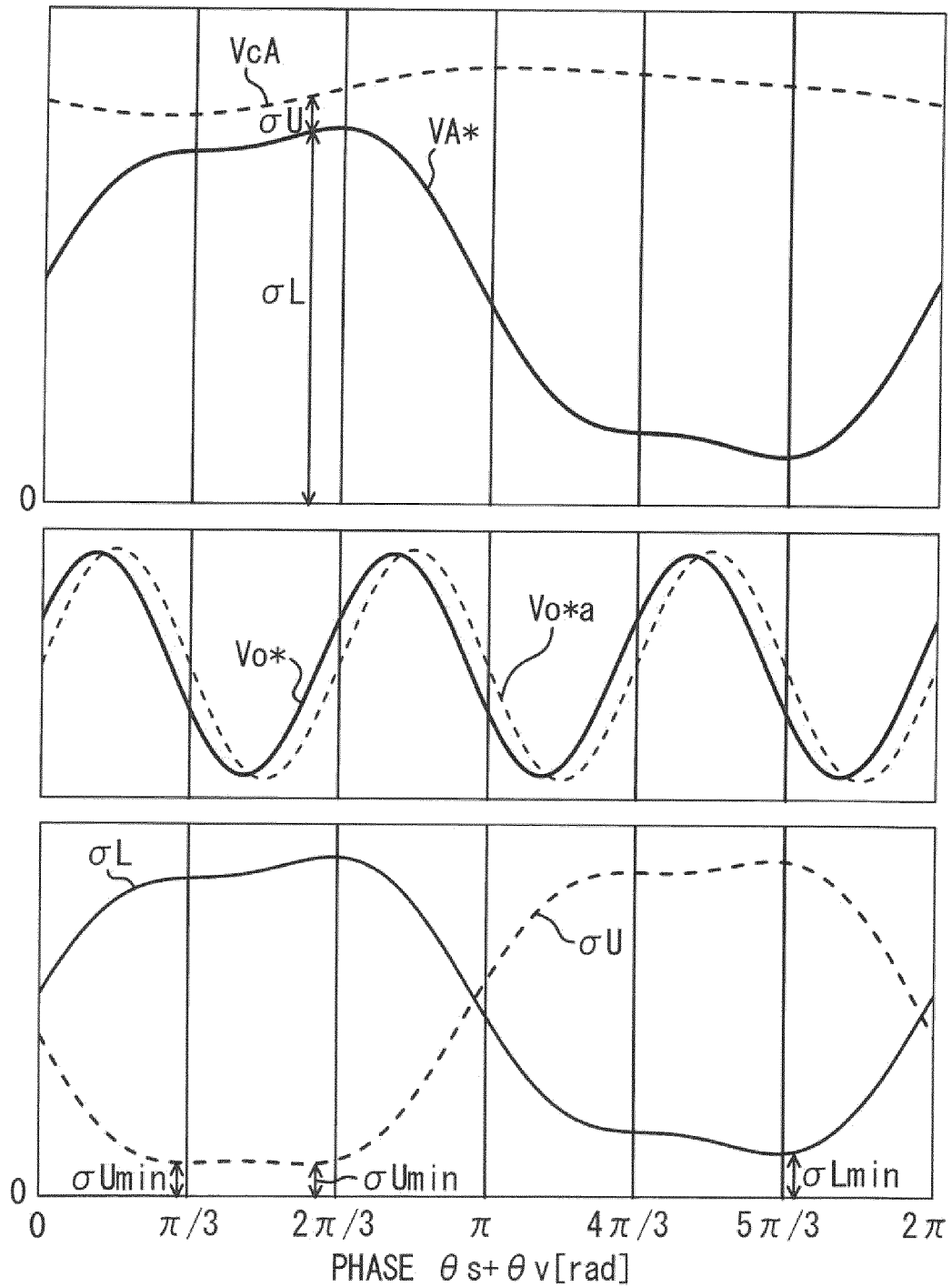


FIG. 12

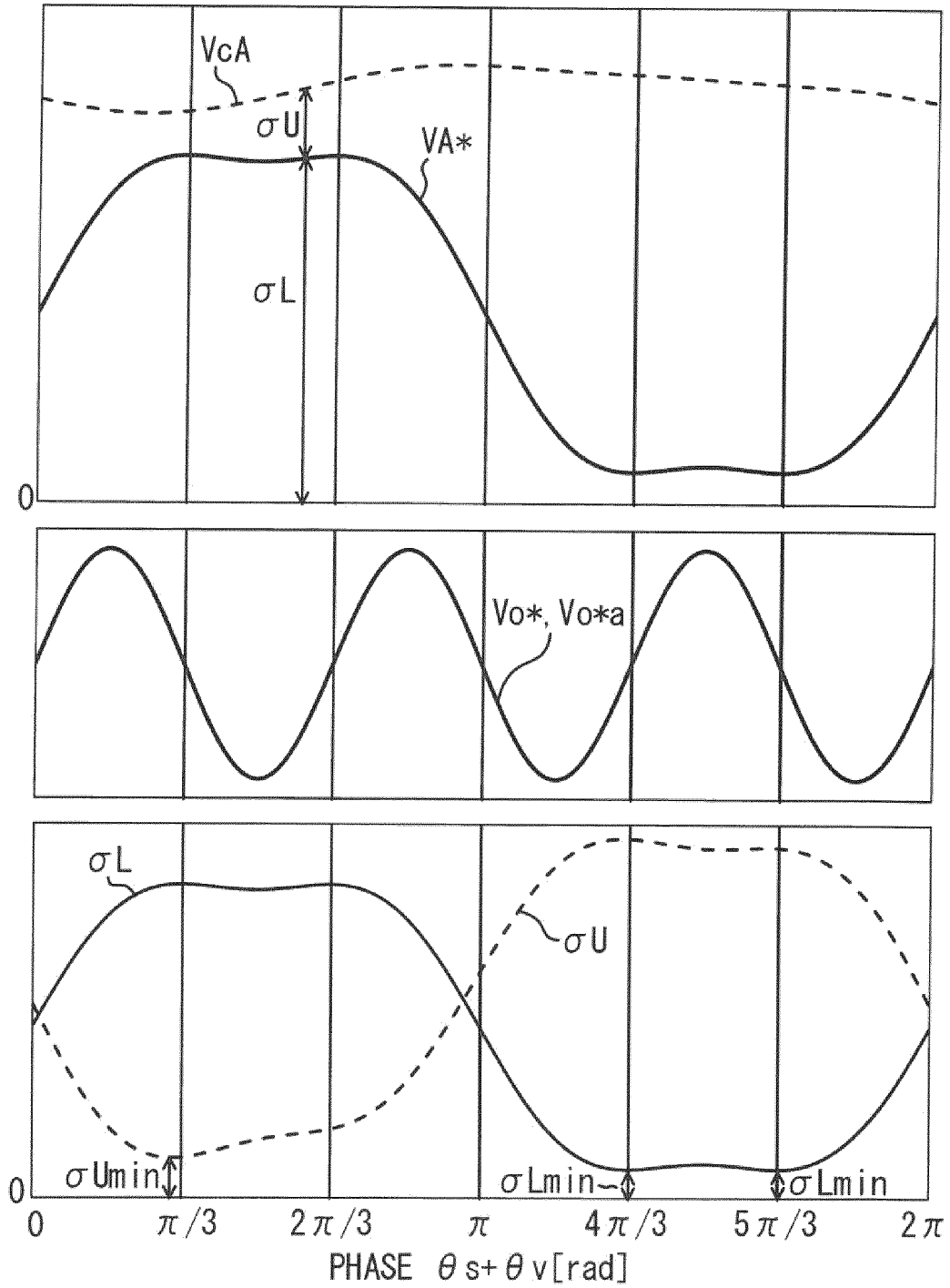


FIG. 13

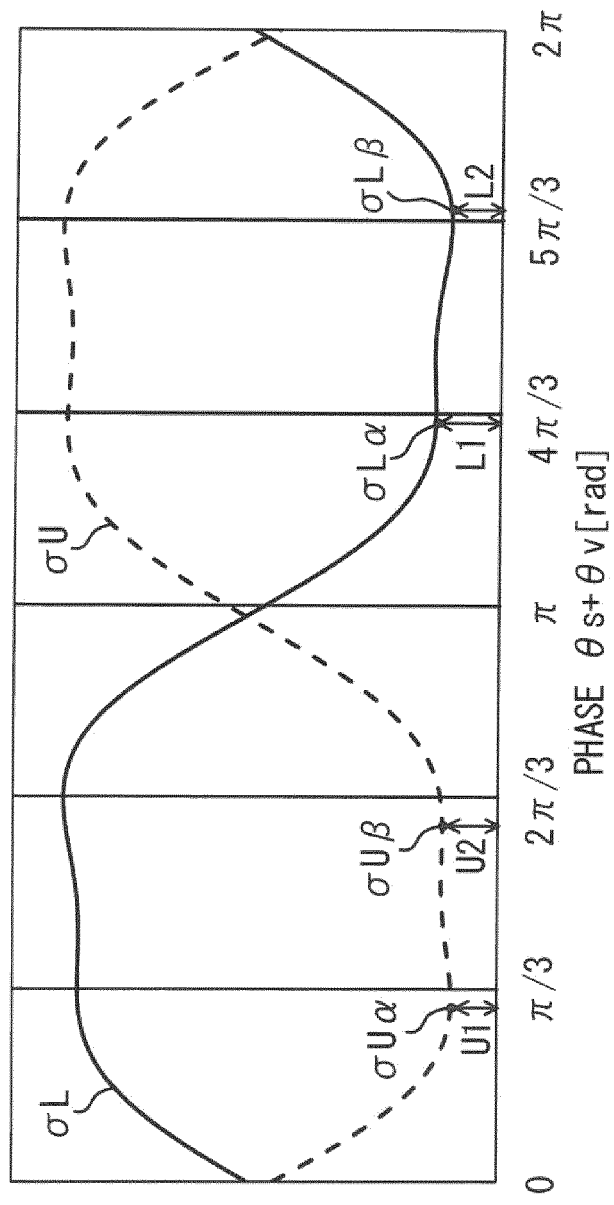


FIG. 14

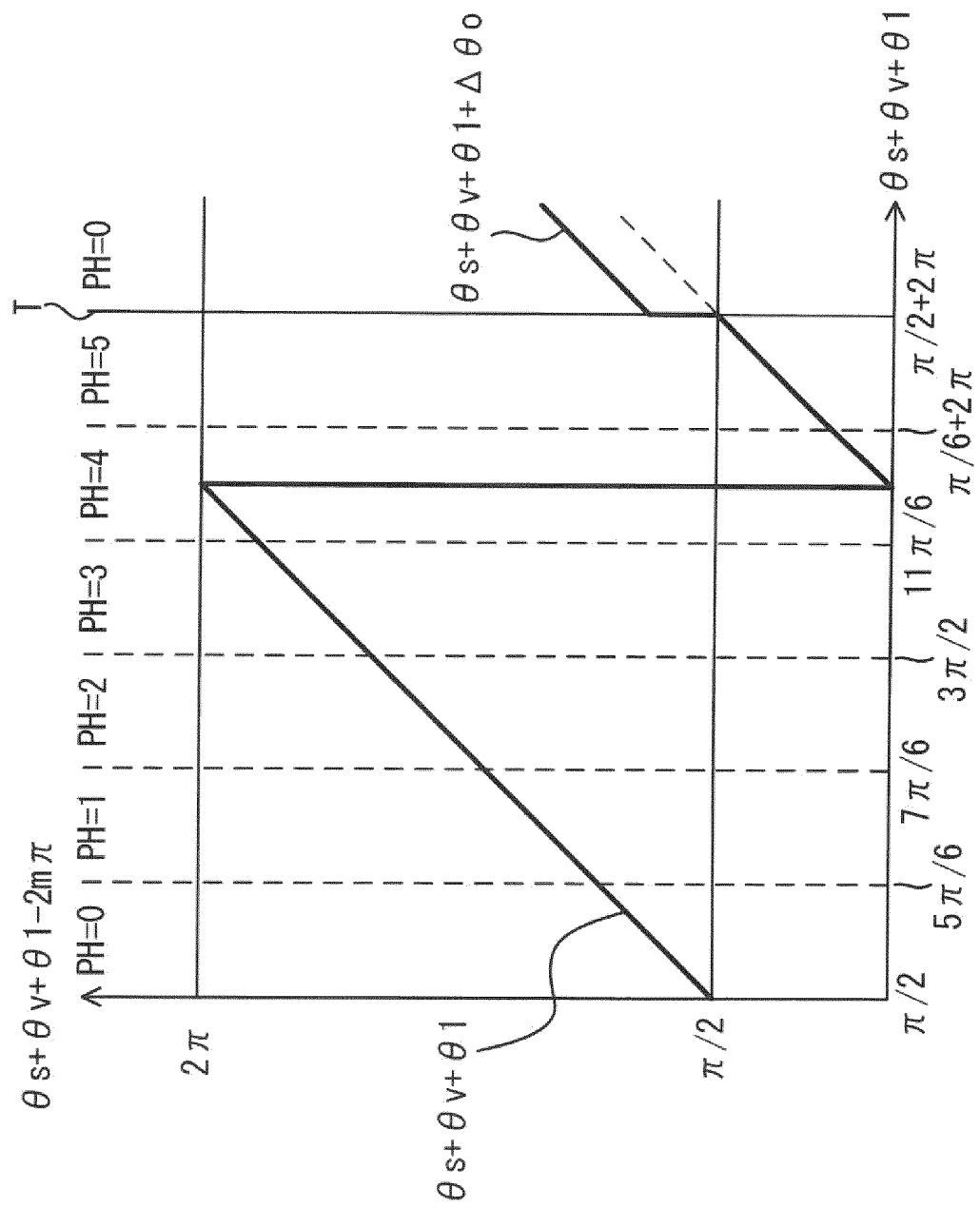
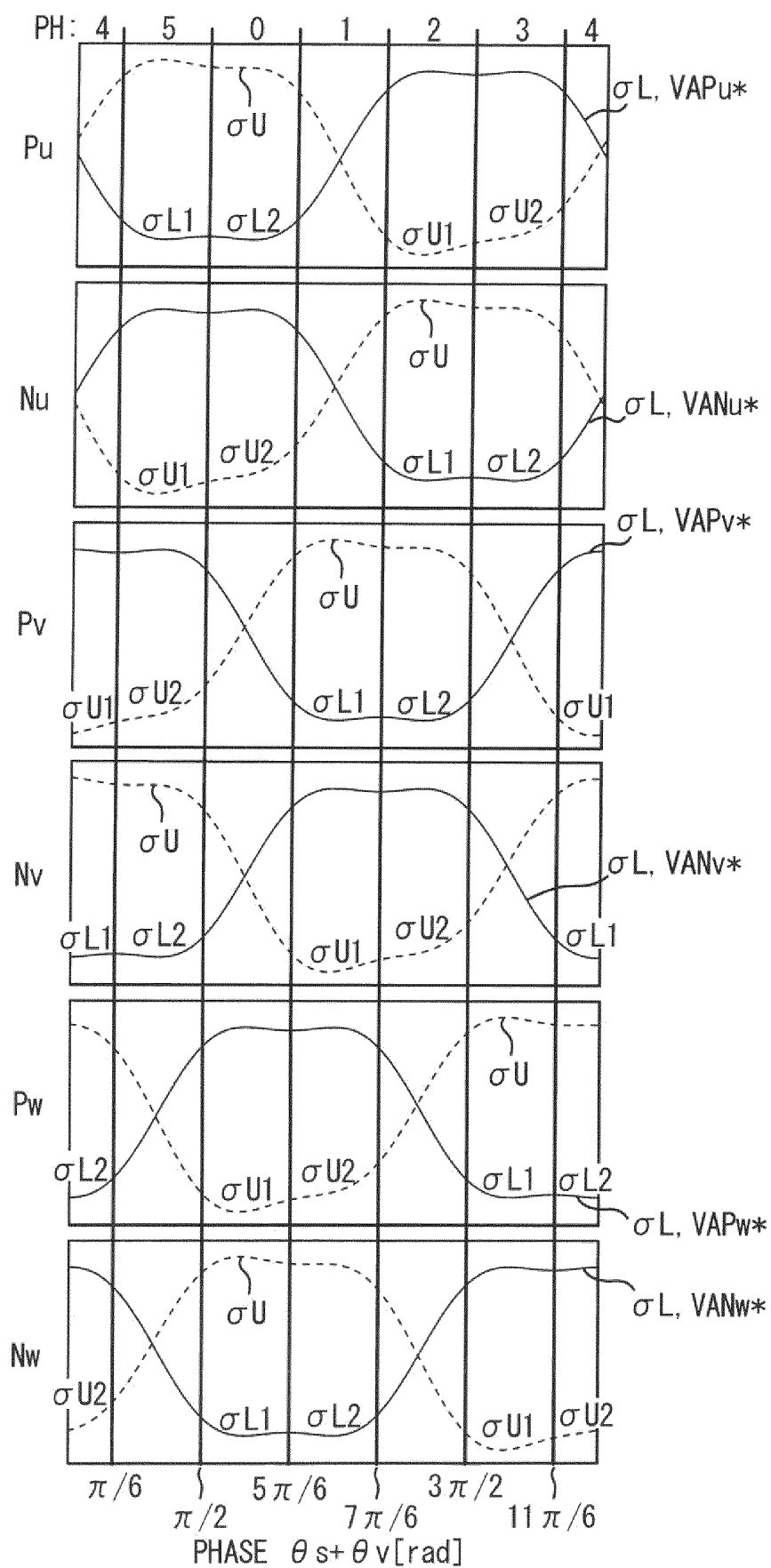


FIG. 15



*FIG. 16*

| PH | $\sigma_{U1}$ | $\sigma_{L1}$ | $\sigma_{U2}$ | $\sigma_{L2}$ |
|----|---------------|---------------|---------------|---------------|
|    | FIRST ARM     | THIRD ARM     | SECOND ARM    | FOURTH ARM    |
| 0  | Pw            | Nw            | Nu            | Pu            |
| 1  | Nv            | Pv            | Pw            | Nw            |
| 2  | Pu            | Nu            | Nv            | Pv            |
| 3  | Nw            | Pw            | Pu            | Nu            |
| 4  | Pv            | Nv            | Nw            | Pw            |
| 5  | Nu            | Pu            | Pv            | Nv            |

FIG. 17

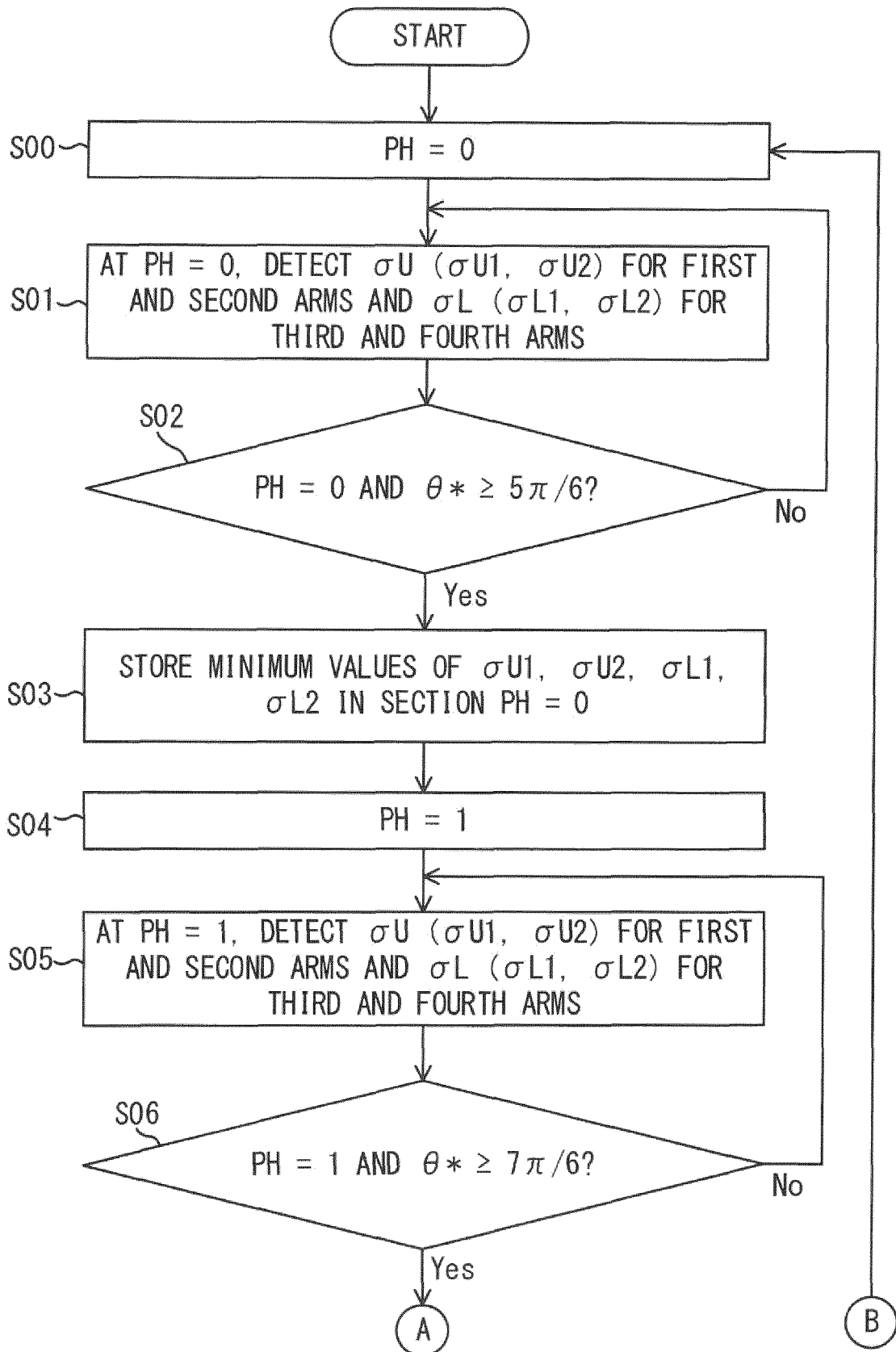


FIG. 18

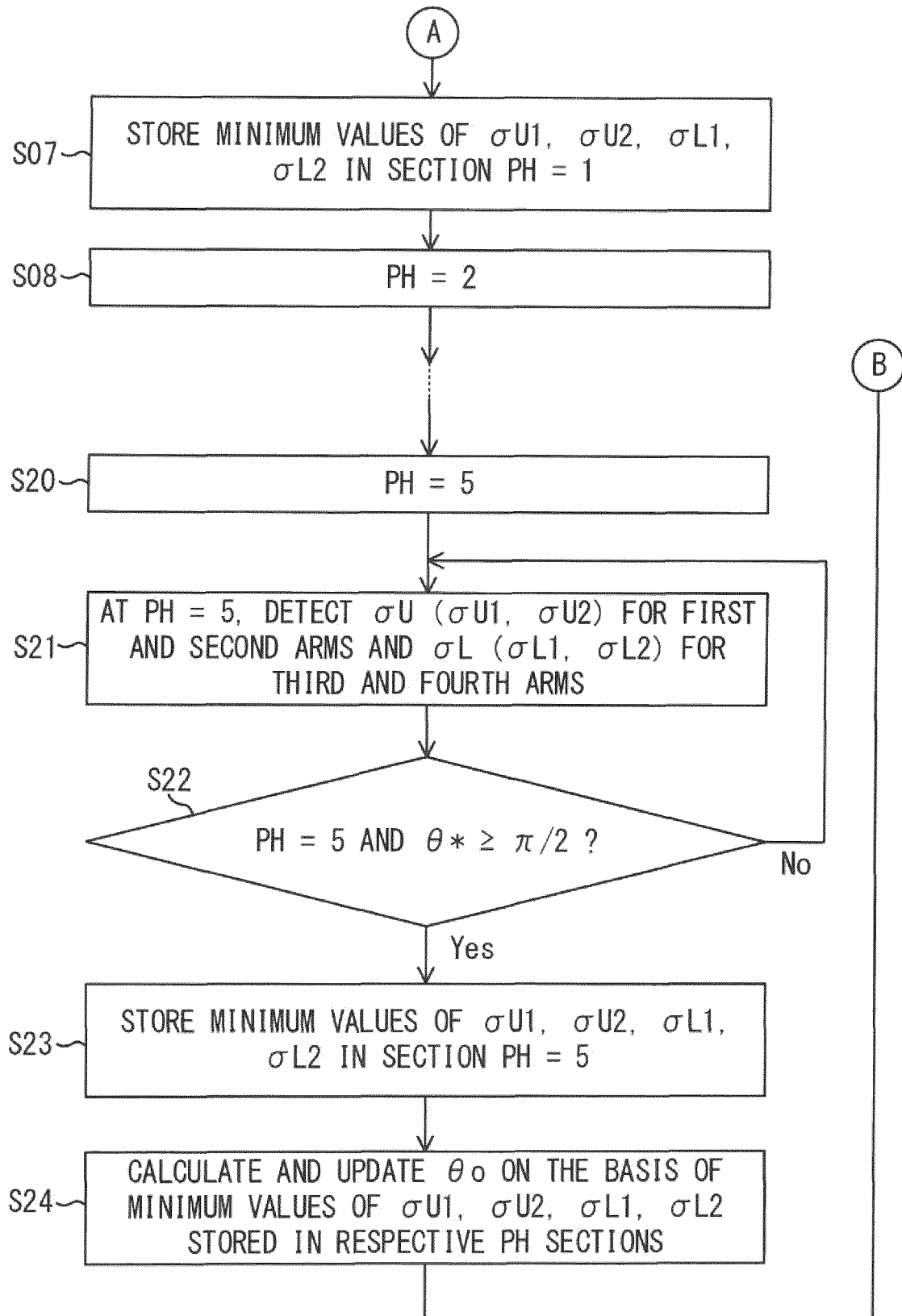
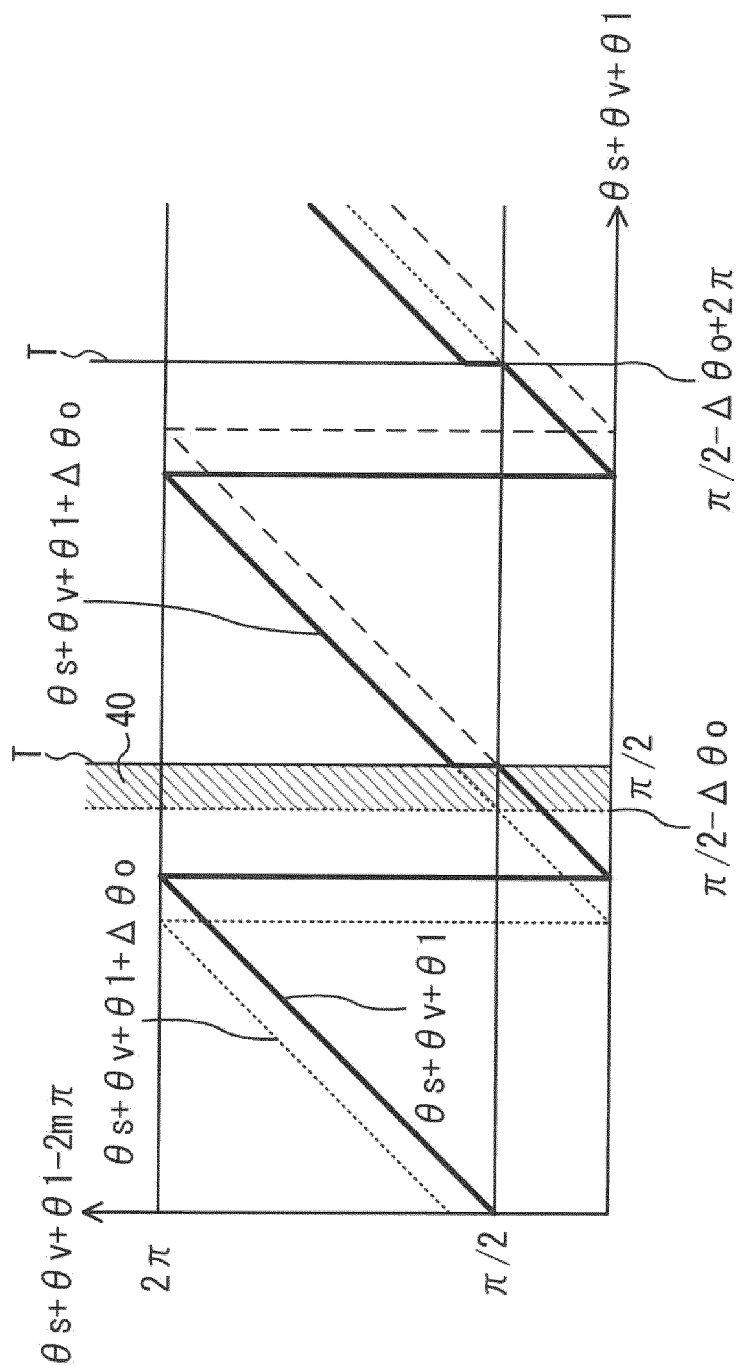


FIG. 19



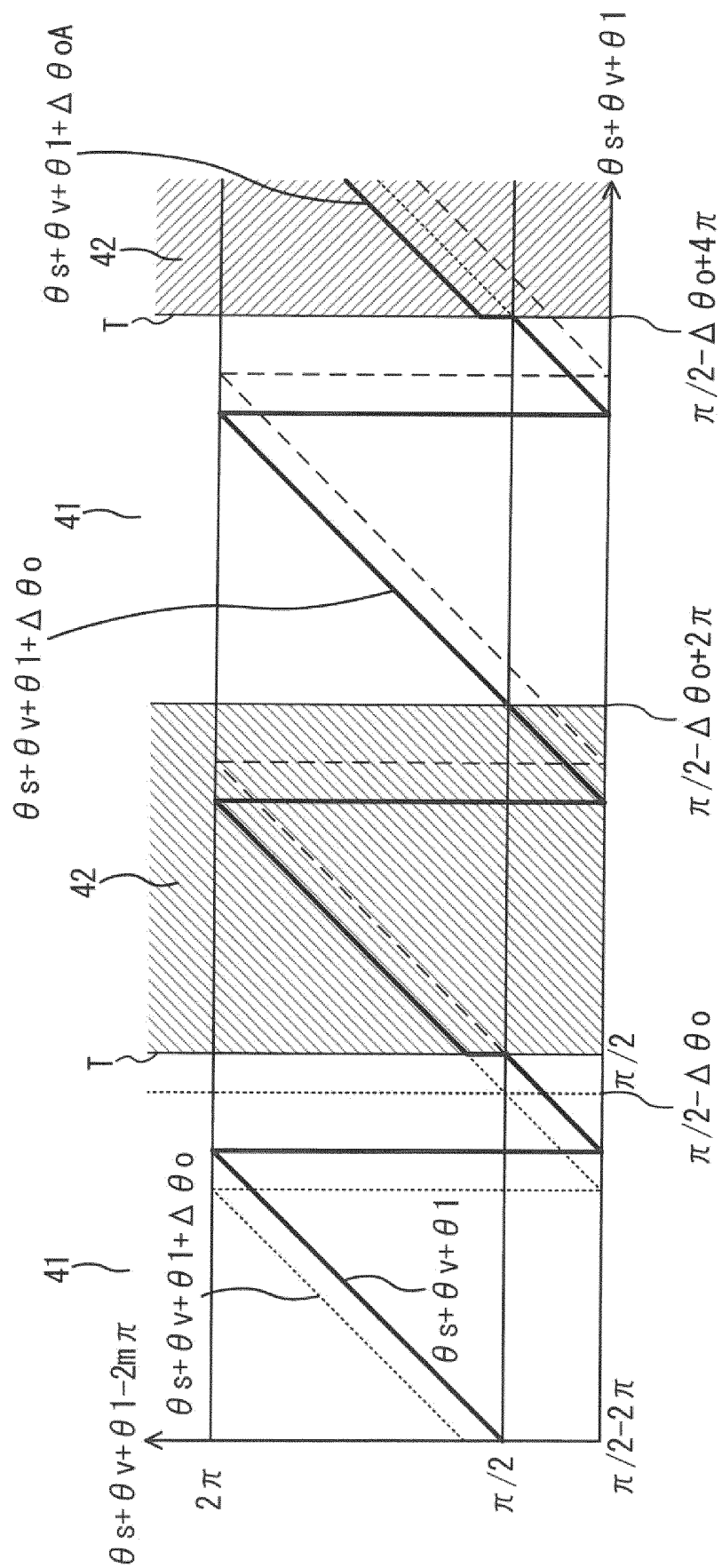
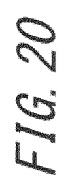
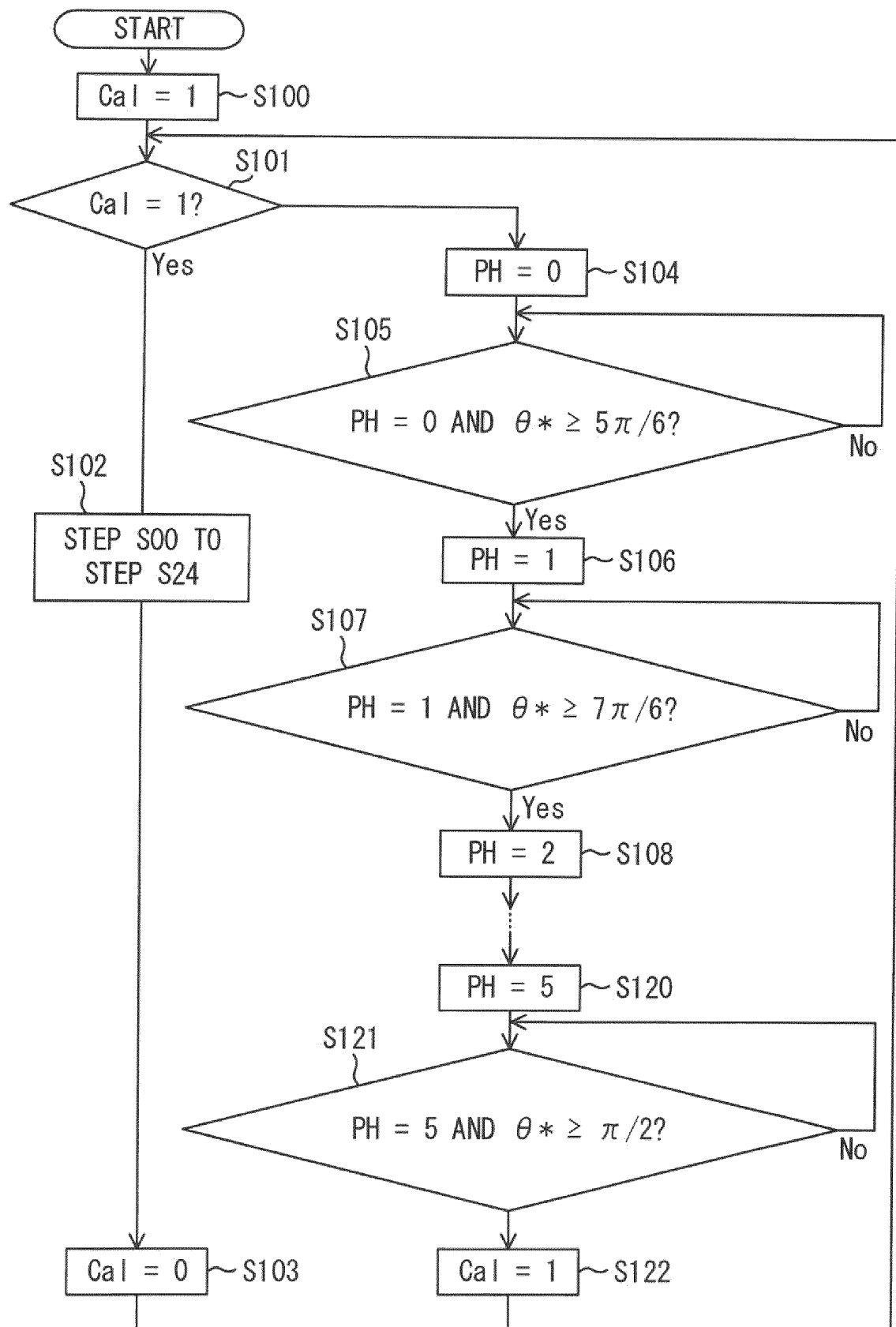


FIG. 21



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2020/028887

## A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. H02M7/49 (2007.01) i

FI: H02M7/49

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl. H02M7/49

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996

Published unexamined utility model applications of Japan 1971-2020

Registered utility model specifications of Japan 1996-2020

Published registered utility model applications of Japan 1994-2020

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                  | Relevant to claim No. |
|-----------|-----------------------------------------------------------------------------------------------------|-----------------------|
| A         | JP 2006-246676 A (THE KANSAI ELECTRIC POWER CO., INC.) 14 September 2006, entire text, all drawings | 1-12                  |
| A         | CN 110233496 A (UNIVERSITY HEFEI TECHNOLOGY) 13 September 2019, entire text, all drawings           | 1-12                  |
| A         | WO 2014/125697 A1 (MITSUBISHI ELECTRIC CORP.) 21 August 2014, entire text, all drawings             | 1-12                  |
| A         | JP 2006-238573 A (MEIDENSHA CORP.) 07 September 2006, entire text, all drawings                     | 1-12                  |
| A         | JP 2015-43660 A (MITSUBISHI ELECTRIC CORP.) 05 March 2015, entire text, all drawings                | 1-12                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

05.10.2020

Date of mailing of the international search report

13.10.2020

Name and mailing address of the ISA/

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku,

Tokyo 100-8915, Japan

Authorized officer

Telephone No.

## INTERNATIONAL SEARCH REPORT

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|----------------------------------------------------|
| International application No.<br>PCT/JP2020/028887 |
|----------------------------------------------------|

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages     | Relevant to claim No. |
|-----------|----------------------------------------------------------------------------------------|-----------------------|
| A         | JP 2013-162658 A (MITSUBISHI ELECTRIC CORP.) 19 August 2013, entire text, all drawings | 1-12                  |

Form PCT/ISA/210 (continuation of second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT  
Information on patent family members

International application No.  
PCT/JP2020/028887

| Patent Documents referred to in<br>the Report | Publication Date | Patent Family                                                            | Publication Date |
|-----------------------------------------------|------------------|--------------------------------------------------------------------------|------------------|
| JP 2006-246676 A                              | 14.09.2006       | (Family: none)                                                           |                  |
| CN 110233496 A                                | 13.09.2019       | (Family: none)                                                           |                  |
| WO 2014/125697 A1                             | 21.08.2014       | US 2015/0357937 A1<br>entire text, all<br>drawings<br>DE 112013006680 T5 |                  |
| JP 2006-238573 A                              | 07.09.2006       | (Family: none)                                                           |                  |
| JP 2015-43660 A                               | 05.03.2015       | (Family: none)                                                           |                  |
| JP 2013-162658 A                              | 19.08.2013       | (Family: none)                                                           |                  |

**REFERENCES CITED IN THE DESCRIPTION**

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- JP 2018014860 A [0005]
- WO 2017046908 A1 [0005]