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(54) **TRANSIENT BOOST CIRCUIT FOR LDO, CHIP SYSTEM AND DEVICE**

(57) A transient performance improvement circuit used for an LDO, a chip system, and a device are configured to reduce a chip area occupied by a capacitor while improving a transient performance of the LDO. The circuit includes an LDO and at least one detection circuit (2) coupled to the LDO, where the LDO is configured to output a first voltage. Each of the at least one detection circuit (2) includes a first capacitor, an amplifier (21), and a second capacitor. The first capacitor is configured to generate a coupling voltage based on a change in the first voltage and couple the coupling voltage to the amplifier (21). The amplifier (21) is configured to amplify the coupling voltage to obtain a second voltage. The second capacitor is configured to couple the second voltage to the LDO. The second voltage is used to regulate the first voltage to maintain constancy of the first voltage.

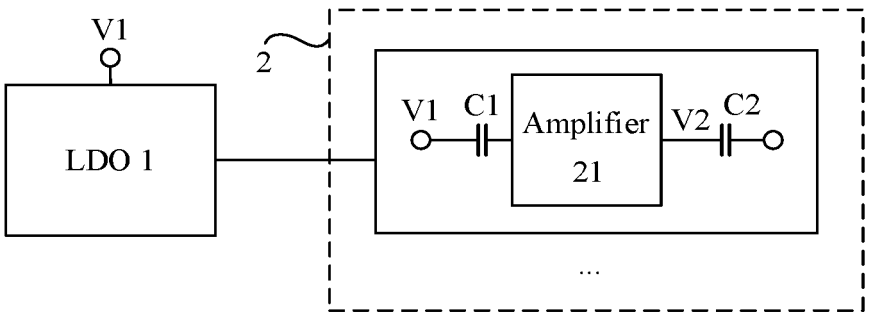

FIG. 2

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Description

TECHNICAL FIELD

[0001] This application relates to the field of electronic technologies, and in particular, to a transient performance improvement circuit used for an LDO, a chip system, and a device.

BACKGROUND

[0002] With rapid development of an internet of things (IOT) system, there is an increasing quantity of application scenarios of IOT chips such as wearable and implantable IOT chips. In the IOT system, some highly sensitive subsystems such as a radio frequency (RF) transceiver, a digital-to-analog converter, an analog-to-digital converter, a high-speed digital circuit, and a phase-locked loop (PLL) have a high transient requirement on a power supply. Therefore, these subsystems are usually powered by some low dropout regulators (LDO) with high transient performance.

[0003] In a conventional technology, an LDO with a large on-chip capacitor or an LDO with an off-chip capacitor (a capacitance of the off-chip capacitor is usually at a μF level) is usually used to supply power to these subsystems. The on-chip capacitor or off-chip capacitor herein can reduce voltage ripples caused by a load transient, ensuring a transient response of the LDO. However, if the LDO with an on-chip capacitor is used, the on-chip capacitor occupies a large chip area, and if the LDO with an off-chip capacitor is used, the off-chip capacitor occupies an additional PCB area.

SUMMARY

[0004] This application provides a transient performance improvement circuit used for an LDO, a chip system, and a device, to reduce a chip area occupied by a capacitor while improving a transient performance of the LDO.

[0005] To achieve the foregoing objectives, the following technical solutions are used in embodiments of this application.

[0006] According to a first aspect, a transient performance improvement circuit used for a low dropout regulator LDO is provided. The circuit includes an LDO and at least one detection circuit coupled to the LDO. The LDO is configured to output a first voltage. The first voltage may be a voltage used to supply power to various subsystems or systems. The first voltage may also be referred to as an output voltage of the LDO. Each of the at least one detection circuit includes a first capacitor, an amplifier, and a second capacitor. The first capacitor is configured to generate a coupling voltage based on a change in the first voltage and couple the coupling voltage to the amplifier. The first capacitor couples the first voltage to the amplifier in an alternating current coupling (AC coupling) manner. The amplifier is configured to amplify the coupling voltage to obtain a second voltage. For example, the amplifier may be a non-inverting amplifier or an inverting amplifier. The second capacitor is configured to couple the second voltage to the LDO. That is, the second capacitor couples the second voltage to the LDO in the alternating current coupling manner to form negative feedback. The second voltage is used to regulate the first voltage to maintain constancy of the first voltage.

[0007] In the technical solution, the first voltage output by the LDO is coupled to the amplifier by the first capacitor, and is amplified by the amplifier. Therefore, while a transient performance of the LDO is improved, the small first capacitor can be used to implement coupling of the first voltage, reducing a chip area occupied by the first capacitor. In addition, the second voltage output by the amplifier is coupled to the LDO by the second capacitor, so that the second voltage does not act directly on an inherent loop of the LDO, avoiding destroying a direct current characteristic of the LDO, and ensuring stability of the loop of the LDO. Moreover, the amplifier is coupled to the LDO by using the first capacitor and the second capacitor. In this way, a bias of the amplifier can be separated from a direct current component of the first voltage, effectively reducing difficulty and complexity of biasing in the amplifier. That is, requirements such as offset and matching do not need to be considered during design of the amplifier, further reducing an area of a chip and implementing low power consumption and high energy efficiency.

[0008] In a possible implementation of the first aspect, the amplifier includes a first transistor, a second transistor, a third transistor, and a first resistor. One electrode of the first transistor, one electrode of the second transistor, and one terminal of the first resistor are coupled and serve as an output terminal of the amplifier. A control terminal of the first transistor, a control terminal of the second transistor, and the other terminal of the first resistor are coupled and serve as an input terminal of the amplifier. The other electrode of the second transistor and one electrode of the third transistor are coupled. One of the other electrode of the first transistor and the other electrode of the third transistor is coupled to a power terminal, and the other is coupled to a ground terminal. A control terminal of the third transistor is coupled to a bias voltage terminal. Optionally, the first transistor is an NMOS transistor, and the second transistor and the third transistor are both PMOS transistors. The one electrode is a drain, the other electrode is a source, and the control terminal is a gate. In the foregoing possible implementation, the amplifier is a phase inverter based amplifier. A transimpedance of the amplifier is a sum of a transimpedance of the first transistor and a transimpedance of the second transistor. Under same power consumption, the transimpedance of the amplifier is twice that of a common amplifier, effectively improving energy efficiency. The third transistor is configured to supply a bias current to the amplifier, to prevent power consumption of the am-

plifier from changing with a voltage at the power terminal and a process corner. In addition, the amplifier is coupled to the LDO by using the first capacitor and the second capacitor. This allows a direct current operating point of the amplifier to be separately biased by using only the first resistor, effectively reducing a matching requirement of the amplifier.

[0009] In a possible implementation of the first aspect, the at least one detection circuit includes a first detection circuit. The first detection circuit further includes a compensation circuit coupled between the second capacitor and the LDO. The compensation circuit is configured to regulate the first voltage based on the second voltage to maintain constancy of the first voltage. In the foregoing possible implementation, by using the compensation circuit, the first voltage output by the LDO can be quickly and effectively compensated for based on the second voltage, improving transient performance of the LDO.

[0010] In a possible implementation of the first aspect, the compensation circuit includes a fourth transistor, a fifth transistor, a sixth transistor, a second resistor, and a third resistor. One electrode of the fourth transistor, one terminal of the third resistor, and one electrode of the sixth transistor are coupled to a first node. The other electrode of the fourth transistor, a control terminal of the fifth transistor, and one terminal of the second resistor are coupled and serve as an input terminal of the compensation circuit. One electrode of the fifth transistor and the other terminal of the second resistor are coupled to a second node. The other electrode of the fifth transistor, a control terminal of the sixth transistor, and the other terminal of the third resistor are coupled. The other electrode of the sixth transistor serves as an output terminal of the compensation circuit. One of the first node and the second node is coupled to the power terminal, and the other is coupled to the ground terminal. Optionally, the fifth transistor is an NMOS transistor, and the fourth transistor and the sixth transistor are both PMOS transistors. Alternatively, the fifth transistor is a PMOS transistor, and the fourth transistor and the sixth transistor are both NMOS transistors. The one electrode is a drain, the other electrode is a source, and the control terminal is a gate. In the foregoing possible implementation, the provided compensation circuit is simple and effective, further reducing the area of the chip while improving transient performance of the LDO.

[0011] In a possible implementation of the first aspect, the LDO has an output terminal, and the output terminal of the compensation circuit and the output terminal of the LDO are coupled. In the foregoing possible implementation, the compensation circuit provides feedback to the output terminal of the LDO to compensate for the first voltage output by the LDO, improving transient performance of the LDO.

[0012] In a possible implementation of the first aspect, the compensation circuit includes a fourth transistor, a fifth transistor, and a second resistor. One electrode of the fourth transistor is coupled to a first node. The other electrode of the fourth transistor, a control terminal of the fifth transistor, and one terminal of the second resistor are coupled and serve as an input terminal of the compensation circuit. One electrode of the fifth transistor and the other terminal of the second resistor are coupled to a second node. The other electrode of the fifth transistor serves as an output terminal of the compensation circuit. One of the first node and the second node is coupled to the power terminal, and the other is coupled to the ground terminal. Optionally, the fourth transistor is a PMOS transistor, and the fifth transistor is an NMOS transistor. The one electrode is a drain, the other electrode is a source, and the control terminal is a gate. In the foregoing possible implementation, the provided compensation circuit is simple and effective, further reducing the area of the chip while improving transient performance of the LDO.

[0013] In a possible implementation of the first aspect, the LDO includes an operational amplifier, a voltage regulating transistor, and a sampling circuit. An output terminal of the operational amplifier and a control terminal of the voltage regulating transistor are coupled. One electrode of the voltage regulating transistor is coupled to the power terminal. The other electrode of the voltage regulating transistor and an input terminal of the sampling circuit are coupled and serve as an output terminal of the LDO. An output terminal of the sampling circuit and a non-inverting input terminal of the operational amplifier are coupled. An inverting input terminal of the operational amplifier is configured to receive a reference voltage. The output terminal of the compensation circuit and the control terminal of the voltage regulating transistor are coupled. In the foregoing possible implementation, the compensation circuit provides feedback to the control terminal of the voltage regulating transistor to compensate for the first voltage output by the LDO, improving transient performance of the LDO.

[0014] In a possible implementation of the first aspect, the LDO includes a seventh transistor, an eighth transistor, a ninth transistor, a tenth transistor, an eleventh transistor, and a fourth resistor. One electrode of the seventh transistor and one electrode of the eighth transistor are both coupled to the power terminal. The other electrode of the seventh transistor and one electrode of the ninth transistor are coupled and serve as the output terminal of the LDO. The other electrode of the eighth transistor, one electrode of the tenth transistor, and a control terminal of the seventh transistor are coupled. The other electrode of the ninth transistor, the other electrode of the tenth transistor, and one electrode of the eleventh transistor are coupled. The other electrode of the eleventh transistor is coupled to the ground terminal. A control terminal of the eleventh transistor and one terminal of the fourth resistor are coupled. The other terminal of the fourth resistor is connected to a bias voltage terminal. Optionally, the seventh transistor, the eighth transistor, and the ninth transistor are all PMOS transistors, and the tenth transistor and the eleventh transistor are both NMOS transistors. The one electrodes of the seventh

transistor to the ninth transistor are sources, and the other electrodes of the seventh transistor to the ninth transistor are drains. The one electrodes of the tenth transistor and the eleventh transistor are drains, and the other electrodes of the tenth transistor and the eleventh transistor are sources. The control terminals are gates. In the foregoing possible implementation, an FVF LDO is provided. By using at least one detection circuit coupled to the FVF LDO, a chip area occupied by a capacitor can be reduced while a transient performance of the LDO is improved.

[0015] In a possible implementation of the first aspect, the at least one detection circuit further includes a second detection circuit. A second capacitor in the second detection circuit is coupled between an output terminal of an amplifier and a control terminal of the eighth transistor. In the foregoing possible implementation, the detection circuit provides feedback to the control terminal of the eighth transistor to compensate for the first voltage output by the LDO, improving transient performance of the LDO.

[0016] In a possible implementation of the first aspect, the at least one detection circuit further includes a third detection circuit, and a second capacitor in the third detection circuit is coupled between an output terminal of an amplifier and a control terminal of the tenth transistor. In the foregoing possible implementation, the detection circuit provides feedback to the control terminal of the tenth transistor to compensate for the first voltage output by the LDO, improving transient performance of the LDO.

[0017] In a possible implementation of the first aspect, the at least one detection circuit further includes a fourth detection circuit, and a second capacitor in the fourth detection circuit is coupled between an output terminal of an amplifier and the control terminal of the eleventh transistor. In the foregoing possible implementation, the detection circuit provides feedback to the control terminal of the eleventh transistor to compensate for the first voltage output by the LDO, improving transient performance of the LDO.

[0018] According to a second aspect, a chip system is provided. The chip system includes a load circuit and the transient performance improvement circuit used for a low dropout regulator LDO as provided in any one of the first aspect or the possible implementations of the first aspect. The transient performance improvement circuit includes an LDO and at least one detection circuit coupled to the LDO. The LDO is configured to supply power to the load circuit. The at least one detection circuit is configured to improve a transient performance of the LDO.

[0019] According to a third aspect, a device is provided. The device includes a load circuit and a circuit board. The circuit board includes the transient performance improvement circuit used for a low dropout regulator LDO as provided in any one of the first aspect or the possible implementations of the first aspect. The transient performance improvement circuit includes an LDO and at least one detection circuit coupled to the LDO. The LDO is configured to supply power to the load circuit. The at least one detection circuit is configured to improve a transient performance of the LDO.

[0020] It can be understood that any chip system and device provided above include the transient performance improvement circuit used for an LDO provided above. Therefore, for beneficial effects that can be achieved by the chip system and device, refer to beneficial effects of the transient performance improvement circuit used for an LDO provided above. Details are not described herein again.

BRIEF DESCRIPTION OF DRAWINGS

[0021]

FIG. 1 is a schematic diagram of a structure of an LDO according to an embodiment of this application;

FIG. 2 is a schematic diagram of a structure of a transient performance improvement circuit used for an LDO according to an embodiment of this application;

FIG. 3 is a schematic diagram of a structure of an amplifier according to an embodiment of this application;

FIG. 4 is a schematic diagram of a structure of another transient performance improvement circuit used for an LDO according to an embodiment of this application;

FIG. 5 is a schematic diagram of a structure of still another transient performance improvement circuit used for an LDO according to an embodiment of this application;

FIG. 6 is a schematic diagram of a structure of an operational amplifier according to an embodiment of this application;

FIG. 7 is a schematic diagram of a structure of an FVF LDO according to an embodiment of this application;

FIG. 8 is a schematic diagram of a structure of another transient performance improvement circuit used for an LDO according to an embodiment of this application;

FIG. 9 is a schematic diagram of a structure of still another transient performance improvement circuit used for an LDO according to an embodiment of this application;

FIG. 10 is a schematic diagram of a structure of another transient performance improvement circuit used for an LDO according to an embodiment of this application; and

FIG. 11 is a schematic diagram of a structure of still another transient performance improvement circuit used for an LDO according to an embodiment of this application.

DESCRIPTION OF EMBODIMENTS

[0022] The following describes production and use of embodiments in detail. However, it should be understood

that many applicable invention concepts provided in this application may be implemented in a plurality of specific environments. The described specific embodiments describe only specific manners in which this specification and this technology are implemented are used, and are not intended to limit a scope of this application.

[0023] Unless otherwise defined, all scientific and technological terms used in this specification have same meanings as those commonly known to a person of ordinary skill in the art.

[0024] Circuits or other components may be described or referred to as "configured to" perform one or more tasks. In this case, "configured to" is used to imply a structure by indicating that a circuit/component includes a structure (for example, a circuit system) that performs one or more tasks during operation. Therefore, even when a specified circuit/component is currently inoperable (for example, not turned on), the circuit/component may also be referred to as being configured to perform the task. The circuit/component used with the phrase "configured to" includes hardware, for example, a circuit performing an operation.

[0025] The following describes technical solutions in embodiments of this application with reference to the accompanying drawings in embodiments of this application. In this application, "at least one" means one or more, and "a plurality of" means two or more. "And/or" describes an association relationship between associated objects, and represents that three relationships may exist. For example, A and/or B may represent the following cases: Only A exists, both A and B exist, and only B exists, where A and B may be singular or plural. The character "/" usually indicates an "or" relationship between associated objects. "At least one of the following items (pieces)" or a similar expression thereof refers to any combination of these items, including any combination of singular items (pieces) or plural items (pieces). For example, at least one of a, b, or c may represent a, b, c, a and b, a and c, b and c, or a, b, and c, where each of a, b, or c may represent a single item or a plurality of items. In addition, in embodiments of this application, words such as "first" and "second" do not limit a quantity and an order.

[0026] It should be noted that, in embodiments of this application, the term such as "example" or "for example" is used to represent giving an example, an illustration, or descriptions. Any embodiment or design described as an "example" or "for example" in embodiments of this application should not be explained as being more preferred or having more advantages than another embodiment or design. Exactly, use of the word "example", "for example", or the like is intended to present a related concept in a specific manner.

[0027] In addition, a transistor in embodiments of this application may be a metal oxide semiconductor (MOS) field-effect transistor (which may be referred to as a MOS transistor for short). In embodiments of this application, a control terminal of a transistor may be a gate of the transistor. In a possible embodiment, one electrode of the transistor may be a source, and the other electrode of the transistor may be a drain. In another possible embodiment, one electrode of the transistor may be a drain, and the other electrode of the transistor may be a source.

[0028] The technical solutions in this application may be applied to various subsystems or systems powered by a low dropout regulator (LDO). For example, the technical solutions in this application may be applied to a radio frequency (RF) transceiver, a digital-to-analog converter (DAC), an analog-to-digital converter (ADC), a high-speed digital circuit (for example, a system-on-a-chip SoC), a phase-locked loop (PLL), and the like that are powered by an LDO.

[0029] FIG. 1 is a schematic diagram of a circuit of a general-purpose LDO according to an embodiment of this application. The LDO may include an operational amplifier A0, a voltage regulating transistor M0, a sampling circuit, and a load capacitor C0. The sampling circuit may include a resistor Ra and a resistor Rb. For example, the voltage regulating transistor M0 is a PMOS transistor. An output terminal of the operational amplifier A0 and a control terminal (that is, a gate of the PMOS transistor) of the voltage regulating transistor M0 are coupled. One electrode (that is, a source of the PMOS) of the voltage regulating transistor M0 is coupled to a voltage input terminal (VDD). The other electrode (that is, a drain of the PMOS) of the voltage regulating transistor M0 and an input terminal of the sampling circuit are coupled and serve as an output terminal of the LDO. An output terminal of the sampling circuit and a non-inverting input terminal of the operational amplifier A0 are coupled. An inverting input terminal of the operational amplifier A0 is configured to receive a reference voltage V_{REF}. One terminal of the load capacitor C0 is coupled to the output terminal of the LDO, and the other terminal of the load capacitor C0 is coupled to a ground terminal (GND).

[0030] When the LDO is operating, the sampling circuit samples an output voltage V_{OUT} by using the resistor Ra and the resistor Rb, and feeds the sampled voltage back to the non-inverting input terminal of the operational amplifier. The operational amplifier compares the collected voltage with the reference voltage V_{REF} received by the inverting input terminal, and amplifies the collected voltage. The amplified voltage is fed back to the input terminal through the gate of the voltage regulating transistor M0. Dynamic regulated output is performed by using a forward voltage drop of the voltage regulating transistor M0.

[0031] When the LDO is powered on, a load of a following stage changes drastically, or the like, the output voltage V_{OUT} of the LDO overshoots or undershoots, resulting in poor transient performance of the LDO. Overshooting may mean that a peak value or valley value of an actual output voltage is greater than a specified output voltage range. Undershooting may mean that a peak value or valley value of an actual output voltage is less than a specified output voltage range. Currently, to ensure that an LDO has a good transient response, an LDO with

a large on-chip capacitor or an LDO with an off-chip capacitor is usually used. However, if the LDO with an on-chip capacitor is used, the on-chip capacitor occupies a large chip area, and if the LDO with an off-chip capacitor is used, the off-chip capacitor occupies an additional PCB area. Based on this, an embodiment of this application provides a transient performance improvement circuit used for an LDO. A principle of the transient performance improvement circuit used for an LDO is that at least one detection circuit coupled to the LDO improves transient performance of the LDO. The at least one detection circuit may provide feedback to any node (for example, an output node or an internal node of the LDO) in the LDO, provided that negative feedback is formed. The circuit may be configured to reduce an area occupied by a capacitor in the LDO while improving transient performance of the LDO, reducing an area of a chip on which the LDO is located.

[0032] FIG. 2 is a schematic diagram of a structure of a transient performance improvement circuit used for an LDO according to an embodiment of this application. With reference to FIG. 2, the circuit includes an LDO 1 and at least one detection circuit 2 coupled to the LDO 1. The at least one detection circuit 2 may include one or more detection circuits.

[0033] The LDO 1 is configured to output a first voltage V1. The first voltage V1 may be a voltage used to supply power to various subsystems or systems. The first voltage V1 may also be referred to as an output voltage of the LDO 1. For example, the LDO 1 is the LDO shown in FIG. 1. The first voltage V1 is the output voltage V_{OUT} shown in FIG. 1.

[0034] In addition, each of the at least one detection circuit 2 includes a first capacitor C1, an amplifier 21, and a second capacitor C2. The first capacitor C1 is configured to generate a coupling voltage based on a change in the first voltage V1 and couple the coupling voltage to the amplifier 21. That is, the first capacitor C1 couples the first voltage V1 to the amplifier 21 in an alternating current coupling (AC coupling) manner. A direct current component in the first voltage V1 may be filtered out by the first capacitor C1. The amplifier 21 is configured to amplify the coupling voltage to obtain a second voltage V2. That is, the second voltage V2 is a voltage obtained after the coupling voltage is amplified. For example, the amplifier 21 may be a non-inverting amplifier or an inverting amplifier, and is configured to amplify the coupling voltage to obtain the second voltage V2. The second capacitor C2 is configured to couple the second voltage V2 to the LDO 1. That is, the second capacitor C2 couples the second voltage V2 to the LDO 1 in the alternating current coupling manner. The second voltage V2 is used to regulate the first voltage V1 to maintain constancy of the first voltage V1.

[0035] It can be understood that, that the second capacitor C2 is configured to couple the second voltage V2 to the LDO 1 may include: The second capacitor C2 directly couples the second voltage V2 to the LDO 1, to maintain constancy of the first voltage V1 by regulating the first voltage V1 inside the LDO 1; or the second capacitor C2 indirectly couples the second voltage V2 to the LDO 1, for example, the second capacitor C2 couples the second voltage V2 to the LDO 1 by using an intermediate circuit. The intermediate circuit may be configured to regulate the first voltage V1 to maintain constancy of the first voltage V1. For example, the intermediate circuit is a compensation circuit 22 below. In addition, maintaining constancy of the first voltage V1 may be understood as maintaining the first voltage V1 to be equal to a preset voltage value or maintaining the first voltage V1 to fluctuate in a small range around a preset voltage value. For example, the preset voltage value is 5 V If the first voltage V1 fluctuates in a range of [4.9 V, 5.1 V], it can be understood as that the first voltage V1 is constant.

[0036] Optionally, the amplifier 21 may be an integrated amplifier module. For example, the amplifier 21 may be an operational transimpedance amplifier (OTA) module. Alternatively, the amplifier 21 may be an amplifier built of electronic components. For example, as shown in FIG. 3, the amplifier 21 may include a first transistor M1, a second transistor M2, a third transistor M3, and a first resistor R1. One electrode of the first transistor M1, one electrode of the second transistor M2, and one terminal of the first resistor R1 are coupled and serve as an output terminal of the amplifier 21. A control terminal of the first transistor M1, a control terminal of the second transistor M2, and the other terminal of the first resistor R1 are coupled and serve as an input terminal of the amplifier 21. The other electrode of the second transistor M2 and one electrode of the third transistor M3 are coupled. One of the other electrode of the first transistor M1 and the other electrode of the third transistor M3 is coupled to a power terminal, and the other is coupled to a ground terminal. A control terminal of the third transistor M3 is coupled to a bias voltage terminal VBP.

[0037] The bias voltage terminal VBP is configured to supply a bias voltage to the third transistor M3. The third transistor M3 serves as a current source to supply a bias current to the amplifier 21. The first transistor M1 and the second transistor M2 form a common source amplifier. The first resistor R1 provides a static direct current bias voltage through direct coupling, so that the first transistor M1 and the second transistor M2 are both in a saturation region or a subthreshold region. Specifically, after being coupled to the input terminal of the amplifier 21 by using the first capacitor C1, the first voltage V1 is reversely amplified by the first transistor M1 and the second transistor M2, and the second voltage V2 is output from the output terminal of the amplifier 21.

[0038] It should be noted that in FIG. 3, an example is used for description in which the first transistor M1 is an NMOS transistor, the second transistor M2 and the third transistor M3 are both PMOS transistors, the one electrode is a drain, the other electrode is a source, and the control terminal is a gate. In actual application, the first transistor M1, the second transistor M2, and the third

transistor M3 may be alternatively replaced with other transistors with similar functions. FIG. 3 does not constitute any limitation on embodiments of this application.

[0039] The amplifier 21 is a phase inverter based amplifier. A transimpedance of the amplifier 21 is a sum of a transimpedance of the first transistor M1 and a transimpedance of the second transistor M2. Under same power consumption, the transimpedance of the amplifier 21 is twice that of a common amplifier. The third transistor M3 is configured to supply a bias current to the amplifier 21, to prevent power consumption of the amplifier 21 from changing with a voltage at the power terminal and a process corner. The amplifier 21 is coupled to the LDO 1 by using the first capacitor C1 and the second capacitor C2. This allows a direct current operating point of the amplifier 21 to be separately biased by using only the first resistor R1, effectively reducing a matching requirement of the amplifier 21.

[0040] In this embodiment of this application, the first voltage V1 output by the LDO 1 is coupled to the amplifier 21 by the first capacitor C1, and is amplified by the amplifier 21. Therefore, while a transient performance of the LDO 1 is improved, the small first capacitor C1 can be used to implement coupling of the first voltage V1, reducing a chip area occupied by the first capacitor C 1. In addition, the second voltage V2 output by the amplifier 21 is coupled to the LDO 1 by the second capacitor C2, so that the second voltage V2 does not act directly on an inherent loop of the LDO 1, avoiding destroying a direct current characteristic of the LDO 1, and ensuring stability of the loop of the LDO 1. Moreover, the amplifier 21 is coupled to the LDO 1 by using the first capacitor C1 and the second capacitor C2. In this way, a bias of the amplifier 21 can be separated from a direct current component of the first voltage V1, effectively reducing difficulty and complexity of biasing in the amplifier 21. That is, requirements such as offset and matching do not need to be considered during design of the amplifier 21, further reducing an area of a chip and implementing low power consumption and high energy efficiency.

[0041] Further, depending on whether the second capacitor C2 directly couples the second voltage V2 to the LDO 1, detection circuits may be classified into two types. A first type of detection circuit is a detection circuit including a compensation circuit. That is, the second capacitor C2 indirectly couples the second voltage V2 to the LDO 1. A second type of detection circuit is a detection circuit not including a compensation circuit. That is, the second capacitor C2 directly couples the second voltage V2 to the LDO 1. The at least one detection circuit 2 may include at least one of the two types of detection circuits. The following separately describes the two types of detection circuits.

[0042] The first type of detection circuit is a detection circuit including a compensation circuit. That is, the second capacitor C2 indirectly couples the second voltage V2 to the LDO 1.

[0043] Specifically, the at least one detection circuit 2 includes a first detection circuit 2a. The first detection circuit 2a includes a compensation circuit 22 coupled between the second capacitor C2 and the LDO 1. The compensation circuit 22 is configured to regulate the first voltage V1 based on the second voltage V2 to maintain constancy of the first voltage V1. The first detection circuit 2a in this specification may be a detection circuit including the compensation circuit 22.

[0044] In a possible embodiment, as shown in FIG. 4, the compensation circuit 22 includes a fourth transistor M4, a fifth transistor M5, a sixth transistor M6, a second resistor R2, and a third resistor R3. One electrode of the fourth transistor M4, one terminal of the third resistor R3, and one electrode of the sixth transistor M6 are coupled to a first node □. The other electrode of the fourth transistor M4, a control terminal of the fifth transistor M5, and one terminal of the second resistor R2 are coupled and serve as an input terminal of the compensation circuit 22. One electrode of the fifth transistor M5 and the other terminal of the second resistor R2 are coupled to a second node □. The other electrode of the fifth transistor M5, a control terminal of the sixth transistor M6, and the other terminal of the third resistor R3 are coupled. The other electrode of the sixth transistor M6 serves as an output terminal of the compensation circuit 22. One of the first node □ and the second node □ is coupled to the power terminal, and the other is coupled to the ground terminal.

[0045] Optionally, the at least one detection circuit 2 may include one or more first detection circuits. Output terminals of the one or more first detection circuits may be coupled to different nodes or a same node in the LDO 1. That is, the plurality of first detection circuits provide feedback to different nodes or a same node in the LDO 1. For example, as shown in FIG. 4, it is assumed that the at least one detection circuit 2 includes two first detection circuits, a first node □ in a compensation circuit 22 in one (denoted as 2a-1 in FIG. 4) of the two first detection circuits is coupled to the power terminal, and a second node □ in the compensation circuit 22 is coupled to the ground terminal; and a first node □ in a compensation circuit 22 in the other (denoted as 2a-2 in FIG. 4) of the two first detection circuits is coupled to the ground terminal, and a second node □ in the compensation circuit 22 is coupled to the power terminal. In FIG. 4, an example is used for description in which output terminals of the two first detection circuits are both coupled to an output terminal of the LDO 1 (that is, the two first detection circuits both provide feedback to the output terminal of the LDO 1), and the LDO is the LDO shown in FIG. 1. A VBP and a VBN represent different bias voltage terminals, respectively.

[0046] It should be noted that an example is used for description in which a fifth transistor M5 is an NMOS transistor, and a fourth transistor M4 and a sixth transistor M6 are both PMOS transistors in the first detection circuit 2a-1; a fifth transistor M5 is a PMOS transistor, and a fourth transistor M4 and a sixth transistor M6 are both

NMOS transistors in the first detection circuit 2a-2; and the one electrode is a drain, the other electrode is a source, and the control terminal is a gate. In actual application, the fourth transistor M4, the fifth transistor M5, and the sixth transistor M6 may be alternatively replaced with other transistors with similar functions. FIG. 4 does not constitute any limitation on embodiments of this application.

[0047] In addition, the second resistor R2 and the third resistor R3 in FIG. 4 may be alternatively replaced with other devices with similar functions. For example, the second resistor R2 may be replaced with an NMOS transistor, and the third resistor R3 may be replaced with a PMOS transistor. A gate of the NMOS transistor and a gate of the PMOS transistor may be connected to a bias voltage terminal.

[0048] In FIG. 4, the first detection circuit 2a-1 may be referred to as an undershoot detection circuit, and is configured to implement boost compensation for the first voltage V1 when the first voltage V1 output by the LDO 1 undershoots. Specifically, when the first voltage V1 output by the LDO 1 undershoots, the first detection circuit 2a-1 detects an undershoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the undershoot glitch is amplified by an amplifier 21 that includes M1, M2, M3, and R1, a second voltage V2 is obtained. The second voltage V2 is coupled to a gate of the fifth transistor M5 in the compensation circuit 22 by a second capacitor C2. In this case, the fifth transistor M5 is turned on, and a gate voltage of the sixth transistor M6 is pulled low. Therefore, the sixth transistor M6 is turned on. A drain voltage of the sixth transistor M6 is used to compensate for the first voltage V1 output by the LDO 1, to implement boost compensation for the first voltage V1, that is, to implement transient compensation for a case in which the first voltage V1 undershoots.

[0049] In a process in which the first detection circuit 2a-1 operates, transient compensation is triggered only when the second voltage V2 output by the amplifier 21 exceeds a threshold voltage of the fifth transistor M5. A bias voltage is formed after a drain current of the fourth transistor M4 passes through the second resistor R2, and can reduce the threshold voltage of the fifth transistor M5, so that a signal coupled by the second capacitor C2 can immediately turn on the fifth transistor M5. In addition, when the first voltage V1 output by the LDO 1 does not undershoot or an undershoot is less than the threshold voltage of the fifth transistor M5, the fifth transistor M5 in the compensation circuit 22 is turned off, and the third resistor R3 pulls up to turn off the sixth transistor M6. In this case, the first detection circuit 2a-1 has no impact on the LDO 1.

[0050] In FIG. 4, the first detection circuit 2a-2 may be referred to as an overshoot detection circuit, and is configured to implement buck regulation for the first voltage V1 when the first voltage V1 output by the LDO 1 overshoots. Specifically, when the first voltage V1 output by the LDO 1 overshoots, the first detection circuit 2a-2 detects an overshoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the overshoot glitch is amplified by an amplifier 21 that includes M1, M2, M3, and R1, a second voltage V2 is obtained. The second voltage V2 is coupled to a gate of the fifth transistor M5 in the compensation circuit 22 by a second capacitor C2. In this case, the fifth transistor M5 is turned on, and a gate voltage of the sixth transistor M6 is pulled low. Therefore, the sixth transistor M6 is turned on. A drain voltage of the sixth transistor M6 is used to pull low the first voltage V1 output by the LDO 1, to implement buck regulation for the first voltage V1, that is, to implement transient compensation for a case in which the first voltage V1 overshoots.

[0051] In a process in which the first detection circuit 2a-2 operates, transient compensation is triggered only when the second voltage V2 output by the amplifier 21 exceeds a threshold voltage of the fifth transistor M5. A bias voltage is formed after a drain current of the fourth transistor M4 passes through the second resistor R2, and can reduce the threshold voltage of the fifth transistor M5, so that a signal coupled by the second capacitor C2 can immediately turn on the fifth transistor M5. In addition, when the first voltage V1 output by the LDO 1 does not overshoot or an overshoot is less than the threshold voltage of the fifth transistor M5, the fifth transistor M5 in the compensation circuit 22 is turned off, and the third resistor R3 pulls low to turn off the sixth transistor M6. In this case, the first detection circuit 2a-2 has no impact on the LDO 1.

[0052] In another possible embodiment, as shown in FIG. 5, the compensation circuit 22 includes a fourth transistor M4, a fifth transistor M5, and a second resistor R2. One electrode of the fourth transistor M4 is coupled to a first node □. The other electrode of the fourth transistor M4, a control terminal of the fifth transistor M5, and one terminal of the second resistor R2 are coupled and serve as an input terminal of the compensation circuit 22. One electrode of the fifth transistor M5 and the other terminal of the second resistor R2 are coupled to a second node □. The other electrode of the fifth transistor M5 serves as an output terminal of the compensation circuit 22. One of the first node □ and the second node □ is coupled to the power terminal, and the other is coupled to the ground terminal.

[0053] Optionally, the at least one detection circuit 2 may include one or more first detection circuits. Output terminals of the one or more first detection circuits may be coupled to different nodes or a same node in the LDO 1. That is, the plurality of first detection circuits provide feedback to a plurality of first detection circuits. For example, as shown in FIG. 5, it is assumed that the at least one detection circuit 2 includes a first detection circuit 2a, a first node □ in a compensation circuit 22 in the first detection circuit 2a is coupled to the power terminal, a

second node □ in the compensation circuit 22 is coupled to the ground terminal, the LDO is the LDO shown in FIG. 1, and an output terminal of the first detection circuit 2a is coupled to the gate of the voltage regulating transistor M0 in the LDO 1 (that is, the first detection circuit 2a provides feedback to the gate of the voltage regulating transistor M0 in the LDO 1). A working principle of the first detection circuit 2a is similar to a working principle of the first detection circuit 2a-1. Therefore, details are not described herein again in this embodiment of this application.

[0054] It should be noted that in FIG. 5, an example is used for description in which the fourth transistor M4 is a PMOS transistor, the fifth transistor M5 is an NMOS transistor, the one electrode is a drain, the other electrode is a source, and the control terminal is a gate. In actual application, the fourth transistor M4 and the fifth transistor M5 may be alternatively replaced with other transistors with similar functions. In addition, in FIG. 5, an example is used for description in which the at least one detection circuit 2 includes the first detection circuit 2a. FIG. 5 does not constitute any limitation on embodiments of this application.

[0055] Further, in addition to the LDO 1 shown in FIG. 1, the first detection circuits shown in FIG. 4 and FIG. 5 may be applied to an LDO of another structure. For example, the operational amplifier A0 in the LDO 1 may be an operational amplifier built of a plurality of transistors, or the LDO may be a flipped voltage follower (FVF) LDO, that is, an FVF LDO.

[0056] For example, as shown in FIG. 6, the operational amplifier A0 in the LDO 1 may include a total of 12 transistors from T1 to T12. Specific connection relationships between the transistors T1 to T12 are shown in the figure. VBP and VBN represent bias voltages, respectively. The at least one detection circuit 2 may provide feedback to any node in the operational amplifier A0, provided that negative feedback is formed. For example, the at least one detection circuit 2 provides feedback to a gate of the transistor T2 (which may also be referred to as a gate of the transistor T3). Alternatively, the at least one detection circuit 2 provides feedback to a gate of the transistor T5 (which may also be referred to as a gate of the transistor T6). It should be noted that in FIG. 6, an example is used for description in which the transistors T1, T4, T8, T9, T10, T11, and T12 are all PMOS transistors, and the transistors T2, T3, T5, T6, and T7 are all NMOS transistors. The transistors T1 to T12 may be alternatively replaced with other transistors with similar functions, or the operational amplifier A0 includes more or fewer transistors. FIG. 6 does not constitute any limitation on embodiments of this application.

[0057] For example, as shown in FIG. 7, when the LDO 1 is an FVF LDO, the LDO 1 may include a seventh transistor M7, an eighth transistor M8, a ninth transistor M9, a tenth transistor M10, an eleventh transistor M11, and a fourth resistor R4. One electrode of the seventh transistor M7 and one electrode of the eighth transistor M8 are both coupled to the power terminal. The other electrode of the seventh transistor M7 and one electrode of the ninth transistor M9 are coupled and serve as the output terminal of the LDO 1. The other electrode of the eighth transistor M8, one electrode of the tenth transistor M10, and a control terminal of the seventh transistor M7 are coupled (a voltage at a coupling point is denoted as V_{FB2}). The other electrode of the ninth transistor M9, the other electrode of the tenth transistor M10, and one electrode of the eleventh transistor M11 are coupled (a voltage at a coupling point is denoted as V_{FB1}). The other electrode of the eleventh transistor M11 is coupled to the ground terminal. A control terminal of the eleventh transistor M11 and one terminal of the fourth resistor R4 are coupled. The other terminal of the fourth resistor R4 is connected to a bias voltage terminal VBN1.

[0058] It should be noted that in FIG. 7, an example is used for description in which the seventh transistor M7, the eighth transistor M8, and the ninth transistor M9 are all PMOS transistors; the tenth transistor M10 and the eleventh transistor M11 are both NMOS transistors; the one electrodes of the seventh transistor M7 to the ninth transistor are sources, and the other electrodes of the seventh transistor M7 to the ninth transistor are drains; the one electrodes of the tenth transistor M10 and the eleventh transistor M11 are drains, and the other electrodes of the tenth transistor M10 and the eleventh transistor M11 are sources; and the control terminals are gates. In actual application, the seventh transistor M7 to the eleventh transistor M11 may be alternatively replaced with other transistors with similar functions. FIG. 7 does not constitute any limitation on embodiments of this application.

[0059] The output terminal of the first detection circuit shown in FIG. 4 or FIG. 5 may be alternatively coupled to the output terminal of the FVF LDO or another node inside the FVF LDO. For example, the output terminal of the first detection circuit is coupled to the control terminal of the seventh transistor M7 in the FVF LDO, or the output terminal of the first detection circuit is coupled to a control terminal of the eighth transistor M8 in the FVF LDO, or the output terminal of the first detection circuit is coupled to a control terminal of the tenth transistor M10 in the FVF LDO, or the output terminal of the first detection circuit is coupled to the control terminal of the eleventh transistor M11 in the FVF LDO.

[0060] The second type of detection circuit is a detection circuit not including a compensation circuit. That is, the second capacitor C2 directly couples the second voltage V2 to the LDO 1. The following uses a structure of the FVF LDO shown in FIG. 7 as an example for description.

[0061] In a possible embodiment, as shown in FIG. 8, the at least one detection circuit 2 includes a second detection circuit 2b. A second capacitor C2 in the second detection circuit 2b is coupled between an output terminal of an amplifier 21 and the control terminal (that is, a gate) of the eighth transistor M8. That is, the second detection

circuit 2b provides feedback to the gate of the eighth transistor M8 in the FVF LDO.

[0062] Specifically, when a first voltage V1 output by the FVF LDO is normal, the second detection circuit 2b does not operate. It is assumed that a current flowing through the eleventh transistor M11 is 111, a current flowing through the eighth transistor M8 is I8, a current flowing through the tenth transistor M10 is I10, and a current flowing through the ninth transistor M9 is I9. I11=I9+I8. I8=I10.

[0063] When the FVF LDO undershoots, the second detection circuit 2b detects an undershoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the undershoot glitch is amplified by the amplifier 21, a second voltage V2 is obtained. The second voltage V2 is coupled to the gate of the eighth transistor M8 in the FVF LDO by the second capacitor C2. In this case, a gate-source voltage (that is, Vgs) of the eighth transistor M8 decreases, to control the current I8 flowing through the eighth transistor M8 to decrease. In addition, because the current I10 flowing through the tenth transistor M10 remains unchanged, I10 is greater than I8 in this case. As a result, a gate voltage V_{BF2} of the seventh transistor is pulled low, and a gate-source voltage (that is, Vgs) of the seventh transistor M7 increases rapidly, increasing an output current of the FVF LDO, that is, implementing transient compensation for a case in which the first voltage V1 undershoots.

[0064] When the FVF LDO overshoots, the second detection circuit 2b detects an overshoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the overshoot glitch is amplified by the amplifier 21, a second voltage V2 is obtained. The second voltage V2 is coupled to the gate of the eighth transistor M8 in the FVF LDO by the second capacitor C2. In this case, a gate-source voltage (that is, Vgs) of the eighth transistor M8 increases, to control the current I8 flowing through the eighth transistor M8 to increase. In addition, because the current I10 flowing through the tenth transistor M10 remains unchanged, I10 is less than I8 in this case. As a result, a gate voltage V_{BF2} of the seventh transistor is pulled up, and a gate-source voltage (that is, Vgs) of the seventh transistor M7 decreases, decreasing an output current of the FVF LDO, that is, implementing transient compensation for a case in which the first voltage V1 overshoots.

[0065] In another possible embodiment, as shown in FIG. 9, the at least one detection circuit 2 includes a third detection circuit 2c. A second capacitor C2 in the third detection circuit 2c is coupled between an output terminal of an inverting amplifier 21 and the control terminal (that is, a gate) of the tenth transistor M10. That is, the third detection circuit 2c provides feedback to the gate of the tenth transistor M10 in the FVF LDO.

[0066] Specifically, when a first voltage V1 output by the FVF LDO is normal, the second detection circuit 2b does not operate. It is assumed that a current flowing through the eleventh transistor M11 is 111, a current flowing through the eighth transistor M8 is I8, a current flowing through the tenth transistor M10 is I10, and a current flowing through the ninth transistor M9 is I9. I11=I9+I8. I8=I10.

[0067] When the FVF LDO undershoots, the third detection circuit 2c detects an undershoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the undershoot glitch is amplified by the inverting amplifier 21, a second voltage V2 is obtained. The second voltage V2 is coupled to the gate of the tenth transistor M10 in the FVF LDO by the second capacitor C2. In this case, a gate-source voltage (that is, Vgs) of the tenth transistor M10 increases, to control the current I10 flowing through the tenth transistor M10 to increase. In addition, because the current I8 flowing through the eighth transistor M8 remains unchanged, I10 is greater than I8 in this case. As a result, a gate voltage V_{BF2} of the seventh transistor is pulled low, and a gate-source voltage (that is, Vgs) of the seventh transistor M7 increases rapidly, increasing an output current of the FVF LDO, that is, implementing transient compensation for a case in which the first voltage V1 undershoots.

[0068] When the FVF LDO overshoots, the third detection circuit 2c detects an overshoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the overshoot glitch is amplified by the inverting amplifier 21, a second voltage V2 is obtained. The second voltage V2 is coupled to the gate of the tenth transistor M10 in the FVF LDO by the second capacitor C2. In this case, a gate-source voltage (that is, Vgs) of the tenth transistor M10 decreases, to control the current I10 flowing through the tenth transistor M10 to decrease. In addition, because the current I8 flowing through the eighth transistor M8 remains unchanged, I10 is less than I8 in this case. As a result, a gate voltage V_{BF2} of the seventh transistor is pulled up, and a gate-source voltage (that is, Vgs) of the seventh transistor M7 decreases, decreasing an output current of the FVF LDO, that is, implementing transient compensation for a case in which the first voltage V1 overshoots.

[0069] In still another possible embodiment, as shown in FIG. 10, the at least one detection circuit 2 includes a fourth detection circuit 2d. A second capacitor C2 in the fourth detection circuit 2d is coupled between an output terminal of an inverting amplifier 21 and the control terminal (that is, a gate) of the eleventh transistor M11. That is, the fourth detection circuit 2d provides feedback to the gate of the eleventh transistor M11 in the FVF LDO.

[0070] Specifically, when a first voltage V1 output by the FVF LDO is normal, the second detection circuit 2b does not operate. It is assumed that a current flowing through the eleventh transistor M11 is 111, a current flowing through the eighth transistor M8 is I8, a current flowing through the tenth transistor M10 is I10, and a current

flowing through the ninth transistor M9 is I9. I11=I9+I8. I8=I10.

[0071] When the FVF LDO undershoots, the fourth detection circuit 2d detects an undershoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the undershoot glitch is amplified by the inverting amplifier 21, a second voltage V2 is obtained. The second voltage V2 is coupled to the gate of the eleventh transistor M11 in the FVF LDO by the second capacitor C2. In this case, a gate-source voltage (that is, Vgs) of the eleventh transistor M11 increases, to control the current I10 flowing through the eleventh transistor M10 to increase. In addition, because the current I8 flowing through the eighth transistor M8 remains unchanged, the current I9 flowing through the ninth transistor M9 decreases, and the current I10 flowing through the tenth transistor M10 increases, I10 is greater than I8 in this case. As a result, a gate voltage V_{BF2} of the seventh transistor is pulled low, and a gate-source voltage (that is, Vgs) of the seventh transistor M7 increases rapidly, increasing an output current of the FVF LDO, that is, implementing transient compensation for a case in which the first voltage V1 undershoots.

[0072] When the FVF LDO overshoots, the fourth detection circuit 2d detects an overshoot glitch (that is, a coupling voltage that is generated based on a change in the first voltage V1) of the first voltage V1 by using a first capacitor C1. After the overshoot glitch is amplified by the amplifier 21, a second voltage V2 is obtained. The second voltage V2 is coupled to the gate of the eleventh transistor M11 in the FVF LDO by the second capacitor C2. In this case, a gate-source voltage (that is, Vgs) of the eleventh transistor M11 decreases, to control the current I11 flowing through the eleventh transistor M11 to decrease. In addition, because the current I8 flowing through the eighth transistor M8 remains unchanged, the current I9 flowing through the ninth transistor M9 increases, and the current I10 flowing through the tenth transistor M10 decreases, I10 is less than I8 in this case. As a result, a gate voltage V_{BF2} of the seventh transistor is pulled up, and a gate-source voltage (that is, Vgs) of the seventh transistor M7 decreases, decreasing an output current of the FVF LDO, that is, implementing transient compensation for a case in which the first voltage V1 overshoots.

[0073] Further, for overshoot compensation or undershoot compensation for the LDO 1, a plurality of detection circuits may be used to implement transient compensation for the LDO 1. Output terminals of the plurality of detection circuits may be coupled to different nodes in the LDO 1, provided that it is ensured that coupling between each detection circuit and the LDO 1 forms negative feedback.

[0074] For example, as shown in FIG. 11, undershoot compensation for the FVF LDO is used as an example. The at least one detection circuit 2 may include four detection circuits that are denoted as 201 to 204, respectively. An output terminal of the detection circuit 201 is coupled to the output terminal of the FVF LDO. An output terminal of the detection circuit 202 is coupled to a gate of the seventh transistor M7 in the FVF LDO. An output terminal of the detection circuit 203 is coupled to the gate of the eighth transistor M8 in the FVF LDO. An output terminal of the detection circuit 204 is coupled to the gate of the eleventh transistor M11 in the FVF LDO.

[0075] A working principle of the detection circuit 201 is similar to a working principle of the first detection circuit 2a-1 shown in FIG. 4. A working principle of the detection circuit 202 is similar to a working principle of the first detection circuit 2a shown in FIG. 5. A working principle of the detection circuit 203 is similar to a working principle of the second detection circuit 2b shown in FIG. 8. A working principle of the detection circuit 204 is similar to a working principle of the fourth detection circuit 2d shown in FIG. 10. For details, refer to relevant descriptions above. Details are not described herein again in this embodiment of this application.

[0076] In this embodiment of this application, transient compensation is performed for overshooting or undershooting of the LDO 1 by using the plurality of detection circuits, more quickly implementing transient compensation for the LDO 1 and improving transient performance of the LDO 1. In addition, when the first voltage V1 output by the LDO 1 is normal or a change in the first voltage V1 is small, the plurality of detection circuits may be in an off state, not affecting a direct current characteristic of the LDO 1, and ensuring stability of a loop of the LDO 1.

[0077] Based on this, an embodiment of this application further provides a chip system. The chip system includes a load circuit and any transient performance improvement circuit used for an LDO provided above. The transient performance improvement circuit includes an LDO and at least one detection circuit coupled to the LDO. The LDO is configured to supply power to the load circuit. The at least one detection circuit is configured to improve a transient performance of the LDO. Optionally, the load circuit may include at least one of the following: an RF transceiver, a DAC, an ADC, a high-speed digital circuit (for example, a system-on-a-chip SoC), and a PLL.

[0078] An embodiment of this application further provides a device. The device includes a load circuit and a circuit board. The circuit board includes any transient performance improvement circuit used for an LDO provided above. The transient performance improvement circuit includes an LDO and at least one detection circuit coupled to the LDO. The LDO is configured to supply power to the load circuit. The at least one detection circuit is configured to improve a transient performance of the LDO. Optionally, the load circuit may include at least one of the following: an RF transceiver, a DAC, an ADC, a high-speed digital circuit (for example, a system-on-a-chip SoC), and a PLL. In addition, the device may be a communication device, a voltage regulating device, or the like. This is not specifically limited in this embodiment of this application.

[0079] It should be noted that relevant descriptions of the transient performance improvement circuit used for an LDO provided above may all be cited and incorporated into a description of the chip system or the device. Details are not described herein again in embodiments of this application.

[0080] According to another aspect of this application, a non-transitory computer-readable storage medium used with a computer is further provided. The computer has software used for creating an integrated circuit. The computer-readable storage medium stores one or more computer-readable data structures. The one or more computer-readable data structures have photomask data used for manufacturing the transient performance improvement circuit used for an LDO provided in any of the figures provided above.

[0081] In conclusion, the foregoing descriptions are merely specific implementations of this application, but are not intended to limit the protection scope of this application. Any variation or replacement within the technical scope disclosed in this application shall fall within the protection scope of this application. Therefore, the protection scope of this application shall be subject to the protection scope of the claims.

Claims

1. A transient performance improvement circuit used for a low dropout regulator, LDO, comprising:

   an LDO, configured to output a first voltage; and at least one detection circuit coupled to the LDO, wherein each of the at least one detection circuit comprises a first capacitor, an amplifier, and a second capacitor, wherein
   the first capacitor is configured to generate a coupling voltage based on a change in the first voltage and couple the coupling voltage to the amplifier;
   the amplifier is configured to amplify the coupling voltage to obtain a second voltage; and
   the second capacitor is configured to couple the second voltage to the LDO, wherein the second voltage is used to regulate the first voltage to maintain constancy of the first voltage.

2. The circuit according to claim 1, wherein the amplifier comprises a first transistor, a second transistor, a third transistor, and a first resistor; and
   one electrode of the first transistor, one electrode of the second transistor, and one terminal of the first resistor are coupled and serve as an output terminal of the amplifier; a control terminal of the first transistor, a control terminal of the second transistor, and the other terminal of the first resistor are coupled and serve as an input terminal of the amplifier; the other electrode of the second transistor and one electrode of the third transistor are coupled; one of the other electrode of the first transistor and the other electrode of the third transistor is coupled to a power terminal, and the other is coupled to a ground terminal; and a control terminal of the third transistor is coupled to a bias voltage terminal.

3. The circuit according to claim 1 or 2, wherein the at least one detection circuit comprises a first detection circuit, and the first detection circuit further comprises a compensation circuit coupled between the second capacitor and the LDO; and
   the compensation circuit is configured to regulate the first voltage based on the second voltage to maintain constancy of the first voltage.

4. The circuit according to claim 3, wherein the compensation circuit comprises a fourth transistor, a fifth transistor, a sixth transistor, a second resistor, and a third resistor;

   one electrode of the fourth transistor, one terminal of the third resistor, and one electrode of the sixth transistor are coupled to a first node; the other electrode of the fourth transistor, a control terminal of the fifth transistor, and one terminal of the second resistor are coupled and serve as an input terminal of the compensation circuit; one electrode of the fifth transistor and the other terminal of the second resistor are coupled to a second node; the other electrode of the fifth transistor, a control terminal of the sixth transistor, and the other terminal of the third resistor are coupled; and the other electrode of the sixth transistor serves as an output terminal of the compensation circuit; and
   one of the first node and the second node is coupled to the power terminal, and the other is coupled to the ground terminal.

5. The circuit according to claim 4, wherein the LDO has an output terminal, and the output terminal of the compensation circuit and the output terminal of the LDO are coupled.

6. The circuit according to claim 3, wherein the compensation circuit comprises a fourth transistor, a fifth transistor, and a second resistor; and
   one electrode of the fourth transistor is coupled to a first node; the other electrode of the fourth transistor, a control terminal of the fifth transistor, and one terminal of the second resistor are coupled and serve as an input terminal of the compensation circuit; one electrode of the fifth transistor and the other terminal of the second resistor are coupled to a second node; the other electrode of the fifth transistor serves as an output terminal of the compensation circuit; and one of the first node and the second node is coupled

to the power terminal, and the other is coupled to the ground terminal.

7. The circuit according to claim 6, wherein the LDO comprises an operational amplifier, a voltage regulating transistor, and a sampling circuit; an output terminal of the operational amplifier and a control terminal of the voltage regulating transistor are coupled; one electrode of the voltage regulating transistor is coupled to the power terminal; the other electrode of the voltage regulating transistor and an input terminal of the sampling circuit are coupled and serve as an output terminal of the LDO; an output terminal of the sampling circuit and a non-inverting input terminal of the operational amplifier are coupled; and an inverting input terminal of the operational amplifier is configured to receive a reference voltage; and
the output terminal of the compensation circuit and the control terminal of the voltage regulating transistor are coupled.

8. The circuit according to any one of claims 1 to 5, wherein the LDO comprises a seventh transistor, an eighth transistor, a ninth transistor, a tenth transistor, an eleventh transistor, and a fourth resistor; and
one electrode of the seventh transistor and one electrode of the eighth transistor are both coupled to the power terminal; the other electrode of the seventh transistor and one electrode of the ninth transistor are coupled and serve as the output terminal of the LDO; the other electrode of the eighth transistor, one electrode of the tenth transistor, and a control terminal of the seventh transistor are coupled; the other electrode of the ninth transistor, the other electrode of the tenth transistor, and one electrode of the eleventh transistor are coupled; the other electrode of the eleventh transistor is coupled to the ground terminal; a control terminal of the eleventh transistor and one terminal of the fourth resistor are coupled; and the other terminal of the fourth resistor is connected to the bias voltage terminal.

9. The circuit according to claim 8, wherein the at least one detection circuit further comprises a second detection circuit, and a second capacitor in the second detection circuit is coupled between an output terminal of an amplifier and a control terminal of the eighth transistor.

10. The circuit according to claim 8 or 9, wherein the at least one detection circuit further comprises a third detection circuit, and a second capacitor in the third detection circuit is coupled between an output terminal of an amplifier and a control terminal of the tenth transistor.

11. The circuit according to any one of claims 8 to 10, wherein the at least one detection circuit further comprises a fourth detection circuit, and a second capacitor in the fourth detection circuit is coupled between an output terminal of an amplifier and the control terminal of the eleventh transistor.

12. A chip system, wherein the chip system comprises a load circuit and the transient performance improvement circuit used for a low dropout regulator, LDO, according to any one of claims 1 to 11; the transient performance improvement circuit comprises an LDO and at least one detection circuit coupled to the LDO; the LDO is configured to supply power to the load circuit; and the at least one detection circuit is configured to improve a transient performance of the LDO.

13. A device, wherein the device comprises a load circuit and a circuit board; the circuit board comprises the transient performance improvement circuit used for a low dropout regulator, LDO, according to any one of claims 1 to 11; the transient performance improvement circuit comprises an LDO and at least one detection circuit coupled to the LDO; the LDO is configured to supply power to the load circuit; and the at least one detection circuit is configured to improve a transient performance of the LDO.

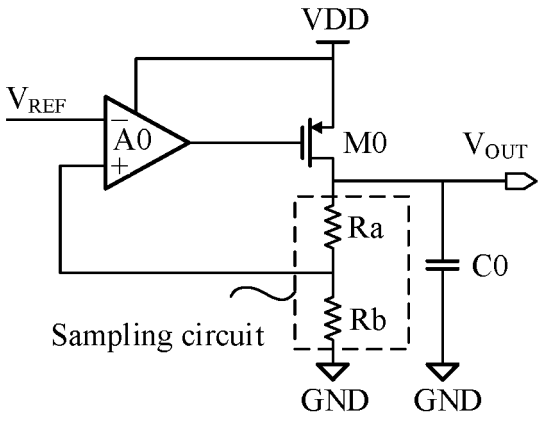

FIG. 1

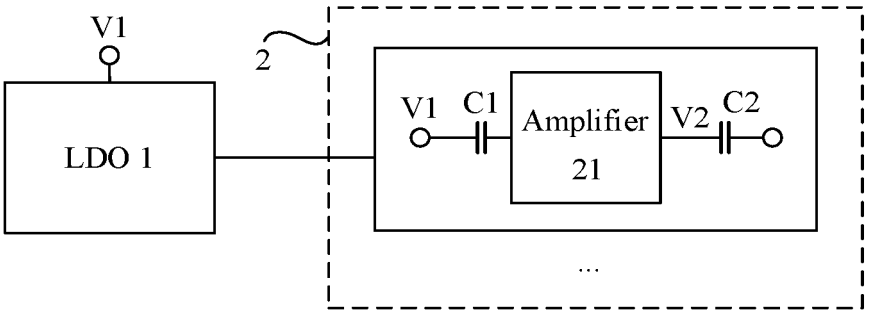

FIG. 2

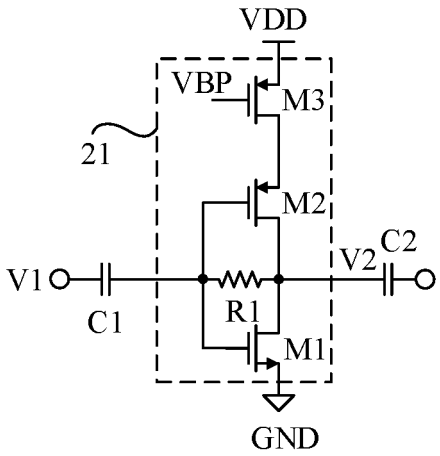

FIG. 3

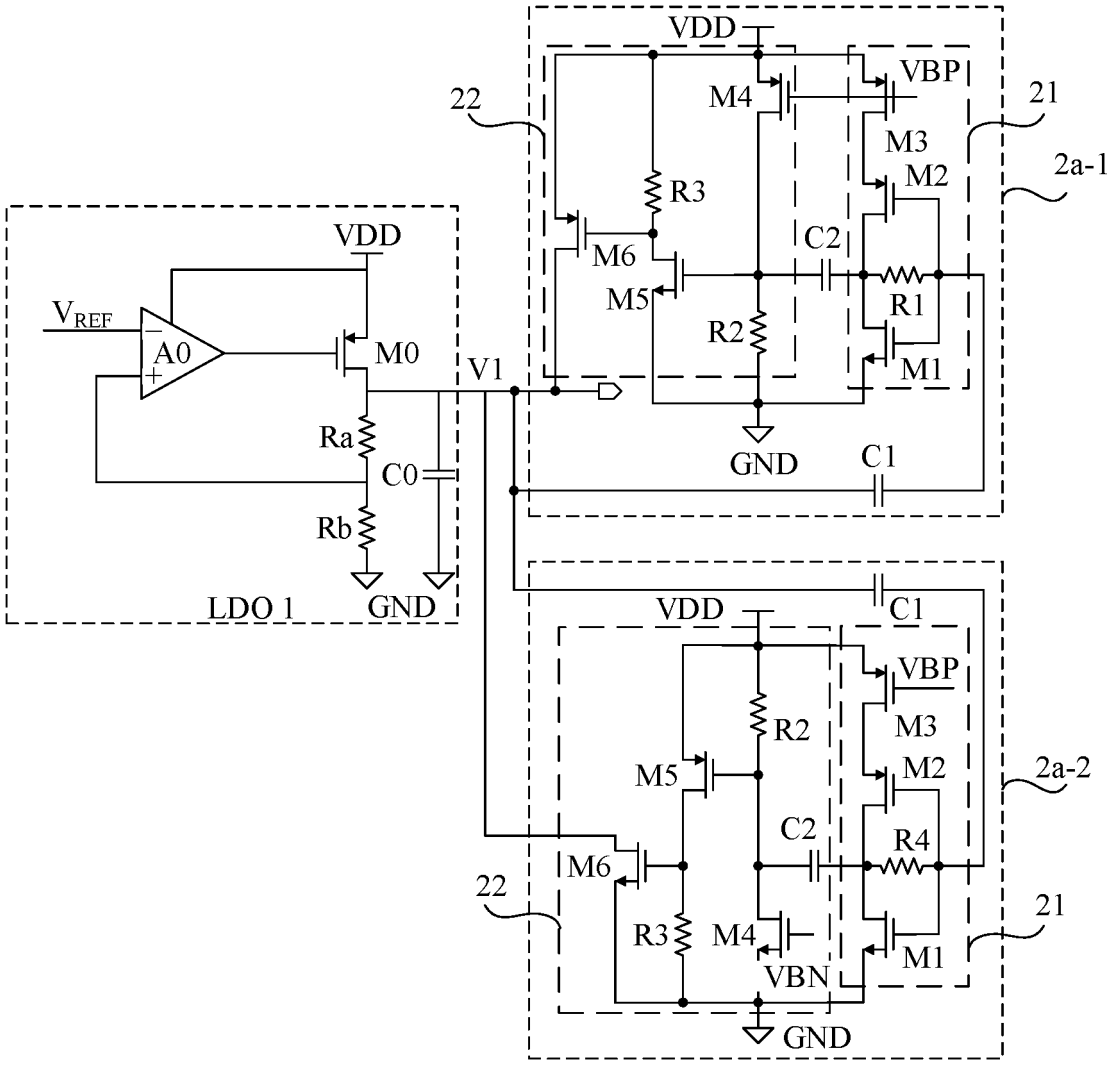
VDD
VBP
M4
M3
M2
R3
M6
C2
M5
R1
R2
M1
GND
C1
22
21
2a-1
VDD
VREF
A0
M0
V1
Ra
C0
Rb
LDO 1
GND
VDD
C1
VBP
R2
M3
M5
M2
2a-2
C2
R4
M6
22
R3
M4
21
M1
VBN
GND

FIG. 4

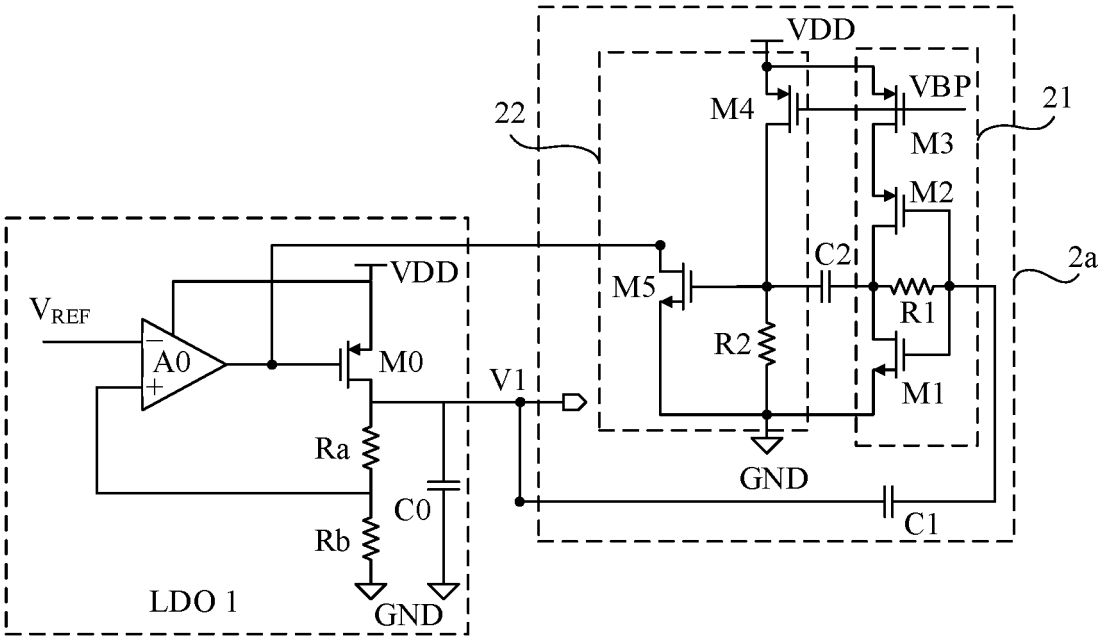
VDD
VBP
M4
M3
M2
22
21
2a
C2
M5
R1
R2
M1
VDD
V_{REF}
A0
M0
V1
Ra
GND
C0
C1
Rb
LDO 1
GND

FIG. 5

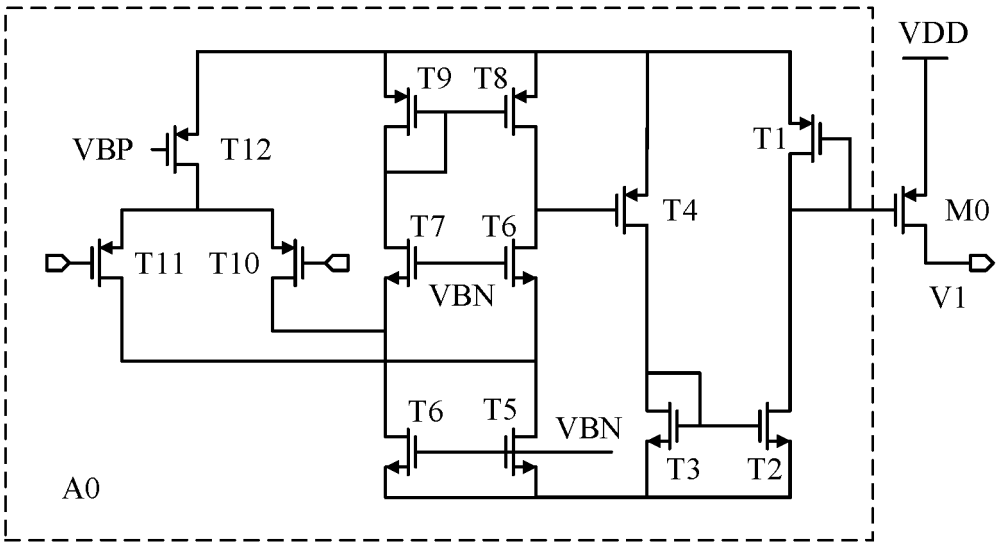
VDD
T9
T8
VBP
T12
T1
T4
M0
T7
T6
T11
T10
V1
VBN
T6
T5
VBN
T3
T2
A0

FIG. 6

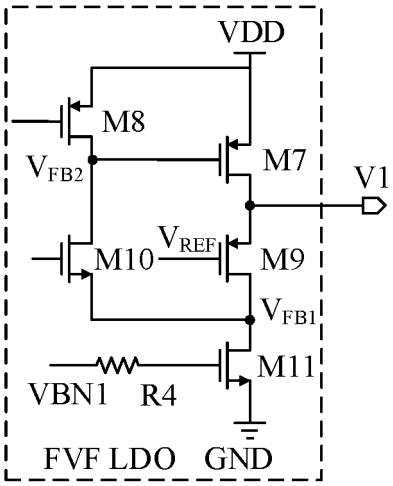
VDD
M8
V_{FB2}
M7
V1
V_{REF}
M10
M9
V_{FB1}
M11
VBN1
R4
FVF LDO
GND

FIG. 7

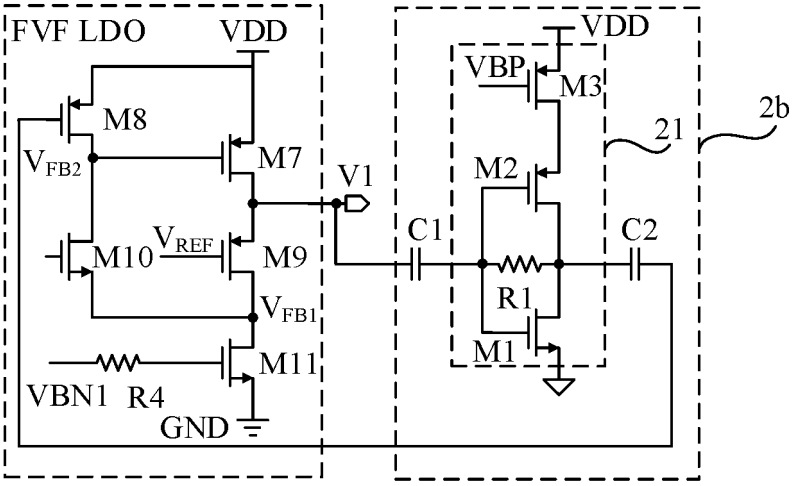
FVF LDO
VDD
M8
V_{FB2}
M7
V1
V_{REF}
M10
M9
V_{FB1}
M11
VBN1
R4
GND
VDD
VBP
M3
2b
21
M2
C1
C2
R1
M1

FIG. 8

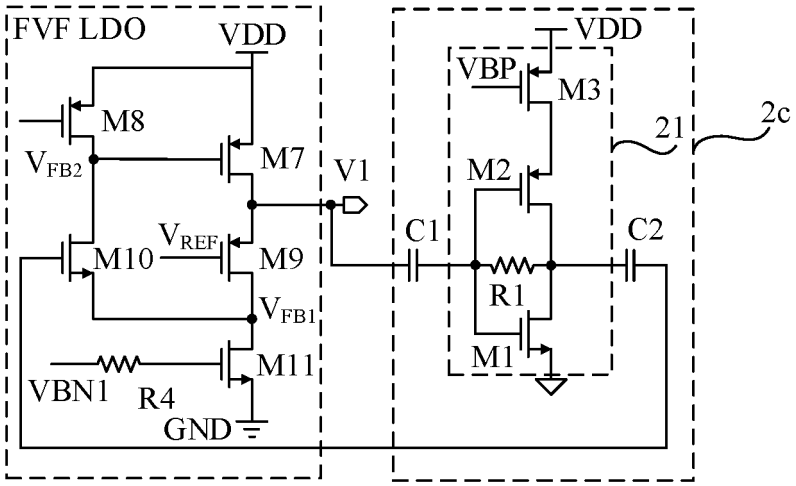
FVF LDO
VDD
M8
V_{FB2}
M7
V1
V_{REF}
M10
M9
V_{FB1}
M11
VBN1
R4
GND
VDD
VBP
M3
21
2c
M2
C1
C2
R1
M1

FIG. 9

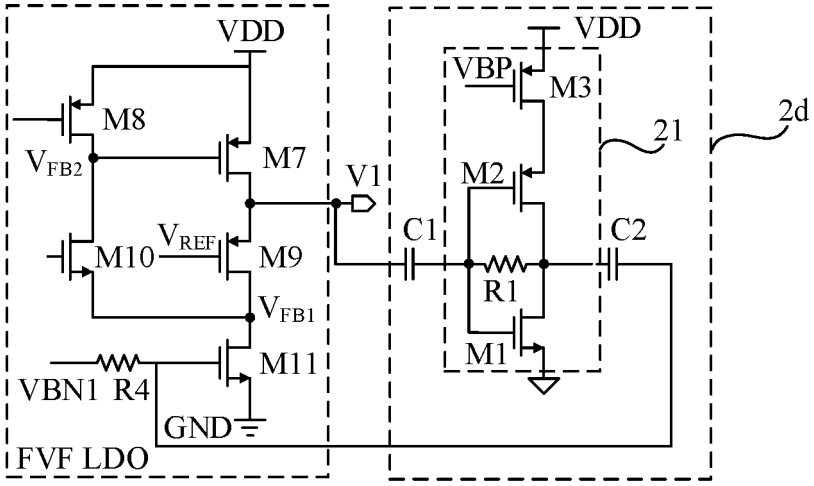
VDD
M8
V_{FB2}
M7
V1
V_{REF}
M10
M9
V_{FB1}
M11
VBN1
R4
GND
FVF LDO
VDD
VBP
M3
21
2d
M2
C1
C2
R1
M1

FIG. 10

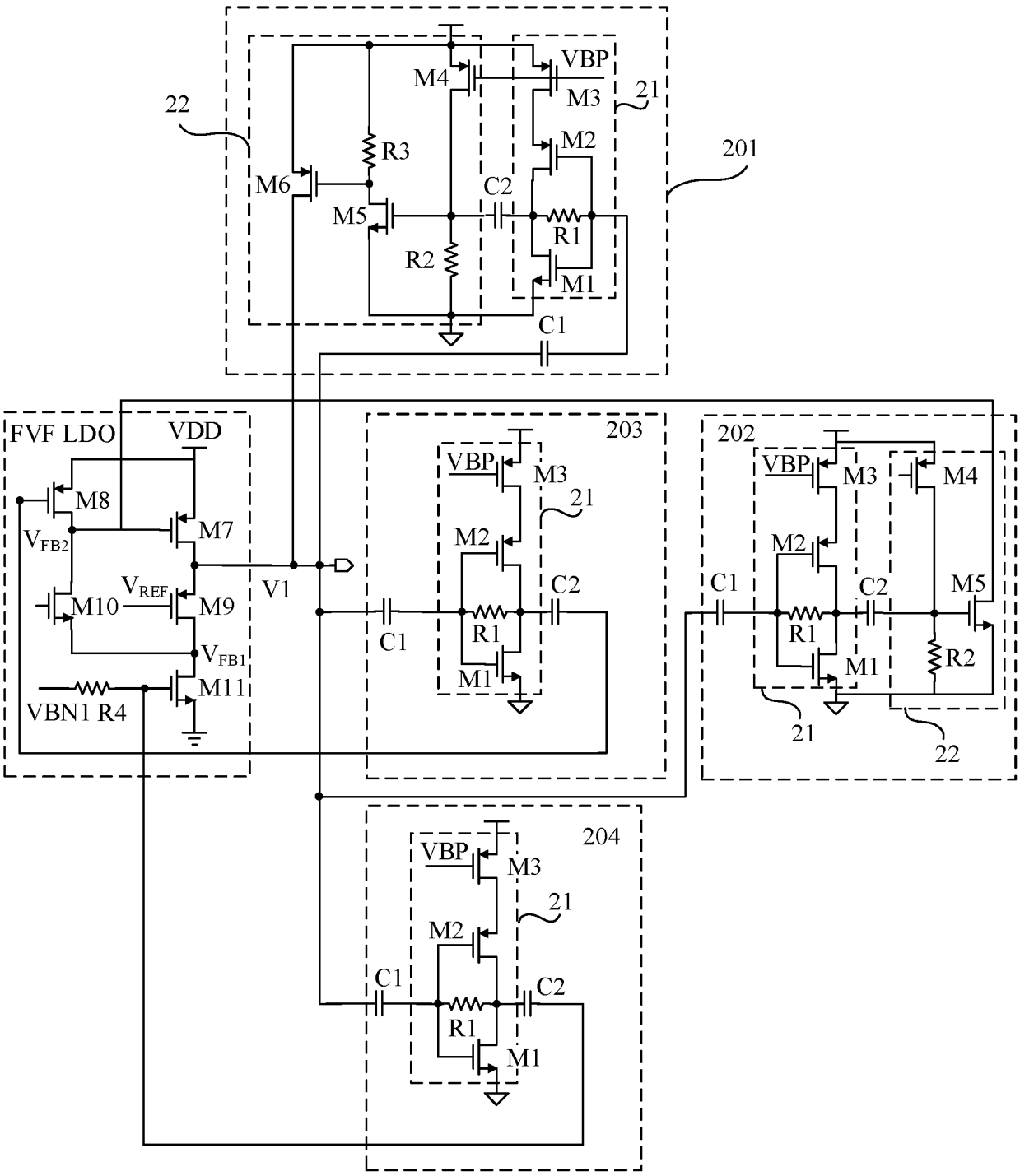
22
M4
VBP
M3
21
201
R3
M2
M6
C2
M5
R1
R2
M1
C1
FVF LDO
VDD
M8
M7
V_{FB2}
V_{REF}
M10
M9
V1
V_{FB1}
M11
VBN1 R4
203
202
204
C1
C2
M5
R2

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/111524

A. CLASSIFICATION OF SUBJECT MATTER

G05F 1/56(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: 线性稳压器, 低压差, 放大器, 电容, 芯片, 面积, 减少, 降低, 节省, 片内, 片外, 补偿, 上冲, 下冲, 过冲, 电压, LDO, low dropout regulator, regulator, amplifier, capacitance, capacitor, chip, area, reduce, compensat+, undershoot, overshoot, voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 107102666 A (MEDIATEK SINGAPORE PTE. LTD.) 29 August 2017 (2017-08-29) description paragraphs 0013-0043, figure 2	1-3, 12, 13
A	CN 106774580 A (WUHAN ZHONGWEI INFORMATION TECHNOLOGY CO., LTD.) 31 May 2017 (2017-05-31) entire document	1-13
A	CN 102722207 A (HUAWEI TECHNOLOGIES CO., LTD.) 10 October 2012 (2012-10-10) entire document	1-13
A	CN 110162130 A (NINGBO UNIVERSITY) 23 August 2019 (2019-08-23) entire document	1-13
A	US 7221213 B2 (AIMTRON TECHNOLOGY CORP.) 22 May 2007 (2007-05-22) entire document	1-13

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 May 2021	**26 May 2021**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088** **China**	Authorized officer
Facsimile No. **(86-10)62019451**	Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2020/111524

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
CN 107102666 A	29 August 2017	CN 107102676 A	29 August 2017
		US 2017242449 A1	24 August 2017
CN 106774580 A	31 May 2017	CN 106774580 B	22 June 2018
CN 102722207 A	10 October 2012	CN 102722207 B	20 August 2014
CN 110162130 A	23 August 2019	CN 110162130 B	02 June 2020
US 7221213 B2	22 May 2007	US 2007030054 A1	08 February 2007

Form PCT/ISA/210 (patent family annex) (January 2015)