(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 202 895 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
28.06.2023 Bulletin 2023/26

(21) Application number: **21217449.4**

(22) Date of filing: **23.12.2021**

(51) International Patent Classification (IPC):
G09G 3/20 *(2006.01)* ***G09G 3/3208*** *(2016.01)*

(52) Cooperative Patent Classification (CPC):
G09G 3/2014; G09G 3/2018; G09G 3/3208;
G09G 2300/0804; G09G 2300/0814;
G09G 2300/0852; G09G 2300/0857

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

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(54) **PIXEL ARRANGEMENT**

(57) A pixel arrangement (100) is integrable as part of a display (200), said display (200) comprising a plurality of self-emitting pixel elements (108), said pixel arrangement (100) comprising a pixel data storage block (102) connected to a pixel data line and comprising a pixel data storage element (110); a pixel driver block (106) for generating a pixel current; and a selection block (104) connected to said pixel data storage block and to a plurality of selection lines (s_1, s_2, EN1, EN2, EN3, EN4), wherein said selection block (104) is configured to switch said pixel current through a respective self-emitting pixel element (108) of said plurality of self-emitting pixel elements (108) based on said plurality of selection lines.

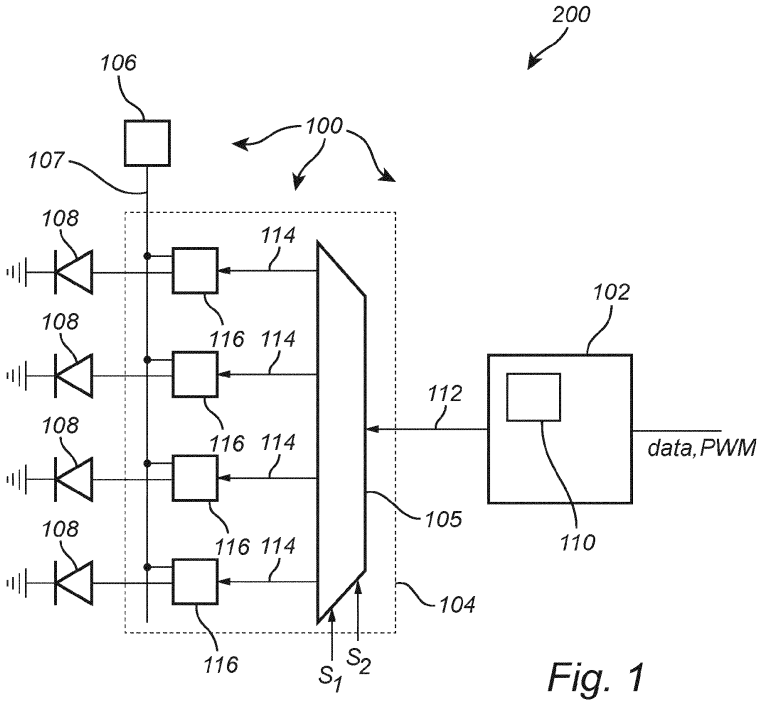

Fig. 1

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Description

Technical field

[0001] The present inventive concept relates to a pixel arrangement and to a display.

Background

[0002] Displays comprising self-emitting pixel elements, such as AMOLED and AMLED displays find wide application. Such displays may be active matrix (AM) displays and comprise thin-film transistors (TFTs).

[0003] Complex pixel arrangements, comprising many devices, such as, e.g., TFTs, require considerably circuit area, hereby limiting the achievable resolution of the display. When one tries to achieve higher resolutions, these complex pixel circuits may not fit in the available circuit area anymore. Therefore, different architectures may be required to fit the pixel inside the achievable area.

Summary

[0004] An objective of the present inventive concept is to provide a pixel arrangement allowing for more efficient use of the available circuit area.

[0005] To this end, according to a first aspect, there is provided a pixel arrangement integrable as part of a display, said display comprising a plurality of self-emitting pixel elements, said pixel arrangement comprising a pixel data storage block connected to a pixel data line and comprising a pixel data storage element; a pixel driver block for generating a pixel current; and a selection block connected to said pixel data storage block and to a plurality of selection lines, wherein said selection block is configured to switch said pixel current through a respective self-emitting pixel element of said plurality of self-emitting pixel elements based on said plurality of selection lines.

[0006] As "pixel arrangement" should be understood circuitry associated with one or more pixels or sub-pixels.

[0007] A pixel may be associated with or comprise a single self-emitting pixel element. In another case, a pixel may comprise several sub-pixels, each associated with or comprising a respective self-emitting pixel element. For example, the respective self-emitting pixel element of each sub-pixel may emit a different primary color. For example, there may be one sub-pixel for each of the colors red, green, and blue.

[0008] This, the pixel arrangement may correspond to one or more pixel circuits as understood in the art, i.e., the circuitry associated with the driving of a specific pixel or sub-pixel.

[0009] With "pixel data" should be understood data indicating an intended instantaneous brightness of the self-emitting pixel element. For example, and typically, the pixel data may be either an analog or a digital voltage. In the case of an analog voltage, increasing voltage may indicate a higher instantaneous brightness level of the self-emitting pixel element. In the case of a digital voltage, the digital voltage may indicate whether the self-emitting pixel element should be turned on or off. In this case, the self-emitting pixel element may be arranged to repeatedly turn on and off, e.g., through pulse width modulation (PWM).

[0010] As the selection block being configured to switch said pixel current through a respective self-emitting pixel element of said plurality of self-emitting pixel elements based on said plurality of selection lines should be understood the case of, e.g., the selection block providing a signal to a switching element located outside the selection block, for example in the pixel driver block.

[0011] Through the selection block being part of the pixel arrangement, parts of the pixel arrangement can be shared among different pixels, in particular involving several self-emitting pixel elements. Since multiple pixels may use the same pixel arrangement, the circuit area required may be split over multiple pixels, resulting in a smaller average pixel size, and thus allowing for higher resolution of the display.

[0012] According to an embodiment, the selection block is configured to connect the pixel driver block to a respective said self-emitting pixel element of said plurality of self-emitting pixel elements based on said plurality of selection lines. This allows for the sharing of the pixel driver block between several pixels and/or self-emitting pixel elements, allowing for further saving of circuit area, and thus for higher display resolution.

[0013] According to an embodiment, said selection block comprises a plurality of logic gates, wherein an output of a logic gate of said plurality of logic gates controls a switch element, such as a transistor, connected in series with a self-emitting pixel element of said plurality of self-emitting pixel elements. This is a particularly beneficial way of implementing the selection block.

[0014] According to an embodiment, said pixel arrangement comprises a plurality of pixel driver blocks, each connected to a respective self-emitting pixel element of said plurality of self-emitting pixel elements and wherein said selection block is configured to switch said pixel data storage block to a pixel driver block of said plurality of pixel driver blocks based on said plurality of selection lines. This allows for individual control of each self-emitting pixel element. For example, each self-emitting pixel element can be turned on at the same time and may be individually calibrated or compensated with regard to, e.g., current.

[0015] According to an embodiment, said selection block comprises a logic gate directly input from said pixel data storage element of said pixel data storage block. This allows for the logic gate of the selection block to act as a buffer stage for the pixel data storage element, removing any need for a separate buffer stage in the pixel data storage element, further saving on circuit area.

[0016] According to an embodiment, said selection block comprises a plurality of logic gates, wherein each

pixel driver block of said plurality of pixel driver blocks is connected to an output of a respective logic gate of said plurality of logic gates. This is a particularly beneficial way of implementing the selection block.

[0017] According to an embodiment, each pixel driver block of said plurality of pixel driver blocks comprises a respective driver-side pixel data storage element input from said selection block. Through each driver-side pixel data storage element keeping pixel data also at a time where the selection block has not selected corresponding to the self-emitting pixel element, this allows for all self-emitting pixel elements connected to the pixel element to be driven simultaneously.

[0018] According to an embodiment, said pixel data storage block comprises a plurality of pixel data storage elements each connected to said selection block and corresponding to a respective pixel. This may further save on circuit area.

[0019] According to an embodiment, said pixel data storage block comprises an input block connected to said pixel data line; and a latch transistor controlled by a latch line and connected to said input block and to said pixel data storage element. This is a particularly simple way of implementing the pixel data storage block.

[0020] According to an embodiment, said pixel data storage block further comprises a buffer stage input from said pixel data storage element and connected to said selection block.

[0021] According to an embodiment, said pixel data said buffer stage is a logic gate further input from a reset line. This allows for simultaneous resetting of all self-emitting pixel elements associated with the pixel arrangement through the reset line.

[0022] According to an embodiment, each said pixel driver block comprises a current mirror connected to a pixel current data line for setting the respective said pixel current. This is a particularly beneficial way of implementing the pixel driver block.

[0023] According to a second aspect, there is provided a display comprising one or more pixel arrangements according to the first aspect and the plurality of self-emitting pixel elements. This aspect may generally present the same or corresponding advantages as the first aspect.

Brief description of the drawings

[0024] The above, as well as additional objects, features and advantages of the present inventive concept, will be better understood through the following illustrative and non-limiting detailed description, with reference to the appended drawings. In the drawings like reference numerals will be used for like elements unless stated otherwise.

[0025] Figs 1, 2, 3, 4, 5, 6, 7, and 8 show respective pixel arrangements.

Detailed description

[0026] Fig. 1 schematically shows part of a display 200. Comprised in the display is a pixel arrangement 100. Thus the pixel arrangement 100 forms part of, and is integrable into, the display 200.

[0027] Any display 200 referred to throughout this disclosure may comprise self-emitting pixel elements and may as such, for example, be an AMOLED display, an AMLED display, or an AMμLED display. Thus, the display 200 may be an active matrix (AM) display. Any self-emitting pixel element 108 to which is referred throughout this disclosure may, for example, be an LED, OLED, or μLED.

[0028] For example, the display 200 may be a TV, and in particular a large TV, for example usable as part of a tiled arrangement. In another example, the display 200 may be an LED or μLED wall.

[0029] Turing back to Fig. 1, the pixel arrangement 100 comprises a pixel data storage block 102, a selection block 104, and a pixel driver block 106. Further, the display 200 comprises a plurality of self-emitting pixel elements 108.

[0030] The pixel data storage block 102 is connected to a pixel data line $data_{PWM}$.

[0031] The pixel data storage block comprises a pixel data storage element 110. As known per se in the art, such a pixel data storage element 110 may store pixel data related to a pixel. The pixel data may relate to an instantaneous luminosity intended to emanate from a self-emitting pixel element 108. For example, the pixel data may be a binary digit indicating whether a corresponding self-emitting pixel element 108 should be lit, or not.

[0032] The pixel data storage element 110 may, for example, be a capacitor, a logic gate, a latch, a flip-flop, or similar, as generally known per se in the art. Further examples and elaborations regarding the pixel data storage element 110 will be provided below.

[0033] As shown in Fig. 1, the pixel data storage block 102 may be connected to and/or output to the selection block 104.

[0034] In particular, the pixel data storage block 102 may be connected and/or output to a selector 105 forming part of the selection block 104. The selection block 104 is connected to the pixel data storage block 102 through a selection block input line 112. Thus, the selection block 104 may be input from the pixel data storage block 102.

[0035] The pixel driver block 106 is configured to generate a pixel current suitable for driving one or more self-emitting pixel elements 108, as known per se in the art. As shown in Fig. 1, the pixel-driving block may be connected to the selection block 104 through a pixel current line 107.

[0036] Further, the selection block 104 is connected to a plurality of selection lines. In the example of Fig. 1 there are two selection lines s_1, s_2, corresponding to the addressing, through respective binary signals on each of

the selection lines s_1, s_2, to addressing the four self-emitting pixel elements 108. Alternatively, there may be one selection line corresponding to each self-emitting pixel element 108.

[0037] As shown in the example of Fig. 1, within the selection block 104, the selector 105 may be connected to a plurality of selector output lines 114. Further, each selector output line 114 may be input to a respective switch element 116.

[0038] Further, each switch element 116 may be connected to the pixel current line 107. Thus, the selection block 104 may be connected to the pixel driver block 106.

[0039] Further, each switch element 116 may output to a respective self-emitting pixel element 108.

[0040] Each switch element 116 may be configured to pass a pixel current from the pixel current line 107 to the respective self-emitting pixel element 108 based on a signal on the respective selector output line 114. The switch element may be a transistor, logic element or other suitable block or component as generally known in the art.

[0041] In the example of Fig. 1 there are four selector output lines 114 and four switch elements 116, corresponding to the four self-emitting pixel elements 108 connected to the pixel driver block 106. Thus, there may be as many switch elements 116 and/or selector output lines 114 as there are self-emitting pixel elements associated with the selection block 104.

[0042] Through the above arrangement, the selection block is configured to, based on the selection lines s_1, s_2, connect the pixel data storage block 102 to one of the selector output lines 114. Thereby, a pixel current generated in the pixel driver block 106 may be output to a self-emitting pixel element 108 corresponding to the selection block output line 114 based on the pixel data of the pixel data storage element 110 of the pixel data storage block 102.

[0043] Thus, the selection block 104 may be configured to switch the resulting pixel current through the respective self-emitting pixel element 108 of the plurality of self-emitting pixel elements 108 based on the plurality of selection lines s_1, s_2.

[0044] However, the above arrangement should only be seen as an example and the skilled person could equally contemplate other arrangements for the selection block being configured to switch the pixel current through a respective self-emitting pixel element of the plurality of self-emitting pixel elements based on the plurality of selection lines.

[0045] Fig. 2 schematically shows a specific implementation of the pixel arrangement 100 of Fig. 1, forming part of the display 200. Specific examples of implementing the pixel data storage block 102, the selection block 104, and the pixel driver block 106 are disclosed. However, as the skilled person would understand, each such implementation of the pixel data storage block 102, the selection block 104, and/or the pixel driver block 106 may be independently modified and is not intrinsically technically linked to the others.

[0046] As shown in Fig. 2, the pixel data storage block 102 may comprise a pixel data storage element 110 in the form of a capacitor.

[0047] As shown in Fig. 2, the pixel data storage block 102 may be connected to pixel data lines $data_{PWM, i}$ and $data_{PWM, i-1}$ and to a clock signal clk. In particular, the pixel data storage block 102 may comprise a flip-flop FF 118 input from the clock signal clk and from the pixel data line $data_{PWM, i-1}$. Further, the flip-flop 118 may be output to the pixel data line $data_{PWM, i}$.

[0048] Further, the pixel data storage block 102 may comprise a latch transistor 120 controlled by a latch line and connected between the flip-flop 118 and the pixel data storage element 110.

[0049] Thus, the flip-flop 118 may form an input block connected to the pixel data line $data_{PWM, i-1}$ and the latch transistor 120 may be controlled by the latch line and connected to the input block (flip-flop) 118 and to the pixel data storage element 110.

[0050] The following discloses an example of how pixel data may be read into the display 200 comprising the pixel data storage block 102 comprising the pixel data storage element 110. However, as the skilled person would appreciate, other schemes for reading pixel data into the pixel data storage block 102 may be equally contemplated by the skilled person.

[0051] Pixel data may be read into the flip-flop 118 from the pixel data line $data_{PWM, i-1}$ upon assertion of the clock signal clk. The $data_{PWM, i-1}$ may be connected to the $data_{PWM, i}$ line of another pixel data storage block 102 comprised in the display 200, and so on, the pixel data storage blocks 102 thereby forming a flip-flop chain. Hereby, pixel data may be successively read into the flip-flop chain on successive assertion of the clk line. In other words, data may be written on the $data_{PWM, i-1}$ line of a first pixel data storage block 102, and then the data may be shifted, to the flip-flop 118 of the next pixel data storage block 102 upon activating the clk line again, while reading in the new data in the first flip-flop 118. This may continue until data has been read into all pixel-data storage blocks 102 of the flip-flop chain.

[0052] Finally, the latch line may be asserted simultaneously for all pixel data storage blocks 102, each latch transistor 120 thereby leading the pixel data stored in the flip-flop 118 to the pixel data storage element 110.

[0053] It should be noted that the flip-flop 118 and the latch transistor 120 and are not required in present inventive concept and other arrangement for reading pixel data into the pixel-data storage block 102 may equally be contemplated by the skilled person, as generally known in the art.

[0054] As shown in Fig.2, the selector 105 may comprise a plurality of NAND-gates 122 each input from the pixel data storage element 110 of the pixel data storage block 102 and from a respective enable line EN1, EN2, EN3, EN4, the enable lines EN1, EN2, EN3, EN4 functioning as selection lines for the selector 105 formed by

the NAND gates 122. Further, each NAND-gate 122 may be output to a respective selector output line 114.

[0055] Further, each switch element 116 may be a transistor 116 controlled by a respective selector output line 114 and connected between the pixel current line 107 and a respective self-emitting pixel element 108.

[0056] As the skilled person would understand, other arrangements comprising other logic gates than NAND gates are equally possible.

[0057] Thus, the pixel arrangement 100 of Fig. 2 comprises a plurality of logic gates 122, wherein an output on a selector output line 114 of a logic gate 122 of the plurality of logic gates 122 controls a transistor 116 connected in series with a self-emitting pixel element 108 of the plurality of self-emitting pixel elements 108.

[0058] The pixel driver block 106 may, as shown in Fig.2, comprise a current-mirror circuit. The specific current-mirror circuitry of Fig.2 should only be seen as an example, and the skilled person could equally contemplate other current-mirror circuits, as generally known in the art.

[0059] The current-mirror may comprise a first current mirror transistor 124 connected to a supply voltage V_{DD} and in series with a primary current path 128 and a second current mirror transistor 126 connected to the supply voltage V_{DD} and in series with a secondary current path 130. The gate of the first current mirror transistor 124 is connected to the gate of the second current mirror transistor 126. Further, a current mirror capacitor 132 is connected between the supply voltage V_{DD} and the gates of the first current mirror transistor 124 and the second current mirror transistor 126.

[0060] A first current-setting transistor 134 may be connected in series with the first current mirror transistor 124 in the primary current path 128. The first current-setting transistor 134 may be controlled by a current selection line seli 136 and connected between the primary current path 128 and a reference current line $data_i$ 138 leading to a reference current source 140.

[0061] A second current-setting transistor 142 may also controlled by the selection line seli 136, and connected between, on the one hand, the gates of the first current mirror transistor 124 and the second current mirror transistor 126 and the current mirror capacitor 132, and, on the other hand, the reference current line.

[0062] Through this arrangement, the current of the current mirror may be set through the reference current line 138 when asserting the current selection line 136.

[0063] Thus, the pixel driver block 106 comprises a current mirror connected to a pixel current data line 138, in the form of the reference current line 138, for setting the respective said pixel current.

[0064] Fig. 3 schematically shows part of a display 200. Comprised in the display is a pixel arrangement 100. Thus the pixel arrangement 100 forms part of, and is integrable into, the display 200.

[0065] The pixel arrangement 100 comprises a pixel data storage block 102, a selection block 104, and a plurality of pixel driver blocks 106. Further, the display 200 comprises a plurality of self-emitting pixel elements 108.

[0066] The pixel data storage block 102 is connected to a pixel data line $data_{PWM}$.

[0067] The pixel data storage block comprises a pixel data storage element 110. As known per se in the art, such a pixel data storage element 110 may store pixel data related to a pixel. The pixel data may relate to an instantaneous luminosity intended to emanate from a self-emitting pixel element 108. For example, the pixel data may be a binary digit indicating whether a corresponding self-emitting pixel element 108 should be lit, or not.

[0068] The pixel data storage element 110 may, for example, be a capacitor, a logic gate, a latch, a flip-flop, or similar, as generally known per se in the art.

[0069] As shown in Fig. 3, the pixel data storage block 102 may be connected to and/or output to the selection block 104. The selection block 104 is connected to the pixel data storage block 102 through a selection block input line 112. Thus, the selection block 104 may be input from the pixel data storage block 102.

[0070] Each pixel driver block 106 is configured to generate a pixel current suitable for driving one or more self-emitting pixel elements 108, as known per se in the art, and output the pixel current to a pixel current line 107.

[0071] Further, the selection block 104 is connected to a plurality of selection lines. In the example of Fig. 3 there are two selection lines s_1, s_2, corresponding to the addressing, through respective binary signals on each of the selection lines s_1, s_2, to addressing the four self-emitting pixel elements 108. Alternatively, there may be one selection line corresponding to each self-emitting pixel element 108.

[0072] As shown in the example of Fig. 3, the selection block 104 may be connected to a plurality of selector output lines 114. Further, each selector output line 114 may be input to a respective pixel driver block 106.

[0073] In the example of Fig. 3, there are four selector output lines 114 and four pixel driver blocks 106, corresponding to the four self-emitting pixel elements 108. Thus, there may be as many pixel driver blocks 106 and/or selector output lines 114 as there are self-emitting pixel elements 108 associated with the selection block 104.

[0074] Each pixel driver block 106 may be configured to pass a generated pixel current through the respective pixel current line 107 to the respective self-emitting pixel element 108 based on a signal on the respective selector output line 114. As shown in Fig. 3, this may be accomplished through the pixel driver block comprising a switch element 116 controlled by the respective selector output line 114.

[0075] The switch element 116 may be a transistor, logic gate or other suitable block or component as generally known in the art. Each switch element 116 may be configured to pass the pixel current from the pixel current line 107 to the respective self-emitting pixel element 108

based on a signal on the respective selector output line 114. Alternatively, each switch element 116 may be comprised in the selection block 104.

[0076] Through the above arrangement, the selection block is configured to, based on the selection lines s_1, s_2,connect the pixel data storage block 102 to one of the selector output lines 114. Thereby, a pixel current generated in the pixel driver block 106 may be output to a self-emitting pixel element 108 corresponding to the selector block output line 114 based on the pixel data of the pixel data storage element 110 of the pixel data storage block 102.

[0077] Thus, the selection block 104 may be configured to, through a respective selector output line 114, switch the pixel current generated in the respective pixel driver block through the respective self-emitting pixel element 108 of the plurality of self-emitting pixel elements 108 based on the plurality of selection lines s_1, s_2.

[0078] Through the pixel arrangement of Fig. 3, the pixel data storage block 102 may be shared between a plurality of different self-emitting pixel elements 108, in the example of Fig. 3 four different self-emitting pixel elements 108, which may correspond to four different pixels and/or sub-pixels. The output of the pixel data storage block 102 is connected to the selection block 104. Depending on the values of the selection block selection signals on selection lines s_1, s_2, the output of the pixel data storage block 102 will be passed on to a different pixel driver block 106 based on the selection block 104.

[0079] However, the above arrangement should only be seen as an example and the skilled person could equally contemplate other arrangements for the selection block being configured to switch the pixel current through a respective self-emitting pixel element of the plurality of self-emitting pixel elements based on the plurality of selection lines.

[0080] In other words, the pixel arrangement 100 comprises a plurality of pixel driver blocks 106, each connected to a respective self-emitting pixel element 108 of the plurality of self-emitting pixel elements 108 and the selection block 104 is configured to switch the pixel data storage block 102 to a pixel driver block 106 of the plurality of pixel driver blocks 106 based on the plurality of selector output lines 114, depending on the values on selection lines s_1, s_2.

[0081] Fig. 4 schematically shows a specific implementation of the pixel arrangement 100 of Fig. 3, forming part of the display 200. Specific examples of implementing the pixel data storage block 102, the selection block 104, and the pixel driver blocks 106 are disclosed. However, as the skilled person would understand, each such implementation of the pixel data storage block 102, the selection block 104, and/or the pixel driver block 106 may be independently modified and is not intrinsically technically linked to the others.

[0082] As shown in Fig. 4, the pixel data storage block 102 may comprise a pixel data storage element 110 in the form of a capacitor.

[0083] Further as shown in Fig. 4, the pixel data storage block 102 may be connected to pixel data line $data_{PWM, i}$ and $data_{PWM, i-1}$ and to a clock signal clk. In particular, the pixel data storage block 102 may comprise a flip-flop FF 118 input from the clock signal clk and from the pixel data line $data_{PWM, i-1}$. Further, the flip-flop 118 may be output to the pixel data line $data_{PWM, i}$.

[0084] Further, the pixel data storage block 102 may comprise a latch transistor 120 controlled by a latch line and connected between the flip-flop 118 and the pixel data storage element 110.

[0085] Thus, the flip-flop 118 may form an input block connected to the pixel data line $data_{PWM, i-1}$ and the latch transistor 120 is controlled by the latch line and connected to the input block (flip-flop 118) and to the pixel data storage element 110.

[0086] Pixel data may be read into the display 200 comprising the pixel data storage block 102 comprising the pixel data storage element 110 as elaborated upon in detailed above in conjunction with Fig. 2.

[0087] It should be noted that the flip-flop 118 and the latch transistor 120 are not required in present inventive concept and other arrangements for reading pixel data into the pixel-data storage block 102 may equally be contemplated by the skilled person, as generally known in the art.

[0088] The logic gate 402 may function as a buffer stage 402 from the pixel data storage element 110 and connected to the selection block 104.

[0089] As shown, the logic gate 402 may be a NAND gate 402. However, as the skilled person would understand, other logic gates would equally be possible, as generally known in the art.

[0090] The NAND gate may as shown in Fig. 4 comprise a first logic gate transistor 404 controlled by the pixel data storage element 110 and connected between a logic supply voltage $V_{,DD,logic}$ and a central node 401.

[0091] Further, the logic gate 402 may comprise a second logic gate transistor 406 controlled by a reset line RST and connected between the logic supply voltage $V_{,DD,logic}$ and the central node 401.

[0092] Further, connected in series between the central node 401 and logic ground $V_{GNG,logic}$, the logic gate 402 may comprise a third logic gate transistor 408 controlled by the reset line RST and a fourth logic gate transistor 410 controlled by the pixel data storage element 110.

[0093] Further, the central node 401 may be connected to the selection block input line 112, connecting the pixel data storage block 102 to the selection block 104.

[0094] The selection block 104 may, as shown in Fig. 4, comprise a plurality of logic gates 412.

[0095] In the example of Fig. 4, each logic gate 412 is a NAND gate. Arrangements using other kinds of logic gates are equally possible.

[0096] Each pixel driver block 106 of the plurality of pixel driver blocks 106 is connected to a respective output (selector output line 114) of a respective logic gate 412

of the plurality of logic gates 412 in the selection block 104.

[0097] As shown in Fig. 4, each logic gate 412 may be input from the selection block input line 112, and from a plurality of selection lines, in the example of Fig. 4 two selection lines s1, s2.

[0098] A pixel driver block 106 may, as shown as one example in Fig. 4, comprise a current-mirror circuit. The specific current-mirror circuitry of Fig. 4 should only be seen as an example, and the skilled person could equally contemplate other current-mirror circuits, as generally known in the art.

[0099] The current-mirror may be configured as elaborated upon in detail above in conjunction with Fig. 2. Through that arrangement, the current of the current mirror may be set through the reference current line 138 when asserting the current selection line 136.

[0100] Thus, the pixel driver block 106 comprises a current mirror connected to a pixel current data line, in the form of the reference current line 138, for setting the respective said pixel current.

[0101] Further, each switch element 116 may be a transistor controlled by the respective selector output line 114 and connected between the pixel current line 107 and the respective self-emitting pixel element 108.

[0102] Thus, the pixel arrangement 100 of Fig. 4 comprises a plurality of logic gates 412, wherein an output on selector output line 114 of a logic gate 412 of the plurality of logic gates 412 controls a transistor (switch element 116) connected in series with a self-emitting pixel element 108 of the plurality of self-emitting pixel elements 108.

[0103] Fig. 5 schematically shows another specific implementation of the pixel arrangement 100 of Fig. 3, forming part of the display 200. Specific examples of implementing the pixel data storage block 102, the selection block 104, and the pixel driver blocks 106 are disclosed. However, as the skilled person would understand, each such implementation of the pixel data storage block 102, the selection block 104, and/or the pixel driver block 106 may be independently modified and is not intrinsically technically linked to the others.

[0104] As shown in Fig. 5, the pixel data storage block 102 may comprise a pixel data storage element 110 in the form of a capacitor.

[0105] Further as shown in Fig. 5, the pixel data storage block 102 may be connected to pixel data line $data_{PWM, i}$ and $data_{PWM, i-1}$ and to a clock signal clk. In particular, the pixel data storage block 102 may comprise a flip-flop FF 118 input from the clock signal clk and from the pixel data line $data_{PWM, i-1}$. Further, the flip-flop 118 may be output to the pixel data line $data_{PWM, i}$.

[0106] Further, the pixel data storage block 102 may comprise a latch transistor 120 controlled by a latch line and connected between the flip-flop 118 and the pixel data storage element 110.

[0107] Thus, the flip-flop 118 may form an input block 118 connected to the pixel data line $data_{PWM, i-1}$ and the latch transistor 120 is controlled by the latch line and connected to the input block (flip-flop 118) and to the pixel data storage element 110.

[0108] Pixel data may be read into the display 200 comprising the pixel data storage block 102 comprising the pixel data storage element 110 as elaborated upon in detailed above in conjunction with Fig. 2.

[0109] It should be noted that the flip-flop 118 and the latch transistor 120 and are not required in present inventive concept and other arrangement for reading pixel data into the pixel-data storage block 102 may equally be contemplated by the skilled person, as generally known in the art.

[0110] As shown in Fig. 5, the selection block 104 may comprise a plurality of logic gates 412. Each logic gate 412 may be directly input from the pixel data storage element 110 of the pixel data storage block 102.

[0111] In the example of Fig. 5, each logic gate 412 is a NAND gate. Arrangements using other kinds of logic gates are equally possible.

[0112] As shown with one example in Fig. 5, each such logic gate 412, may comprise a first logic gate transistor 404 controlled by the pixel data storage element 110 of the pixel data storage element of the pixel data storage block 102 through the selection block input line 112 and connected between a logic supply voltage $V_{,DD,logic}$ and a central node 401.

[0113] Further, the logic gate 412 may comprise a second logic gate transistor 406 controlled by an enable line EN1 and connected between the logic supply voltage $V_{,DD,logic}$ and the central node 401.

[0114] Further, connected in series between the central node 401 and logic ground $V_{GNG,logic}$, the logic gate 402 may comprise a third logic gate transistor 408 controlled by the selection line, and a fourth logic gate transistor 410 controlled by the pixel data storage element 110 through the selection block input line 112.

[0115] Further, the central node 401 may be connected to the selector output line 114, connecting the selection block 104 to the respective pixel driver block 106.

[0116] Thus, each pixel driving block 106 of the plurality of pixel driver blocks 106 is connected to a respective output on selector output line 114 of a respective logic gate 412 of the plurality of logic gates 412 in the selection block 104.

[0117] Further, as shown in Fig. 5, each logic gate 412 may be input from the selection block input line 112, and a respective enable line EN1, EN2, EN3, EN4.

[0118] A pixel driver block 106 may, as shown as one example in Fig. 5, comprise a current-mirror circuit. The specific current-mirror circuitry of Fig. 5 should only be seen as an example, and the skilled person could equally contemplate other current-mirror circuits, as generally known in the art.

[0119] The current-mirror may be configured as elaborated upon in detail above in conjunction with Fig. 2. Through that arrangement, the current of the current mirror may be set through the reference current line 138

when asserting the current selection line 136.

[0120] Thus, the pixel driver block 106 comprises a current mirror connected to a pixel current data line, in the form of the reference current line 138, for setting the respective said pixel current.

[0121] Further, each switch element 116 may be a transistor 116 controlled by the respective selector output line 114 and connected between the pixel current line 107 and the respective self-emitting pixel element 108.

[0122] Thus, the pixel arrangement 100 of Fig. 5 comprises a plurality of logic gates 412, wherein an output 114 of a logic gate 412 of the plurality of logic gates 412 controls a transistor (switch element 116) connected in series with a self-emitting pixel element 108 of the plurality of self-emitting pixel elements 108.

[0123] Fig. 6 schematically shows part of a display 200. Comprised in the display is a pixel arrangement 100. Thus the pixel arrangement 100 forms part of, and is integrable into, the display 200.

[0124] The pixel arrangement 100 of Fig. 6 generally has identical features as disclosed above in conjunction with Fig. 3. Thus, the specific examples of pixel data storage blocks 102, selections blocks 104 and pixel driver blocks 106 are equally applicable to the pixel arrangement 100 of Fig. 6.

[0125] However, further to the pixel arrangement 100 of Fig. 3, the pixel arrangement 100 of Fig. 6 comprises a plurality of driver-side pixel data storage blocks 602, each comprising a driver-side pixel data storage element 604, wherein each driver-side pixel data storage block 602 and thereby driver-side pixel data storage element 604 is connected to a respective selector output line 114 between the selection block 104 and each respective pixel driver block 106. Thus, the driver-side pixel data storage block 602 and the driver-side pixel data storage element 604 is input from the selection block 104 and output to the respective pixel driver block 106.

[0126] The driver-side pixel data storage element may be considered to be comprised in the respective pixel driver block 106. The driver-side pixel data storage element 604 may, for example, be a capacitor, a logic gate, a latch, a flip-flop, or similar, as generally known per se in the art.

[0127] Fig. 7 schematically shows a specific implementation of the pixel arrangement 100 of Fig. 6, forming part of the display 200, comprising the pixel data storage block 102, the selection block 104, a plurality of pixel driver blocks 106.

[0128] As shown in Fig. 7, the pixel data storage block 102 may be identically arranged and connected to the selection block 104 as disclosed above in conjunction with, e.g., Figs 2 and 5.

[0129] Further, as shown with one example in Fig. 7, each pixel driver block 106 may be identically arranged and connected to the selection block 104 and to a respective self-emitting pixel element 108 as disclosed above, e.g., in conjunction with Figs 2 and 4.

[0130] As shown in Fig. 7, the selection block 104 may comprise a plurality of logic gates 122, in the example of Fig. 7, NAND-gates 122, each input from the pixel data storage element 110 of the pixel data storage block 102 though the selection block input line 112, and from a respective enable line EN1, EN2, EN3, EN4, the enable lines EN1, EN2, EN3, EN4 functioning as selection lines for the selection block 104 formed by the NAND gates 122. Further, each NAND-gate 122 may be output to a respective selector output line 114.

[0131] Each driver-side pixel data storage block 602 comprises a driver-side pixel data storage element 604 connected between a logic supply voltage $V_{DD,logic}$ and the switch transistor (switch element 116), in the form of a capacitor. Further, the driver-side pixel data storage block 602 comprises a driver-side pixel data storage block transistor 606 controlled by the respective enable line EN1, EN2, EN3, EN4 and connected between the respective selector output line 114 and the driver-side pixel data storage element 604.

[0132] Fig. 8 schematically shows part of a display 200. Comprised in the display is a pixel arrangement 100. Thus the pixel arrangement 100 forms part of, and is integrable into, the display 200.

[0133] The pixel arrangement 100 comprises a pixel data storage block 102, a selection block 104, and a pixel driver block 106. Further, the display 200 comprises a plurality of self-emitting pixel elements 108.

[0134] As shown in Fig. 8, the pixel data storage block 102 may comprise a flip-flop 118 identically arranged and connected to pixel data lines $data_{PWMi-1}$, $data_{PWMi}$ as disclosed above in conjunction with, e.g., Fig. 2.

[0135] Further the pixel data storage block 102 comprises a plurality of pixel data storage elements 110, each being a capacitor, and a plurality of latch transistors 120. Each latch transistor is controlled by the latch signal and connected between an output of the flip-flop 118 and to the selection block 104 through a respective selection block input line 112.

[0136] The selection block 104 comprises a plurality of logic gates 122 in the form of NAND gates 122, each connected to a respective pixel data storage element 110 of the pixel data storage block 102. Further, each NAND gate is connected to a respective enable line EN1, EN2, EN3, EN4. Further, each NAND gate outputs to a respective selector output line 114.

[0137] Further, as shown with one example in Fig. 8, each pixel driver block 106 may be identically arranged and connected to the selection block 104 through a respective selector output line 114 and to a respective self-emitting pixel element 108 as disclosed above, e.g., in conjunction with Figs 2 and 4.

[0138] Thus, the pixel data storage block comprises a plurality of pixel data storage elements 110 each connected to the selection block 104 and corresponding to a respective pixel.

[0139] In the above the inventive concept has mainly been described with reference to a limited number of examples. However, as is readily appreciated by a person

skilled in the art, other examples than the ones disclosed above are equally possible within the scope of the inventive concept, as defined by the appended claims.

[0140] In particular, although this description discloses a limited number of pixel circuits, it should be noted that many different embodiments are possible without going beyond the scope of the invention. For example, the scope of the present inventive concept is not limited to p-type transistor pixel circuits, but can also be applied to n-type or mixed (CMOS) transistor pixel circuits. Moreover, the present inventive concept is not limited to the disclosed pixel circuits, but can also be applied to more complex pixel circuits or to less complex pixel circuits, as contemplatable by the skilled person, within the scope of the claims.

[0141] Further, while all examples above are provided for selection blocks corresponding to four self-emitting pixel elements, the present inventive concept naturally is not limited to specifically four outputs of the selection block, but rather any plurality of outputs is equally possible. Furthermore, other embodiments and combination of circuit parts of different embodiments are possible, as well as modifying the circuits parts within the scope of the claims according to the skilled person's general knowledge.

Claims

1. A pixel arrangement (100) integrable as part of a display (200), said display (200) comprising a plurality of self-emitting pixel elements (108), said pixel arrangement (100) comprising:

   a pixel data storage block (102) connected to a pixel data line and comprising a pixel data storage element (110);
   a pixel driver block (106) for generating a pixel current; and
   a selection block (104) connected to said pixel data storage block and to a plurality of selection lines (s_1, s_2, EN1, EN2, EN3, EN4), wherein said selection block (104) is configured to switch said pixel current through a respective self-emitting pixel element (108) of said plurality of self-emitting pixel elements (108) based on said plurality of selection lines.

2. The pixel arrangement (100) of claim 1, wherein said selection block (104) is configured to connect said pixel driver block (106) to a respective said self-emitting pixel element (108) of said plurality of self-emitting pixel elements (108) based on said plurality of selection lines.

3. The pixel arrangement (100) of claim 2, wherein said selection block (104) comprises a plurality of logic gates (122), wherein an output of a logic gate (122) of said plurality of logic gates (122) controls a switch element (116) connected in series with a self-emitting pixel element (108) of said plurality of self-emitting pixel elements (108).

4. The pixel arrangement (100) of claim 1, wherein said pixel arrangement (100) comprises a plurality of pixel driver blocks (106), each connected to a respective self-emitting pixel element (108) of said plurality of self-emitting pixel elements (108) and wherein said selection block (104) is configured to switch said pixel data storage block (102) to a pixel driver block (106) of said plurality of pixel driver blocks (106) based on said plurality of selection lines.

5. The pixel arrangement (100) of any one of claims 1-4, wherein said selection block (104) comprises a logic gate (122) directly input from said pixel data storage element (110) of said pixel data storage block (102).

6. The pixel arrangement (100) of any one of claims 4-5, wherein said selection block (104) comprises a plurality of logic gates (122), wherein each pixel driver block (106) of said plurality of pixel driver blocks (106) is connected to an output of a respective logic gate (122) of said plurality of logic gates (122).

7. The pixel arrangement (100) of any one of claims 4-6, wherein each pixel driver block (106) of said plurality of pixel driver blocks (106) comprises a respective driver-side pixel data storage element (604) input from said selection block (104).

8. The pixel arrangement (100) of any one of claims 1-7, wherein said pixel data storage block (102) comprises a plurality of pixel data storage elements (110) each connected to said selection block (104) and corresponding to a respective pixel.

9. The pixel arrangement (100) of any one of claims 1-8, wherein said pixel data storage block comprises:

   an input block (118) connected to said pixel data line; and
   a latch transistor (120) controlled by a latch line and connected to said input block (118) and to said pixel data storage element (110).

10. The pixel arrangement (100) of claim 9, wherein said pixel data storage block further comprises:
    a buffer stage (402) input from said pixel data storage element (110) and connected to said selection block (104).

11. The pixel arrangement (100) of claim 10, wherein said buffer stage (402) is a logic gate further input from a reset line.

12. The pixel arrangement (100) of any one of claims 1-11, wherein each said pixel driver block (106) comprises a current mirror connected to a pixel current data line for setting the respective said pixel current.

13. A display (200) comprising one or more pixel arrangements according to any one of claims 1-12 and said plurality of self-emitting pixel elements (108).

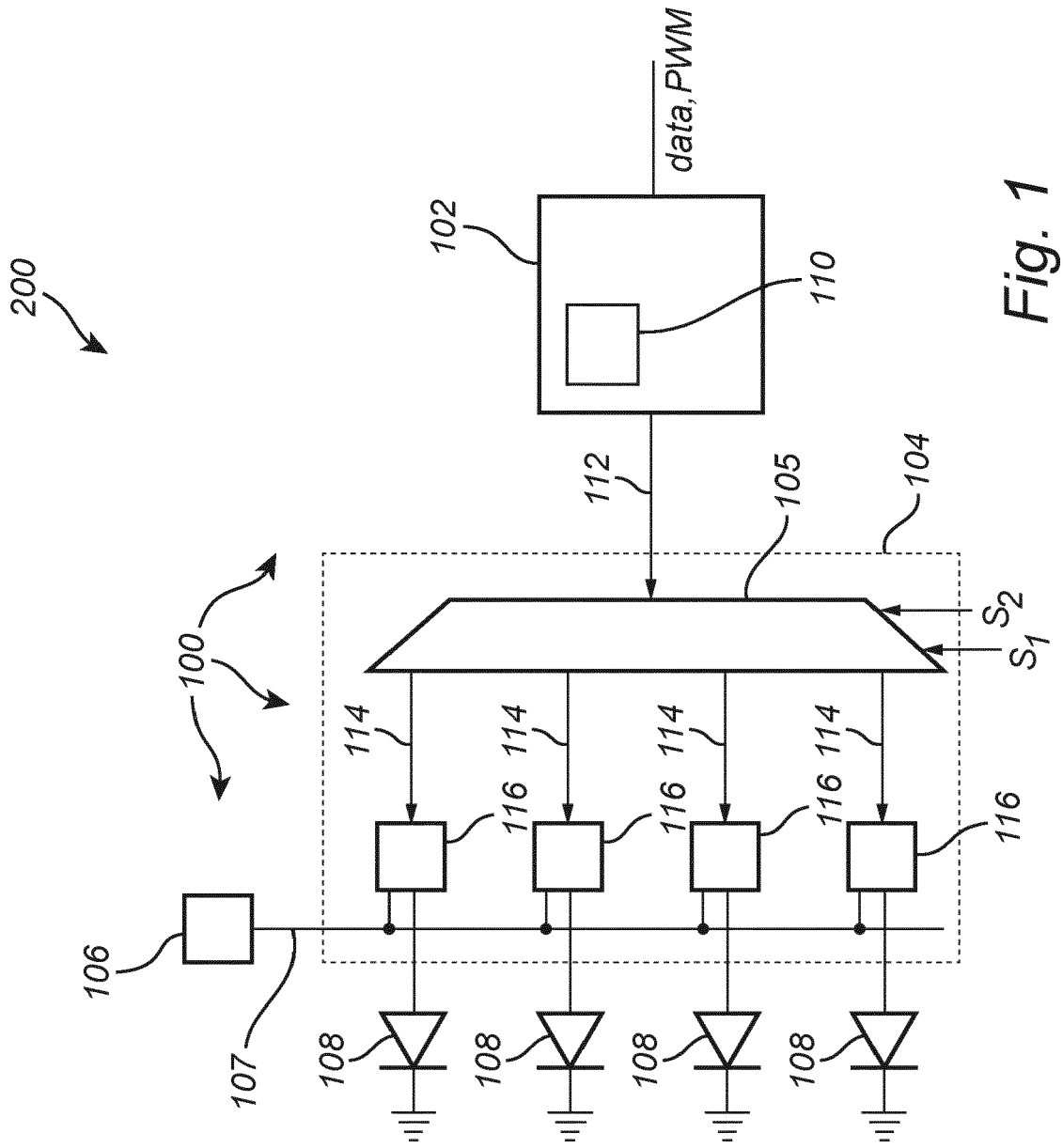
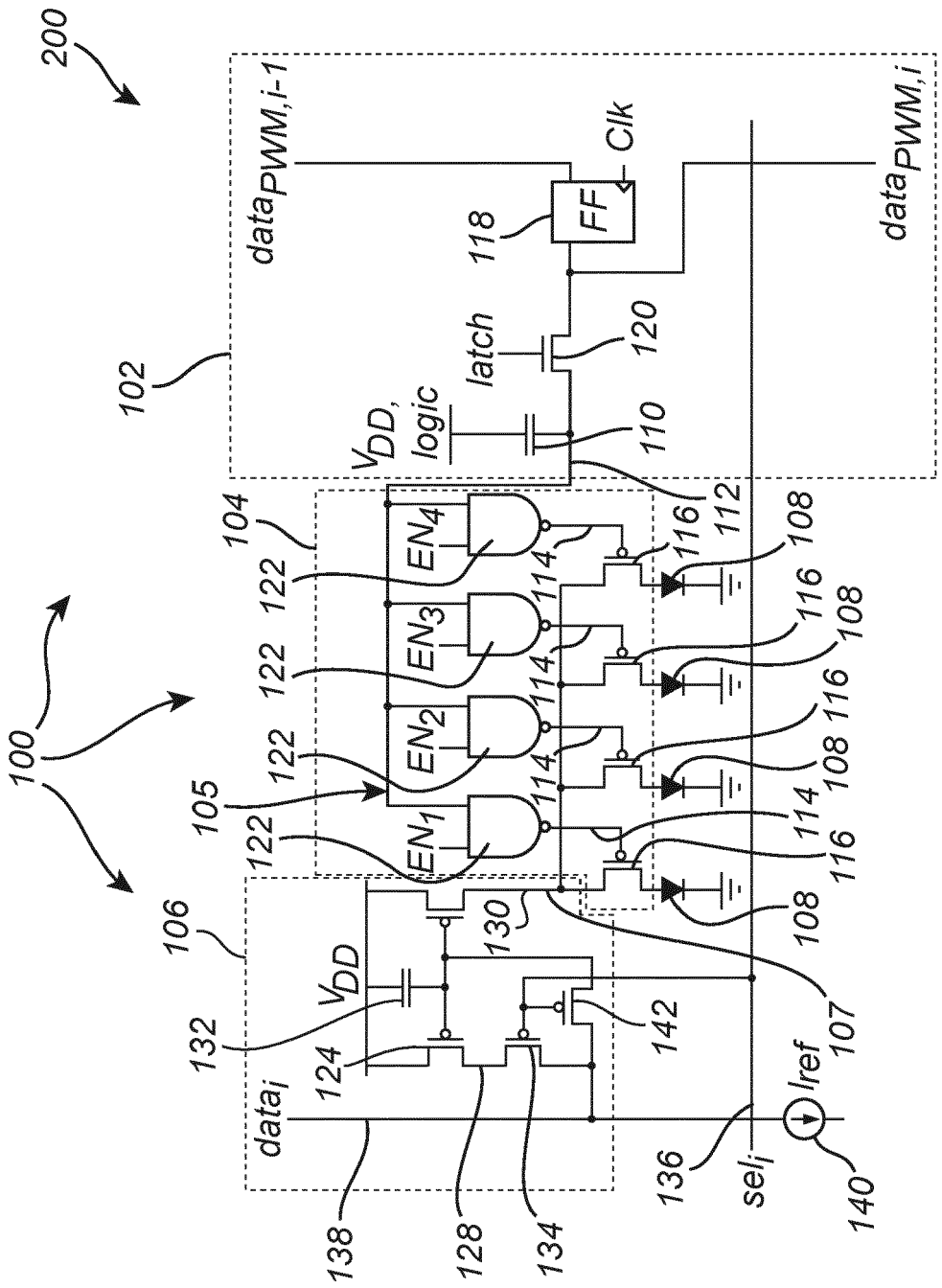


Fig. 1


200
100
102
104
105
106
107
108
110
112
114
116
118
120
122
124
128
130
132
134
136
138
140
142
$data_{PWM,i-1}$
$data_{PWM,i}$
Clk
FF
latch
V_{DD}, logic
EN_4
EN_3
EN_2
EN_1
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sel_i
Iref

Fig. 2

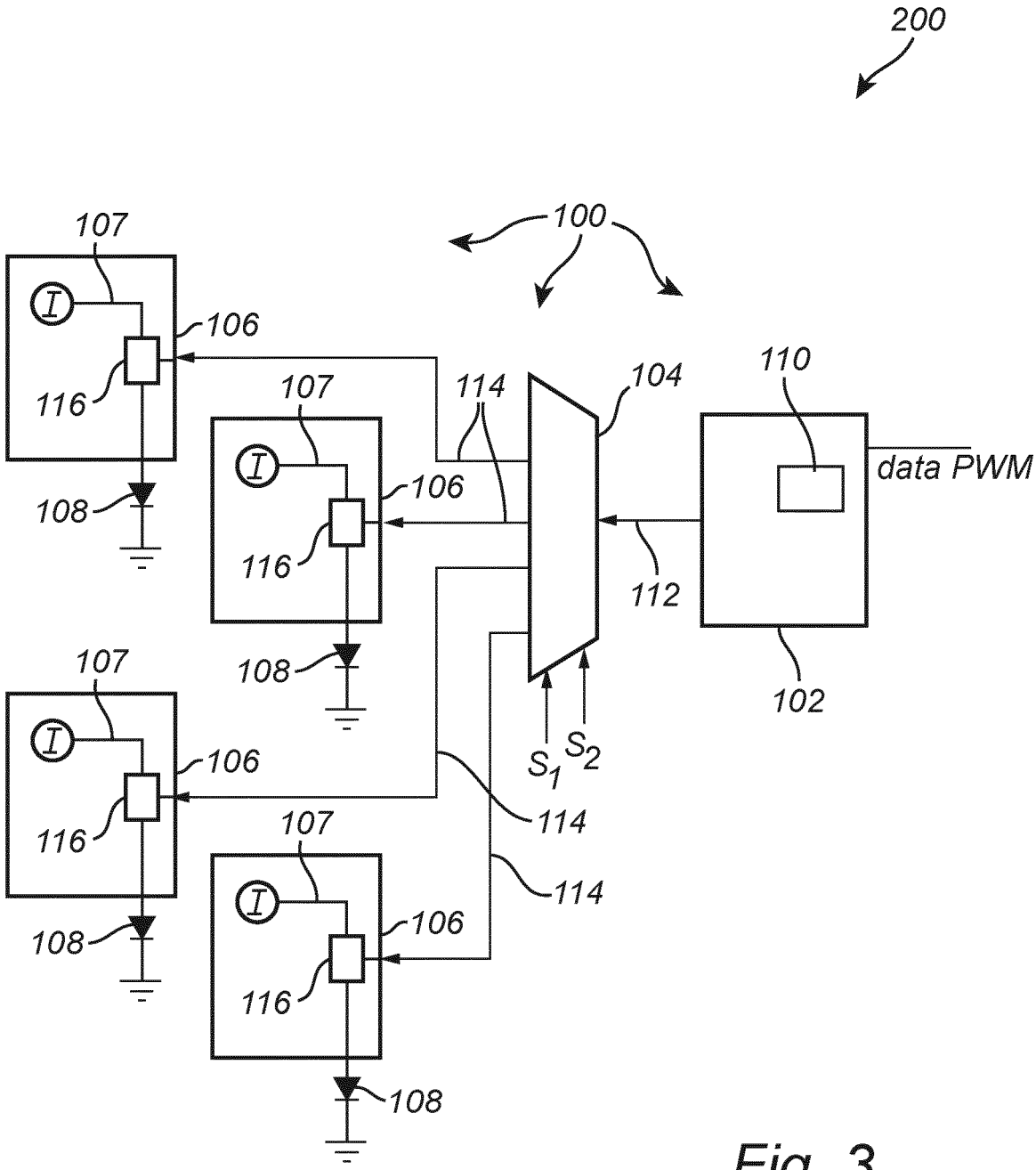
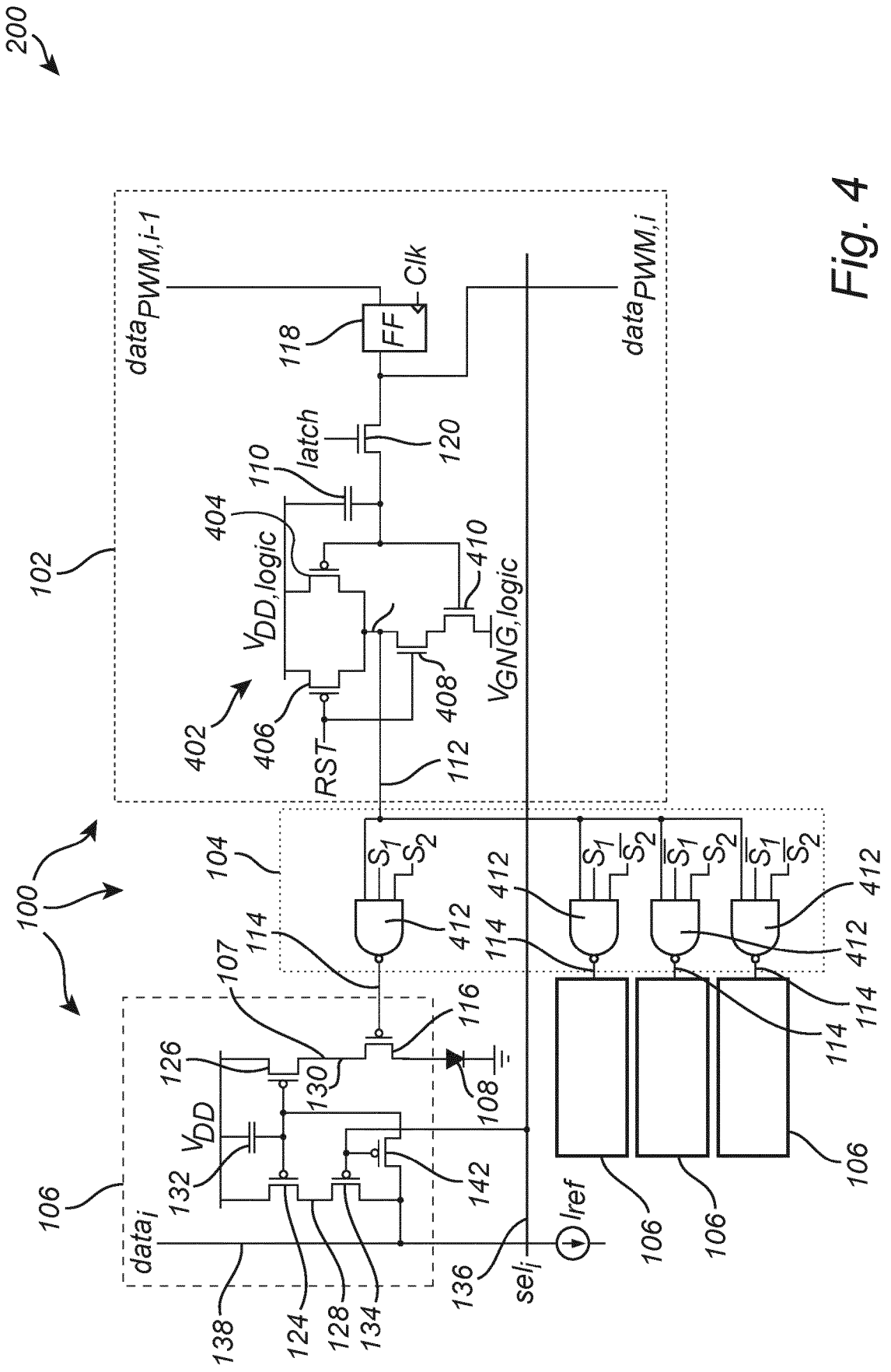


Fig. 3


200
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102
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107
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134
136
138
142
402
404
406
408
410
412
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sel_i
I_{ref}
V_{DD}
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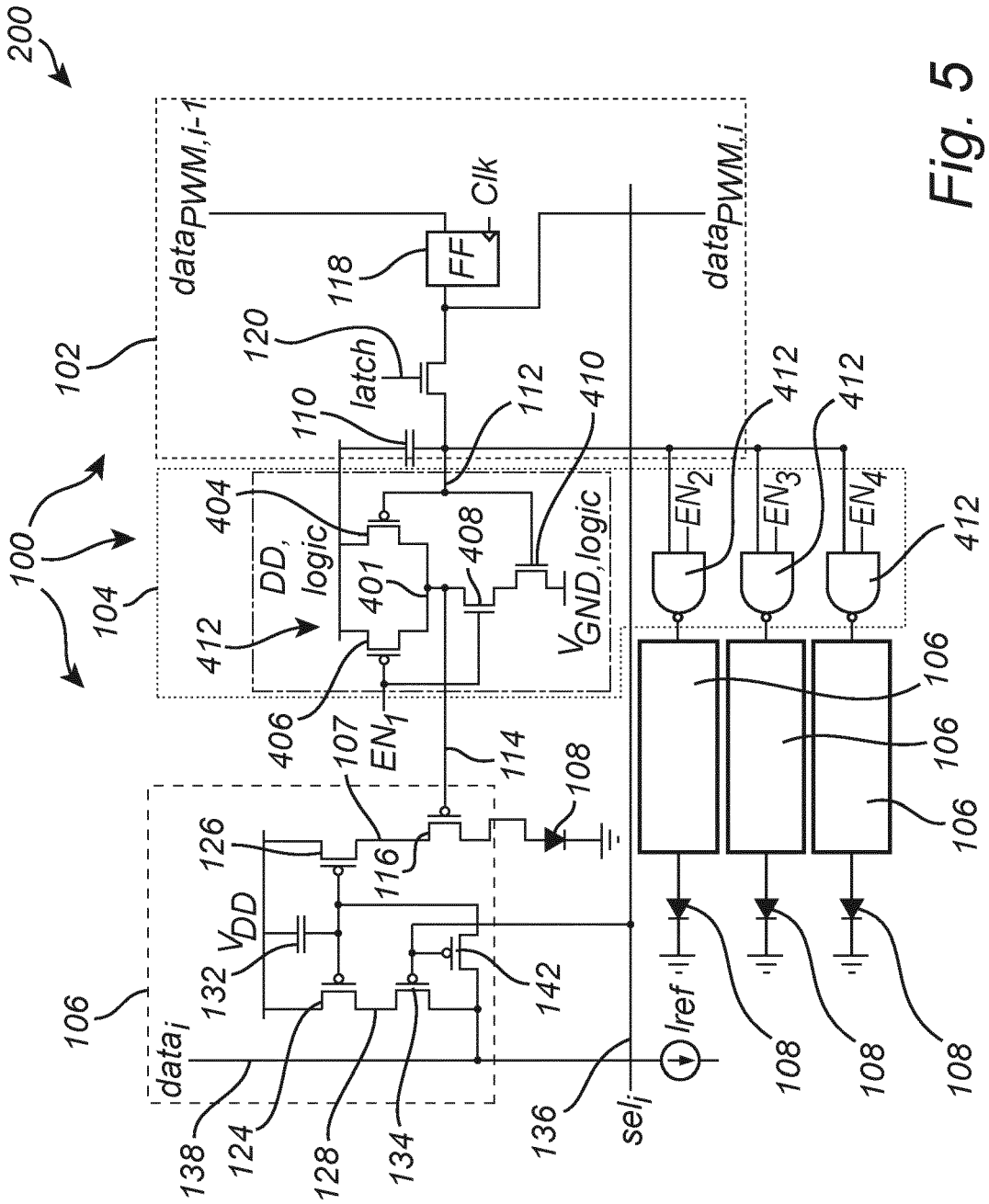
$V_{GNG,logic}$
RST
latch
FF
Clk
S_1
S_2

Fig. 4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V_{DD}
EN_1
EN_2
EN_3
EN_4
I_{ref}
sel_i
107
108
110
112
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132
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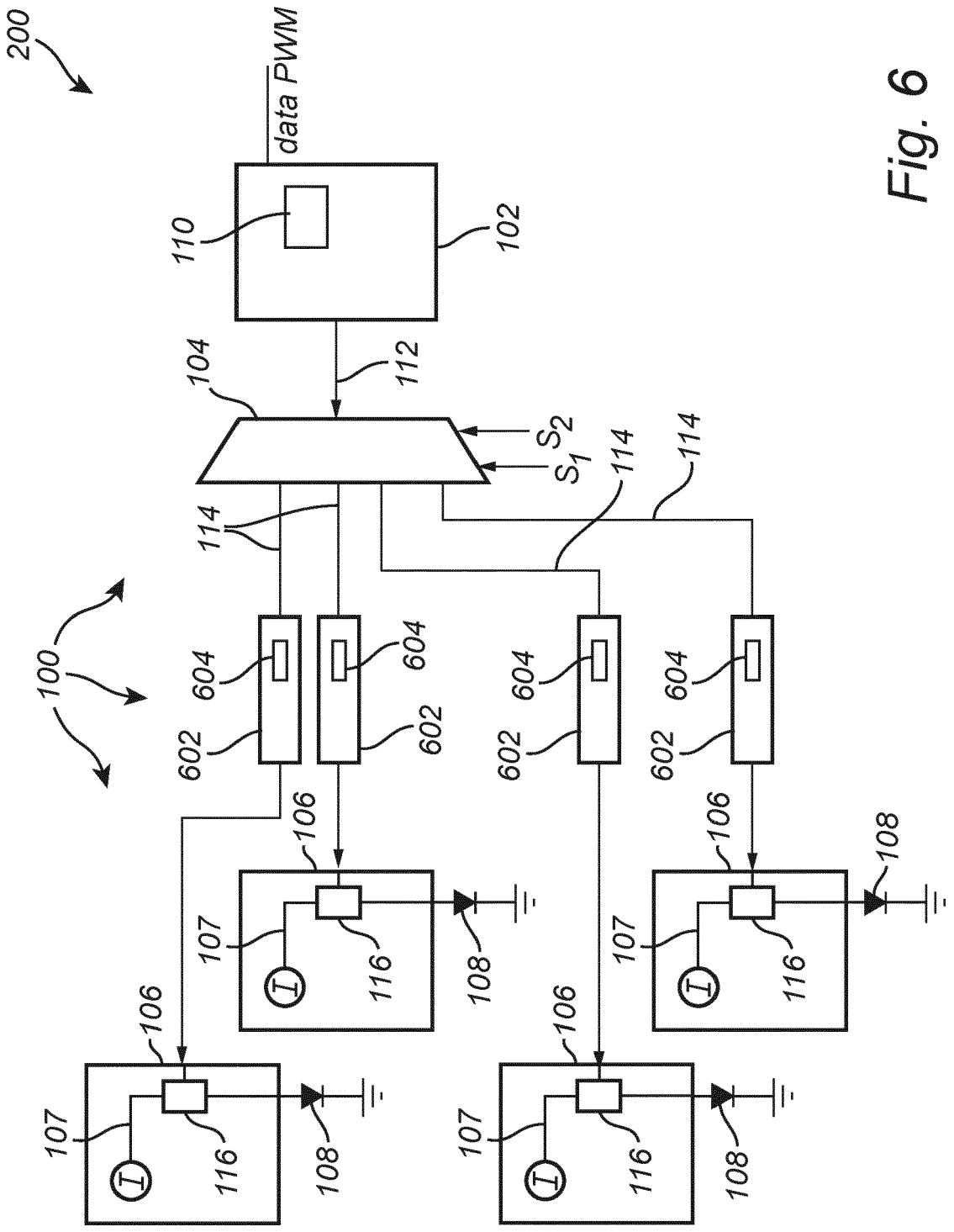
412

Fig. 5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data PWM
110
102
104
112
S_2
S_1
114
114
114
100
604
602
604
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604
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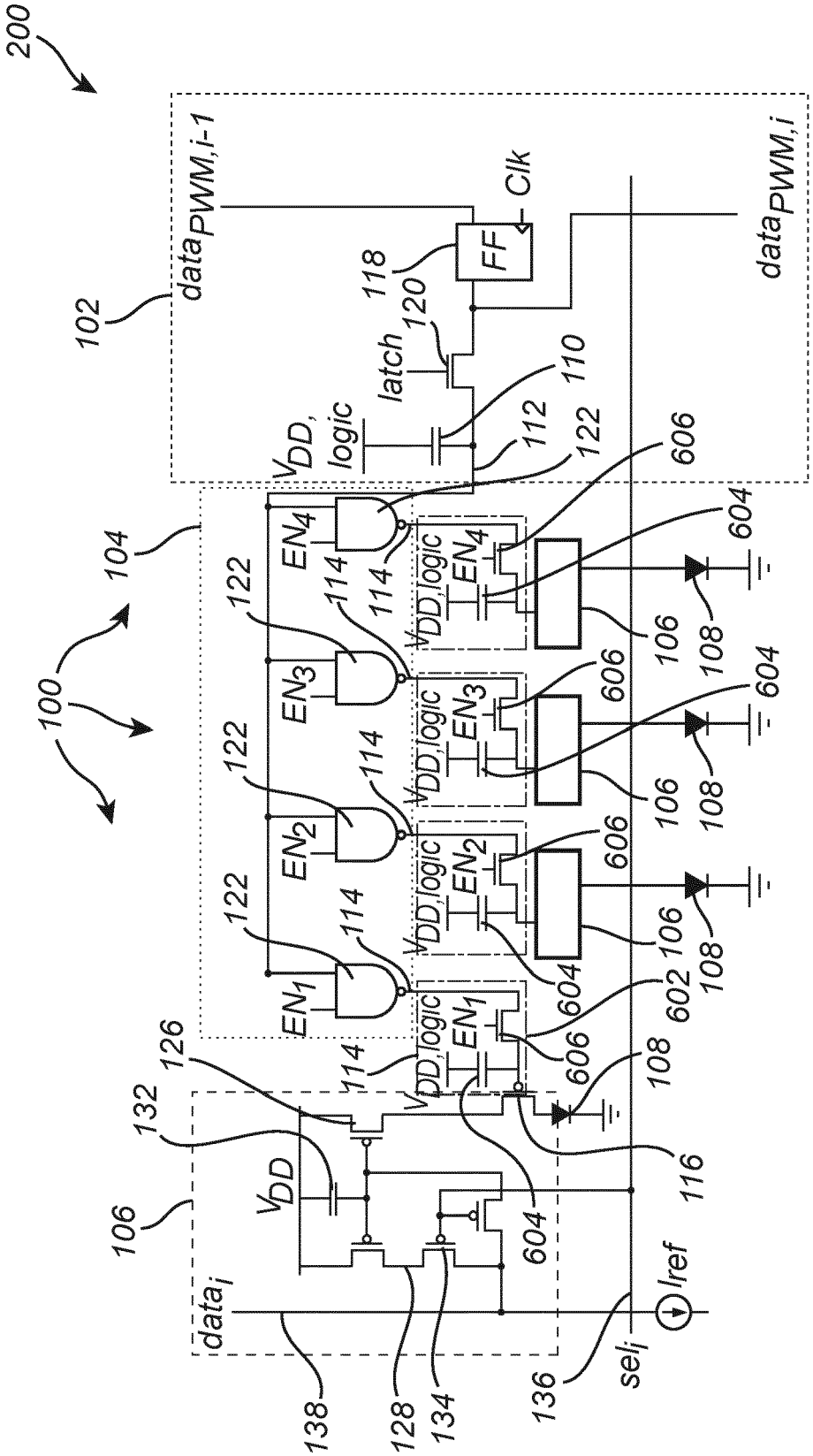
116
108

Fig. 6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sel_i
Iref
EN_1
EN_2
EN_3
EN_4
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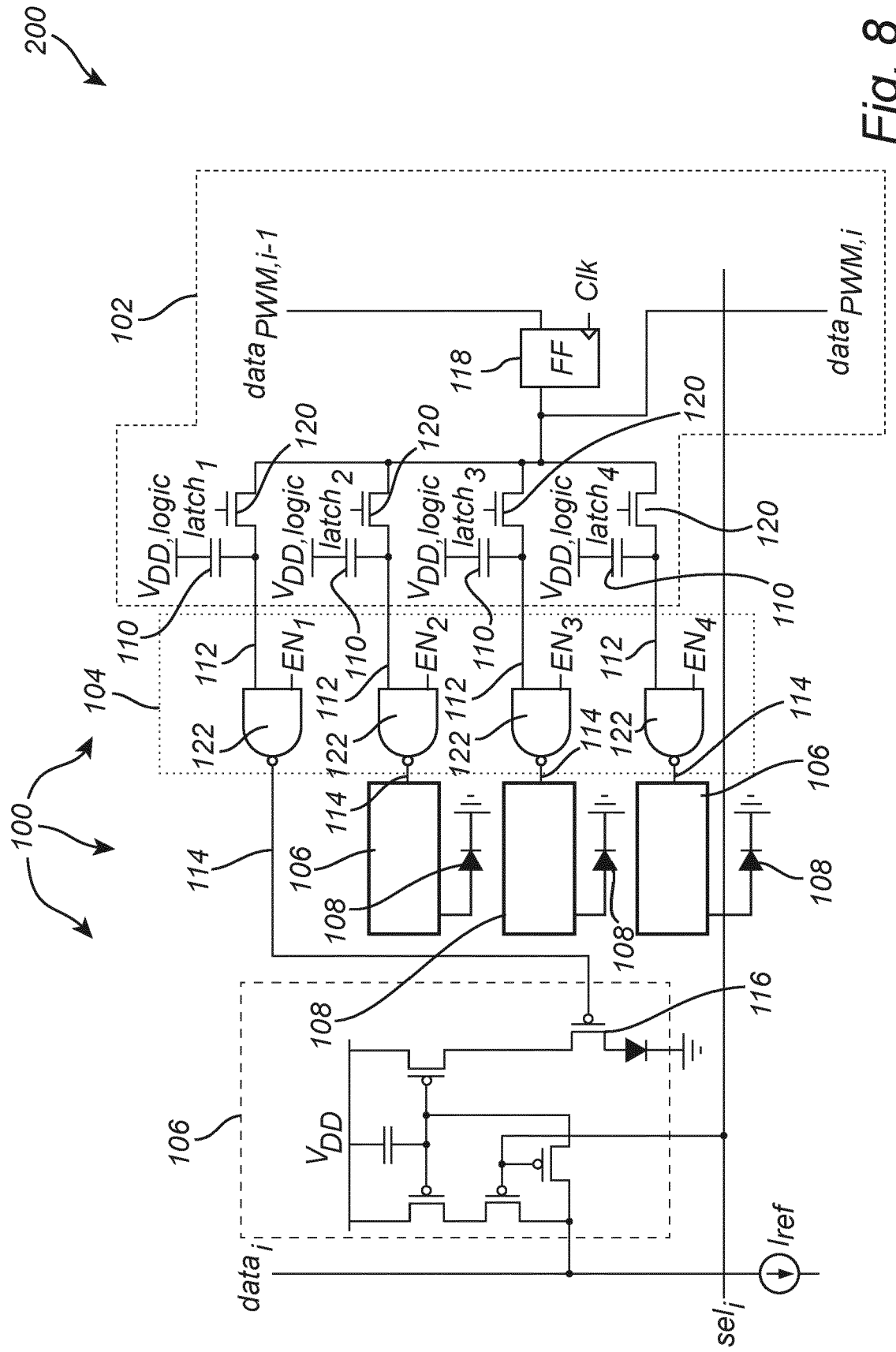
602
604
606
108

Fig. 7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106
108
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122
FF
Clk
$data_{PWM,i-1}$
$data_{PWM,i}$
$data_i$
sel_i
I_{ref}
V_{DD}
$V_{DD,logic}$
$latch_1$
$latch_2$
$latch_3$
$latch_4$
EN_1
EN_2
EN_3
EN_4

Fig. 8

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EUROPEAN SEARCH REPORT

Application Number
EP 21 21 7449

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	WO 2021/064061 A1 (BARCO NV [BE]) 8 April 2021 (2021-04-08) * page 3, line 25 - page 51, line 33; figures 1-26 *	1-13	INV. G09G3/20 G09G3/3208
Y	US 2016/210892 A1 (OHARA MASANORI [JP] ET AL) 21 July 2016 (2016-07-21) * paragraphs [0205] - [0210]; figures 27-30, 7 *	1-13	

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G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	18 May 2022	Vázquez del Real, S

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18-05-2022

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