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(54) **VOLTAGE BIAS CIRCUIT WITH ADJUSTABLE OUTPUT, AND CHIP AND COMMUNICATION TERMINAL**

(57) Provided are a voltage bias circuit with an adjustable output, and a chip and a communication terminal. The bias circuit comprises a bandgap voltage reference unit, a low-dropout linear voltage regulation unit, a first transmission gate switch unit, a logic encoding control unit and a second transmission gate switch unit. In the bias circuit, a resistance voltage-dividing network and a feedback resistance network are correspondingly arranged in a bandgap voltage reference unit and a low-dropout linear voltage regulation unit, so as to generate a plurality of voltages with different temperature coefficients and different values, and different gain coefficients; a logic encoding control unit is used to control a corresponding transmission gate switch unit to select an input reference voltage with a required value and temperature coefficient, and a required gain coefficient, so as to output a voltage with a required value and temperature coefficient; and a suitable bias state is provided for a radio frequency front-end module, such that the radio frequency front-end module realizes better performance, and a communication terminal has better flexibility and adaptability in a complicated environment.

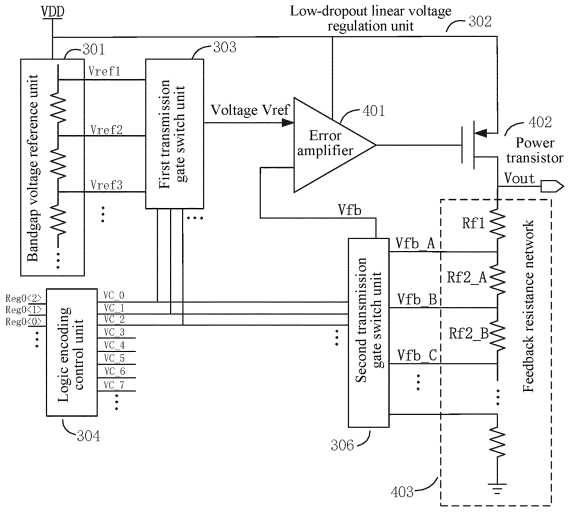

FIG. 2

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Description

BACKGROUND

Technical Field

[0001] The present disclosure relates to a voltage bias circuit with an adjustable output, an integrated circuit chip including the voltage bias circuit, and a corresponding communication terminal, and belongs to the technical field of integrated circuits.

Related Art

[0002] With the rapid development of communication technology, higher requirements are put forward for performance of communication terminals. Integrated circuit chips need to have higher flexibility and higher adaptability. A bias circuit for providing a direct current working point for a radio frequency front-end module, especially a heterojunction bipolar transistor (HBT) radio frequency bias circuit, is the first one needed to meet the requirements. The performance of the radio frequency front-end module is closely related to the working state of the bias circuit. Because it is needed to repeatedly debug the radio frequency front-end module during research and development and application, the scale and quantity of portable communication terminals (mainly mobile phones and tablet computers) are huge and the application environment is complicated, so it is very important to provide a high-flexibility direct current working point for the radio frequency front-end module. Otherwise, the development of the new generation of communication technology might be greatly limited.

[0003] A bandgap voltage reference circuit (bandgap for short) and a low dropout regulator (LDO for short) are common typical voltage bias circuits, and the flexibility of the radio frequency front-end module (mainly a power amplifier) depends on the flexibility of the output voltage of the bandgap and the LDO. That is, the more flexible the output voltage of the bandgap and the LDO is, the easier the radio frequency front-end module achieves better performance, and the more the communication terminal can adapt to a complicated application environment. However, output voltages of an existing bandgap and an existing LDO are simple, an output voltage with any temperature coefficient and any value cannot be achieved on the same circuit module, and the low flexibility limits the research and development and debugging of the radio frequency front-end module as well as the application of the communication terminal.

SUMMARY

[0004] The primary technical problem to be solved by the present disclosure is to provide a voltage bias circuit with an adjustable output.

[0005] Another technical problem to be solved by the present disclosure is to provide an integrated circuit chip including the above voltage bias circuit and a corresponding communication terminal.

[0006] In order to achieve the above objectives, the present disclosure adopts the following technical solutions:

According to a first aspect of an embodiment of the present disclosure, a voltage bias circuit with an adjustable output is provided, including a bandgap voltage reference unit, a low-dropout linear voltage regulation unit, a first transmission gate switch unit, a logic encoding control unit and a second transmission gate switch unit, where the bandgap voltage reference unit is connected to the low-dropout linear voltage regulation unit through the first transmission gate switch unit, the low-dropout linear voltage regulation unit is connected to the second transmission gate switch unit, and the logic encoding control unit is connected to the first transmission gate switch unit and the second transmission gate switch unit;

the logic encoding control unit is configured to control the first transmission gate switch unit to select a voltage with a required value and temperature coefficient from a plurality of voltages with different temperature coefficients and different values generated by the bandgap voltage reference unit, and the voltage is outputted to the low-dropout linear voltage regulation unit to serve as an input reference voltage; meanwhile, the logic encoding control unit controls the second transmission gate switch unit to select a corresponding required gain coefficient from a plurality of gain coefficients of the low-dropout linear voltage regulation unit; and a negative feedback closed-loop system is formed through the low-dropout linear voltage regulation unit, thus the voltage of a gain coefficient feedback node is approximately equal to the input reference voltage, and then the voltage with the required value and temperature coefficient can be outputted.

[0007] Preferably, the bandgap voltage reference unit includes an operational amplifier, a first PMOS transistor, a second PMOS transistor, a third PMOS transistor, a first resistor, a first bipolar transistor, a second bipolar transistor, a

third bipolar transistor and a resistance voltage-dividing network; a non-inverting input terminal of the operational amplifier is connected to a drain electrode of the first PMOS transistor and one end of the first resistor, and the other end of the first resistor is connected to an emitting electrode of the first bipolar transistor; an inverting input terminal of the operational amplifier is connected to a drain electrode of the second PMOS transistor and an emitting electrode of the second bipolar transistor; an output terminal of the operational amplifier is connected to grid electrodes of the first PMOS transistor, the second PMOS transistor and the third PMOS transistor; a drain electrode of the third PMOS transistor is connected to one end of the resistance voltage-dividing network, and the other end of the resistance voltage-dividing network is connected to an emitting electrode of the third bipolar transistor; an output terminal of the resistance voltage-dividing network is connected to the first transmission gate switch unit; source electrodes of the first PMOS transistor, the second PMOS transistor and the third PMOS transistor are connected to a supply voltage; and collector electrodes of the first bipolar transistor, the second bipolar transistor and the third bipolar transistor are grounded.

[0008] Preferably, the resistance voltage-dividing network is formed by connecting a plurality of second resistors in series; and different resistance nodes of the resistance voltage-dividing network correspondingly output voltages with different temperature coefficients and different values.

[0009] Preferably, the low-dropout linear voltage regulation unit includes an error amplifier, a power transistor and a feedback resistance network; a non-inverting input terminal of the error amplifier is connected to the first transmission gate switch unit; an inverting input terminal of the error amplifier is connected to the feedback resistance network through the second transmission gate switch unit; an output terminal of the error amplifier is connected to a grid electrode of the power transistor; a drain electrode of the power transistor is connected to one end of the feedback resistance network, and the other end of the feedback resistance network is grounded; and a source electrode of the power transistor is connected to the supply voltage.

[0010] Preferably, the feedback resistance network is formed by connecting a plurality of third resistors in series; and each resistance feedback node correspondingly outputs different gain coefficients.

[0011] Preferably, the logic encoding control unit is a binary encoding circuit formed by an NOT gate circuit and an AND gate circuit.

[0012] Preferably, the first transmission gate switch unit includes a plurality of first transmission gate switches; each first transmission gate switch includes a tenth PMOS transistor, a seventh NMOS transistor and a first phase inverter; a source electrode of each tenth PMOS transistor is connected to a drain electrode of the corresponding seventh NMOS transistor to be used as a corresponding input terminal of the first transmission gate switch, and is configured to connect a resistance node corresponding to the resistance voltage-dividing network; a drain electrode of each tenth PMOS transistor is connected to a source electrode of the corresponding seventh NMOS transistor to be used as an output terminal of the corresponding first transmission gate switch, and is configured to connect a non-inverting input terminal of the error amplifier; a grid electrode of each seventh NMOS transistor is connected to a corresponding output terminal of the logic encoding control unit and an input terminal of the corresponding first phase inverter; and an output terminal of each first phase inverter is connected to a grid electrode of the corresponding tenth PMOS transistor.

[0013] Preferably, the second transmission gate switch unit includes a plurality of second transmission gate switches; each second transmission gate switch includes an eleventh PMOS transistor, an eighth NMOS transistor and a second phase inverter; a source electrode of each eleventh PMOS transistor is connected to a drain electrode of the corresponding eighth NMOS transistor to be used as an input terminal of the corresponding second transmission gate switch, and is configured to connect a corresponding resistance feedback node of the feedback resistance network; a drain electrode of each eleventh PMOS transistor is connected to a source electrode of the corresponding eighth NMOS transistor to be used as an output terminal of the corresponding second transmission gate switch, and is configured to connect an inverting input terminal of the error amplifier; a grid electrode of each eighth NMOS transistor is connected to the corresponding output terminal of the logic encoding control unit and an input terminal of the corresponding second phase inverter; and an output terminal of each second phase inverter is connected to a grid electrode of the corresponding eleventh PMOS transistor.

[0014] According to a second aspect of an embodiment of the present disclosure, an integrated circuit chip is provided; and the integrated circuit chip includes the above voltage bias circuit.

[0015] According to a third aspect of an embodiment of the present disclosure, a communication terminal is provided; and the communication terminal includes the above voltage bias circuit.

[0016] According to the voltage bias circuit with adjustable output provided by the present disclosure, the resistance voltage-driving network and the feedback resistance network are correspondingly arranged in the bandgap voltage reference unit and the low-dropout linear voltage regulation unit, so as to generate a plurality of voltages with different temperature coefficients and different values, and different gain coefficients; the logic encoding control unit is configured to control the corresponding transmission gate switch unit to select the input reference voltage with the required value and temperature coefficient, and the required gain coefficient, so as to output the voltage with the required value and temperature coefficient; and a suitable bias state is provided for a radio frequency front-end module, such that the radio frequency front-end module realizes better performance, and the communication terminal has better flexibility and adapt-

ability in a complicated environment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

FIG. 1 is a schematic diagram of a typical voltage bias circuit;
FIG. 2 is a schematic diagram of a voltage bias circuit with an adjustable output according to an embodiment of the present disclosure;
FIG. 3 is a schematic diagram of a circuit of a bandgap voltage reference unit in a voltage bias circuit with an adjustable output according to an embodiment of the present disclosure;
FIG. 4 is a schematic diagram of a circuit of an error amplifier in a voltage bias circuit with an adjustable output according to an embodiment of the present disclosure;
FIG. 5 is a schematic diagram of 3-8 encoding circuits in a logic encoding control unit in a voltage bias circuit with an adjustable output according to an embodiment of the present disclosure;
FIG. 6 is a schematic diagram of a circuit of a first transmission gate switch unit in a voltage bias circuit with an adjustable output according to an embodiment of the present disclosure; and
FIG. 7 is a schematic diagram of a circuit of a second transmission gate switch unit in a voltage bias circuit with an adjustable output according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0018] The technical content of the present disclosure will be further described below in combination with the accompanying drawings and specific embodiments.

[0019] As shown in FIG. 1, a typical voltage bias circuit includes a bandgap voltage reference unit 101 and a low-dropout linear voltage regulation unit 102. The bandgap voltage reference unit is configured to generate a reference voltage Vref which has a zero temperature coefficient and is not affected by a supply voltage, and then provide the reference voltage Vref to the low-dropout linear voltage regulation unit 102 as an input reference voltage.

[0020] The low-dropout linear voltage regulation unit 102 includes an error amplifier 201, a power transistor 202 and a feedback resistance network 203. The feedback resistance network 203 includes a resistor Rf1 and a resistor Rf2.

[0021] An expression of an output voltage Vout is $V_{\mathrm{out}} = \frac{\mathrm{Rf1+Rf2}}{\mathrm{Rf2}} * \mathrm{Vref}$, in the formula, $\frac{\mathrm{Rf1+Rf2}}{\mathrm{Rf2}}$ can be called a gain coefficient, and its magnitude is determined by a proportional relationship between the resistor Rf1 and the resistor Rf2. The output voltage Vout is determined by the reference voltage Vref of the bandgap voltage reference unit 101 and the gain coefficient of the low-dropout linear voltage regulation unit 102 together.

[0022] In order to solve the problems that output voltages of the above bandgap voltage reference circuit and the low dropout regulator are simple and an output voltage with any temperature coefficient and any value cannot be realized on the same circuit module, and achieve the purposes that a radio frequency front-end module realizes better performance and a communication terminal has better application in a complicated environment, an embodiment of the present disclosure provides a voltage bias circuit with an adjustable output, which is configured to provide voltages with different temperature coefficients and different values for the radio frequency front-end module. As shown in FIG. 2, the voltage bias circuit includes a bandgap voltage reference unit 301, a low-dropout linear voltage regulation unit 302, a first transmission gate switch unit 303, a logic encoding control unit 304 and a second transmission gate switch unit 306; the bandgap voltage reference unit 301 and the low-dropout linear voltage regulation unit 302 are connected to a supply voltage (VDD); the bandgap voltage reference unit 301 is connected to the low-dropout linear voltage regulation unit 302 through the first transmission gate switch unit 303; the low-dropout linear voltage regulation unit 302 is connected to the second transmission gate switch unit 306; and the logic encoding control unit 304 is connected to the first transmission gate switch unit 303 and the second transmission gate switch unit 306.

[0023] The logic encoding control unit 304 is configured to control the first transmission gate switch unit 303 to select a voltage with a required value and temperature coefficient from a plurality of voltages with different temperature coefficients and different values generated by the band-gap voltage reference unit 301, and the voltage is outputted to the low-dropout linear voltage regulation unit 302 to serve as an input reference voltage of the low-dropout linear voltage regulation unit 302; meanwhile, the logic encoding control unit 304 controls the second transmission gate switch unit 306 to select a corresponding required gain coefficient from a plurality of gain coefficients of the low-dropout linear voltage regulation unit 302, and a negative feedback closed-loop system is formed through the low-dropout linear voltage regulation unit 302, thus the voltage of a gain coefficient feedback node is approximately equal to the input reference voltage, and then the voltage with the required value and temperature coefficient is outputted; a suitable proper bias

state is provided for the radio frequency front-end module, such that the radio frequency front-end module realizes better performance, and the communication terminal has better application in a complicated environment.

[0024] The bandgap voltage reference unit 301 is configured to generate a plurality of voltages with different temperature coefficients and different values. The quantity of the voltages with different temperature coefficients and different values generated by the bandgap voltage reference unit 301 is adjusted according to the quantity actually required by the radio frequency front-end module. As shown in FIG. 3, the bandgap voltage reference unit 301 includes an operational amplifier A1, a first PMOS transistor 701, a second PMOS transistor 702, a third PMOS transistor 703, a first resistor R1, a first bipolar transistor 706, a second bipolar transistor 707, a third bipolar transistor 708 and a resistance voltage-dividing network 709. A non-inverting input terminal of the operational amplifier A1 is connected to a drain electrode of the first PMOS transistor 701 and one end of the first resistor R1, and the other end of the first resistor R1 is connected to an emitting electrode of the first bipolar transistor 706; an inverting input terminal of the operational amplifier A1 is connected to a drain electrode of the second PMOS transistor 702 and an emitting electrode of the second bipolar transistor 707; an output terminal of the operational amplifier A1 is connected to grid electrodes of the first PMOS transistor 701, the second PMOS transistor 702 and the third PMOS transistor 703; a drain electrode of the third PMOS transistor 703 is connected to one end of the resistance voltage-dividing network 709, and the other end of the resistance voltage-dividing network 709 is connected to an emitting electrode of the third bipolar transistor 708; an output terminal of the resistance voltage-dividing network 709 is connected to the first transmission gate switch unit 303; source electrodes of the first PMOS transistor 701, the second PMOS transistor 702 and the third PMOS transistor 703 are connected to the VDD; and collector electrodes of the first bipolar transistor 706, the second bipolar transistor 707 and the third bipolar transistor 708 are grounded.

[0025] As shown in FIG. 3, the resistance voltage-dividing network 709 is formed by connecting a plurality of second resistors (resistors R2_A, R2_B, R2_C ... R2_N) in series; and a plurality of voltages (Vref1, Vref2... Vrefn) with different temperature coefficients and different values are generated by resistance voltage-dividing, that is, different resistance nodes of the resistance voltage-dividing network 709 correspondingly output the voltages with different temperature coefficients and different values. The logic encoding control unit 304 is configured to control an on-off state of the first transmission gate switch unit 303, such that a voltage with a required value and temperature coefficient can be selected from the plurality of voltages with different temperature coefficients and different values generated by the resistance voltage-dividing network 709, and the different voltages are provided for the low-dropout linear voltage regulation unit 302 to serve as input reference voltages so as to realize the diversity of the input reference voltages. The adjustable precision of the output voltage of the voltage bias circuit with the adjustable output is determined by the proportion of the second resistors in the resistance voltage-dividing network 709, and the resistance voltage-dividing network 709 with a proper proportion can be designed according to the value and temperature coefficient precision of the voltage required by application.

[0026] As shown in FIG. 3, the first PMOS transistor 701, the second PMOS transistor 702 and the third PMOS transistor 703 form a current mirror, and the width-to-length ratio of the first PMOS transistor 701 is the same as that of the second PMOS transistor 702, so the current flowing through the first bipolar transistor 706 is equal to the current flowing through the second bipolar transistor 707, and thus a difference value $\Delta V_{BE} = Inn * V_T$ of base electrode-emitting electrode voltages of the first bipolar transistor 706 and the second bipolar transistor 707 is further obtained; n is the ratio of the parallel number of the bipolar transistor 706 and the bipolar transistor 707; V_T is the thermal voltage of the bipolar transistor, shown as $V_T = \frac{k}{q}T$; k is a Boltzmann constant; q is an electron charge, shown as $\Delta V_{BE} = Inn * \frac{k}{q}T$, therefore, the difference value ΔV_{BE} of the base electrode-emitting electrode voltages of the first bipolar transistor 706 and the second bipolar transistor 707 is in a direct proportion to an absolute temperature T, namely a PTAT current. In addition, due to the existence of the operational amplifier A1 of the non-inverting input terminal and the inverting input terminal of the operational amplifier A1 have the same voltage, the voltage dropout on the first resistor R1 is the difference value ΔV_{BE} of the base electrode-emitting electrode voltages of the first bipolar transistor 706 and the second bipolar transistor 707, and the currents flowing through the first PMOS transistor 701 and the second PMOS transistor 702 are shown as $I_1 = I_2 = \frac{\Delta V_{BE}}{R1} = \frac{Inn}{R1} * \frac{k}{q}T$; and it is assumed that the proportion of current mirror of the third PMOS transistor 703 relative to the first PMOS transistor 701 and the second PMOS transistor 702 is M, then the current flowing through the third PMOS transistor 703 is shown as $I_3 = M * I_1 = M * I_2 = M * \frac{\Delta V_{BE}}{R1} = M * \frac{Inn}{R1} * \frac{k}{q}T$. Therefore, the plurality of voltages (Vref1, Vref2...

Vrefn) with different temperature coefficients and different values by the resistance voltage-dividing network 709 is determined by the voltage generated by a current I_3 flowing through a corresponding resistor in the resistance voltage-dividing network 709 and a base electrode-emitting electrode voltage V_{BE} of the third bipolar transistor 708, for example, $Vref1=I_3*(R2\_A+R2\_B+R2\_C+...R2\_N)+V_{BE}$, $Vref2=I_3*(R2\_B+R2\_C+...R2\_N)+V_{BE}$, such that different resistance nodes of the resistance voltage-dividing network 709 can output voltages with different values and different temperature coefficients.

[0027] As shown in FIG. 2, the low-dropout linear voltage regulation unit 302 includes an error amplifier 401, a power transistor 402 and a feedback resistance network 403; a non-inverting input terminal of the error amplifier 401 is connected to the first transmission gate switch unit 303, and an inverting input terminal of the error amplifier 401 is connected to the feedback resistance network 403 through the second transmission gate switch unit 306; an output terminal of the error amplifier 401 is connected to a grid electrode of the power transistor 402; a drain electrode of the power transistor 402 is connected to one end of the feedback resistance network 403, and the other end of the feedback resistance network 403 is grounded; and a source electrode of the power transistor 402 is connected to the VDD.

[0028] As shown in FIG. 2, the feedback resistance network 403 is formed by connecting a plurality of third resistors (Rf2_A, Rf2_B, Rf2_C... Rf2_H) in series; and different resistance feedback nodes (Vfb_A, Vfb_B, Vfb_C... Vfb_H) in the feedback resistance network 403 correspond to different gain coefficients. The error amplifier 401, the power transistor 402 and the feedback resistance network 403 form a negative feedback closed-loop system, so that the voltages of the non-inverting input terminal and the inverting input terminal of the error amplifier 401 are approximately equal, and then the clamping of an input reference voltage node and a resistance feedback node (namely a gain coefficient feedback node) of the error amplifier 401 is realized, namely the voltage of the resistance feedback node is approximately equal to the input reference voltage. A resistance feedback node is arranged between every two adjacent third resistors in the feedback resistance network 403; and the resistance feedback nodes correspond to different voltages, and each resistance feedback node correspondingly outputs a different gain coefficient so as to realize the diversity of the gain coefficients. The adjustable precision of the output voltage gain coefficient of the voltage bias circuit with the adjustable output is determined by the proportion of the third resistors in the feedback resistance network 403, and the feedback resistance network 403 with a proper proportion can be designed according to the gain coefficient of the voltage required by the application.

[0029] As shown in FIG. 4, the error amplifier 401 includes a fourth PMOS transistor 601, a fifth PMOS transistor 602, a first NMOS transistor 603, a second NMOS transistor 604, a sixth PMOS transistor 605, a seventh PMOS transistor 606, a third NMOS transistor 607, a fourth NMOS transistor 608, a fifth NMOS transistor 609, a sixth NMOS transistor 610, an eighth PMOS transistor 611 and a ninth PMOS transistor 612; a grid electrode of the fourth PMOS transistor 601 is used as the non-inverting input terminal of the error amplifier 401, and is configured to connect the first transmission gate switch unit 303; a grid electrode of the fifth PMOS transistor 602 is used as the inverting input terminal of the error amplifier 401, and is configured to connect the second transmission gate switch unit 306; a drain electrode of the fourth PMOS transistor 601 is connected to a grid electrode and a drain electrode of the first NMOS transistor 603 and a grid electrode of the second NMOS transistor 604; a drain electrode of the second NMOS transistor 604 is connected to a grid electrode and a drain electrode of the sixth PMOS transistor 605 and a grid electrode of the seventh PMOS transistor 606; a drain electrode of the seventh PMOS transistor 606 is used as an output terminal Vop of the error amplifier 401, and is configured to connect a grid electrode of the power transistor 402 and a drain electrode of the fourth NMOS transistor 608; a grid electrode of the fourth NMOS transistor 608 is connected to a grid electrode and a drain electrode of the third NMOS transistor 607 and a drain electrode of the fifth PMOS transistor 602; a source electrode of the fifth PMOS transistor 602 is connected to a source electrode of the fourth PMOS transistor 601 and a drain electrode of the ninth PMOS transistor 612; a grid electrode of the ninth PMOS transistor 612 is connected to a grid electrode and a drain electrode of the eighth PMOS transistor 611 and a drain electrode of the sixth NMOS transistor 610; a grid electrode of the sixth NMOS transistor 610 is connected to a grid electrode and a drain electrode of the fifth NMOS transistor 609; a drain electrode of the fifth NMOS transistor 609 is connected to an external bias voltage Ibias; source electrodes of the sixth PMOS transistor 605, the seventh PMOS transistor 606, the eighth PMOS transistor 611 and the ninth PMOS transistor 612 are all connected to the VDD; and source electrodes of the first NMOS transistor 603, the second NMOS transistor 604, the third NMOS transistor 607, the fourth NMOS transistor 608, the fifth NMOS transistor 609 and the sixth NMOS transistor 610 are all grounded.

[0030] According to the embodiment of the present disclosure, in the error amplifier 401, the fourth PMOS transistor 601 and the fifth PMOS transistor 602 are input amplification geminate transistors; the first NMOS transistor 603 and the second NMOS transistor 604, the sixth PMOS transistor 605 and the seventh PMOS transistor 606, the third NMOS transistor 607 and the fourth NMOS transistor 608, the fifth NMOS transistor 609 and the sixth NMOS transistor 610, and the eighth PMOS transistor 611 and the ninth PMOS transistor 612 form mirror current mirrors respectively. The bias current Ibias is mirrored through the fifth NMOS transistor 609 and the sixth NMOS transistor 610, and the eighth PMOS transistor 611 and the ninth PMOS transistor 612 to provide current bias for the fourth PMOS transistor 601 and

the fifth PMOS transistor 602. The fourth PMOS transistor 601 receives the voltage with the required value and temperature coefficient provided by the bandgap voltage reference unit 301 as a reference input voltage of the low-dropout linear voltage regulation unit; and the fifth PMOS transistor 602 receives a resistance feedback node corresponding to the required gain coefficient provided by the feedback resistance network 403, and is mirrored through the first NMOS transistor 603 and the second NMOS transistor 604, the sixth PMOS transistor 605 and the seventh PMOS transistor 606, and the third NMOS transistor 607 and the fourth NMOS transistor 608. Essentially, the error amplifier 401 is an operational amplifier with a current mirror load. The error amplifier, the power transistor and the feedback resistance network of the low-dropout linear voltage regulation unit form a negative feedback closed-loop system, so that the voltages of the non-inverting input terminal and the inverting input terminal of the error amplifier are approximately equal, and the clamping of the input reference voltage node and the resistance feedback node is realized, namely the voltage of the resistance feedback node is approximately equal to the input reference voltage.

[0031] The logic encoding control unit 304 is to generate a plurality of logic combinations by using a plurality of fewer logic control bits so as to control the first transmission gate switch unit 303 and the second transmission gate switch unit 306 to select different input reference voltages and different gain coefficients, thereby realizing a plurality of different voltage combinations. The logic encoding control unit 304 can be a binary encoding circuit composed of an NOT gate circuit and an AND gate circuit; and for example, the logic encoding control unit 304 can be a binary encoding circuit such as 2-4 encoding circuits, 3-8 encoding circuits, and 4-16 encoding circuits. The quantity of the logic control bits of the logic encoding control unit 304 is determined by the type of the voltage required to be outputted and the mode of logic encoding, and the voltage types are realized as much as possible by using the logic control bits as few as possible in general so as to adapt to more application requirements. That is, the quantity of control levels generated by the logic encoding control unit 304 is determined by the quantity of the voltage with the temperature coefficient and value required by the radio frequency front-end module.

[0032] As shown in FIG. 5, that the logic encoding control unit 304 is the 3-8 encoding circuits is taken as an example, logic control bits Reg0<2>, Reg0<1> and Reg0<0> firstly pass through the NOT gate circuit in sequence to obtain levels Reg0<2>_Bar and Reg0<2>_Buf, Reg0<1>_Bar and Reg0<1>_Buf, Reg0<0>_Bar and Reg0<0>_Buf. Then the levels are subjected to logic combination to obtain control levels through a three-input AND gate circuit, one logic combination of Reg0<2:0> corresponds to one control level, and Reg0<2:0>=000; 001...; and 111 sequentially correspond output control levels VC_0; VC_1...; and VC_7.

[0033] The first transmission gate switch unit 303 includes a plurality of first transmission gate switches, the quantity of the first transmission gate switches is the same as the quantity of voltages with different values and different temperature coefficients generated by the resistance voltage-dividing network 709 in an one-by-one way. Different resistance nodes of the resistance voltage-dividing network 709 are correspondingly connected to the plurality of first transmission gate switches, such that each voltage with fixed value and fixed temperature coefficient outputted by the resistance voltage-dividing network 709 corresponds to one first transmission gate switch.

[0034] As shown in FIG. 6, each first transmission gate switch includes a tenth PMOS transistor, a seventh NMOS transistor and a first phase inverter; a source electrode of each tenth PMOS transistor is connected to a drain electrode of the corresponding seventh NMOS transistor to serve as an input terminal of the corresponding first transmission gate switch, and is configured to connect a resistance node corresponding to the resistance voltage-dividing network 709; a drain electrode of each tenth PMOS transistor is connected to a source electrode of the corresponding seventh NMOS transistor to serve as an output terminal of the corresponding first transmission gate switch, and is configured to connect the non-inverting input terminal of the error amplifier 401; a grid electrode of each seventh NMOS transistor is connected to the corresponding output terminal of the logic encoding control unit 304 and an input terminal of the corresponding first phase inverter; and an output terminal of each first phase inverter is connected to a grid electrode of the corresponding tenth PMOS transistor. A PMOS transistor M1, a NMOS transistor M2, a first phase inverter J1, a PMOS transistor M5, a NMOS transistor M6, a first phase inverter J2...a PMOS transistor M30, a NMOS transistor M29 and a first phase inverter J15 shown in FIG. 6 correspondingly form the plurality of first transmission gate switches. The connecting and disconnecting of a branch are correspondingly controlled by the connecting and disconnecting of the MOS transistors, thus one-to-one correspondence between the logic combination and the voltage obtained by resistance voltage dividing of the bandgap voltage reference unit 301 is realized, and then one-to-one correspondence between the logic combination and output voltage is realized, and one logic corresponds to a voltage with a determined value and determined temperature coefficient. Voltages Vref1, Vref2... Vrefn are controlled by the first transmission gate switch unit 303 to output a voltage Vref with a determined value and determined temperature coefficient to the low-dropout regulation unit 302 as the input reference voltage.

[0035] As shown in FIG. 6, control levels VC_0; VC_1...; and VC_7 outputted by the logic encoding control unit 304 are used as enable signals to sequentially control the on and off of the corresponding first transmission gate switch. Taking the control level VC_0 as an example, when the control level VC_0 is a high level, the PMOS transistor M1 and the NMOS transistor M2 are connected, so that the corresponding first transmission gate switch is on; and a voltage Vref_1 is transmitted to the output terminal of the first transmission gate switch, thus a voltage Vref with a fixed value

and fixed temperature coefficient is outputted to the low-dropout linear voltage regulation unit 302 to be used as the input reference voltage. When the control level VC_0 is a low level, the PMOS transistor M1 and the NMOS transistor M2 are disconnected, so that the first transmission gate switch is off, that is, it is stopped to output the voltage Vref with the fixed value and fixed temperature coefficient to the low-dropout linear voltage regulation unit 302. Therefore, each logic combination corresponds to one control level, and each control level correspondingly controls the voltage with the fixed value and fixed temperature coefficient.

[0036] The second transmission gate switch unit 306 includes a plurality of second transmission gate switches, and the quantity of the second transmission gate switches is the same as the quantity of the voltages with different values and different temperature coefficients generated by the resistance voltage-dividing network 709. Different resistance feedback nodes in the feedback resistance network 403 are correspondingly connected to the plurality of second transmission gate switches, such that the voltage with each gain coefficient outputted by the feedback resistance network 403 corresponds to one second transmission gate switch.

[0037] As shown in FIG. 7, each second transmission gate switch includes an eleventh PMOS transistor, an eighth NMOS transistor and a second phase inverter; a source electrode of each eleventh PMOS transistor is connected to a drain electrode of the corresponding eighth NMOS transistor to serve as an input terminal of the corresponding second transmission gate switch, and is configured to connect the corresponding resistance feedback node of the feedback resistance network 403; a drain electrode of each eleventh PMOS transistor is connected to a source electrode of the corresponding eighth NMOS transistor to serve as an output terminal of the corresponding second transmission gate switch, and is configured to connect the inverting input terminal of the error amplifier 401; a grid electrode of each eighth NMOS transistor is connected to the corresponding output terminal of the logic encoding control unit 304 and an input terminal of the corresponding second phase inverter; and an output terminal of each second phase inverter is connected to a grid electrode of the corresponding eleventh PMOS transistor. APMOS transistor M3, an NMOS transistor M4, a second phase inverter J16, a PMOS transistor M7, a NMOS transistor M8, a second phase inverter J17...a PMOS transistor M31, an NMOS transistor M32 and a second phase inverter J30 shown in FIG. 7 correspondingly form the plurality of second transmission gate switches. The connecting and disconnecting of the branch are correspondingly controlled by the connecting and disconnecting of the MOS transistors, thus one-to-one correspondence between the logic combination and the grain coefficient obtained by resistance of the feedback resistance network 403 is realized, then the one-to-one correspondence between the logic combination and the output voltage is further realized, and one logic corresponds to a fixed gain coefficient.

[0038] As shown in FIG. 7, control levels VC_0; VC_1...; and VC_7 outputted by the logic encoding control unit 304 are used as enable signals to sequentially control the on and off of the corresponding second transmission gate switch. Taking the control level VC_0 as an example, when the control level VC_0 is a high level, the PMOS transistor M3 and the NMOS transistor M4 are connected, such that the corresponding second transmission gate switch is on; and the voltage with a certain gain coefficient outputted by a resistance feedback node Vfb_A is transmitted to the output terminal of the corresponding second transmission gate switch, and then a voltage Vfb with a fixed gain coefficient is outputted to the low-dropout linear voltage regulation unit 302. When the control level VC_0 is a low level, the PMOS transistor M3 and the NMOS transistor M4 are disconnected, thus the corresponding second transmission gate switch is off, that is, it is stopped to output the voltage Vfb with the fixed gain coefficient to the low-dropout linear voltage regulation unit 302. Therefore, one logic combination corresponds to a control level, and each control level correspondingly controls the voltage with the fixed value and fixed temperature coefficient.

[0039] Therefore, corresponding resistance nodes and resistance feedback nodes are correspondingly selected and controlled according to the voltage with the value and temperature coefficient required by the radio frequency front-end module and the control levels VC_0; VC_1...; and VC_7 outputted by the logic encoding control unit 304, so as to control the first transmission gate switch unit 303 to select a required input reference voltage; meanwhile, the second transmission gate switch unit 306 is also controlled through the control levels to select a required corresponding gain coefficient; and the control levels and the gain coefficient are combined together, and the voltage with the value and temperature coefficient required by the radio frequency front-end module is outputted through the low-dropout linear voltage regulation unit 102. Different logic combinations correspond to the voltages with different values and temperature coefficients.

[0040] In addition, according to this embodiment of the present disclosure, the voltage bias circuit with the adjustable output can be used in an integrated circuit chip. The specific structure of the voltage bias circuit with the adjustable output in the integrated circuit chip is not described in detail any more.

[0041] The above voltage bias circuit with the adjustable output can also be used in a communication terminal to serve as an important component of a radio frequency integrated circuit. The communication terminal herein refers to computer devices which can be used in a mobile environment and support multiple communication modes such as GSM, EDGE, TD_SCDMA, TDD_LTE and FDD LTE, and the computer devices include a mobile phone, a notebook computer, a tablet computer, a vehicle-mounted computer and the like. In addition, the technical solution provided by the present disclosure is also suitable for occasions where other radio frequency integrated circuits are applied, such as a communication base station.

[0042] According to the voltage bias circuit with the adjustable output provided by the present disclosure, the resistance voltage-driving network and the feedback resistance network are correspondingly arranged in the bandgap voltage reference unit and the low-dropout linear voltage regulation unit, so as to generate a plurality of voltages with different temperature coefficients and different values, and different gain coefficients; the logic encoding control unit is configured to control the corresponding transmission gate switch unit to select the input reference voltage with the required value and temperature coefficient, and the required gain coefficient, so as to output the voltage with the required value and temperature coefficient; and a suitable bias state is provided for the radio frequency front-end module, such that the radio frequency front-end module realizes better performance, and the communication terminal has better flexibility and adaptability in a complicated environment.

[0043] The voltage bias circuit with the adjustable output, the chip and the communication terminal according to the present disclosure are described above in detail. Any non-substantial change and replacement made by those skilled in the art based on the present disclosure are within the scope of protection required by the present disclosure.

Claims

1. A voltage bias circuit with an adjustable output, comprising a bandgap voltage reference unit, a low-dropout linear voltage regulation unit, a first transmission gate switch unit, a logic encoding control unit and a second transmission gate switch unit, wherein the bandgap voltage reference unit is connected to the low-dropout linear voltage regulation unit through the first transmission gate switch unit, the low-dropout linear voltage regulation unit is connected to the second transmission gate switch unit, and the logic encoding control unit is connected to the first transmission gate switch unit and the second transmission gate switch unit;
the logic encoding control unit is configured to control the first transmission gate switch unit to select a voltage with a required value and temperature coefficient from a plurality of voltages with different temperature coefficients and different values generated by the bandgap voltage reference unit, and the voltage is outputted to the low-dropout linear voltage regulation unit to serve as an input reference voltage; meanwhile, the logic encoding control unit controls the second transmission gate switch unit to select a corresponding required gain coefficient from a plurality of gain coefficients of the low-dropout linear voltage regulation unit; and a negative feedback closed-loop system is formed through the low-dropout linear voltage regulation unit, thus the voltage of a gain coefficient feedback node is approximately equal to the input reference voltage, and then the voltage with the required value and temperature coefficient can be outputted.

2. The voltage bias circuit with the adjustable output according to claim 1, wherein the bandgap voltage reference unit comprises an operational amplifier, a first PMOS transistor, a second PMOS transistor, a third PMOS transistor, a first resistor, a first bipolar transistor, a second bipolar transistor, a third bipolar transistor and a resistance voltage-dividing network; a non-inverting input terminal of the operational amplifier is connected to a drain electrode of the first PMOS transistor and one end of the first resistor, and the other end of the first resistor is connected to an emitting electrode of the first bipolar transistor; an inverting input terminal of the operational amplifier is connected to a drain electrode of the second PMOS transistor and an emitting electrode of the second bipolar transistor; an output terminal of the operational amplifier is connected to grid electrodes of the first PMOS transistor, the second PMOS transistor and the third PMOS transistor; a drain electrode of the third PMOS transistor is connected to one end of the resistance voltage-dividing network, and the other end of the resistance voltage-dividing network is connected to an emitting electrode of the third bipolar transistor; an output terminal of the resistance voltage-dividing network is connected to the first transmission gate switch unit; source electrodes of the first PMOS transistor, the second PMOS transistor and the third PMOS transistor are connected to a supply voltage; and collector electrodes of the first bipolar transistor, the second bipolar transistor and the third bipolar transistor are grounded.

3. The voltage bias circuit with the adjustable output according to claim 2, wherein
the resistance voltage-dividing network is formed by connecting a plurality of second resistors in series; and different resistance nodes of the resistance voltage-dividing network correspondingly output voltages with different temperature coefficients and different values.

4. The voltage bias circuit with the adjustable output according to claim 2, wherein the low-dropout linear voltage regulation unit comprises an error amplifier, a power transistor and a feedback resistance network; a non-inverting input terminal of the error amplifier is connected to the first transmission gate switch unit; an inverting input terminal of the error amplifier is connected to the feedback resistance network through the second transmission gate switch unit; an output terminal of the error amplifier is connected to a grid electrode of the power transistor; a drain electrode of the power transistor is connected to one end of the feedback resistance network, and the other end of the feedback

resistance network is grounded; and a source electrode of the power transistor is connected to the supply voltage.

5. The voltage bias circuit with the adjustable output according to claim 4, wherein the feedback resistance network is formed by connecting a plurality of third resistors in series; and each resistance feedback node correspondingly outputs different gain coefficients.

6. The voltage bias circuit with the adjustable output according to claim 1, wherein the logic encoding control unit is a binary encoding circuit formed by an NOT gate circuit and an AND gate circuit.

7. The voltage bias circuit with the adjustable output according to claim 4, wherein the first transmission gate switch unit comprises a plurality of first transmission gate switches; each first transmission gate switch comprises a tenth PMOS transistor, a seventh NMOS transistor and a first phase inverter; a source electrode of each tenth PMOS transistor is connected to a drain electrode of the corresponding seventh NMOS transistor to be used as a corresponding input terminal of the first transmission gate switch, and is configured to connect a resistance node corresponding to the resistance voltage-dividing network; a drain electrode of each tenth PMOS transistor is connected to a source electrode of the corresponding seventh NMOS transistor to be used as an output terminal of the corresponding first transmission gate switch, and is configured to connect a non-inverting input terminal of the error amplifier; a grid electrode of each seventh NMOS transistor is connected to a corresponding output terminal of the logic encoding control unit and an input terminal of the corresponding first phase inverter; and an output terminal of each first phase inverter is connected to a grid electrode of the corresponding tenth PMOS transistor.

8. The voltage bias circuit with the adjustable output according to claim 4, wherein the second transmission gate switch unit comprises a plurality of second transmission gate switches; each second transmission gate switch comprises an eleventh PMOS transistor, an eighth NMOS transistor and a second phase inverter; a source electrode of each eleventh PMOS transistor is connected to a drain electrode of the corresponding eighth NMOS transistor to be used as an input terminal of the corresponding second transmission gate switch, and is configured to connect a corresponding resistance feedback node of the feedback resistance network; a drain electrode of each eleventh PMOS transistor is connected to a source electrode of the corresponding eighth NMOS transistor to be used as an output terminal of the corresponding second transmission gate switch, and is configured to connect an inverting input terminal of the error amplifier; a grid electrode of each eighth NMOS transistor is connected to the corresponding output terminal of the logic encoding control unit and an input terminal of the corresponding second phase inverter; and an output terminal of each second phase inverter is connected to a grid electrode of the corresponding eleventh PMOS transistor.

9. An integrated circuit chip, comprising the voltage bias circuit with the adjustable output according to any one of claims 1 to 8.

10. A communication terminal, comprising the voltage bias circuit with the adjustable output according to any one of claims 1 to 8.

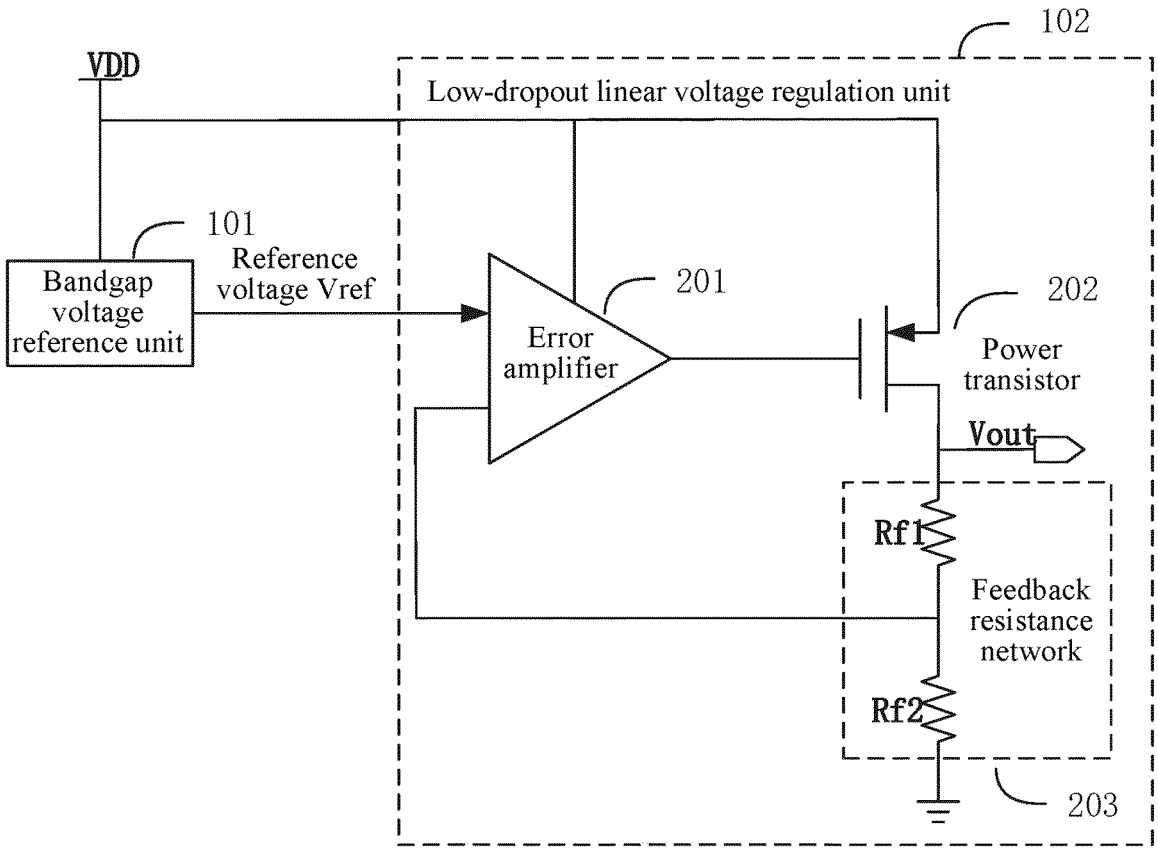
102
VDD
Low-dropout linear voltage regulation unit
101
Reference voltage Vref
Bandgap voltage reference unit
201
Error amplifier
202
Power transistor
Vout
Rf1
Feedback resistance network
Rf2
203

FIG. 1

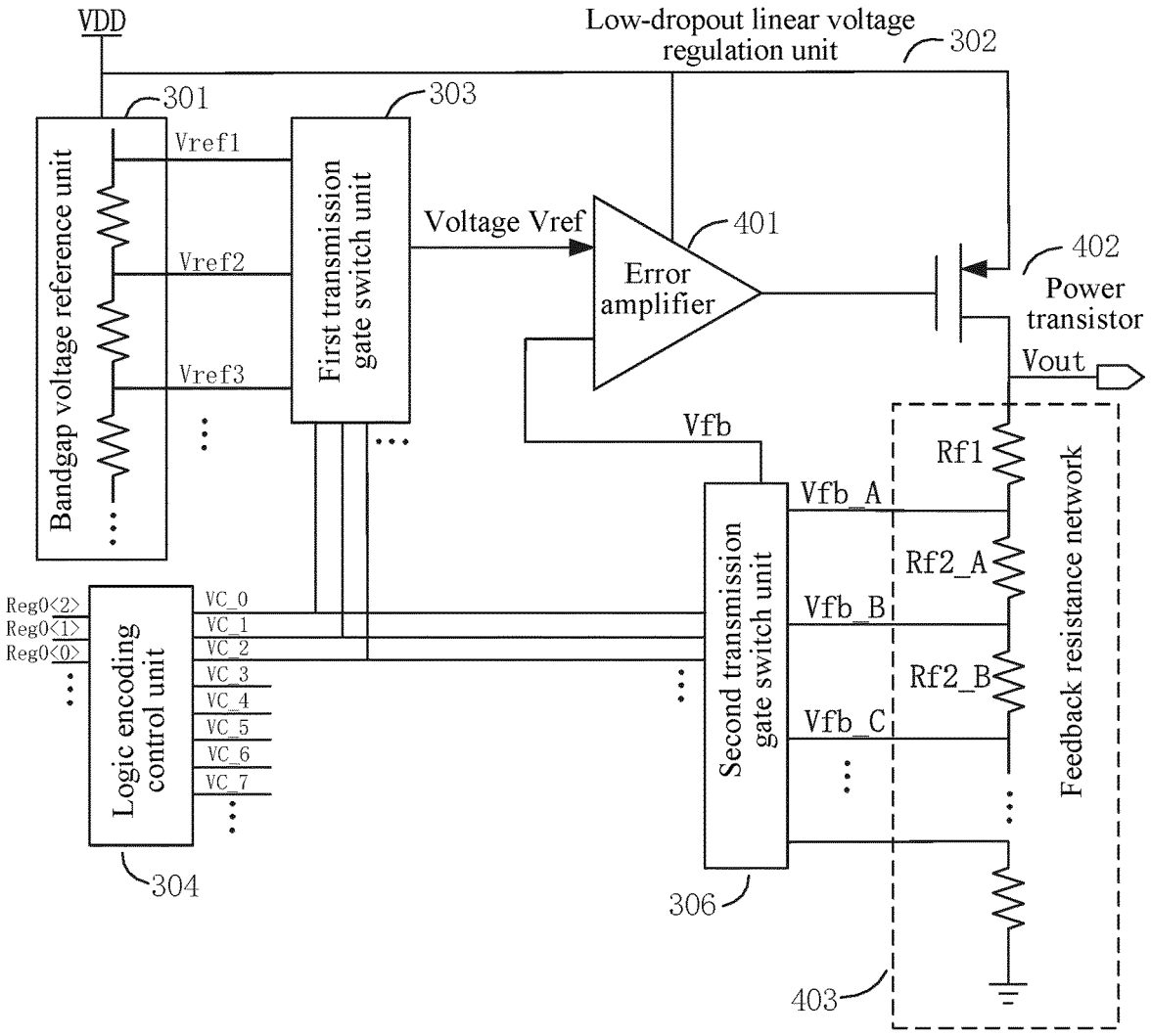
VDD
Low-dropout linear voltage regulation unit
302
301
303
Vref1
Vref2
Vref3
Bandgap voltage reference unit
First transmission gate switch unit
Voltage Vref
401
Error amplifier
402
Power transistor
Vout
Vfb
Rf1
Vfb_A
Rf2_A
Vfb_B
Rf2_B
Vfb_C
Feedback resistance network
Second transmission gate switch unit
Reg0<2>
Reg0<1>
Reg0<0>
VC_0
VC_1
VC_2
VC_3
VC_4
VC_5
VC_6
VC_7
Logic encoding control unit
304
306
403

FIG. 2

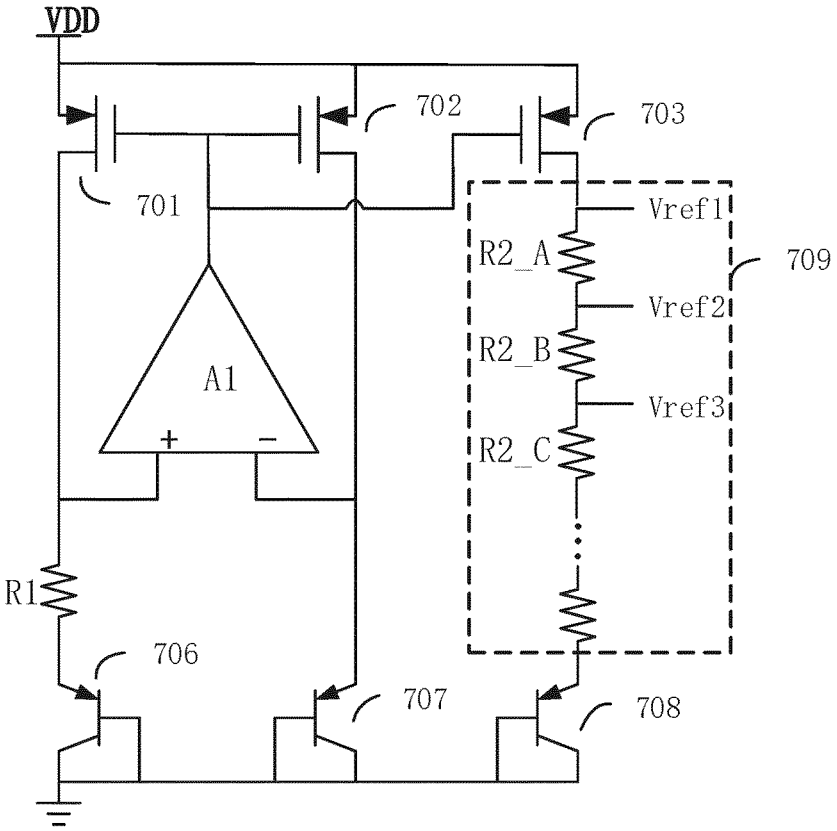
VDD
702
703
701
Vref1
R2_A
709
Vref2
R2_B
A1
+
−
Vref3
R2_C
R1
706
707
708

FIG. 3

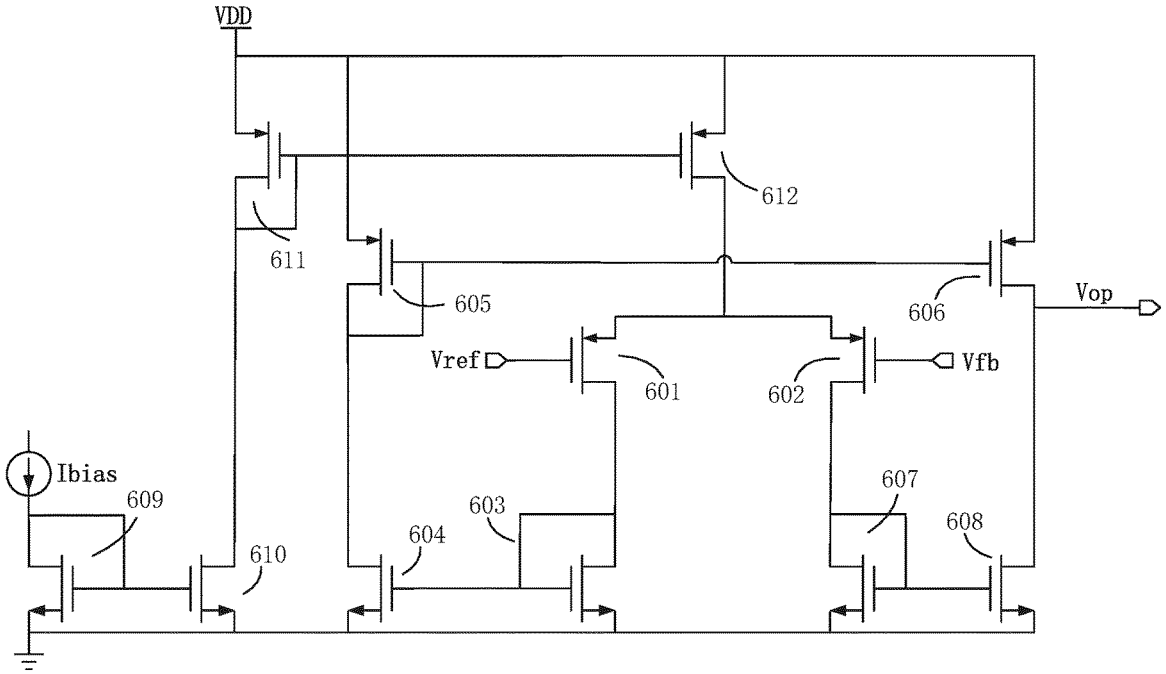
VDD
612
611
605
606
Vop
Vref
601
602
Vfb
Ibias
609
607
603
608
604
610

FIG. 4

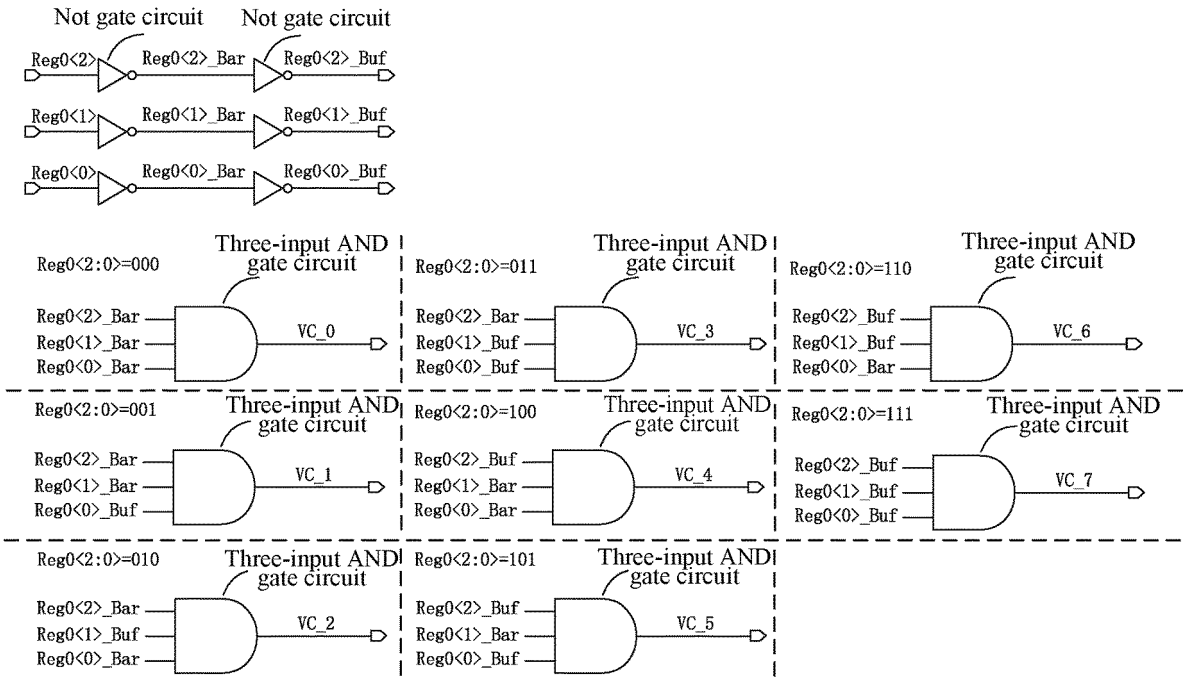
Not gate circuit
Not gate circuit
Reg0<2>
Reg0<2>_Bar
Reg0<2>_Buf
Reg0<1>
Reg0<1>_Bar
Reg0<1>_Buf
Reg0<0>
Reg0<0>_Bar
Reg0<0>_Buf
Reg0<2:0>=000
Three-input AND gate circuit
Reg0<2>_Bar
Reg0<1>_Bar
Reg0<0>_Bar
VC_0
Reg0<2:0>=011
Three-input AND gate circuit
Reg0<2>_Bar
Reg0<1>_Buf
Reg0<0>_Buf
VC_3
Reg0<2:0>=110
Three-input AND gate circuit
Reg0<2>_Buf
Reg0<1>_Buf
Reg0<0>_Bar
VC_6
Reg0<2:0>=001
Three-input AND gate circuit
Reg0<2>_Bar
Reg0<1>_Bar
Reg0<0>_Buf
VC_1
Reg0<2:0>=100
Three-input AND gate circuit
Reg0<2>_Buf
Reg0<1>_Bar
Reg0<0>_Bar
VC_4
Reg0<2:0>=111
Three-input AND gate circuit
Reg0<2>_Buf
Reg0<1>_Buf
Reg0<0>_Buf
VC_7
Reg0<2:0>=010
Three-input AND gate circuit
Reg0<2>_Bar
Reg0<1>_Buf
Reg0<0>_Bar
VC_2
Reg0<2:0>=101
Three-input AND gate circuit
Reg0<2>_Buf
Reg0<1>_Bar
Reg0<0>_Buf
VC_5

FIG. 5

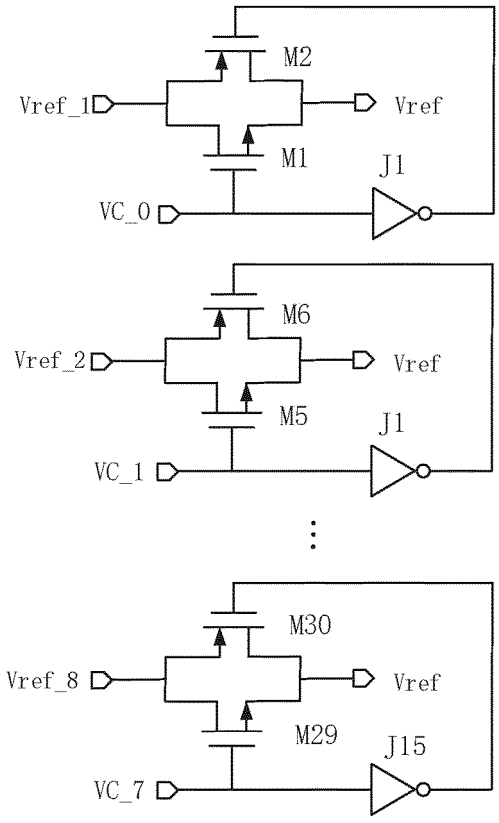
M2
Vref_1
Vref
M1
J1
VC_0
M6
Vref_2
Vref
M5
J1
VC_1
M30
Vref_8
Vref
M29
J15
VC_7

FIG. 6

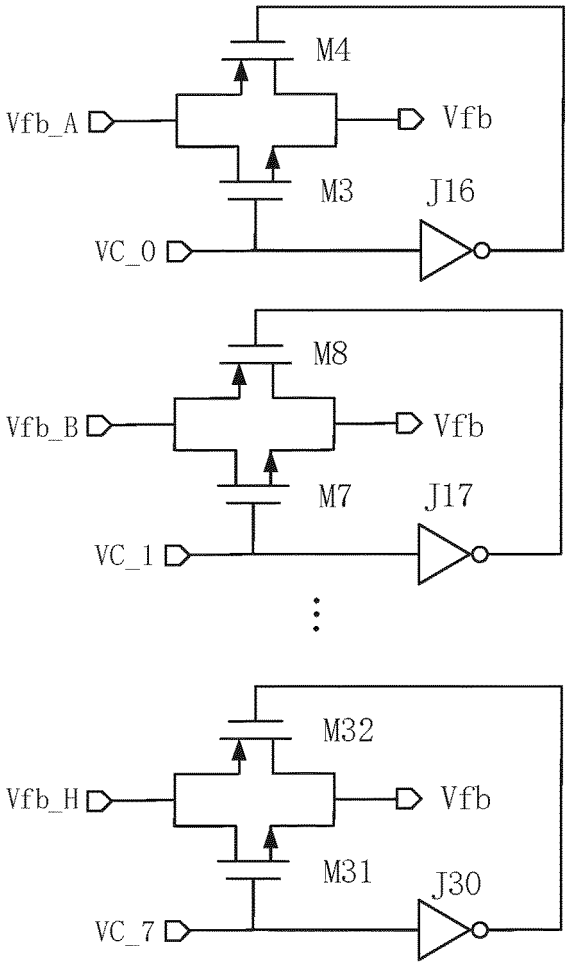
M4
Vfb_A
Vfb
M3
J16
VC_0
M8
Vfb_B
Vfb
M7
J17
VC_1
M32
Vfb_H
Vfb
M31
J30
VC_7

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2021/131898

A. CLASSIFICATION OF SUBJECT MATTER

G05F 1/567(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS; CNTXT; CNKI; VEN; USTXT; EPTXT; WOTXT: 输出, 可调, 调节, 调整, 逻辑, 编程, 编码, 低压差, 低压降, output, voltage, adjust+, regulat+, program+, cod+, LDO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 112327992 A (JINICP, TIANJIN ELECTRONIC TECHNOLOGY CO., LTD.) 05 February 2021 (2021-02-05) claims 1-10	1-10
X	CN 102289238 A (SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.) 21 December 2011 (2011-12-21) description, paragraphs [0020]-[0106], and figures 1-15	1-10
A	CN 106227282 A (NO.771 INSTITUTE OF NINTH ACADEMY OF CHINA AEROSPACE SCIENCE AND TECHNOLOGY CORPORATION) 14 December 2016 (2016-12-14) entire document	1-10
A	US 6177785 B1 (SAMSUNG ELECTRONICS CO., LTD.) 23 January 2001 (2001-01-23) entire document	1-10

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 January 2022	**29 January 2022**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2021/131898

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	112327992	A	05 February 2021	None			
CN	102289238	A	21 December 2011	CN	102289238	B	27 January 2016
				TW	201211716	A	16 March 2012
				TW	I537697	B	11 June 2016
				US	2011248688	A1	13 October 2011
				US	9411348	B2	09 August 2016
				HK	1165030	A0	28 September 2012
				HK	1165030	A1	17 March 2017
CN	106227282	A	14 December 2016	None			
US	6177785	B1	23 January 2001	KR	20000021487	A	25 April 2000
				KR	289846	B1	15 May 2001

Form PCT/ISA/210 (patent family annex) (January 2015)