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(54) DRIVING CIRCUIT AND DISPLAY DEVICE

(57) A drive circuit and a display apparatus are provided, to improve a charging/discharging rate of a capacitor in a liquid crystal display and reduce system power consumption. The drive circuit includes: a digital-to-analog converter (401), configured to output an analog signal; an amplifier (402), configured to generate a drive signal based on the analog signal, where the amplifier (402) includes an amplification circuit and a current source circuit, the amplification circuit is configured to amplify the analog signal, and the current source circuit is configured to provide a bias current for the amplification circuit in a controllable manner; and a comparison control circuit (403), configured to compare a voltage value of the drive signal with a preset voltage value, and control, based on a comparative result, the current source circuit to output the bias current.

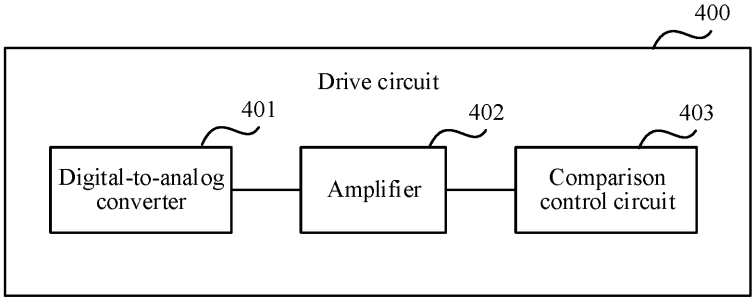


FIG. 4

EP 4 276 812 A1

Description

TECHNICAL FIELD

[0001] This application relates to the field of display technologies, and in particular, to a drive circuit and a display apparatus.

BACKGROUND

[0002] A liquid crystal display is an indispensable component of an electronic product such as a television or computer. Usually, a pixel unit of the liquid crystal display may include a resistor-capacitance (resistor-capacitance, RC) network. The RC network includes N*N pixel units, where N>1, and each pixel unit includes a capacitor 101 and a resistor 102. In each pixel unit, voltage values at two ends of the capacitor 101 are different, and correspond to different torsion angles of a liquid crystal. Charging/discharging of each capacitor 101 in the RC network is controlled, so that a torsion angle of the liquid crystal in the liquid crystal display may be controlled. Therefore, transmittance of the liquid crystal is controlled, to achieve different display effects.

[0003] A nematic liquid crystal display and a drive circuit thereof may be shown in FIG. 1. Multiple control signals are obtained by processing red green blue (red green blue, RGB) data by a data processing unit and an electrical level shifter, and each control signal is used to control a column of pixel units. Specifically, the multiple control signals are respectively input to multiple digital-to-analog converters (digital-to-analog converters, DACs), and each DAC is coupled to one column of pixel units by using one amplifier. A drive signal output by the amplifier controls turn-on and turn-off of a switching transistor 103 coupled to each pixel unit, to control charging/discharging of the capacitor 101, so as to achieve different display effects. The amplifier may also be referred to as a channel buffer (channel buffer) or an output buffer.

[0004] As resolution of the liquid crystal display increases (for example, from 4k to 8k), a size of the RC network increases (in other words, a quantity of pixel units increases), and load of the channel buffer increases accordingly. At the same time, as a data refresh rate of the liquid crystal display increases (for example, from 60 Hz to 120 Hz), a requirement for a charging/discharging rate of the channel buffer is also improved accordingly. It may be easily understood that people's increasing requirements for performance of the liquid crystal display require a drive circuit at a high charging/discharging rate.

[0005] To improve the charging/discharging rate of the channel buffer, a solution provided in a conventional technology provides a large bias current for the channel buffer within fixed duration (to be specific, a fast charging current is superimposed on an original bias current, to enlarge the bias current). Therefore, the channel buffer can quickly complete charging/discharging of the capacitor 101 in the liquid crystal display. As shown in FIG. 2, a load data (load data, LD) signal is an RGB data refresh flag, and a moment at which the LD signal jumps from a low electrical level to a high electrical level is a data refresh moment. When each frame of image is displayed, data usually needs to be refreshed for multiple times. A digital high driving (digital high driving, DHDR) signal is a flag signal indicating that a large bias current is supplied to a channel buffer. When the DHDR signal is at a high electrical level, the large bias current is supplied to the channel buffer (for example, a fast charging current is superimposed on an original bias current). When the DHDR signal is at a low electrical level, a small bias current is supplied to the channel buffer. DHDR duration is a fixed value.

[0006] By using the solution provided in the conventional technology, the DHDR duration is a fixed value. To ensure that the DHDR duration can meet different load requirements, the DHDR duration is usually set to a large value. Extremely high power consumption overheads may be caused by supplying the large bias current to the channel buffer for long duration. Each time data is refreshed, a load requirement sometimes is high and sometimes is low. To meet a high load requirement, the DHDR duration is set to a large fixed value. Consequently, system power consumption increases.

[0007] In conclusion, the drive solution provided in the conventional technology has a problem of high system power consumption.

SUMMARY

[0008] Embodiments of this application provide a drive circuit and a display apparatus, to improve a charging/discharging rate of a capacitor in a liquid crystal display and reduce system power consumption.

[0009] According to a first aspect, an embodiment of this application provides a drive circuit. The drive circuit includes: a digital-to-analog converter, configured to output an analog signal; an amplifier, configured to generate a drive signal based on the analog signal, where the amplifier includes an amplification circuit and a current source circuit, the amplification circuit is configured to amplify the analog signal, and the current source circuit is configured to provide a bias current for the amplification circuit in a controllable manner; and a comparison control circuit, configured to compare a voltage value of the drive signal with a preset voltage value, and control, based on a comparative result, the current source circuit to output the bias current.

[0010] The comparison control circuit may be implemented by using two functional modules: a comparator and a controller. The comparator is configured to compare the voltage value of the drive signal with the preset voltage value; and the controller is configured to control, based on the comparative result of the comparator, the current source circuit to output the bias current.

[0011] According to the foregoing solution, the current

source circuit in the amplifier may provide the bias current for the amplification circuit in a controllable manner. When the bias current of the amplification circuit is small, a charging/discharging rate of a capacitor in a liquid crystal display coupled to the amplification circuit is low. When the bias current of the amplification circuit is large, a charging/discharging rate of a capacitor in a liquid crystal display coupled to the amplification circuit is high. The comparison control circuit 403 compares the voltage value of the drive signal output by the amplifier with the preset voltage value, and controls, based on the comparative result, the current source circuit to output the bias current. In this test manner, the comparison control circuit can control, based on a real comparative result between the voltage value of the drive signal and the preset voltage value, the bias current provided by the current source circuit. This improves the charging/discharging rate of the capacitor in the liquid crystal display coupled to the drive circuit. Compared with a manner in which DHDR duration is set to a large fixed value in a conventional technology, the bias current provided by the current source circuit is controlled through testing by using the drive circuit, so that the bias current output by the current source circuit can be more accurately adapted to the capacitor in the liquid crystal display. This reduces system power consumption.

[0012] In a possible design, the digital-to-analog converter is specifically configured to: output the analog signal at a first moment; the current source circuit is specifically configured to: provide a first bias current for the amplification circuit before the first moment, and provide a second bias current for the amplification circuit at the first moment, where a current value of the second bias current is greater than a current value of the first bias current; and the controller is specifically configured to: determine that a difference between a second moment at which the drive signal is inverted and the first moment is fast charging duration, and control, based on the fast charging duration, the current source circuit to output the bias current.

[0013] According to the foregoing solution, when the second bias current is supplied to the amplification circuit, in a time period from the first moment to the second moment, the drive signal output by the amplifier can change from a maximum voltage value to a minimum voltage value or from a minimum voltage value to a maximum voltage value along with an input analog signal. Therefore, the fast charging duration determined according to the solution can meet charging/discharging time needed by all capacitors that are coupled to the operational amplifier and that are in the liquid crystal display.

[0014] Specifically, when controlling, based on the fast charging duration, the current source circuit to output the bias current, the controller is specifically configured to: each time the liquid crystal display coupled to the drive circuit refreshes data, control duration in which the current source circuit outputs the second bias current to be the fast charging duration.

[0015] In a possible design, a difference between a maximum voltage value and a minimum voltage value that are of the analog signal is greater than or equal to a maximum charging voltage value of a capacitor in the liquid crystal display coupled to the drive circuit, and the preset voltage value is the maximum voltage value or the minimum voltage value of the analog signal.

[0016] According to the foregoing solution, the difference between the maximum voltage value and the minimum voltage value that are of the analog signal may be set to be equal to the maximum charging voltage value of the capacitor in the liquid crystal display, or the difference between the maximum voltage value and the minimum voltage value that are of the analog signal may be set to be slightly greater than the maximum charging voltage value of the capacitor in the liquid crystal display. In this way, the fast charging duration determined according to the foregoing solution can meet charging/discharging requirements of all capacitors in the liquid crystal display, and the fast charging duration can be shortened as much as possible. Therefore, system power consumption is reduced.

[0017] In a possible design, the analog signal is a first step signal, and a voltage value of the first step signal increases from a first voltage value to a second voltage value at the first moment; and the comparator is configured to compare the voltage value of the drive signal with the second voltage value, and a moment at which an output signal of the comparator is inverted from a low electrical level to a high electrical level is the second moment.

[0018] According to the foregoing solution, in the time period from the first moment to the second moment, the drive signal can increase from the minimum voltage value of the analog signal to the maximum voltage value of the analog signal along with the input analog signal. Because the difference between the maximum voltage value and the minimum voltage value that are of the analog signal is greater than or equal to the maximum charging voltage value of the capacitor in the liquid crystal display, the fast charging duration determined according to the solution can meet the charging/discharging time needed by all the capacitors that are coupled to the amplifier and that are in the liquid crystal display.

[0019] In another possible design, the analog signal is a second step signal, and a voltage value of the second step signal decreases from a third voltage value to a fourth voltage value at the first moment; and the comparator is configured to compare the voltage value of the drive signal with the fourth voltage value, and a moment at which an output signal of the comparator is inverted from a high electrical level to a low electrical level is the second moment.

[0020] According to the foregoing solution, in the time period from the first moment to the second moment, the drive signal can decrease from the maximum voltage value of the analog signal to the minimum voltage value of the analog signal along with the input analog signal. Be-

cause the difference between the maximum voltage value and the minimum voltage value that are of the analog signal is greater than or equal to the maximum charging voltage value of the capacitor in the liquid crystal display, the fast charging duration determined according to the solution can meet the charging/discharging time needed by all the capacitors that are coupled to the amplifier and that are in the liquid crystal display.

[0021] In addition, both the first moment and the second moment may fall within a blanking region between a first frame of image and a second frame of image that are displayed by the liquid crystal display, and display time of the first frame of image is earlier than display time of the second frame of image.

[0022] According to the foregoing solution, when the liquid crystal display displays an image, there is a blanking region interval before each frame of displayed image is refreshed, and there is no signal input in the liquid crystal display in a time period of the blanking region. A viewer does not visually perceive that the liquid crystal display does not display an image in the time period of the blanking region. Therefore, the foregoing solution of determining fast charging duration may be performed in the time period of the blanking region after the first frame of image is displayed and before the second frame of image is not displayed.

[0023] In a possible design, the digital-to-analog converter is further configured to: perform digital-to-analog conversion on a digital control signal corresponding to the second frame of image, to obtain an analog control signal; the amplification circuit is further configured to amplify the analog control signal; and the controller is further configured to: control the current source circuit to output the second bias current at a third moment at which the amplification circuit receives the analog control signal, and control the current source circuit to output the first bias current at a fourth moment, where a time difference between the fourth moment and the third moment is the fast charging duration.

[0024] According to the foregoing solution, it is determined that the fast charging duration may be applied to display of the second frame of image after the second moment.

[0025] In a possible design, the drive circuit provided in the first aspect may further include: a data processing unit, configured to perform serial-to-parallel conversion on red green blue RGB data to obtain parallel RGB data; and an electrical level shifter, coupled to the data processing unit and configured to perform shift processing on the parallel RGB data to obtain the foregoing digital control signal.

[0026] In a possible design, the first moment is a moment at which the liquid crystal display refreshes data.

[0027] According to the foregoing solution, when each frame of image is displayed, the liquid crystal display needs to refresh data for multiple times. During actual application, an LD signal may be used to indicate the liquid crystal display to refresh data. For example, the LD signal may be a periodic pulse signal, and a moment at which the LD signal jumps from a low electrical level to a high electrical level (that is, a moment at which the LD signal is valid) is the moment at which the liquid crystal display refreshes data. The LD signal is a periodic signal, and the LD signal is output no matter when the liquid crystal display displays an image or in a blanking region before the image is displayed. The digital-to-analog converter may choose to output the analog signal to the amplifier at the first moment at which the LD signal is valid, and the amplifier also increases the bias current (from the first bias current to the second bias current) at the first moment.

[0028] According to a second aspect, an embodiment of this application further provides a display apparatus. The display apparatus includes a liquid crystal display and the drive circuit provided in any one of the first aspect and the possible designs of the first aspect.

[0029] It should be noted that, for technical effects brought by any one of the second aspect and the possible designs of the second aspect, refer to technical effects brought by different designs in the first aspect. Details are not described herein again.

BRIEF DESCRIPTION OF DRAWINGS

[0030]

FIG. 1 is a schematic structural diagram of a liquid crystal display and a drive circuit thereof according to a conventional technology;

FIG. 2 is a sequence diagram of an LD signal and a DHDR signal according to a conventional technology;

FIG. 3 is a schematic structural diagram of an amplifier according to an embodiment of this application;

FIG. 4 is a schematic structural diagram of a first drive circuit according to an embodiment of this application;

FIG. 5 is a schematic structural diagram of a second drive circuit according to an embodiment of this application;

FIG. 6 is a signal sequence diagram of a drive circuit according to an embodiment of this application;

FIG. 7 is a schematic structural diagram of a third drive circuit according to an embodiment of this application;

FIG. 8 is a signal sequence diagram of another drive circuit according to an embodiment of this application; and

FIG. 9 is a schematic structural diagram of a display apparatus according to an embodiment of this application.

DESCRIPTION OF EMBODIMENTS

[0031] The following first describes an application sce-

nario in embodiments of this application.

[0032] Embodiments of this application may be applied to a display apparatus shown in FIG. 1. The display apparatus includes a liquid crystal display and a drive circuit. The drive circuit controls transmittance of a liquid crystal in the liquid crystal display based on received RGB data, to achieve different display effects.

[0033] Specifically, a data processing unit in the drive circuit is configured to perform serial-to-parallel conversion on the RGB data to output parallel RGB data. An electrical level shifter is configured to perform shift processing on the parallel RGB data to obtain multiple control signals. A DAC is configured to perform digital-to-analog conversion on a control signal. An amplifier is configured to buffer and output the control signal to obtain a drive signal.

[0034] Specifically, the liquid crystal display includes a resistor-capacitance (resistor-capacitance, RC) network. The RC network includes N*N pixel units, where N>1, and each pixel unit includes a capacitor 101 and a resistor 102. Each pixel unit is further coupled to a switching transistor 103, and the drive signal output by the amplifier is used to control turn-on time and turn-off time of the switching transistor 103, and further control a charging/discharging process of the capacitor 101 in the pixel unit. Each group of DACs and amplifiers is configured to control a column of pixel units in the liquid crystal display.

[0035] In addition, the display apparatus shown in FIG. 1 further includes a row driver (Row Driver). The row driver is coupled to a control end (for example, a gate electrode or a base electrode) of the switching transistor 103 in the liquid crystal display, and the row driver cooperates with the drive circuit to control turn-on and turn-off of the switching transistor 103.

[0036] It should be noted that, in embodiments of this application, when an image is displayed, specific functions and operations of the data processing unit, the electrical level shifter, and the DAC in the drive circuit may use the conventional technology. Details are not described herein. In embodiments of this application, only how to improve a charging/discharging rate and reduce system power consumption when the capacitor 101 in the liquid crystal display is charged/discharged by using the drive circuit is concerned.

[0037] During actual application, when the capacitor 101 in the liquid crystal display is charged/discharged by using the drive circuit, a large bias current may be supplied to a power supply end of the amplifier, to improve a charging/discharging rate of the capacitor 101 in the liquid crystal display. Specifically, when each frame of image is displayed, the liquid crystal display needs to refresh data for multiple times. Each time the data is refreshed, the large bias current may be supplied to the power supply end of the amplifier.

[0038] FIG. 3 is a schematic structural diagram of an amplifier, where V_{in} is an input end of the amplifier, and V_{out} is an output end of the amplifier. In FIG. 3, Example a shows an overall structure of the amplifier, and Example b shows an internal structure of the amplifier. In Example b, V_{DD} is a power supply end of the amplifier, and is configured to input a bias current. A small bias current is supplied to the power supply end of the amplifier, in other words, a bias current Iss is supplied to the power supply end. A large bias current is supplied to the power supply end of the amplifier, in other words, I1 is superimposed on Iss that is supplied to the power supply end, and a current value of I1 is large. When a bias current of the amplifier is large, a charging/discharging rate of a capacitor 101 in a pixel unit coupled to the amplifier is high.

[0039] Although the charging/discharging rate of the capacitor 101 can be improved by supplying the large bias current to the power supply end of the amplifier, extremely high power consumption overheads may be caused by supplying the large bias current to the amplifier for long duration. Therefore, how to determine duration in which the large bias current is supplied to the amplifier, to enable the charging duration to meet a load requirement (meet a fast charging/discharging requirement of the capacitor 101) without causing high system power consumption overheads, is an implementation objective of embodiments of this application.

[0040] The following further describes embodiments of this application in detail with reference to accompanying drawings.

[0041] It should be noted that "multiple" in embodiments of this application means two or at least two. In addition, in the descriptions of this application, terms such as "first" and "second" are merely used for distinction and description, and shall not be understood as an indication or implication of relative importance, or as an indication or implication of an order.

[0042] An embodiment of this application provides a drive circuit. Refer to FIG. 4. A drive circuit 400 includes a digital-to-analog converter 401, an amplifier 402, and a comparison control circuit 403.

[0043] The digital-to-analog converter 401 is configured to output an analog signal. The amplifier 402, coupled to the digital-to-analog converter 401, is configured to generate a drive signal based on the analog signal. The amplifier 402 includes an amplification circuit and a current source circuit, the amplification circuit is configured to amplify the analog signal, and the current source circuit is configured to provide a bias current for the amplification circuit in a controllable manner. The comparison control circuit 403 is configured to compare a voltage value of the drive signal with a preset voltage value, and control, based on a comparative result, the current source circuit to output the bias current.

[0044] During actual application, the drive circuit 400 may be coupled to a liquid crystal display, and the drive circuit 400 controls charging/discharging of a capacitor in the liquid crystal display, to control a torsion angle of a liquid crystal in the liquid crystal display. Therefore, transmittance of the liquid crystal is controlled, to achieve different display effects.

[0045] In the drive circuit 400, the amplification circuit

may be an operational amplifier. The current source circuit is configured to provide the bias current for the amplification circuit. Specifically, a magnitude of the bias current provided by the current source circuit for the amplification circuit may be controlled by the comparison control circuit 403. When a current value of the bias current provided by the current source circuit is small, a rate of charging/discharging the capacitor in the liquid crystal display by using the drive circuit 400 is low. When a current value of the bias current provided by the current source circuit is large, a rate of charging/discharging the capacitor in the liquid crystal display by using the drive circuit 400 is high.

[0046] Specifically, the comparison control circuit 403 may include a comparator and a controller. The comparator is configured to compare the voltage value of the drive signal with the preset voltage value; and the controller is configured to control, based on the comparative result of the comparator, the current source circuit to output the bias current. In other words, functions of the comparison control circuit 403 may be implemented by using two functional modules.

[0047] Further, the digital-to-analog converter 401 is specifically configured to output the analog signal at a first moment (which is referred to as a moment T1 for short). The current source circuit is specifically configured to: provide a first bias current for the amplification circuit before the first moment, and provide a second bias current for the amplification circuit at the first moment, where a current value of the second bias current is greater than a current value of the first bias current. The controller is specifically configured to: determine that a difference between a second moment (which is referred to as a moment T2 for short) at which an output signal of the comparator is inverted is fast charging duration, and control, based on the fast charging duration, the current source circuit to output the bias current.

[0048] It may be easily learned that the current source circuit provides a large bias current for the amplification circuit from the moment T1. As the bias current increases, the drive signal output by the amplification circuit changes. The output signal of the comparator changes as the drive signal changes. The moment at which the output signal of the comparator is inverted is defined as the moment T2. The time difference between the moment T2 and the moment T1 is the fast charging duration. The controller may control, based on the fast charging duration, the current source to output the bias current.

[0049] Specifically, each time the liquid crystal display coupled to the drive circuit 400 refreshes data, the controller may control duration in which the current source circuit outputs the second bias current to be the fast charging duration. In other words, duration in which the large bias current is supplied to the amplification circuit is controlled to be the fast charging duration.

[0050] It is assumed that duration for refreshing data once is Tr, and the fast charging duration is Tf. In this case, within a Tr time period, the controller may control duration in which the current source circuit provides the second bias current (the large bias current) for the amplification circuit to be Tf, and control duration in which the current source circuit provides the first bias current (a small bias current) for the amplification circuit to be Tr-Tf.

[0051] When the liquid crystal display refreshes data, the bias current of the amplification circuit is increased. This can improve the charging/discharging rate of the capacitor in the liquid crystal display. Therefore, a data refresh rate of the liquid crystal display and performance of the liquid crystal display are improved.

[0052] Specifically, the drive circuit 400 may perform the foregoing solution in a blanking region (V-Blanking) between a first frame of image and a second frame of image, to determine the fast charging duration. Display time of the first frame of image is earlier than display time of the second frame of image. In other words, both the moment T1 and the moment T2 fall within the blanking region between the first frame of image and the second frame of image that are displayed by the liquid crystal display.

[0053] When the liquid crystal display displays an image, there is a blanking region interval before each frame of the displayed image is refreshed, and there is no signal input in the liquid crystal display in a V-Blanking time period. A viewer does not visually perceive that the liquid crystal display does not display an image in the V-Blanking time period. Therefore, the foregoing solution of determining the fast charging duration may be performed in the V-Blanking time period after the first frame of image is displayed and before the second frame of image is not displayed. Then, after the second moment, the fast charging duration is applied when the liquid crystal display refreshes data.

[0054] It should be noted that the fast charging duration obtained by using the solution provided in this embodiment of this application may be applied only to display of the second frame of image, or may be applied to display of another image after the second frame of image. An application scope of the fast charging duration is not specifically limited in this embodiment of this application.

[0055] In a specific example, the drive circuit 400 may perform the foregoing solution in a blanking region before each frame of image is displayed, and the obtained fast charging duration is applied only to display of a next frame image.

[0056] In another example, the drive circuit 400 may perform the foregoing solution only once, and the obtained fast charging duration is applied to display of all images.

[0057] In still another example, the drive circuit 400 may periodically perform the foregoing solution, and the obtained fast charging duration is applied to display of all images in one periodicity. For example, each time five frames of images are displayed, the drive circuit 400 performs the foregoing solution once, and the obtained fast charging duration is applied to display of next five frames

of images.

[0058] When the fast charging duration is applied to the display of the second frame of image after the second moment, specifically, when the second frame of image is displayed, the digital-to-analog converter 401 is further configured to: perform digital-to-analog conversion on a digital control signal corresponding to the second frame of image to obtain an analog control signal; the amplification circuit is further configured to amplify the analog control signal; and the controller is further configured to: control the current source circuit to output the second bias current at a third moment at which the amplification circuit receives the analog control signal, and control the current source circuit to output the first bias current at a fourth moment, where a time difference between the fourth moment and the third moment is the fast charging duration.

[0059] That is, the controller controls the duration in which the current source circuit outputs the second bias current (the large bias current) to be the fast charging duration.

[0060] As described above, when the second frame of image is displayed, the liquid crystal display needs to refresh data for multiple times. In this case, when the second frame of image is displayed, it is assumed that the duration for refreshing data once is Tr, and the fast charging duration is Tf. In this case, within the Tr time period, the controller may control the duration in which the current source circuit provides the second bias current (the large bias current) for the amplification circuit to be Tf, and control the duration in which the current source circuit provides the first bias current (the small bias current) for the amplification circuit to be Tr-Tf.

[0061] In addition, the drive circuit 400 may further include: a data processing unit, configured to perform serial-to-parallel conversion on RGB data input to the drive circuit 400 to obtain parallel RGB data; and an electrical level shifter, coupled to the data processing unit and configured to perform shift processing on the parallel RGB data to obtain the digital control signal corresponding to the second frame of image.

[0062] The foregoing describes an execution occasion of the solution in this embodiment of this application and application of the fast charging duration, and the following describes a specific solution for determining the fast charging duration in this embodiment of this application.

[0063] In this embodiment of this application, the digital-to-analog converter 401 outputs the analog signal to the amplifier 402 at the moment T1, and the bias current supplied to a power supply end of the amplifier 402 increases from the first bias current to the second bias current at the moment T1. After the foregoing steps are performed, the drive signal output by the amplifier 402 changes as an input analog signal changes. The comparison control circuit 403 compares the drive signal output by the amplifier 402 with the preset voltage value (a maximum voltage value or a minimum voltage value of the analog signal), and defines the moment at which the output signal of the comparison control circuit 403 is inverted as the moment T2, where the difference between the moment T2 and the moment T1 is the fast charging duration.

[0064] The difference between the moment T2 and the moment T1 may be collected by using a pulse sample circuit (pulse sample circuit) in the controller. For a specific structure and function of the pulse sample circuit, refer to descriptions in a conventional technology. Details are not described herein.

[0065] In addition, in this embodiment of this application, the first moment may be a moment at which the liquid crystal display refreshes data.

[0066] As described above, when each frame of image is displayed, the liquid crystal display needs to refresh data for multiple times. During actual application, an LD signal may be used to indicate the liquid crystal display to refresh data. For example, the LD signal may be a periodic pulse signal, and a moment at which the LD signal jumps from a low electrical level to a high electrical level (that is, a moment at which the LD signal is valid) is the moment at which the liquid crystal display refreshes data. It should be noted that the LD signal is a periodic signal, and the LD signal is output no matter when the liquid crystal display displays an image or in a blanking region before the liquid crystal display displays an image. In this case, the LD signal is also output in the blanking region between the first frame of image and the second frame of image. When the solution in this embodiment of this application is performed, the digital-to-analog converter 401 may choose to output the analog signal to the amplifier 402 at the moment T1 at which the LD signal is valid, and the bias current of the amplifier 402 is also increased from the first bias current to the second bias current at the moment T1.

[0067] In this embodiment of this application, a difference between the maximum voltage value and the minimum voltage value of the analog signal is greater than or equal to a maximum charging voltage value of the capacitor in the liquid crystal display. Specifically, there may be multiple types of analog signals, and the following describes different types of analog signals by using several specific examples.

Example 1

[0068] The analog signal may be a first step signal, and a voltage value of the first step signal increases from a first voltage value to a second voltage value at the first moment. The comparison control circuit 403 is configured to compare the voltage value of the drive signal with the second voltage value, and a moment at which the output signal of the comparison control circuit 403 is inverted from a low electrical level to a high electrical level is the second moment.

[0069] It may be easily learned that, in Example 1, the minimum voltage value of the analog signal is the first voltage value, and the maximum voltage value is the sec-

ond voltage value.

[0070] In this embodiment of this application, when the first step signal is input to the amplifier 402, the second bias current is supplied to the power supply end of the amplifier 402. The amplifier 402 buffers and outputs the first step signal. Under a joint action of the first step signal and the second bias current, the amplifier 402 charges the capacitor in the liquid crystal display. The voltage value of the drive signal output by the amplifier 402 gradually increases from the first voltage value. The comparison control circuit 403 compares the voltage value of the drive signal with the maximum voltage value of the analog signal (namely, the second voltage value). When the voltage value of the drive signal increases to the second voltage value, the output signal of the comparison control circuit 403 is inverted from a low electrical level to a high electrical level, and the moment at which the output signal of the comparison control circuit 403 is inverted is defined as the moment T2, where the difference between the moment T2 and the moment T1 is the fast charging duration.

[0071] It should be noted that, in Example 1, the comparison control circuit 403 is configured to compare the voltage value of the drive signal with the maximum voltage value of the analog signal. To be specific, a non-inverting input end of the comparator in the comparison control circuit 403 is configured to receive the drive signal, and an inverting input end is configured to receive the maximum voltage value of the analog signal (namely, the second voltage value). Therefore, when the voltage value of the drive signal is less than the maximum voltage value of the analog signal, the comparison control circuit 403 outputs a low electrical level. When the voltage value of the drive signal is greater than or equal to the maximum voltage value of the analog signal, the comparison control circuit 403 outputs a high electrical level. In this case, when the voltage value of the drive signal increases to the maximum voltage value of the analog signal, the output signal of the comparison control circuit 403 is inverted from a low electrical level to a high electrical level. The moment at which the output signal of the comparison control circuit 403 is inverted from a low electrical level to a high electrical level is the moment T2. If a received signal of the non-inverting input end of the comparator and a received signal of the inverting input end of the comparator are exchanged (to be specific, the non-inverting input end of the comparator is configured to receive the maximum voltage value of the analog signal, and the inverting input end is configured to receive the drive signal), the output signal of the comparison control circuit 403 is inverted from a high electrical level to a low electrical level when the voltage value of the drive signal increases to the maximum voltage value of the analog signal. A moment at which the output signal of the comparison control circuit 403 is inverted from a high electrical level to a low electrical level is the moment T2.

[0072] In a time period from the moment T1 to the moment T2, the drive signal output by the amplifier 402 can increase from the minimum voltage value of the analog signal to the maximum voltage value of the analog signal along with the input analog signal. Because the difference between the maximum voltage value and the minimum voltage value of the analog signal is greater than or equal to the maximum charging voltage value of the capacitor in the liquid crystal display, the fast charging duration determined according to the solution can meet charging/discharging time needed by all capacitors that are coupled to the amplifier 402 and that are in the liquid crystal display.

[0073] During actual application, a voltage applied to the liquid crystal in the liquid crystal display (in other words, the voltage applied to the capacitor) may be referred to as a gamma voltage, and the gamma voltage may be represented by VGMA<1>, VGMA<2>, VGMA<3>, ..., and VGMA<14>. VGMA<1> corresponds to a smallest voltage value, VGMA<14> corresponds to a largest voltage value, and voltage values corresponding to VGMA<1>→VGMA<14> increase in ascending order. For a capacitor in the liquid crystal display, a voltage change range of the capacitor may be 0 to VGMA<7>, for example, corresponding to 0 V to 9 V, or may be VGMA<8> to VGMA<14>, for example, corresponding to 9 V to 18 V It may be easily learned that, in the liquid crystal display, the maximum charging voltage value of the capacitor is 9 V In this case, in Example 1, the minimum voltage value of the first step signal (namely, the first voltage value) may be 0 V, and the maximum voltage value of the first step signal (namely, the second voltage value) may be VGMA<7>.

[0074] FIG. 5 is a schematic diagram of a drive circuit according to an embodiment of this application. The drive circuit includes a DAC, an amplifier AMP, a current source circuit, and a comparator Comp. In addition, the drive circuit may further include a controller, not shown in FIG. 5. The DAC inputs a digital signal and outputs an analog signal after digital-to-analog conversion. The output analog signal is a step signal (which may also be referred to as a Hline pattern signal) that jumps from 0 to VGMA<7>, and a bias current of the AMP is increased by using the current source circuit. In this case, an AHDR signal is set to a high electrical level. The AHDR signal is a signal that is defined in embodiments of this application and that indicates fast charging duration. A moment at which the AHDR signal jumps to a high electrical level may be understood as the foregoing moment T1. An output signal CH1 of the AMP is compared with a high reference voltage VGMA<7> output by a gamma voltage generation circuit. After the AMP completes charging of a capacitor in a liquid crystal display, the CH1 outputs the high reference voltage VGMA<7>, and magnitudes of the CH1 and the high reference voltage VGMA<7> can be determined by using a comparator Comp having an offset voltage. When an output of the comparator is high, the AHDR becomes low (where a moment at which the AHDR signal becomes low may be understood as the foregoing moment T2), and bias current increase is

stopped. An AHDR effective width, namely, the foregoing fast charging duration, is obtained through sampling by the controller (not shown in FIG. 5). After a V-Blanking interval ends, a large bias current interval whose width is the same as the AHDR width is provided for the AMP during each data refresh (LD), to achieve fast charging.

[0075] FIG. 6 is a sequence diagram of signals in the drive circuit shown in FIG. 5. It may be seen from FIG. 6 that, when the foregoing solution is performed in a V-Blanking interval, the DAC outputs the Hline pattern signal to the AMP at a moment at which LD is valid. In this case, the AHDR signal is set to a high electrical level. The output CH1 of the AMP gradually increases from 0 to VGMA<7>. When the CH1 reaches VGMA<7>, the output of the Comp changes from a low electrical level to a high electrical level. In this case, the AHDR signal is set to a low electrical level. Duration in which the AHDR signal is at a high electrical level is the fast charging duration. When an image is displayed subsequently (that is, an active interval), the fast charging duration is used as acceleration duration for the AMP during each data refresh.

Example 2

[0076] The analog signal may be a second step signal, and a voltage value of the second step signal decreases from a third voltage value to a fourth voltage value at the first moment. The comparison control circuit 403 is configured to compare the voltage value of the drive signal with the fourth voltage value, and a moment at which the output signal of the comparison control circuit 403 is inverted from a high electrical level to a low electrical level is the second moment.

[0077] It may be easily learned that, in Example 2, the minimum voltage value of the analog signal is the fourth voltage value, and the maximum voltage value is the third voltage value.

[0078] In this embodiment of this application, when the second step signal is input to the amplifier 402, the second bias current is supplied to the power supply end of the amplifier 402. The amplifier 402 buffers and outputs the second step signal. Under a joint action of the second step signal and the second bias current, the amplifier 402 discharges the capacitor in the liquid crystal display. In addition, the voltage value of the drive signal output by the amplifier 402 gradually decreases from the third voltage value. The comparison control circuit 403 compares the voltage value of the drive signal with the minimum voltage value of the analog signal (namely, the fourth voltage value). When the voltage value of the drive signal decreases to the fourth voltage value, the output signal of the comparison control circuit 403 is inverted from a high electrical level to a low electrical level, and the moment at which the output signal of the comparison control circuit 403 is inverted is defined as the moment T2, where a difference between the moment T2 and the moment T1 is the fast charging duration.

[0079] It should be noted that, in Example 2, the comparison control circuit 403 is configured to compare the voltage value of the drive signal with the minimum voltage value of the analog signal. To be specific, a non-inverting input end of the comparator in the comparison control circuit 403 is configured to receive the drive signal, and an inverting input end is configured to receive the minimum voltage value of the analog signal (namely, the fourth voltage value). Therefore, when the voltage value of the drive signal is greater than the minimum voltage value of the analog signal, the comparison control circuit 403 outputs a high electrical level. When the voltage value of the drive signal is less than or equal to the minimum voltage value of the analog signal, the comparison control circuit 403 outputs a low electrical level. In this case, when the voltage value of the drive signal decreases to the minimum voltage value of the analog signal, the output signal of the comparison control circuit 403 is inverted from a high electrical level to a low electrical level. A moment at which the output signal of the comparison control circuit 403 is inverted from a high electrical level to a low electrical level is the moment T2. If a received signal of the non-inverting input end of the comparator and a received signal of the inverting input end of the comparator are exchanged (to be specific, the non-inverting input end of the comparator is configured to receive the minimum voltage value of the analog signal, and the inverting input end is configured to receive the drive signal), the output signal of the comparison control circuit 403 is inverted from a low electrical level to a high electrical level when the voltage value of the drive signal decreases to the minimum voltage value of the analog signal. A moment at which the output signal of the comparison control circuit 403 is inverted from a low electrical level to a high electrical level is the moment T2.

[0080] In a time period from the moment T1 to the moment T2, the drive signal output by the amplifier 402 can decrease from the maximum voltage value of the analog signal to the minimum voltage value of the analog signal along with the input analog signal. Because the difference between the maximum voltage value and the minimum voltage value of the analog signal is greater than or equal to the maximum charging voltage value of the capacitor in the liquid crystal display, the fast charging duration determined according to the solution can meet charging/discharging time needed by all capacitors that are coupled to the amplifier 402 and that are in the liquid crystal display.

[0081] FIG. 7 is a schematic diagram of a drive circuit according to an embodiment of this application. The drive circuit includes a DAC, an amplifier AMP, a current source circuit, and a comparator Comp. In addition, the drive circuit may further include a controller, not shown in FIG. 7. The DAC inputs a digital signal and outputs an analog signal after digital-to-analog conversion. The output analog signal is a step signal that jumps from VGMA<14> to VGMA<8>, and a bias current of the AMP is increased by using the current source circuit. In this case,

an AHDR signal is set to a high electrical level. The AHDR signal is a signal that is defined in embodiments of this application and that indicates fast charging duration. A moment at which the AHDR signal jumps to a high electrical level may be understood as the foregoing moment T1. An output CH1 of the AMP is compared with a low reference voltage VGMA<8> output by a gamma voltage generation circuit. After the AMP completes discharging of a capacitor in a liquid crystal display, the CH1 outputs the low reference voltage VGMA<8>, and magnitudes of the CH1 and the low reference voltage VGMA<8> can be determined by using a comparator Comp having an offset voltage. When an output of the comparator is low, the AHDR becomes low (where a moment at which the AHDR signal becomes low may be understood as the foregoing moment T2), and bias current increase is stopped. An AHDR effective width, namely, the foregoing fast charging duration, is obtained through sampling by the controller (not shown in FIG. 7). After a V-Blanking interval ends, a large bias current interval whose width is the same as the AHDR width is provided for the AMP during each data refresh (LD), to achieve fast charging.

[0082] FIG. 8 is a sequence diagram of signals in the drive circuit shown in FIG. 7. It may be seen from FIG. 8 that, when the foregoing solution is performed in a V-Blanking interval, the DAC outputs the Hline pattern signal to the AMP at a moment at which LD is valid. In this case, the AHDR signal is set to a high electrical level. The output CH1 of the AMP gradually decreases from VGMA<14> to VGMA<8>. When the CH1 reaches VGMA<8>, the output of the Comp changes from a high electrical level to a low electrical level. In this case, the AHDR signal is set to a low electrical level. Duration in which the AHDR signal is at a high electrical level is the fast charging duration. When an image is displayed subsequently (that is, an active interval), the fast charging duration is used as acceleration duration for the AMP during each data refresh.

[0083] It should be noted that, in embodiments of this application, the current source circuit in the amplifier 402 may provide the bias current for the amplification circuit in a controllable manner. When the bias current of the amplification circuit is small, the charging/discharging rate of the capacitor in the liquid crystal display coupled to the amplification circuit is low. When the bias current of the amplification circuit is large, the charging/discharging rate of the capacitor in the liquid crystal display coupled to the amplification circuit is high. The comparison control circuit 403 compares the voltage value of the drive signal output by the amplifier 402 with the preset voltage value, and controls, based on the comparative result, the current source circuit to output the bias current. In this test manner, the comparison control circuit can control, based on a real comparative result between the voltage value of the drive signal and the preset voltage value, the bias current provided by the current source circuit. This improves the charging/discharging rate of the capacitor in the liquid crystal display coupled to the drive circuit 400. Compared with a manner in which DHDR duration is set to a large fixed value in the conventional technology, the bias current provided by the current source circuit is controlled through testing by using the drive circuit 400, so that the bias current output by the current source circuit can be more accurately adapted to the capacitor in the liquid crystal display. This reduces system power consumption.

[0084] Further, the current source circuit may be set to provide the first bias current for the amplification circuit before the first moment, and provide the second bias current for the amplification circuit at the first moment, where a current value of the second bias current is greater than a current value of the first bias current. The controller in the comparison control circuit 403 determines the difference between the second moment at which the comparator in the comparison control circuit 403 is inverted and the first moment as the fast charging duration. In this case, when the second bias current is supplied to the amplifier 402, in the time period from the first moment to the second moment, the drive signal can change from the maximum voltage value to the minimum voltage value or from the minimum voltage value to the maximum voltage value along with the input analog signal. Therefore, the fast charging duration determined according to the solution can meet charging/discharging time needed by all capacitors that are coupled to the amplifier 402 and that are in the liquid crystal display. In addition, the difference between the maximum voltage value and the minimum voltage value that are of the analog signal may further be set to be equal to the maximum charging voltage value of the capacitor in the liquid crystal display, or the difference between the maximum voltage value and the minimum voltage value that are of the analog signal may be set to be slightly greater than the maximum charging voltage value of the capacitor in the liquid crystal display. In this way, the fast charging duration determined according to the foregoing solution can meet charging/discharging requirements of all capacitors in the liquid crystal display, and the fast charging duration can be shortened as much as possible. Therefore, system power consumption is further reduced.

[0085] Based on a same inventive concept, an embodiment of this application further provides a display apparatus. As shown in FIG. 9, a display apparatus 900 includes a liquid crystal display 901 and the foregoing drive circuit 400.

[0086] The drive circuit 400 is configured to drive the liquid crystal display 901. For a specific operation of the drive circuit 400, refer to the foregoing descriptions. Details are not described herein again.

[0087] It is clear that a person skilled in the art can make various modifications and variations to embodiments of this application without departing from the scope of embodiments of this application. In this way, this application is intended to cover these modifications and variations provided that they fall within the scope of protection defined by the following claims and their equivalent

technologies.

Claims

1. A drive circuit, comprising:

   a digital-to-analog converter, configured to output an analog signal;
   an amplifier, configured to generate a drive signal based on the analog signal, wherein the amplifier comprises an amplification circuit and a current source circuit, the amplification circuit is configured to amplify the analog signal, and the current source circuit is configured to provide a bias current for the amplification circuit in a controllable manner; and
   a comparison control circuit, configured to compare a voltage value of the drive signal with a preset voltage value, and control, based on a comparative result, the current source circuit to output the bias current.

2. The drive circuit according to claim 1, wherein the comparison control circuit comprises:

   a comparator, configured to compare the voltage value of the drive signal with the preset voltage value; and
   a controller, configured to control, based on the comparative result of the comparator, the current source circuit to output the bias current.

3. The drive circuit according to claim 2, wherein the digital-to-analog converter is specifically configured to:

   output the analog signal at a first moment;
   the current source circuit is specifically configured to:

      provide a first bias current for the amplification circuit before the first moment, and provide a second bias current for the amplification circuit at the first moment, wherein a current value of the second bias current is greater than a current value of the first bias current; and
      the controller is specifically configured to: determine that a difference between a second moment at which the drive signal is inverted and the first moment is fast charging duration, and control, based on the fast charging duration, the current source circuit to output the bias current.

4. The drive circuit according to claim 3, wherein when controlling, based on the fast charging duration, the current source circuit to output the bias current, the controller is specifically configured to:
   each time a liquid crystal display coupled to the drive circuit refreshes data, control duration in which the current source circuit outputs the second bias current to be the fast charging duration.

5. The drive circuit according to any one of claims 1 to 4, wherein a difference between a maximum voltage value and a minimum voltage value that are of the analog signal is greater than or equal to a maximum charging voltage value of a capacitor in the liquid crystal display coupled to the drive circuit, and the preset voltage value is the maximum voltage value or the minimum voltage value of the analog signal.

6. The drive circuit according to any one of claims 3 to 5, wherein the analog signal is a first step signal, and a voltage value of the first step signal increases from a first voltage value to a second voltage value at the first moment; and the comparator is configured to compare the voltage value of the drive signal with the second voltage value, and a moment at which an output signal of the comparator is inverted from a low electrical level to a high electrical level is the second moment.

7. The drive circuit according to any one of claims 3 to 5, wherein the analog signal is a second step signal, and a voltage value of the second step signal decreases from a third voltage value to a fourth voltage value at the first moment. The comparator is configured to compare the voltage value of the drive signal with the fourth voltage value, and a moment at which an output signal of the comparator is inverted from a high electrical level to a low electrical level is the second moment.

8. The drive circuit according to any one of claims 3 to 7, wherein both the first moment and the second moment fall within a blanking region between a first frame of image and a second frame of image that are displayed by the liquid crystal display coupled to the drive circuit, and display time of the first frame of image is earlier than display time of the second frame of image.

9. The drive circuit according to claim 8, wherein the digital-to-analog converter is further configured to:

   perform digital-to-analog conversion on a digital control signal corresponding to the second frame of image, to obtain an analog control signal;
   the amplification circuit is further configured to:

      amplify the analog control signal; and
      the controller is further configured to: control

the current source circuit to output the second bias current at a third moment at which the amplification circuit receives the analog control signal, and control the current source circuit to output the first bias current at a fourth moment, wherein a time difference between the fourth moment and the third moment is the fast charging duration.

10. The drive circuit according to any one of claims 3 to 9, wherein the first moment is a moment at which the liquid crystal display refreshes data.

11. A display apparatus, comprising a liquid crystal display and the drive circuit according to any one of claims 1 to 10.

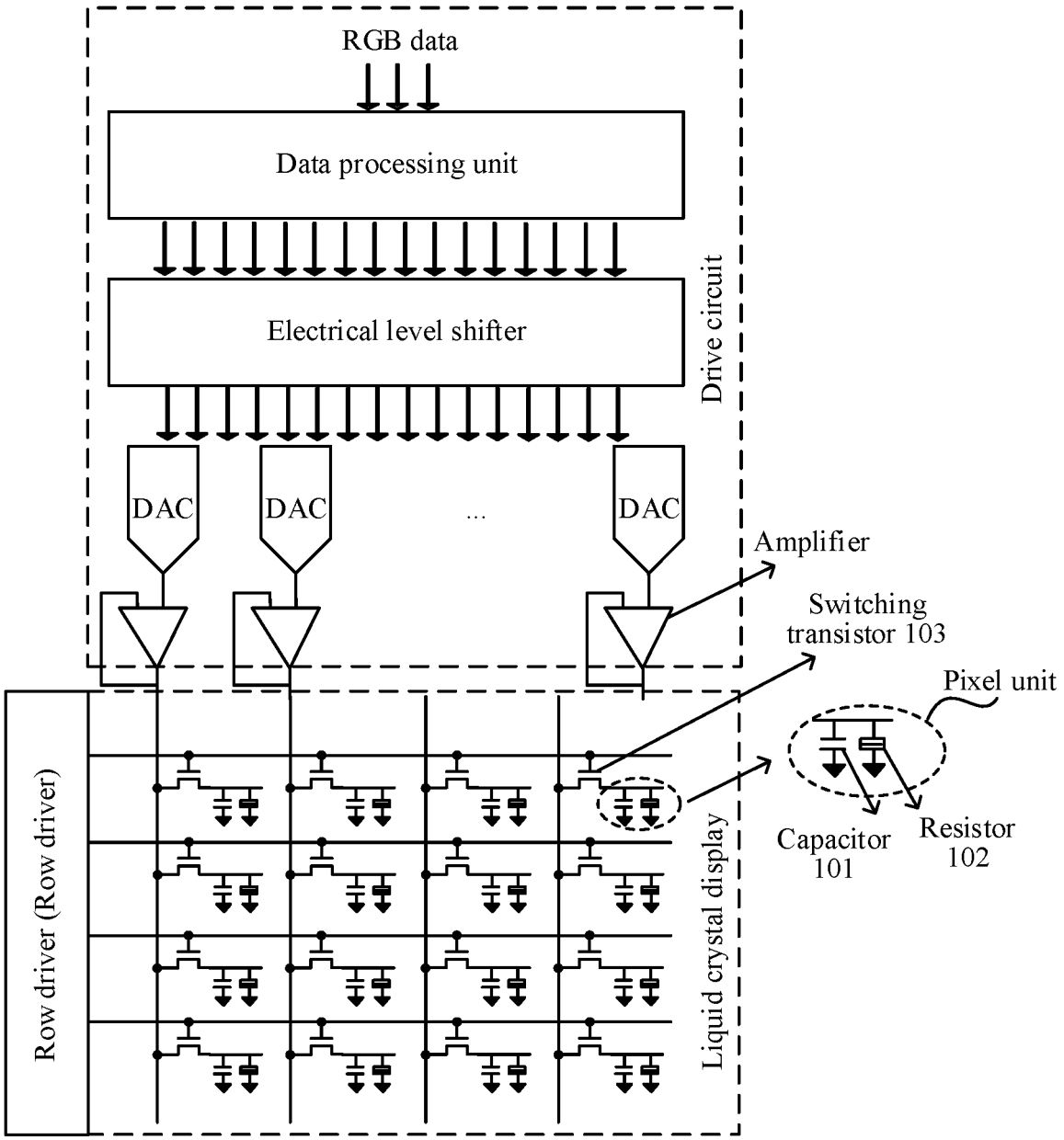

RGB data
Data processing unit
Electrical level shifter
Drive circuit
DAC
DAC
...
DAC
Amplifier
Switching transistor 103
Pixel unit
Capacitor 101
Resistor 102
Row driver (Row driver)
Liquid crystal display

FIG. 1

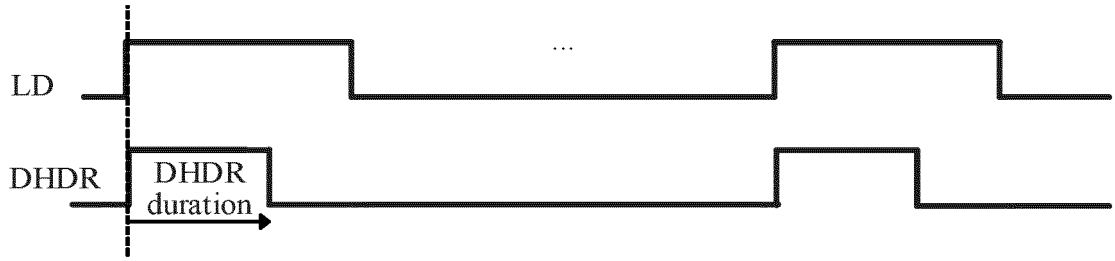
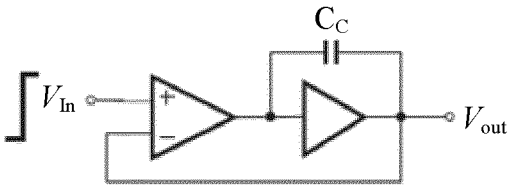
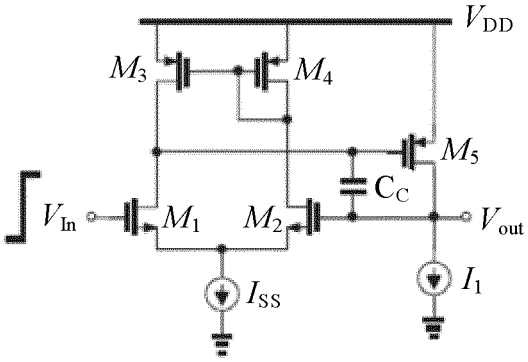

LD
...
DHDR
DHDR duration

FIG. 2



Example a



Example b

FIG. 3

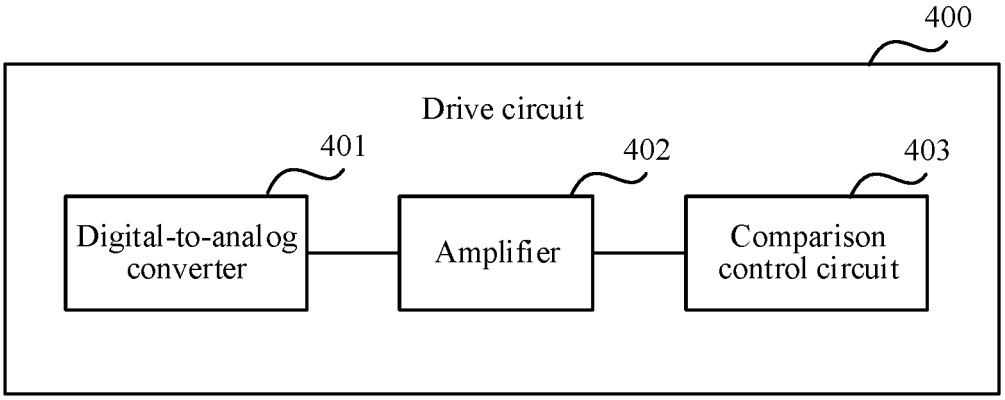


FIG. 4

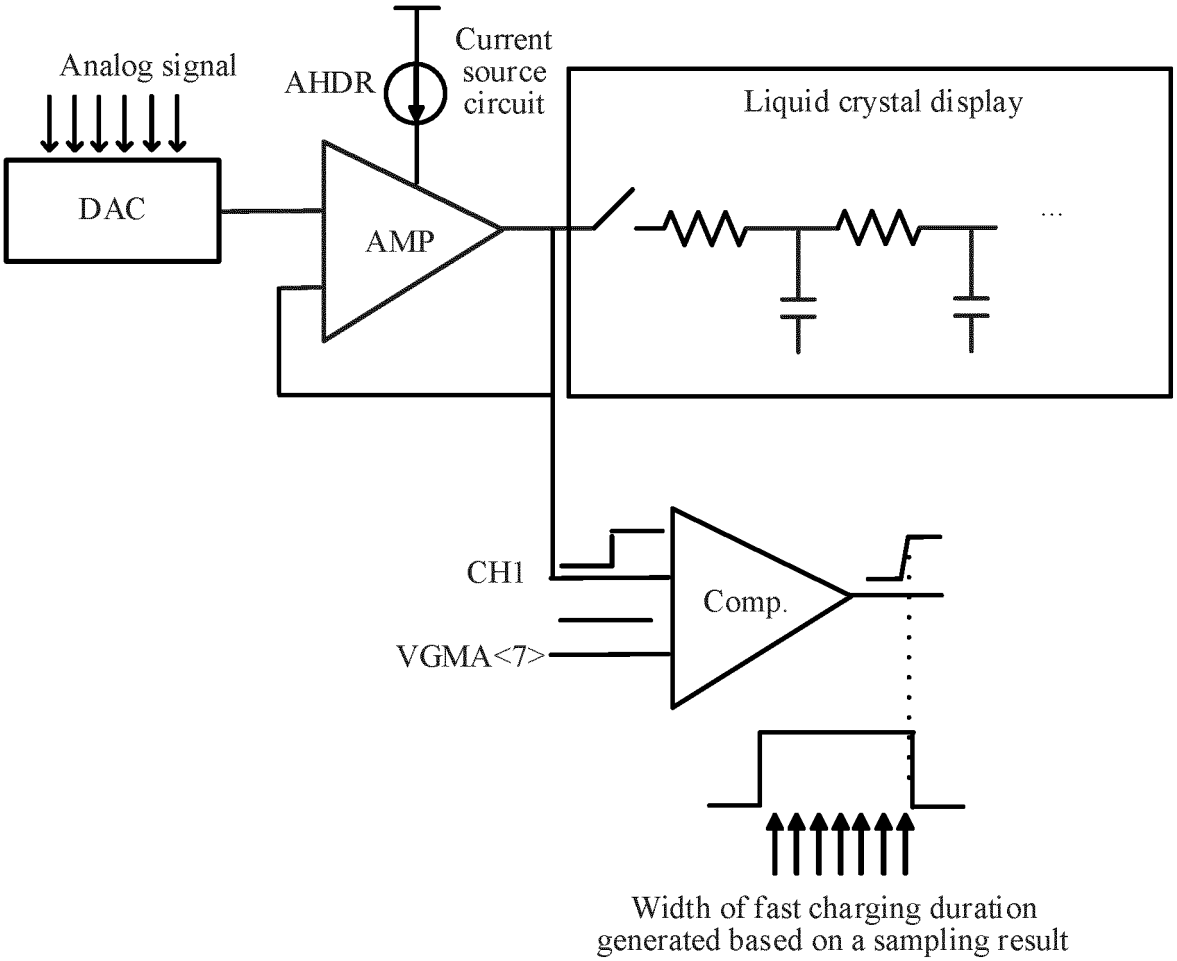

Analog signal
AHDR
Current source circuit
Liquid crystal display
DAC
AMP
...
CH1
Comp.
VGMA<7>
Width of fast charging duration generated based on a sampling result

FIG. 5

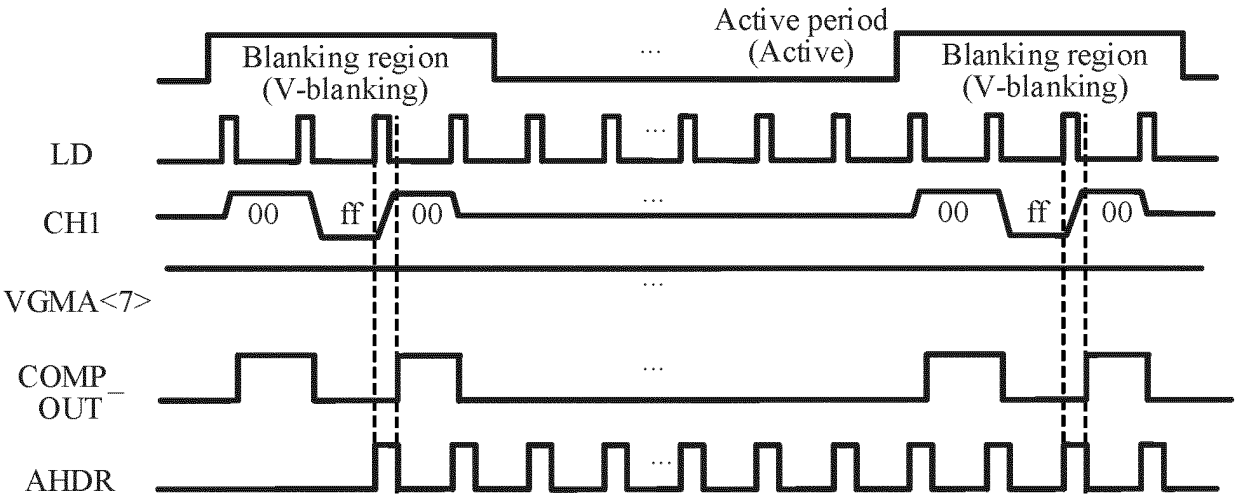

Blanking region
(V-blanking)
Active period
(Active)
Blanking region
(V-blanking)
LD
CH1
00
ff
00
00
ff
00
VGMA<7>
COMP_
OUT
AHDR

FIG. 6

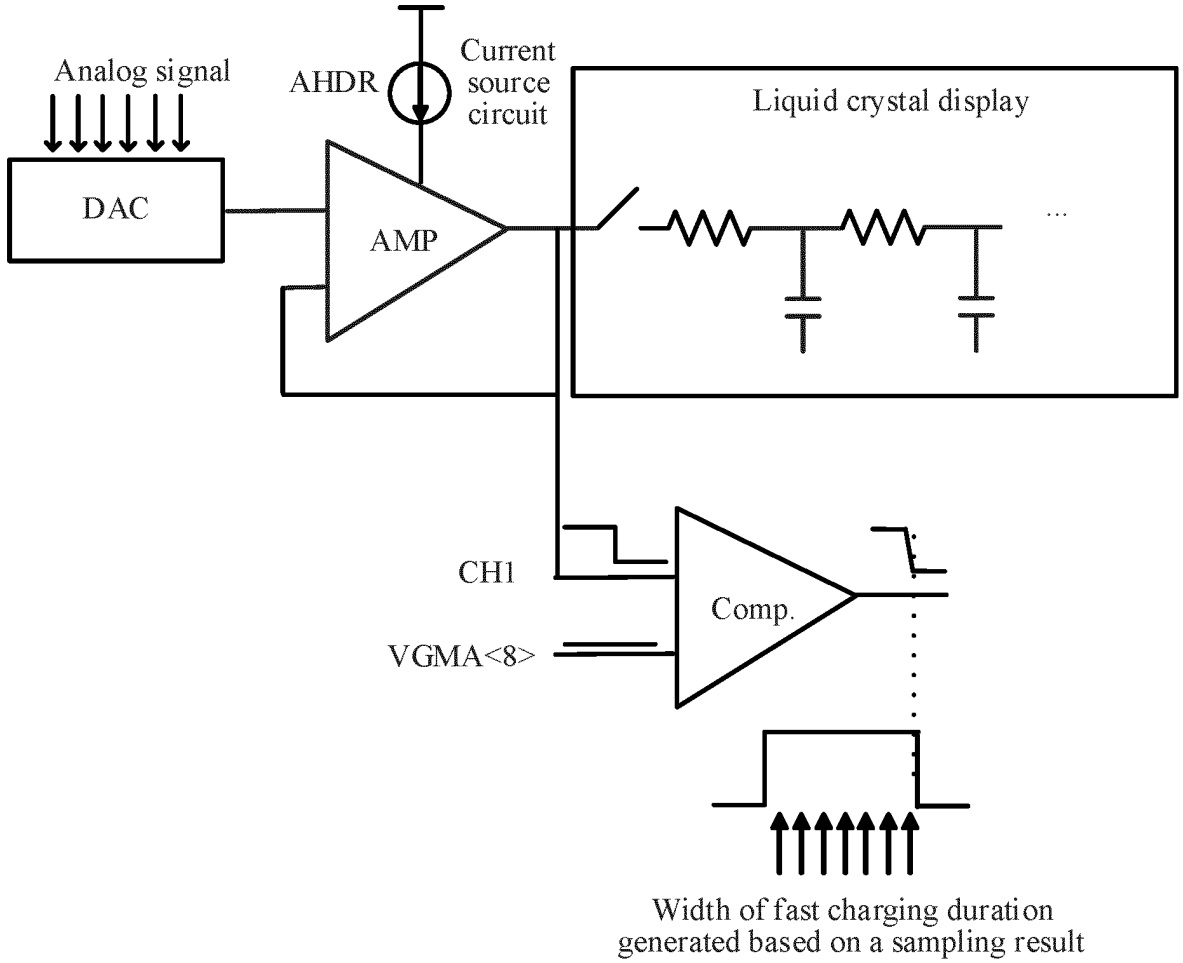

Analog signal
AHDR
Current
source
circuit
Liquid crystal display
DAC
AMP
CH1
Comp.
VGMA<8>
Width of fast charging duration
generated based on a sampling result

FIG. 7

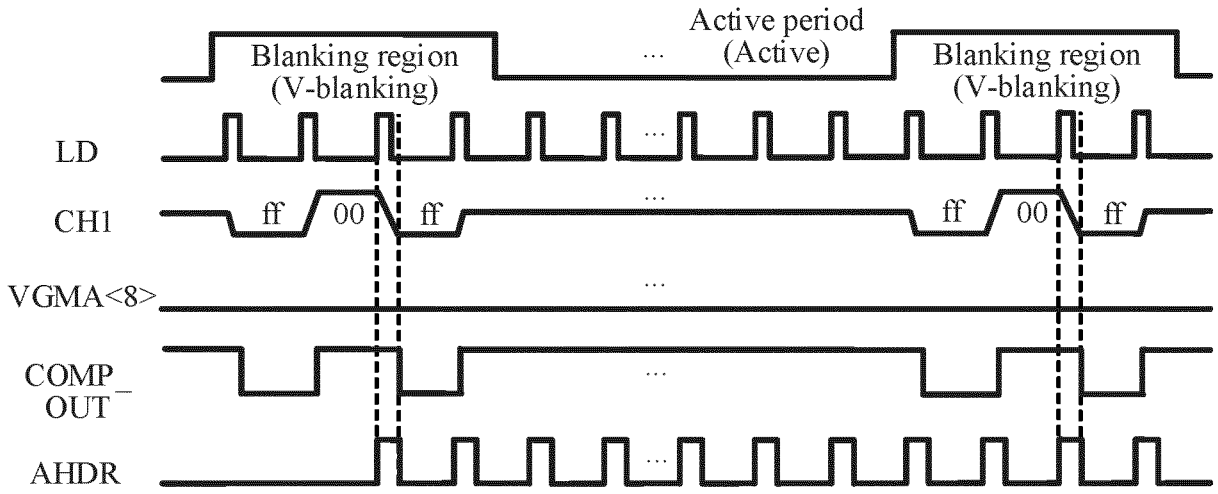

Active period
(Active)
Blanking region
(V-blanking)
Blanking region
(V-blanking)
LD
CH1
ff
00
ff
ff
00
ff
VGMA<8>
COMP_
OUT
AHDR

FIG. 8

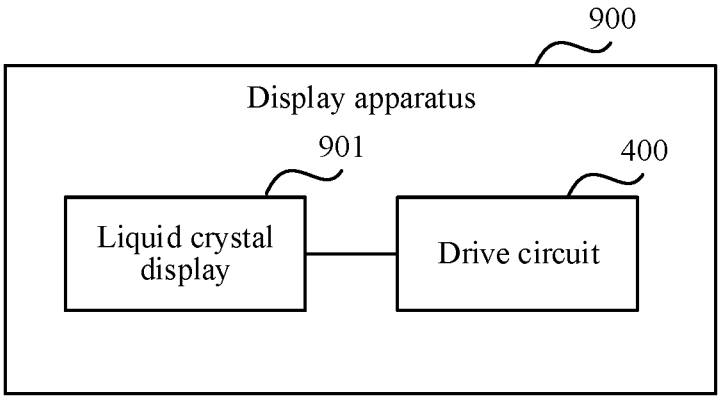

900
Display apparatus
901
400
Liquid crystal
display
Drive circuit

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2021/074237

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/36(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G; G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, VEN: 显示, 驱动, 源, 数据, 数模, DAC, 放大, 缓冲, 比较, 偏置, 电流, 电压display, drive, source, data, DAC, digital, analog, convert, amplify, buffer, compare, bias, current, voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018158408 A1 (SAMSUNG DISPLAY CO., LTD.) 07 June 2018 (2018-06-07) description, paragraphs [0002]-[0112], and figures 1-7	1-11
A	CN 109672834 A (SAMSUNG ELECTRONICS CO., LTD.) 23 April 2019 (2019-04-23) entire document	1-11
A	CN 109478891 A (SONY SEMICONDUCTOR SOLUTIONS CORP.) 15 March 2019 (2019-03-15) entire document	1-11
A	KR 20140109135 A (SAMSUNG ELECTRONICS CO., LTD.) 15 September 2014 (2014-09-15) entire document	1-11
A	WO 2007032285 A1 (SHARP K. K. et al.) 22 March 2007 (2007-03-22) entire document	1-11

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2021	**03 November 2021**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2021/074237

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2018158408 A1	07 June 2018	CN 108172177 A	15 June 2018
		US 10535301 B2	14 January 2020
		KR 20180066313 A	19 June 2018
CN 109672834 A	23 April 2019	US 2019116331 A1	18 April 2019
		US 10616518 B2	07 April 2020
		KR 20190042389 A	24 April 2019
CN 109478891 A	15 March 2019	EP 3493407 A1	07 August 2019
		US 2021185256 A1	17 June 2021
		EP 3493407 A4	07 August 2019
		WO 2018021055 A1	01 February 2018
KR 20140109135 A	15 September 2014	KR 102055841 B1	13 December 2019
		TW 201436464 A	16 September 2014
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		CN 104038206 A	10 September 2014
		TW I621334 B	11 April 2018
		US 9275595 B2	01 March 2016
WO 2007032285 A1	22 March 2007	CN 101263544 A	10 September 2008
		CN 101263544 B	02 November 2011
		US 2009109153 A1	30 April 2009
		US 8159442 B2	17 April 2012

Form PCT/ISA/210 (patent family annex) (January 2015)