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(71) Applicant: Sapien Semiconductors Inc.
Ulju-gun
Ulsan 44919 (KR)

(72) Inventors:

- LEE, Jae Hoon 46230 Busan (KR)
- JANG, Jin Woong 16679 Gyeonggi-do (KR)
- (74) Representative: Vossius & Partner Patentanwälte Rechtsanwälte mbB Siebertstrasse 3 81675 München (DE)

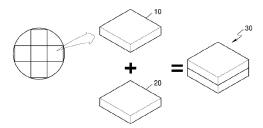
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(54) MICRO DISPLAY DEVICE, DATA DRIVING CIRCUIT, AND METHOD FOR INSPECTING SAME

A display device comprising a pixel unit including a plurality of pixels, each including a luminous element and a pixel circuit connected to the luminous element; a clock generator configured to generate a plurality of clock signals each corresponding to each of a plurality of subframes constituting a frame; and a parallel to serial converter configured to convert the plurality of clock signals to a serial clock signal and transfer the serial clock signal to the pixel unit; and wherein the pixel circuit of each pixel includes a first pixel circuit configured to control light-emission and non-emission of the luminous element in response to a control signal applied to each of the plurality of subframes; and a second pixel circuit configured to store bit values of image data in the frame and generate the control signal based on the stored bit values and the serial clock signal such that each subframe included in the frame is controlled according to each bit value.

FIG. 1



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CROSS-REFERENCE TO RELATED APPLICATIONS

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[0001] This application is a 371 National Stage of International Application No. PCT/KR2020/009942, filed July 28, 2020, which claims priority to Korean Patent Application No. 10-2019-0127865, filed October 15, 2019, the disclosures of which are herein incorporated by reference in their entirety.

FIELD OF THE INVENTION

[0002] Aspect(s) of the present invention relates to a data drive circuit and a display device including the data drive circuit. In addition, aspects of the present disclosure related to a micro-display device and its checking method thereof. In addition, aspect(s) of the present invention related to a device having a Memory Inside Pixel (MIP) display.

BACKGROUND OF THE INVENTION

[0003] As an information society develops, the demand for display devices to display images is increasing, and various types of display devices such as liquid crystal display devices, plasma display devices, organic light illumination display devices, etc. are being utilized. In recent years, interest in display devices using micro light emitting diodes (μ LED) (hereinafter referred to as "microdisplays") has also increased.

[0004] With the need for excellent display characteristics for Virtual Reality (VR), Augmented Reality (AR), and Mixed Reality (MR) technologies, the development of micro LED on Silicon or AMOLED on Silicon is increasing, especially for high-resolution implementations, and the demand for minimizing pixel sizes is increasing.

[0005] In addition, with the rapid growth of the AR and MR markets in recent years, the growth of the microdisplay (or micro display) market with Cu-Cu bonding and micro-LEDs is expected due to its low power consumption characteristics and excellent luminance characteristics.

[0006] For pulse width modulation PWM drive of pixel circuits with built-in memory, a large number of wirings are required in the display activation area because a connection is required to the pixel circuit for a large number of gray scale representation signals. Therefore, in order to test the defective bonding conventionally, in particular, a large display panel with a separate pixel drive circuit (IC) and scan/data driver drive circuit (Scan / Data Driver IC) requires a number of input PADs in the pixel drive circuit

[0007] As such, when a number of micro light emitting devices (LEDs) are joined and attached to one display device as the display resolution increases, it is necessary to take measures against this because a defective bonding inevitably occurs. In order to determine existence of

a pixel containing a defective bonding of a micro light emitting device, information about the pixel containing the defective bonding is required.

[0008] Conventionally, there is a method of placing daisy chains in the micro-display adjacent area and indirectly checking the joining characteristics, but there is a disadvantage that it is impossible to determine the exact bad bonding position. In addition, the Mobile Industry Processor Interface (MIPI) is a Preferred Display Standard for Portable Electronic Devices, Supporting Two Display Standards: Video Mode and Command Mode.

[0009] In addition, the mobile industry processor interface (MIPI[®]) is a recent display standard for portable electronic devices, supporting two display standards: video mode and command mode.

[0010] In video mode, frame data is transmitted from the host to the display driver IC in real time. In the video mode, even if the image to be transmitted to the display driver IC is a still image, the host continues to transmit the same still image to the display driver IC. Thus, the power consumption of the host increases.

[0011] In a command mode, a start of the transmission of frame data is controlled by a tearing effect TE signal. When displaying a still image on the display, the display driving integrated circuit (IC) may periodically read the still image stored in the frame buffer embedded in the display driving IC and transmit the read still image to the display. This operation is called a panel self-refresh. However, the command mode may have the disadvantage that the size and price of IC development are affected because there must be additional frame memory.

[0012] On the other hand, the conventional display, as described above, must be continuously refreshed to maintain the output of the still image, while the memory inside pixel (MIP) display has memory in each pixel, so that the image can be displayed once and then displayed without a screen refresh.

[0013] When driving video mode in a MIP environment, the host may continue to transmit data to the display driving IC, which adds to the burden on the host and increases the host's power consumption. In addition, when driving in the command mode in the MIP environment, the transmission amount cannot be predicted, so there may be a disadvantage that additional memory is required to implement it.

DETAILED DESCRIPTIONS OF THE EMBODIMENT

TECHNICAL PROBLEMS TO BE SOLVED

[0014] Aspect(s) of the present invention is to provide a data driver and a display device including the data driving circuit, which accurately implement gamma characteristics even in process changes by implementing a gamma circuit matched with a pixel circuit.

[0015] In addition, Aspect(s) the present invention is provided to the above-described necessity, for the purpose of providing a micro LED display and a method of

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checking thereof to determine whether the pixel is defective for the result of performing the bonding of the micro LED display device substrate and the CMOS driver substrate.

[0016] In addition, aspect(s) of the present invention provides an electronic device and the method thereof for improving power consumption in a memory inside pixel (MIP) display.

[0017] However, this problem is exemplary, and the scope of the present invention is not limited thereto.

[0018] A data driver according to one embodiment of the present invention may include a reference current generation circuit that generates a reference current corresponding to a predetermined brightness; a gamma current generator including a plurality of transistors of different sizes operated by the reference current and a current mirror, configured to convert the reference current into a first to M gamma current and output; a reference gamma voltage generation circuit configured to convert the first to the first M gamma current into the first to the Mth reference gamma voltages;

a gamma voltage generation circuit configured to convert the first to the Mth reference gamma voltages into a first to a Mth gamma voltages; and a divider configured to generate the first to M gamma voltages by dividing the first to N gamma buffer voltage

[0019] The gamma current generation circuit may include the first to the Mth transistors outputting the first to the Mth gamma currents, respectively. Each of the first to the Mth transistors may be composed of one or more transistors of the same or different sizes connected in series and/or parallel.

[0020] The reference gamma voltage generation circuit may include the first to the Mth transistors, and the first to the Mth transistors may have the same size as the drive transistors of the pixels. Each gate voltage of each of the first to the Mth transistors may be the first to the Mth reference gamma voltages, respectively.

[0021] A micro display device according to an embodiment of the present invention may include: a plurality of pixels arranged in a display area; and a power supply provided around the display area and outputting a power voltage to a power line connected to the plurality of pixels; wherein each of the plurality of pixels includes a first electrode and a second electrode, at least one light emitting device having a first electrode connected to the power line; and an AND gate connected to an input terminal of the second electrode of the at least one light emitting device, an input terminal of a first AND gate included in a first pixel among the plurality of pixels receives a node voltage and a test pulse signal applied to a second electrode of at least one emitting device included in the first pixel; an output terminal of the first AND gate outputs an operation result obtained by performing an AND operation based on the node voltage and the test pulse signal,

the operation result may be transmitted by being connected to an input terminal of a second AND gate included in a second pixel arranged adjacent to the same row as the first pixel among the plurality of pixels.

[0022] In addition, the micro display device may include: a measuring unit for measuring current to test whether bonding is defective; a first switch for connecting the plurality of pixels arranged in the display area in a row unit; and a second switch for sequentially connecting the plurality of pixels arranged in the display area in units of columns, wherein the measurement unit may measure a current corresponding to an AND gate operation result by sequentially connecting a plurality of pixels included in a row to which the first switch is connected through the second switch.

[0023] In addition, the display area is separated into a predetermined number of sub-regions of the column nit, the second switch is provided for each of the sub-regions, and the first switch may be connected sequentially to each of the sub-regions for a plurality of pixels contained in the connected row.

[0024] In addition, the micro-display may include: a checking unit configured to test for defects in the pixel circuit; and a third switch; connected to the checking unit, the first switch includes a first pole and a second pole, the first pole is connected to the second electrode of the plurality of light emitting devices, the second switch connects the measuring unit and the second pole of the first switch, the third switch configured to connect the second pole of the first switch with the checking unit, the measuring unit may test whether the bonding is defective based on the current flowing through the first switch and the second switch by turning on the first switch and the second switch in the first checking mode; and the checking unit may test the defect of the pixel circuit based on the current flowing through the first switch and the third switch by turning on the first switch and the third switch in the second checking mode.

[0025] The electronic device according to an embodiment of the present invention may include: a controller configured to receive a first video data including at least one or more bit values, generate clock signals having different assigned periods corresponding to each of the at least one or more bit values in the order of least significant bit (LSB) to most significant bit (MSB), and determine control data by reading each of the at least one or more bit values from a first memory in response to each of the generated clock signals; a first memory configured to store at least one bit value of the first video data; and a circuit including a pixel circuit configured to control light emission of a pixel (PX) based on the control data.

[0026] Other aspects, features and advantages other than those described above will become apparent from the following detailed description, claims and drawings for carrying out the invention.

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[0027] According to one embodiment of the present invention, a data driving circuit and a display device, which includes the data driving circuit may provide accu-

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which includes the data driving circuit may provide accurately gamma characteristics even in process changes by implementing gamma circuits matched with pixel circuits

[0028] According to an embodiment of the present invention, it is possible to easily detect the defective bonding of micro-LEDs, thereby improving other productivity. In addition, it may be possible to determine the exact defect bonding position when performing repair operation, thereby improving yield.

[0029] In addition, according to an embodiment of the present invention, by adjusting a position of the most significant bit (MSB) and the least significant bit (LSB) of the bit string in the data displayed by pulse width module (PWM) drive, and adding a separate storage device for the MSB to which a relatively long time is assigned to the bit string reading, thereby it is possible to reduce the power consumption at a system level of the device.

[0030] In addition, according to an embodiment of the present invention, in the mobile industry processor interface (MIPI) command mode (MIPI) where the writing rate is fast in memory, a memory inside pixel (MIP) may avoid problems that can be caused by differences between bit string reading time and data writing time stored in memory in memory circuitry (e.g., screen tearing).

[0031] It will be appreciated by persons skilled in the art that that the effects that could be achieved with the present invention are not limited to what has been particularly described hereinabove and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The above and other aspects, features, and advantages of certain embodiments of the disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic view shows the manufacturing process of the display device according to some embodiments.

FIG. 2 is a view schematic view shows a display device according to some embodiments.

FIGS. 3 and 4 are examples of pixels of display devices shown in FIG. 2.

FIG. 5 is a schematic view shows a data driver according to some embodiments.

FIG. 6 is a schematic view shows a gamma voltage generator according to some embodiments.

FIG. 7 is a schematic view shows the gamma voltage generator according to some embodiments.

FIGS. 8 and 9 are shows a schematic view of the

gamma voltage generator according to some embodiments.

FIG. 10 is a schematic view shows a display device according to some embodiments.

FIG. 11 is a block degree for explaining how to check whether a row (line) unit defect according to some embodiments.

FIG. 12 is a drawing for describing a gate chain of the pixel unit according to some embodiments.

FIG. 13a and FIG. 13b is figures for describing the structure of the gate of the pixel circuit according to some embodiments.

FIG. 14 shows a voltage-current graph in a common anode type to illustrate the operation of the gate of the pixel circuit according to some embodiments.

FIG. 15 is a schematic view showing a display device 30B inspecting a defective pixel based on the current according to some embodiments.

FIG. 16 is a diagram describing a configuration for driving the checking mode according to some embodiments.

FIG. 17 is an example of a pixel of a display device 30B according to some embodiments.

FIG. 18 is a timing degree for explaining the timing in the first checking mode according to some embodiments.

FIG. 19 is an example of an electronic device according to some embodiments.

FIG. 20 is another example of an electronic device according to some embodiments.

FIG. 21 illustrates a schematic for driving a current supply, pixel (PX) of an electronic device according to some embodiments.

FIG. 22 is an example showing the driving timing of a general clock signal according to some embodiments

FIG. 23 is another example showing the driving timing of a general clock signal according to some embodiments.

FIG. 24 is an example of a display operation in a mobile industry processor interface (MPIP) video mode (video mode) and a command mode according to clock signal drive according to some embodiments.

FIG. 25 is an example of an operation according to the clock signal drive timing change according to some embodiments.

FIG. 26 is an example of an electronic device including additional memory in a memory inside pixel (MIP) circuit according to some embodiments.

Best Mode for Carrying out the Invention

[0033] The electronic device according to an embodiment of the present invention may include: a controller configured to receive a first video data including at least one or more bit values, generate clock signals having different assigned periods corresponding to each of the

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at least one or more bit values in the order of least significant bit (LSB) to most significant bit (MSB), and determine control data by reading each of the at least one or more bit values from a first memory in response to each of the generated clock signals; a first memory configured to store at least one bit value of the first video data; and a circuit including a pixel circuit configured to control light emission of a pixel (PX) based on the control data

Modes for carrying out the invention

[0034] Since the present invention can apply various transformations and can have various embodiments, specific embodiments are illustrated in the drawings and described in detail in the detailed description. Effects and features of the present invention, and a method of achieving them, will become apparent with reference to the embodiments described below in detail in conjunction with the drawings. However, the present invention is not limited to the embodiments disclosed below and may be implemented in various forms.

[0035] Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings, and when described with reference to the drawings, the same or corresponding components are given the same reference numerals, and the overlapping description thereof will be omitted.

[0036] In the following description, terms such as first, second, and the like are used for the purpose of distinguishing one component from another, not in a limiting sense. Also, in the following description, the singular expression may include the plural expression unless the context clearly dictates otherwise.

[0037] In the following description, when X and Y are connected, X and Y are electrically connected, X and Y are functionally connected, and X and Y are directly connected. have. Here, X and Y may be objects (eg, devices, elements, circuits, wirings, electrodes, terminals, conductive films, layers, etc.). Therefore, it is not limited to a predetermined connection relationship, for example, the connection relationship shown in the drawings or detailed description, and may include other than the connection relationship shown in the drawings or detailed description.

[0038] When X and Y are electrically connected, for example, an element (for example, a switch, a transistor, a capacitor, an inductor, a resistance element, a diode, etc.) that enables the electric connection of X and Y, it may include a case where one or more connections are made between X and Y.

[0039] When X and Y are functionally connected, a circuit that enables the functional connection of X and Y (for example, a logic circuit (OR gate, inverter, etc.), signal conversion circuits (AD conversion circuits, gamma correction circuits, etc.), potential level conversion circuits (level shifter circuits, etc.), current supply circuits, amplifier circuits (circuits that can increase signal ampli-

tude or current amount, etc.), signal generation circuits, a case in which one or more memory circuits (memory, etc.) are connected between X and Y may be included. **[0040]** In the following description, "ON" used in connection with a device state may refer to an activated state of a device, and "OFF" may refer to an inactive state of a device. As used in connection with a signal received by a device, "on" may refer to a signal that activates a device, and "off" refers to a signal that deactivates a device. The device can be activated by a high voltage or a low voltage. For example, a P-type transistor is activated by a low voltage, and an N-type transistor is activated by a high voltage. Accordingly, it should be understood that the "on" voltages for a P-type and N-type transistor are opposite (low vs. high) voltage levels.

[0041] A term that refers to a variable (e.g., a parameter) related to the display of data used in the following description, and an object (e.g., an electronic device, a display device, a display device, etc.) used to perform the operation of the invention. Terms referring to components of the device (e.g., circuit, pixel circuit, pixel, driving circuit, controller, processor, controller, etc.) are exemplified for convenience of description. Accordingly, the present disclosure is not limited to the terms described below, and other terms having equivalent technical meanings may be used. In the following description, terms such as include or have means that a feature or element described in the specification is present, and the possibility that one or more other features or elements may be added is not excluded in advance.

[0042] FIG. 1 is a schematic view showing the manufacturing process of the display device according to some embodiments.

[0043] Referring to FIG. 1, the display device 30 may include a light emitting device array 10 and a drive circuit board 20. The light emitting device array 10 may be combined with the drive circuit substrate 20. The display device 30 may be a micro display device.

[0044] The light emitting device array 10 may include a plurality of light emitting devices. The emitting device may be a light emitting diode (LED). The light emitting device may be a light emitting diode (LED) of a micro to a nano-unit size. At least one light emitting device array 10 may be prepared by growing a plurality of light emitting diodes on the semiconductor wafer (SW). Thus, the display device 30 may be prepared by combining the light emitting device array 10 with the drive circuit substrate 20 without having to transfer the light emitting diode individually to the drive circuit substrate 20.

[0045] The driving circuit board 20 may be a Si-CMOS substrate in which pixel circuits corresponding to each of the light emitting diodes on the light emitting device array 10 and independently controlling the light emitting diodes are arranged. A pixel circuit may include at least one transistor and at least one capacitor.

[0046] Micro LEDs may require a high processing temperature of 1000 °C or more and cannot be directly grown and patterned on top of the transistor of the drive circuit

board 20. A pixel may be formed by connecting light emitting device array 10 and the pixel circuit of the drive circuit substrate 20 electrically by combining after respectively forming a pixel circuit array on the light emitting device array 10 and the drive circuit substrate 20 according to an embodiment of the present invention. At this time, the exact arrangement of the pixel circuit array and the light emitting diode array is important.

[0047] The pixel circuit on the light emitting diode and the drive circuit board 20 on the light emitting device array 10 may be electrically connected to configure the pixel (PX). FIG. 2 is a view that outlines the display device according to some embodiments. Referring to FIG. 2, the display device 30 may include a pixel unit 110 and a driver 120.

[0048] The pixel unit 110 may display the image using a m-bit digital image signal that can display a one to 2^m gradation levels. The pixel unit 110 may be placed in the display area displaying the image. The pixel unit 110 may include a predetermined pattern, for example, a matrix type, a plurality of pixels PX arranged in various patterns such as zigzag type. Pixels PX may emit one color, for example, emit the color of one of red, blue, green, or white. Pixels (PX) may emit other colors other than red, blue, green, and white.

[0049] Pixels (PX) may include light emitting devices. The light emitting device may be a self-illuminating device. For example, the light emitting device may be an inorganic light emitting diode (LED). The light emitting device may be a micro light emitting diode (LED). The light emitting device may emit a single peak wavelength or a plurality of peak wavelengths.

[0050] Pixel (PX) may further include a pixel circuit connected to a light emitting device. The pixel circuit may include at least one transistor and at least one capacitor. Transistors may be CMOS transistors.

[0051] The pixel unit 110 may include scan lines SL1 -SLi applying the scan signal to the pixel PX and a data line DL1-DLj applying the data signal to the pixels PX. The pixel unit 110 may further include a light emitting control line applying a light emitting control signal (see EM, FIG. 4) to the pixel PX.

[0052] Scan lines SL1-SLi are connected to pixels PX arranged in the same row, and the data lines DL1-DLj each may be connected to the pixels PX arranged in the same column. Light emitting control lines may be connected to pixels PX arranged in the same row.

[0053] The driver 120 is provided in the undisplay area around the pixel unit 110, and the pixel unit 110 may be driven and controlled. The driver 120 may include a controller 121, a scan driver 122, a data driver 123 and a power supply 124.

[0054] Under the control of the controller 121, the scan driver 122 may sequentially apply a scan signal to the scan lines SL1-SLi, and the data driver 123 may apply the data signal to each pixel PX. According to the control of the controller 121, the scan driver 122 may sequentially apply the light emitting control signal to the light emitting

control lines. The pixels PX may emit light with a brightness corresponding to the voltage level or current level of the data signal received through the data lines DL1-DLj in response to the scan signal received through the scan lines SL1-SLi.

[0055] The power supply 124 may receive an external power source and/or an internal power supply apply and converts it to a voltage of various levels necessary for the operation of each component, and the voltage may be supplied to the pixel unit 110 according to the power control signal input from the controller 121.

[0056] The power supply 124 may apply the first power voltage (VDD) to the pixel unit 110. The power supply 124 may generate a drive voltage and apply it to the scan driver 122 and the data driver 123.

[0057] The controller 121, the scan driver 122, the data driver 123, and the power supply 124 are each formed in the form of a separate integrated circuit chip or one integrated circuit chip and are mounted directly on the substrate where the pixel unit 110 is formed. Or The controller 121, the scan driver 122, the data driver 123, and the power supply 124 may be mounted on a flexible printed circuit film or attached to a substrate in the form of a tape carrier package (TCP).

[0058] FIG. 3 and FIG. 4 are examples of the pixel of the display device shown in FIG. 2.

[0059] Referring to FIG. 3, the pixel PX1 may be connected to a scan line SL, a data line DL, and a power line. [0060] The scan line may transmit a scan signal. The data line intersecting with the scan line may transmit a data signal. The power line may transmit the first power voltage (VDD).

[0061] The pixel (PX1) may include the light emitting diode (LED) and a pixel circuit connected to the light emitting diode (LED). The pixel circuit may include the first transistor T1 and the second transistors T2, and capacitors C.

[0062] The first transistor T1 may include a gate electrode connected to the first electrode of the capacitor C, a first electrode connected to the light emitting diode LED, and a second electrode connected to the second power voltage VSS. The second power voltage VSS may be a ground voltage GND. The first transistor T1 may serve as a driving transistor, and may receive a data signal according to a switching operation of the second transistor T2 to supply current to the light emitting diode LED. [0063] The second transistor T2 may include a gate electrode connected to the scan line SL, a first electrode connected to the data line DL, and a second electrode connected to the gate electrode of the first transistor T1. The second transistor T2 may be turned on according to the scan signal SCAN transmitted through the scan line SL, transmit the data signal DATA transmitted through the data line DL to the gate of the first transistor T1, and act as a switching transistor.

[0064] The capacitor C may include a first electrode connected to the gate electrode of the first transistor T1, and a second electrode connected to the second power

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voltage VSS.

[0065] The first electrode of the light emitting diode LED may receive the first power voltage VDD from the power line. The second electrode of the light emitting diode LED may be connected to the first electrode of the first transistor T1. The light emitting diode LED may display an image by emitting light with a luminance corresponding to the data signal.

[0066] Referring to FIG. 4, a pixel PX2 may include a third transistor T3 between the first transistor T1 and the light emitting diode LED in the pixel PX1 shown in FIG. 3. [0067] The third transistor T3 may include a gate electrode connected to the light emitting control line, a first electrode connected to the second electrode of the light emitting diode LED, and a second electrode connected to the first electrode of the first transistor T1.

[0068] The third transistor T3 may be turned on according to a light emitting control signal EM received through the light emitting control line to allow the driving current of the first transistor T1 to flow through the light emitting diode LED. In FIG. 2, the light emitting control line is connected to the scan driver 122. The light emitting control line may receive the light emitting control signal EM from the scan driver 122.

[0069] The light emitting control line may be connected to a light emitting control driver (not shown) separate from the scan driver 122 to receive the light emitting control signal EM according to an embodiment.

[0070] FIG. 5 is a schematic diagram illustrating a data driver according to some exemplary embodiments.

[0071] Referring to FIG. 5, the data driver 123 may include a gamma voltage generator 1231, a decoder 1233, and a buffer 1235.

[0072] The gamma voltage generator 1231 may generate a plurality of gamma voltages V<0> to V<N-1> (N is a natural number). According to an embodiment, the gamma voltage generator 1231 may generate an arbitrary number of gamma voltages. For example, the gamma voltage generator 1231 may generate gamma voltages V<0> to V<255> having 256 gray levels. In another embodiment, the gamma voltage generator 1231 may generate gamma voltages V<0> to V<1023> having 1024 grayscale levels.

[0073] The decoder 1233 may receive input data I_DATA from the controller 121 and gamma voltages V<0> to V<N-1> from the gamma voltage generator 1231. The decoder 1233 may select one of the plurality of gamma voltages V<0> to V<N-1> based on the input data I_DATA and output it as the input voltage VIN. The decoder 1233 may be configured for each channel corresponding to each of the data lines DL1 to DLj. The buffer 1235 may generate a data signal DATA corresponding to the input voltage VIN and output the data signal DATA to the data lines DL1 to DLj. The buffer 1235 may be configured for each channel corresponding to each of the data lines DL1 to DLj. The buffer 1235 may output the data signal DATA to a corresponding data line among the plurality of data lines DL1 to DLj.

[0074] FIG. 6 shows a schematic diagram illustrating a gamma voltage generator according to some exemplary embodiments.

[0075] Referring to FIG. 6, the gamma voltage generator 1231 may include a reference current generator circuit 141, a gamma current generator circuit 143, a reference gamma voltage generator circuit 145, and a gamma voltage generator circuit 147, and a divider 149 according to an embodiment of the present invention.

[0076] The reference current generation circuit 141 may generate a reference current lref. The reference current generation circuit 141 may generate a reference current lref corresponding to the brightness set in the display device.

[0077] The gamma current generating circuit 143 may generate first to Mth gamma currents lgamma_1 to lgamma_M (M is a natural number, M≤N) based on the reference current lref. For example, M may be 13 and N may be 256. The first to Mth gamma currents lgamma_1 to lgamma_M may be currents corresponding to M gamma voltages among the gamma voltages V<0> to V<N-1>, respectively.

[0078] The reference gamma voltage generation circuit 145 may output the first to Mth reference gamma voltages VGMA_1 to VGMA_M corresponding to the first to Mth gamma currents lgamma_1 to lgamma_M output from the gamma current generation circuit 143.

[0079] The gamma voltage generating circuit 147 may buffer the first to Mth reference gamma voltages VGMA_1 to VGMA_M to output the first to Mth gamma buffer voltages VG_1 to VG_M. The gamma voltage generation circuit 147 may include a plurality of voltage followers for providing a stabilized voltage.

[0080] The divider 149 may be formed of a resistor string. The divider 149 may generate and output the first to the Nth gamma voltages V<0>,..., V<N-1>) by dividing the voltages between the first to Mth gamma buffer voltages VG_1 to VG_M output from the gamma voltage generating circuit 147. For example, when outputting 256 gamma voltages, the divider 149 may generate a first gamma voltage V<0> to a 255th gamma voltage V<255>.

[0081] FIG. 7 is a schematic diagram illustrating a gamma voltage generator according to some exemplary embodiments.

[0082] Referring to FIG. 7, the gamma voltage generator 1231A may include a reference current generator circuit 141A, a gamma current generator circuit 143A, a reference gamma voltage generator circuit 145A, a gamma voltage generator circuit 147A, and a divider 149A.
[0083] The reference current generation circuit 141A

may include a first transistor 21, a second transistor 22, an operational amplifier 23, and a resistor 24. The first transistor 21 may include a gate connected to the first control line 151, a first terminal connected to a source of the first power voltage VDD, and a second terminal connected to a gate and a first terminal of the second transistor 22

[0084] The second transistor 22 has a gate connected

to the output terminal of the operational amplifier 23, a first terminal connected to a second terminal of the first transistor 21, and a second terminal connected to the second terminal (-) of the operational amplifier 23.

[0085] The first input terminal (+) of the operational amplifier 23 is connected to a source of the reference voltage Vref, and the second input terminal (-) is connected to the resistor 24. The output terminal of the operational amplifier 23 is connected to a gate of the second transistor 22. When the reference voltage Vref is applied to the first input terminal (+), the second transistor 22 may be turned on or off according to a voltage of the output terminal due to a voltage difference between the second input terminal (-) and the output terminal. The reference voltage Vref may have a value corresponding to a predetermined brightness (luminance).

[0086] In the operational amplifier 23 may determine the output terminal voltage is determined according to the reference voltage Vref and the resistance value of the resistor 24, and determine may determine the reference current Iref flowing through the first transistor 21 and the second transistor 22 turned on from the first power voltage VDD.

[0087] The reference current generation circuit 141A may supply the reference current lref to the gamma current generation circuit 143A by forming a current mirror with the gamma current generation circuit 143A.

[0088] Although the above-described embodiment shows an example in which the reference current generation circuit 141A includes the first transistor 21 implemented as a P-type transistor and the second transistor 22 implemented as an N-type transistor, an embodiment of the present invention is not limited an example thereto, and the reference current generation circuit 141A may be configured by implementing the first transistor 21 and the second transistor 22 as different types of transistors, and configuring an operational amplifier corresponding thereto.

[0089] The gamma current generation circuit 143A may generate the first to the Mth gamma currents Igamma_1 to Igamma_M based on the reference current Iref. The gamma current generation circuit 143A may include the first to the Mth transistors 41_1 to 41_M. The first to the Mth transistors 41_1 to 41_M may be implemented as P-type transistors.

[0090] Each of the first to the Mth transistors 41_1 to 41_M may include a gate connected to the first control line 151, a first terminal connected to a source of the first power voltage VDD, and a second terminal connected to a reference gamma voltage generating circuit 145A. The first to the Mth transistors 41_1 to 41_M may have different sizes. Here, the size may be a channel length (W/L) for a channel width.

[0091] The first to the Mth transistors 41_1 to 41_M have a size that can create the first to the Mth gamma currents Igamma_1 to Igamma_M corresponding to M gamma voltages among the gamma voltages V<0> to V<N-1>, respectively.

[0092] As shown in FIG. 7, each of the first to the Mth transistors 41_1 to 41_M is illustrated as one transistor. In another example, each of the first to the Mth transistors 41_1 to 41_M may be implemented as one or more transistors under the condition that a predetermined transistor size is satisfied.

[0093] The first to the Mth transistors 41_1 to 41_M may constitute the reference current generation circuit 141A and the current mirror circuit, respectively. Accordingly, based on the reference current lref formed in the reference current generation circuit 141A while the first transistor 21 of the reference current generation circuit 141A is turned on, the first to the Mth transistors 41_1 to 41_M are the first to the Mth gamma currents lgamma_1 to lgamma M may be generated, respectively.

[0094] The reference gamma voltage generation circuit 145A is configured to generate the first to the Mth reference gamma voltages VGMA_1 to VGMA_M based on the first to the Mth gamma currents Igamma_1 to Igamma_M output from the gamma current generation circuit 143A. The reference gamma voltage generation circuit 145A may include the first to the Mth transistors 61_1 to 61_M. The first to the Mth transistors 61_1 to 61_M may be implemented as N-type transistors.

[0095] Each of the first to the Mth transistors 61_1 to 61_M may include a gate connected to a corresponding control line of the 2-1 to 2-M control lines 153_1 to 153_M, a gamma current generating circuit 143A, a first terminal, and a second terminal connected to the gate.

[0096] The second terminals of the first to the Mth transistors 61_1 to 61_M are connected to a power supply that supplies a power voltage (e.g., the second power voltage VSS, a ground voltage, etc.) different from the first power voltage VDD.

[0097] The first to the Mth transistors 61_1 to 61_M may have the same size. The first to the Mth transistors 61_1 to 61_M may have the same size as the driving transistor T1 of the pixel PX in FIG. 3. The gate voltages of the first to Mth transistors 61_1 to 61_M may be the first to the Mth reference gamma voltages VGMA_1 to VGMA M.

[0098] The gamma voltage generating circuit 147A may generate the first to the Mth gamma buffer voltages VG_1 to VG_M based on the first to the Mth reference gamma voltages VGMA_1 to VGMA_M. The gamma voltage generating circuit 147A may include the first to the Mth buffers 81_1 to 81_M.

[0099] The first to the Mth buffers 81_1 to 81_M may include a first input terminal (+) receiving one of the first to the Mth reference gamma voltages VGMA_1 to VGMA_M, an output terminal, a second input terminal (-) connected to the output terminal. The first to Mth buffers 81_1 to 81_M may output the first to Mth gamma buffer voltages VG_1 to VG_M to respective output terminals. [0100] The divider 149A may be formed of a resistor string. The divider 149A may generate the first to Nth gamma voltages V<0>, ..., V<N-1> through divide volt-

ages between the first to the Mth gamma buffer voltages

VG_1 to VG_M output from the gamma voltage generating circuit 147A.

[0101] FIGS. 8-9 are schematic diagrams illustrating a gamma voltage generator according to some exemplary embodiments.

[0102] Referring to FIG. 8, the gamma voltage generator 1231B may include a reference current generation circuit 141B, a gamma current generation circuit 143B, and a reference gamma voltage generation circuit 145B. [0103] For convenience of explanation, in FIG. 8, the gamma voltage generation circuit and the divider are omitted. The gamma voltage generation circuit and the divider omitted in FIG. 8 are the same as those of the gamma voltage generating circuit 147A and the divider 149A shown in FIG. 7.

[0104] The reference current generation circuit 141B may include a first transistor 21, a second transistor 22, an operational amplifier 23, and a resistor 24.

[0105] The first transistor 21 may include a pair of 1-1 transistors 21a and 1-2 transistors 21b connected in series. The 1-1 transistor 21a may include a gate connected to the 1-1 control line 151a, a first terminal connected to a source of the first power voltage VDD, and a second terminal connected to the gate and the first- 2 and the first terminal of the transistor 21b.

[0106] The 1-1 transistor 21a may be turned on and off by the gate voltage Bias1. The 1-2 transistor 21b may include a gate connected to the 1-2th control line 151b, a first terminal connected to the second terminal of the 1-1 transistor 21a, and a second terminal connected to the gate and the first terminal of the second transistor 22. The 1-2 transistor 21b may be turned on and off by the gate voltage Bias2.

[0107] The second transistor 22 may include a gate connected to the output terminal of the operational amplifier 23, a first terminal connected to the second terminal of the 1-2 transistor 21b, and a second terminal connected to the second input terminal " - " of the operational amplifier 23.

[0108] The first input terminal (+) of the operational amplifier 23 may be connected to the source of the reference voltage Vref, and the second input terminal (-) may be connected to the resistor 24. The output terminal of the operational amplifier 23 is connected to the gate of the second transistor 22. When the reference voltage Vref is applied to the first input terminal (+), the second transistor 22 may be turned on or off according to the voltage of the output terminal due to the voltage difference between the second input terminal (-) and the output terminal. The reference voltage Vref may have a value corresponding to brightness (luminance).

[0109] An output terminal voltage of the operational amplifier 23 is determined according to the reference voltage Vref and the resistance value of the resistor 24. A reference current Iref of the operational amplifier 23 may be determined by the first transistor 21 and the second transistor 22 turned on from the first power supply voltage VDD.

[0110] Although the above-described embodiment shows an example in which the reference current generation circuit 141B includes the first transistor 21 implemented as a P-type transistor and the second transistor 22 implemented as an N-type transistor according to an embodiment of the present invention, the example is not limited thereto, and the reference current generation circuit 141B may be configured by implementing the first transistor 21 and the second transistor 22 as different types of transistors, and configuring an operational amplifier corresponding thereto.

[0111] The gamma current generating circuit 143B may operate as a reference current generating circuit 141B and a current mirror. The gamma current generation circuit 143B may generate the first to the Mth gamma currents Igamma_1 to Igamma_M corresponding to mbit gamma data from a register (not shown) based on the reference current Iref. The gamma current generation circuit 143B may include the first to the Mth current conversion circuits 43_1 to 43_M. Each of the first to the Mth current conversion circuits 43_1 to 43_M may include one or more transistors connected in series and/or in parallel. The first to the Mth current conversion circuits 43_1 to 43_M may constitute a reference current generating circuit 141B and a current mirror circuit, respectively.

[0112] The gamma data may be a digital value of m bits (e.g., 8 bits of D0 to D7) corresponding to one of the first to Nth gamma voltages (V<0>, ..., V<N-1>). For example, the first current conversion circuit 43_1 may receive gamma data corresponding to the first gamma voltage V<0>, and the second current conversion circuit 43_2 may receive the fourth gamma voltage V<3)., and the third current conversion circuit 43_3 may receive gamma data corresponding to the twelfth gamma voltage V<11>.

[0113] FIG. 9 shows a first current conversion circuit 43_1, the second to the Mth current conversion circuits 43_2 to 43_M may be similarly applied.

[0114] The first current conversion circuit 43_1 may include a plurality of first transistors 431 whose gates are connected to the 1-1 control line 151a, a plurality of switches 433_1 to 433_K-1 that are turned on and off according to a gamma data, a second transistor 437, and a third transistor 439 having gates connected to the 1-2th control line 151b. The first current conversion circuit 43_1 may include the first to the Kth circuit 430_1 to 430_K. Each of the first transistor 431, the second transistor 437, and, the third transistor 439 may be implemented as a P-type transistor.

[0115] The first circuit 430_1 may include a gate connected to the 1-1 control line 151a, and a pair of first transistors 431 connected in series and provided between the first node Q1 and the third transistor 439. The pair of first transistors 431 of the first circuit 430_1 may have the same size. Each of the pair of first transistors 431 of the first circuit 430_1 may have the same size as the driving transistor of the pixel PX.

[0116] The second circuit 430_2 may include three the first transistors 431 and a first switch 433_1. The second circuit 430_2 may include a gate connected to the first-first control line 151a, a pair of first transistors 431 connected in series between the first node Q1 and the first switch 433_1, and a first transistor 431 provided between the first node Q1 and the second node Q2.

[0117] The three first transistors 431 of the second circuit 430_2 may have the same size. Each of the three first transistors 431 of the second circuit 430_2 may have the same size as the driving transistor of the pixel PX. The first switch 433_1 optionally connect the output terminal, the second terminal, of the first transistor 431 to the second transistor 437 or the third transistor 439 according to the bit value of a first bit D0 of the gamma data. [0118] The third circuit 430_3 may include three first transistors 431 and a second switch 433_2. The third circuit 430_3 may include the gate connected to the 1-1 control line 151a, a pair of first transistors 431 connected in series between the second node Q2 and the second switch 433_2, and the first transistor 431 provided between the second node Q2 and the third node Q3.

[0119] The three first transistors 431 of the third circuit 430_3 may have the same size. Each of the three first transistors 431 of the third circuit 430_3 may have the same size as the driving transistor of the pixel PX. The second switch 433_2 may optionally connect the output terminal, a second terminal, of the first transistor 431 to the second transistor 437 or the third transistor 439 according to a bit value of a second bit D1 of the gamma data.

[0120] The fourth circuit 430_4 may include three first transistors 431 and a third switch 433_3. The fourth circuit 430_4 may include a gate connected to the first-first control line 151a and a pair of first transistors 431 connected in series between a third node Q3 and the third switch 433_3. The pair of first transistors 431 of the fourth circuit 430_4 may have the same size.

[0121] Each of the pair of first transistors 431 of the fourth circuit 430_4 may have the same size as the driving transistor of the pixel PX. The third switch 433_3 may optionally connect the output terminal (second terminal) of the first transistor 431 to the second transistor 437 or the third transistor 439 according to the bit value of the third bit D2 of the gamma data.

[0122] The fifth circuit 430_5 may include a first transistor 431 and a fourth switch 433_4. The gate of the first transistor 431 of the fifth circuit 430_5 is connected to the first-first control line 151a and may be provided between the third node Q3 and the fourth switch 433_4. The first transistor 431 of the fifth circuit 430_5 may have the same size as the driving transistor of the pixel PX. The fourth switch 433_4 may selectively connect the output terminal (the second terminal) of the first transistor 431 to the second transistor 437 according to the bit value of the fourth bit D3 of the gamma data.

[0123] The sixth circuit 430_6 may include one first transistor 431 and a fifth switch 433_5. The first transistor

431 may include a gate connected to the first-first control line 151a and may be provided between the third node Q3 and the fifth switch 433_5. The size of the first transistor 431 of the sixth circuit 430_6 may be twice the size of the driving transistor of the pixel PX. The fifth switch 433_5 may selectively connect an output terminal (second terminal) of the first transistor 431 to the second transistor 437 according to the bit value of the fifth bit D4 of the gamma data.

[0124] The seventh circuit 430_7 may include one first transistor 431 and a sixth switch 433_6. the seventh circuit may include a gate of the first transistor 431 of the seventh circuit is connected to the first control line 151a and may be provided between the third node Q3 and the sixth switch 433_6. The size of the first transistor 431 of the seventh circuit may be four times that of the driving transistor of the pixel PX. The sixth switch 433_6 may selectively connect an output terminal (second terminal) of the first transistor 431 to the second transistor 437 according to the bit value of the bit selected by the selector 170 among the sixth to eighth bits D5 to D7 of the gamma data.

[0125] The selector 170 may select one of the sixth to eighth bits D5 to D7 and output the sixth to K-1th switches 433_6 to 433_K-1 of the seventh to Kth circuit 430_7 to 430_K. As shown in FIG. 9, for example, the selector 170 may select one of the sixth to eighth bits D5 to D7 and output the selected one to seven circuit according to aspect(s) of the present invention.

[0126] Since each of the eighth to Kth circuit 430_8 to 430_K is the same as the seventh circuit, a detailed description thereof will be omitted. The first to K-1th switches 433_1 to 433_K-1 may be implemented as transistors. [0127] The second transistor 437 may include a gate connected to the 1-2-th control line 151b, a first terminal, and a second terminal electrically connected to the first transistor 431 through the first to K-1th switches 433_1 to 433_K-1. The first gamma current Igamma_1 may be output through a second terminal of the second transistor 437.

[0128] A third transistor 439 may include a gate connected to the 1-2th control line 151b, a first terminal and a second terminal electrically connected to the first transistor 431 through the first to third switches 433_1 to 433_3.

[0129] The second terminal of the third transistor 439 may be connected to a power supply that supplies a voltage different from the first power voltage VDD (e.g., the second power voltage VSS, a ground voltage, etc.).

[0130] Referring back to FIG. 8, the reference gamma voltage generation circuit 145B may generate the first to Mth reference gamma voltages VGMA_1, VGMA_M based on the first to the MTh gamma currents Igamma_1, Igamma_M output from the gamma current generation circuit 143B. The reference gamma voltage generating circuit 145B may include the first to Mth transistor pairs 61 1.61 M.

[0131] The first to the Mth transistor pairs 61_1 to 61_M

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may be implemented as a pair of series-connected transistors 61a_1/61b_1, ..., 61a_M-1/61b_M-1, 61a_M/61b_M, respectively.

[0132] The transistors 61a_1 to 61a_M may include each gate connected to a corresponding control line among the 2-1 to 2-M control lines 153_1 to 153_M, a first termina connected to the gate and the gamma current generating circuit 143B, and a second terminal.

[0133] The transistors 61b_1 to 61b_M may include a gate, a first terminal, and a second terminal connected to the gate. A first terminal of the transistors 61b_1 to 61b_M may be connected to a second terminal of a corresponding one of the transistors 61a_1 to 61a_M.

[0134] The second terminal of the transistors (61b_1 to 61b_M) may be connected to a power source supplying a different power voltage(e.g., a second power voltage (VSS), ground voltage, etc.) from the first power voltage (VDD).

[0135] Each of transistors 61a_1/61b_1, 61a_2/61b_2, ..., 61a_M-1/61b_M-1, 61a_M/61b_M may have the same size. Transistors 61a_1/61b_1, 61a_2/61b_2, ..., 61a_M-1 / 61b_M-1, 61a_M/61b_M may have the same size as the drive transistors of pixels (PX).

[0136] Each gate voltage of the transistors 61a_1 to 61a_M may be a first to M reference gamma voltage VGMA_1 to VGMA_M. Each gate of transistors 61a_1 to 61a_M may be connected to the gamma voltage generation circuit.

[0137] As shown in FIG. 8, a pair of transistors 61a_1/61b_1, ..., 61a_M-1/61b_M-1, 61a_M/61b_M are examples implemented as N-type transistors. In another embodiment, the transistors (61a_1 to 61a_M) are each implemented as N-type transistors, and transistors 61b_1 to 61b_M may be implemented as P-type transistors, respectively.

[0138] Here, the transistors 61b_1 to 61b_M may each include a gate, a first terminal, and a second terminal connected to the gate. A first terminal of the transistors 61b_1 to 61b_M may be connected to a second terminal of a corresponding one of the transistors 61a_1 to 61a_M. Second terminals of the transistors 61b_1 to 61b_M may be connected to a power supply that supplies a power voltage different from the first power voltage VDD (e.g., a second power voltage VSS, a ground voltage, etc.).

[0139] Conventional gamma circuits measure gamma properties to generate a gamma voltage by a predetermined voltage setting, and a gamma adjustment is required by display device characteristic changes due to process variation. Embodiments of the present invention can implement gamma circuit using a transistor matched with the drive transistor by producing transistors of gamma circuits in the same process on the same substrate as the drive transistor of the pixel. Accordingly, the gamma characteristics required by the display device can be accurately implemented regardless of the changes that occur in the process, and the gamma voltage can be set without measuring the gamma characteristics.

[0140] In addition, embodiments of the present invention may simply generate and adjust the gamma current Igamma inherently containing gamma information by adjusting the brightness using the reference current generation circuit.

[0141] FIG. 10 is a schematic diagram shows a display device according to some embodiments.

[0142] Referring to FIG. 10, the display device 30A may include a pixel unit 110 and a driving unit.

[0143] The pixel unit 110 may be placed in the display area displaying the image. The pixel unit 110 may include a predetermined pattern, for example, it may include a plurality of pixels (PX) arranged in various patterns, such as matrix type, zigzag type, etc. Pixels (PX) may emit one color, for example, it can emit the color of one of red, blue, green, or white. Pixels (PX) may emit other colors other than red, blue, green, and white.

[0144] Pixels (PX) may include lighting devices. Lighting device can be a self-emitting device. For example, a light emitting device may be a light emitting diode (LED). Light emitting device can emit a single peak wavelength or multiple peak wavelengths.

[0145] The pixel (PX) may further include a pixel circuit connected to the pixel circuit. The pixel circuit may include at least one thin film transistor and at least one capacitor. The pixel circuit can be implemented by a semiconductor lamination structure on the substrate.

[0146] The pixel unit 110 may include scan lines SL1-SLn supplying scan signals to pixels PX, light emitting control lines EL1-ELn and pixels PX applying data signals to the pixels DL1-DLm to apply the light emitting control signal to the pixels PX. In addition, the pixel unit 110 may include a test pulse line TL1-TLn applying a test pulse signal to the pixels PX and a bias line BL1-BLn applying the bias voltage. Scan lines SL1-SLn, light emitting control lines EL1-ELn, test pulse lines TL1-TLn and bias lines BL1-BLn may be each connected to pixels PX in the same row, and each of the data lines DL1-DLm may be connected to the pixels PX arranged in the same column.

[0147] The driver and the generator are provided in a non-display area around the pixel unit 110, and drive and control the pixel unit 110. The driver and the generator may include the controller 121, the scan driver 122, the data driver 123, the power supply 124, the test pulse generation unit 125, and the bias voltage driver 126. The driver may be operated according to a drive mode and a checking mode.

[0148] In the driving mode, according to the control of the controller 121, the scan driver 122 may apply a scanning signal to scan lines SL1-SLn, and the data driver 123 may apply data signal to each pixel (PX). According to the control of the controller 121, the scan driver 122 may apply in turn a light emitting control signal to the light emitting control line EL1-ELn. Pixels (PX) may emit at a predetermined brightness corresponding to the voltage level or current level of the data signal received through the data line DL1-DLm in response to the scan signal received through scan lines SL1-SLn.

[0149] In a checking mode, according to the control of the controller 121, the scan driver 122 may apply the scan signal in turn with to scan lines (SL1-SLn), and the data driver 123 may apply a checking signal to each pixel (PX). According to the control of the controller 121, the scan driver 122 may apply the light emitting control signal in turn to the light emitting control line (EL1-ELn). According to the control of the controller 121, the test pulse generator 125 may apply the test pulse signal to each pixel (PX).

[0150] The power supply 124 may receive an external power source and/or an internal power supply apply and converts it to a voltage of various levels necessary for the operation of each component, and the voltage may be supplied to the pixel unit 110 according to the power control signal input from the controller 121.

[0151] The power supply 124 may generate a power voltage and apply the power voltage to the pixel unit 110. The power supply 124 may generate a driving voltage and supply a driving voltage to the scan driver 122, the data driver 123, and the bias voltage driver 126.

[0152] The test pulse generator 125 may generate a test pulse in the checking mode and apply it to the pixel unit 110. The test data processor 130 may measure the output test pulse in units of each row (line) of the pixel unit 110 and determine the pixel circuit is defective based on the measured value.

[0153] The controller 121, scan driver 122, the data driver 123, the power supply 124, the test pulse generator 125, and the bias voltage driver 126 may be each formed in the form of a separate integrated circuit chip or one integrated circuit chip, or mounted directly on the substrate where the pixel unit 110 is formed, mounted on flexible printed circuit film or attached to a substrate in the form of tape carrier package (TCP), or formed directly on the substrate.

[0154] FIG. 11 is a block diagram for explaining how to check whether a row (line) unit defect according to some embodiments.

[0155] Referring to FIG. 11, the test data processor 130 may include the test data latch 131 and the shift register 132.

[0156] When a test signal is input from the control unit 121, the test pulse generator 125 may generate a test pulse signal and transmit the test pulse signal in rows (lines) of the pixel unit 110 through the test pulse line TL1 to TLn.

[0157] A test data latch 131 may store a test pulse signal passed a gate chain of the pixel unit 110 contained in one row of pixels e.g., P11 to P1m. A shift registers 132 may be confirmed sequentially in rows (lines) through the test pulse signal stored in the test data latch 131 according to an aspect of the present invention.

[0158] For example, the test pulse generator 125 may apply the test pulse to the pixel unit 110 through the first test pulse line TL1 by generating a test pulse when a test signal is input from the controler 121. At this time, the test pulse applied to the first row of the pixel unit 110 may

be output through P11, P12, P13, to P1m. The test data latch 131 may store the output test pulse and can be sequentially delivered to the shift register 132.

[0159] Each pixel (e.g., P11 to P1m) may include a logical device such as an AND gate inside thereof, and each logical device may form a gate chain to pass the test pulse. The detailed structure for the gate chain is FIG. 4.

[0160] FIG. 12 is a drawing for describing the gate chain of the pixel unit according to some embodiments. [0161] Each pixel included in each row (line) of the pixel unit 110 may include an AND gate, respectively. The respective AND gate included in each pixel may include terminals corresponding to R, G, and B node voltages as input terminals.

[0162] Referring to FIG. 12, the test pulse 410 input through the first test pulse line TL1 may be input through one of the input terminals of the AND gate included in the first pixel P11. Also, an output terminal of an AND gate included in the first pixel P11 may be connected to an input terminal of an AND gate included in the second pixel P12.

[0163] Specifically, the first test pulse 410 through the first test pulse line TL1 may be input to the first row of the pixel unit 110. At this time, a state in which the output voltage is high is called 1, that is, true, and a state where the output voltage is low is called 0, that is, false. That is, when there is no defect in the bonding and the voltage states of R, G, and B nodes are all true 1, as a result of performing an AND operation between the voltage of each node and the test pulse signal, the test pulse signal may pass through the pixel P11. In other words, when the test pulse signal is true 1, the operation result output from the AND gate may also be true 1.

[0164] The operation result output from the first pixel P11 may be input to an input terminal of an AND gate included in the second pixel P12 arrayed adjacent to the same row as the first pixel P11. The AND gate included in the second pixel P12 may perform AND operation based on a voltage of the node corresponding to the subpixels (e.g., R, G, and B) included in the second pixel P12 and the operation result received from the AND gate of the first pixel P11.

[0165] Similarly, an operation result output from the second pixel P12 may be transmitted to the AND gate in the third pixel P13. The AND operation may be performed based on a voltage of the node corresponding to the subpixels (e.g., R, G, and B) in the third pixel P13 and the operation result output from the second pixel P12.

[0166] That is, when the bonding of all pixels (e.g., P11 to P1m) included in the first row is not defective and the test pulse 410 input to the first pixel P11 is true, the pulse 411 output from the mth pixel P1m may also be true 1. Conversely, if any one of the pixels included in the line has a bad bonding, the output pulse may be false 0.

[0167] For example, when any one of the pixels P21 to P2m included in the second row (e.g., P22) has a bad bonding FAIL, the test pulse 420 input through the second

test pulse line TL2 may be true 1 while the output pulse 421 may be false 0. Through this, it may be determined that at least one pixel among the pixels included in the second row is in a defective bonding, i.e., fail state.

[0168] FIG. 13A and FIG. 13B are diagrams for explaining a structure of a gate of a pixel circuit according to some embodiments. In particular, FIG.13A illustrates a common anode type pixel circuit and FIG. 13B illustrates a common cathode type pixel circuit according to aspect(s) of the present invention.

[0169] Referring to FIG. 13A and FIG. 13B, the bias voltage driver 126 may apply the bias voltage through the bias voltage line BLn to test whether the sub-pixels (eg, LED_R, LED_G, LED_B) have poor bonding. That is, when the transistor is turned on according to the bias voltage, V_R, V_G, and V_B node values corresponding to R, G, and B may be input to the AND gate.

[0170] The AND gate may determine whether to pass the test pulse signal input through the test pulse line TLn based on the V_R, V_G, and V_B node values.

[0171] Specifically, in a normal circuit without bad bonding, when the transistor is turned on by applying a bias voltage for testing, V_R, V_G, and V_B node values that are true 1 can be input to the AND gate, so that the test pulse signal with a true 1 value can be passed.

[0172] On the other hand, when bonding of any one of the PADs of the LEDs corresponding to R, G, and B is bad, the corresponding node value may be false 0. For example, when the PAD bonding corresponding to B is bad, the V_B node value becomes false 0, and the output of the AND gate also becomes false 0.

[0173] FIG. 14 illustrates a voltage-current graph in a common anode type to describe an operation of a gate of a pixel circuit according to some embodiments.

[0174] Referring to FIG. 14, the current Id flowing through the LED corresponding to each of V_R, V_G, and V_B may change according to the voltage values Vds of the V_R, V_G, and V_B nodes input to the AND gate. For example, a current graph represents a linear region up to a specific voltage value, and a saturation region from a voltage value thereafter.

[0175] In other words, the voltage values Vds of the V_R, V_G, and V_B nodes are variable according to the current Id, and in the pixel according to an embodiment of the present invention, the voltage values Vds of each of the V_R, V_G, and V_B nodes are A bias and a pixel circuit may be set to have an appropriate logic value according to the current Id.

[0176] When the respective voltage values Vds of the V_R, V_G, and V_B nodes enter a saturation region, the AND gate may determine that the corresponding node is true 1, high. That is, if bonding of the light emitting diode (LED) pad (PAD) corresponding to the V_R, V_G, and V_B nodes is all normal, when all nodes enter the saturation region, it is determined that the logic values of all nodes are true 1, High, and the test pulse signal can pass PASS.

[0177] On the other hand, when bonding of any one of

the light emitting diode LED pads corresponding to the V_R, V_G, and V_B nodes is defective, the value of the node corresponding to the defective pad does not enter the saturation region. That is, since the value of one of the input terminals of the AND gate is false 0, low, the output of the AND gate is also false 0, low and may not pass the test pulse signal Fail.

[0178] FIG. 15 is a diagram schematically illustrating a display device 30B for checking a bad pixel based on a current according to some embodiments.

[0179] The pixel unit 210 may be disposed in a display area for displaying an image. The pixel unit 210 may include a plurality of pixels PXs arranged in various patterns such as a predetermined pattern, for example, a matrix type or a zigzag type. The pixel PX emits one color, for example, one color among red, blue, green, and white. The pixel PX may emit colors other than red, blue, green, and white.

[0180] The pixel PX may include a light emitting device. The light emitting device may be a secondary light emitting device. For example, the light emitting device may be a light emitting diode (LED). The light emitting device may emit a single peak wavelength or emit a plurality of peak wavelengths.

[0181] The pixel PX may further include a pixel circuit connected to the light emitting device. The pixel circuit may include at least one thin film transistor and at least one capacitor. The pixel circuit may be implemented by a semiconductor stacked structure on a substrate.

[0182] In the pixel unit 210, scan lines SL1-SLn applying a scan signal to the pixels PX, emission control lines EL1-ELn applying an emission control signal to the pixels PX, and pixels PX) may include data lines DL1-DLm to which the data signal is applied. Also, the pixel unit 110 may include bias apply lines BL1-BLn for applying a bias voltage to the pixels PX.

[0183] The scan lines SL1-SLn, light emitting control lines EL1-ELn, and the bias apply lines BL1-BLn are respectively connected to the pixels PX arranged in the same row, and the respective data lines DL1-DLm, may be connected to the pixels PXs arranged in the same column.

[0184] The driver is provided in the un-displaying area around a pixel unit 210, and the pixel unit 210 can be driven and controlled. The driver may include a controller 221, a scan driver 222, a data driver 223, a power supply 224, a test switch driver 225 and a bias voltage driver 227. The driver may operate according to a driving mode and a checking mode.

[0185] In the driving mode, under the control of the controller 221, the scan driver 222 sequentially applies a scan signal to the scan lines SL1-SLn, and the data driver 223 applies a data signal to each pixel PX.

[0186] According to the control of the controller 221, the scan driver 222 may sequentially apply the light emitting control signal to the light emitting control lines EL1-ELn. The pixels PX may emit light with a brightness corresponding to a voltage level or a current level of a data

signal received through the data lines DL1 to DLm in response to a scan signal received through the scan lines SL1 to SLn.

[0187] In the checking mode, under the control of the controller 221, the scan driver 222 may sequentially applly a scan signal to the scan lines SL1-SLn, and the data driver 223 may apply a checking signal to each pixel PX. According to the control of the controller 221, the scan driver 222 may sequentially apply the light emitting control signal to the light emitting control lines EL1-ELn. Under the control of the controller 221, the test switch driver 225 may apply a signal for turning on the checking switch to each pixel.

[0188] Meanwhile, the checking mode may be classified into a first checking mode for checking whether pad bonding is defective, and a second checking mode for checking the chip itself.

[0189] In the first checking mode, under the control of the controller 221, a multiplexer driver 228 may sequentially control a connection of the multiplexers to check whether the pad bonding is defective in line units. The multiplexer driver 228 may measure the current flowing through the pixel unit 110 in line units of the pixel unit 110 and may be determine a defect at least one pixel PX among the pixels PX of the corresponding line based on the measured current value.

[0190] In a second checking mode, under the control of the controller 221, the chip checking unit 226 may apply a signal for turning on a switch for chip checking. In the second checking mode, the circuit of the chip itself may be checked based on the second power voltage VDD_2 flowing through the second power line VL2.

[0191] The power supply 224 may receive external power and/or internal power and convert it into voltages of various levels necessary for the operation of each component, and supply the voltage to the pixel unit 210 according to the power control signal input from the controller 221.

[0192] The power supply 224 may generate a first power voltage VDD_1 and apply it to the pixel unit 210 through the first power line VL1. The power supply 224 may generate a driving voltage and supply y it to the scan driver 222, the data driver 223, and the bias voltage driver 227. The power supply 224 may generate the second power voltage VDD_2 and supply it to the chip checking unit 226.

[0193] The controller 221, the scan driver 222, the data driver 223, the power supply 224, the test switch driver 225, the chip checking unit 226, and the bias voltage driver 227 are separated or integrated formed on a circuit chip(s), respectively.

[0194] Alternatively, the controller 221, the scan driver 222, the data driver 223, the power supply 224, the test switch driver 225, the chip checking unit 226, and the bias voltage driver 227 formed in the form of one integrated circuit chip or mounted directly on the substrate on which the pixel unit 210 is formed.

[0195] The controlle 221, the scan driver 222, the data

driver 223, the power supply 224, the test switch driver 225, the chip checking unit 226, and the bias voltage driver 227 are separated or integrated formed on a circuit chip(s) may be mounted on a flexible printed circuit film, attached to a substrate in the form of a tape carrier package (TCP), or directly formed on the substrate.

[0196] FIG. 16 is a diagram for explaining a configuration for driving a checking mode according to some embodiments

[0197] The multiplexer may divide the entire pixel unit 210 into at least one section and may include at least one multiplexer 228-1, 228-2 to 228-n connected to an output terminal of each section. The multiplexer driver 228 may control the connection to the pixel unit 210 of the at least one multiplexer 228-1, 228-2 to 228-n, respectively, to sequentially measure the current for each line of the output terminal.

[0198] When a measuring unit 230 receives a current flowing through the pixel unit 210 from the at least one multiplexer 228-1, 228-2 to 228-n, the at least one multiplexer 228-1, 228-2 to 228-n can directly measure the current value of the selected pixel, and test whether bonding is defective and based on this.

[0199] The measuring unit 230 may further include a current-voltage converter (not shown), through which the current may be converted into a voltage and then measured. As another example, the measuring unit 230 may further include a signal amplifier (not shown), through which the signal may be amplified and measured.

[0200] Meanwhile, in the checking mode of the present invention, the test switch driver 225 may control the first switch to be connected to the pixel unit 210. When the first switch is on, the pixel unit 210 may be connected to a configuration for checking the circuit itself chip and a configuration for checking the micro LED bonding state. In this case, the first switch may be implemented as a transistor, but is not limited thereto.

[0201] In the first checking mode, the test switch driver 225 may turn on the first switch, and the multiplexer driver 228 may select at least one of the multiplexers 228-1, 228-2 to 228-n. The second switch may be controlled to be connected to the pixel unit 210. That is, in the first checking mode, the measuring unit 230 may determine whether the micro LED bonding is defective for each line based on the current value input through the multiplexer. [0202] Specifically, the first switch may connect a plurality of pixels arranged in the pixel unit 210 in a row unit. According to an embodiment of the present invention, when receiving the test signal from the controller 221, the test switch driver 225 may drive the first switch so that the test pulse signal is input in units of rows (lines). [0203] Meanwhile, the second switch may connect a plurality of pixels arranged in the pixel unit 210 in units of columns. According to an embodiment of the present invention, in the first checking mode, the multiplexer driver 228 may control the second switch to sequentially connect the plurality of pixels included in the row connected by the first switch through the second switch.

[0204] For example, when the first row of the pixel unit 210 is connected by the first switch, the second switch may be connected to the pixels in the first row and first column, and the measuring unit 230 may measure a current corresponding to an operation result of an AND gate included in the pixels in the first row and first column.

[0205] Thereafter, the second switch may be sequentially connected to the pixel of in the second column of the first row, and the measuring unit 230 may measure a current corresponding to the operation result of the AND gate included in the pixel in second column of the first row. **[0206]** The pixel unit 210 may be divided into a predetermined number of sub-regions (e.g., n) in units of columns, and the multiplexers 228-1, 228-2, to 228-n may correspond to the sub-regions, respectively. In this case, each multiplexer may control the second switch to sequentially connect each of the plurality of pixels in a column unit in the sub-region.

[0207] For example, when the first multiplexer 228-1 corresponds to the first to fifth columns and the second multiplexer 228-2 corresponds to the sixth to tenth columns, the first multiplexer 228-1 may be connected to the first column, the second multiplexer 228-2 may be connected to the sixth column. Thereafter, each multiplexer may be sequentially connected to the 2nd columns and 6th columns, or the like.

[0208] According to the above-described embodiment, there is an effect that it is possible to quickly check whether bonding is defective for the entire pixel unit 210, and it is possible to determine the exact position of the defect. **[0209]** In this case, the second switch is included in the multiplexers 228-1, 228-2 to 228-n and may be implemented as an analog or digital logic circuit for connecting to at least one line of the pixel unit 210, but it is not limited thereto.

[0210] In a second checking mode, the test switch driver 225 may turn on the first switch. That is, in the second checking mode, the controller 221 may control a third switch included in the chip checking unit 226 to electrically connect the chip checking unit 226 and the pixel unit 210. That is, in the second checking mode, the chip checking unit 226 may determine whether the pixel driving circuit chip itself has an error based on the current value. In this case, the third switch may be implemented as a transistor, but is not limited thereto.

[0211] FIG. 17 is an example of a pixel of the display device 30B according to some embodiments.

[0212] In FIG. 17, for convenience of description, a pixel (Pnm) of the nth row and the mth column will be described as an example. The pixel Pnm is one of a plurality of pixels included in the nth row, and is connected to the scan line SLn corresponding to the nth row and the data line DLm corresponding to the mth column.

[0213] The pixel Pnm may connect a scan line SLn transmitting a scan signal, a data line DLm crossing the scan line SLn and transmitting a data signal, and a power line supplying a first power voltage VDD_1 and a second power voltage VDD_2.

[0214] The pixel Pnm may include a light emitting diode LED and a pixel circuit connected to the light emitting diode LED. The pixel circuit may include first to third transistors T1 to T3, a capacitor C, a checking transistor TT, and a bias transistor BT. A first electrode or a first terminal of each of the first to third transistors T1 to T3 and the bias transistor BT may be a drain terminal, and a second electrode or a second terminal may be a source terminal. [0215] The first transistor T1 has a gate electrode connected to the first electrode of the capacitor C, a first electrode connected to the light emitting diode LED through the third transistor T3, and a second electrode connected to the third power supply voltage VSS. The third power voltage VSS may be a ground voltage GND. The first transistor T1 serves as a driving transistor, and may receive a data signal according to a switching operation of the second transistor T2 to supply current to the light emitting diode LED.

[0216] The first transistor T1 may operate in a low voltage region. For example, the first transistor T1 may operate in a triode region.

[0217] The second transistor T2 may include a gate electrode connected to the scan line SLn, a first electrode connected to the data line DLm, and a second electrode connected to the gate electrode of the first transistor T1. The second transistor T2 is turned on according to the scan signal transmitted through the scan line SLn and transmits the data signal transmitted through the data line DLm to the gate electrode of the first transistor T1 as a switching transistor.

[0218] The second transistor T2 may operate in a low voltage region together with the first transistor T1. That is, the second transistor T2 may operate in a triode region. In this case, the data signal may be converted into a voltage range corresponding to the low voltage operation of the first transistor T1 and the second transistor T2.

[0219] The third transistor T3 may include a gate electrode connected to the emitting control line ELn, a first electrode connected to the second electrode of the bias transistor BT, and a second electrode connected to the first electrode of the first transistor T1.

[0220] The third transistor T3 may be turned on according to the light emitting control signal received through the light emitting control line ELn to allow the driving current of the first transistor T1 to flow through the light emitting diode LED. the light emitting control line ELn may be connected to the scan driver 222, and receive a light emitting control signal from the scan driver 222 according to FIG. 17.

[0221] In another embodiment, the light emitting control line ELn may be connected to a light emitting control driver (not shown) separate from the scan driver 122 to receive a light emitting control signal applied thereto.

[0222] The bias transistor BT may include a gate terminal connected to the bias line BLn, a first electrode connected to the second electrode of the light emitting diode LED, and a second terminal connected to the first

terminal of the third transistor T3. The bias transistor BT may be a voltage control transistor that maintains a turnon state in the driving mode by a bias voltage applied to the gate terminal and controls the drain voltage of the first transistor T1.

[0223] According to an embodiment of the present invention, since the drain voltage of the first transistor T1 is controlled by the bias transistor BT, the first transistors T1 to T3 may serve as low voltage transistors. That is, the bias transistor BT may control the drain voltage of the first transistor T1 so that the first transistor T1 operates in the triode region.

[0224] The bias transistor BT may be turned on by a bias voltage applied through the bias line BLn. The bias voltage may be a DC voltage DC of a predetermined level that allows the bias transistor BT to always maintain a turned-on state. A node voltage Vx between the third transistor T3 and the bias transistor BT, that is, a drain voltage of the third transistor T3 may be controlled according to the turn-on state of the bias transistor BT. A channel resistance of the bias transistor BT may vary according to the bias voltage. That is, the bias transistor BT may operate as a variable linear resistor.

[0225] The node voltage Vx, that is, the drain voltage of the third transistor T3 may be determined according to the channel resistance of the bias transistor BT. Accordingly, by controlling the bias voltage, the drain voltage of the third transistor T3 may be controlled to a voltage satisfying the condition that the third transistor T3 operates in the triode region.

[0226] The capacitor C may include a first electrode connected to the gate electrode of the first transistor T1 and a second electrode connected to the third power supply voltage VSS.

[0227] The first electrode of the light emitting diode LED may be supplied with the first power voltage VDD_1. The second electrode of the light emitting diode LED may be connected to the first electrode of the bias transistor BT. The light emitting diode (LED) may display an image by emitting light with a luminance corresponding to the data signal. In the checking mode, the light emitting diode (LED) may not emit light.

[0228] A first switch SW1 may be connected to a second electrode of the bias transistor BT and a first electrode of the third transistor T3. At this time, the first switch SW1 is controlled by the test switch driver 225 and may be turned on in the checking mode (the first checking mode and the second checking mode). Specifically, the first switch may include a first pole and a second pole, the first pole may be connected to the second electrode of the bias transistor BT connected to the second electrode of the plurality of light emitting devices, the two poles may be connected to nodes corresponding to the second switch SW2 and the third switch SW3.

[0229] In the first checking mode, the second switch SW2 in the multiplexer may be turned on by the multiplexer driver 228. That is, in the first checking mode, the first switch SW1 and the second switch SW2 may be

turned on.

[0230] In this case, the current flowing through a first power line VL1 may sequentially flow through the light emitting diode LED, the bias transistor BT, the first switch SW1, and the second switch SW2, and the measurement unit 230 may measure whether bonding of the pad PAD is defective by measuring a current value.

[0231] The light emitting device (LED) may be an LED included in a sub-pixel of a pixel.

[0232] In this case, the multiplexer driver 228 may control the second switch SW2 to inspect each sub-pixel.

[0233] In the second checking mode, the third switch SW3 implemented by being included in the chip checking unit 226 may be turned on by the controller 221. The third switch SW3 may be connected to the second power line VL2 to be turned on in the second checking mode, and may be turned off in the driving mode and the first checking mode. That is, in the second checking mode, the first switch SW1 and the third switch SW3 may be turned on.

[0234] In units of rows, a scan signal may be applied to the second transistor T2 through the scan line SLn, and a data signal may be applied to the data line DLm in response to the scan signal. Subsequently, the light emitting control signal may be applied to the third transistor T3 through the light emitting control line ELn. A checking control signal from the controller 221 may be applied to the third switch SW3. In this case, when the third switch SW3 is implemented as a separate transistor, a separate checking control line may be included.

[0235] The checking control signal may be applied to the third switch SW3 while the scan signal is applied to the second transistor T2 through the scan line SLn. The third switch SW3 is turned on by the checking control signal so that current can flow through the second power line VL2 passes through the third switch SW3, the third transistor T3, and the first transistor T1. The current measuring circuit of the checking unit 226 may measure the current flowing through the second power line VL2 to which the second power voltage VDD 2 is applied.

40 [0236] That is, in a second checking mode, by applying the second power voltage VDD_2 through the second power line VL2 to the pixel circuit using the third switch SW3, the pixel circuit including the first transistors to the third T1 to T3 may be checked whether being operated correctly.

[0237] FIG. 18 is a timing diagram for explaining timing in the first checking mode according to some embodiments.

[0238] Referring to FIG. 18, during the test time (SCAN_OUT1, SCAN_OUT2, etc.) at least one of multiplexer 228-1 to 228-n may be connected by sequentially changing the multiplexer code MUX code so that the current passes through the first switch SW1 and the second switch SW2. The measuring unit 230 may measure an on-current passing through to determine whether bonding of the pad is defective.

[0239] Specifically, in response to the test signal TEST_SCAN, when a test pulse signal is applied to each

row of the pixel unit 210 for 1 Line Test Time, the multiplexers 228-1 to 228-n may sequentially change the multiplexer code (MUX code) to change the second switch SW2 so that the pixels included in the corresponding row are sequentially connected according to the column order.

[0240] For example, when the test pulse signal for the first row is applied during the first test time SCAN_OUT1, the multiplexers 228-1 to 228-n may sequentially connect the pixels included in the first row in the corresponding sub-regions.

[0241] A test time for each line, 1 Line Test Time, may be flexibly set to correspond to a resolution of the display device 30 or the number of sections of the pixel unit.

[0242] On the other hand, a display device 30A of FIG. 10 and a display device 30B of FIG. 15 may be implemented as one display device. In the first checking mode, the display device may detect a pad bonding defect in a row unit through a test pulse signal, and may detect a pad bonding defect in each section by a column unit through a multiplexer according to an aspect of the present invention.

[0243] However, the above-described example is only an example, and the display device may detect a row unit pad bonding defect through a test pulse signal in a first checking mode, and detect pad bonding defects for each section in units of columns through a multiplexer in a second checking mode, and detect a circuit of the chip itself in a third checking mode, but it is not limited thereto. [0244] FIG. 19 is an example of an electronic device according to some embodiments. FIG. 20 is another example of an electronic device according to some embodiments. Referring to FIG. 19 and FIG. 20, the display device 300 may include a pixel unit 110, a driver 3120, and a parallel-to-serial converter 3130.

[0245] The pixel unit 110 may display an image using an n bit digital image signal capable of displaying 1 to 2ⁿ gray scales. The pixel unit 110 may include a plurality of pixels (pixels, PX) arranged in various patterns such as a predetermined pattern, for example, a matrix type or a zigzag type. The pixel PX may emit one color, for example, one color among red, blue, green, and white. The pixel PX may emit colors other than red, blue, green, and white.

[0246] The pixel PX may include a light emitting device. The light emitting device may be a self-light emitting device. For example, the light emitting device may be a light emitting diode (LED). The light emitting device may be a light emitting diode (LED) having a micro to nano unit size. The light emitting device may emit a single peak wavelength or emit a plurality of peak wavelengths.

[0247] The pixel PX may further include a pixel circuit connected to the light emitting device. The pixel circuit may include at least one thin film transistor and at least one capacitor. The pixel circuit may be implemented by a semiconductor stacked structure on a substrate.

[0248] The pixel PX may operate in units of frames. Each frame may include a data writing period and a light

emitting period. In the data writing period, digital data of a predetermined bit may be applied to and stored in the pixel PX. A predetermined bit of digital data stored in the light emitting period is read in synchronization with a clock signal, and the digital data is converted into a pulse width modulation (PWM) signal so that the pixel PX can express a gray level.

[0249] Meanwhile, according to an embodiment of the present invention, one frame may be composed of a plurality of subframes. Even in this case, each subframe may include a data writing period and a light emitting period, and the light emitting period of the subframe may be the sum of time allocated to each bit of digital data.

[0250] The driver 3120 may drive and control the pixel unit 110. The driver 3120 may include a controller 3121, a gamma setting unit 3123, a data driver 3125, a current supply 3127, and a clock (CK) generator 3129.

[0251] The controller 3121 may receive input image data DATA1 of one frame from an external (e.g., graphic controller), receives a correction value from the gamma setting unit 3123, and may generate correction image data by performing gamma correction on the input image data DATA1 using the correction value.

[0252] The controller 3121 may extract a grayscale for each pixel PX from the corrected image data of one frame, and convert the extracted grayscale into digital data DATA2 of a predetermined number of bits (e.g., n bits).

[0253] The controller 3121 may output nbit digital data to the data driver 3125. The time (length) of the frame may be equal to the sum of the time allocated to each bit of the n-bit digital data. The time allocated to each bit may be the same or different.

[0254] The gamma setting unit 3123 may set a gamma value using a gamma curve, set a correction value of image data according to the set gamma value, and output the set correction value to the controller 3121. The gamma setting unit 3123 may be provided as a circuit separate from the controller 3121, or may be provided to be included in the controller 3121.

[0255] The data driver 3125 may receive n bit digital data in frame units from the controller 3121 and transmit the received n bit digital data to each pixel PX of the pixel unit 110. The data driver 3125 may include a line buffer and a shift register circuit. The line buffer may be a oneline buffer or a two-line buffer. However, it is not limited thereto. The data driver 3125 may provide n-bit digital data to each pixel for each frame in line units (row units). [0256] The clock generator 3129 may generate n clock signals during one frame and output the n clock signals to the pixels PX. the clock signal may be a vertical synchronization signal (Vsync). The n clock signals may be outputted corresponding to each bit of the bit data. The signal width (length or ON time) of the clock signal may be determined according to a time allocated to each bit of the n-bit digital data. The clock generator 3129 may sequentially supply n clock signals to a clock line CL for each frame according to an embodiment of the present

invention.

[0257] Each component of the driver 3120 is formed in the form of a separate integrated circuit chip or one integrated circuit chip, directly formed on the substrate and is mounted directly on the substrate on which the pixel unit 110 is formed. The each component of the driver 3120 may be mounted on a flexible printed circuit film, attached to a substrate in the form of a tape carrier package (TCP), or formed directly on the substrate.

[0258] The controller 3121, the gamma setting unit 3123, and the data driver 3125 may be connected to the pixel unit 110 in a form of an integrated circuit chip, and the current supply 3127 and the clock generator 3129 may be formed directly on the substrate according to aspect(s) of the present invention. However, it is not limited thereto.

[0259] The parallel-to-serial converter 3130 is configured to convert n clock signals generated in parallel for each bit (e.g., MSB, LSB) into serial signals by the clock generator 3129. The parallel-to-serial converter 3130 may be a component including a logic circuit including an OR gate.

[0260] FIG. 21 is an example of explaining a circuit diagram for driving a current supply and a pixel (PX) of an electronic device according to aspect(s) of the present invention.

[0261] Referring FIG. to 21, the circuit may include a current supply 3127 and a pixel PX.

[0262] The current supply 3127 may include a first transistor 51, a second transistor 53, an operational amplifier 55, and a variable resistor 57.

[0263] The first transistor 51 may have a gate connected to the pixel PX, a first terminal connected to a power supply voltage VDD, and a second terminal connected to a gate and a first terminal of the second transistor 55. [0264] The second transistor 53 may have a gate connected to the output terminal of the operational amplifier 55, a first terminal connected to a second terminal of the first transistor 51, and a second terminal connected to the second terminal - of the operational amplifier 55.

[0265] The first input terminal (+) of an operational amplifier 55 is connected to a source of the reference voltage Vref, and a second input terminal (-) is connected to a variable resistor 57. An output terminal of the operational amplifier 55 is connected to a gate of the second transistor 53. When the reference voltage Vref is applied to the first input terminal (+), the second transistor 53 is turned on or can be turned off.

[0266] A resistance value of the variable resistor 57 may be determined according to a control signal SC from the controller 121. An output terminal voltage of the operational amplifier 55 is changed according to the resistance value of the variable resistor 57, and the current lref may be determined the first transistor 51 and the second transistor 53 turned on by the power supply voltage VDD.

[0267] A current supply 3127 may supply a driving current corresponding to the current lref to the pixel PX by

configuring a transistor and a current mirror in the pixel PX. The driving current may determine the overall luminance (brightness) of the pixel unit 110.

[0268] Although the above-described embodiment shows an example in which the current supply 127 may include a first transistor 51 implemented as a P-type transistor and a second transistor 53 implemented as an N-type transistor, it is not limited thereto, and the current supply 3127 may be configured by implementing the first transistor 51 and the second transistor 53 as different types of transistors, and configuring the operational amplifier corresponding thereto according to aspects of the present invention.

[0269] An embodiment of FIG. 21, the current supply 3127 is connected to one pixel PX, but the current supply 3127 may be shared by the plurality of pixels PX. For example, a first transistor 51 of the current supply 3127 may be electrically connected to a first transistor 501 of each of all the pixels PX of the pixel unit 110 to constitute a current mirror circuit. In another embodiment, a current supply 3127 may be provided for each row, and the current supply 3127 in each row may be shared by a plurality of pixels PX in the same row.

[0270] The pixel PX may include a light emitting device ED and a pixel circuit including a first pixel circuit 40 and a second pixel circuit 50 connected thereto. The first pixel circuit 40 may be a low voltage driving circuit, and the second pixel circuit 50 may be a high voltage driving circuit. The first pixel circuit 40 may be implemented as a plurality of logic circuits.

[0271] The light emitting device (ED) selectively may emit light or may not emit light based on a bit value (logic level) of image data provided from the data driver 3125 for each frame, so that the light emitting time is adjusted within one frame to display grayscale.

[0272] The first pixel circuit 40 may store bit values of n-bit digital data applied from the data driver 3125 in the data writing period for each frame and generate a first PWM signal based on n bit values and the clock signal in the light emission period. The first pixel circuit 40 may include a PWM controller 401 and a memory 403. In this case, the clock signal may be a serial clock signal in which n clock signals generated in parallel by the clock generator 3129 are converted into serial signals through the parallel-to-serial converter 3130. The clock generator 3129 may transmit a clock signal to each of the PWM controller 401 and the memory 403 in the first pixel circuit 40

[0273] According to an embodiment of the present invention, a frame may include a subframe. In this case, the light emitting device (ED) may emit light or may not emit light based on the bit value of image data provided for each subframe. The first pixel circuit 40 may store a bit value of data applied from the data driver 3125 in the data writing period for each subframe and generate a first PWM signal based on the bit value and the clock signal in the light emitting period.

[0274] The PWM controller 401 may generate the first

PWM signal based on the clock signal CK input from the clock generator 3129 and the bit value of the image data read from the memory 403 during the light emitting period. When a clock signal is input from the clock generator 3120, the PWM controller 401 may read a corresponding image data bit value from the memory 403 to generate a first PWM signal.

[0275] The PWM controller 401 may control the pulse width of the first PWM signal based on the bit value of the digital data and the signal width of the clock signal in units of frames. For example, if the bit value of the image data is 1, the pulse output of the PWM signal is turned on by the signal width of the clock signal, and if the bit value of the image data is 0, the pulse output of the PWM signal is turned off by the signal width of the clock signal. That is, the on time of the pulse output of the PWM signal and the off time of the pulse output may be determined by the signal width (signal length) of the clock signal.

[0276] However, this is only an embodiment, and the PWM controller 401 may control the pulse output of the PWM signal based on time information of an edge of the clock signal. In this case, the edge of the clock signal may mean that the clock signal is transitioned from a high level to a low level or from a low level to a high level. An edge transitioning from a high level to a low level may be a falling edge or a falling edge, and an edge transitioning from a low level to a high level may be a rising edge or a rising edge.

[0277] According to various embodiments of the present disclosure, the PWM controller 401 may generate a control signal of the PWM signal based on at least one of a rising edge and/or a falling edge.

[0278] For example, if the bit value of the image data is 1, the pulse output of the PWM signal is on from the time when the edge (e.g., rising edge) of the clock signal occurs until the next edge (e.g., the falling edge) occurs, and if the bit value is 0, the pulse output of the PWM signal may be turned off from the time when the edge of the clock signal occurs until the next edge.

[0279] The PWM controller 401 may include one or a plurality of logic circuits (e.g., an OR gate circuit, etc.) implemented with one or a plurality of transistors.

[0280] The memory 403 may receive n-bit data applied through the data line DL from the data driver 3125 during a data writing period for each frame or subframe in synchronization with the frame start signal or the subframe start signal and store it in advance.

[0281] In the case of a still image, image data previously stored in the memory 403 may be continuously used for image display for a plurality of frames until the image is updated or refreshed. A bit value (logic level) of n-bit data may be input from the data driver 3125 to the memory 403 in a predetermined order.

[0282] In an embodiment, the predetermined order in which bit values of n-bit data are stored may be from a least significant bit (LSB) to a most significant bit (MSB) of a bit string. In another embodiment, the predetermined order in which bit values of n-bit data are stored may be

from MSB to LSB. The memory 403 may store at least 1 bit data.

[0283] In one embodiment, the memory 403 may be an n bit memory. In the memory 403, n bit values of n bit data may be written during the data writing period. The memory 403 may be implemented with one or a plurality of transistors. The memory 403 may be implemented with random access memory (RAM), for example, SRAM or DRAM.

[0284] The memory 403 responds to the clock signal CK input from the clock generator 3129 during the light emission period, and a bit value of a part of the bit values of the n bit digital data applied and stored from the data driver 3125. may be additionally stored, and the additionally stored bit value may be used for displaying an image during at least one or more frames. In one embodiment, the additionally stored bit value may be an MSB of n-bit data.

[0285] In one embodiment, in a case of a difference between a writing rate of the first n bit data on a memory and reading rate of the pre-stored the first n bit data from the memory during a writing period, the PWM controller 401 may incompletely read by storing a new second n bit data before reading all the prestored the first n bits data from the memory 403, thereby displaying image data on the display may be failed. For example, when an electronic device operates in a MIPI command mode, a difference may occur in the reading rate by the PWM controller 401 and the writing rate at which the video data is stored in memory 403.

[0286] For example, if the first n bit data is stored in memory 403 during a data writing period, the PWM controller 401 may incompletely read the pre-stored n bit data if the new second n-bit data is stored while reading the pre-stored the first n bit data in the memory 403.

[0287] In this case, all bit values of the existing stored n bit data can be fully read by reading some of the additional stored bit values of the data of the first n bit. Memory 403 may be used for continuous image display for a plurality of frames with additional stored bit values even if another clock signal is input from the clock generator 129 during the luminescence period.

[0288] In an embodiment, the memory 403 may additionally store the bit values of some of the stored bit values of the n-bit digital data at a time point when the memory 403 receives the clock signal after the data writing period. [0289] For example, during the data writing period, data of 1st n bits of data may be stored in the memory 403, and the memory 403 may additionally store the bit value of a part of the first n-bit data, the PWM controller 401 may read the bit value of the first n-bit data when the clock generator 129 transmits the k-1th clock signal to the memory 403 and the PWM controller 401.

[0290] Thereafter, for example, due to the difference between the writing speed and the reading speed, when the new second n-bit data is stored in the memory 403 while the first n-bit data is read, the PWM controller 401 may read all the bit values of the first n bits of data based

on the values of some of the additionally stored bits.

[0291] After that, when the generator 129 transmits the k-th clock signal to the memory 403 and the PWM controller 401, the memory 403 additionally may store a bit value of a part of the second n-bit data, and the PWM controller 401 may read the bit value of the data of the second n bits.

[0292] Through the same process, the bit values of the image data can be completely read without any problems despite the difference between the writing speed and the reading speed.

[0293] When the n-bit digital data is stored to the memory 403 without conversion, the memory 403 must have a capacity for storing the n-bit digital data, which may be a constraint on the size of the pixel.

[0294] When the memory 403 has a 1-bit capacity, since the pixel has to be driven in a plurality of subframes, the driving frequency increases, and the current consumption due to the increase in the driving frequency increases, which may be a limiting factor in the case of a battery-using product.

[0295] In addition, a different time must be allocated for each subframe. In an embodiment of the present invention, by using a bit memory smaller than n bits for the memory 403, the memory capacity can be reduced, thereby reducing the pixel size. In addition, by using a bit memory smaller than n bits, the number of subframes can be reduced compared to a 1-bit memory, so that the driving frequency can be properly maintained.

[0296] The second pixel circuit 50 may control light emitting and non-light emitting of the light emitting device (ED) in response to the control signal applied from the first pixel circuit 40 to each in one frame unit or subframe unit. The control signal may be a PWM signal. The second pixel circuit 50 may include the first transistor 501, the second transistor 503 and the level shifter 505 electrically connected to a current supply 127.

[0297] The first transistor 501 may output a driving current. The first transistor 501 may include a gate connected to a current supply 3127, a first terminal connected to a source voltage VDD, and a second terminal connected to a first terminal of the second transistor 503.

[0298] The gate of the first transistor 501 may be connected to the gate of the first transistor 51 of the current supply 3127 to form a current supply 3127 and a current mirror circuit.

[0299] Accordingly, as the first transistor 51 of the current supply 3127 is turned on, the turned-on first transistor 501 may supply a driving current corresponding to the current Iref formed in the current supply 3127. The driving current may be the same as the current Iref flowing through the current supply 3127.

[0300] The second transistor 503 may transmit or block the driving current to the light emitting device ED according to the PWM signal. The second transistor 503 may include a gate connected to the output terminal of the level shifter 505, a first terminal connected to a second terminal of the first transistor 501, and a second terminal

connected to the light emitting device ED.

[0301] The second transistor 503 may be turned on or off according to a voltage output from the level shift 505. The emission time of the light emitting device ED may be adjusted according to the turn-on or turn-off time of the second transistor 503. The second transistor 503 is turned on when a gate-on level signal (a low level in FIG. 21) is applied to the gate and outputs the driving current Iref output from the first transistor 501 to the light emitting device ED so that the light emitting device ED may emit light.

[0302] As shown in FIG. 21, the second transistor 503 is turned off when a gate-off level signal is applied to the gate, the driving current lref output from the first transistor 501 to the light emitting device ED may be blocked so that the light emitting device (ED) may not emit light.

[0303] The light emitting time and non-emission time of the light emitting device ED may be controlled by the turn-on time and turn-off time of the second transistor 503 during one frame, so that the color depth of the pixel unit 110 can be expressed. A turn-on time and turn-off time of the second transistor 503 for one frame may be determined according to the pulse width of the first PWM signal.

[0304] A level shifter 505 may be connected to the output terminal of the PWM controller 401 of the first pixel circuit 40 and convert the voltage level of the first PWM signal output by the PWM controller 401 to generate the second PWM signal. The level shifter 505 may generate the first PWM signal, a gate-on voltage level signal for turning on the second transistor 503 and the second PWM signal, a gate-off level signal for turning off the second transistor 503.

[0305] When the first PWM signal output from the PWM controller 401 is sufficient to drive the second transistor 503, the level shifter 505 may be omitted. The pulse voltage level of the second PWM signal output from the level shifter 505 may be higher than the pulse voltage level of the first PWM signal, and the level shifter 505 may include a boosting circuit for boosting the input voltage. The level shifter 505 may be implemented with a plurality of transistors.

[0306] Although the above-described embodiment shows an example in which the pixel is composed of P-type transistors, the embodiment of the present invention is not limited thereto, and the pixel is composed of N-type transistors, and in this case, the pixel is applied with P-type transistors. It can be driven by a signal whose level is inverted.

[0307] FIG. 22 is an example illustrating driving timing of a general clock signal according to some embodiments. Referring to FIG. 22, the vertical synchronization signal Vsync may be a signal representing a frame of a video signal. In one embodiment. The vertical synchronization signal Vsync may be a signal representing a subframe of a video signal. One frame may be composed of at least one or more scan signals, and the scan signal may be generated and transmitted by the clock generator

129.

[0308] The scan signals may correspond to a horizontal synchronization signal (H-sync). The frame may include an active period, and the active period may include a plurality of scan signals carrying video data according to an aspect of the present invention. The frame may include a front porch and a back porch period before and after the active period, and may include a front capture period of the scan signal before and after the scan signal, and a back porch period of the scan signal.

[0309] Each scan signal may include a plurality of pixels, and actual video data may be read based on the PWM controller receiving the scan signal. For example, the vertical synchronization signal Vsync may be a clock signal CK for outputting data to the pixels PX in the vertical direction of the display device, and the scan signal is transmitted to the pixels PX in the horizontal direction of the display. It may be a clock CK signal for outputting data

[0310] The display device may include the pixels PX, which may output image data from the bottom to the top and from the left to the right of the display device based on the vertical synchronization signal and the scan signal according to an aspect of the present invention. The display device screen may be synchronized by outputting image data to the pixels PX based on the vertical synchronization signal and the scan signal according to an aspect of the present invention.

[0311] FIG. 23 is another example showing a driving timing of a typical clock signal according to some embodiments. FIG. 23 shows a pixel-driven example of the first row of the display device. Referring to FIG. 23, the pixel (PX) may be driven including the data writing period DT and light emitting period T for one frame. The light emitting period T may be driven by dividing it into the first subframe SF1 to the first subframe SFn.

[0312] In the data writing period T, the bit value of the image data DATA from the data driver 125 may be written to the memory 403 in the pixel PX.

[0313] The clock signal CK may be applied to the PWM controller 401 in each subframe of the light emitting period T, and the PWM controller 401 may generated the PWM signal based on the bit value of the image data DATA recorded in the memory 403 and the clock signal CK.

[0314] The length of time allocated to each of the first subframe SF1 to the nth subframe SFn may be different. For example, the first length T/2 is allocated to the first subframe SF1, the second length $T/2^2$ is allocated to the second subframe SF2, and the third subframe SF3 may be allocated a third length $T/2^3$, and an nth subframe SFn may be allocated an nth length $T/2^n$.

[0315] The image data DATA may be expressed by n bits including the most significant bit and the least significant bit. For example, the order of the most significant bit MSB to the least significant bit LSB may correspond to the order of the first subframe SF1 to the nth subframe SFn.

[0316] The clock signal CK may include the first clock signal CK1 to the nth clock signal CKn, and the first clock signal CK1 to the nth clock signal CKn may be output in order corresponding to the order of the first subframe SF1 to the nth clock signal CKn.

[0317] The length of the clock signal CK may be different for each subframe. For example, the first clock signal CK1 corresponding to the first subframe SF1 allocated to the most significant bit MSB of the image data DATA has a first length T/2, The second clock signal CK2 corresponding to the second subframe SF2 allocated to the second significant bit MSB-1 of the image data DATA has a second length T/2², and the nth clock signal CKn corresponding to the nth subframe SFTn allocated to the least significant bit LSB of the image data DATA may have an nth length T/2n.

[0318] In each of the first subframes SF1 to nth subframes SFn, the PWM controller 401 may read the corresponding bit value of the image data DATA from the memory 403. The pulse width of the PWM signal may be controlled based on the signal width of the clock signal CK and the bit value of the image data DATA.

[0319] The PWM controller 401 may generate the PWM signal PWM based on the bit values of the clock signal CK and the image data DATA output to the first subframe SF1 to the nth subframe SFn.

[0320] For example, when the image data DATA has n bit values of 101....1, the PWM controller 401 may output a pulse having a pulse width of a first length T/2 based on the bit value 1 of the MSB of the image data DATA and the first clock signal CK1. The PWM controller 401 may turn off the pulse output for the second length T/22 based on the bit value 0 of MSB-1 of the image data DATA and the second clock signal CK2. The PWM controller 401 may output a pulse having a pulse width of an nth length (T/2n) based on the bit value 1 of the LSB of the image data DATA and the nth clock signal CKn.

[0321] The light emitting device ED may emit light or may not emit light according to a pulse output of the PWM signal during one frame. When the pulse output is turned on, the light emitting device ED may emit light for a predetermined time corresponding to a pulse width. The light emitting device ED may not emit light as long as the pulse output is off.

[0322] FIG. 24 is an example of a display operation in a mobile industry processor interface MPIP video mode and a command mode according to clock signal(s) according to an aspect of the present invention.

[0323] The left figure of FIG. 24 is an example of display operation in MPIP video mode according to an aspect of the embodiment. Referring to the left figure of FIG.24, in the video mode, the difference between the writing speed at which video data is stored in the memory and the reading speed at which the video data stored in the memory is read may be ignored or may be not ignored. In an embodiment, the display device may store video data in the pixels PX from the bottom to the top and from the left to the right of the display device based on the vertical

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sync signal and the scan signal, when outputting, there is no difference between the data writing speed and the reading speed based on the scan signal, so video data can be output from the host in real time.

[0324] A right figure of FIG. 24 is an example of display operation in MPIP command mode. Referring to right figure of FIG. 24, in a command mode, a difference occurs between a writing speed at which video data is stored in the memory and a reading speed at which video data stored in the memory is read.

In one embodiment, when the display device may store and output video data to the pixels (PX) from the first row of the display device, from the left to the right, based on the vertical sync signal and the scan signal, a difference in the reading speed based on the data writing rate and the scan signal may not normally display the video data in the pixel (PX) of a specific area of the display device. [0325] An aspect of the present invention may have a configuration for adjusting the clock signal driving timing from the LSB to the MSB direction, which will be described in FIG. 25.

[0326] An aspect of the present invention may have a configuration for additionally storing some of the bit values of the video data in the memory 403 in the pixel PX, the above configurations can solve an output failure that may cause a difference between the data writing speed and the reading speed based on the scan signal in the MIPI command mode in FIG. 26.

[0327] FIG. 25 illustrates an example of an operation according to a clock signal driving timing change according to aspects of the present invention. Referring to FIG. 25, the display device 30 may include a driving timing of a clock signal different from a driving timing of a general clock signal. A figure 801 on the left side of FIG. 25 shows a driving timing of the general clock signal of the display device 30 described in FIG. 6 and a figure 803 on the right side of FIG. 25 shows the driving timing of the clock signal different from the general driving timing of the clock signal of the display device 30 shown in FIG. 23.

[0328] Referring to the right figure of FIG. 25, unlike a driving timing of the general clock signal, the pixel PX of the display device 30 may adjust the driving timing of the clock signal from "the MSB to the LSB" to "the LSB to the MSB" to minimize the number of affected bit values, thereby preventing a situation in which a plurality of bit values is affected.

[0329] For example, the emission period T of the display device 30 having a driving timing of a clock signal different from a driving timing of a typical clock signal is divided into the first subframe SF1 to the nth subframe SFn. The length of time allocated to each of the first subframe SF1 to the nth subframe SFn may be different. For example, a first length $T/2^n$ is allocated to the first subframe SF1, a second length $T/2^{n-1}$ is allocated to the second subframe SF2, and a third subframe A third length $T/2^{n-2}$ may be allocated to (SF3), and an nth length T/2 may be allocated to an n-th subframe SFn.

[0330] The image data DATA may be expressed by n

bits including the least significant bit and the most significant bit, and may correspond to the order of the first subframe SF1 to the nth subframe SFn in the order of the least significant bit to the most significant bit.

[0331] The clock signal CK may include the first clock signal CK1 to the nth clock signal CKn, and the first clock signal CK1 to the nth clock signal CKn includes the first subframe SF1 to the nth clock signal CKn. They may be output in order corresponding to the order of the n subframes SFn.

[0332] The length of the clock signal CK may be different for each subframe. For example, the first clock signal CK1 corresponding to the first subframe SF1 allocated to the least significant bit LSB of the image data DATA has a first length T/2n, and the image data (DATA), the second clock signal CK2 corresponding to the second subframe SF2 allocated to the lower-order bit LSB+1 of the DATA) has a second length T/2n-1, and the image data DATA The n-th clock signal CKn corresponding to the n-th subframe SFTn allocated to the most significant bit MSB may have an n-th length T/2).

[0333] In each of the first subframes SF1 to nth subframes SFn, the PWM controller 401 may read the corresponding bit value of the image data DATA from the memory 403, control the pulse width of the PWM signal based on the signal width of the clock signal CK and the bit value of the image data DATA.

[0334] The PWM controller 401 may generate the PWM signal PWM based on the clock signal CK output to the first subframe SF1 to the nth subframe SFn and the bit values of the image data DATA.

[0335] For example, when the image data DATA has n bit values of 1....101, the PWM controller 401 may output a pulse having a pulse width of a first length T/2ⁿ based on a bit value 1 of the LSB of the image data DATA and the first clock signal CK1.The PWM controller 401 may turn off the pulse output for the second length T/2ⁿ⁻¹ based on the bit value 0 of the LSB+1 of the image data DATA and the second clock signal CK2. The PWM controller 401 may output a pulse having a pulse width of an nth length T/2 based on the bit value 1 of the MSB of the image data DATA and the nth clock signal CKn.

[0336] The light emitting device ED may emit light or may not emit light according to the pulse output of the PWM signal during one frame. When the pulse output is turned on, the light emitting device ED may emit light for a predetermined time corresponding to the pulse width. The emitting device ED may not emit light as long as the pulse output is off.

[0337] Unlike the driving timing of the general clock signal, the display device 30 may drive to read the bit values of the video data in the order of the least significant bit to the most significant bit, so that the difference between the data writing speed and the reading speed of the memory is reduced as in the MIPI command mode. It is possible to prevent a case in which the bit value of data is incompletely read and an error occurs in displaying the image data on the display.

[0338] For example, if there is a difference between the data writing speed and the reading speed of the memory in the driving timing of the general clock signal, the data is read from the most significant bit to the least significant bit, so at least one lower bit including the LSB is included. Before the reading of the bit values to be read is completed, video data to be received thereafter may be received by the display device and stored in the memory, and a plurality of low-order bit values may not be read because the times allocated to the subframe corresponding to the high-order bits are longer than the times allocated to the subframe corresponding to the low-order bits

[0339] Accordingly, by adjusting the driving timing of the clock signal to read the clock signal in the order of the least significant bit to the most significant bit, it is possible to reduce the number of bits that may be affected by the difference between the data write speed and the read speed.

[0340] For example, since the time allocated to the subframe corresponding to the MSB corresponds to the latter half of the light emission period T, only one MSB may be affected by the difference between the data writing speed and reading speed.

If the driving timing of the clock signal is adjusted to read from the least significant bit to the most significant bit, incomplete reading of data can be prevented by storing the reduced number of bits in advance through minimal hardware or storage space, and driving the existing clock signal since a minimum amount of hardware or storage space is used compared to timing, power consumption of the display device 30 may be reduced.

[0341] FIG. 26 is an example of an electronic device including an additional memory in a memory inside pixel (MIP) circuit according to an aspect of the present invention

[0342] Referring to FIG. 26, the first pixel circuit 40 may include a PWM controller 401 and a memory 403. The display device 30 may store the number of bits that may be affected by the difference between the data writing speed and the reading speed in advance using the memory 403 in the first pixel circuit 40 by controlling a timing of the clock signal to read the bit values of the video data in the order of the least significant bit to the most significant bit.

[0343] According to an embodiment of the present invention, in responds to a clock signal CK input from the clock generator 3129, the memory 403 in the first pixel circuit 40 may additionally store some bit values of the bit values of the n-bit digital data supplied and stored from the data driver 3125, the additionally stored bit values may be used for image display during at least one frame or more.

[0344] In one embodiment, the additionally stored bit value may be an MSB of n bit data. For example, during the data writing period, data of first n bits of data is stored in the memory 403, when the new second n-bit data is stored in the memory 403 while the PWM controller 401

receives the m-th clock signal and reads the first n-bit data, the bit value of the first n-bit data may be incompletely read.

[0345] In this case, it is possible to completely read all the bit values of the previously stored n-bit digital data by reading some bit values additionally stored among the first n-bit data.

[0346] The memory 403 may use the additionally stored bit values to continuously display images for a plurality of frames even when another clock signal is input from the clock generator 3129 during the light emission period.

[0347] In an embodiment, the memory 403 may additionally store the MSB among the stored bit values of the n-bit digital data at a time point when the memory 403 receives the clock signal after the data writing period. For example, during the data writing period, data of the first n bits of data is stored in the memory 403, and the clock generator 129 transmits the m-1-th clock signal to the memory 403 and the PWM controller 401. When the memory 403 additionally stores the MSB of the first n-bit data, the PWM controller 401 may read the bit value of the first n-bit data.

[0348] Thereafter, due to the difference between the write speed and the read speed, when the new second n-bit data is stored in the memory 403 while the first n-bit data is read, the PWM controller 401 stores the additionally stored MSB, the PWM controller 401 may read all bit values of the first n-bit data based on the additionally stored MSB.

[0349] Thereafter, when the generator 129 transmits the mth clock signal to the memory 403 and the PWM controller 401, the memory 403 additionally may store the MSB of the second n-bit data, and the PWM controller 401 may send the second by reading the bit value of n bits of data, it is possible to completely read the bit values of data without failure.

[0350] According to various embodiments, the electronic device (e.g., the display device 30) may receive the first video data including at least one or more bit values, and generate other clock signals, an allocated period corresponding to each of the at least one or more bit values is mutually exclusive, in order from least significant bit (LSB) to most significant bit (MSB).

[0351] A controller configured to read each of the at least one or more bit values from a first memory in response to each of the generated clock signals to determine control data, a first memory configured to store at least one or more bit values of the first video data and a pixel circuit configured to control light emission of a pixel (PX) based on the control data.

[0352] According to various embodiments, the electronic device may further include a second memory configured to store the MSB when a clock signal other than a clock signal corresponding to the MSB of the first video data stored in the first memory is generated.

[0353] According to various embodiments, when the controller receives second video data including at least

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one or more bit values, the second video corresponding to at least one or more bit values of the first video data of the first memory and store and change at least one or more bit values of data, and the second memory may be further configured to read the stored MSB from the second memory to determine the control data.

[0354] According to various embodiments, a clock signal other than the corresponding clock signal may be a clock signal corresponding to the higher order bit.

[0355] According to various embodiments, the allocated period may increase in an order of a least significant bit (LSB) to a most significant bit (MSB) of the corresponding at least one or more bit values.

[0356] According to various embodiments, the increment of the increasing allocated period may be twice that of the lower bit.

[0357] According to various embodiments, the controller may be further configured to store the at least one or more bit values in the first memory in the order of the LSB to the MSB.

[0358] According to various embodiments, the controller may receive video data from the host through a mobile industry processor interface (MIPI) command mode.

[0359] Electronic devices according to various embodiments of the present disclosure may be devices of various types. The electronic device may include, for example, a portable communication device (e.g., a smart phone), a computer device, a portable multimedia device, a portable medical device, a camera, a wearable device, or a home appliance device. The electronic device according to the embodiment is not limited to the above-described devices.

[0360] In the current disclosure, reference is made to various embodiments. However, the scope of the present disclosure is not limited to specific described embodiments. Instead, any combination of the described features and elements, whether related to different embodiments or not, is contemplated to implement and practice contemplated embodiments. Additionally, when elements of the embodiments are described in the form of "at least one of A and B," it will be understood that embodiments including element A exclusively, including element B exclusively, and including element A and B are each contemplated. Furthermore, although some embodiments disclosed herein may achieve advantages over other possible solutions or over the prior art, whether or not a particular advantage is achieved by a given embodiment is not limiting of the scope of the present disclosure. Thus, the aspects, features, embodiments and advantages disclosed herein are merely illustrative and are not considered elements or limitations of the appended claims except where explicitly recited in a claim(s). Likewise, reference to "the invention" shall not be construed as a generalization of any inventive subject matter disclosed herein and shall not be considered to be an element or limitation of the appended claims except where explicitly recited in a claim(s).

[0361] As will be appreciated by one skilled in the art,

the embodiments disclosed herein may be embodied as a system, method or computer program product. Accordingly, embodiments may take the form of an entirely hardware embodiment, an entirely software embodiment (including firmware, resident software, micro-code, etc.) or an embodiment combining software and hardware aspects that may all generally be referred to herein as a "circuit," "module" or "system." Furthermore, embodiments may take the form of a computer program product embodied in one or more computer readable medium(s) having computer readable program code embodied thereon. For example, according to an embodiment, the module may be implemented in the form of an application-specific integrated circuit (ASIC).

[0362] Program code embodied on a computer readable medium may be transmitted using any appropriate medium, including but not limited to wireless, wireline, optical fiber cable, RF, etc., or any suitable combination of the foregoing.

[0363] Computer program code for carrying out operations for embodiments of the present disclosure may be written in any combination of one or more programming languages, including an object oriented programming language such as Java, Smalltalk, C++ or the like and conventional procedural programming languages, such as the "C" programming language or similar programming languages. The program code may execute entirely on the user's computer, partly on the user's computer, as a stand-alone software package, partly on the user's computer and partly on a remote computer or entirely on the remote computer or server. In the latter scenario, the remote computer may be connected to the user's computer through any type of network, including a local area network (LAN) or a wide area network (WAN), or the connection may be made to an external computer (for example, through the Internet using an Internet Service Provider).

Aspects of the present disclosure are described [0364] herein with reference to flowchart illustrations and/or block diagrams of methods, apparatuses (systems), and computer program products according to embodiments presented in this disclosure. It will be understood that each block of the flowchart illustrations and/or block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, can be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the block(s) of the flowchart illustrations and/or block diagrams.

[0365] The steps of the method or algorithm described in the embodiments of the disclosure may be implemented in a hardware manner, and may also be implemented in a manner of executing, by a processor, software. A

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software instruction may consist of a corresponding software module, and the software module may be stored in a RAM, a flash memory, a Read Only Memory (ROM), an Erasable Programmable ROM (EPROM), an Electrically EPROM (EEPROM), a register, a hard disk, a mobile hard disk, a Compact Disc-ROM (CD-ROM) or a storage medium in any other form well known in the field. An exemplary storage medium is coupled to the processor, thereby enabling the processor to read information from the storage medium and write information into the storage medium. Of course, the storage medium may also be a component of the processor. The processor and the storage medium may be located in an ASIC. In addition, the ASIC may be located in an access network device. a target network device or a core network device. Of course, the processor and the storage medium may also exist in the access network device, the target network device or the core network device as discrete components.

[0366] In addition, the programs may be stored in an attachable storage device which is accessible through communication networks such as the Internet, Intranet, local area network (LAN), wide area network (WAN), and storage area network (SAN), or a combination thereof. Such a storage device may access the electronic device via an external port. Further, a separate storage device on the communication network may access a portable electronic device.

[0367] The abovementioned specific implementation modes further describe the purposes, technical solutions and beneficial effects of the embodiments of the disclosure in detail. It is to be understood that the above is only the specific implementation mode of the embodiments of the disclosure and not intended to limit the scope of protection of the embodiments of the disclosure. Any modifications, equivalent replacements, improvements and the like made based on the technical solutions of the embodiments of the disclosure shall fall within the scope of protection of the embodiments of the disclosure.

[0368] Following the above-described embodiments, the invention is further related to the following numbered items:

1. The electronic device comprising:

a controller configured to receive a first video data including at least one or more bit values, generate clock signals having different assigned periods corresponding to each of the at least one or more bit values in the order of least significant bit (LSB) to most significant bit (MSB), and determine control data by reading each of the at least one or more bit values from a first memory in response to each of the generated clock signals; a first memory configured to store at least one bit value of the first video data; and a circuit including a pixel circuit configured to control light emission of a pixel (PX) based on the control data.

- 2. The electronic device of item 1, the electronic device further comprising:
- a second memory configured to store the MSB if the controller generates an another clock signal other than the clock signal the corresponds to the MSB of the first video data.
- 3. The electronic device of item 2, wherein the controller upon receiving the second video data including at least one or more bit values, converts the at least one or more bit values of the first video data of the first memory to the corresponding at least one or more bits of the second video data, and stores to the second memory, reads the stored the MSB, and determines control data.
- 4. The electronic device of item 2, wherein the clock signal other than the corresponding clock signal is a clock signal corresponding to a lower order bit.
- 5. The electronic device of item 1, wherein the allocated period increases in the order of the LSB to the MSB of the corresponding at least one bit or more than bit values.
- 6. The electronic device of item 5, wherein an increment of the increasing allocated period is twice that of the lower bit.one
- 7. The electronic device of item 1, wherein the controller is further configured to store the at least one bit or more than bit values in the first memory in order from the LSB to the MSB.
- 8. The electronic device of item 1, wherein the controller receives video data from a host through a mobile industry processor interface (MIPI) command mode.

Claims

1. A display device comprising:

- a pixel unit including a plurality of pixels, each including a luminous element and a pixel circuit connected to the luminous element;
- a clock generator configured to generate a plurality of clock signals each corresponding to each of a plurality of subframes constituting a frame; and
- a parallel to serial converter configured to convert the plurality of clock signals to a serial clock signal and transfer the serial clock signal to the pixel unit; and
- wherein the pixel circuit of each pixel includes:

a first pixel circuit configured to control light-

emission and non-emission of the luminous element in response to a control signal applied to each of the plurality of subframes; and

a second pixel circuit configured to store bit values of image data in the frame and generate the control signal based on the stored bit values and the serial clock signal such that each subframe included in the frame is controlled according to each bit value.

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2. The display device of claim 1,

wherein each of the plurality clock signals is generated to include an edge at which level is switched when corresponding subframe starts; and

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wherein the serial clock signal includes the edges included in the clock signals.

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3. The display device of claim 1, wherein the second pixel circuit includes:

a memory configured to store the bit values of the image data; and

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a pulse width modulation (PWM) controller configured to read the bit values from the memory and determine a pulse width of the control signal for the subframe based on a length of the subframe and the bit value corresponding to the subframe.

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FIG. 1

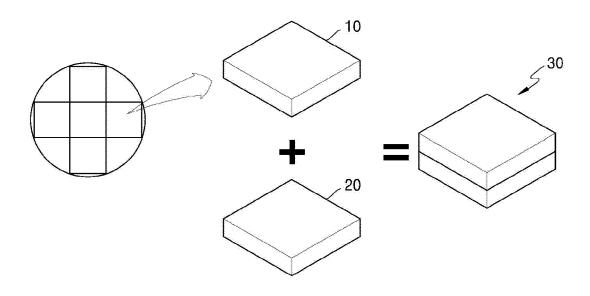


FIG. 2

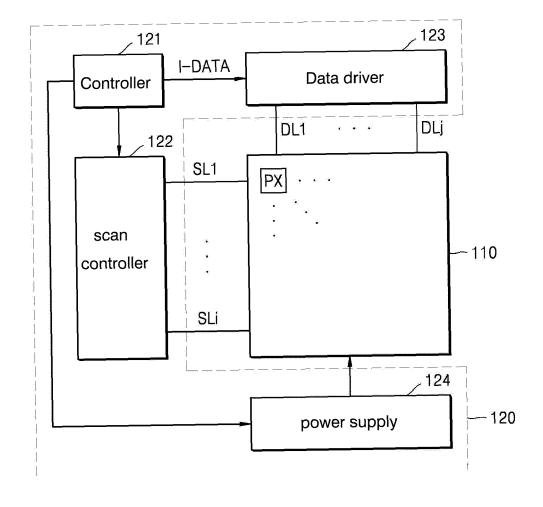


FIG. 3

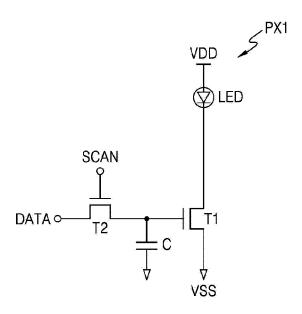


FIG. 4

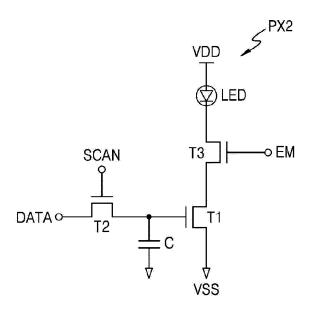
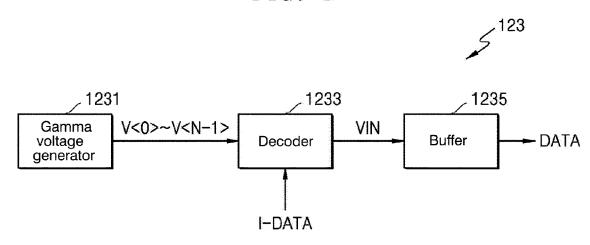
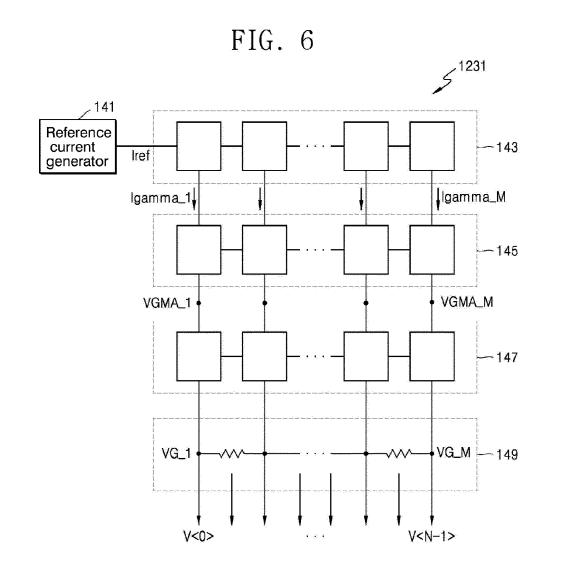


FIG. 5





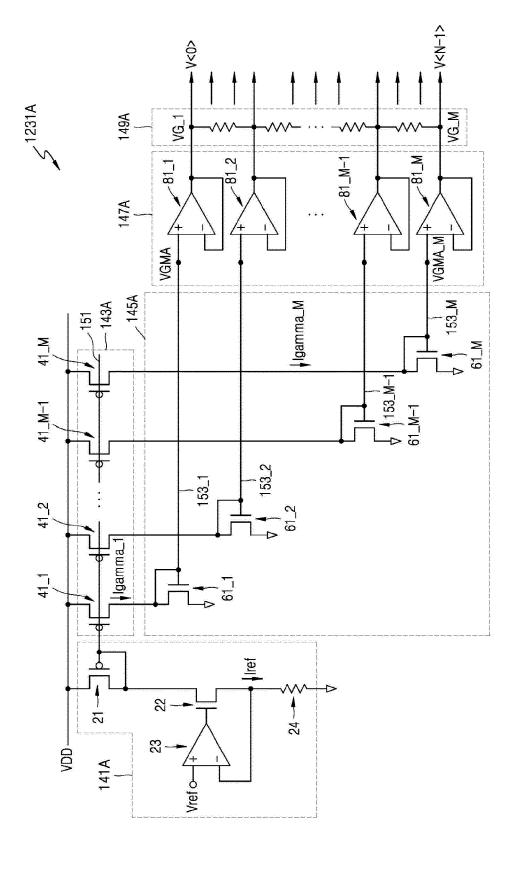
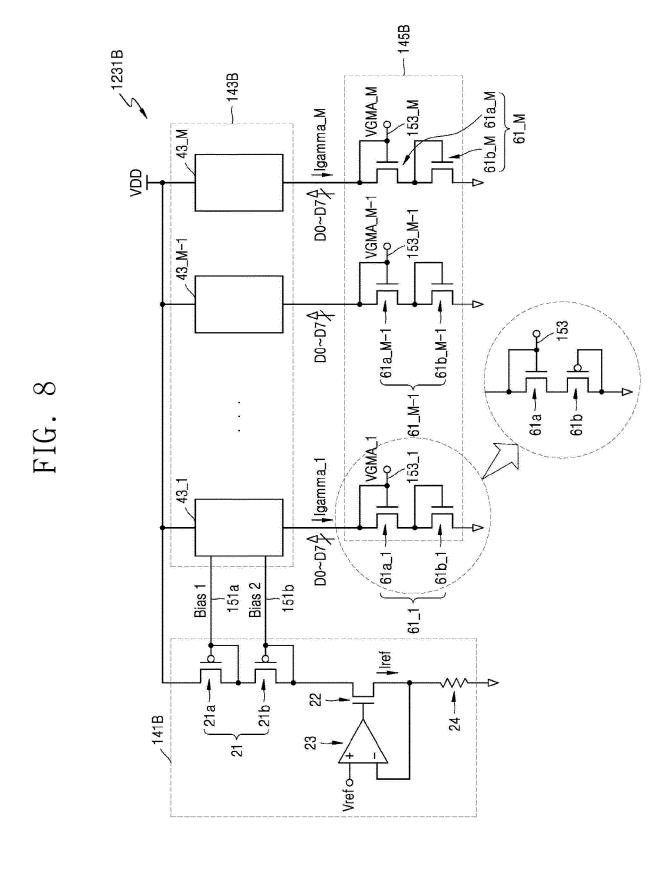


FIG.



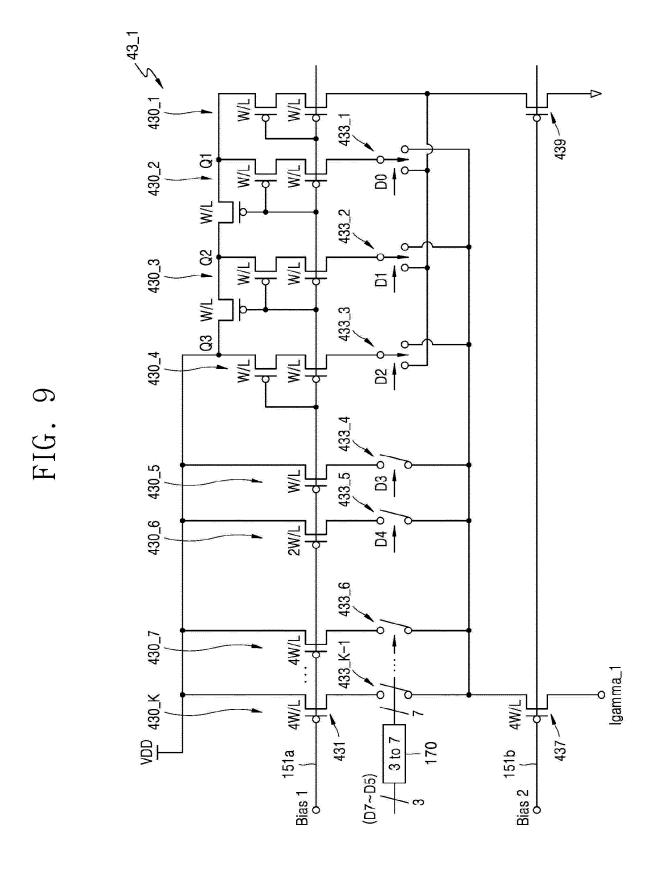
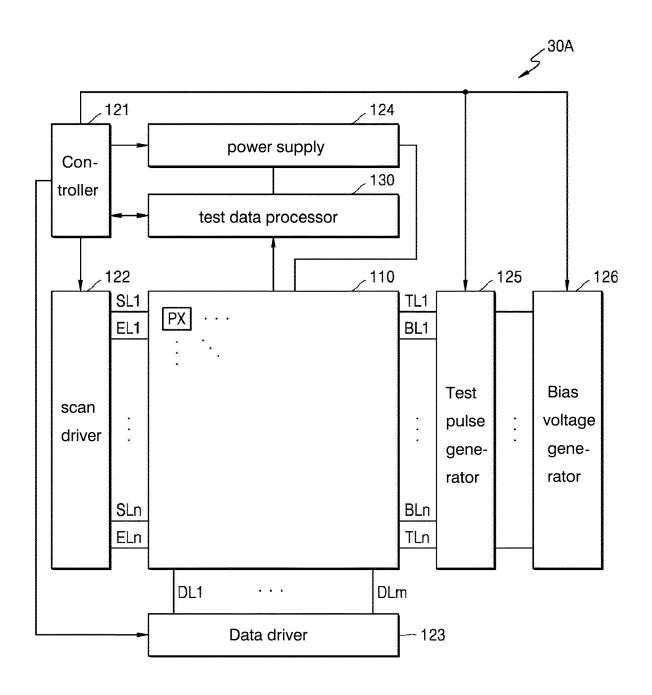


FIG. 10



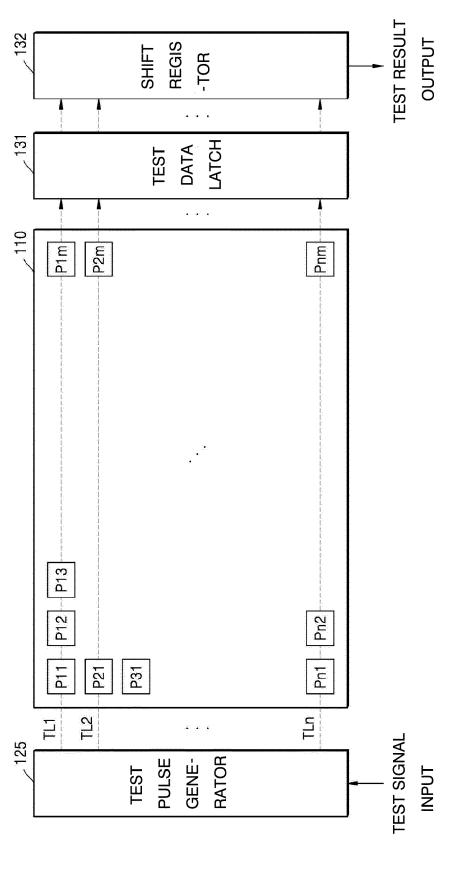


FIG. 11

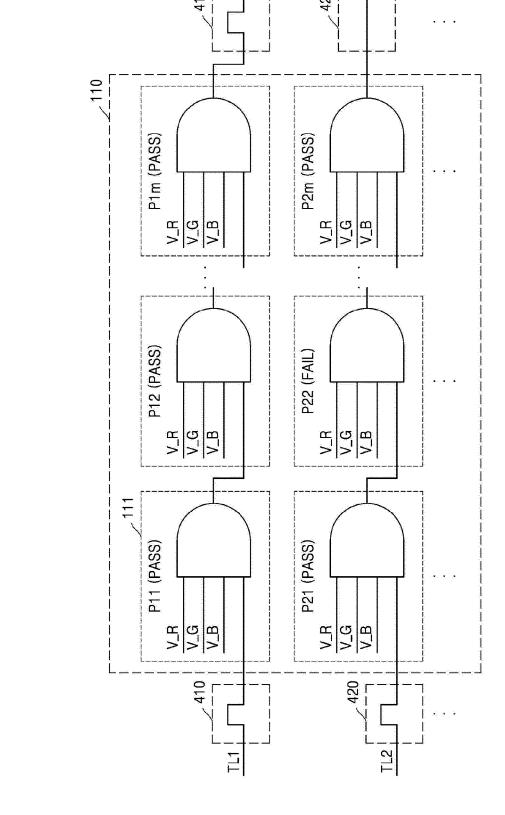


FIG. 12

FIG. 13a

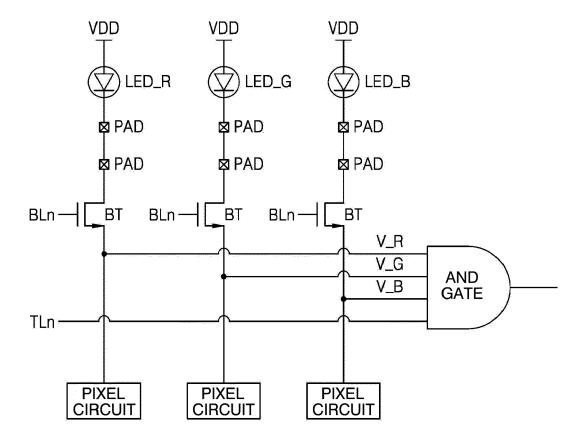


FIG. 13b

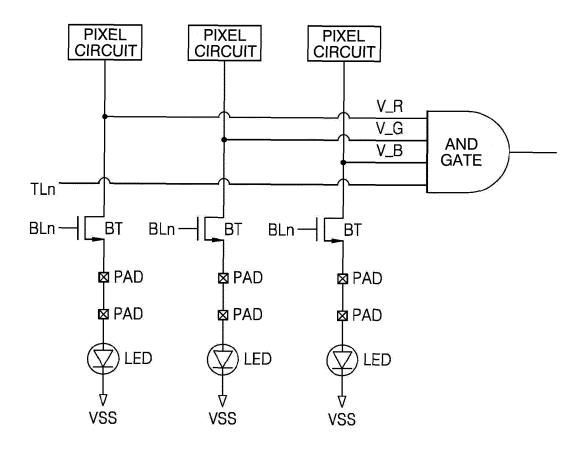


FIG. 14

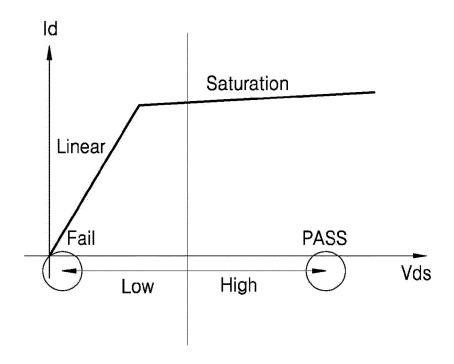
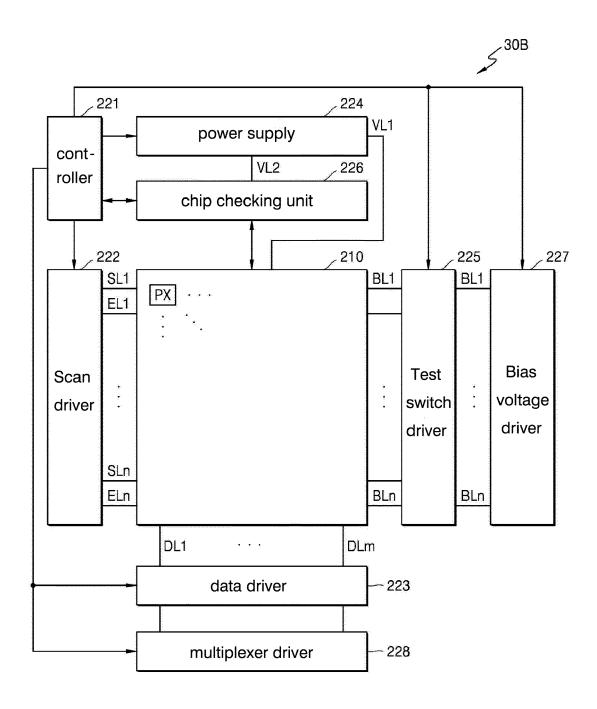
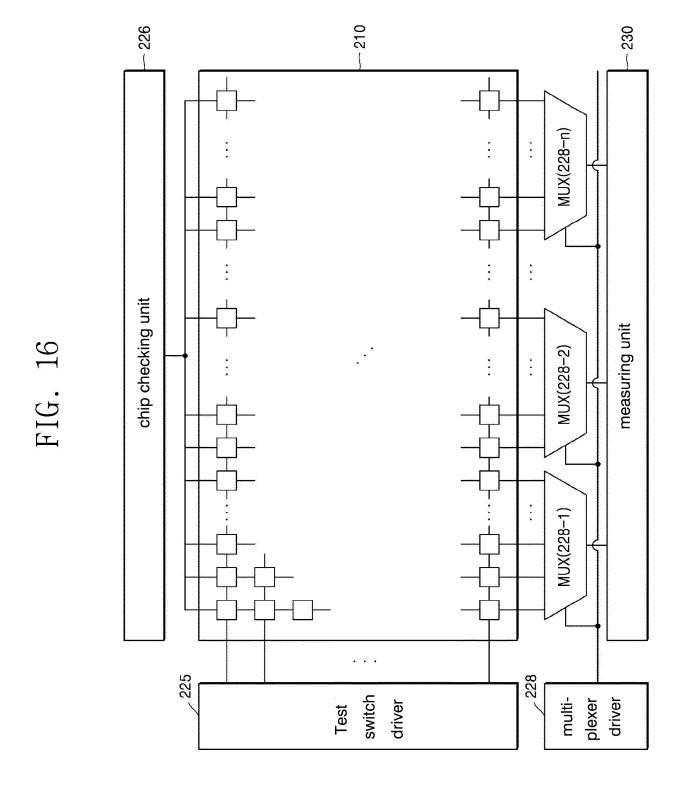


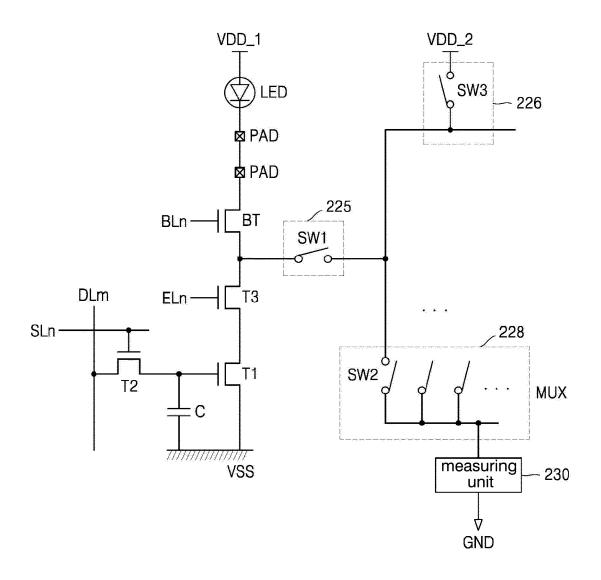
FIG. 15





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FIG. 17



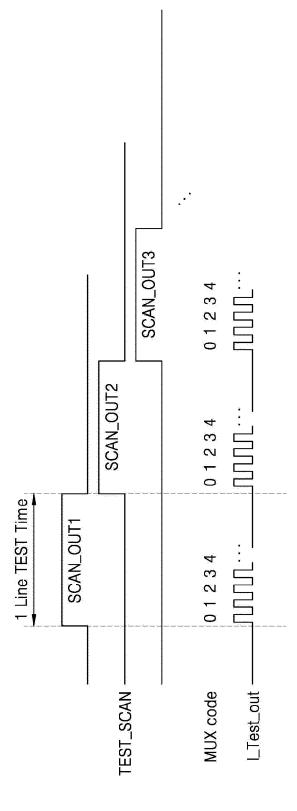


FIG. 18

FIG. 19

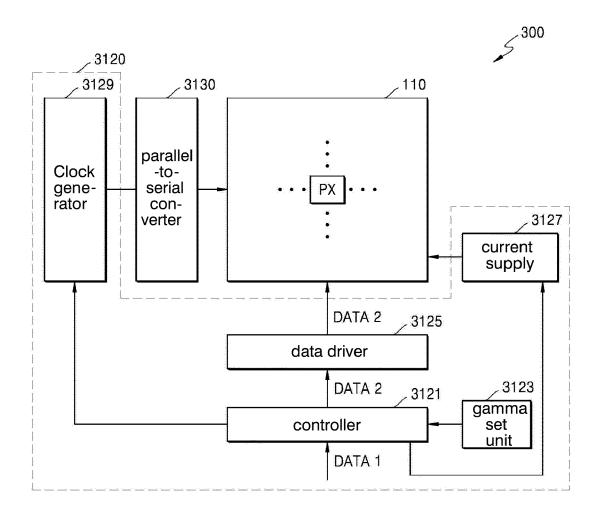
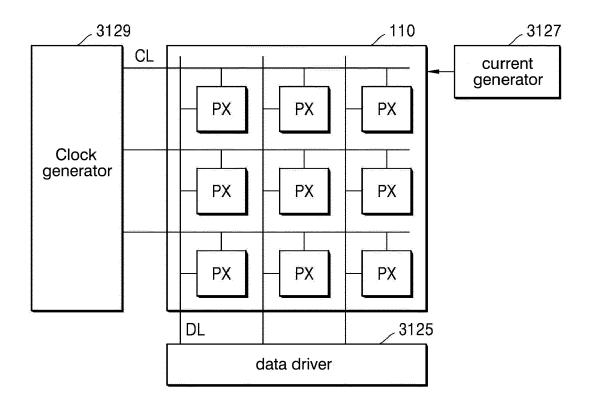


FIG. 20





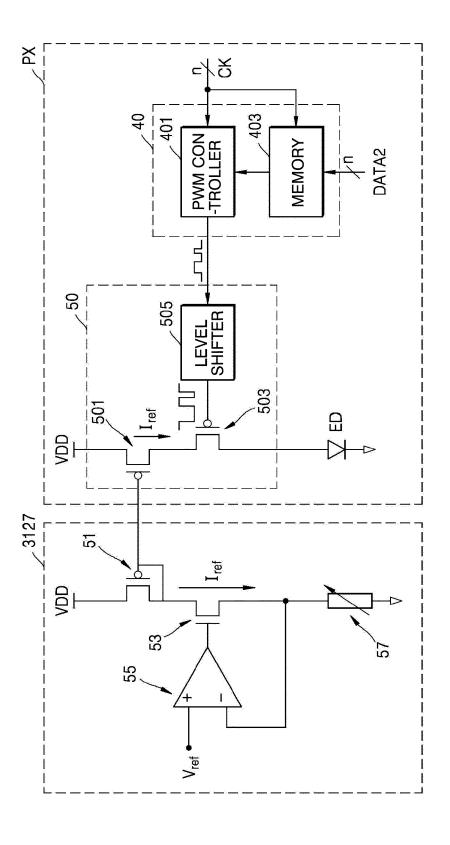


FIG. 22

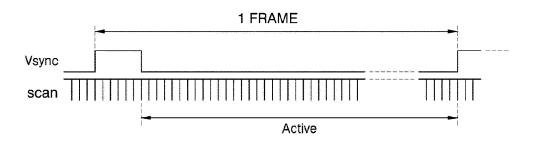
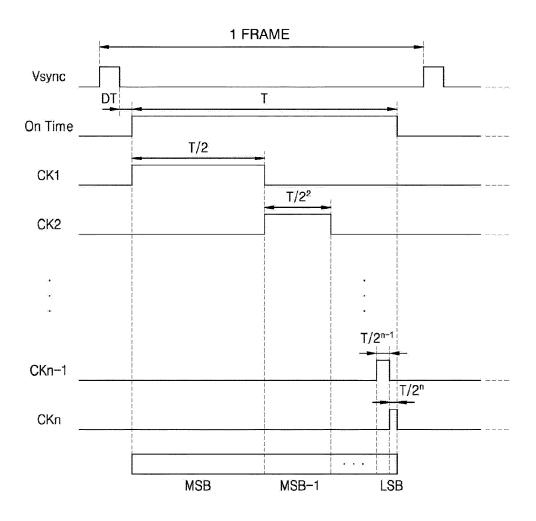


FIG. 23



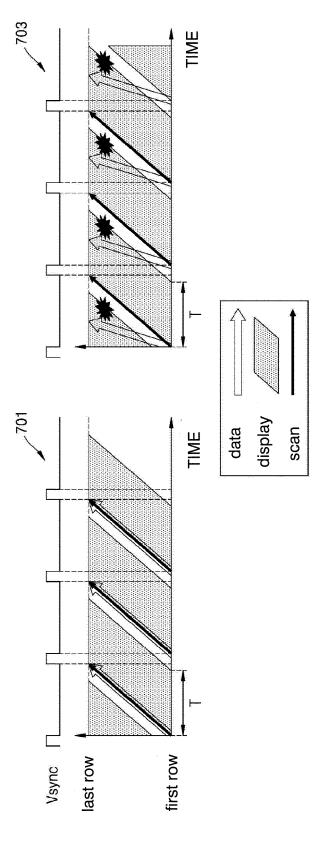


FIG. 24

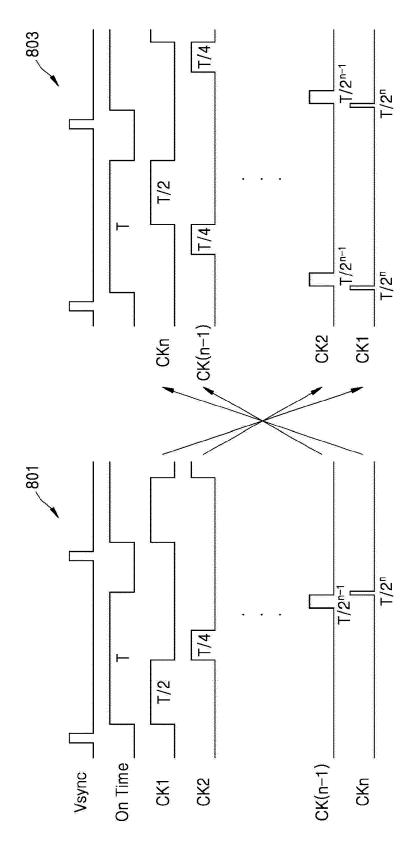
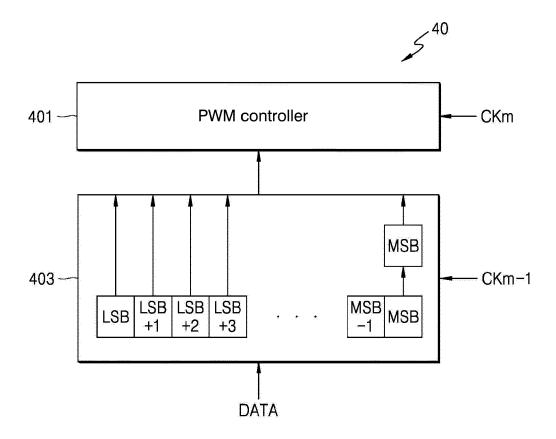


FIG. 25

FIG. 26



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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

KR 2020009942 W [0001]

• KR 1020190127865 [0001]