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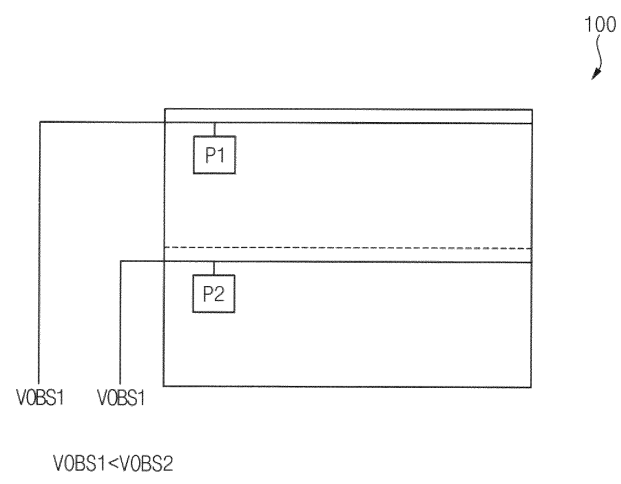
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(54) **DISPLAY DEVICE**

(57) A display device includes: a display panel including pixels; a data driver configured to output data voltages to the pixels; a gate driver configured to output a write gate signal to write the data voltages to the pixels having an inactivation level in a frame stop period; a timing controller configured to control the data driver and the gate driver; and a voltage generator configured to apply a first bias voltage to first pixels to which the data voltages are written before the frame stop period among the pixels, and to apply a second bias voltage to second pixels to which the data voltages are written after the frame stop period among the pixels.

FIG. 3



EP 4 328 897 A1

Description

BACKGROUND

1. Field

[0001] Aspects of the present inventive concept relate to a display device.

2. Description of the Related Art

[0002] Generally, a display device may include a display panel, a timing controller, gate driver, and a data driver. The display panel may include a plurality of gate lines, a plurality of data lines, and a plurality of pixels electrically connected to the gate lines and the data lines. The gate driver may provide gate signals to the gate lines. The data driver may provide data voltages to the data lines. The timing controller may control the gate driver and the data driver.

[0003] The display device may further include a touch panel for recognizing an input action or touch event by a user. When the touch panel is touched by a conductive object such as a finger or a stylus pen, the touch panel may generate an electrical signal to detect a presence and location of the touch. The touch panel may be mounted on an upper surface of a display panel such as an organic light emitting display panel or a liquid crystal display panel, or may be formed in a display panel, and may be divided into a resistive film method, a capacitive method, an electromagnetic field method, an infrared method, a surface acoustic wave (SAW) method, and a near field imaging (NFI) method, and the like.

[0004] For a touch sensing operation for sensing a touch, the display device may have a frame stop period between display operation for displaying images, and may perform the touch sensing operation in the frame stop period. However, in one frame, a difference in luminance may occur before and after the frame stop period.

[0005] The above information disclosed in this Background section is only for enhancement of understanding of the background and therefore the information discussed in this Background section does not necessarily constitute prior art.

SUMMARY

[0006] The present invention is defined by the independent claims. The present inventive concept relates to a display device having a frame stop period.

[0007] Aspects of some embodiments of the present inventive concept include a display device that may minimize or reduce a difference in luminance occurring before and after a frame stop period.

[0008] According to a first aspect of the present inventive concept, a display device includes a display panel including pixels, a data driver configured to output data voltages to the pixels, a gate driver configured to output

a write gate signal for writing the data voltages to the pixels having an inactivation level in a frame stop period, a timing controller configured to control the data driver and the gate driver, and a voltage generator configured to apply a first bias voltage to first pixels to which the data voltages are written before the frame stop period among the pixels, and to apply a second bias voltage to second pixels to which the data voltages are written after the frame stop period among the pixels.

[0009] According to some embodiments, the second bias voltage may be smaller than the first bias voltage.

[0010] According to some embodiments, each of the pixels may include a driving transistor, the gate driver is configured to output a bias gate signal to the pixels, the first bias voltage may be applied to the driving transistor of each of the first pixels in response to the bias gate signal, and the second bias voltage may be applied to the driving transistor of each of the second pixels in response to the bias gate signal.

[0011] According to some embodiments, the bias gate signal may have an inactivation level in the frame stop period.

[0012] According to some embodiments, the display device may further include an emission driver configured to output an emission signal for emitting the pixels to the pixels, and the timing controller may be configured to maintain an output of the emission signal in the frame stop period.

[0013] According to some embodiments, the timing controller may be configured to maintain an output of the bias gate signal in the frame stop period, and a time between an activation timing of the bias gate signal and an activation timing of the emission signal may be constant.

[0014] According to some embodiments, the voltage generator may be configured to apply a first gate initialization voltage to the first pixels and to apply a second gate initialization voltage to the second pixels, each of the pixels may include a driving transistor, the gate driver may be configured to output an initialization gate signal to the pixels, the first gate initialization voltage may be applied to a control electrode of the driving transistor of each of the first pixels in response to the initialization gate signal, and the second gate initialization voltage may be applied to the control electrode of the driving transistor of each of the second pixels in response to the initialization gate signal.

[0015] According to some embodiments, the second gate initialization voltage may be greater than the first gate initialization voltage.

[0016] According to some embodiments, the initialization gate signal may have an inactivation level in the frame stop period.

[0017] According to some embodiments, the voltage generator may be configured to apply a first anode initialization voltage to the first pixels and to apply a second anode initialization voltage to the second pixels, each of the pixels may include a light emitting element, the gate driver may be configured to output a bias gate signal to

the pixels, the first anode initialization voltage may be applied to the light emitting element of each of the first pixels in response to the bias gate signal, and the second anode initialization voltage may be applied to the light emitting element of each of the second pixels in response to the bias gate signal.

[0018] According to some embodiments, the second anode initialization voltage may be smaller than the first anode initialization voltage.

[0019] According to some embodiments, the timing controller may be configured to perform a touch sensing operation in the frame stop period.

[0020] According to a second aspect of the present inventive concept, a display device includes a display panel including pixels, a data driver configured to output data voltages to the pixels, a gate driver configured to output a write gate signal for writing the data voltages to the pixels having an inactivation level in a frame stop period, a timing controller configured to control the data driver and the gate driver, and a voltage generator configured to apply a bias voltage to the pixels and to vary the bias voltage after the frame stop period.

[0021] According to some embodiments, the voltage generator may be configured to decrease the bias voltage after the frame stop period.

[0022] According to some embodiments, the voltage generator may be configured to apply a gate initialization voltage to the pixels, and to vary the gate initialization voltage after the frame stop period, each of the pixels may include a driving transistor, the gate driver may be configured to output an initialization gate signal to the pixels, and the gate initialization voltage may be applied to a control electrode of the driving transistor of each of the pixels in response to the initialization gate signal.

[0023] According to some embodiments, the voltage generator may be configured to increase the gate initialization voltage after the frame stop period.

[0024] According to some embodiments, the voltage generator may be configured to apply an anode initialization voltage to the pixels, and to vary the anode initialization voltage after the frame stop period, each of the pixels may include a light emitting element, the gate driver may be configured to output a bias gate signal to the pixels, and the anode initialization voltage may be applied to the light emitting element of each of the pixels in response to the bias gate signal.

[0025] According to some embodiments, the voltage generator may be configured to decrease the anode initialization voltage after the frame stop period.

[0026] According to a third aspect of the present inventive concept, a display device includes a display panel including pixels, a data driver configured to output data voltages to the pixels, a gate driver configured to output a write gate signal for writing the data voltages to the pixels having an inactivation level in a frame stop period and to output a bias gate signal for applying a bias voltage to a driving transistor included in each of the pixels having an activation level, an emission driver configured to out-

put an emission signal for emitting the pixels to the pixels, a timing controller configured to control the data driver, the gate driver, and the emission driver, and a voltage generator configured to apply the bias voltage to the pixels.

[0027] According to some embodiments, a time between an activation timing of the bias gate signal and an activation timing of the emission signal may be constant.

[0028] Therefore, the display device according to some embodiments may compensate for an insufficient bias time of second pixels compared to first pixels by applying a first bias voltage to the first pixels to which data voltages are written before a frame stop period among pixels and applying a second bias voltage to second pixels to which the data voltages are written after the frame stop period among the pixels. Accordingly, the display device may minimize or reduce a difference in luminance occurring before and after the frame stop period.

[0029] In addition, the display device may minimize or reduce a difference in luminance occurring before and after the frame stop period by applying a first gate initialization voltage to first pixels and a second gate initialization voltage to second pixels.

[0030] Further, the display device may compensate for an insufficient anode initialization time of second pixels compared to first pixels by applying a first anode initialization voltage to first pixels and a second anode initialization voltage to second pixels. Accordingly, the display device may minimize or reduce a difference in luminance occurring before and after the frame stop period.

[0031] Also, the display device may have the same bias time for first pixel and second pixel by outputting a write gate signal for writing data voltages to pixels having an inactivation level in a frame stop period, outputting a bias gate signal for applying a bias voltage to a driving transistor included in each of the pixels having an activation level, and outputting an emission signal for emitting the pixels to the pixels. Accordingly, the display device may minimize or reduce a difference in luminance occurring before and after the frame stop period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

FIG. 1 is a block diagram illustrating a display device according to some embodiments of the present inventive concept.

FIG. 2 is a circuit diagram illustrating an example of pixels of the display device of FIG. 1.

FIG. 3 is a block diagram illustrating an example of a first pixel and a second pixel of the display device of FIG. 1.

FIG. 4 is a timing diagram illustrating an example in which the display device of FIG. 1 is driven in one frame.

FIG. 5 is a circuit diagram illustrating an example of pixels P of a display device according to some em-

bodiments of the present inventive concept.

FIG. 6 is a diagram illustrating an example of a bias voltage of the display device of FIG. 5.

FIG. 7 is a circuit diagram illustrating an example of pixels of a display device according to some embodiments of the present inventive concept.

FIG. 8 is a block diagram illustrating an example of first pixels and second pixels of the display device of FIG. 7.

FIG. 9 is a diagram illustrating an example of a gate initialization voltage of a display device according to some embodiments of the present inventive concept.

FIG. 10 is a circuit diagram illustrating an example of pixels of a display device according to some embodiments of the present inventive concept.

FIG. 11 is a block diagram illustrating an example of first pixels and second pixels of the display device of FIG. 10.

FIG. 12 is a diagram illustrating an example of an anode initialization voltage of a display device according to some embodiments of the present inventive concept.

FIG. 13 is a timing diagram illustrating an example in which a display device according to some embodiments of the present inventive concept is driven in one frame.

FIG. 14 is a block diagram showing an electronic device according to some embodiments of the present inventive concept.

FIG. 15 is a diagram showing an example in which the electronic device of FIG. 14 is implemented as a smart phone.

DETAILED DESCRIPTION

[0033] Hereinafter, aspects of some embodiments of the present inventive concept will be explained in more detail with reference to the accompanying drawings.

[0034] FIG. 1 is a block diagram illustrating a display device according to some embodiments of the present inventive concept.

[0035] Referring to FIG. 1, the display device includes a display panel 100, a timing controller 200, a gate driver 300, a data driver 400, an emission driver 500, and a voltage generator 600. According to some embodiments, the timing controller 200 and the data driver 400 may be integrated into one chip.

[0036] The display panel 100 has a display region AA on which an image is displayed and a peripheral region PA adjacent to the display region AA. According to some embodiments, the gate driver 300 and the emission driver 500 may be mounted on the peripheral region PA of the display panel 100.

[0037] The display panel 100 may include a plurality of gate lines GL, a plurality of data lines DL, a plurality of emission lines EL, and a plurality of pixels P electrically connected to the data lines DL, the gate lines GL, and

the emission lines EL. The gate lines GL and the emission lines EL may extend in a first direction D1 and the data lines DL may extend in a second direction D2 crossing the first direction D1.

[0038] The timing controller 200 may receive input image data IMG and an input control signal CONT from a host processor (e.g., a graphic processing unit; GPU). For example, the input image data IMG may include red image data, green image data and blue image data. According to some embodiments, the input image data IMG may further include white image data. For another example, the input image data IMG may include magenta image data, yellow image data, and cyan image data. The input control signal CONT may include a master clock signal and a data enable signal. The input control signal CONT may further include a vertical synchronizing signal and a horizontal synchronizing signal.

[0039] The timing controller 200 may generate a first control signal CONT1, a second control signal CONT2, a third control signal CONT3, and data signal DATA based on the input image data IMG and the input control signal CONT.

[0040] The timing controller 200 may generate the first control signal CONT1 for controlling operation of the gate driver 300 based on the input control signal CONT and output the first control signal CONT1 to the gate driver 300. The first control signal CONT1 may include a vertical start signal and a gate clock signal.

[0041] The timing controller 200 may generate the second control signal CONT2 for controlling operation of the data driver 400 based on the input control signal CONT and output the second control signal CONT2 to the data driver 400. The second control signal CONT2 may include a horizontal start signal and a load signal.

[0042] The timing controller 200 may generate the third control signal CONT3 for controlling operation of the emission driver 500 based on the input control signal CONT and output the third control signal CONT3 to the emission driver 500. The third control signal CONT3 may include a vertical start signal and an emission clock signal.

[0043] The timing controller 200 may receive the input image data IMG and the input control signal CONT, and generate the data signal DATA. The timing controller 200 may output the data signal DATA to the data driver 400.

[0044] The gate driver 300 may generate gate signals for driving the gate lines GL in response to the first control signal CONT1 input from the timing controller 200. The gate driver 300 may output the gate signals to the gate lines GL. For example, the gate driver 300 may sequentially output the gate signals to the gate lines GL.

[0045] The data driver 400 may receive the second control signal CONT2 and the data signal DATA from the timing controller 200. The data driver 400 may convert the data signal DATA into data voltages having an analog type. The data driver 400 may output the data voltage to the data lines DL.

[0046] The emission driver 500 may generate gate sig-

nals for driving the emission lines EL in response to the third control signal CONT3 input from the timing controller 200. The emission driver 500 may output the emission signals to the emission lines EL. For example, the emission driver 500 may sequentially output the emission signals to the emission lines EL.

[0047] The voltage generator 600 may generate a first bias voltage VOBS1 and a second bias voltage VOBS2. The voltage generator 600 may output the first bias voltage VOBS1 and the second bias voltage VOBS2 to the display panel 100. For example, the voltage generator 600 may output the first bias voltage VOBS1 and the second bias voltage VOBS2 to the pixels P.

[0048] FIG. 2 is a circuit diagram illustrating an example of the pixels P of the display device of FIG. 1.

[0049] Referring to FIGS. 1 and 2, the gate driver 300 may output a write gate signal GW for writing the data voltages VDATA to the pixels P. The emission driver 500 may output the emission signal EM for emitting the pixels P.

[0050] Each of the pixels P may include a first transistor T1 (i.e., a driving transistor T1) including a control electrode connected to a first node N1, a first electrode connected to a second node N2, and a second electrode connected to a third node N3, a second transistor T2 including a control electrode receiving the write gate signal GW, a first electrode receiving the data voltage VDATA, and a second electrode connected to the second node N2, a third transistor T3 including a control electrode receiving a compensation gate signal GC, a first electrode connected to the third node N3, and a second electrode connected to the first node N1, a fourth transistor T4 including a control electrode receiving an initialization gate signal GI, a first electrode receiving a gate initialization voltage VINT, and a second electrode connected to the first node N1, a fifth transistor T5 including a control electrode receiving the emission signal EM, a first electrode receiving a first power voltage ELVDD (e.g., a high power voltage), and a second electrode connected to the second node N2, a sixth transistor T6 including a control electrode receiving the emission signal EM, a first electrode connected to the third node N3, and a second electrode connected to a fourth node N4, a seventh transistor T7 including a control electrode receiving a bias gate signal GB, a first electrode receiving an anode initialization voltage VAINIT, and a second electrode connected to the fourth node N4, an eighth transistor T8 including a control electrode receiving the bias gate signal GB, a first electrode receiving the first bias voltage VOBS1 or the second bias voltage VOBS2, and a second electrode connected to the second node N2, a storage capacitor CST including a first electrode receiving the first power voltage ELVDD and a second electrode connected to the first node N1, and a light emitting element EE including a first electrode connected to the fourth node N4 and a second electrode receiving a second power voltage ELVSS (e.g., a low power voltage). However, embodiments according to the present inventive concept are not

limited thereto. For example, each of the pixels P may have a 3T1C structure composed of 3 transistors and 1 capacitor, a 5T2C structure composed of 5 transistors and 2 capacitors, a 7T1C structure composed of 7 transistors and 1 capacitor, etc., and a bias transistor for applying a bias voltage (e.g., VOBS1, VOBS2) to the driving transistor T1 (e.g., the eighth transistor T8). The circuit of each of the pixels P may include additional components or fewer components without departing from the scope of embodiments according to the present disclosure.

[0051] According to some embodiments, the driving transistor T1 may further include a lower electrode. For example, the lower electrode of the driving transistor T1 may be connected to the first electrode of the driving transistor T1.

[0052] The first, second, and fifth to eighth transistors T1, T2, T5, T6, T7, and T8 may be implemented as p-channel metal oxide semiconductor (PMOS) transistors. In this case, a low voltage level may be an activation level, and a high voltage level may be an inactivation level. For example, when a signal applied to a control electrode of the PMOS transistor has the low voltage level, the PMOS transistor may be turned on. For example, when a signal applied to the control electrode of the PMOS transistor has the high voltage level, the PMOS transistor may be turned off.

[0053] The third and fourth transistors T3 and T4 may be implemented as n-channel metal oxide semiconductor (NMOS) transistors. In this case, the low voltage level may be an inactivation level, and the high voltage level may be an activation level. For example, when a signal applied to a control electrode of the NMOS transistor has the low voltage level, the NMOS transistor may be turned off. For example, when a signal applied to the control electrode of the NMOS transistor has the high voltage level, the NMOS transistor may be turned on.

[0054] However, embodiments according to the present inventive concept are not limited thereto. For example, the first, second, and fifth to eighth transistors T1, T2, T5, T6, T7, and T8 may be NMOS transistors. For example, the third and fourth transistors T3 and T4 may be PMOS transistors.

[0055] For example, in an initialization period, the initialization gate signal GI may have the activation level, and the fourth transistor T4 may be turned on. Accordingly, the gate initialization voltage VINT may be applied to the control electrode (i.e., the first node N1) of the driving transistor T1 (i.e., a gate initialization operation). That is, the control electrode of the driving transistor T1 (i.e., the data voltage VDATA written to the storage capacitor CST) may be initialized.

[0056] For example, in a data writing period, the write gate signal GW and the compensation gate signal GC may have the activation level, and the second transistor T2 and the third transistor T3 may be turned on. Accordingly, the data voltage VDATA may be written to the stor-

age capacitor CST (i.e., a data write operation).

[0057] For example, in a bias period, the bias gate signal GB may have the activation level, and the seventh transistor T7 and the eighth transistor T8 may be turned on. Accordingly, the anode initialization voltage VAINT may be applied to the first electrode (i.e., an anode electrode) of the light emitting element EE (i.e., an anode initialization operation), and the first bias voltage VOBS1 or the second bias voltage VOBS2 may be applied to the first electrode of the driving transistor T1 (i.e., a bias operation). That is, the anode electrode of the light emitting element EE may be initialized, and a bias of the driving transistor T1 may be on-bias.

[0058] For example, in a light emitting period, the emission signal EM may have the activation level, and the fifth transistor T5 and the sixth transistor T6 may be turned on. Accordingly, the first power voltage ELVDD may be applied to the driving transistor T1 to generate a driving current, and the driving current may be applied to the light emitting element EE (i.e., a light emission operation). That is, the light emitting element EE may emit light with a luminance corresponding to the driving current.

[0059] FIG. 3 is a block diagram illustrating an example of a first pixel P1 and a second pixel P1 of the display device of FIG. 1, and FIG. 4 is a timing diagram illustrating an example in which the display device of FIG. 1 is driven in one frame. FIG. 4 illustrates the activation levels of the emission signal EM, the write gate signal GW, and the bias gate signal GB as the low voltage level, and the activation level of the initialization gate signal GI as the high voltage level.

[0060] Referring to FIGS. 1 to 4, FIG. 4 illustrates that the emission signal EM is sequentially applied to Nth to N+6th emission lines EL (e.g., EM[N], EM[N+1], ..., EM[N+6]). FIG. 4 illustrates that the write gate signal GW is sequentially applied to Nth to N+6th gate lines GL (e.g., GW[N], GW[N+1], ..., GW[N+6]). FIG. 4 illustrates that the bias gate signal GB is sequentially applied to Nth to N+6th gate lines GL (e.g., GB[N], GB[N+1], ..., GB[N+6]). Here, N is a positive integer.

[0061] The gate driver 300 may output the write gate signal GW having the inactivation level in the frame stop period IFP. For example, the timing controller 200 may temporarily suspend output of the write gate signal GW in the frame stop period IFP. The gate driver 300 may output the bias gate signal GB having the inactivation level in the frame stop period IFP. For example, the timing controller 200 may temporarily suspend output of the bias gate signal GB in the frame stop period IFP. The gate driver 300 may output the initialization gate signal GI having the inactivation level in the frame stop period IFP. For example, the timing controller 200 may temporarily suspend output of the initialization gate signal GI in the frame stop period IFP. The emission driver 500 may output the emission signal EM having the activation level in the frame stop period IFP. For example, the timing controller 200 may maintain output of the emission signal EM in

the frame stop period IFP. The timing controller 200 may perform a touch sensing operation in the frame stop period IFP.

[0062] For example, the gate initialization operation, the data writing operation, the anode initialization operation, and the bias operation may be sequentially performed up to a N+2th pixel row. Thereafter, in the frame stop period IFP, the timing controller 200 may stop the gate initialization operation, the data writing operation, the anode initialization operation, and the bias operation, and may perform the touch sensing operation. After the frame stop period IFP ends, the gate initialization operation, the data writing operation, the anode initialization operation, and the bias operation may be sequentially performed from a N+3th pixel row. On the other hand, the light emission operation may be performed regardless of the frame stop period IFP. That is, the emission signal EM may be sequentially output regardless of the frame stop period IFP.

[0063] The pixel row may include pixels P connected to one gate line GL and one emission line EL. For example, the timing controller 200 may sequentially drive the pixel rows.

[0064] The display device may further include a touch panel for recognizing an input action or event by a user. The display device may recognize a touch when there is the input action or event by the user on the touch panel (i.e., the touch sensing operation). When the display device simultaneously performs the touch sensing operation and a display operation (i.e., operations for displaying an image, such as the gate initialization operation, the data writing operation, the bias operation, the anode initialization operation, and the light emission operation), Each operation may affect other operation. Accordingly, the display device may have the frame stop period IFP and may perform the touch sensing operation in the frame stop period IFP. In addition, by separating the touch sensing operation and the display operation, the touch sensing operation and the display operation may operate at different frequencies.

[0065] The voltage generator 600 may apply the first bias voltage VOBS1 to the first pixels P1 to which the data voltages VDATA are written before the frame stop period IFP among the pixels P, and the second bias voltage VOBS2 may be applied to the second pixels P2 in which the data voltages VDATA are written after the frame stop period IFP among the pixels P. For example, the first bias voltage VOBS1 may be applied to the driving transistor T1 of each of the first pixels P1 in response to the bias gate signal GB. For example, the second bias voltage VOBS2 may be applied to the driving transistor T1 of each of the second pixels P2 in response to the bias gate signal GB. The second bias voltage VOBS2 may be smaller than the first bias voltage VOBS1.

[0066] For example, the first pixels P1 may be pixels P to which the write gate signal GW having the activation level is applied before the frame stop period IFP in one frame. For example, the second pixels P2 may be pixels

P to which the write gate signal GW having the activation level is applied after the frame stop period IFP in one frame.

[0067] For example, as shown in FIG. 3, the voltage generator 600 may apply the first bias voltage VOBS1 and the second bias voltage VOBS2 to the first pixels P1 and the second pixels P2 through separate voltage lines. Accordingly, the first bias voltage VOBS1 may be applied only to the first pixels P1, and the second bias voltage VOBS2 may be applied only to the second pixels P2.

[0068] As shown in FIG. 4, a bias time of the second pixels P2 may be shorter than a bias time of the first pixels P1. The bias time may be a time after the bias operation is performed until the light emission operation is performed. For example, the bias time may be a time from when the bias gate signal GB becomes the activation level until the emission signal EM becomes the activation level.

[0069] That is, if the first bias voltage VOBS1 and the second bias voltage VOBS2 are the same, which may be also called as a bias voltage VOBS, a difference in luminance may be generated between the first pixels P1 and the second pixels P2 due to the difference in the bias time. However, because the second bias voltage VOBS2 smaller than the first bias voltage VOBS1 is applied to the second pixels P2, the bias of the second pixels P2 may be quickly turned on-bias. Accordingly, the display device may compensate for the insufficient bias time of the second pixel P2 compared to the first pixel P1. Accordingly, the display device may minimize or reduce the difference in luminance occurring before and after the frame stop period IFP.

[0070] FIG. 5 is a circuit diagram illustrating an example of the pixels P of a display device according to some embodiments of the present inventive concept, and FIG. 6 is a diagram illustrating an example of a bias voltage VOBS of the display device of FIG. 5. The bias voltage VOBS may include the first bias voltage VOBS1 and the second bias voltage VOBS2.

[0071] The display device according to some embodiments is substantially the same as the display device of FIG. 1 except for the bias voltage VOBS. Thus, the same reference numerals are used to refer to the same or similar element, and any repetitive explanation will be omitted.

[0072] Referring to FIGS. 1, 5, and 6, the voltage generator 600 may apply the bias voltage VOBS to the pixels P, which may include first pixels P1 and second pixels P2, and vary the bias voltage VOBS after the frame stop period IFP. However, the present inventive concept is not limited thereto. For example, the present inventive concept may vary the bias voltage VOBS when the frame stop period IFP starts.

[0073] Each of the pixels P may include an eighth transistor T8 including a control electrode receiving the bias gate signal GB, a first electrode receiving the bias voltage VOBS, and a second electrode connected to the second node N2.

[0074] For example, in a bias period, the bias gate signal GB may have the activation level, and the seventh transistor T7 and the eighth transistor T8 may be turned on. Accordingly, the anode initialization voltage VATIN may be applied to the first electrode (i.e., the anode electrode) of the light emitting element EE (i.e., the anode initialization operation), and the bias voltage VOBS may be applied to the first electrode of the driving transistor T1 (i.e., the bias operation). That is, the anode electrode of the light emitting element EE may be initialized, and the bias of the driving transistor T1 may be on-bias.

[0075] The voltage generator 600 may decrease the bias voltage VOBS after the frame stop period IFP. That is, the bias voltage VOBS applied after the frame stop period IFP may be smaller than the bias voltage VOBS applied before the frame stop period IFP.

[0076] If the bias voltage VOBS is the same before and after the frame stop period IFP, the difference in the luminance may occur between the first pixels P1 and the second pixels P2 due to the difference in the bias time. However, by reducing the bias voltage VOBS after the frame stop period IFP, the bias of the second pixels P2 may be quickly turned on-bias. Accordingly, the display device may compensate for the insufficient bias time of the second pixel P2 compared to the first pixel P1. Accordingly, the display device may minimize or reduce the difference in luminance occurring before and after the frame stop period IFP.

[0077] FIG. 7 is a circuit diagram illustrating an example of the pixels P of a display device according to some embodiments of the present inventive concept, and FIG. 8 is a block diagram illustrating an example of the first pixels P1 and the second pixels P2 of the display device of FIG. 7.

[0078] The display device according to some embodiments is substantially the same as the display device of FIG. 1 except for the bias voltage VOBS and the gate initialization voltage VINT. Thus, the same reference numerals are used to refer to the same or similar element, and any repetitive explanation will be omitted.

[0079] Referring to FIGS. 1, 4, 7, and 8, each of the pixels P may include the fourth transistor T4 including a control electrode receiving the initialization gate signal GI, a first electrode receiving the first gate initialization voltage VINT1 or the second gate initialization voltage VINT2, and a second electrode connected to the first node N1, and a eighth transistor T8 including a control electrode receiving the bias gate signal GB, a first electrode receiving the bias voltage VOBS, and a second electrode connected to the second node N2.

[0080] For example, in the initialization period, the initialization gate signal GI may have the activation level, and the fourth transistor T4 may be turned on. Accordingly, the first gate initialization voltage VINT1 or the second gate initialization voltage VINT2 may be applied to the control electrode (i.e., the first node N1) of the driving transistor T1 (i.e., the gate initialization operation). That is, the control electrode of the driving transistor T1 (i.e.,

the data voltage VDATA written to the storage capacitor CST) may be initialized.

[0081] For example, in the bias period, the bias gate signal GB may have the activation level, and the seventh transistor T7 and the eighth transistor T8 may be turned on. Accordingly, the anode initialization voltage VATIN may be applied to the first electrode (i.e., the anode electrode) of the light emitting element EE (i.e., the anode initialization operation), and the bias voltage VOBS may be applied to the first electrode of the driving transistor T1 (i.e., the bias operation). That is, the anode electrode of the light emitting element EE may be initialized, and the bias of the driving transistor T1 may be on-bias.

[0082] The voltage generator 600 may apply the first gate initialization voltage VINT1 to the first pixels P1 to which the data voltages VDATA are written before the frame stop period IFP among the pixels P, and may apply the second gate initialization voltage VINT2 to the second pixels P2 in which the data voltages VDATA are written after the frame stop period IFP among the pixels P. For example, the first gate initialization voltage VINT1 may be applied to the control electrode of the driving transistor T1 of each of the first pixels P1 in response to the initialization gate signal GI. For example, the second gate initialization voltage VINT2 may be applied to the control electrode of the driving transistor T1 of each of the second pixels P2 in response to the initialization gate signal GI. The second gate initialization voltage VINT2 may be greater than the first gate initialization voltage VINT1.

[0083] For example, as shown in FIG. 8, the voltage generator 600 may provide the first gate initialization voltage VINT1 and the second gate initialization voltage VINT2 to the first pixels P1 and the second pixels P2 through separate voltage lines. Accordingly, the first gate initialization voltage VINT1 may be applied only to the first pixels P1, and the second gate initialization voltage VINT2 may be applied only to the second pixels P2.

[0084] If the first gate initialization voltage VINT1 and the second gate initialization voltage VINT2 are the same, the difference in luminance may occur between the first pixels P1 and the second pixels P2 due to the difference in the bias time. However, because the second gate initialization voltage VINT2 greater than the first gate initialization voltage VINT1 is applied to the second pixels P2, a voltage of the control electrode of the driving transistor T1 of the second pixels P2 may be increased. Accordingly, because the driving transistor T1 is the PMOS transistor, the driving current of the second pixels P2 may be smaller than the driving current of the first pixels P1. Accordingly, the display device may minimize or reduce the difference in luminance occurring before and after the frame stop period IFP.

[0085] FIG. 9 is a diagram illustrating an example of the gate initialization voltage VINT of a display device according to some embodiments of the present inventive concept.

[0086] The display device according to some embodiments is substantially the same as the display device of

FIG. 5 except for varying the gate initialization voltage VINT instead of the bias voltage VOBS. Thus, the same reference numerals are used to refer to the same or similar element, and any repetitive explanation will be omitted.

[0087] Referring to FIGS. 1, 5, and 9, the voltage generator 600 may apply the gate initialization voltage VINT to the pixels P, and may vary the gate initialization voltage VINT after the frame stop period IFP. However, embodiments according to the present inventive concept are not limited thereto. For example, according to some embodiments of the present inventive concept, the gate initialization voltage VINT may be varied when the frame stop period IFP starts.

[0088] The voltage generator 600 may increase the gate initialization voltage VINT after the frame stop period IFP. That is, the gate initialization voltage VINT applied after the frame stop period IFP may be greater than the gate initialization voltage VINT applied before the frame stop period IFP.

[0089] If the gate initialization voltage VINT is the same before and after the frame stop period IFP, the difference in luminance may occur between the first pixels P1 and the second pixels P2 due to the difference in the bias time. However, by increasing the gate initialization voltage VINT after the frame stop period IFP, the voltage of the control electrode of the driving transistor T1 of the second pixels P2 may be increased. Accordingly, because the driving transistor T1 is the PMOS transistor, the driving current of the second pixels P2 may be smaller than the driving current of the first pixels P1. So, the display device may minimize or reduce the difference in luminance occurring before and after the frame stop period IFP.

[0090] FIG. 10 is a circuit diagram illustrating an example of the pixels P of a display device according to some embodiments of the present inventive concept, and FIG. 11 is a block diagram illustrating an example of the first pixels P1 and the second pixels P2 of the display device of FIG. 10.

[0091] The display device according to some embodiments is substantially the same as the display device of FIG. 1 except for the bias voltage VOBS and the anode initialization voltage VAINT. Thus, the same reference numerals are used to refer to the same or similar element, and any repetitive explanation will be omitted.

[0092] Referring to FIGS. 1, 4, 10, and 11, each of the pixels P may include a fourth transistor T4 including a control electrode receiving the bias gate signal GB, a first electrode receiving the first anode initialization voltage VAINT1 or the second anode initialization voltage VAINT2, and a second electrode connected to the fourth node N4, and an eighth transistor T8 including a control electrode receiving the bias gate signal GB, a first electrode receiving the bias voltage VOBS, and a second electrode connected to the second node N2.

[0093] For example, in the bias period, the bias gate signal GB may have the activation level, and the seventh

transistor T7 and the eighth transistor T8 may be turned on. Accordingly, the first anode initialization voltage VATIN1 or the second anode initialization voltage VAINT2 may be applied to the first electrode (i.e., the anode electrode) of the light emitting element EE (i.e., the anode initialization operation), and the bias voltage VOBS may be applied to the first electrode of the driving transistor T1 (i.e., the bias operation). That is, the anode electrode of the light emitting element EE may be initialized, and the bias of the driving transistor T1 may be on-bias.

[0094] The voltage generator 600 may apply the first anode initialization voltage VAINT1 to the first pixels P1 in which the data voltages VDATA are written before the frame stop period IFP among the pixels P, and may apply the second anode initialization voltage VAINT2 to the second pixels P2 in which the data voltages VDATA are written after the frame stop period IFP among the pixels P. For example, the first anode initialization voltage VAINT1 may be applied to the light emitting element EE of each of the first pixels P1 in response to the bias gate signal GB. For example, the second anode initialization voltage VAINT2 may be applied to the light emitting element EE of each of the second pixels P2 in response to the bias gate signal GB. The second anode initialization voltage VAINT2 may be smaller than the first anode initialization voltage VAINT1.

[0095] For example, as shown in FIG. 11, the voltage generator 600 may provide the first anode initialization voltage VAINT1 and the second anode initialization voltage VAINT2 to the first pixels P1 and the second pixels P2 through separate voltage lines. Accordingly, the first anode initialization voltage VAINT1 may be applied only to the first pixels P1, and the second anode initialization voltage VAINT2 may be applied only to the second pixels P2.

[0096] As shown in FIG. 4, an anode initialization time of the second pixels P2 may be shorter than an anode initialization time of the first pixels P1. The anode initialization time may be a time from when the anode initialization operation is performed until the light emission operation is performed. For example, the anode initialization time may be a time from when the bias gate signal GB becomes the activation level until the emission signal EM becomes the activation level.

[0097] That is, if the first anode initialization voltage VAINT1 and the second anode initialization voltage VAINT2 are the same, the difference in luminance occurs between the first pixels P1 and the second pixels P2 due to the difference in the anode initialization time. However, because the second anode initialization voltage VAINT2 smaller than the first anode initialization voltage VAINT1 is applied to the second pixels P2, the second pixels P2 may be initialized quickly. Accordingly, the display device may compensate for the insufficient anode initialization time of the second pixel P2 compared to the first pixel P1. Accordingly, the display device may minimize or reduce the difference in luminance occurring before and

after the frame stop period IFP.

[0098] FIG. 12 is a diagram illustrating an example of the anode initialization voltage VAINT of a display device according to some embodiments of the present inventive concept.

[0099] The display device according to some embodiments is substantially the same as the display device of FIG. 5 except for varying the anode initialization voltage VAINT instead of the bias voltage VOBS. Thus, the same reference numerals are used to refer to the same or similar element, and any repetitive explanation will be omitted.

[0100] Referring to FIGS. 1, 5, and 12, the voltage generator 600 may apply the anode initialization voltage VAINT to the pixels P, and may vary the anode initialization voltage VAINT after the frame stop period IFP. However, the present inventive concept is not limited thereto. For example, the present inventive concept may vary the anode initialization voltage VAINT when the frame stop period IFP starts.

[0101] The voltage generator 600 may decrease the anode initialization voltage VAINT after the frame stop period IFP. That is, the anode initialization voltage VAINT applied after the frame stop period IFP may be smaller than the anode initialization voltage VAINT applied before the frame stop period IFP.

[0102] If the anode initialization voltage VAINT is the same before and after the frame stop period IFP, the difference in luminance may occur between the first pixels P1 and the second pixels P2 due to the difference in the anode initialization time. However, by reducing the anode initialization voltage VAINT after the frame stop period IFP, the second pixels P2 may be initialized quickly. Accordingly, the display device may compensate for the insufficient anode initialization time of the second pixel P2 compared to the first pixel P1. Accordingly, the display device may minimize or reduce the difference in luminance occurring before and after the frame stop period IFP.

[0103] FIG. 13 is a timing diagram illustrating an example in which a display device according to some embodiments of the present inventive concept is driven in one frame.

[0104] The display device according to some embodiments is substantially the same as the display device of FIG. 5 except for the bias gate signal GB and not varying the bias voltage VOBS. Thus, the same reference numerals are used to refer to the same or similar element, and any repetitive explanation will be omitted.

[0105] Referring to FIGS. 1, 5, and 13, FIG. 13 illustrates that the emission signal EM is sequentially applied to the Nth to N+6th emission lines EL (e.g., EM[N], EM[N+1], ..., EM[N+6]). FIG. 4 illustrates that the write gate signal GW is sequentially applied to the Nth to N+6th gate lines GL (e.g., GW[N], GW[N+1], ..., GW[N+6]). FIG. 4 illustrates that the bias gate signal GB is sequentially applied to the Nth to N+6th gate lines GL (e.g., GB[N], GB[N+1], ..., GB[N+6]).

[0106] The gate driver 300 may output the write gate signal GW having the inactivation level in the frame stop period IFP and output the bias gate signal GB having the activation level in the frame stop period IFP. The emission driver 500 may output the emission signal EM having the activation level. For example, the timing controller 200 temporarily suspends output of the write gate signal GW in the frame stop period IFP, may maintain the output of the bias gate signal GB in the frame stop period IFP, and may maintain the output of the emission signal EM in the frame stop period IFP.

[0107] For example, the gate initialization operation and the data writing operation may be sequentially performed up to the N+2th pixel row. Thereafter, in the frame stop period IFP, the timing controller 200 may stop the gate initialization operation and the data writing operation, and may perform the touch sensing operation. After the frame stop period IFP ends, the gate initialization operation and the data writing operation may be sequentially performed from the N+3th pixel row. On the other hand, the anode initialization operation, the bias operation, and the light emission operation may be performed regardless of the frame stop period IFP. That is, the bias gate signal GB and the emission signal EM may be sequentially output regardless of the frame stop period IFP.

[0108] A time between an activation timing of the bias gate signal GB and an activation timing of the emission signal EM may be constant. Consequently, the display device may have the same anode initialization time and the same bias time of the first pixels P1 and the second pixels P2. That is, in the display device, the anode initialization time and the bias time of all pixels P may be the same. Accordingly, the display device may minimize or reduce the difference in luminance occurring before and after the frame stop period IFP.

[0109] FIGS. 1 to 13 illustrates embodiments in which the difference in luminance is minimized or reduced through the bias voltage VOBS (or, the first bias voltage VOBS1 and the second bias voltage VOBS2), the gate initialization voltage VINT (or, the first gate initialization voltage VINT1 and the second gate initialization voltage VINT2), the anode initialization voltage VAINT (or, the first anode initialization voltage VAINT1 and the second anode initialization voltage VAINT2), or the bias gate signal GB. However, the present inventive concept is not limited thereto. For example, the display device may minimize or reduce the difference in luminance by using a combination of the above embodiments.

[0110] FIG. 14 is a block diagram showing an electronic device according to some embodiments of the present inventive concept, and FIG. 15 is a diagram showing an example in which the electronic device of FIG. 14 is implemented as a smart phone.

[0111] Referring to FIGS. 14 and 15, the electronic device 2000 may include a processor 2010, a memory device 2020, a storage device 2030, an input/output (I/O) device 2040, a power supply 2050, and a display device 2060. Here, the display device 2060 may be the display

device of FIG. 1. In addition, the electronic device 2000 may further include a plurality of ports for communicating with a video card, a sound card, a memory card, a universal serial bus (USB) device, other electronic devices, etc. According to some embodiments, as shown in FIG. 15, the electronic device 2000 may be implemented as a smart phone. However, the electronic device 2000 is not limited thereto. For example, the electronic device 2000 may be implemented as a cellular phone, a video phone, a smart pad, a smart watch, a tablet PC, a car navigation system, a computer monitor, a laptop, a head mounted display (HMD) device, etc.

[0112] The processor 2010 may perform various computing functions. The processor 2010 may be a micro processor, a central processing unit (CPU), an application processor (AP), etc. The processor 2010 may be coupled to other components via an address bus, a control bus, a data bus, etc. Further, the processor 2010 may be coupled to an extended bus such as a peripheral component interconnection (PCI) bus.

[0113] The memory device 2020 may store data for operations of the electronic device 2000. For example, the memory device 2020 may include at least one non-volatile memory device such as an erasable programmable read-only memory (EPROM) device, an electrically erasable programmable read-only memory (EEPROM) device, a flash memory device, a phase change random access memory (PRAM) device, a resistance random access memory (RRAM) device, a nano floating gate memory (NFGM) device, a polymer random access memory (PoRAM) device, a magnetic random access memory (MRAM) device, a ferroelectric random access memory (FRAM) device, etc and/or at least one volatile memory device such as a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a mobile DRAM device, etc.

[0114] The storage device 2030 may include a solid state drive (SSD) device, a hard disk drive (HDD) device, a CD-ROM device, etc.

[0115] The I/O device 2040 may include an input device such as a keyboard, a keypad, a mouse device, a touch pad, a touch screen, etc, and an output device such as a printer, a speaker, etc. In some embodiments, the I/O device 2040 may include the display device 2060.

[0116] The power supply 2050 may provide power for operations of the electronic device 2000. For example, the power supply 2050 may be a power management integrated circuit (PMIC).

[0117] The display device 2060 may display an image corresponding to visual information of the electronic device 2000. For example, the display device 2060 may be an organic light emitting display device or a quantum dot light emitting display device, but is not limited thereto. The display device 2060 may be coupled to other components via the buses or other communication links. Here, the display device 2060 may compensate for the insufficient bias time of the second pixels compared to the first pixels. Accordingly, the display device may min-

imize or reduce the difference in luminance occurring before and after the frame stop period.

[0118] The inventive concepts may be applied to any electronic device including the display device. For example, the inventive concepts may be applied to a television (TV), a digital TV, a 3D TV, a mobile phone, a smart phone, a tablet computer, a virtual reality (VR) device, a wearable electronic device, a personal computer (PC), a home appliance, a laptop computer, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera, a music player, a portable game console, a navigation device, etc.

Claims

1. A display device (2060) comprising:

a display panel (100) including pixels (P);
 a data driver (400) configured to output data voltages (VDATA) to the pixels (P);
 a gate driver (300) configured to output a write gate signal (GW) to write the data voltages (VDATA) to the pixels (P) having an inactivation level in a frame stop period (IFP);
 a timing controller (200) configured to control the data driver (400) and the gate driver (300); and
 a voltage generator (600) configured to apply a first bias voltage (VOBS1) to first pixels (P1) to which the data voltages (VDATA) are written before the frame stop period (IFP) among the pixels (P), and to apply a second bias voltage (VOBS2) to second pixels (P2) to which the data voltages (VDATA) are written after the frame stop period (IFP) among the pixels (P).

2. The display device (2060) of claim 1, wherein the second bias voltage (VOBS2) is smaller than the first bias voltage (VOBS1).

3. The display device (2060) of claim 1 or 2, wherein each of the pixels (P) includes a driving transistor (T1),

wherein the gate driver (300) is configured to output a bias gate signal (GW) to the pixels (P), wherein the first bias voltage (VOBS1) is applied to the driving transistor (T1) of each of the first pixels (P1) in response to the bias gate signal (GW), and
 wherein the second bias voltage (VOBS2) is applied to the driving transistor (T1) of each of the second pixels (P2) in response to the bias gate signal (GW).

4. The display device (2060) of claim 3, wherein the bias gate signal (GW) has an inactivation level in the

frame stop period (IFP).

5. The display device (2060) of at least one of claims 1 to 4, further comprising:

an emission driver (500) configured to output an emission signal (EM) to the pixels (P), wherein the timing controller (200) is configured to maintain an output of the emission signal (EM) in the frame stop period (IFP).

6. The display device (2060) of at least one of claims 1 to 5, wherein the timing controller (200) is configured to maintain an output of the bias gate signal (GW) in the frame stop period (IFP), and wherein a time between an activation timing of the bias gate signal (GW) and an activation timing of the emission signal (EM) is constant.

7. The display device (2060) of at least one of claims 1 to 6, wherein the voltage generator (600) is configured to apply a first gate initialization voltage (VINT1) to the first pixels (P1) and to apply a second gate initialization voltage (VINT2) to the second pixels (P2),

wherein each of the pixels (P) includes a driving transistor (T1),
 wherein the gate driver (300) is configured to output an initialization gate signal (GW) to the pixels (P),
 wherein the first gate initialization voltage (VINT1) is applied to a control electrode of the driving transistor (T1) of each of the first pixels (P1) in response to the initialization gate signal (GW), and
 wherein the second gate initialization voltage (VINT2) is applied to the control electrode of the driving transistor (T1) of each of the second pixels (P2) in response to the initialization gate signal (GW).

8. The display device (2060) of claim 7, wherein the second gate initialization voltage (VINT2) is greater than the first gate initialization voltage (VINT1).

9. The display device (2060) of at least one of claims 1 to 8, wherein the initialization gate signal (GW) has an inactivation level in the frame stop period (IFP).

10. The display device (2060) of at least one of claims 1 to 9, wherein the voltage generator (600) is configured to apply a first anode initialization voltage (VAINT1) to the first pixels (P1) and to apply a second anode initialization voltage (VAINT2) to the second pixels (P2),

wherein each of the pixels (P) includes a light

- emitting element (EE),
 wherein the gate driver (300) is configured to output a bias gate signal (GW) to the pixels (P), wherein the first anode initialization voltage (VAINT1) is applied to the light emitting element (EE) of each of the first pixels (P1) in response to the bias gate signal (GW), and
 wherein the second anode initialization voltage (VAINT2) is applied to the light emitting element (EE) of each of the second pixels (P2) in response to the bias gate signal (GW).
11. The display device (2060) of claim 10, wherein the second anode initialization voltage (VAINT2) is smaller than the first anode initialization voltage (VAINT1).
12. The display device (2060) of at least one of claims 1 to 11, wherein the timing controller (200) is configured to perform a touch sensing operation in the frame stop period (IFP).
13. A display device (2060) comprising:
 a display panel (100) including pixels (P);
 a data driver (400) configured to output data voltages (VDATA) to the pixels (P);
 a gate driver (300) configured to output a write gate signal (GW) to write the data voltages (VDATA) to the pixels (P) having an inactivation level in a frame stop period (IFP);
 a timing controller (200) configured to control the data driver (400) and the gate driver (300); and
 a voltage generator (600) configured to apply a bias voltage (VOBS) to the pixels (P) and to vary the bias voltage (VOBS) after the frame stop period (IFP).
14. The display device (2060) of claim 13, wherein the voltage generator (600) is configured to decrease the bias voltage (VOBS) after the frame stop period (IFP).
15. The display device (2060) of claim 13 or 14, wherein the voltage generator (600) is configured to apply a gate initialization voltage (VINT) to the pixels (P), and to vary the gate initialization voltage (VINT) after the frame stop period (IFP),
 wherein each of the pixels (P) includes a driving transistor (T1),
 wherein the gate driver (300) is configured to output an initialization gate signal (GW) to the pixels (P), and
 wherein the gate initialization voltage (VINT) is applied to a control electrode of the driving transistor (T1) of each of the pixels (P) in response
- to the initialization gate signal (GW).
16. The display device (2060) of at least one of claims 13 to 15, wherein the voltage generator (600) is configured to increase the gate initialization voltage (VINT) after the frame stop period (IFP).
17. The display device (2060) of at least one of claims 13 to 16, wherein the voltage generator (600) is configured to apply an anode initialization voltage (VAINT) to the pixels (P), and to vary the anode initialization voltage (VAINT) after the frame stop period (IFP),
 wherein each of the pixels (P) includes a light emitting element (EE),
 wherein the gate driver (300) is configured to output a bias gate signal (GW) to the pixels (P), and
 wherein the anode initialization voltage (VAINT) is applied to the light emitting element (EE) of each of the pixels (P) in response to the bias gate signal (GW).
18. The display device (2060) of claim 17, wherein the voltage generator (600) is configured to decrease the anode initialization voltage (VAINT) after the frame stop period (IFP).
19. A display device (2060) comprising:
 a display panel (100) including pixels (P);
 a data driver (400) configured to output data voltages (VDATA) to the pixels (P);
 a gate driver (300) configured to output a write gate signal (GW) to write the data voltages (VDATA) to the pixels (P) having an inactivation level in a frame stop period (IFP) and to output a bias gate signal (GW) to apply a bias voltage (VOBS) to a driving transistor (T1) included in each of the pixels (P) having an activation level; an emission driver (500) configured to output an emission signal (EM) to the pixels (P);
 a timing controller (200) configured to control the data driver (400), the gate driver (300), and the emission driver (500); and
 a voltage generator (600) configured to apply the bias voltage (VOBS) to the pixels (P).
20. The display device (2060) of claim 19, wherein a time between an activation timing of the bias gate signal (GW) and an activation timing of the emission signal (EM) is constant.

FIG. 1

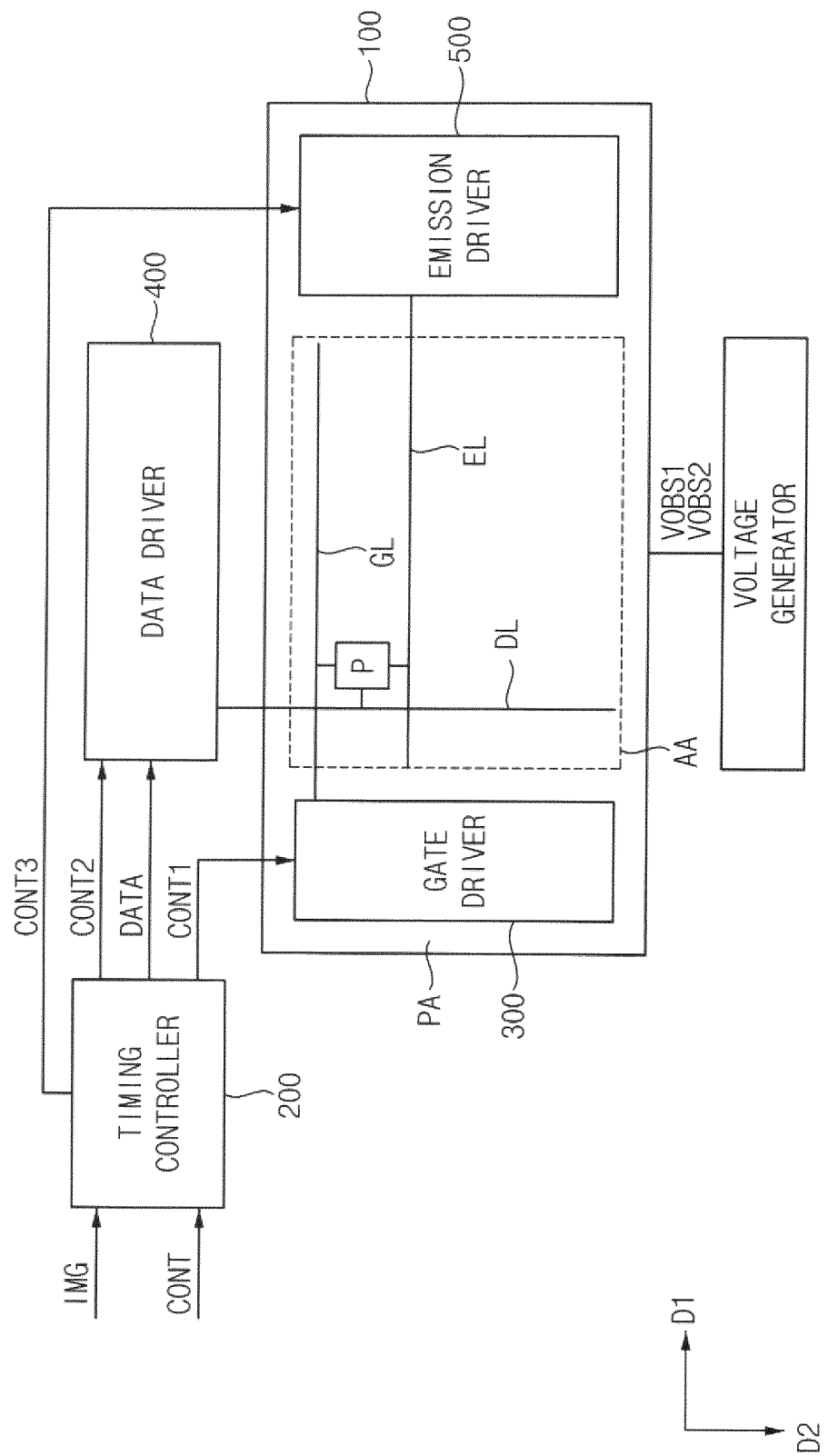


FIG. 2

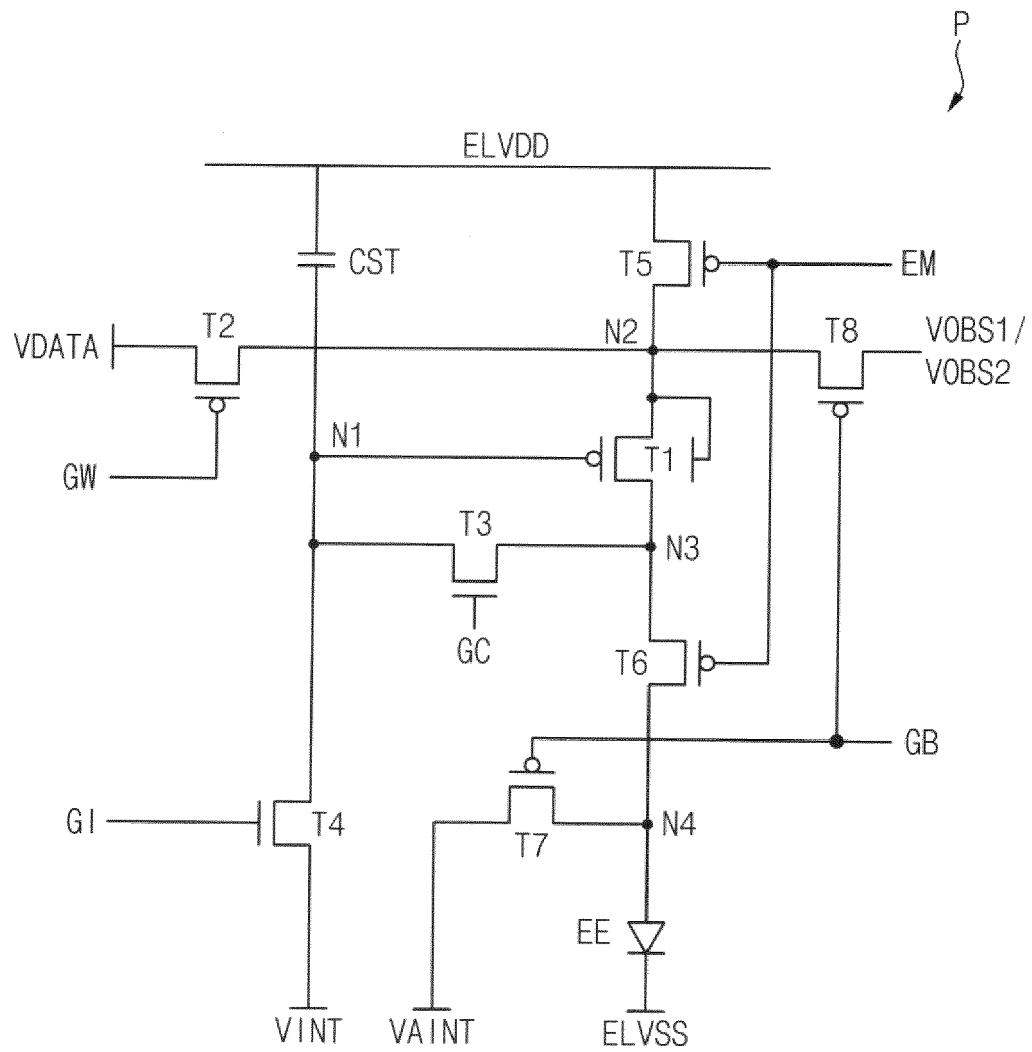


FIG. 3

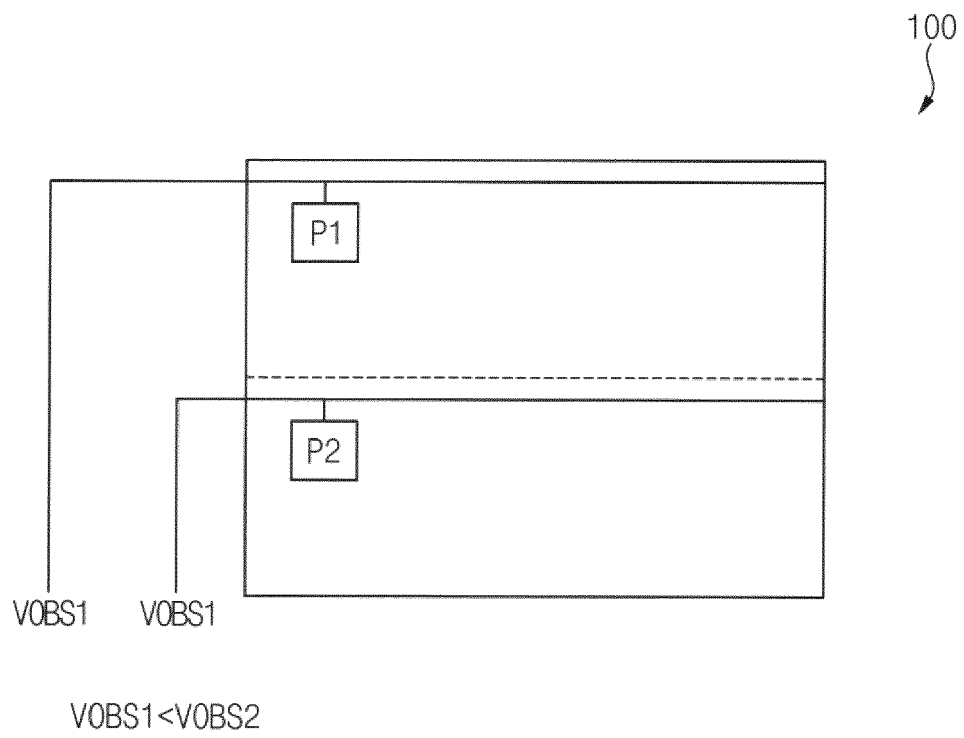


FIG. 4

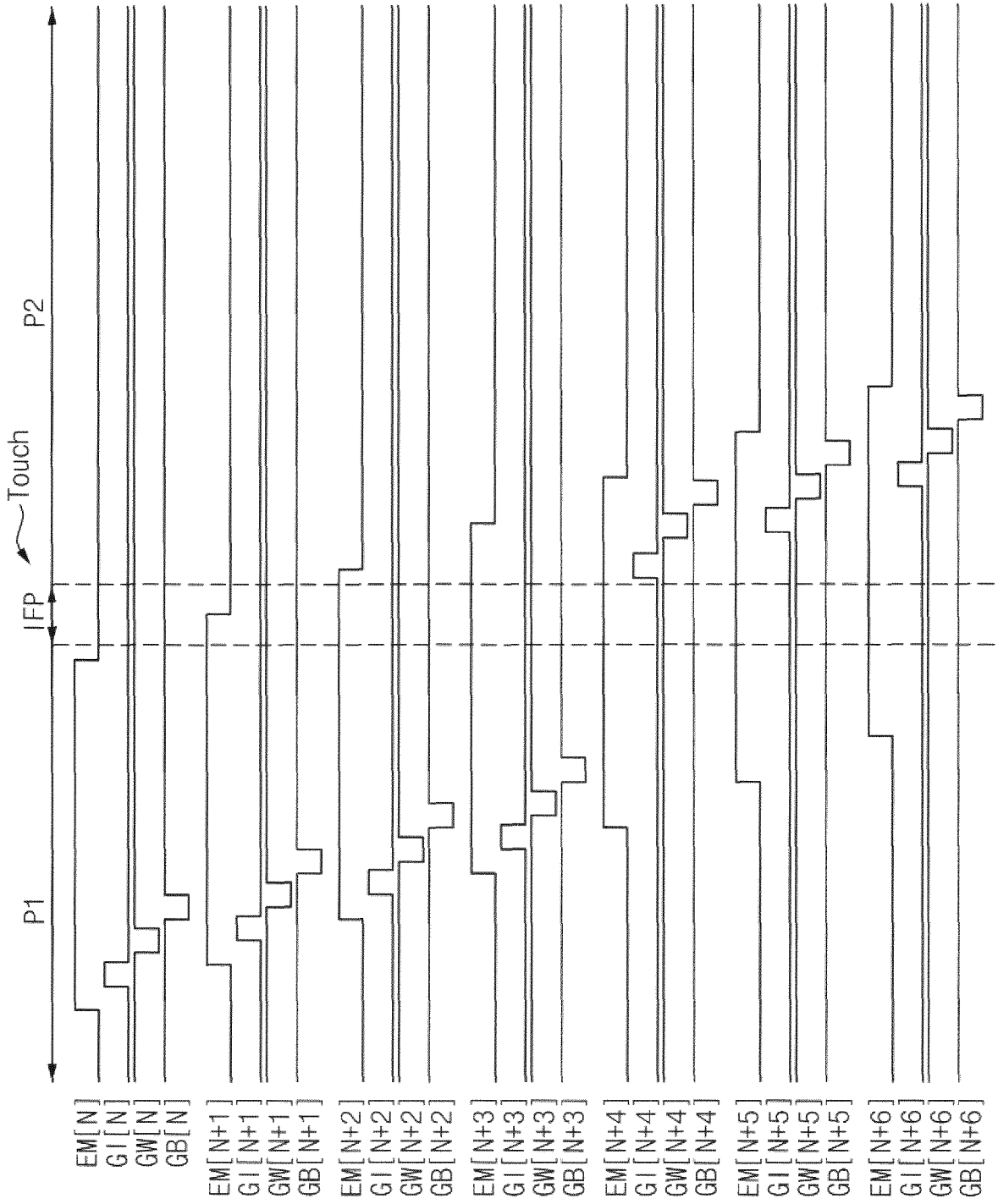


FIG. 5

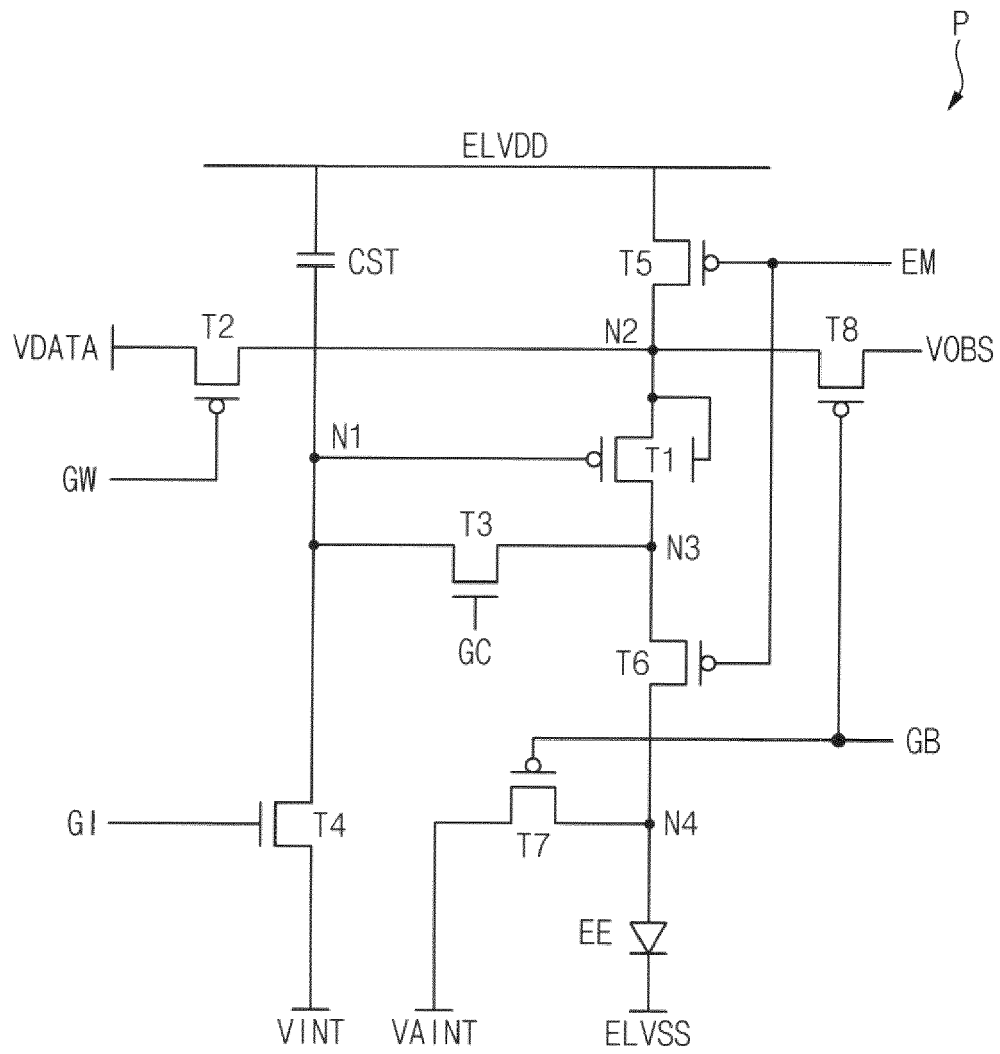


FIG. 6

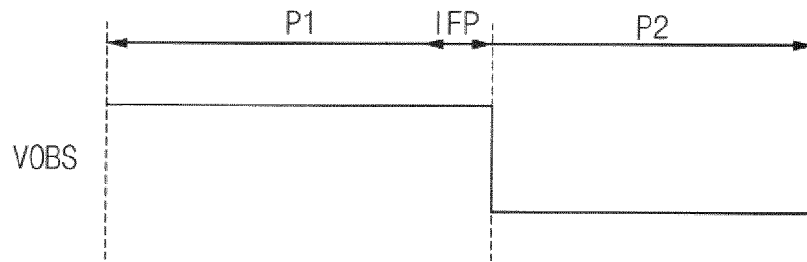


FIG. 7

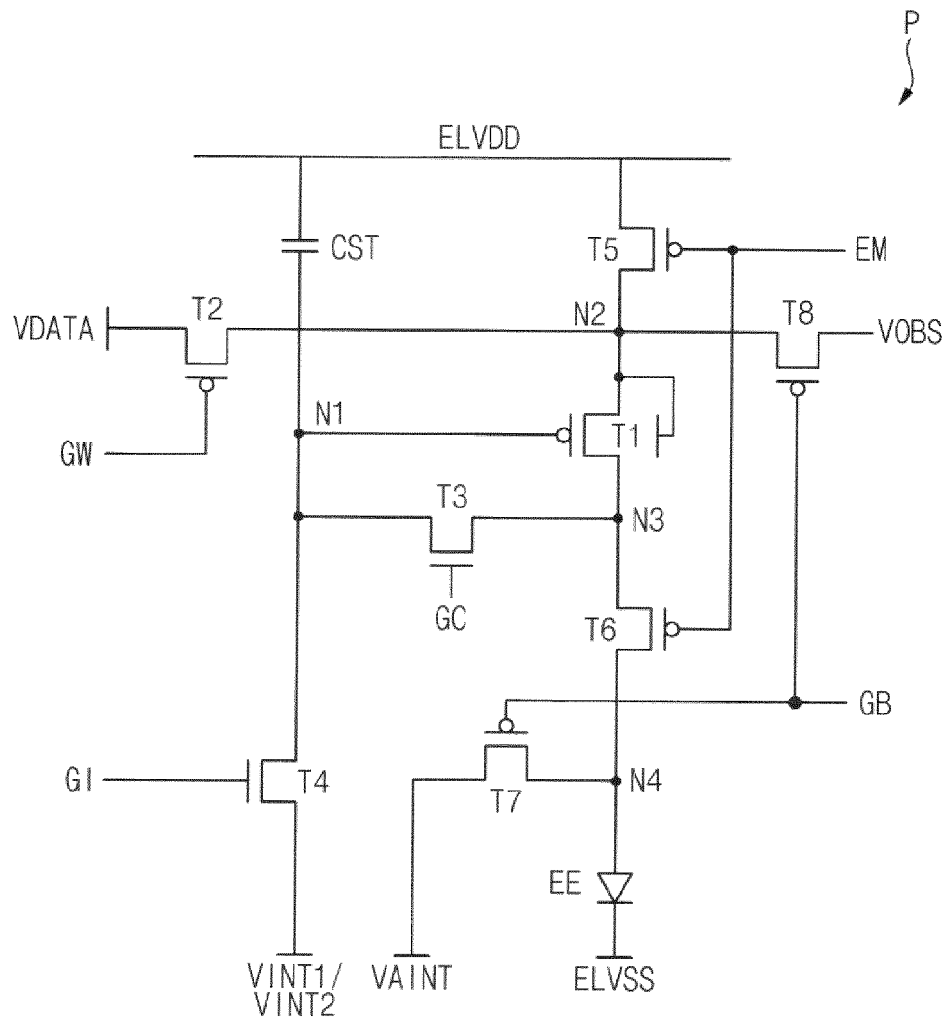


FIG. 8

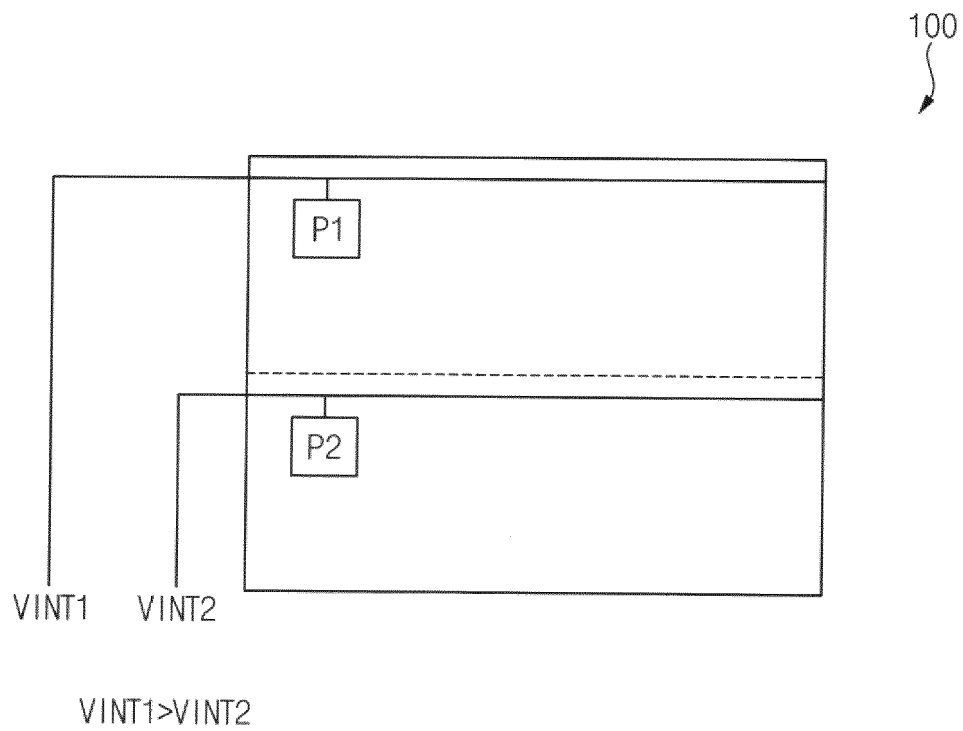


FIG. 9

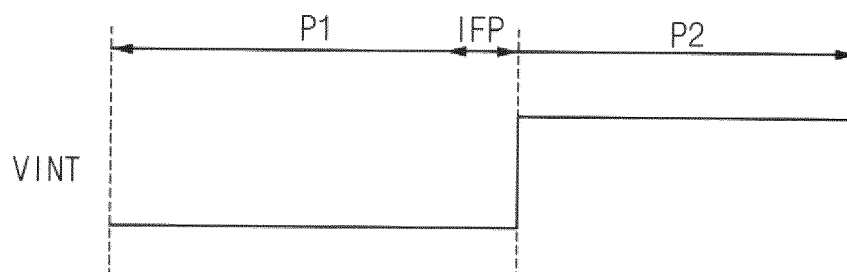


FIG. 10

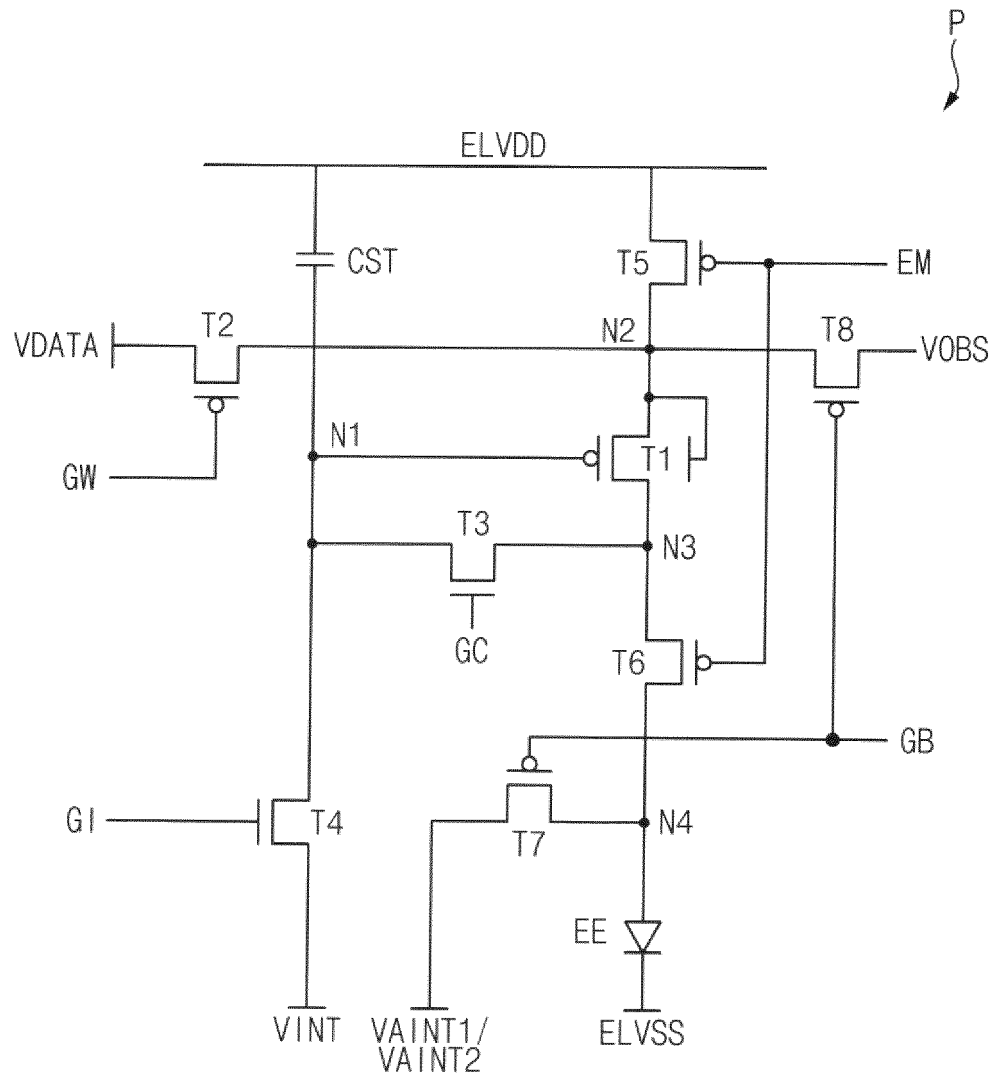


FIG. 11

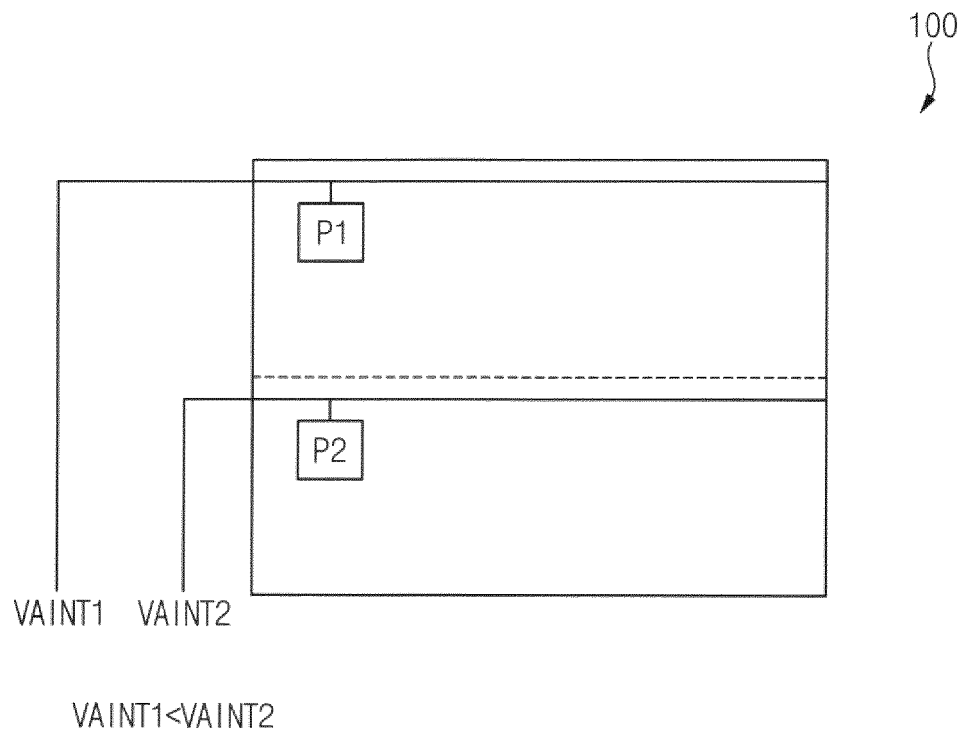


FIG. 12

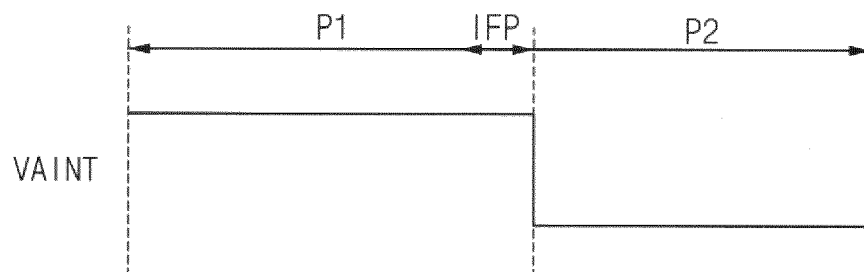


FIG. 13

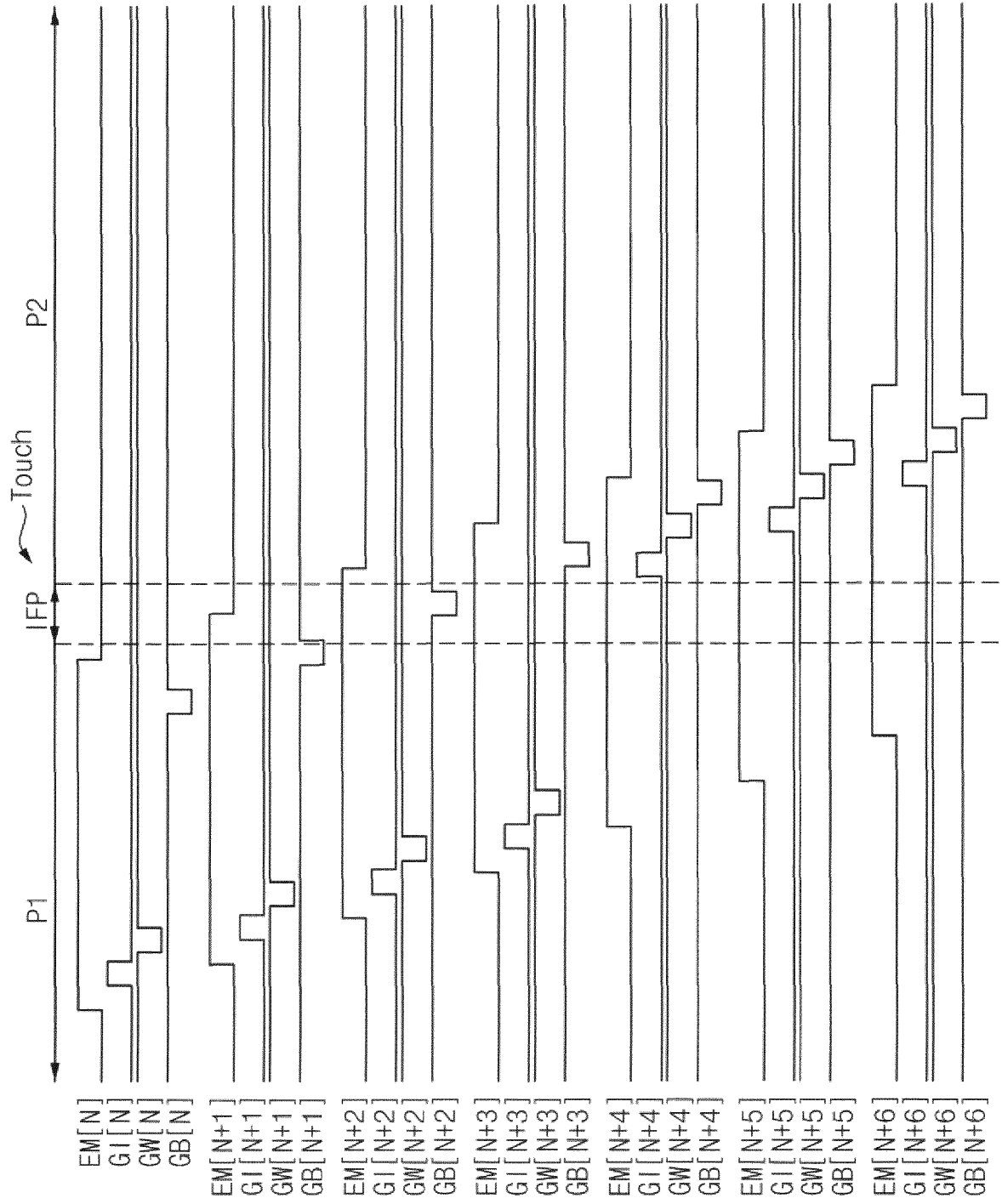


FIG. 14

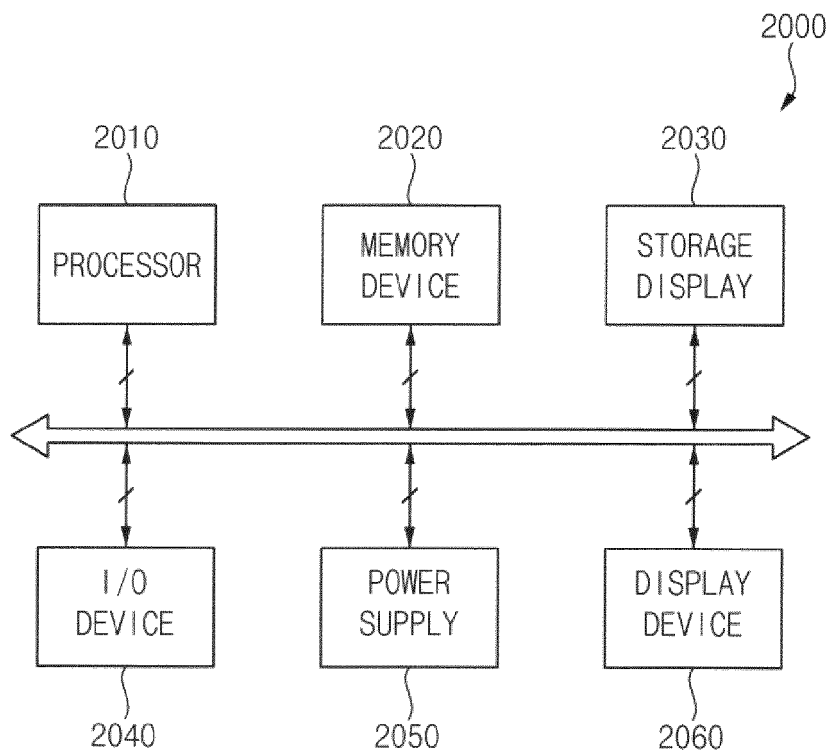
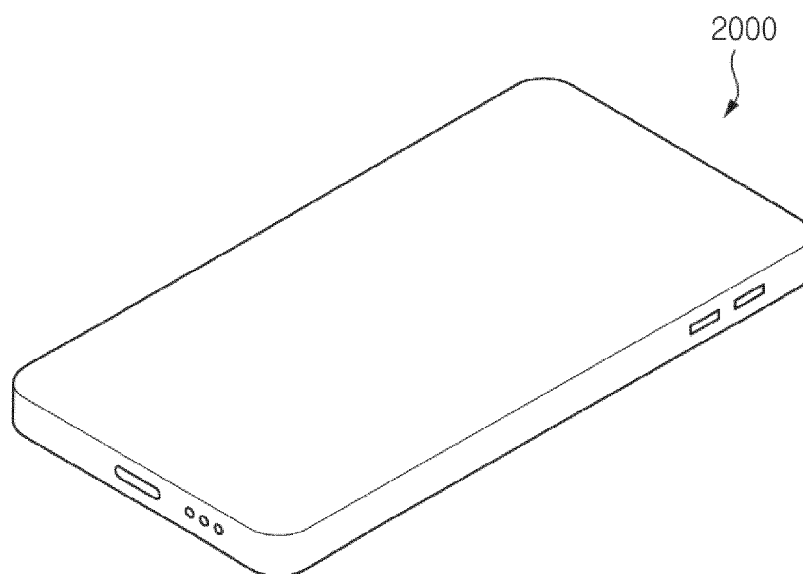


FIG. 15





EUROPEAN SEARCH REPORT

Application Number

EP 23 16 5489

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2021/343238 A1 (OKABE TOHRU [JP] ET AL) 4 November 2021 (2021-11-04) * paragraphs [0001], [0051] - [0062]; figures 1,2,3,4,11,12 * -----	1-17, 19, 20	INV. G09G3/3233
X	US 2022/076627 A1 (KIM HYUNSOO [US] ET AL) 10 March 2022 (2022-03-10) * paragraphs [0041] - [0051]; figures 6,7,8 * -----	1-20	
A	US 2022/180812 A1 (LIN CHIN-WEI [US] ET AL) 9 June 2022 (2022-06-09) * figures 3,10 * -----	1,3-5, 13,19	
			TECHNICAL FIELDS SEARCHED (IPC)
			G09G
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
The Hague		10 November 2023	Ladiray, Olivier
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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 23 16 5489

5

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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10-11-2023

10

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