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(54) **DUMMY CELL AND TAP CELL LAYOUT STRUCTURE**

DUMMYZELLE UND LAYOUTSTRUKTUR FÜR TAP-ZELLE

CELLULE FACTICE ET STRUCTURE D'AGENCEMENT DE CELLULES DE PRISE

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## Description

### CROSS-REFERENCE TO RELATED APPLICATION

**[0001]** This application claims the benefit of U.S. Non-Provisional Patent Application Serial No. 17/362,746, entitled "DUMMY CELL AND TAP CELL LAYOUT STRUCTURE" and filed on June 29, 2021.

### TECHNICAL FIELD

**[0002]** The present disclosure relates generally to a layout structure, and more particularly, to a dummy cell and tap cell layout structure.

### INTRODUCTION

**[0003]** A cell device is an integrated circuit (IC) that implements digital logic. Such cell device may be reused multiple times within an application-specific IC (ASIC). An ASIC, such as a system-on-a-chip (SoC) device, may contain thousands to millions of cell devices. A typical IC includes a stack of sequentially formed layers. Each layer may be stacked or overlaid on a prior layer and patterned to form the shapes that define transistors (e.g., field effect transistors (FETs), fin FETs (FinFETs), gate-all-around (GAA) FETs (GAAFETs), and/or other multigate FETs) and connect the transistors into circuits. Cell devices may be arranged based on a particular layout structure. There is currently a need for improved layout structures.

**[0004]** Further attention is drawn to US 2017/243888 A1 describing that in a circuit block, a plurality of cell rows, each being comprised of a plurality of standard cells arranged in a first direction, are arranged in a second direction perpendicular to the first direction, thereby forming a circuit of SOI transistors. The circuit block includes a plurality of antenna cells, each including an antenna diode provided between a power supply line and a substrate or a well. In at least a part of the circuit block, the antenna cells are arranged at constant intervals in at least one of the first and second directions.

**[0005]** Attention is further drawn to US 2020/243128 A1 describing that first and second memory cell arrays each having memory cells arranged in the X and Y directions lie side by side in the Y direction with space between them. A relay buffer is provided between first and second row decoders for buffering a control signal to be supplied to the second row decoder. An inter-array block between the first and second memory cell arrays is constituted by at least either a tap cell or a dummy memory cell. The relay buffer and the inter-array block are the same in position and size in the Y direction.

**[0006]** Attention is also drawn to US 2017/194319 A1 describing an example circuit which includes: one or more power rails and a tap cell structure. The tap cell structure includes one or more decoupling capacitor cells and one or more tap cells. The one or more tap cells are electrically coupled to the one or more power rails. The one or more decoupling capacitor cells are disposed adjacent to the tap cells and electrically coupled to the one or more power rails.

### BRIEF SUMMARY

**[0007]** The present invention is set forth in the independent claim. Further embodiments of the invention are described in the dependent claims.

**[0008]** In an aspect of the disclosure, a metal oxide semiconductor (MOS) IC includes a first circuit and a second circuit. The first circuit includes a first plurality of n-type MOS (nMOS) devices, a first p-type tap (p-tap) cell, and a first dummy nMOS cell. The first plurality of nMOS devices is spaced apart in a first direction. The first p-tap cell and the first dummy nMOS cell are adjacent to each other in the first direction between the first plurality of nMOS devices. The first p-tap cell is configured to be coupled to a first voltage source. The second circuit includes a first plurality of p-type MOS (pMOS) devices, a first dummy pMOS cell, and a first n-type tap (n-tap) cell. The first plurality of pMOS devices is adjacent to the first plurality of nMOS devices in a second direction orthogonal to the first direction. The first plurality of pMOS devices is spaced apart in the first direction. The first dummy pMOS cell and the first n-tap cell are adjacent to each other in the first direction between the first plurality of pMOS devices. The first n-tap cell is configured to be coupled to a second voltage source. The first p-tap cell and the first dummy pMOS cell are adjacent to each other in the second direction. The first dummy nMOS cell and the first n-tap cell are adjacent to each other in the second direction.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]**

FIG. 1 is a first diagram illustrating a side view of various layers within a cell of an IC.

FIG. 2 is a second diagram illustrating a side view of various layers within a cell of an IC.

FIG. 3 is a diagram conceptually illustrating a top-view of a tap cell layout structure.

FIG. 4 is a first diagram conceptually illustrating a top-view of a dummy cell and tap cell layout structure.

FIG. 5 is a second diagram conceptually illustrating a top-view of a dummy cell and tap cell layout structure.

FIG. 6 is a first diagram conceptually illustrating a top-view of a first configuration of a dummy cell and tap cell layout structure.

FIG. 7 is a second diagram conceptually illustrating a top-view of the first configuration of a dummy cell and tap cell layout structure.

FIG. 8 is a diagram conceptually illustrating a top-view of a second configuration of a dummy cell and

tap cell layout structure.

FIG. 9 is a diagram conceptually illustrating a top-view of a third configuration of a dummy cell and tap cell layout structure.

FIG. 10 is a diagram conceptually illustrating a top-view of a fourth configuration of a dummy cell and tap cell layout structure.

FIG. 11 is a third diagram conceptually illustrating a top-view of a dummy cell and tap cell layout structure.

## DETAILED DESCRIPTION

**[0010]** The detailed description set forth below in connection with the appended drawings is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well known structures and components are shown in block diagram form in order to avoid obscuring such concepts. Apparatuses and methods will be described in the following detailed description and may be illustrated in the accompanying drawings by various blocks, modules, components, circuits, steps, processes, algorithms, elements, etc.

**[0011]** FIG. 1 is a first diagram 100 illustrating a side view of various layers within a cell device and IC. The various layers change in the y direction. As illustrated in FIG. 1, a transistor has a gate 102 (which may be referred to as POLY in some instances even though the gate may be formed of metal, polysilicon, or a combination of polysilicon and metal), a source 104, and a drain 106. The source 104 and the drain 106 may be formed by fins. The gate 102 may extend in a second direction (e.g., vertical direction along the z axis coming out of the page), and the fins may extend in a first direction orthogonal to the second direction (e.g., horizontal direction along the x axis). A contact layer interconnect 108 (also referred to as a metal POLY (MP) layer interconnect, or contact B (CB) layer interconnect) may contact the gate 102. A contact layer interconnect 110 (also referred to as a metal diffusion (MD) layer interconnect, or contact A (CA) layer interconnect) may contact the source 104 and/or the drain 106. A via 112 (also referred to as via A (VA)) may contact the contact layer interconnect 110. A metal 1 (M1) layer interconnect 114 may contact the via 112. The M1 layer interconnect 114 may extend in the first direction only (i.e., unidirectional in the first direction). A via V1 116 may contact the M1 layer interconnect 114. A metal 2 (M2) layer interconnect 118 may contact the via V1 116. The M2 layer interconnect 118 may extend in the second direction only (i.e., unidirectional in the second direction). Higher layers include a via layer including vias V2 and a metal 3 (M3) layer including M3 layer interconnects. The M3 layer interconnects may extend in the first direction. A cell device may be implemented with FinFETs (as illustrated), GAAFETs, or other multigate FETs. For a continuous oxide diffusion (OD) region across multiple devices, the fins are continuous (in the first direction) across the multiple devices. For a discontinuous OD region across multiple devices, the fins are separate at a diffusion break (e.g., single/double diffusion break extending in the second direction) between different sets of the multiple devices.

**[0012]** FIG. 2 is a second diagram 200 illustrating a side view of various layers within a standard cell and IC. The various layers change in the y direction. As illustrated in FIG. 2, a transistor has a gate 202, a source 204, and a drain 206. The source 204 and the drain 206 may be formed by fins. The gate 202 may extend in a second direction (e.g., vertical direction along the z axis coming out of the page), and the fins may extend in a first direction orthogonal to the second direction (e.g., horizontal direction along the x axis). A contact layer interconnect 208 (also referred to as CB layer interconnect) may contact the gate 202. A contact layer interconnect 210 (also referred to as CA layer interconnect) may contact the source 204 and/or the drain 206. A via 212 (also referred to as via B (VB)) may contact the contact layer interconnect 208. An M1 layer interconnect 214 may contact the via 212. The M1 layer interconnect 214 may extend in the first direction only (i.e., unidirectional in the first direction). A via V1 216 may contact the M1 layer interconnect 214. An M2 layer interconnect 218 may contact the via V1 216. The M2 layer interconnect 218 may extend in the second direction only (i.e., unidirectional in the second direction). Higher layers include a via layer including vias V2 and an M3 layer including M3 layer interconnects. The M3 layer interconnects may extend in the first direction. A cell device may be implemented with FinFETs (as illustrated), GAAFETs, or other multigate FETs. For a continuous OD region across multiple devices, the fins are continuous (in the first direction) across the multiple devices. For a discontinuous OD region across multiple devices, the fins are separate at a diffusion break (e.g., single/double diffusion break extending in the second direction) between different sets of the multiple devices.

**[0013]** FIG. 3 is a diagram 300 conceptually illustrating a top-view of a tap cell layout structure. A cell device may include pMOS devices and/or nMOS devices. The nMOS devices include n-type doped (n+) source and drain regions. The n+ source and drain regions may be referred to as n-plus (NP) implant layers. Each set of nMOS devices is illustrated by an NP layer with an OD layer on the NP layer. The pMOS devices include p-type doped (p+) source and drain regions. The p+ source and drain regions may be referred to as p-plus (PP) implant layers. Each set of pMOS devices is illustrated by a PP layer with an OD layer on the PP layer. Of an IC, tap cells (also referred to as guard tap cells) may be located adjacent to a set of pMOS devices and to a set of nMOS devices to provide body connections to the pMOS devices and to the

nMOS devices, respectively. A p-tap cell includes a p-type doped (p+) region and provides a body connection for a set of nMOS devices. The p+ region of the p-tap cell may be referred to as a PP implant layer. Each p-tap cell is illustrated by a PP layer with an OD layer on the PP layer. An n-tap cell includes an n-type doped (n+) region and provides a body connection for a set of pMOS devices. The n+ region of the n-tap cell may be referred to as an NP implant layer. Each n-tap cell is illustrated by an NP layer with an OD layer on the NP layer. A set of pMOS devices and adjacent n-tap cells may be within an n-type well (n-well), assuming the IC is implemented with a p-type substrate.

**[0014]** For some fabrication processes, design rule check (DRC) violations may be encountered at corner areas 302 (see markers within the circles 302 illustrating the four-corner areas, with PP,NP, PP,NP layers meeting at each corner) of the NP layers and PP layers, where PP layers of a set of pMOS devices and a p-tap cell are diagonal from each other and NP layers of a set of nMOS devices and an n-tap cell are diagonal from each other. Specifically, the four-corner areas are defined by 90° edges of an nMOS device (NP), a p-tap cell (PP), an n-tap cell (NP), and a pMOS device (PP) all meeting at one corner. The DRC violations may occur for the illustrated corner case abutment of nMOS devices, pMOS devices, and corresponding tap cells, and may report width and spacing errors in association with the corner case abutment of the NP/PP layers. To avoid such DRC violations, a dummy cell and tap cell layout structure is provided below with respect to FIGs. 4-11.

**[0015]** FIG. 4 is a first diagram 400 conceptually illustrating a top-view of a dummy cell and tap cell layout structure. The illustrated dummy cell and tap cell layout structure is a subsection of a larger layout structure, where the pattern illustrated may be repeated The illustrated dummy cell and tap cell layout structure includes four columns of devices/cells, including a first column 402 of active devices, a second column 404 of PP implant cells including dummy pMOS cells (P-D) / p-tap cells (P-T), a third column 406 of NP implant cells including dummy nMOS cells (N-D) / n-tap cells (N-T), and a fourth column 408 of active devices. The active devices in the columns 402, 408 include both nMOS devices 410 and pMOS devices 412. In an alternative configuration, the columns 404, 406 may be swapped, with the NP implant cells in the second column 404 and the PP implant cells in the third column 406. Such a layout structure can be obtained by flipping / mirroring the illustrated layout structure, or rotating the illustrated layout structure clockwise/counterclockwise by 180°. The active devices in the columns 402, 408 are illustrated with pairs of adjacent nMOS devices 410 interleaved with pairs of adjacent pMOS devices 412. Generally, each row of active devices may include $n$ adjacent nMOS devices 410 interleaved with $m$ adjacent pMOS devices 412, where $n \geq 1$ and $m \geq 1$ (see FIG. 11). In the illustrated dummy cell and tap cell layout structure, $n = 2$ and $m = 2$.

**[0016]** As illustrated in the dummy cell and tap cell layout structure, a dummy nMOS cell 422 is located adjacent to each p-tap cell 420, and a dummy pMOS cell 424 is located adjacent to each n-tap cell 426, where cells with PP layers are in one column and cells with NP layers are in an adjacent column. Through placement of the dummy nMOS cells 422 and the dummy pMOS cells 424 within the layout structure, the four-corner areas (see 302) with the PP, NP, PP, NP layers meeting at one corner can be avoided. Accordingly, by avoiding such four-corner areas, associated DRC violations can be avoided. Avoid DRC violations can improve the yield of corresponding fabricated MOS ICs and performance of the fabricated MOS ICs.

**[0017]** FIG. 5 is a second diagram 500 conceptually illustrating a top-view of a dummy cell and tap cell layout structure. As illustrated in FIG. 5, the addition of the dummy pMOS cells 424 and dummy nMOS cells 422 within the layout structure as illustrated in FIG. 4 provides a layout structure that excludes the four-corner areas of the NP/PP layers. As illustrated by the arrows in FIG. 5, the PP/NP layers each have a C-shape within the layout structure. Four-corner areas of the NP/PP layers are non-existent in the configuration.

**[0018]** FIG. 6 is a first diagram 600 conceptually illustrating a top-view of a first configuration of a dummy cell and tap cell layout structure. FIG. 7 is a second diagram 700 conceptually illustrating a top-view of the first configuration of a dummy cell and tap cell layout structure. The first and second diagrams 600, 700 illustrate a MOS IC. The MOS IC includes circuits 690 - 697. The circuit 690 includes a plurality of nMOS devices 602/608, a p-tap cell 604, and a dummy nMOS cell 606. The plurality of nMOS devices 602/608 is spaced apart in a first direction. The p-tap cell 604 and the dummy nMOS cell 606 are adjacent to each other in the first direction between the plurality of nMOS devices 602/608. The p-tap cell 604 is configured to be coupled to a first voltage source. The p-tap cell 604 provides a body connection for the plurality of nMOS devices 602/608. In one example, the first voltage source is configured to provide the voltage Vss.

**[0019]** The circuit 691 includes a plurality of pMOS devices 612/618, a dummy pMOS cell 614, and an n-tap cell 616. Assuming the IC is implemented with a p-type substrate, the circuit 691 is located within an n-well on the p-type substrate. The plurality of pMOS devices 612/618 is adjacent to the plurality of nMOS devices 602/608 in a second direction orthogonal to the first direction. The plurality of pMOS devices 612/618 is spaced apart in the first direction. The dummy pMOS cell 614 and the n-tap cell 616 are adjacent to each other in the first direction between the plurality of pMOS devices 612/618. The n-tap cell 616 is configured to be coupled to a second voltage source. The n-tap cell 616 provides a body connection for the plurality of pMOS devices 612/618. In one example, the second voltage source is configured to provide the voltage Vdd. The p-tap cell 604 and the dummy pMOS cell 614 are adjacent

to each other in the second direction. The dummy nMOS cell 606 and the n-tap cell 616 are adjacent to each other in the second direction.

**[0020]** The circuit 692 includes a plurality of nMOS devices 622/628, a p-tap cell 624, and a dummy nMOS cell 626. The plurality of nMOS devices 622/628 is adjacent to the plurality of pMOS devices 612/618 in the second direction. The plurality of nMOS devices 622/628 is spaced apart in the first direction. The p-tap cell 624 and the dummy nMOS cell 626 are adjacent to each other in the first direction between the plurality of nMOS devices 622/628. The p-tap cell 624 is configured to be coupled to the first voltage source. The p-tap cell 624 provides a body connection for the plurality of nMOS devices 622/628. The dummy pMOS cell 614 and the p-tap cell 624 are adjacent to each other in the second direction. The n-tap cell 616 and the dummy nMOS cell 626 are adjacent to each other in the second direction.

**[0021]** The circuit 693 includes a plurality of pMOS devices 632/638, a dummy pMOS cell 634, and an n-tap cell 636. Assuming the IC is implemented with a p-type substrate, the circuit 693 is located within an n-well on the p-type substrate. The plurality of pMOS devices 632/638 is adjacent to the plurality of nMOS devices 622/628 in the second direction. The plurality of pMOS devices 632/638 is spaced apart in the first direction. The dummy pMOS cell 634 and the n-tap cell 636 are adjacent to each other in the first direction between the plurality of pMOS devices 632/638. The n-tap cell 636 is configured to be coupled to the second voltage source. The n-tap cell 636 provides a body connection for the plurality of pMOS devices 632/638. The p-tap cell 624 and the dummy pMOS cell 634 are adjacent to each other in the second direction. The dummy nMOS cell 626 and the n-tap cell 636 are adjacent to each other in the second direction.

**[0022]** The circuit 694 includes a plurality of nMOS devices 642/648, a p-tap cell 644, and a dummy nMOS cell 646. The plurality of nMOS devices 642/648 is adjacent to the plurality of pMOS devices 632/638 in the second direction. The plurality of nMOS devices 642/648 is spaced apart in the first direction. The p-tap cell 644 and the dummy nMOS cell 646 are adjacent to each other in the first direction between the plurality of nMOS devices 642/648. The p-tap cell 644 is configured to be coupled to the first voltage source. The p-tap cell 644 provides a body connection for the plurality of nMOS devices 642/648. The dummy pMOS cell 634 and the p-tap cell 644 are adjacent to each other in the second direction. The n-tap cell 636 and the dummy nMOS cell 646 are adjacent to each other in the second direction.

**[0023]** The circuit 695 includes a plurality of pMOS devices 652/658, a dummy pMOS cell 654, and an n-tap cell 656. Assuming the IC is implemented with a p-type substrate, the circuit 695 is located within an n-well on the p-type substrate. The plurality of pMOS devices 652/658 is adjacent to the plurality of nMOS devices 642/648 in the second direction. The plurality of pMOS devices 652/658 is spaced apart in the first direction. The dummy pMOS cell 654 and the n-tap cell 656 are adjacent to each other in the first direction between the plurality of pMOS devices 652/658. The n-tap cell 656 is configured to be coupled to the second voltage source. The n-tap cell 656 provides a body connection for the plurality of pMOS devices 652/658. The p-tap cell 644 and the dummy pMOS cell 654 are adjacent to each other in the second direction. The dummy nMOS cell 646 and the n-tap cell 656 are adjacent to each other in the second direction.

**[0024]** The circuit 696 includes a plurality of nMOS devices 662/668, a p-tap cell 664, and a dummy nMOS cell 666. The plurality of nMOS devices 662/668 is adjacent to the plurality of pMOS devices 652/658 in the second direction. The plurality of nMOS devices 662/668 is spaced apart in the first direction. The p-tap cell 664 and the dummy nMOS cell 666 are adjacent to each other in the first direction between the plurality of nMOS devices 662/668. The p-tap cell 664 is configured to be coupled to the first voltage source. The p-tap cell 664 provides a body connection for the plurality of nMOS devices 662/668. The dummy pMOS cell 654 and the p-tap cell 664 are adjacent to each other in the second direction. The n-tap cell 656 and the dummy nMOS cell 666 are adjacent to each other in the second direction.

**[0025]** The circuit 697 includes a plurality of pMOS devices 672/678, a dummy pMOS cell 674, and an n-tap cell 676. Assuming the IC is implemented with a p-type substrate, the circuit 697 is located within an n-well on the p-type substrate. The plurality of pMOS devices 672/678 is adjacent to the plurality of nMOS devices 662/668 in the second direction. The plurality of pMOS devices 672/678 is spaced apart in the first direction. The dummy pMOS cell 674 and the n-tap cell 676 are adjacent to each other in the first direction between the plurality of pMOS devices 672/678. The n-tap cell 676 is configured to be coupled to the second voltage source. The n-tap cell 676 provides a body connection for the plurality of pMOS devices 672/678. The p-tap cell 664 and the dummy pMOS cell 674 are adjacent to each other in the second direction. The dummy nMOS cell 666 and the n-tap cell 676 are adjacent to each other in the second direction.

**[0026]** The dummy nMOS cells 606, 626, 646, 666 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. Likewise, the dummy pMOS cells 614, 634, 654, 674 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. The second voltage source, for example Vdd, may be configured to provide a higher voltage than the first voltage source, for example Vss. As can be appreciated in FIG. 6, an area of each of the p-tap cells 604, 624, 644, 664; the dummy nMOS cells 606, 626, 646, 666; the dummy pMOS cells 614, 634, 654, 674; and the n-tap cells 616, 636, 656, 676 is approximately equal. OD regions (shown in FIG. 4 by the inner rectangle within each

device/cell; may also be referred to as OD islands in this case) of the p-tap cells 604, 624, 644, 664; the dummy nMOS cells 606, 626, 646, 666; the dummy pMOS cells 614, 634, 654, 674; and the n-tap cells 616, 636, 656, 676 are separate and discontinuous with respect to each other.

**[0027]** Referring to FIG. 7, the NP layers of the nMOS devices, dummy nMOS cells, and n-tap cells form C-shapes 702, 706 around PP layers of pMOS devices, and the PP layers of the pMOS devices, dummy pMOS cells, and p-tap cells form C-shapes 704, 708 around NP layers of nMOS devices. The dummy cell and tap cell layout structure excludes corner case abutment of four-corner areas of adjoining NP, PP, NP, PP layers, and consequently, avoids DRC violations in association with such corner case abutment.

**[0028]** The dummy cell and tap cell layout structure discussed in relation to FIGs. 6, 7, include dummy nMOS/pMOS cells that change the configuration of the NP/PP layers in order to exclude corner case abutment of NP, PP, NP, PP four-corner areas. The addition of the dummy nMOS/pMOS cells increases an overall area of the IC. Several alternative configurations of the dummy cell and tap cell layout structure that may reduce the amount of area utilized by the dummy cells are provided below with respect to FIGs. 8, 9, 10.

**[0029]** FIG. 8 is a diagram 800 conceptually illustrating a top-view of a second configuration of a dummy cell and tap cell layout structure. In FIG. 8, the dummy nMOS/pMOS cells are reduced in width and the adjacent p-tap cells and n-tap cells are enlarged in width by the same amount as the reduction in width of the dummy nMOS/pMOS cells. Providing a larger OD area for the tap cell body connections may provide some performance improvements in some configurations. The diagram 800 illustrates a MOS IC. The MOS IC includes circuits 890 - 897. The circuit 890 includes a plurality of nMOS devices 802/808, a p-tap cell 804, and a dummy nMOS cell 806. The plurality of nMOS devices 802/808 is spaced apart in a first direction. The p-tap cell 804 and the dummy nMOS cell 806 are adjacent to each other in the first direction between the plurality of nMOS devices 802/808. The p-tap cell 804 is configured to be coupled to a first voltage source. The p-tap cell 804 provides a body connection for the plurality of nMOS devices 802/808. In one example, the first voltage source is configured to provide the voltage Vss.

**[0030]** The circuit 891 includes a plurality of pMOS devices 812/818, a dummy pMOS cell 814, and an n-tap cell 816. Assuming the IC is implemented with a p-type substrate, the circuit 891 is located within an n-well on the p-type substrate. The plurality of pMOS devices 812/818 is adjacent to the plurality of nMOS devices 802/808 in a second direction orthogonal to the first direction. The plurality of pMOS devices 812/818 is spaced apart in the first direction. The dummy pMOS cell 814 and the n-tap cell 816 are adjacent to each other in the first direction between the plurality of pMOS devices 812/818. The n-tap cell 816 is configured to be coupled to a second voltage source. The n-tap cell 816 provides a body connection for the plurality of pMOS devices 812/818. In one example, the second voltage source is configured to provide the voltage Vdd. In this configuration, the p-tap cell 804 is adjacent to both the dummy pMOS cell 814 and the n-tap cell 816 in the second direction. In addition, the n-tap cell 816 is adjacent to both the p-tap cell 804 and the dummy nMOS cell 806 in the second direction. Further, the nMOS devices 802/808 are non-adjacent in the second direction to the dummy pMOS cell 814 and the n-tap cell 816, and the pMOS devices 812/818 are non-adjacent in the second direction to the p-tap cell 804 and the dummy nMOS cell 806.

**[0031]** The circuit 892 includes a plurality of nMOS devices 822/828, a p-tap cell 824, and a dummy nMOS cell 826. The plurality of nMOS devices 822/828 is adjacent to the plurality of pMOS devices 812/818 in the second direction. The plurality of nMOS devices 822/828 is spaced apart in the first direction. The p-tap cell 824 and the dummy nMOS cell 826 are adjacent to each other in the first direction between the plurality of nMOS devices 822/828. The p-tap cell 824 is configured to be coupled to the first voltage source. The p-tap cell 824 provides a body connection for the plurality of nMOS devices 822/828. In this configuration, the n-tap cell 816 is adjacent to both the p-tap cell 824 and the dummy nMOS cell 826 in the second direction. In addition, the p-tap cell 824 is adjacent to both the dummy pMOS cell 814 and the n-tap cell 816 in the second direction. Further, the pMOS devices 812/818 are non-adjacent in the second direction to the p-tap cell 824 and the dummy nMOS cell 826, and the nMOS devices 822/828 are non-adjacent in the second direction to the dummy pMOS cell 814 and the n-tap cell 816.

**[0032]** The circuit 893 includes a plurality of pMOS devices 832/838, a dummy pMOS cell 834, and an n-tap cell 836. Assuming the IC is implemented with a p-type substrate, the circuit 893 is located within an n-well on the p-type substrate. The plurality of pMOS devices 832/838 is adjacent to the plurality of nMOS devices 822/828 in the second direction. The plurality of pMOS devices 832/838 is spaced apart in the first direction. The dummy pMOS cell 834 and the n-tap cell 836 are adjacent to each other in the first direction between the plurality of pMOS devices 832/838. The n-tap cell 836 is configured to be coupled to the second voltage source. The n-tap cell 836 provides a body connection for the plurality of pMOS devices 832/838. In this configuration, the p-tap cell 824 is adjacent to both the dummy pMOS cell 834 and the n-tap cell 836 in the second direction. In addition, the n-tap cell 836 is adjacent to both the p-tap cell 824 and the dummy nMOS cell 826 in the second direction. Further, the nMOS devices 822/828 are non-adjacent in the second direction to the dummy pMOS cell 834 and the n-tap cell 836, and the pMOS devices 832/838 are non-adjacent in the second direction to

the p-tap cell 824 and the dummy nMOS cell 826.

**[0033]** The circuit 894 includes a plurality of nMOS devices 842/848, a p-tap cell 844, and a dummy nMOS cell 846. The plurality of nMOS devices 842/848 is adjacent to the plurality of pMOS devices 832/838 in the second direction. The plurality of nMOS devices 842/848 is spaced apart in the first direction. The p-tap cell 844 and the dummy nMOS cell 846 are adjacent to each other in the first direction between the plurality of nMOS devices 842/848. The p-tap cell 844 is configured to be coupled to the first voltage source. The p-tap cell 844 provides a body connection for the plurality of nMOS devices 842/848. In this configuration, the n-tap cell 836 is adjacent to both the p-tap cell 844 and the dummy nMOS cell 846 in the second direction. In addition, the p-tap cell 844 is adjacent to both the dummy pMOS cell 834 and the n-tap cell 836 in the second direction. Further, the pMOS devices 832/838 are non-adjacent in the second direction to the p-tap cell 844 and the dummy nMOS cell 846, and the nMOS devices 842/848 are non-adjacent in the second direction to the dummy pMOS cell 834 and the n-tap cell 836.

**[0034]** The circuit 895 includes a plurality of pMOS devices 852/858, a dummy pMOS cell 854, and an n-tap cell 856. Assuming the IC is implemented with a p-type substrate, the circuit 895 is located within an n-well on the p-type substrate. The plurality of pMOS devices 852/858 is adjacent to the plurality of nMOS devices 842/848 in the second direction. The plurality of pMOS devices 852/858 is spaced apart in the first direction. The dummy pMOS cell 854 and the n-tap cell 856 are adjacent to each other in the first direction between the plurality of pMOS devices 852/858. The n-tap cell 856 is configured to be coupled to the second voltage source. The n-tap cell 856 provides a body connection for the plurality of pMOS devices 852/858. In this configuration, the p-tap cell 844 is adjacent to both the dummy pMOS cell 854 and the n-tap cell 856 in the second direction. In addition, the n-tap cell 856 is adjacent to both the p-tap cell 844 and the dummy nMOS cell 846 in the second direction. Further, the nMOS devices 842/848 are non-adjacent in the second direction to the dummy pMOS cell 854 and the n-tap cell 856, and the pMOS devices 852/858 are non-adjacent in the second direction to the p-tap cell 844 and the dummy nMOS cell 846.

**[0035]** The circuit 896 includes a plurality of nMOS devices 862/868, a p-tap cell 864, and a dummy nMOS cell 866. The plurality of nMOS devices 862/868 is adjacent to the plurality of pMOS devices 852/858 in the second direction. The plurality of nMOS devices 862/868 is spaced apart in the first direction. The p-tap cell 864 and the dummy nMOS cell 866 are adjacent to each other in the first direction between the plurality of nMOS devices 862/868. The p-tap cell 864 is configured to be coupled to the first voltage source. The p-tap cell 864 provides a body connection for the plurality of nMOS devices 862/868. In this configuration, the n-tap cell 856 is adjacent to both the p-tap cell 864 and the dummy nMOS cell 866 in the second direction. In addition, the p-tap cell 864 is adjacent to both the dummy pMOS cell 854 and the n-tap cell 856 in the second direction. Further, the pMOS devices 852/858 are non-adjacent in the second direction to the p-tap cell 864 and the dummy nMOS cell 866, and the nMOS devices 862/868 are non-adjacent in the second direction to the dummy pMOS cell 854 and the n-tap cell 856.

**[0036]** The circuit 897 includes a plurality of pMOS devices 872/878, a dummy pMOS cell 874, and an n-tap cell 876. Assuming the IC is implemented with a p-type substrate, the circuit 897 is located within an n-well on the p-type substrate. The plurality of pMOS devices 872/878 is adjacent to the plurality of nMOS devices 862/868 in the second direction. The plurality of pMOS devices 872/878 is spaced apart in the first direction. The dummy pMOS cell 874 and the n-tap cell 876 are adjacent to each other in the first direction between the plurality of pMOS devices 872/878. The n-tap cell 876 is configured to be coupled to the second voltage source. The n-tap cell 876 provides a body connection for the plurality of pMOS devices 872/878. In this configuration, the p-tap cell 864 is adjacent to both the dummy pMOS cell 874 and the n-tap cell 876 in the second direction. In addition, the n-tap cell 876 is adjacent to both the p-tap cell 864 and the dummy nMOS cell 866 in the second direction. Further, the nMOS devices 862/868 are non-adjacent in the second direction to the dummy pMOS cell 874 and the n-tap cell 876, and the pMOS devices 872/878 are non-adjacent in the second direction to the p-tap cell 864 and the dummy nMOS cell 866.

**[0037]** The dummy nMOS cells 806, 826, 846, 866 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. Likewise, the dummy pMOS cells 814, 834, 854, 874 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. The second voltage source, for example Vdd, may be configured to provide a higher voltage than the first voltage source, for example Vss. As can be appreciated in FIG. 8, an area of each of the p-tap cells 804, 824, 844, 864 is greater than an area of each of the dummy nMOS cells 806, 826, 846, 866. In addition, an area of each of the n-tap cells 816, 836, 856, 876 is greater than an area of each of the dummy pMOS cells 814, 834, 854, 874. OD regions (shown in FIG. 4 by the inner rectangle within each device/cell; may also be referred to as OD islands in this case) of the p-tap cells 804, 824, 844, 864; the dummy nMOS cells 806, 826, 846, 866; the dummy pMOS cells 814, 834, 854, 874; and the n-tap cells 816, 836, 856, 876 are separate and discontinuous with respect to each other.

**[0038]** The dummy cell and tap cell layout structure discussed in relation to FIG. 8, includes dummy nMOS/pMOS cells that change the configuration of the NP/PP layers in order to exclude corner case abutment of NP, PP, NP, PP four-corner areas. The addition of the dummy nMOS/pMOS cells increases an overall area of the IC.

However, the area utilized by the dummy nMOS/pMOS cells is reduced by reducing a width of the dummy nMOS/pMOS cells as compared the dummy nMOS/pMOS cells in the layout structure discussed in relation to FIG. 6. Further, the n-tap cells are enlarged by the same width reduced from the dummy nMOS/pMOS cells, providing a larger OD area for the nMOS/pMOS device body connections, which may provide some performance improvements in some configurations.

**[0039]** FIG. 9 is a diagram 900 conceptually illustrating a top-view of a third configuration of a dummy cell and tap cell layout structure. In FIG. 9, the dummy nMOS/pMO S cells are reduced in width and the adjacent nMOS/pMOS devices are enlarged in width by the same amount as the reduction in width of the dummy nMOS/pMOS cells. Providing a larger OD area for the active nMOS/pMOS devices may provide some performance improvements in some configurations. The diagram 900 illustrates a MOS IC. The MOS IC includes circuits 990 - 997. The circuit 990 includes a plurality of nMOS devices 902/908, a p-tap cell 904, and a dummy nMOS cell 906. The plurality of nMOS devices 902/908 is spaced apart in a first direction. The p-tap cell 904 and the dummy nMOS cell 906 are adjacent to each other in the first direction between the plurality of nMOS devices 902/908. The p-tap cell 904 is configured to be coupled to a first voltage source. The p-tap cell 904 provides a body connection for the plurality of nMOS devices 902/908. In one example, the first voltage source is configured to provide the voltage Vss.

**[0040]** The circuit 991 includes a plurality of pMOS devices 912/918, a dummy pMOS cell 914, and an n-tap cell 916. Assuming the IC is implemented with a p-type substrate, the circuit 991 is located within an n-well on the p-type substrate. The plurality of pMOS devices 912/918 is adjacent to the plurality of nMOS devices 902/908 in a second direction orthogonal to the first direction. The plurality of pMOS devices 912/918 is spaced apart in the first direction. The dummy pMOS cell 914 and the n-tap cell 916 are adjacent to each other in the first direction between the plurality of pMOS devices 912/918. The n-tap cell 916 is configured to be coupled to a second voltage source. The n-tap cell 916 provides a body connection for the plurality of pMOS devices 912/918. In one example, the second voltage source is configured to provide the voltage Vdd. In this configuration, the p-tap cell 904 is adjacent in the second direction to both the dummy pMOS cell 914 and the pMOS device 912. In addition, the n-tap cell 916 is adjacent in the second direction to both the dummy nMOS cell 906 and the nMOS device 908.

**[0041]** The circuit 992 includes a plurality of nMOS devices 922/928, a p-tap cell 924, and a dummy nMOS cell 926. The plurality of nMOS devices 922/928 is adjacent to the plurality of pMOS devices 912/918 in the second direction. The plurality of nMOS devices 922/928 is spaced apart in the first direction. The p-tap cell 924 and the dummy nMOS cell 926 are adjacent to each other in the first direction between the plurality of nMOS devices 922/928. The p-tap cell 924 is configured to be coupled to the first voltage source. The p-tap cell 924 provides a body connection for the plurality of nMOS devices 922/928. In this configuration, the n-tap cell 916 is adjacent in the second direction to both the dummy nMOS cell 926 and the nMOS device 928. In addition, the p-tap cell 924 is adjacent in the second direction to both the dummy pMOS cell 914 and the pMOS device 912.

**[0042]** The circuit 993 includes a plurality of pMOS devices 932/938, a dummy pMOS cell 934, and an n-tap cell 936. Assuming the IC is implemented with a p-type substrate, the circuit 993 is located within an n-well on the p-type substrate. The plurality of pMOS devices 932/938 is adjacent to the plurality of nMOS devices 922/928 in the second direction. The plurality of pMOS devices 932/938 is spaced apart in the first direction. The dummy pMOS cell 934 and the n-tap cell 936 are adjacent to each other in the first direction between the plurality of pMOS devices 932/938. The n-tap cell 936 is configured to be coupled to the second voltage source. The n-tap cell 936 provides a body connection for the plurality of pMOS devices 932/938. In this configuration, the p-tap cell 924 is adjacent in the second direction to both the dummy pMOS cell 934 and the pMOS device 932. In addition, the n-tap cell 936 is adjacent in the second direction to both the dummy nMOS cell 926 and the nMOS device 928.

**[0043]** The circuit 994 includes a plurality of nMOS devices 942/948, a p-tap cell 944, and a dummy nMOS cell 946. The plurality of nMOS devices 942/948 is adjacent to the plurality of pMOS devices 932/938 in the second direction. The plurality of nMOS devices 942/948 is spaced apart in the first direction. The p-tap cell 944 and the dummy nMOS cell 946 are adjacent to each other in the first direction between the plurality of nMOS devices 942/948. The p-tap cell 944 is configured to be coupled to the first voltage source. The p-tap cell 944 provides a body connection for the plurality of nMOS devices 942/948. In this configuration, the n-tap cell 936 is adjacent in the second direction to both the dummy nMOS cell 946 and the nMOS device 948. In addition, the p-tap cell 944 is adjacent in the second direction to both the dummy pMOS cell 934 and the pMOS device 932.

**[0044]** The circuit 995 includes a plurality of pMOS devices 952/958, a dummy pMOS cell 954, and an n-tap cell 956. Assuming the IC is implemented with a p-type substrate, the circuit 995 is located within an n-well on the p-type substrate. The plurality of pMOS devices 952/958 is adjacent to the plurality of nMOS devices 942/948 in the second direction. The plurality of pMOS devices 952/958 is spaced apart in the first direction. The dummy pMOS cell 954 and the n-tap cell 956 are adjacent to each other in the first direction between the plurality of pMOS devices 952/958. The n-tap cell 956 is configured to be coupled to the second voltage source. The n-tap cell 956 provides a body connection for the plurality of pMOS devices 952/958. In this configuration,

the p-tap cell 944 is adjacent in the second direction to both the dummy pMOS cell 954 and the pMOS device 952. In addition, the n-tap cell 956 is adjacent in the second direction to both the dummy nMOS cell 946 and the nMOS device 948.

**[0045]** The circuit 996 includes a plurality of nMOS devices 962/968, a p-tap cell 964, and a dummy nMOS cell 966. The plurality of nMOS devices 962/968 is adjacent to the plurality of pMOS devices 952/958 in the second direction. The plurality of nMOS devices 962/968 is spaced apart in the first direction. The p-tap cell 964 and the dummy nMOS cell 966 are adjacent to each other in the first direction between the plurality of nMOS devices 962/968. The p-tap cell 964 is configured to be coupled to the first voltage source. The p-tap cell 964 provides a body connection for the plurality of nMOS devices 962/968. In this configuration, the n-tap cell 956 is adjacent in the second direction to both the dummy nMOS cell 966 and the nMOS device 968. In addition, the p-tap cell 964 is adjacent in the second direction to both the dummy pMOS cell 954 and the pMOS device 952.

**[0046]** The circuit 997 includes a plurality of pMOS devices 972/978, a dummy pMOS cell 974, and an n-tap cell 976. Assuming the IC is implemented with a p-type substrate, the circuit 997 is located within an n-well on the p-type substrate. The plurality of pMOS devices 972/978 is adjacent to the plurality of nMOS devices 962/968 in the second direction. The plurality of pMOS devices 972/978 is spaced apart in the first direction. The dummy pMOS cell 974 and the n-tap cell 976 are adjacent to each other in the first direction between the plurality of pMOS devices 972/978. The n-tap cell 976 is configured to be coupled to the second voltage source. The n-tap cell 976 provides a body connection for the plurality of pMOS devices 972/978. In this configuration, the p-tap cell 964 is adjacent in the second direction to both the dummy pMOS cell 974 and the pMOS device 972. In addition, the n-tap cell 976 is adjacent in the second direction to both the dummy nMOS cell 966 and the nMOS device 968.

**[0047]** The dummy nMOS cells 906, 926, 946, 966 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. Likewise, the dummy pMOS cells 914, 934, 954, 974 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. The second voltage source, for example Vdd, may be configured to provide a higher voltage than the first voltage source, for example Vss. As can be appreciated in FIG. 9, an area of each of the p-tap cells 904, 924, 944, 964 is greater than an area of each of the dummy nMO S cells 906, 926, 946, 966. In addition, an area of each of the n-tap cells 916, 936, 956, 976 is greater than an area of each of the dummy pMOS cells 914, 934, 954, 974. OD regions (shown in FIG. 4 by the inner rectangle within each device/cell; may also be referred to as OD islands in this case) of the p-tap cells 904, 924, 944, 964; the dummy nMOS cells 906, 926, 946, 966; the dummy pMOS cells 914, 934, 954, 974; and the n-tap cells 916, 936, 956, 976 are separate and discontinuous with respect to each other.

**[0048]** The dummy cell and tap cell layout structure discussed in relation to FIG. 9, includes dummy nMOS/pMOS cells that change the configuration of the NP/PP layers in order to exclude corner case abutment of NP, PP, NP, PP four-corner areas. The addition of the dummy nMOS/pMOS cells increases an overall area of the IC. However, the area utilized by the dummy nMOS/pMOS cells is reduced by reducing a width of the dummy nMOS/pMOS cells as compared the dummy nMOS/pMOS cells in the layout structure discussed in relation to FIG. 6. Further, the adjacent nMOS/pMOS devices are enlarged by the same width reduced from the dummy nMOS/pMOS cells, providing a larger OD area for the nMOS/pMOS devices, which may provide some performance improvements in some configurations.

**[0049]** The dummy cell and layout structure discussed in relation to FIGs. 8, 9, avoids the corner case abutment of NP, PP, NP, PP four-corner areas, but the implant is unbalanced, as evidenced by the 2nd and 3rd columns of dummy/tap cells having a jagged boundary of the NP/PP layers. Having an unbalanced implant may potentially cause manufacturing yield issues. An alternative configuration is provided with respect to FIG. 10 that provides a balanced implant while also avoiding the corner case abutment of NP, PP, NP, PP four-corner areas.

**[0050]** FIG. 10 is a diagram 1000 conceptually illustrating a top-view of a fourth configuration of a dummy cell and tap cell layout structure. In FIG. 10, the dummy nMOS cells have a continuous OD region with adjacent nMOS devices, and the dummy pMOS cells have a continuous OD region with adjacent pMOS devices. Providing for a continuous OD region of the active devices and dummy nMOS/pMO S cells may also provide some performance improvements in some configurations, as the active devices may have more OD area to utilize for performing the designed functions without taking up space for diffusion breaks. The MOS IC includes circuits 1090 - 1097. The circuit 1090 includes a plurality of nMOS devices 1002/1008, a p-tap cell 1004, and a dummy nMOS cell 1006. The plurality of nMOS devices 1002/1008 is spaced apart in a first direction. The p-tap cell 1004 and the dummy nMOS cell 1006 are adjacent to each other in the first direction between the plurality of nMOS devices 1002/1008. The p-tap cell 1004 is configured to be coupled to a first voltage source. The p-tap cell 1004 provides a body connection for the plurality of nMOS devices 1002/1008. In one example, the first voltage source is configured to provide the voltage Vss. The nMOS device 1008 and the dummy nMOS cell 1006 have a continuous OD region in the first direction.

**[0051]** The circuit 1091 includes a plurality of pMOS devices 1012/1018, a dummy pMOS cell 1014, and an n-tap cell 1016. Assuming the IC is implemented with a p-type substrate, the circuit 1091 is located within an n-well on the p-type substrate. The plurality of pMOS devices

1012/1018 is adjacent to the plurality of nMOS devices 1002/1008 in a second direction orthogonal to the first direction. The plurality of pMOS devices 1012/1018 is spaced apart in the first direction. The dummy pMOS cell 1014 and the n-tap cell 1016 are adjacent to each other in the first direction between the plurality of pMOS devices 1012/1018. The n-tap cell 1016 is configured to be coupled to a second voltage source. The n-tap cell 1016 provides a body connection for the plurality of pMOS devices 1012/1018. In one example, the second voltage source is configured to provide the voltage Vdd. The p-tap cell 1004 and the dummy pMOS cell 1014 are adjacent to each other in the second direction. The dummy nMOS cell 1006 and the n-tap cell 1016 are adjacent to each other in the second direction. The pMOS device 1012 and the dummy pMOS cell 1014 have a continuous OD region in the first direction.

**[0052]** The circuit 1092 includes a plurality of nMOS devices 1022/1028, a p-tap cell 1024, and a dummy nMOS cell 1026. The plurality of nMOS devices 1022/1028 is adjacent to the plurality of pMOS devices 1012/1018 in the second direction. The plurality of nMOS devices 1022/1028 is spaced apart in the first direction. The p-tap cell 1024 and the dummy nMOS cell 1026 are adjacent to each other in the first direction between the plurality of nMOS devices 1022/1028. The p-tap cell 1024 is configured to be coupled to the first voltage source. The p-tap cell 1024 provides a body connection for the plurality of nMOS devices 1022/1028. The dummy pMOS cell 1014 and the p-tap cell 1024 are adjacent to each other in the second direction. The n-tap cell 1016 and the dummy nMOS cell 1026 are adjacent to each other in the second direction. The nMOS device 1028 and the dummy nMOS cell 1026 have a continuous OD region in the first direction.

**[0053]** The circuit 1093 includes a plurality of pMOS devices 1032/1038, a dummy pMOS cell 1034, and an n-tap cell 1036. Assuming the IC is implemented with a p-type substrate, the circuit 1093 is located within an n-well on the p-type substrate. The plurality of pMOS devices 1032/1038 is adjacent to the plurality of nMOS devices 1022/1028 in the second direction. The plurality of pMOS devices 1032/1038 is spaced apart in the first direction. The dummy pMOS cell 1034 and the n-tap cell 1036 are adjacent to each other in the first direction between the plurality of pMOS devices 1032/1038. The n-tap cell 1036 is configured to be coupled to the second voltage source. The n-tap cell 1036 provides a body connection for the plurality of pMOS devices 1032/1038. The p-tap cell 1024 and the dummy pMOS cell 1034 are adjacent to each other in the second direction. The dummy nMOS cell 1026 and the n-tap cell 1036 are adjacent to each other in the second direction. The pMOS device 1032 and the dummy pMOS cell 1034 have a continuous OD region in the first direction.

**[0054]** The circuit 1094 includes a plurality of nMOS devices 1042/1048, a p-tap cell 1044, and a dummy nMOS cell 1046. The plurality of nMOS devices 1042/1048 is adjacent to the plurality of pMOS devices 1032/1038 in the second direction. The plurality of nMOS devices 1042/1048 is spaced apart in the first direction. The p-tap cell 1044 and the dummy nMOS cell 1046 are adjacent to each other in the first direction between the plurality of nMOS devices 1042/1048. The p-tap cell 1044 is configured to be coupled to the first voltage source. The p-tap cell 1044 provides a body connection for the plurality of nMOS devices 1042/1048. The dummy pMOS cell 1034 and the p-tap cell 1044 are adjacent to each other in the second direction. The n-tap cell 1036 and the dummy nMOS cell 1046 are adjacent to each other in the second direction. The nMOS device 1048 and the dummy nMOS cell 1046 have a continuous OD region in the first direction.

**[0055]** The circuit 1095 includes a plurality of pMOS devices 1052/1058, a dummy pMOS cell 1054, and an n-tap cell 1056. Assuming the IC is implemented with a p-type substrate, the circuit 1095 is located within an n-well on the p-type substrate. The plurality of pMOS devices 1052/1058 is adjacent to the plurality of nMOS devices 1042/1048 in the second direction. The plurality of pMOS devices 1052/1058 is spaced apart in the first direction. The dummy pMOS cell 1054 and the n-tap cell 1056 are adjacent to each other in the first direction between the plurality of pMOS devices 1052/1058. The n-tap cell 1056 is configured to be coupled to the second voltage source. The n-tap cell 1056 provides a body connection for the plurality of pMOS devices 1052/1058. The p-tap cell 1044 and the dummy pMOS cell 1054 are adjacent to each other in the second direction. The dummy nMOS cell 1046 and the n-tap cell 1056 are adjacent to each other in the second direction. The pMOS device 1052 and the dummy pMOS cell 1054 have a continuous OD region in the first direction.

**[0056]** The circuit 1096 includes a plurality of nMOS devices 1062/1068, a p-tap cell 1064, and a dummy nMOS cell 1066. The plurality of nMOS devices 1062/1068 is adjacent to the plurality of pMOS devices 1052/1058 in the second direction. The plurality of nMOS devices 1062/1068 is spaced apart in the first direction. The p-tap cell 1064 and the dummy nMOS cell 1066 are adjacent to each other in the first direction between the plurality of nMOS devices 1062/1068. The p-tap cell 1064 is configured to be coupled to the first voltage source. The p-tap cell 1064 provides a body connection for the plurality of nMOS devices 1062/1068. The dummy pMOS cell 1054 and the p-tap cell 1064 are adjacent to each other in the second direction. The n-tap cell 1056 and the dummy nMOS cell 1066 are adjacent to each other in the second direction. The nMOS device 1068 and the dummy nMOS cell 1066 have a continuous OD region in the first direction.

**[0057]** The circuit 1097 includes a plurality of pMOS devices 1072/1078, a dummy pMOS cell 1074, and an n-tap cell 1076. Assuming the IC is implemented with a p-type substrate, the circuit 1097 is located within an n-well on the p-type substrate. The plurality of pMOS devices

1072/1078 is adjacent to the plurality of nMOS devices 1062/1068 in the second direction. The plurality of pMOS devices 1072/1078 is spaced apart in the first direction. The dummy pMOS cell 1074 and the n-tap cell 1076 are adjacent to each other in the first direction between the plurality of pMOS devices 1072/1078. The n-tap cell 1076 is configured to be coupled to the second voltage source. The n-tap cell 1076 provides a body connection for the plurality of pMOS devices 1072/1078. The p-tap cell 1064 and the dummy pMOS cell 1074 are adjacent to each other in the second direction. The dummy nMOS cell 1066 and the n-tap cell 1076 are adjacent to each other in the second direction. The pMOS device 1072 and the dummy pMOS cell 1074 have a continuous OD region in the first direction.

**[0058]** The dummy nMOS cells 1006, 1026, 1046, 1066 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. Likewise, the dummy pMOS cells 1014, 1034, 1054, 1074 may be configured to be floating, coupled to the first voltage source, or coupled to the second voltage source. The second voltage source, for example Vdd, may be configured to provide a higher voltage than the first voltage source, for example Vss. OD regions for each dummy nMOS/pMOS cell in each circuit 1090 - 1097 is continuous with the OD region of the adjacent nMOS/pMOS device in the first direction. Accordingly, each dummy nMOS cell has a continuous OD region with the corresponding adjacent nMOS device, and each dummy pMOS cell has a continuous OD region with the corresponding adjacent pMOS device.

**[0059]** The dummy cell and tap cell layout structure discussed in relation to FIG. 10, includes dummy nMOS/pMOS cells that change the configuration of the NP/PP layers in order to exclude corner case abutment of NP, PP, NP, PP four-corner areas. The addition of the dummy nMOS/pMOS cells increases an overall area of the IC. However, the area utilized by the dummy nMOS/pMOS cells is reduced as compared to the dummy cell and tap cell layout structure in FIG. 6 through the use of continuous OD regions for the dummy cells and adjacent active devices. Accordingly, the dummy cell and tap cell layout structure of FIG. 10 may provide a larger OD area for the nMOS/pMO S devices due to the absence of diffusion breaks than that provided by FIG. 6, and the larger OD area for the nMOS/pMOS devices may provide some performance improvements in some configurations.

**[0060]** FIG. 11 is a third diagram 1100 conceptually illustrating a top-view of a dummy cell and tap cell layout structure. Each of the plurality of nMOS devices in a circuit may include $n$ rows of nMOS devices, where $n \geq 1$, and each of the plurality of pMOS devices in a circuit may include $m$ rows of pMOS devices, where $m \geq 1$. In one example, $m$ may be equal to $n$. In addition, each p-tap cell in a circuit may include $n$ rows of p-tap cells, and each dummy nMOS cell may include n rows of dummy nMOS cells. Further, each dummy pMOS cell may include $m$ rows of dummy pMOS cells, and each n-tap cell may include $m$ rows of n-tap cells. Referring to FIGs. 4, 5, $m$=2 and n=2. Referring to FIGs. 6 - 10, each circuit of nMOS devices, p-tap cell, and dummy nMOS cell includes n rows, and each circuit of pMOS devices, n-tap cell, and dummy pMOS cell includes $m$ rows. In one example, $m$ is equal to $n$ for FIGs. 6 - 10. However, $m$ and $n$ may be unequal in other configurations.

**[0061]** Referring again to FIGs. 6-11, a MOS IC includes a first circuit (694, 894, 994, 1094) including a first plurality of nMOS devices (642/648, 842/848, 942/948, 1042/1048), a first p-tap cell (644, 844, 944, 1044), and a first dummy nMOS cell (646, 846, 946, 1046). The first plurality of nMOS devices (642/648, 842/848, 942/948, 1042/1048) is spaced apart in a first direction. The first p-tap cell (644, 844, 944, 1044) and the first dummy nMOS cell (646, 846, 946, 1046) are adjacent to each other in the first direction between the first plurality of nMOS devices (642/648, 842/848, 942/948, 1042/1048). The first p-tap cell (644, 844, 944, 1044) is configured to be coupled to a first voltage source. The MOS IC further includes a second circuit (695, 895, 995, 1095) including a first plurality of pMOS devices (652/658, 852/858, 952/958, 1052/1058), a first dummy pMOS cell (654, 854, 954, 1054), and a first n-tap cell (656, 856, 956, 1056). The first plurality of pMOS devices (652/658, 852/858, 952/958, 1052/1058) is adjacent to the first plurality of nMOS devices (642/648, 842/848, 942/948, 1042/1048) in a second direction orthogonal to the first direction. The first plurality of pMOS devices (652/658, 852/858, 952/958, 1052/1058) is spaced apart in the first direction. The first dummy pMOS cell (654, 854, 954, 1054) and the first n-tap cell (656, 856, 956, 1056) are adjacent to each other in the first direction between the first plurality of pMOS devices (652/658, 852/858, 952/958, 1052/1058). The first n-tap cell (656, 856, 956, 1056) is configured to be coupled to a second voltage source. The first p-tap cell (644, 844, 944, 1044) and the first dummy pMOS cell (654, 854, 954, 1054) are adjacent to each other in the second direction. The first dummy nMOS cell (646, 846, 946, 1046) and the first n-tap cell (656, 856, 956, 1056) are adjacent to each other in the second direction.

**[0062]** In one configuration, the MOS IC may further include a third circuit (696, 896, 996, 1096) including a second plurality of nMOS devices (662/668, 862/868, 962/968, 1062/1068), a second p-tap cell (664, 864, 964, 1064), and a second dummy nMOS cell (666, 866, 966, 1066). The second plurality of nMOS devices (662/668, 862/868, 962/968, 1062/1068) is spaced apart in the first direction. The second plurality of nMOS devices (662/668, 862/868, 962/968, 1062/1068) is adjacent to the first plurality of pMOS devices (652/658, 852/858, 952/958, 1052/1058) in the second direction. The second p-tap cell (664, 864, 964, 1064) and the second dummy nMOS cell (666, 866, 966, 1066) are adjacent to each other in the first direction between the second plurality of nMOS devices (662/668, 862/868,

962/968, 1062/1068). The first dummy pMOS cell (654, 854, 954, 1054) and the second p-tap cell (664, 864, 964, 1064) are adjacent to each other in the second direction. The first n-tap cell (656, 856, 956, 1056) and the second dummy nMOS cell (666, 866, 966, 1066) are adjacent to each other in the second direction. The second p-tap cell (664, 864, 964, 1064) is configured to be coupled to the first voltage source.

**[0063]** In one configuration, the first plurality of nMOS devices (642/648) includes a first set of nMOS devices (642) and a second set of nMOS devices (648). The first plurality of pMOS devices (652/658) includes a first set of pMOS devices (652) and a second set of pMOS devices (658). The second plurality of nMOS devices (662/668) includes a third set of nMOS devices (662) and a fourth set of nMOS devices (668). The second set of nMOS devices (648), the first dummy nMOS cell (646), the first n-tap cell (656), the second dummy nMOS cell (666), and the fourth set of nMOS devices (668) form an n-type C-shape (702) on the MOS IC with the second set of pMOS devices (658) located within the n-type C-shape (702). Note that the NP/PP layers form C-shapes 702, 704, 706, 708 in each of the configurations in association with FIGs. 6, 8, 9, 10.

**[0064]** In one configuration, the MOS IC may further include a fourth circuit (697, 897, 997, 1097) including a second plurality of pMOS devices (672/678, 872/878, 972/978, 1072/1078), a second dummy pMOS cell (674, 874, 974, 1074), and a second n-tap cell (676, 776, 876, 976). The second plurality of pMOS devices (672/678, 872/878, 972/978, 1072/1078) is spaced apart in the first direction. The second plurality of pMOS devices (672/678, 872/878, 972/978, 1072/1078) is adjacent to the second plurality of nMOS devices (662/668, 862/868, 962/968, 1062/1068) in the second direction. The second dummy pMOS cell (674, 874, 974, 1074) and the second n-tap cell (676, 776, 876, 976) are adjacent to each other in the first direction between the second plurality of pMOS devices (672/678, 872/878, 972/978, 1072/1078). The second p-tap cell (664, 864, 964, 1064) and the second dummy pMOS cell (674, 874, 974, 1074) are adjacent to each other in the second direction. The second dummy nMOS cell (666, 866, 966, 1066) and the second n-tap cell (676, 776, 876, 976) are adjacent to each other in the second direction. The second n-tap cell (676, 776, 876, 976) is configured to be coupled to the second voltage source.

**[0065]** In one configuration, the first plurality of nMOS devices (642/648) includes a first set of nMOS devices (642) and a second set of nMOS devices (648). The first plurality of pMOS devices (652/658) includes a first set of pMOS devices (652) and a second set of pMOS devices (658). The second plurality of nMOS devices (662/668) includes a third set of nMOS devices (662) and a fourth set of nMOS devices (668). The second plurality of pMOS devices (672/678) includes a third set of pMOS devices (672) and a fourth set of pMOS devices (678). The second set of nMOS devices (648), the first dummy nMOS cell (646), the first n-tap cell (656), the second dummy nMOS cell (666), and the fourth set of nMOS devices (668) form an n-type C-shape (702) on the MOS IC with the second set of pMOS devices (658) located within the n-type C-shape (702), The first set of pMOS devices (652), the first dummy pMOS cell (654), the second p-tap cell (664), the second dummy pMOS cell (674), and the third set of pMOS devices (672) form a p-type C-shape (704) on the MOS IC with the third set of nMOS devices (662) located within the p-type C-shape (704). Note that the NP/PP layers form C-shapes 702, 704, 706, 708 in each of the configurations in association with FIGs. 6, 8, 9, 10.

**[0066]** In one configuration, the MOS IC further includes a third circuit including a second plurality ofpMOS devices (632/638, 832/838, 932/938, 1032/1038), a second dummy pMOS cell (634, 834, 934, 1034), and a second n-tap cell (636, 836, 936, 1036). The second plurality of pMOS devices (632/638, 832/838, 932/938, 1032/1038) is spaced apart in the first direction. The second plurality of pMOS devices (632/638, 832/838, 932/938, 1032/1038) is adjacent to the first plurality of nMOS devices (642/648, 842/848, 942/948, 1042/1048) in the second direction. The second dummy pMOS cell (634, 834, 934, 1034) and the second n-tap cell (636, 836, 936, 1036) are adjacent to each other in the first direction between the second plurality of pMOS devices (632/638, 832/838, 932/938, 1032/1038). The first p-tap cell (644, 844, 944, 1044) and the second dummy pMOS cell (634, 834, 934, 1034) are adjacent to each other in the second direction. The first dummy nMOS cell (646, 846, 946, 1046) and the second n-tap cell (636, 836, 936, 1036) are adjacent to each other in the second direction. The second n-tap cell (636, 836, 936, 1036) is configured to be coupled to the second voltage source.

**[0067]** In one configuration, the first plurality of nMOS devices (642/648) includes a first set of nMOS devices (642) and a second set of nMOS devices (648). The first plurality of pMOS devices (652/658) includes a first set of pMOS devices (652) and a second set of pMOS devices (658). The second plurality ofpMOS devices (632/638) includes a third set of pMOS devices (632) and a fourth set of pMOS devices (638). The first set of pMOS devices (652), the first dummy pMOS cell (654), the first p-tap cell (644), the second dummy pMOS cell (634), and the third set of pMOS devices (632) form a p-type C-shape (708) on the MOS IC with the first set of nMOS devices (642) located within the p-type C-shape (708). Note that the NP/PP layers form C-shapes 702, 704, 706, 708 in each of the configurations in association with FIGs. 6, 8, 9, 10.

**[0068]** In one configuration, the MOS IC further includes a fourth circuit including a second plurality of nMOS devices (622/628, 822/828, 922/928, 1022/1028), a second p-tap cell (624, 824, 924, 1024), and a second dummy nMOS cell (626, 826, 926, 1026). The second plurality of nMOS devices (622/628, 822/828, 922/928, 1022/1028) is spaced apart in the first direction. The second plurality of nMOS devices

(622/628, 822/828, 922/928, 1022/1028) is adjacent to the second plurality of pMOS devices (632/638, 832/838, 932/938, 1032/1038) in the second direction. The second p-tap cell (624, 824, 924, 1024) and the second dummy nMOS cell (626, 826, 926, 1026) are adjacent to each other in the first direction between the second plurality of nMOS devices (622/628, 822/828, 922/928, 1022/1028). The second p-tap cell (624, 824, 924, 1024) and the second dummy pMOS cell (634, 834, 934, 1034) are adjacent to each other in the second direction. The second dummy nMOS cell (626, 826, 926, 1026) and the second n-tap cell (636, 836, 936, 1036) are adjacent to each other in the second direction. The second p-tap cell (624, 824, 924, 1024) is configured to be coupled to the first voltage source.

**[0069]** In one configuration, the first plurality of nMOS devices (642/648) includes a first set of nMOS devices (642) and a second set of nMOS devices (648). The first plurality of pMOS devices (652/658) includes a first set of pMOS devices (652) and a second set of pMOS devices (658). The second plurality of pMOS devices (632/638) includes a third set of pMOS devices (632) and a fourth set of pMOS devices (638). The second plurality of nMOS devices (622/628) includes a third set of nMOS devices (622) and a fourth set of nMOS devices (628). The first set of pMOS devices (652), the first dummy pMOS cell (654), the first p-tap cell (644), the second dummy pMOS cell (634), and the third set of pMOS devices (632) form a p-type C-shape (708) on the MOS IC with the first set of nMOS devices (642) located within the p-type C-shape (708). The second set of nMOS devices (648), the first dummy nMOS cell (646), the second n-tap cell (636), the second dummy nMOS cell (626), and the fourth set of nMOS devices (628) form an n-type C-shape (706) on the MOS IC with the fourth set of pMOS devices (638) located within the n-type C-shape (706). Note that the NP/PP layers form C-shapes 702, 704, 706, 708 in each of the configurations in association with FIGs. 6, 8, 9, 10.

**[0070]** In one configuration, the first dummy nMOS cell (646, 846, 946, 1046) is configured to be one of floating, coupled to the first voltage source, and coupled to the second voltage source. In one configuration, the first dummy pMOS cell (654, 854, 954, 1054) is configured to be one of floating, coupled to the first voltage source, and coupled to the second voltage source.

**[0071]** Referring to FIG. 6, in one configuration, an area of each of the first p-tap cell (644), the first dummy nMOS cell (646), the first dummy pMOS cell (654), and the first n-tap cell (656) is approximately equal.

**[0072]** Referring to FIGs. 8, 9, in one configuration, an area of the first p-tap cell (844, 944) and the first n-tap cell (856, 956) is greater than an area of the first dummy pMOS cell (854, 954) and the first dummy nMOS cell (846, 946). Referring to FIG. 8, in one configuration, the first plurality of nMOS devices (842/848) are non-adjacent the first dummy pMOS cell (854) and the first n-tap cell (856) in the second direction, and the first plurality of pMOS devices (852/858) are non-adjacent the first p-tap cell (844) and the first dummy nMOS cell (846) in the second direction. Referring to FIG. 9, in one configuration, at least one nMOS device (948) of the first plurality of nMOS devices (942/948) is adjacent to the first n-tap cell (956) in the second direction, and at least one pMOS device (952) of the first plurality of pMOS devices (952/958) is adjacent to the first p-tap cell (944) in the second direction.

**[0073]** Referring to FIG. 10, in one configuration, the first plurality of nMOS devices (1042/1048) includes a first set of nMOS devices (1042) and a second set of nMOS devices (1048), and the first dummy nMOS cell (1046) and the second set of nMOS devices (1048) have a continuous OD region in the first direction.

**[0074]** Referring to FIGs. 6 - 9, in one configuration, the first plurality of nMOS devices (642/648, 842/848, 942/948) includes a first set of nMOS devices (642, 842, 942) and a second set of nMOS devices (648, 848, 948), and an OD region of the first dummy nMOS cell (646, 846, 946) and an OD region of the second set of nMOS devices (648, 848, 948) are discontinuous in the first direction with respect to each other.

**[0075]** Referring to FIG. 10, in one configuration, the first plurality of pMOS devices (1052/1058) includes a first set of pMOS devices (1052) and a second set of pMOS devices (1058), and the first set of pMOS devices (1052) and the first dummy pMOS cell (1054) have a continuous OD region in the first direction.

**[0076]** Referring to FIGs. 6 - 9, in one configuration, the first plurality of pMOS devices (652/658, 852/858, 952/958) includes a first set of pMOS devices (652, 852, 952) and a second set of pMOS devices (658, 858, 958), and an OD region of the first set of pMOS devices (652, 852, 952) and an OD region of the first dummy pMOS cell (654, 854, 954) are discontinuous in the first direction with respect to each other.

**[0077]** In one configuration, the second voltage source is higher than the first voltage source.

**[0078]** In one configuration, the first plurality of nMOS devices (642/648, 842/848, 942/948, 1042/1048) includes a first set of nMOS devices (642, 842, 942, 1042) and a second set of nMOS devices (648, 848, 948, 1048). As illustrated in FIG. 11, the first set of nMOS devices (642, 842, 942, 1042) and the second set of nMOS devices (648, 848, 948, 1048) each includes $n$ rows of nMOS devices, where $n \geq 1$. The first plurality of pMOS devices (652/658, 852/858, 952/958, 1052/1058) includes a first set of pMOS devices (652, 852, 952, 1052) and a second set of pMOS devices (658, 858, 958, 1058). As illustrated in FIG. 11, the first set of pMOS devices (652, 852, 952, 1052) and the second set of pMOS devices (658, 858, 958, 1058) each includes $m$ rows of pMOS devices, where $m \geq 1$. In one configuration, $m$ is equal to $n$.

**[0079]** In one configuration, the first p-tap cell (644, 844, 944, 1044) includes n rows of p-tap cells, and the first dummy nMOS cell (646, 846, 946, 1046) includes n rows of dummy nMOS cells. In one configuration, the first

dummy pMOS cell (654, 854, 954, 1054) includes *m* rows of dummy pMOS cells, and the first n-tap cell (656, 856, 956, 1056) includes *m* rows of n-tap cells.

**[0080]** As discussed above, for some fabrication processes, DRC violations may be encountered at four-corner areas where, clockwise or counterclockwise, NP, PP, NP, PP layers meet at one corner with 90° edges. With respect to FIGs. 4 - 11, multiple configurations of a dummy cell and tap cell layout structure are provided that avoid the corner case abutment DRC violations. Each of the multiple configurations of the dummy cell and tap cell layout structure include dummy nMOS/pMOS cells that, while increasing an overall size of the IC, also provide NP/PP layers in a configuration that avoid the corner case abutment DRC violations. By avoiding the corner case abutment DRC violations, yield/performance may be improved of corresponding fabricated MOS ICs.

**[0081]** It is understood that the specific order or hierarchy of steps in the processes disclosed is an illustration of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged. Further, some steps may be combined or omitted. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

**[0082]** The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless specifically so stated, but rather "one or more." The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects." Unless specifically stated otherwise, the term "some" refers to one or more. Combinations such as "at least one of A, B, or C," "at least one of A, B, and C," and "A, B, C, or any combination thereof' include any combination of A, B, and/or C, and may include multiples of A, multiples of B, or multiples of C. Specifically, combinations such as "at least one of A, B, or C," "at least one of A, B, and C," and "A, B, C, or any combination thereof' may be A only, B only, C only, A and B, A and C, B and C, or A and B and C, where any such combinations may contain one or more member or members of A, B, or C. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. No claim element is to be construed as a means plus function unless the element is expressly recited using the phrase "means for."

## Claims

**1.** A metal oxide semiconductor, MOS, integrated circuit, IC, comprising:

a first circuit including a first plurality of n-type MOS, nMOS, devices (410), a first p-type tap, p-tap, cell (420), and a first dummy nMOS cell (422), the first plurality of nMOS devices being spaced apart in a first direction, the first p-tap cell (420) and the first dummy nMOS cell (422) being adjacent to each other in the first direction between the first plurality of nMOS devices (410), the first p-tap cell (420) being configured to be coupled to a first voltage source; and
a second circuit including a first plurality of p-type MOS, pMOS, devices (412), a first dummy pMOS cell (424), and a first n-type tap, n-tap, cell (426), the first plurality of pMOS devices (412) being adjacent to the first plurality of nMOS devices (410) in a second direction orthogonal to the first direction, the first plurality of pMOS devices (412) being spaced apart in the first direction, the first dummy pMOS cell (424) and the first n-tap cell (426) being adjacent to each other in the first direction between the first plurality of pMOS devices (412), the first n-tap cell (426) being configured to be coupled to a second voltage source,

**characterised in that**

the first p-tap cell (420) and the first dummy pMOS cell (424) are adjacent to each other in the second direction, and **in that**
the first dummy nMOS cell (422) and the first n-tap cell (426) are adjacent to each other in the second direction.

**2.** The MOS IC of claim 1, further comprising a third circuit (696) including a second plurality of nMOS devices (662/668), a second p-tap cell (664), and a second dummy nMOS cell (666), wherein the second plurality of nMOS devices is spaced apart in the first direction, the second plurality of nMOS devices is adjacent to the first plurality of pMOS devices in the second direction, the second p-tap cell and the second dummy nMOS cell are adjacent to each other in the first direction between the second plurality of nMOS devices, the first dummy pMOS cell and the second p-tap cell are adjacent to each other in the second direction, the first n-tap cell and the second dummy nMOS cell are adjacent to each other in the second direction, and the second p-tap cell is configured to be coupled to the first voltage source.

**3.** The MOS IC of claim 2, wherein the first plurality of nMOS devices comprises a first set of nMOS devices

(642) and a second set of nMOS devices (648), the first plurality of pMOS devices comprises a first set of pMOS devices (652) and a second set of pMOS devices (658), and the second plurality of nMOS devices comprises a third set of nMOS devices (662) and a fourth set of nMOS devices (668), and wherein the second set of nMOS devices, the first dummy nMOS cell, the first n-tap cell, the second dummy nMOS cell, and the fourth set of nMOS devices form an n-type C-shape on the MOS IC with the second set of pMOS devices located within the n-type C-shape.

**4.** The MOS IC of claim 2, further comprising a fourth circuit (697) including a second plurality of pMOS devices (672, 678), a second dummy pMOS cell (674), and a second n-tap cell (676), wherein the second plurality of pMOS devices is spaced apart in the first direction, the second plurality of pMOS devices is adjacent to the second plurality of nMOS devices in the second direction, the second dummy pMOS cell and the second n-tap cell are adjacent to each other in the first direction between the second plurality of pMOS devices, the second p-tap cell and the second dummy pMOS cell are adjacent to each other in the second direction, the second dummy nMOS cell and the second n-tap cell are adjacent to each other in the second direction, and the second n-tap cell is configured to be coupled to the second voltage source.

**5.** The MOS IC of claim 4, wherein the first plurality of nMOS devices comprises a first set of nMOS devices (642) and a second set of nMOS devices (648), the first plurality of pMOS devices comprises a first set of pMOS devices (652) and a second set of pMOS devices (658), the second plurality of nMOS devices comprises a third set of nMOS devices (662) and a fourth set of nMOS devices (668), and the second plurality of pMOS devices comprises a third set of pMOS devices (672) and a fourth set of pMOS devices (678), and wherein the second set of nMOS devices, the first dummy nMOS cell, the first n-tap cell, the second dummy nMOS cell, and the fourth set of nMOS devices form an n-type C-shape on the MOS IC with the second set of pMOS devices located within the n-type C-shape, and wherein the first set of pMOS devices, the first dummy pMOS cell, the second p-tap cell, the second dummy pMOS cell, and the third set of pMOS devices form a p-type C-shape on the MOS IC with the third set of nMOS devices located within the p-type C-shape.

**6.** The MOS IC of claim 1, further comprising a third circuit including a second plurality of pMOS devices (632, 638), a second dummy pMOS cell (634), and a second n-tap cell (636), wherein the second plurality of pMOS devices is spaced apart in the first direction, the second plurality of pMOS devices is adjacent to the first plurality of nMOS devices in the second direction, the second dummy pMOS cell and the second n-tap cell are adjacent to each other in the first direction between the second plurality of pMOS devices, the first p-tap cell and the second dummy pMOS cell are adjacent to each other in the second direction, the first dummy nMOS cell and the second n-tap cell are adjacent to each other in the second direction, and the second n-tap cell is configured to be coupled to the second voltage source.

**7.** The MOS IC of claim 6, wherein the first plurality of nMOS devices comprises a first set of nMOS devices (642) and a second set of nMOS devices (648), the first plurality of pMOS devices comprises a first set of pMOS devices (652) and a second set of pMOS devices (658), and the second plurality of pMOS devices comprises a third set of pMOS devices (632) and a fourth set of pMOS devices (638), and wherein the first set of pMOS devices, the first dummy pMOS cell, the first p-tap cell, the second dummy pMOS cell, and the third set of pMOS devices form a p-type C-shape on the MOS IC with the first set of nMOS devices located within the p-type C-shape.

**8.** The MOS IC of claim 6, further comprising a fourth circuit including a second plurality of nMOS devices (622, 628), a second p-tap cell (624), and a second dummy nMOS cell (626), wherein the second plurality of nMOS devices is spaced apart in the first direction, the second plurality of nMOS devices is adjacent to the second plurality of pMOS devices in the second direction, the second p-tap cell and the second dummy nMOS cell are adjacent to each other in the first direction between the second plurality of nMOS devices, the second p-tap cell and the second dummy pMOS cell are adjacent to each other in the second direction, the second dummy nMOS cell and the second n-tap cell are adjacent to each other in the second direction, and the second p-tap cell is configured to be coupled to the first voltage source; and wherein the first plurality of nMOS devices comprises a first set of nMOS devices 2. (642) and a second set of nMOS devices (648), the first plurality of pMOS devices comprises a first set of pMOS devices (652) and a second set of pMOS devices (658), the second plurality of pMOS devices comprises a third set of pMOS devices (632) and a fourth set of pMOS devices (638), and the second plurality of nMOS devices comprises a third set of nMOS devices (622) and a fourth set of nMOS devices (628), and wherein the first set of pMOS devices, the first dummy pMOS cell, the first p-tap cell, the second dummy pMOS cell, and the third set of pMOS devices form a p-type C-shape on the MOS IC with the first set of nMOS devices located within the p-type C-shape, and wherein the second set of nMOS

devices, the first dummy nMOS cell, the second n-tap cell, the second dummy nMOS cell, and the fourth set of nMOS devices form an n-type C-shape on the MOS IC with the fourth set of pMOS devices located within the n-type C-shape.

**9.** The MOS IC of claim 1, wherein the first dummy nMOS cell is configured to be one of floating, coupled to the first voltage source, and coupled to the second voltage source; or wherein the first dummy pMOS cell is configured to be one of floating, coupled to the first voltage source, and coupled to the second voltage source; or
wherein an area of each of the first p-tap cell, the first dummy nMOS cell, the first dummy pMOS cell, and the first n-tap cell is approximately equal.

**10.** The MOS IC of claim 1, wherein an area of the first p-tap cell and the first n-tap cell is greater than an area of the first dummy pMOS cell and the first dummy nMOS cell.

**11.** The MOS IC of claim 10, wherein the first plurality of nMOS devices are non-adjacent the first dummy pMOS cell and the first n-tap cell in the second direction, and the first plurality of pMOS devices are non-adjacent the first p-tap cell and the first dummy nMOS cell in the second direction; or
wherein at least one nMOS device of the first plurality of nMOS devices is adjacent to the first n-tap cell in the second direction, and at least one pMOS device of the first plurality of pMOS devices is adjacent to the first p-tap cell in the second direction.

**12.** The MOS IC of claim 1, wherein the first plurality of nMOS devices comprises a first set of nMOS devices (1042) and a second set of nMOS devices (1048), and the first dummy nMOS cell and the second set of nMOS devices have a continuous oxide diffusion, OD, region in the first direction; or

wherein the first plurality of nMOS devices comprises a first set of nMOS devices (642) and a second set of nMOS devices (648), and an oxide diffusion, OD, region of the first dummy nMOS cell and an OD region of the second set of nMOS devices are discontinuous in the first direction with respect to each other; or
wherein the first plurality of pMOS devices comprises a first set of pMOS devices (1052) and a second set of pMOS (1058), and the first set of pMOS devices and the first dummy pMOS cell have a continuous oxide diffusion, OD, region in the first direction; or
wherein the first plurality of pMOS devices comprises a first set of pMOS devices (652) and a second set of pMOS devices (658), and an oxide diffusion, OD, region of the first set of pMOS devices and an OD region of the first dummy pMOS cell are discontinuous in the first direction with respect to each other.

**13.** The MOS IC of claim 1, wherein the second voltage source is adapted to provide a higher voltage than the first voltage source.

**14.** The MOS IC of claim 1, wherein the first plurality of nMOS devices comprises a first set of nMOS devices (642) and a second set of nMOS devices (648), the first set of nMOS devices and the second set of nMOS devices each comprises $n$ rows of nMOS devices, where $n \geq 1$, and wherein the first plurality of pMOS devices comprises a first set of pMOS devices (652) and a second set of pMOS devices (658), the first set of pMOS devices and the second set of pMOS devices each comprises $m$ rows of pMOS devices, where $m \geq 1$.

**15.** The MOS IC of claim 14, wherein $m$ is equal to $n$; or

wherein the first p-tap cell comprises n rows of p-tap cells, and the first dummy nMOS cell comprises n rows of dummy nMOS cells; or
wherein the first dummy pMOS cell comprises $m$ rows of dummy pMOS cells, and the first n-tap cell comprises $m$ rows of n-tap cells.

**Patentansprüche**

**1.** Ein MOS-IC (MOS = metal oxide semiconductor bzw. Metalloxid-Halbleiter, IC = integrated circuit bzw. integrierter Schaltkreis), der Folgendes aufweist:

eine erste Schaltung, die eine erste Vielzahl von n-Typ-MOS-Einrichtungen bzw. nMOS-Einrichtungen (410), eine erste p-Typ-Abgriff-Zelle bzw. p-Tap-Zelle (420) und eine erste Dummy-nMOS-Zelle (422) aufweist, wobei die erste Vielzahl von nMOS-Einrichtungen in einer ersten Richtung voneinander beabstandet ist, wobei die erste p-Tap-Zelle (420) und die erste Dummy-nMOS-Zelle (422) in der ersten Richtung zueinander benachbart bzw. angrenzend zwischen der ersten Vielzahl von nMOS-Einrichtungen (410) sind, wobei die erste p-Tap-Zelle (420) konfiguriert ist an die erste Spannungsquelle gekoppelt zu werden; und
eine zweite Schaltung, die eine erste Vielzahl von p-Typ-MOS-Einrichtungen bzw. pMOS-Einrichtungen (412), eine erste Dummy-pMOS-Zelle (424) und eine erste n-Typ-Abgriff-Zelle bzw. n-Tap-Zelle (426) aufweist, wobei die erste Vielzahl von pMOS-Einrichtungen (412) benachbart bzw. angrenzend ist zu der ersten Vielzahl von

NMOS-Einrichtungen (410) in einer zweiten Richtung orthogonal zu der ersten Richtung, wobei die erste Vielzahl von pMOS-Einrichtungen (412) in der ersten Richtung voneinander beabstandet ist, wobei die erste Dummy-pMOS-Zelle (424) und die erste n-Tap-Zelle (426) benachbart bzw. angrenzend zueinander in der ersten Richtung zwischen der ersten Vielzahl von pMOS-Einrichtungen (412) sind, wobei die erste n-Tap-Zelle (426) konfiguriert ist an eine zweite Spannungsquelle gekoppelt zu werden, **dadurch gekennzeichnet, dass**
die erste p-Tap-Zelle (420) und die erste Dummy-pMOS-Zelle (424) benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, und dadurch, dass die erste Dummy-nMOS-Zelle (422) und die erste n-Tap-Zelle (426) benachbart bzw. angrenzend zueinander in der zweiten Richtung sind.

**2.** MOS-IC nach Anspruch 1, der weiter eine dritte Schaltung (696) aufweist, die eine zweite Vielzahl von nMOS-Einrichtungen (662/668), eine zweite p-Tap-Zelle (664) und eine zweite Dummy-nMOS-Zelle (666) aufweist, wobei die zweite Vielzahl von nMOS-Einrichtungen voneinander in der ersten Richtung beabstandet ist, die zweite Vielzahl von nMOS-Einrichtungen zu der ersten Vielzahl von pMOS-Einrichtungen in der zweiten Richtung benachbart bzw. angrenzend ist, die zweite p-Tap-Zelle und die zweite Dummy-nMOS-Zelle benachbart bzw. angrenzend zueinander in der ersten Richtung zwischen der zweiten Vielzahl von nMOS-Einrichtungen sind, die erste Dummy-pMOS-Zelle und die zweite p-Tap-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, die erste n-Tap-Zelle und die zweite Dummy-nMOS-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, und die zweite p-Tap-Zelle konfiguriert ist, an die erste Spannungsquelle gekoppelt zu werden.

**3.** MOS-IC nach Anspruch 2, wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (642) und einen zweiten Satz von nMOS-Einrichtungen (648) aufweist, wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (652) und einen zweiten Satz von pMOS-Einrichtung (658) aufweist, und die zweite Vielzahl von nMOS-Einrichtungen einen dritten Satz von nMOS-Einrichtungen (662) und einen vierten Satz von nMOS-Einrichtungen (668) aufweist, und wobei der zweite Satz von nMOS-Einrichtungen, die erste Dummy-nMOS-Zelle, die erste n-Tap-Zelle, die zweite Dummy-nMOS-Zelle und der vierte Satz von nMOS-Einrichtungen eine n-Typ-C-Form auf dem MOS-IC bilden, wobei der zweite Satz von pMOS-Einrichtungen innerhalb der n-Typ-C-Form angeordnet ist.

**4.** MOS-IC nach Anspruch 2, der weiter eine vierte Schaltung (697) aufweist, die eine zweite Vielzahl von pMOS-Einrichtungen (672, 678), eine zweite Dummy-pMOS-Zelle (674) und eine zweite n-Tap-Zelle (676) aufweist, wobei die zweite Vielzahl von pMOS-Einrichtungen voneinander in der ersten Richtung beabstandet ist, wobei die zweite Vielzahl von pMOS-Einrichtungen benachbart bzw. angrenzend ist zu der zweiten Vielzahl von nMOS-Einrichtungen in der zweiten Richtung ist, wobei die zweite Dummy-pMOS-Zelle und die zweite n-Tap-Zelle benachbart bzw. angrenzend zueinander in der ersten Richtung sind zwischen der zweiten Vielzahl von pMOS-Einrichtungen, wobei die zweite p-Tap-Zelle und die zweite Dummy-pMOS-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, wobei die zweite Dummy-nMOS-Zelle und die zweite n-Tap-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, und die zweite n-Tap-Zelle konfiguriert ist an die zweite Spannungsquelle gekoppelt zu werden.

**5.** MOS-IC nach Anspruch 4, wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (642) und einen zweiten Satz von nMOS-Einrichtungen (648) aufweist, wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (652) und einen zweiten Satz von pMOS-Einrichtungen (658) aufweist, wobei die zweite Vielzahl von nMOS-Einrichtungen einen dritten Satz von nMOS-Einrichtungen (662) und einen vierten Satz von nMOS-Einrichtungen (668) aufweist, und die zweite Vielzahl von pMOS-Einrichtungen einen dritten Satz von pMOS-Einrichtungen (672) und einen vierten Satz von pMOS-Einrichtungen (678) aufweist, und wobei der zweite Satz von nMOS-Einrichtungen, die erste Dummy-nMOS-Zelle, die erste n-Tap-Zelle, die zweite Dummy-nMOS-Zelle, und der vierte Satz von nMOS-Einrichtungen eine n-Typ-C-Form auf dem MOS-IC mit dem zweiten Satz von pMOS-Einrichtungen, die innerhalb der n-Typ-C-Form angeordnet sind, bilden und wobei der erste Satz von pMOS-Einrichtungen, die erste Dummy-pMOS-Zelle, die zweite p-Tap-Zelle, die zweite Dummy-pMOS-Zelle und der dritte Satz von pMOS-Einrichtungen eine p-Typ-C-Form auf dem MOS-IC mit dem dritten Satz von nMOS-Einrichtungen, die innerhalb der p-Typ-C-Form angeordnet sind, bilden.

**6.** MOS-IC nach Anspruch 1, der weiter eine dritte Schaltung aufweist, die eine zweite Vielzahl von pMOS-Einrichtungen (632, 638), eine zweite Dummy-pMOS-Zelle (634) und eine zweite n-Tap-Zelle (636) aufweist, wobei die zweite Vielzahl von pMOS-Einrichtungen voneinander in der ersten Richtung

beabstandet ist, die zweite Vielzahl von pMOS-Einrichtungen benachbart bzw. angrenzend zu der ersten Vielzahl von nMOS-Einrichtungen in der zweiten Richtung ist, die zweite Dummy-pMOS-Zelle und die zweite n-Tap-Zelle benachbart bzw. angrenzend zueinander in der ersten Richtung sind zwischen der zweiten Vielzahl von pMOS-Einrichtungen, wobei die erste p-Tap-Zelle und die zweite Dummy-pMOS-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, die erste Dummy-nMOS-Zelle und die zweite n-Tap-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, und die zweite n-Tap-Zelle konfiguriert ist, an die zweite Spannungsquelle gekoppelt zu werden.

**7.** MOS-IC nach Anspruch 6, wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (642) und einen zweiten Satz von nMOS-Einrichtungen (648) aufweist, wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (652) und einen zweiten Satz von pMOS-Einrichtungen (658) aufweist, und die zweite Vielzahl von pMOS-Einrichtungen einen dritten Satz von pMOS-Einrichtungen (632) und einen vierten Satz von pMOS-Einrichtungen (638) aufweist, und wobei der erste Satz von pMOS-Einrichtungen, die erste Dummy-pMOS-Zelle, die erste p-Tap-Zelle, die zweite Dummy-pMOS-Zelle und der dritte Satz von pMOS-Einrichtungen eine p-Typ-C-Form auf dem MOS-IC mit dem ersten Satz von nMOS-Einrichtungen, die innerhalb der p-Typ-C-Form angeordnet sind, bilden.

**8.** MOS-IC nach Anspruch 6, der weiter eine dritte Schaltung aufweist, die eine zweite Vielzahl von nMOS-Einrichtungen (622, 628), eine zweite p-Tap-Zelle (624) und eine zweite Dummy-nMOS-Zelle (626) aufweist, wobei die zweite Vielzahl von nMOS-Einrichtungen in der ersten Richtung beabstandet ist, die zweite Vielzahl von nMOS-Einrichtungen benachbart bzw. angrenzend zu der zweiten Vielzahl von pMOS-Einrichtungen in der zweiten Richtung ist, die zweite p-Tap-Zelle und die zweite Dummy-nMOS-Zelle benachbart bzw. angrenzend zueinander in der ersten Richtung zwischen der zweiten Vielzahl von nMOS-Einrichtungen sind, wobei die zweite p-Tap-Zelle und die zweite Dummy-pMOS-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, wobei die zweite Dummy-nMOS-Zelle und die zweite n-Tap-Zelle benachbart bzw. angrenzend zueinander in der zweiten Richtung sind, und die zweite p-Tap-Zelle konfiguriert ist an die erste Spannungsquelle gekoppelt zu werden; und
wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (642) und einen zweiten Satz von nMOS-Einrichtungen (648) aufweist, wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (652) und einen zweiten Satz von pMOS-Einrichtungen (658) aufweist, wobei die zweite Vielzahl von pMOS-Einrichtungen einen dritten Satz von pMOS-Einrichtungen (632) und einen vierten Satz von pMOS-Einrichtungen (638) aufweist, und die zweite Vielzahl von nMOS-Einrichtungen einen dritten Satz von nMOS-Einrichtungen (622) und einen vierten Satz von nMOS-Einrichtungen (628) aufweist, und wobei der erste Satz von pMOS-Einrichtungen, die erste Dummy-pMOS-Zelle, die erste p-Tap-Zelle, die zweite Dummy-pMOS-Zelle und der dritte Satz von pMOS-Einrichtungen eine p-Typ-C-Form auf dem MOS-IC mit dem ersten Satz von nMOS-Einrichtungen, die innerhalb der p-Typ-C-Form angeordnet sind, bilden, und wobei der zweite Satz von nMOS-Einrichtungen, die erste Dummy-nMOS-Zelle, die zweite n-Tap-Zelle, die zweite Dummy-nMOS-Zelle und der vierte Satz von nMOS-Einrichtungen eine n-Typ-C-Form auf dem MOS-IC mit dem vierten Satz von pMOS-Einrichtungen, die innerhalb der n-Typ-C-Form angeordnet sind, bilden.

**9.** MOS-IC nach Anspruch 1, wobei die erste Dummy-nMOS-Zelle konfiguriert ist, eines von Folgendem zu sein: zu floaten bzw. potenzialfrei zu sein, an die erste Spannungsquelle gekoppelt zu sein, und an die zweite Spannungsquelle gekoppelt zu sein; oder wobei die erste Dummy-pMOS-Zelle konfiguriert ist, eines von Folgendem zu sein: zu floaten bzw. potenzialfrei zu sein, an die erste Spannungsquelle gekoppelt zu sein, und an die zweite Spannungsquelle gekoppelt zu sein; oder wobei eine Fläche bzw. ein Bereich von jedem von der ersten p-Tap-Zelle, der ersten Dummy-nMOS-Zelle, der ersten Dummy-pMOS-Zelle und der ersten n-Tap-Zelle ungefähr gleich ist.

**10.** MOS-IC nach Anspruch 1, wobei ein Bereich der ersten p-Tap-Zelle und der ersten n-Tap-Zelle größer ist als ein Bereich der ersten Dummy-pMOS-Zelle und der ersten Dummy-nMOS-Zelle.

**11.** MOS-IC nach Anspruch 10, wobei die erste Vielzahl von nMOS-Einrichtungen nicht benachbart bzw. nicht angrenzend ist zu der ersten Dummy-pMOS-Zelle und der ersten n-Tap-Zelle in der zweiten Richtung, und die erste Vielzahl von pMOS-Einrichtungen nicht benachbart bzw. angrenzend ist zu der ersten p-Tap-Zelle und der ersten Dummy-nMOS-Zelle in der zweiten Richtung; oder
wobei wenigstens eine nMOS-Einrichtung der ersten Vielzahl von nMOS-Einrichtungen benachbart bzw. angrenzend ist zu der ersten n-Tap-Zelle in der zweiten Richtung, und wenigstens eine pMOS-Einrichtung der ersten Vielzahl von pMOS-Einrich-

tungen benachbart bzw. angrenzend ist zu der ersten p-Tap-Zelle in der zweiten Richtung.

**12.** MOS-IC nach Anspruch 1, wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (1042) und einen zweiten Satz von nMOS-Einrichtungen (1048) aufweist, und die erste Dummy-nMOS-Zelle und der zweite Satz von nMOS-Einrichtungen eine kontinuierliche Oxiddiffusionsregion bzw. OD-Region (OD = oxide diffusion) in der ersten Richtung haben; oder

wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (642) und einen zweiten Satz von nMOS-Einrichtungen (648) aufweist, und eine Oxiddiffusions- bzw. OD-Region der ersten Dummy-nMOS-Zelle und eine OD-Region des zweiten Satzes von nMOS-Einrichtungen diskontinuierlich in der ersten Richtung in Bezug aufeinander sind; oder
wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (1052) und einen zweiten Satz von pMOS (1058) aufweist, und der erste Satz von pMOS-Einrichtungen und die erste Dummy-pMOS-Zelle eine kontinuierliche Oxiddiffusionsregion bzw. OD-Region in der ersten Richtung haben; oder
wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (652) und einen zweiten Satz von pMOS-Einrichtungen (658) aufweist, und eine Oxiddiffusionsregion bzw. OD-Region des ersten Satzes von pMOS-Einrichtungen und eine OD-Region der ersten Dummy-pMOS-Zelle in der ersten Richtung diskontinuierlich in Bezug aufeinander sind.

**13.** MOS-IC nach Anspruch 1, wobei die zweite Spannungsquelle ausgelegt ist eine höhere Spannung vorzusehen als die erste Spannungsquelle.

**14.** MOS-IC nach Anspruch 1, wobei die erste Vielzahl von nMOS-Einrichtungen einen ersten Satz von nMOS-Einrichtungen (642) und einen zweiten Satz von nMOS-Einrichtungen (648) aufweist, wobei der erste Satz von nMOS-Einrichtungen und der zweite Satz von nMOS-Einrichtungen jeweils n Reihen von nMOS-Einrichtungen aufweisen, wobei $n \geq 1$, und wobei die erste Vielzahl von pMOS-Einrichtungen einen ersten Satz von pMOS-Einrichtungen (652) und einen zweiten Satz von pMOS-Einrichtungen (658) aufweist, wobei der erste Satz von pMOS-Einrichtungen und der zweite Satz von pMOS-Einrichtungen jeweils *m* Reihen von pMOS-Einrichtungen aufweisen, wobei $m \geq 1$.

**15.** MOS-IC nach Anspruch 14, wobei *m* gleich *n* ist; oder
wobei die erste p-Tap-Zelle n Reihen von p-Tap-Zellen aufweist, und die erste Dummy-nMOS-Zelle n Reihen von Dummy-nMOS-Zellen aufweist; oder wobei die erste Dummy-pMOS-Zelle *m* Reihen von Dummy-pMOS-Zellen aufweist, und die erste n-Tap-Zelle *m* Reihen von n-Tap-Zellen aufweist.

**Revendications**

**1.** Circuit intégré, IC, à métal oxyde semiconducteur, MOS, comprenant :

un premier circuit comportant une première pluralité de dispositifs MOS de type n, nMOS, (410), une première cellule de prise de type p, prise p, (420) et une première cellule nMOS factice (422), la première pluralité de dispositifs nMOS étant espacés dans une première direction, la première cellule de prise p (420) et la première cellule nMOS factice (422) étant adjacentes l'une à l'autre dans la première direction entre la première pluralité de dispositifs nMOS (410), la première cellule de prise p (420) étant configurée pour être reliée à une première source de tension ; et
un deuxième circuit comportant une première pluralité de dispositifs MOS de type p, pMOS, (412), une première cellule pMOS factice (424) et une première cellule de prise de type n, prise n, (426), la première pluralité de dispositifs pMOS (412) étant adjacente à la première pluralité de dispositifs nMOS (410) dans une deuxième direction orthogonale à la première direction, la première pluralité de dispositifs pMOS (412) étant espacés dans la première direction, la première cellule pMOS factice (424) et la première cellule de prise n (426) étant adjacentes l'une à l'autre dans la première direction entre la première pluralité de dispositifs pMOS (412), la première cellule de prise n (426) étant configurée pour être reliée à une deuxième source de tension,
**caractérisé en ce que**
la première cellule de prise p (420) et la première cellule pMOS factice (424) sont adjacentes l'une à l'autre dans la deuxième direction, et **en ce que**
la première cellule nMOS factice (422) et la première cellule de prise n (426) sont adjacentes les unes aux autres dans la deuxième direction.

**2.** IC à MOS selon la revendication 1, comprenant en outre un troisième circuit (696) comportant une deuxième pluralité de dispositifs nMOS (662/668), une

deuxième cellule de prise p (664) et une deuxième cellule nMOS factice (666), dans lequel la deuxième pluralité de dispositifs nMOS est espacée dans la première direction, la deuxième pluralité de dispositifs nMOS est adjacente à la première pluralité de dispositifs pMOS dans la deuxième direction, la deuxième cellule de prise p et la deuxième cellule nMOS factice sont adjacentes l'une à l'autre dans la première direction entre la deuxième pluralité de dispositifs nMOS, la première cellule pMOS factice et la deuxième cellule de prise p sont adjacentes l'une à l'autre dans la deuxième direction, la première cellule de prise n et la deuxième cellule nMOS factice sont adjacentes l'une à l'autre dans la deuxième direction, et la deuxième cellule de prise p est configurée pour être reliée au première source de tension.

**3.** IC à MOS selon la revendication 2, dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (642) et un deuxième ensemble de dispositifs nMOS (648), la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (652) et un deuxième ensemble de dispositifs pMOS (658), et la deuxième pluralité de dispositifs nMOS comprend un troisième ensemble de dispositifs nMOS (662) et un quatrième ensemble de dispositifs nMOS (668), et dans lequel le deuxième ensemble de dispositifs nMOS, la première cellule nMOS factice, la première cellule de prise n, la deuxième cellule nMOS factice et le quatrième ensemble de dispositifs nMOS forment une forme en C de type n sur le IC à MOS, le deuxième ensemble de dispositifs pMOS étant situé à l'intérieur de la forme en C de type n.

**4.** IC à MOS selon la revendication 2, comprenant en outre un quatrième circuit (697) comportant une deuxième pluralité de dispositifs pMOS (672, 678), une deuxième cellule pMOS factice (674) et une deuxième cellule de prise n (676), dans lequel la deuxième pluralité de dispositifs pMOS est espacée dans la première direction, la deuxième pluralité de dispositifs pMOS est adjacente à la deuxième pluralité de dispositifs nMOS dans la deuxième direction, la deuxième cellule pMOS factice et la deuxième cellule de prise n sont adjacentes l'une à l'autre dans la première direction entre la deuxième pluralité de dispositifs pMOS, la deuxième cellule de prise p et la deuxième cellule pMOS factice sont adjacentes l'une à l'autre dans la deuxième direction, la deuxième cellule nMOS factice et la deuxième cellule de prise n sont adjacentes l'une à l'autre dans la deuxième direction, et la deuxième cellule de prise n est configurée pour être reliée à la deuxième source de tension.

**5.** IC à MOS selon la revendication 4, dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (642) et un deuxième ensemble de dispositifs nMOS (648), la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (652) et un deuxième ensemble de dispositifs pMOS (658), la deuxième pluralité de dispositifs nMOS comprend un troisième ensemble de dispositifs nMOS (662) et un quatrième ensemble de dispositifs nMOS (668), et la deuxième pluralité de dispositifs pMOS comprend un troisième ensemble de dispositifs pMOS (672) et un quatrième ensemble de dispositifs pMOS (678), et dans lequel le deuxième ensemble de dispositifs nMOS, la première cellule factice nMOS, la première cellule de prise n, la deuxième cellule factice nMOS et le quatrième ensemble de dispositifs nMOS forment une forme en C de type n sur l'IC à MOS, le deuxième ensemble de dispositifs pMOS étant situé à l'intérieur de la forme en C de type n, et dans lequel le premier ensemble de dispositifs pMOS, la première cellule factice pMOS, la deuxième cellule de prise p, la deuxième cellule factice pMOS et le troisième ensemble de dispositifs pMOS forment une forme en C de type p sur l'IC à MOS, le troisième ensemble de dispositifs nMOS étant situé à l'intérieur de la forme en C de type p.

**6.** IC à MOS selon la revendication 1, comprenant en outre un troisième circuit comportant une deuxième pluralité de dispositifs pMOS (632, 668), une deuxième cellule pMOS factice (634) et une deuxième cellule de prise n (636), dans lequel la deuxième pluralité de dispositifs pMOS est espacée dans la première direction, la deuxième pluralité de dispositifs pMOS est adjacente à la première pluralité de dispositifs nMOS dans la deuxième direction, la deuxième cellule pMOS factice et la deuxième cellule de prise n sont adjacentes l'une à l'autre dans la première direction entre la deuxième pluralité de dispositifs pMOS, la première cellule de prise p et la deuxième cellule pMOS factice sont adjacentes l'une à l'autre dans la deuxième direction, la première cellule nMOS factice et la deuxième cellule de prise n sont adjacentes l'une à l'autre dans la deuxième direction, et la deuxième cellule de prise n est configurée pour être reliée à la deuxième source de tension.

**7.** IC à MOS selon la revendication 6, dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (642) et un deuxième ensemble de dispositifs nMOS (648), la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (652) et un deuxième ensemble de dispositifs pMOS (658), et la deuxième pluralité de dispositifs pMOS comprend un troisième ensemble de dispositifs pMOS (632) et un quatrième ensemble de dispositifs pMOS (638),

et dans lequel le premier ensemble de dispositifs pMOS, la première cellule pMOS factice, la première cellule de prise p, la deuxième cellule pMOS factice et le troisième ensemble de dispositifs pMOS forment une forme en C de type p sur l'IC à MOS, le premier ensemble de dispositifs nMOS étant situé à l'intérieur de la forme en C de type p.

**8.** IC à MOS selon la revendication 6, comprenant en outre un quatrième circuit comportant une deuxième pluralité de dispositifs nMOS (622, 628), une deuxième cellule de prise p (624) et une deuxième cellule nMOS factice (626), dans lequel la deuxième pluralité de dispositifs nMOS est espacée dans la première direction, la deuxième pluralité de dispositifs nMOS est adjacente à la deuxième pluralité de dispositifs pMOS dans la deuxième direction, la deuxième cellule de prise p et la deuxième cellule nMOS factice sont adjacentes l'une à l'autre dans la première direction entre la deuxième pluralité de dispositifs nMOS, la deuxième cellule de prise p et la deuxième cellule pMOS factice sont adjacentes l'une à l'autre dans la deuxième direction, la deuxième cellule nMOS factice et la deuxième cellule de prise n sont adjacentes l'une à l'autre dans la deuxième direction, et la deuxième cellule de prise p est configurée pour être reliée à la première source de tension ; et
dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (642) et un deuxième ensemble de dispositifs nMOS (648), la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (652) et un deuxième ensemble de dispositifs pMOS (658), la deuxième pluralité de dispositifs pMOS comprend un troisième ensemble de dispositifs pMOS (632) et un quatrième ensemble de dispositifs pMOS (638), et la deuxième pluralité de dispositifs nMOS comprend un troisième ensemble de dispositifs nMOS (622) et un quatrième ensemble de dispositifs nMOS (628), et dans lequel le premier ensemble de dispositifs pMOS, la première cellule pMOS factice, la première cellule de prise p, la deuxième cellule pMOS factice et le troisième ensemble de dispositifs pMOS forment une forme en C de type p sur l'IC à MOS, le premier ensemble de dispositifs nMOS étant situé à l'intérieur de la forme en C de type p, et dans lequel le deuxième ensemble de dispositifs nMOS, la première cellule nMOS factice, la deuxième cellule de prise n, la deuxième cellule nMOS factice et le quatrième ensemble de dispositifs nMOS forment une forme en C de type n sur l'IC à MOS, le quatrième ensemble de dispositifs pMOS étant situé à l'intérieur de la forme en C de type n.

**9.** IC à MOS selon la revendication 1, dans lequel la première cellule nMOS factice est configurée pour être flottante, reliée à la première source de tension et reliée à la deuxième source de tension ; ou

dans lequel la première cellule pMOS factice est configurée pour être flottante, reliée à la première source de tension et reliée à la deuxième source de tension ; ou
dans lequel la surface de chacune parmi la première cellule de prise p, la première cellule nMOS factice, la première cellule pMOS factice et la première cellule de prise n est approximativement égale.

**10.** IC à MOS selon la revendication 1, dans lequel la surface de la première cellule de prise p et de la première cellule de prise n est plus grande que la surface de la première cellule pMOS factice et de la première cellule nMOS factice.

**11.** IC à MOS selon la revendication 10, dans lequel la première pluralité de dispositifs nMOS n'est pas adjacente à la première cellule pMOS factice ni à la première cellule de prise n dans la deuxième direction, et la première pluralité de dispositifs pMOS n'est pas adjacente à la première cellule de prise p ni à la première cellule nMOS factice dans la deuxième direction ; ou
dans lequel au moins un dispositif nMOS de la première pluralité de dispositifs nMOS est adjacent à la première cellule de prise n dans la deuxième direction, et au moins un dispositif pMOS de la première pluralité de dispositifs pMOS est adjacent à la première cellule de prise p dans la deuxième direction.

**12.** IC à MOS selon la revendication 1, dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (1042) et un deuxième ensemble de dispositifs nMOS (1048), et la première cellule nMOS factice et le deuxième ensemble de dispositifs nMOS ont une région de diffusion d'oxyde, OD, continue dans la première direction ; ou

dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (642) et un deuxième ensemble de dispositifs nMOS (648), et une région de diffusion d'oxyde, OD, de la première cellule nMOS factice et une région OD du deuxième ensemble de dispositifs nMOS sont discontinues dans la première direction les unes par rapport aux autres ; ou
dans lequel la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (1052) et un deuxième ensemble de dispositifs pMOS (1058), et le premier ensemble de dispositifs pMOS et la première cellule pMOS factice ont une région de diffusion

d'oxyde, OD, continue dans la première direction ; ou
dans lequel la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (652) et un deuxième ensemble de dispositifs pMOS (658), et une région de diffusion d'oxyde, OD, du premier ensemble de dispositifs pMOS et une région OD de la première cellule pMOS factice sont discontinues dans la première direction l'une par rapport à l'autre.

**13.** IC à MOS selon la revendication 1, dans lequel la deuxième source de tension est adaptée à fournir une tension supérieure à la première source de tension.

**14.** IC à MOS selon la revendication 1, dans lequel la première pluralité de dispositifs nMOS comprend un premier ensemble de dispositifs nMOS (642) et un deuxième ensemble de dispositifs nMOS (648), le premier ensemble de dispositifs nMOS et le deuxième ensemble de dispositifs nMOS comprennent chacun n lignes de dispositifs nMOS, où $n \geq 1$, et dans lequel la première pluralité de dispositifs pMOS comprend un premier ensemble de dispositifs pMOS (652) et un deuxième ensemble de dispositifs pMOS (658), le premier ensemble de dispositifs pMOS et le deuxième ensemble de dispositifs pMOS comprennent chacun m lignes de dispositifs pMOS, où $m \geq 1$.

**15.** IC à MOS selon la revendication 14, dans lequel m est égal à n ; ou

dans lequel la première cellule de prise p comprend n lignes de cellules de prise p, et la première cellule nMOS factice comprend n lignes de cellules nMOS factices ; ou
dans lequel la première cellule pMOS factice comprend m lignes de cellules pMOS factices, et la première cellule de n prises comprend m lignes de cellules de prise n.

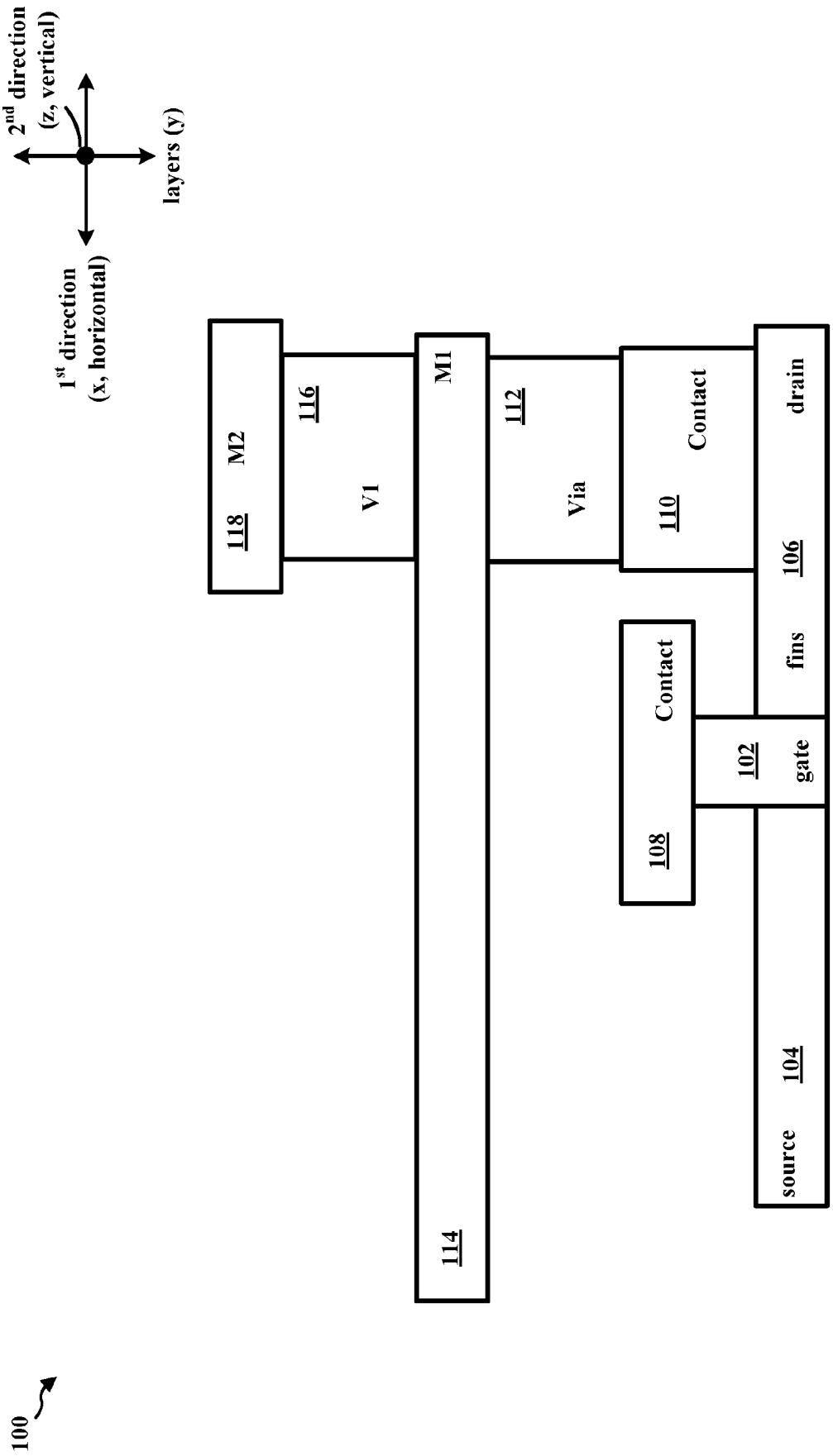

2nd direction
(z, vertical)
layers (y)
1st direction
(x, horizontal)
100
M2
118
116
V1
M1
114
112
Via
Contact
110
drain
106
fins
Contact
108
102
gate
source
104

FIG. 1

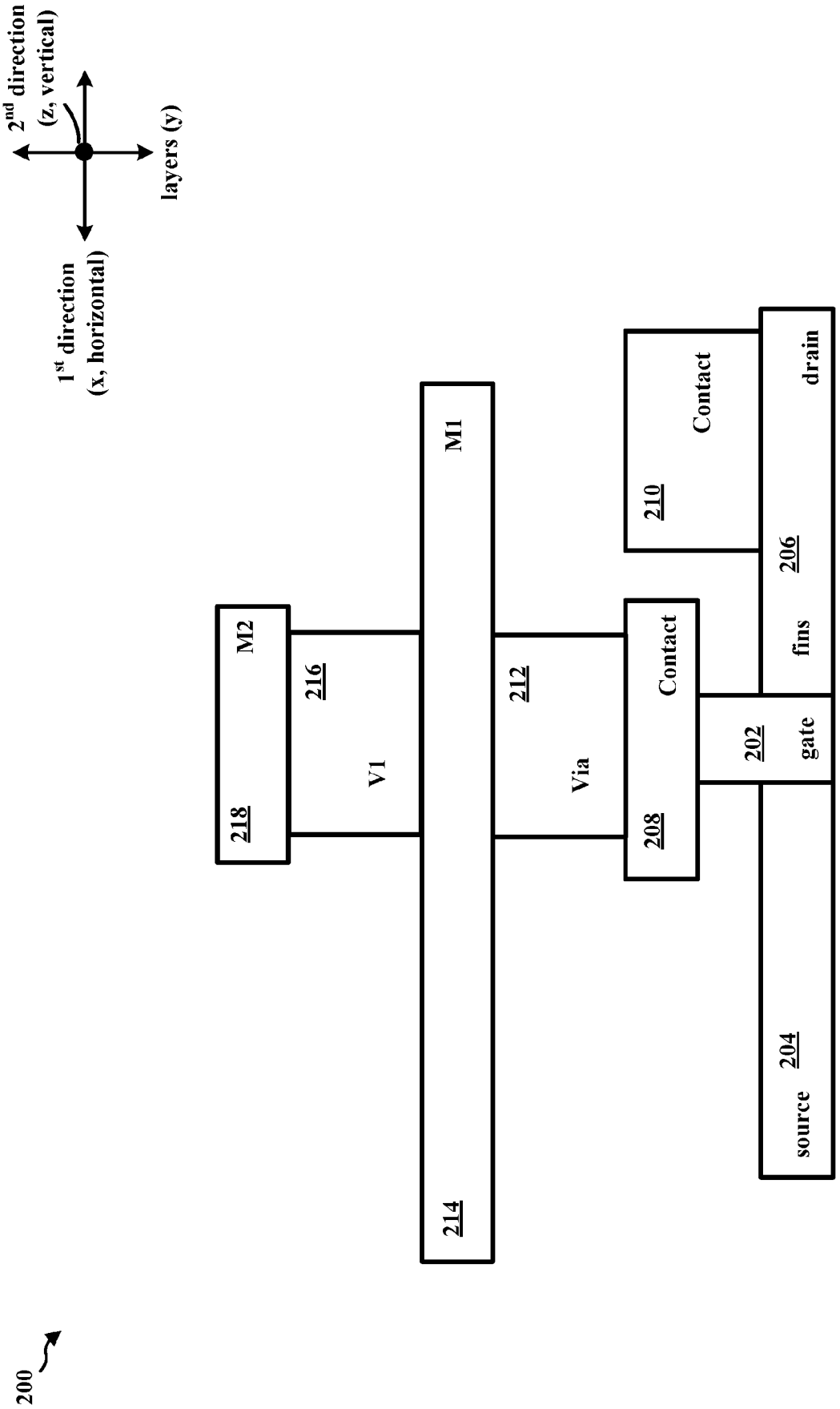

2nd direction
(z, vertical)
layers (y)
1st direction
(x, horizontal)
200
M2
218
216
V1
M1
214
212
Via
Contact
208
Contact
210
drain
206
fins
202
gate
source
204

FIG. 2

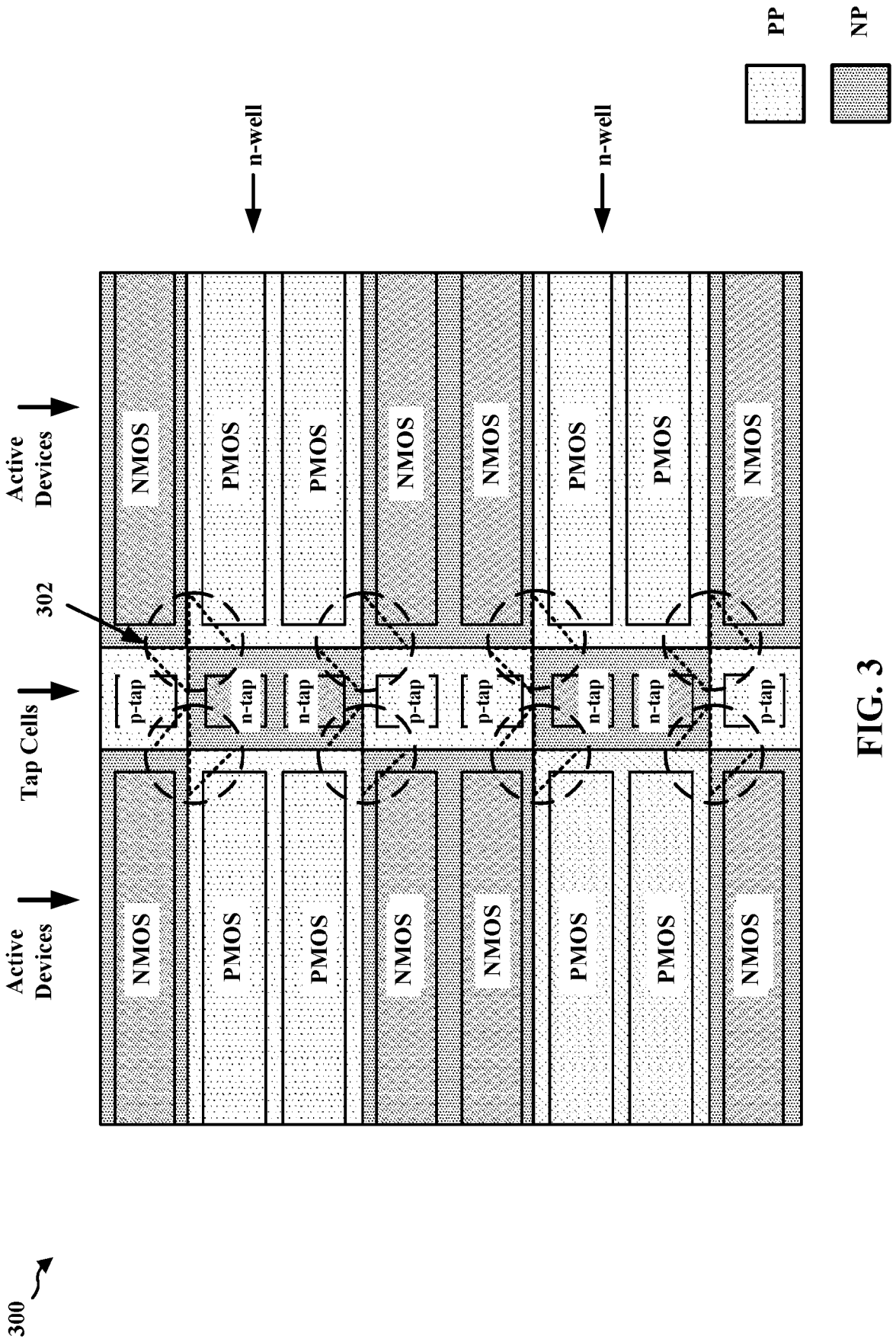

PP
NP
n-well
n-well
Active Devices
Tap Cells
Active Devices
302
300
NMOS
PMOS
p-tap
n-tap

FIG. 3

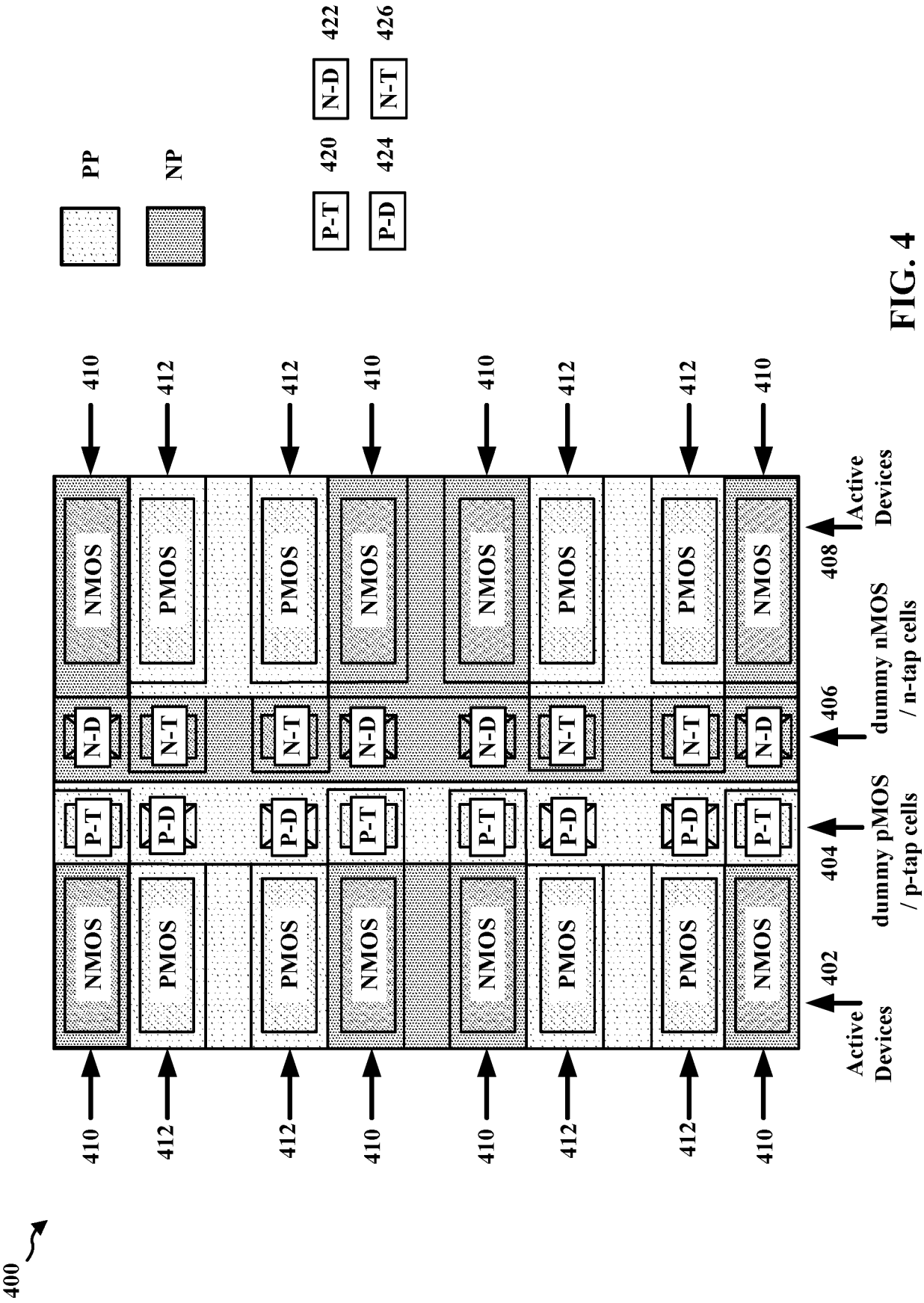

400
410
412
NMOS
PMOS
N-D
N-T
P-T
P-D
402
404
406
408
Active Devices
dummy pMOS / p-tap cells
dummy nMOS / n-tap cells
Active Devices
PP
NP
P-T
420
P-D
424
N-D
422
N-T
426

FIG. 4

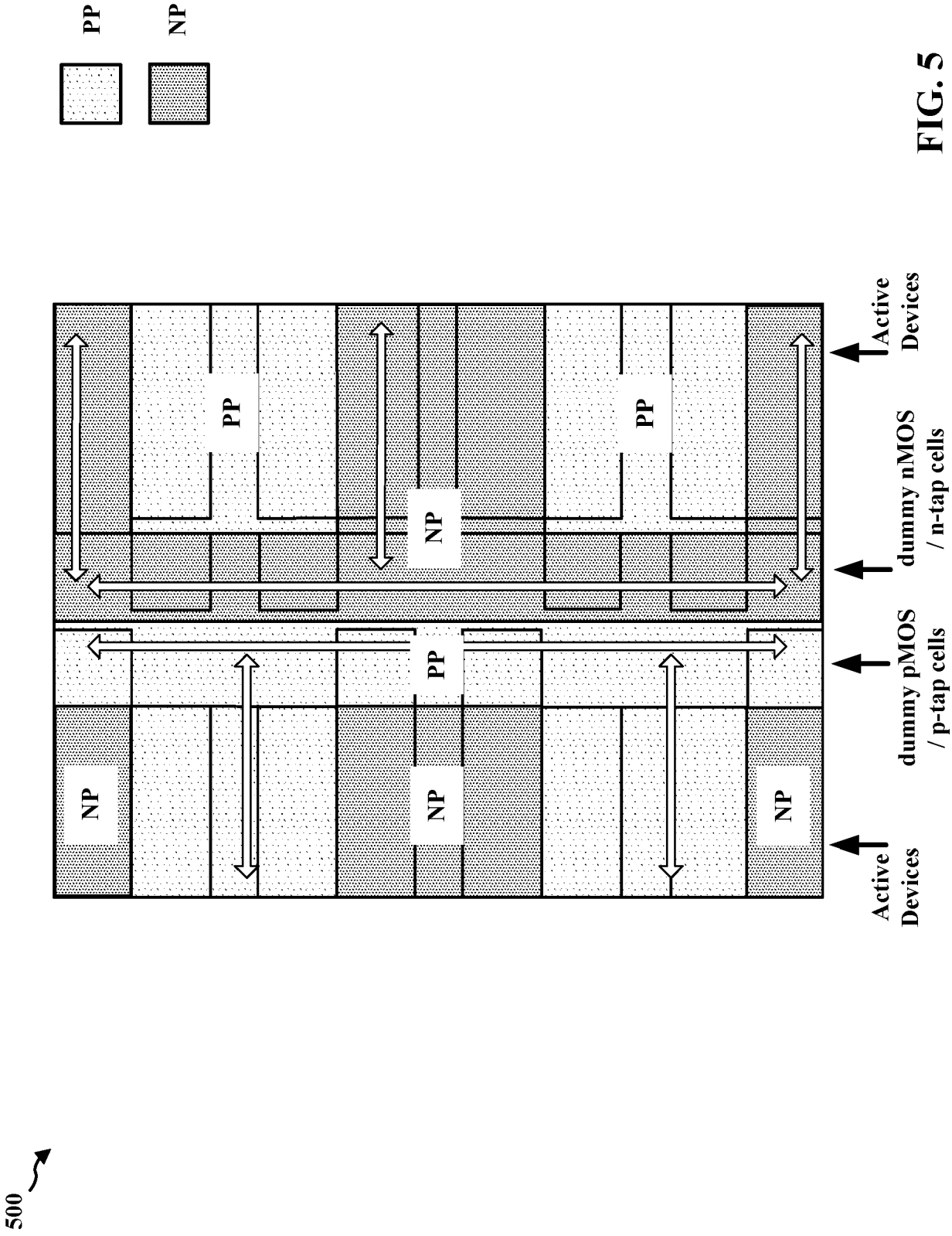

PP
NP
500
Active Devices
dummy pMOS / p-tap cells
dummy nMOS / n-tap cells
Active Devices
NP
PP

FIG. 5

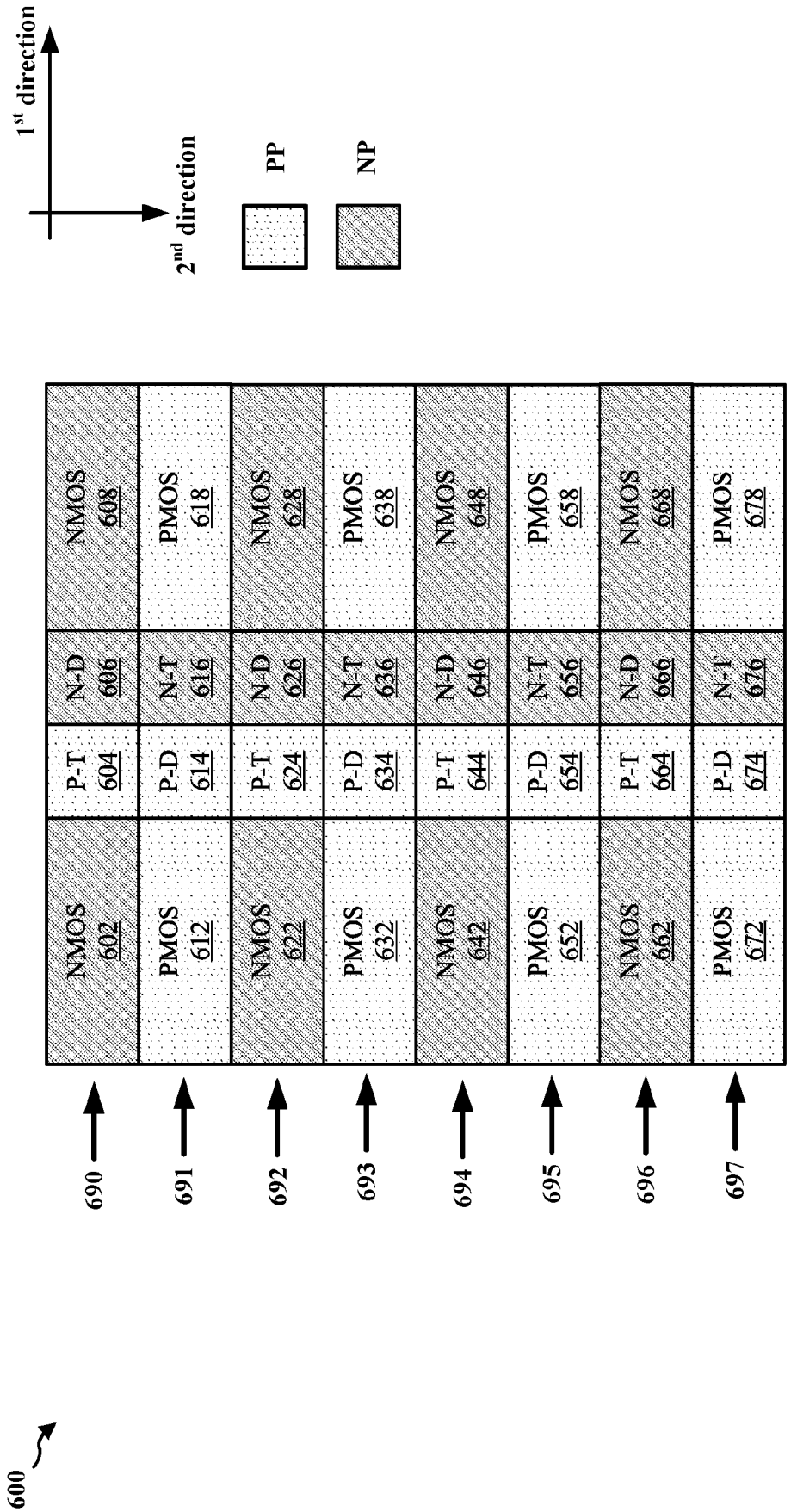

1st direction
2nd direction
PP
NP
600
690
691
692
693
694
695
696
697
NMOS 602
P-T 604
N-D 606
NMOS 608
PMOS 612
P-D 614
N-T 616
PMOS 618
NMOS 622
P-T 624
N-D 626
NMOS 628
PMOS 632
P-D 634
N-T 636
PMOS 638
NMOS 642
P-T 644
N-D 646
NMOS 648
PMOS 652
P-D 654
N-T 656
PMOS 658
NMOS 662
P-T 664
N-D 666
NMOS 668
PMOS 672
P-D 674
N-T 676
PMOS 678

FIG. 6

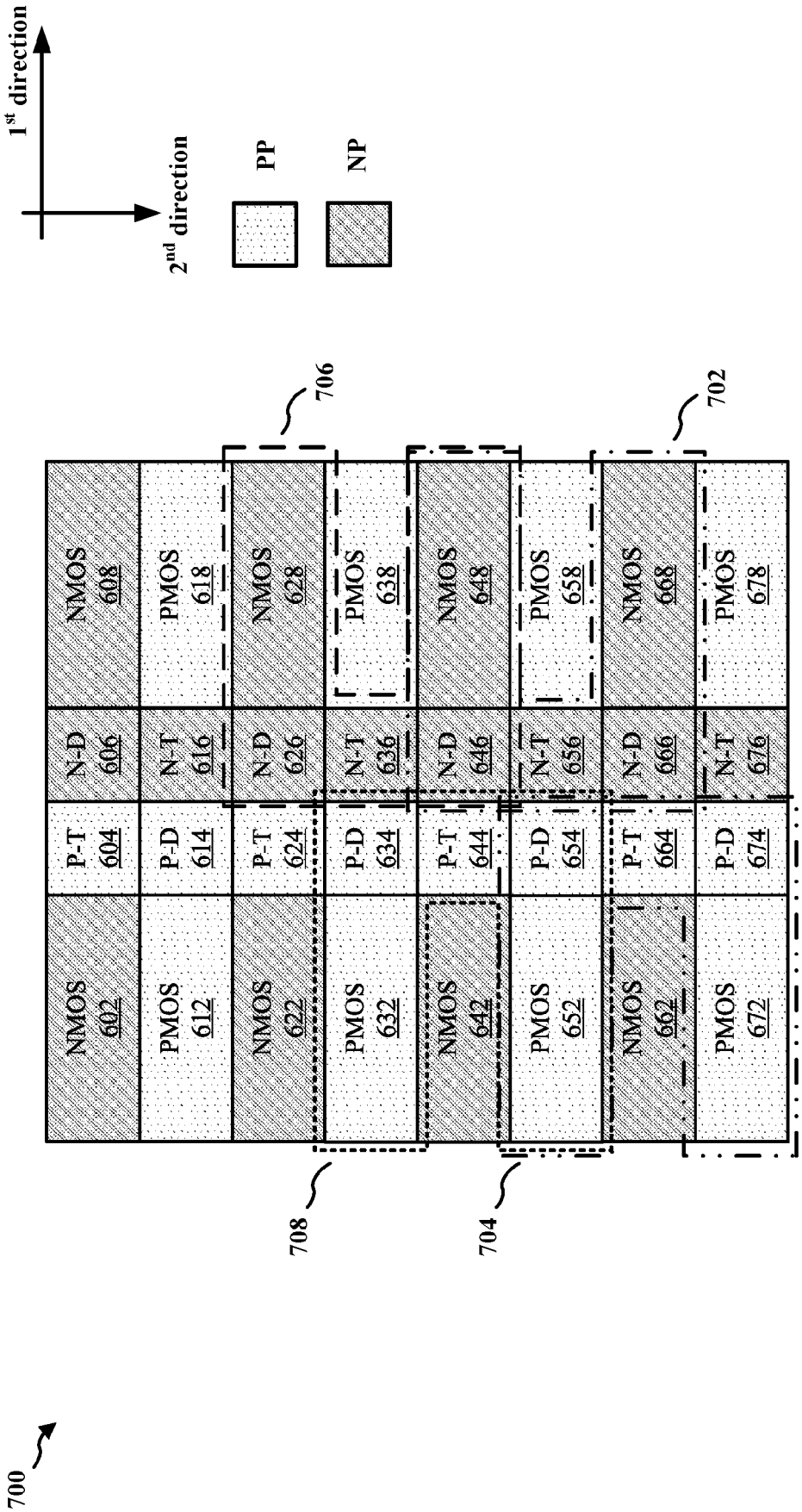
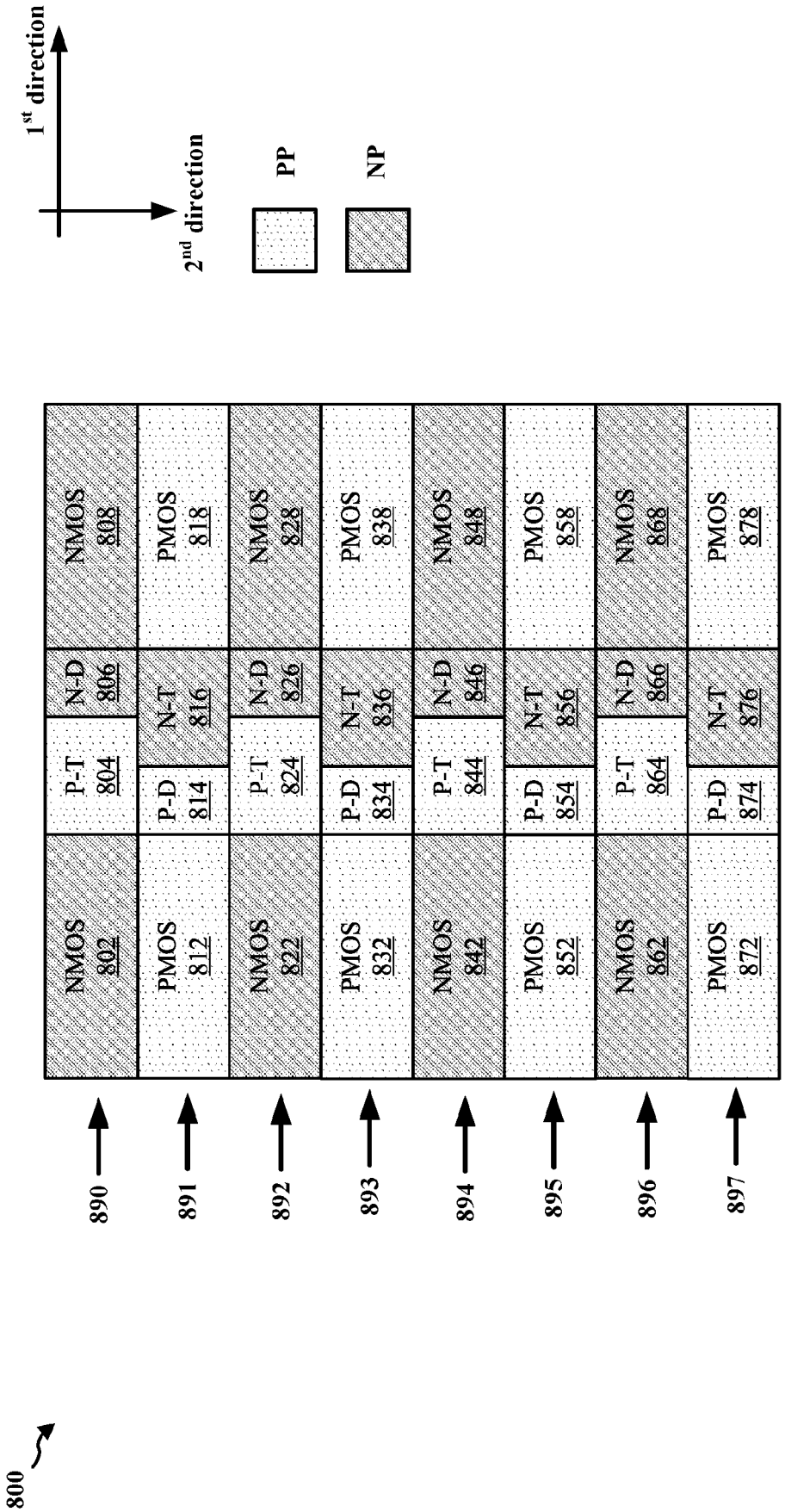

1st direction
2nd direction
PP
NP
700
706
702
708
704
NMOS 602
PMOS 612
NMOS 622
PMOS 632
NMOS 642
PMOS 652
NMOS 662
PMOS 672
P-T 604
P-D 614
P-T 624
P-D 634
P-T 644
P-D 654
P-T 664
P-D 674
N-D 606
N-T 616
N-D 626
N-T 636
N-D 646
N-T 656
N-D 666
N-T 676
NMOS 608
PMOS 618
NMOS 628
PMOS 638
NMOS 648
PMOS 658
NMOS 668
PMOS 678

FIG. 7


1st direction
2nd direction
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NP
NMOS 802
P-T 804
P-D 814
N-T 816
N-D 806
PMOS 812
NMOS 808
PMOS 818
NMOS 822
P-T 824
P-D 834
N-T 836
N-D 826
PMOS 832
NMOS 828
PMOS 838
NMOS 842
P-T 844
P-D 854
N-T 856
N-D 846
PMOS 852
NMOS 848
PMOS 858
NMOS 862
P-T 864
P-D 874
N-T 876
N-D 866
PMOS 872
NMOS 868
PMOS 878
890
891
892
893
894
895
896
897
800

FIG. 8

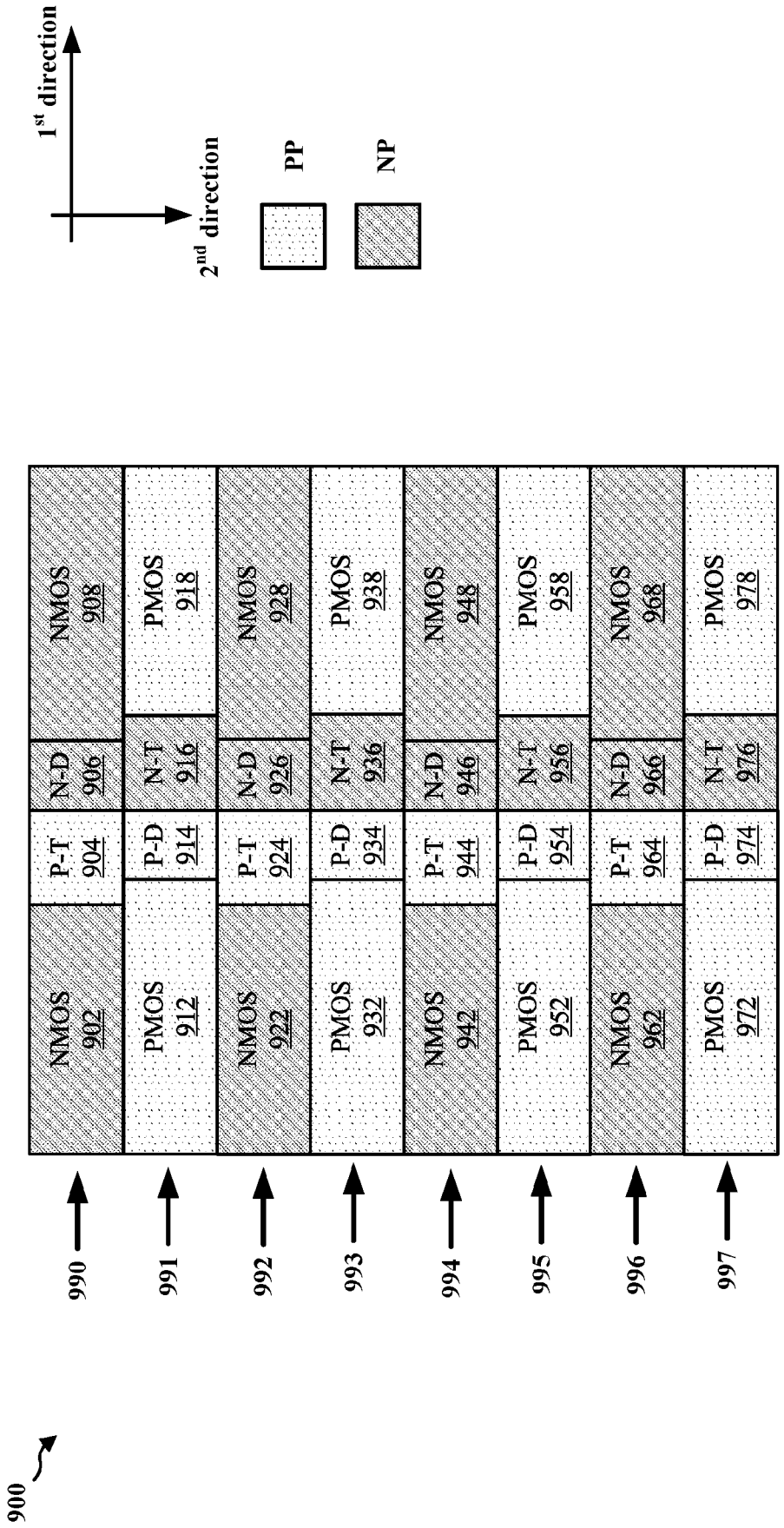
900
990
991
992
993
994
995
996
997
NMOS 902
P-T 904
N-D 906
NMOS 908
PMOS 912
P-D 914
N-T 916
PMOS 918
NMOS 922
P-T 924
N-D 926
NMOS 928
PMOS 932
P-D 934
N-T 936
PMOS 938
NMOS 942
P-T 944
N-D 946
NMOS 948
PMOS 952
P-D 954
N-T 956
PMOS 958
NMOS 962
P-T 964
N-D 966
NMOS 968
PMOS 972
P-D 974
N-T 976
PMOS 978
1st direction
2nd direction
PP
NP

FIG. 9

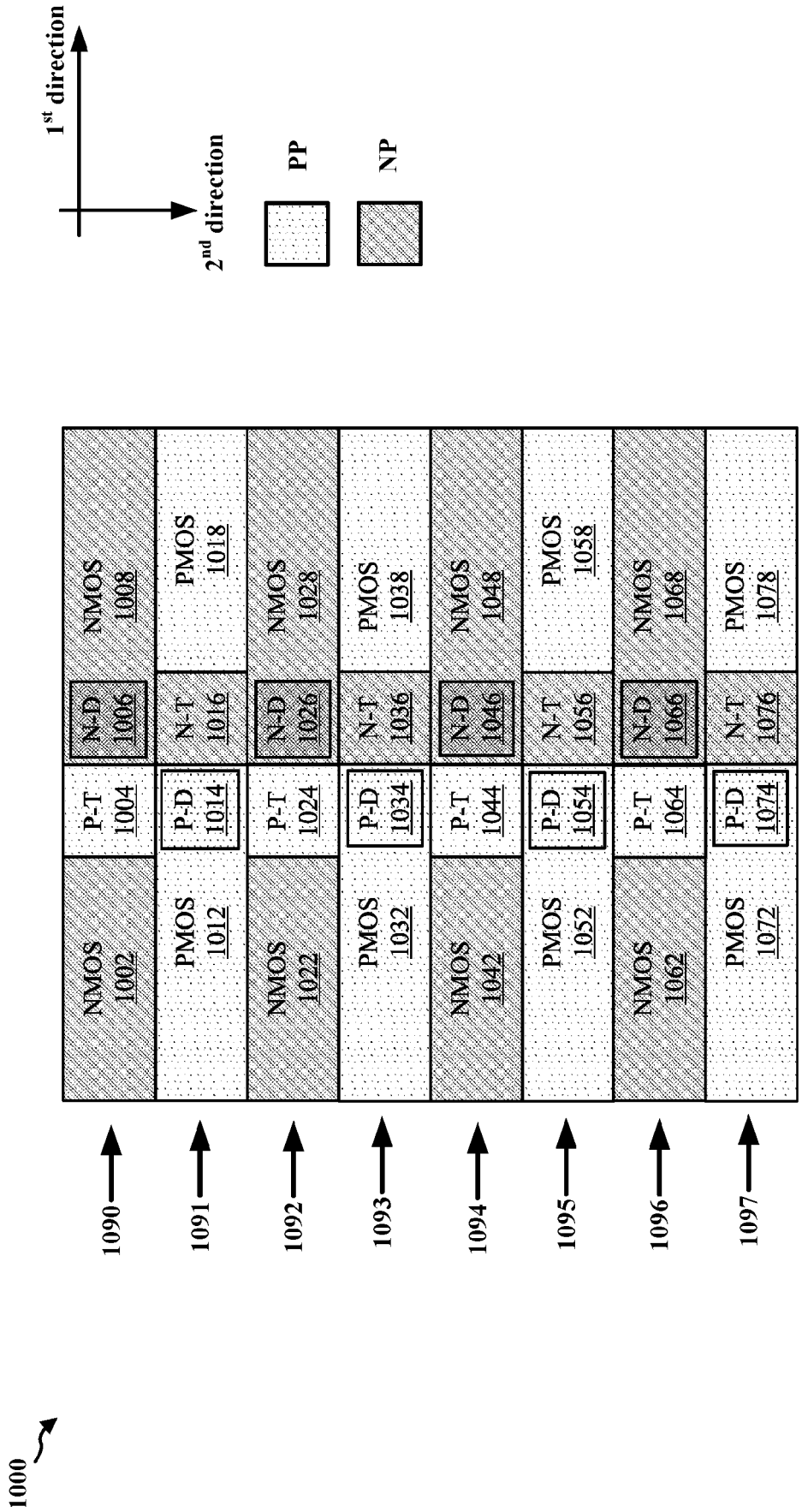
1000
1090
1091
1092
1093
1094
1095
1096
1097
NMOS 1002
P-T 1004
N-D 1006
NMOS 1008
PMOS 1012
P-D 1014
N-T 1016
PMOS 1018
NMOS 1022
P-T 1024
N-D 1026
NMOS 1028
PMOS 1032
P-D 1034
N-T 1036
PMOS 1038
NMOS 1042
P-T 1044
N-D 1046
NMOS 1048
PMOS 1052
P-D 1054
N-T 1056
PMOS 1058
NMOS 1062
P-T 1064
N-D 1066
NMOS 1068
PMOS 1072
P-D 1074
N-T 1076
PMOS 1078
1st direction
2nd direction
PP
NP

FIG. 10

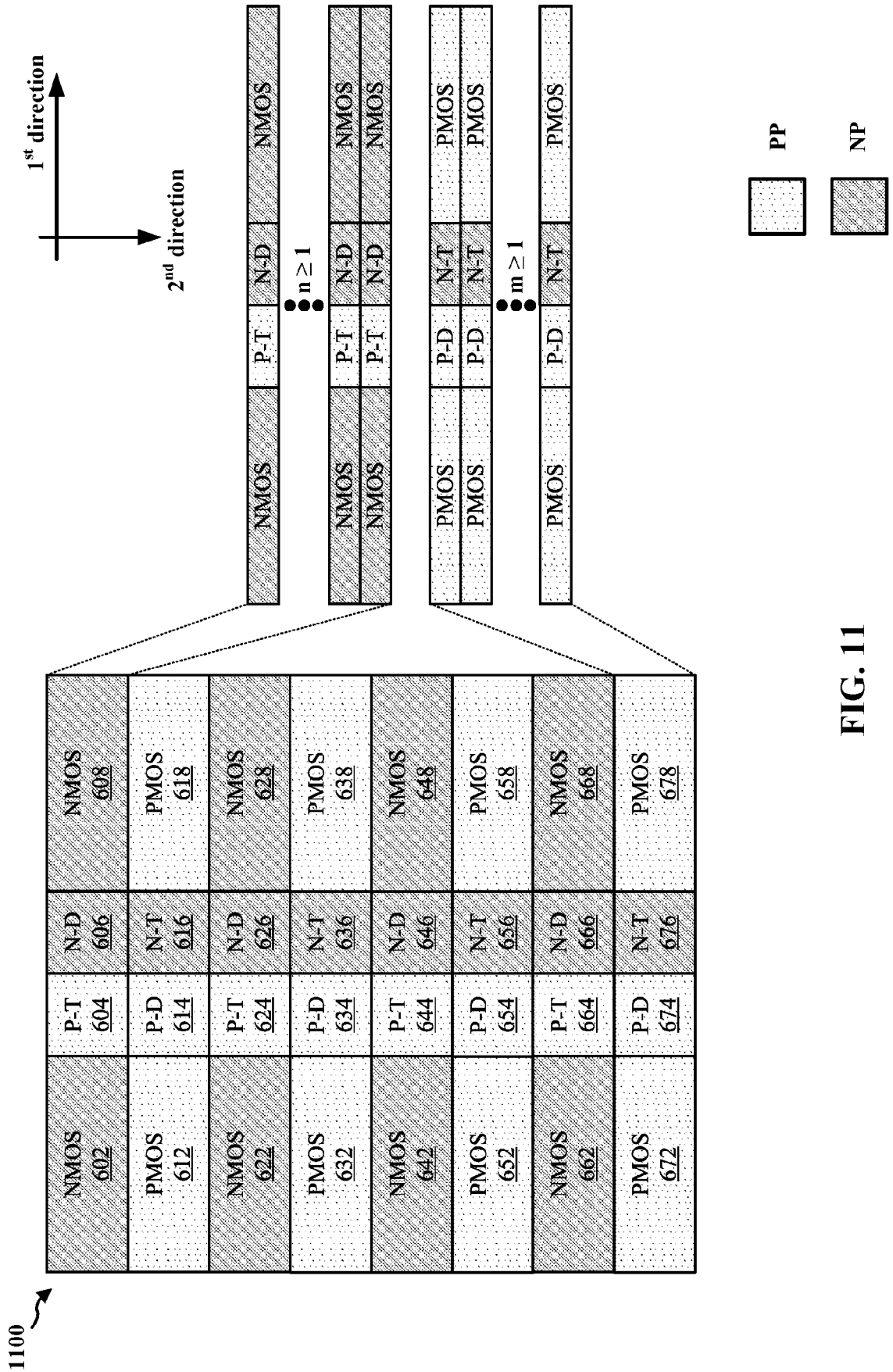
1100
NMOS 602
P-T 604
N-D 606
NMOS 608
PMOS 612
P-D 614
N-T 616
PMOS 618
NMOS 622
P-T 624
N-D 626
NMOS 628
PMOS 632
P-D 634
N-T 636
PMOS 638
NMOS 642
P-T 644
N-D 646
NMOS 648
PMOS 652
P-D 654
N-T 656
PMOS 658
NMOS 662
P-T 664
N-D 666
NMOS 668
PMOS 672
P-D 674
N-T 676
PMOS 678
1st direction
2nd direction
n ≥ 1
m ≥ 1
PP
NP

FIG. 11

## REFERENCES CITED IN THE DESCRIPTION

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