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(71) Applicant: **Tridonic GmbH & Co. KG**
6851 Dornbirn (AT)

(72) Inventors:
- **Romano, Fabio**
  6850 Dornbirn (AT)
- **Kucera, Clemens**
  6850 Dornbirn (AT)
- **Stark, Stefan**
  6850 Dornbirn (AT)

(74) Representative: **Beder, Jens**
Mitscherlich PartmbB
Patent- und Rechtsanwälte
Karlstraße 7
80333 München (DE)

(54) OUTPUT OF MULTIBIT DATA FOR INTEGRATED CIRCUITS

(57) An integrated circuit (2) comprises a register (11) configured to store data comprising plural data bits (9), and a data interface (10) configured to output the data (6) comprising plural data bits. The data interface comprises data converting means (7) configured to convert the data comprising plural data bits (9) into one of an analogue voltage value (6) or a pulse-width modulated output signal (fig. 3. 26) or a digital data stream (fig. 4: 36). The data interface () 10is configured to provide the analogue voltage value (6), or the pulse-width modulated output signal (fig. 3: 26) or the digital data stream (fig. 3: 36), continuously at an output connection (4) of the data interface.

The data interface (10) may comprise a digital-to-analogue converter circuit (7) of the data converting means configured to convert the data comprising plural data bits (9) into the analogue value (6). The data interface may comprise in the data converting means a pulse-width modulating circuit (fig. 2: 20) configured to generate a pulse-width modulated output signal (fig. 2: 26) based on the data comprising plural data bits stored in the register (11). The data interface may comprise in the data converting means a converter circuit (fig. 4: 37) configured to generate a synchronized data stream (fig. 4: 36) including a sequence of bits (fig. 4. 36) based on the data comprising plural data bits (9) stored in the register (11).

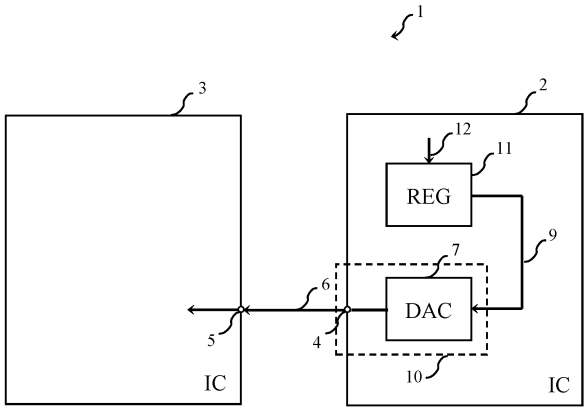

FIG. 2

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Description

[0001] The invention concerns the fields of digital data communication and of integrated circuits. In particular, an integrated circuit, a method for outputting multibit data from the integrated circuits and a respective system particularly adapted for the field of building automation systems and lighting systems is presented.

[0002] In the field of building automation systems and lighting systems, electronic devices that drive actuators and lighting modules by generating and providing load currents based on switched mode power supply (SMPS) technology and control loops for regulating the load current are fielded in large numbers.

[0003] The electronic devices include electronic circuits, which regularly include one or a plurality of integrated circuits. Integrated circuits (IC), sometimes referred to as a microchip or microchip dies, is a set of electronic circuits integrated on one small piece of semiconductor material, hence the term "chip". The semiconductor material maybe silicon, for example.

[0004] The plural ICs of the electronic circuit arranged on a printed circuit board (PCB) may include one or plural standardized ICs, e.g. from a family of ICs available from a multitude of manufacturers, and application specific integrated circuits (ASICs) designed, adapted and possibly manufactured for one specific application. Standardized ICs may include, e.g., microcontroller (μC) and microprocessor circuits.

[0005] In ICs, digital data is generated and processed. ICs may also generate and process analogue signals. The generated and processed analogue signals, which may, for example, include measured parameter values, e.g. temperature values of temperature sensors arranged integrally with the IC.

[0006] Digital data may include binary data including single bits, which may be communicated from one ICs via a single output pin to one other or to a plurality of other ICs via their respective input pin(s).

[0007] In case of the digital data including a plurality of bits (multibit data), e.g. the data including a measured parameter value digitized with a bit length of 10 bit, transmitting the digital data from the IC to another IC is more complex. Current approaches stores the data in a register of the IC, and transmit the data via a bus system on a request from the at least one other IC to the requesting other IC.

[0008] A register is a memory for storing data in an IC, which usually has a small memory size, e.g. for storing a small of amount of data bits, and is quickly accessible, e.g., having very short times for writing the amount of data bits into the register and reading the amount of data bits from the register.

[0009] In the context of transmitting digital data between ICs, the bus systems for transmitting data between ICs currently base on protocols that define the Inter-Integrated Circuit interface (I^2C) and the Serial Peripheral Interface (SPI).

[0010] The SPI interface is a synchronous serial communication interface specification used for short-distance communication, e.g. for use in embedded systems including plural devices. SPI provides communication in full duplex mode using a master-slave architecture usually with a single master. Some devices support changing roles on the fly depending on an external (SS) pin. The master (controller) device provides a frame for reading and writing. SPI may provide support for multiple slave devices by selecting with individual chip select (CS) signals, sometimes called slave select (SS) lines.

[0011] Interfaces for communication according to I^2C interfaces, sometimes known as I2C or IIC, are synchronous, multi-controller/multi-target (controller/target), packet-switched, single-ended, serial communication bus interfaces that are widely used for attaching lower-speed peripheral ICs to processors and microcontrollers in a short-distance, intra-board communication. Using PC interfaces enables transmitting data from one PCB to other PCBs, and therefore offers extended transmission distances compared with SPI. The I^2C interface, however, offers low transmission speeds, and increases power consumption compared with the SPI interface protocol.

[0012] Accessing data values, which exceed a single binary bit stored in a register of one IC from another IC via the I^2C or SPI interface results in a delay time until the requested data is available at the requesting IC for processing. The delay time may result in problems during further processing of the received digital data at the requesting IC. Implementing real time processing for electronic circuits, which include a plurality of ICs and require availability of data to another IC in real time using I^2C or SPI is difficult or even impossible. Nevertheless, building automation and lighting systems may benefit from control loops and parameter monitoring implemented based on real time availability of digital data including plural bits.

[0013] Thus, current concepts for transmitting multibit data from one IC to other electronic circuits with low time delays may be subject to improvement.

[0014] An integrated circuit according to the first aspect, a system according to the second aspect, and the method for outputting data from the integrated circuit according to the third aspect provide advantageous solutions to the aforementioned problem.

[0015] A closed control loop may be implemented using a microcontroller arranged separately from an integrated circuit that includes the parts of the control loop close to the manipulated variables of the control loop, in particular including sensor circuits and control actuating circuits of the closed control loop. The microcontroller implements the controller of the control loop. The low transmission delay and fast transmission rate for digital data between the microcontroller and the integrated circuit enables stable a fast control characteristics for the selected structure of the control loop.

[0016] Detecting failures and debugging, e.g. during a design phase of electronic circuitry, or testing during manufacturing and installing electronic devices including integrated circuits is simplified, or even enabled. Internal parameters of the integrated circuit stored in digital values of an internal register integrated circuit externally available for an analysis, with low time delay and fast.

[0017] Accessing internal data for the integrated circuit, in particular fast accessing internal data of the integrated circuit in real time, provides extended possibility for analysis, e.g. statistical analysis that may use statistical measures such as standard deviation.

[0018] The dependent claims define further advantageous embodiments.

[0019] According to the first aspect, the integrated circuit comprises a register configured to store data comprising plural data bits, and a data interface configured to output the data comprising plural data bits. The data interface comprises data converting means configured to convert the data comprising plural data bits into one of an analogue voltage value or a pulse-width modulated output signal or a digital data stream. The data interface is configured to provide the analogue voltage value, or the pulse-width modulated output signal, or the digital data stream, continuously at an output connection of the data interface.

[0020] The integrated circuit according to the first aspect overcomes the problem of introducing a time delay inherent in common solutions of transmitting multibit data via current bus systems in response to a request. The data comprising plural data bits stored in the register of the integrated circuit is continuously available from an exterior of the integrated circuit.

[0021] The integrated circuit according to the first aspect provides a significantly increased data rate for communicating data from one integrated circuit to another integrated circuit compared with the conventional approach of relying on the protocols of the I^2C interface and the SPI interface.

[0022] Although providing a fast data transmission capability for a digital data including plural bits, the integrated circuit according to the first aspect does not require a plurality of pins for a parallel digital data transmission. The number of pins available in packages of small form factors is restricted. Thus, the integrated circuit according to the first aspect combines low transmission delays desirable a transmission between integrated circuits with a dense circuit design and restricted packages sizes.

[0023] Continuously providing the digital data at an output pin of the integrated circuit according to the first aspect yields the additional benefit that via the output pin, a time sequence of the digital data (chronological sequence, time course) of the digital data is accessible from exterior of the integrated circuit. Contrary thereto, the conventional interface based on the bus system has the digital data concerning an internal parameter value of the integrated circuit only accessible for a particular point in time of the request for data.

[0024] The integrated circuit according to an embodiment has the data interface comprising a digital-to-analogue converter (DAC) circuit configured to convert the data comprising plural data bits into the analogue voltage value. The data interface is configured to provide the analogue voltage value continuously at the output connection of the data interface.

[0025] A DAC circuit frequently forms an integral part of integrated circuits. Using the DAC circuit for converting the digital data comprising plural data bits into a single analogue voltage value continuously available from externally offers therefore a cost effective solution to implement a fast data output of an internal parameter value.

[0026] In an embodiment of the integrated circuit, the data comprising plural data bits includes a measured parameter value, which is generated based on an analogue value by an analogue-to digital converter (ADC) circuit of the integrated circuit.

[0027] ADC circuits frequently from part of a measurement circuit, e.g. a temperature sensor that provides a digital value that corresponds to a sensed temperature. The integrated circuit according to the first aspect may provide the digital value provided by the conventional temperature sensor continuously in form of a corresponding analogue voltage value at a single connection, e.g. a pin or pad of an electric interface of the integrated circuit for further processing, e.g. generating temperature profiles.

[0028] The connection 4 may include either pins or pads. The terms pins and pads may be used interchangeably denoting corresponding structural elements performing a same function, however having different physical forms.

[0029] The analogue voltage value in an embodiment of the integrated circuit is an analogue voltage in a voltage range from 0 V to 3 V.

[0030] The voltage range between 0 V and 3 V may be input without further conversion or adjustment to analogue inputs of other integrated circuits. Thus, a fast and cost-efficient transmission of digital data comprising plural data bits is achieved.

[0031] According to an embodiment of the integrated circuit, the data interface comprises a pulse-width modulating (PWM) circuit configured to generate the pulse-width modulated output signal based on the data comprising plural data bits stored in the register. The data interface is configured to output the pulse-width modulated output signal via the output connection of the data interface.

[0032] The pulse-width modulated output signal may be output via a single connection of the interface circuit of the

integrated circuit according to the first aspect and includes in a duty cycle of the pulse-width modulated output signal a value that corresponds to the digital data including the plural data bits. Thus, a fast output of the digital data is achieved. A low-pass filtering of the pulse-width modulated output signal may provide a simple and cost-efficient means for de-modulating the pulse-width modulated output signal, in order to obtain an analogue value corresponding to the digital data stored in the register of the integrated circuit.

[0033] The integrated circuit may include the data interface comprising a converter circuit configured to generate a synchronized data stream including a sequence of bits based on the data comprising plural data bits stored in the register. The data interface is configured to output the synchronized data stream at the output connection of the data interface.

[0034] The digital data stream provides the digital data stored in the register via single output connection to the exterior of the integrated circuit. The time delay for outputting the data is reduced compared to protocols of the I^2C interface and the SPI interface of conventional bus systems.

[0035] The integrated circuit may form part of a building automation device, in particular of a light driver for driving at least one lighting module.

[0036] Driver devices for driving actuators of building automation systems and lighting modules regularly use integrated circuits of various types for implementing control loops for driver currents (load currents), output voltages, and also include temperature sensors for monitoring device temperatures. A fast transmission of digital data representative for measured parameters including without significant time delay between different integrated circuits forming the driver device is at least advantageous for designing, e.g., temperature monitoring circuits or current control loops, with a reliable, stable, and fast circuit behaviour. The integrated circuit according to the first aspect provides a capability for outputting multibit data, which may provide a basis for electronic circuits with exactly these characteristics.

[0037] The integrated circuit may be an application-specific integrated circuit (ASIC).

[0038] The integrated circuit according to one embodiment includes the data comprising plural data bits including an internal parameter value generated in the integrated circuit. The internal parameter value generated in the integrated circuit may in particular include at least one of a temperature value provided by at least one temperature sensor of the integrated circuit, a current value measured by at least one current sensor of the integrated circuit, and a voltage value measured by at least one current sensor of the integrated circuit.

[0039] The data comprising plural data bits may include a control output parameter value of a control loop, which is implemented including the integrated circuit according to one embodiment.

[0040] Thus, a control loop with high stability and fast response times maybe implemented.

[0041] According to the second aspect, the system for transmitting data comprising plural data bits comprises the integrated circuit according to the first aspect, and at least one of another integrated circuit and an electronic device. The data interface of the integrated circuit is configured to transmit the data comprising plural data bits to the at least one of the other integrated circuit and the electronic device.

[0042] The system provides a data communication capability between integrated circuits that communicates via a single connection of an interface a digital data comprising plural data bits (binary data bits) without significant time delay, and with a high data rate.

[0043] According to one embodiment of the system, the system further comprises a low-pass filter circuit configured to generate a filter output signal based on the pulse-width modulated signal input to the low-pass filter circuit by the integrated circuit via the connection of the data interface. The at least one of another integrated circuit and an electronic device is configured to process the filter output signal generated by the low-pass filter circuit.

[0044] The low-filter filter is a passive electric circuit of low technical complexity and is a cost-efficient, and provides the capability to provide an analogue voltage depending on the duty cycle of the pulse-width modulated signal, thereby conveying the digital data comprising plural data bits of the integrated circuit.

[0045] The method for outputting data comprising plural data bits by a data interface of an integrated circuit according to third aspect comprises steps of: storing, in a register of the integrated circuit, the data comprising plural data bits; converting, by a data converting means of the data interface, the data comprising plural data bits into one of an analogue value or a pulse-width modulated output signal or a digital data stream; and outputting continuously, by an output connection of the data interface, the analogue value or the pulse-width modulated output signal or the digital data stream.

[0046] Further features and advantages will be apparent from the subsequent and more particular description of embodiments, as illustrated in the accompanying figures, in which

Fig. 1 displays a simplified flowchart of a method for outputting digital data from an integrated circuit according to an embodiment;

Fig. 2 shows a block diagram illustrating structural elements for the data transmission from an integrated circuit to another electronic circuit in a first embodiment;

Fig. 3 displays, in block diagram form, structural elements for the data transmission from an integrated circuit to

another electronic circuit in a second embodiment;

Fig. 4 shows a block diagram illustrating structural elements for the data transmission from an integrated circuit to another electronic circuit in a third embodiment; and

Fig. 5 shows a simplified block diagram illustrating structural elements for the data transmission in an application example of a control loop with plural integrated circuits.

[0047] Same reference signs in different figures generally refer to same or corresponding parts or elements. The discussion of figures avoids a discussion of same reference signs for different figures wherever deemed possible without adversely affecting comprehensibility in order to achieve a concise description.

[0048] In mixed-signal integrated circuits, e.g., microprocessors integrated with A/D and D/A converters, an interface comprising the I/O pins must be able to accommodate not only digital signals, but also analogue signals. According to conventional practice, microcontrollers utilize a first set of I/O pins for digital signals and a second set of I/O pins four analogue signals. Differentiating between types of integrated circuits is well known and established in conventional art in order to separate analogue and digital processing circuits, as well as the I/O pins, because of the significant difference in the respective signal processing circuits, analogue signal processing circuits on the one hand and digital signal processing circuits on the other hand. Digital signal processing circuits operate binary. Binary operated circuits tend to generate noise because of a high-speed transition of digital signal. Due to the generated noise signals adversely affecting analogue circuits, such type of operations are highly undesirable in analogue circuits. Therefore, it is established practice to not only separate digital circuits from analogue circuits in mixed-type electronic circuits, but also to maintain the analogue and digital functions distinct as to the integrated I/O pins.

[0049] An analogue signal is a continuous signal representing some other quantity, i.e., analogous to another quantity. For example, in an analogue temperature signal, the instantaneous signal voltage varies continuously with a temperature. The analogue signal
represents continuous values; at any given time, it represents a real number within a continuous range of values.

[0050] In contrast, a digital signal represents the original time-varying quantity as
a sampled sequence of quantized values, which imposes some bandwidth and dynamic range constraints on the representation. A digital signal is a signal that represents data as a sequence of discrete values; at any given time, it can only take on, at most, one of a finite number of values.

[0051] The digital signal represents information in discrete bands of analogue levels. All levels within a band of values represent the same information state. In most digital circuits, the digital signal can have two possible valid values: such digital signal is a binary signal or logic signal. The binary signal is represented by two voltage bands: e.g., one voltage band near a reference value, typically termed as ground or zero volts, and the other voltage band with a value near the supply voltage of the digital circuit. The voltage bands correspond to the two values "zero" ("false", "LOW") and "one" ("true", "HIGH") of the Boolean domain. At any given time, the binary signal represents one binary digit (bit).

[0052] The analogue signal is subject to electronic noise and distortion introduced by a communication path, recording and signal processing operations performed on the analogue signal, which degrade the signal-to-noise ratio (SNR). During transmission or processing of the analogue signal, the noise introduced in the signal path will accumulate, progressively and irreversibly degrading the SNR.

[0053] Contrary to the analogue signal, the digital signal, e.g. a binary signal representing one binary digit (bit), because of the discretization, relatively small changes to the instantaneous analogue signal level of the digital signal do not leave the discrete envelope, and as a result are ignored by electronic circuitry sensing the signal state. As a result, the digital signal has noise immunity, e.g., electronic noise, provided the noise level is not to large, will not affect a digital circuit, whereas noise always degrades the analogue signal to some degree.

[0054] Converting the analogue signal into a digital signal introduces a low-level quantization noise into the converted signal due to finite resolution of digital systems. Contrary to the analogue signal, transmitting, storing, or processing the digital signal without introducing significant additional noise or distortion degrading the digital signal. Most notably, in digital systems, the degradation of the digital signal is detectable and appropriate means may even correct the degraded signal.

[0055] Fig. 1 displays a simplified flowchart of a process including the method steps for outputting data comprising plural data bits according to an embodiment.

[0056] The process of fig. 1 uses the example of transmitting a set of data comprising plural data bits, e.g. binary data bits, from a first integrated circuit to a second integrated circuit.

[0057] Alternatively or additionally, the data comprising plural data bits maybe transmitted from the first integrated circuit to another electronic device. Another electronic device maybe a measurement device for analysing analogue electric signals. The other electronic device may be an oscilloscope. The other electronic device includes at least one electronic circuit and at least one interface for electrical signals.

[0058] The data comprising plural data bits may be a parameter value of an internal parameter in the first integrated circuit.

[0059] The process starts by storing in a register of the first integrated circuit, the data comprising plural data bits.

[0060] The method of transmitting data comprising plural data bits the data interface of the first integrated starts in step S1 with a step of obtaining the data comprising plural data bits by a data interface of the first integrated circuit.

[0061] In subsequent step S2, a data converting means of the data interface of the first integrated circuit converts the data comprising plural data bits into a transmission signal. The transmission signal may include one of an analogue value or a pulse-width modulated output signal or a digital data stream.

[0062] Figs. 2, 3 and 4 display specific examples for the data converting means.

[0063] The data converting means shown in fig. 2 is an analogue-to digital converter (ADC) circuit, which obtains the data comprising the plural data bits from the register, converts the data comprising plural of data bits into the corresponding analogue value and outputs the analogue value to a connection of the data interface of the first integrated circuit.

[0064] The data converting means shown in fig. 3 is a pulse-width modulating (PWM) circuit, which obtains the data comprising the plural data bits from the register, converts the data comprising plural of data bits into the pulse-width modulated output signal and outputs the pulse-width modulated output signal to the connection of the data interface of the first integrated circuit.

[0065] The data converting means shown in fig. 4 is a digital-to digital converter (DDC) circuit, which obtains the data comprising the plural data bits from the register, converts the data comprising plural of data bits into the digital data stream and outputs the generated digital data stream to the connection of the data interface of the first integrated circuit.

[0066] The method of outputting data proceeds in step S3, in which the output connection of the data interface of the first integrated circuit outputs continuously the transmission signal, in particular the analogue value or the pulse-width modulated output signal or the digital data stream generated in step S2.

[0067] Therefore, the data comprising plural data bits (multibit data) is continuously available at a single output connection of the data interface of the first integrated circuit. There may be no request according to a specific system bus protocol by a second integrated circuit, electronic circuit or electronic device required to trigger output of the transmission signal. The output transmission signal, in particular the analogue value or the pulse-width modulated output signal or the digital data stream corresponding to the data comprising plural data bits by the data interface of the first integrated circuit may continuously accessible from the exterior of the first integrated circuit. The output transmission signal may be monitored or recorded or processed by the second integrated circuit without time delay or at least without significant time delay, e.g. introduced by a system bus such as SPI or I2C.

[0068] The output connection 4 includes a single pin or a single pad of the data interface 10.

[0069] The output connection 4 of the data interface of the first integrated circuit is connected with an input connection of an interface of the second integrated circuit. The output connection of the first integrated circuit may be connected with the input connection of the second integrated circuit via at least one of an electrically conducting wire or a transmission line on a printed circuit board (PCB) on which the first integrated circuit and the second integrated circuit are mounted. The electrical connection of the output connection of the first integrated circuit may be connected with the input connection of the second integrated circuit may include a detachable electrical connection, e.g. a socket and connector combination.

[0070] The process of transmitting the data) comprising plural data bits from the first integrated circuit to the second integrated circuit illustrated in fig. 1 proceeds with step S_4. In step S_4, the second integrated circuit obtains the output transmission signal provided via the data interface of the first integrated circuit and the interface of the second electronic circuit.

[0071] In step S_5, the second integrated circuit may process the obtained output transmission signal from the first integrated circuit. Thus, the second integrated circuit is enabled to process an internal parameter value of the first integrated circuit without significant time delay.

[0072] Processing the obtained output transmission signal by the second integrated circuit may include converting the obtained output transmission signal into a different signal format for further processing. Fig. 2 illustrates an example, in which the second integrated circuit includes a low-pass filter circuit for converting the pulse-width modulated signal obtained from the first integrated circuit into an analogue voltage by smoothening a signal characteristic of the pulse-width modulated signal input to the low-pass filter circuit.

[0073] Processing the obtained output transmission signal by the second integrated circuit may include real time processing obtained output transmission signal, e.g. in a microcontroller for implementing a temperature monitoring function for monitoring the device temperature of the first integrated circuit.

[0074] Additionally or alternatively, the second integrated circuit 3 may include the microcontroller for implementing a controller of a control loop, which obtains a current value of process variable as the internal parameter from the first integrated circuit 2, as illustrated and discussed with reference to fig. 5.

[0075] Fig. 2 shows a block diagram illustrating structural elements for the data transmission in a system 1 from an integrated circuit to another integrated circuit according a first embodiment.

[0076] The system 1 for transmitting data that comprises plural data bits transmits the data comprising plural data bits

9 from a first integrated circuit 2 to a second integrated circuit 3.

[0077] The second integrated circuit 3 may alternatively be at least one of an electronic circuit, or an electronic device.

[0078] The first integrated circuit 2 and the second integrated circuit 3 may include at least one of an ASIC, a microcontroller or an electronic device including at least one electronic circuit.

[0079] The first integrated circuit 2 comprises a register 11 configured to store the data comprising plural data bits. The data comprising plural data bits may include a measured parameter value, which an analogue-to digital converter (ADC) circuit of the first integrated circuit 2 not shown in fig. 2 generates based on an analogue value, e.g. an analogue temperature value, and analogue current value or an analogue voltage value.

[0080] In a particular example of the first integrated circuit 2, the ADC circuit forms part of a temperature sensor, a current-measuring sensor or a voltage-measuring sensor of the first integrated circuit 2.

[0081] Alternatively, the ADC circuit forms part of a temperature sensor, a current-measuring sensor or a voltage-measuring sensor of the first integrated circuit 2 externally and not forming part of the first integrated circuit 2.

[0082] The first integrated circuit 2 comprises a data interface 10 configured to output the data comprising plural data bits, which is stored in the register 11. The data interface 10 of the first integrated circuit is configured to transmit the data comprising plural data bits to at least one of the second integrated circuit 3 and the electronic device.

[0083] The data interface 10 comprises data converting means configured to convert the data comprising plural data bits into an analogue voltage value 6.

[0084] The data interface 10 comprises output connection 4. The output connection 4 of the data interface 10 is configured to provide the analogue voltage value 6 continuously at the output connection 4 of the data interface 10.

[0085] The analogue voltage value 6 comprises an analogue value that corresponds to a value of the data comprising plural data bits, which is currently stored in the register 11.

[0086] The analogue voltage value 6 may be an analogue voltage in a voltage range from 0 V to 3 V.

[0087] The data comprising plural data bits 9 may include an internal parameter value generated in the first integrated circuit 2, in particular at least one of a temperature value provided by at least one temperature sensor of the integrated circuit 2, a current value measured by at least one current sensor of the integrated circuit 2, and a voltage value measured by at least one current sensor of the integrated circuit 2.

[0088] The data comprising plural data bits 9 may include a control output parameter value of a control loop.

[0089] The second integrated circuit 3 may obtain the analogue voltage value via the connection 4 of the first integrated circuit 2. The analogue voltage value 6 currently present at the output connection 4 of the data interface 10 comprises the analogue value that corresponds to a value of the data comprising plural data bits 9, which is currently stored in the register 11.

[0090] In particular, the second integrated circuit 3 may comprise an interface with at least one input connection 5, which is directly electrically connected with the output connection 4 of the data interface 10 of the first integrated circuit 2.

[0091] The second integrated circuit 3 may, via the least one input connection 5 and the output connection 4 of the data interface 10 of the first integrated circuit 2, continuously monitor the analogue voltage value 6 currently present at the output connection 4 of the data interface 10.

[0092] The analogue voltage value 6 currently present at the output connection 4 corresponds to the analogue value that corresponds to a value of the data comprising plural data bits 9, which is currently stored in the register 11.

[0093] Therefore, the system 1 enables to obtain, to monitor, or to record continuously over time the data comprising plural data bits 9, which the register 11 of the first integrated circuit 2 stores without significant time delay for accessing the register 11 and for transferring the stored data comprising plural data bits 9 to the second integrated circuit 3.

[0094] Internal register of the first integrated circuit 2 are accessible from external of the integrated circuit 2 via a single output connection 4 of the data interface 10.

[0095] The SPI bus system is a synchronous serial communication interface protocol (specification) used for short-distance communication, e.g. in embedded systems. SPI devices communicate in full duplex mode using a master-slave architecture usually with a single master. The master (controller) device originates the frame for reading and writing. Multiple slave-devices may be supported through selection with individual chip select (CS), sometimes called slave select (SS) lines. Thus, the SPI maybe called a four-wire serial bus. The system 1 is significantly less complex than the SPI system bus and provides via a single connection 4 of the first integrated circuit 2 instant and continuous access to the internal register 10 and data comprising plural bits 9 stored in the internal register 11 without time delay.

[0096] The I^2C system bus is a synchronous, multi-controller/multi-target, packet switched, single-ended, serial communication bus widely used for attaching lower-speed peripheral integrated circuits to processors and microcontrollers for short-distance, intra-board communication. Although I^2C enables transmitting data to other PCBs, a transmission speed via the I^2C bus system is low and the delay times are less favorable than offered by the system 1 for transmitting data from the first integrated device 2 to the second integrated device 3.

[0097] Fig. 3 shows a block diagram illustrating structural elements for a system 1' implementing a data transmission from a first integrated circuit 22 to another integrated circuit 23 according to a second embodiment.

[0098] The first integrated circuit comprises a data interface 20, which has a different structure to the data interface

10 of fig. 2.

[0099] The data interface 20 includes a PWM circuit 27 configured to generate a pulse-width modulated output signal 26 based on the data comprising plural data bits 9 stored in the register 11 of the first integrated circuit 2.

[0100] The data comprising plural data bits 9 representing an internal parameter of the integrated circuit 2 is modelled in a corresponding duty cycle of the a pulse-width modulated output signal 26 generated based on the data comprising plural data bits 9.

[0101] The data interface 20 is configured to output the generated pulse-width modulated output signal 26 at the output connection 4 of the data interface 20.

[0102] There exist alternative arrangements of the second integrated circuit 23 for obtaining the value of the data comprising plural data bits 9, which is present in the pulse-width modulated output signal 36.

[0103] The interface of the second integrated circuit 23 shown in fig. 3 includes a low-pass filter circuit 23 configured to generate a filter output signal 24 based on the pulse-width modulated signal 26 input to the low-pass filter circuit 25 from the first integrated circuit 22 via the input connection 5 of the data interface 25, and the output connection 4 of the data interface 20.

[0104] Alternatively, the second integrated circuit 23, in particular the interface circuit 25 of the second integrated circuit 23, may include a receiver circuit not illustrated by a figure, which is configured to process the pulse-width modulated signal 26 received from the first integrated circuit 22 via the input connection 5 of the data interface 25 and the output connection 4 of the data interface 20. The receiver circuit may determine the duty cycle of the pulse-width modulated signal 26 and thereby determine the value of the internal parameter of the integrated circuit 2 that is modelled in the duty cycle of the a pulse-width modulated output signal 26 generated based on the data comprising plural data bits 9.

[0105] The pulse-width modulated signal 26 received from the output connection 4 of the first integrated circuit 22 comprises the duty cycle that corresponds to the value of the data comprising plural data bits 9, which is currently stored in the register 11.

[0106] Therefore, the system 1 is able to obtain, to monitor, or to record continuously over time the data comprising plural data bits 9, which the register 11 of the first integrated circuit 22 stores without significant time delay for accessing the register 11 and for transferring the stored data comprising plural data bits 9 to the second integrated circuit 23.

[0107] Fig. 4 shows a block diagram illustrating structural elements for a system 1" implementing a data transmission from a first integrated circuit 32 to another integrated circuit 33 according to a third embodiment.

[0108] The first integrated circuit 32 comprises a data interface 30, which differs in its structure from the data interface 10 of fig. 2 and the data interface 20 of fig. 3.

[0109] The data interface 30 comprises a converter circuit 37 configured to generate a synchronized data stream 37 including a sequence of bits based on the data comprising plural data bits 9 stored in the register 11 of the first integrated circuit 32.

[0110] The converter circuit 37 corresponds to a DC-to-DC converter circuit. The DC-to-DC converter circuit outputs the synchronized data stream 37, which includes in the bit stream the coded value corresponding to the data comprising plural data bits 9.

[0111] The synchronized data stream 37 may comprise synchronisation means that enable a interface circuit 35 of the second integrated circuit 33 to synchronize on the bit stream and to extract the value encoding the data comprising plural data bits 9

[0112] The data interface 30 is configured to output the generated synchronized data stream 36 via the output connection 4 of the data interface 30 to the exterior of the integrated circuit 32.

[0113] The synchronized data stream 36 received from the output connection 4 of the first integrated circuit 32 comprises the coded value of the data comprising plural data bits 9, which is currently stored in the register 11.

[0114] Therefore, the system 1" is able to obtain, to monitor, or to record continuously over time the data comprising plural data bits 9, which the register 11 of the first integrated circuit 32 stores without significant time delay for accessing the register 11 and for transferring the stored data comprising plural data bits 9 to the second integrated circuit 33.

[0115] Fig. 5 shows a simplified block diagram illustrating structural elements for the data transmission in a first application example of a control loop with plural integrated circuits.

[0116] The first application example may form part of a light driver device as an example for a building automation system. The light driver device generates and outputs a load current I_{LOAD} to a lighting module comprising a plurality of light emitting modules (LED). The driver device is configured to control the load current I_{LOAD} to a preset load current value $I_{LOAD, SET}$. The set load current value may correspond to a dimming value provided by a dimmer or a light control server.

[0117] The light driver device may include at least one converter in a switched mode power supply (SMPS) topology for generating the load current I_{LOAD} as a DC current, e.g. based on a mains power supply grid, and, alternatively or additionally, from a battery or DC emergency supply grid. The at least one converter use may use any SMPS topologies, e.g. a flyback topology, a forward topology, a buck topology, a boost topology, a buck-boost topology, in order to name examples.

[0118] The block diagram of fig. 5 illustrates one example of the control loop for controlling the load current I_{LOAD} and displays the components of the light driver device which contribute to forming the control loop.

[0119] The first integrated circuit may be and ASIC including current measurement means configured to measure the load current I_{LOAD} and to provide a digital value corresponding to the analogue current value of the load current I_{LOAD} by using an ADC circuit. The digital value of measured load current obtained in the integrated circuit may form a process value (PV) of a control loop for controlling the load current I_{LOAD}.

[0120] The load current I_{LOAD} represents the manipulated variable (MV) in the control loop of fig. 5.

[0121] The second integrated circuit in the example of fig. 5 includes a microcontroller. The microcontroller is arranged separately and remote from the ASIC and implements a controller of the control loop. The microcontroller requires an actual value of the load current I_{LOAD} as the process value (PV) of the control loop as input variable for the controller of the control loop.

[0122] The microcontroller implementing the controller of the control loop and separate from the integrated circuit calculates a current controller output (CO) based on the obtained current value of the load current I_{LOAD} as the process value (PV) and based on the preset load current value $I_{LOAD, SET}$. The microcontroller provides the calculated controller output CO to the first integrated circuit, in particular the ASIC, for adapting the manipulated variable MV according to the calculated controller output CO.

[0123] A limited data rate and, in particular a time delay introduced by a conventional transmission of the digital value of measured load current I_{LOAD} via a bus system, e.g. SPI or I^2C, might affect or even avoid a designing a stable, and a fast current control via the control loop including the ASIC and the microcontroller. Contrary thereto, the data interface of the first integrated circuit or ASIC provides the current digital value of measured load current I_{LOAD} without significant time delay in real time for the second integrated circuit or microcontroller. This enables using the ASIC and the microcontroller for implementing a fast and stable control loop for the load current I_{LOAD}.

[0124] Additionally or alternatively, and different to the example shown in fig. 5, the microcontroller may include a data interface configured to output the calculated current controller output CO as data comprising plural data bits to the ASIC.

[0125] The data interface of the microcontroller may comprise data converting means configured to convert the current controller output CO as data comprising plural data bits into one of an analogue voltage value or a pulse-width modulated output signal or a digital data stream. and The data interface of the microcontroller may then provide the analogue voltage value, the pulse-width modulated output signal, or the digital data stream, continuously at an output connection of the data interface of the microcontroller.

[0126] Thus, corresponding advantages for transmitting the calculated current controller output CO to the ASIC for adapting the manipulated variable MV based on the current controller output CO are achievable. The current controller output CO for adapting the current digital value of measured load current I_{LOAD} is available at the ASIC without additional time delay, e.g. due to transmission from the microcontroller to the ASIC. This enables using the ASIC and the microcontroller for implementing a fast and stable control loop for the load current I_{LOAD}.

[0127] For monitoring a stability of the current control loop implemented using the integrated circuits, the embodiment provides improved values for the manipulated variable MV of the current control loop. The conventional approach only provides instantaneous values for the output current I_{LOAD} in the integrated circuit, which are updated every 2ms in an example of a currently available, exemplary light driver device. Analyzing and judging the stability of the control loop from the exterior of the integrated circuit is therefore at least difficult if not impossible in the conventional approach. Contrary thereto, the data including plural bits as the manipulated variable MV, in particular the current value of the load current I_{LOAD} stored in the register is immediately accessible from the exterior of the ASIC for inspection by a design engineer, or perhaps even more advantageous, for recording

[0128] The exemplary first application integrates the method for outputting data comprising plural data bits in a control loop for controlling the load current I_{LOAD} output by a light driver device. The data comprising plural data bits is a measured parameter value for the load current I_{LOAD}.

[0129] Alternatively or additionally to the control loop for controlling the load current I_{LOAD}, a control loop for controlling a voltage U_{OUT} generated and output by the light driver device may be implemented in the light driver device. In that case, the data comprising plural data bits may correspond to a measured parameter value for the voltage U_{OUT} for the control loop controlling the voltage U_{OUT}. The first integrated circuit, e.g. the ASIC, may then use the data interface to provide the data comprising plural data bits, e.g. the measured voltage U_{OUT} to the second integrated circuit, e.g. the microcontroller in a corresponding manner to the output current I_{LOAD} as the data comprising plural data bits.

[0130] Another advantageous application of the integrated circuit may concern the start-up phase of an electronic device.

[0131] Accelerating the start-up phase of an electronic device that provides a drive current to a load, e.g. a light driver providing the load current I_{LOAD} (LED current) to at least one lighting module, may require determining the time at which the load begins actually conducting a current. The first integrated circuit may be configured to measure the output voltage U_{OUT} of the electronic device driving the at least one lighting module, and to provide the value to a the second integrated circuit, e.g. a microprocessor for determining the first derivative

$$\frac{dU_{OUT}}{dt} \qquad (1)$$

in order to determine the time at which the load actually starts to draw the load current load current I_{LOAD}. However, the conventional layout does suffer from problems when attempting to calculate the derivative of the load current I_{LOAD} at the second integrated circuit, e.g. the microcontroller, based on measured voltage data from the first integrated circuit, which is arranged remote from the integrated circuit and only available after transmission via a conventional bus system at the second integrated circuit.

[0132] A sample rate of the measured voltage data provided by an AD converter of the first integrated circuit via a bus system may vary, which has the effect of variations in the term *dt* in the expression (1) calculated in the second integrated circuit or microprocessor arranged separate from the first integrated circuit. This may result either from different registers set by the microcontroller, or from time delays introduced by transferring the data of the measured voltage via the bus system from the first integrated circuit to the second integrated circuit. A variation in dU_{OUT} may occur due to the integrated circuit only providing averaged values for the term dU_{OUT} in expression (1).

[0133] The first integrated circuit according to the embodiment enables to provide analogue values representative for the measured voltage data provided by the AD converter of the integrated circuit without significant time delay and with a high accuracy with regard to variations of dU_{OUT}. Therefore, the microcontroller may calculate the first derivative according to expression (1) without significant time delay and with increased accuracy when compared to a circuit design including data transmission between integrated circuits using conventional bus systems. The integrated circuit according to the discussed embodiments enables an efficient implementation of algorithms for accelerating the start-up phase of an electronic device, and offers therefore advantageous options for the circuit design of electronic devices.

Claims

1. Integrated circuit, comprising

a register (11) configured to store data comprising plural data bits (9), and
a data interface (10, 20, 30) configured to output the data comprising plural data bits (9),
wherein the data interface (10, 20, 30) comprises data converting means (7, 27, 37) configured to convert the data comprising plural data bits (9) into one of an analogue voltage value (6) or a pulse-width modulated output signal (26) or a digital data stream (36), and
the data interface (10, 20, 30) is configured to provide the analogue voltage value (6), the pulse-width modulated output signal (26) or the digital data stream (36), continuously at an output connection (4) of the data interface (10, 20, 30).

2. The integrated circuit according to claim 1, wherein

the data interface (10) comprises
a digital-to-analogue converter circuit (7) configured to convert the data comprising plural data bits (9) into the analogue voltage value (6), and
the data interface (10) is configured to provide the analogue voltage value (6) continuously at the output connection of the data interface (10).

3. The integrated circuit according to claim 1 or 2, wherein
the data comprising plural data bits (9) includes a measured parameter value, which is generated based on an analogue value by an analogue-to digital converter circuit of the integrated circuit (2).

4. The integrated circuit according to any of the preceding claims, wherein
the analogue voltage value (6) is an analogue voltage in a range from 0 V to 3 V.

5. The integrated circuit according to claim 1, wherein

the data interface (20) comprises a pulse-width modulating circuit (27) configured to generate the pulse-width modulated output signal (26) based on the data comprising plural data bits (9) stored in the register (11), and
the data interface (20) is configured to output the pulse-width modulated output signal (26) at the output connection (4) of the data interface (20).

6. The integrated circuit according to claim 1, wherein

the data interface (30) comprises a converter circuit (37) configured to generate a synchronized data stream (36) including a sequence of bits based on the data comprising plural data bits (9) stored in the register (11), and the data interface (30) is configured to output the synchronized data stream (36) at the output connection (4) of the data interface (30).

7. The integrated circuit according to according to any one of the preceding claims, wherein
the integrated circuit (2, 22, 32) is part of a building automation device, in particular of a light driver device for driving at least one lighting module.

8. The integrated circuit according to any one of the preceding claims, wherein
the integrated circuit (2, 22, 32) is an application-specific integrated circuit ASIC.

9. The integrated circuit according to any one of the preceding claims, wherein

the data comprising plural data bits (9) includes an internal parameter value generated in the integrated circuit (10, 20, 30), in particular at least one of
a temperature value provided by at least one temperature sensor of the integrated circuit,
a current value measured by at least one current sensor of the integrated circuit (10, 20, 30), and a
a voltage value measured by at least one current sensor of the integrated circuit (10, 20 30).

10. The integrated circuit according to any one of the preceding claims, wherein
the data comprising plural data bits (9) includes an a control output parameter value (CO) of a control loop.

11. System for transmitting data comprising plural data bits, wherein the system comprises

the integrated circuit (2, 22, 32) according to one of claims 1 to 10, and
at least one of another integrated circuit (3, 23, 33) and an electronic device,
wherein the data interface (10, 20, 30) of the integrated circuit (3, 23, 32) is configured to transmit the data comprising plural data bits (9) to the at least one of the other integrated circuit (3, 23, 33) and the electronic device.

12. The system according to claim 11, the system further comprising

a low-pass filter circuit (R, C) configured to generate a filter output signal (24) based on the pulse-width modulated signal (26) input to the low-pass filter circuit (R, C) from the integrated circuit (2, 22, 32) via the connection (4) of the data interface (10, 20, 30), and
wherein the at least one of another integrated circuit (3, 23, 33) and an electronic device is configured to process the filter output signal (24) generated by the low-pass filter circuit (R, C).

13. Method for outputting data comprising plural data bits (9) by a data interface (10, 20, 30) of an integrated circuit (2, 22, 32), the method comprising steps of

storing, in a register (11) of the integrated circuit (2, 22, 32), the data comprising plural data bits (9),
converting (S2), by a data converting means (7, 27, 37) of the data interface (10, 20 30), the data comprising plural data bits (9) into one of an analogue value (6) or a pulse-width modulated output signal (26) or a digital data stream (36),
outputting continuously (S_3), by an output connection (4) of the data interface (10, 20, 30), the analogue value (6) or the pulse-width modulated output signal (26) or the digital data stream (36).

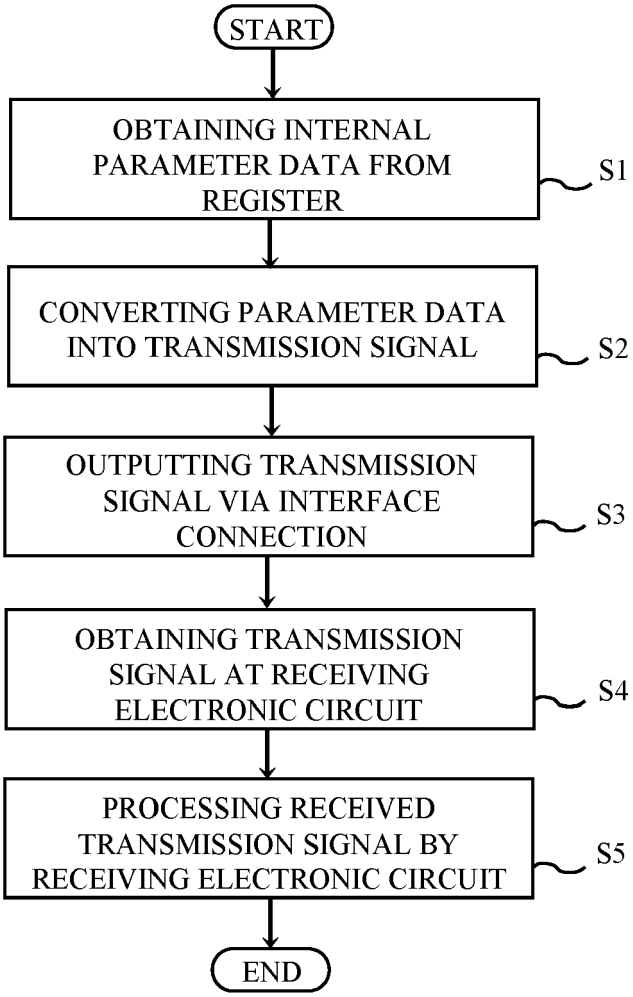
START
OBTAINING INTERNAL PARAMETER DATA FROM REGISTER
S1
CONVERTING PARAMETER DATA INTO TRANSMISSION SIGNAL
S2
OUTPUTTING TRANSMISSION SIGNAL VIA INTERFACE CONNECTION
S3
OBTAINING TRANSMISSION SIGNAL AT RECEIVING ELECTRONIC CIRCUIT
S4
PROCESSING RECEIVED TRANSMISSION SIGNAL BY RECEIVING ELECTRONIC CIRCUIT
S5
END

FIG. 1

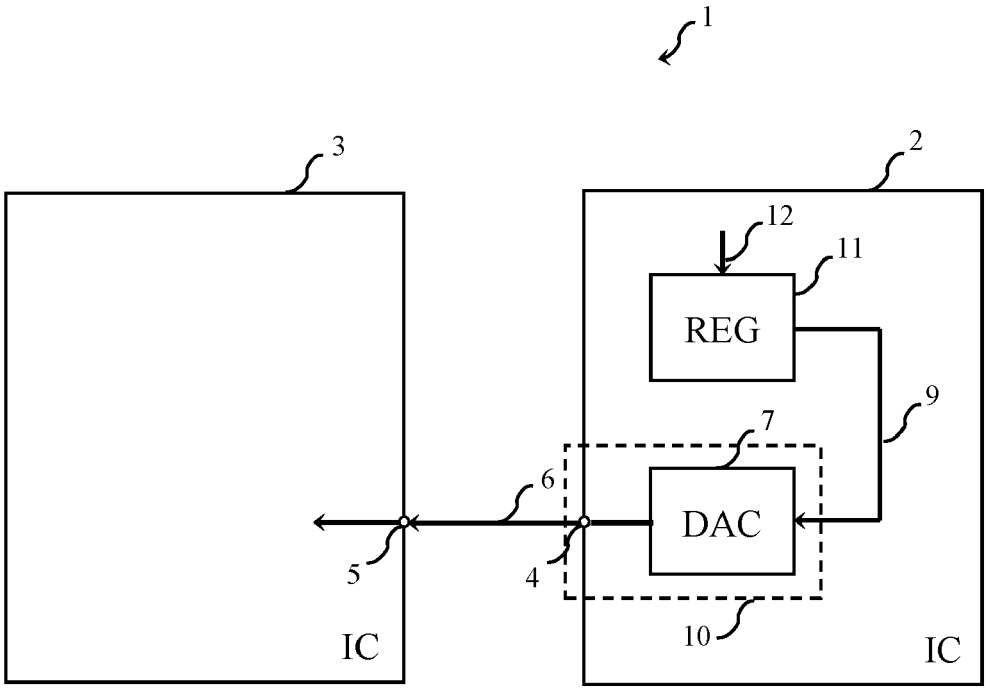

FIG. 2

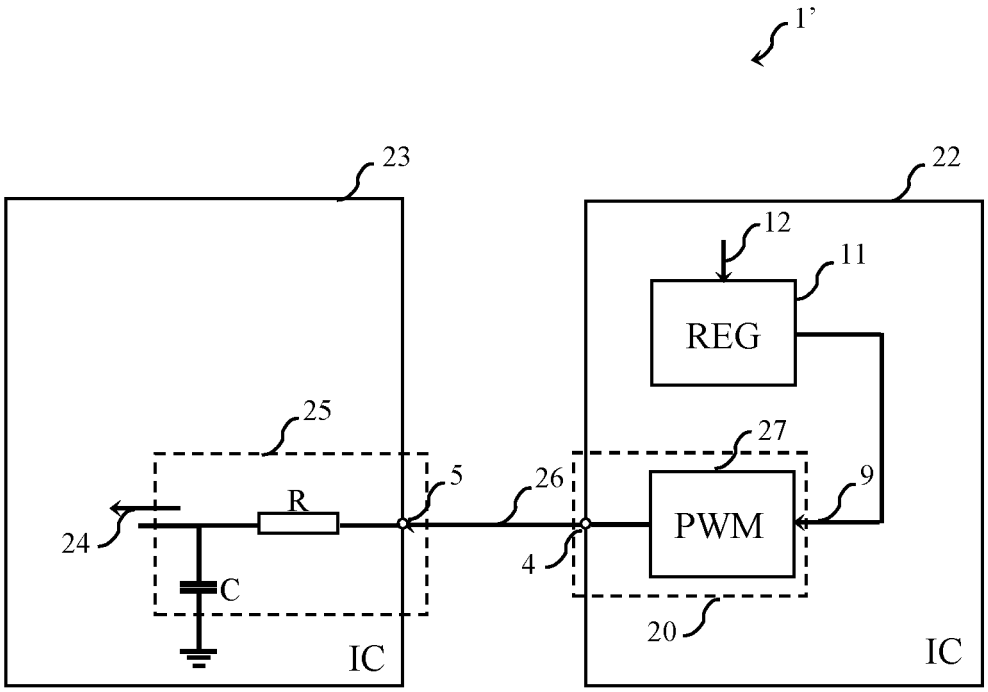

FIG. 3

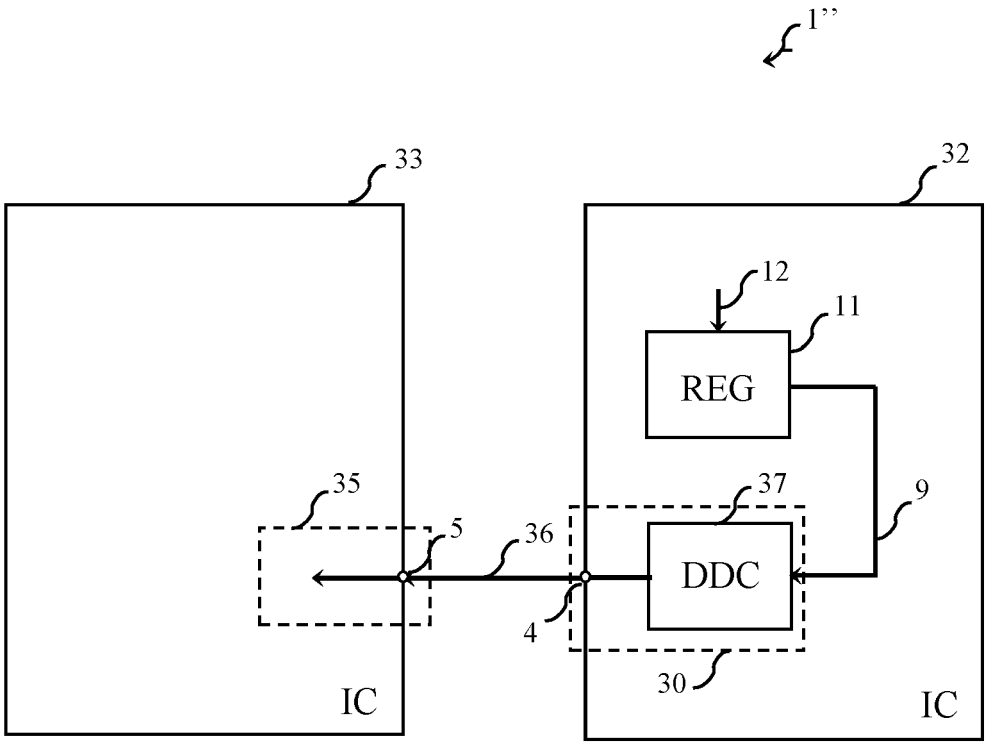

FIG. 4

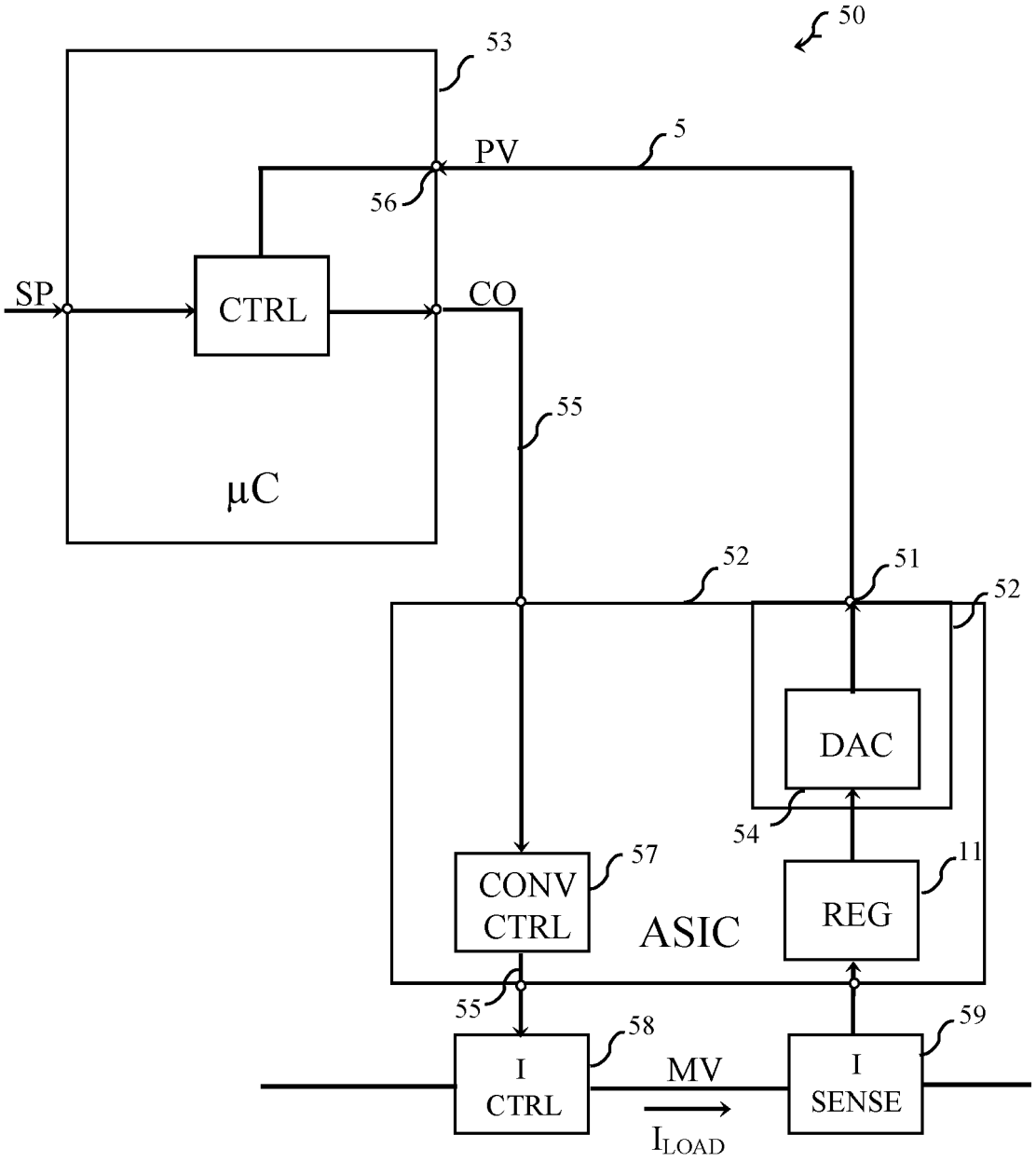
50
53
PV
5
56
SP
CTRL
CO
55
µC
52
51
52
DAC
54
57
CONV
CTRL
ASIC
REG
11
55
58
59
I
CTRL
MV
I
SENSE
I_{LOAD}

FIG. 5

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EUROPEAN SEARCH REPORT

Application Number
EP 22 20 7456

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X	US 2008/170012 A1 (S DILIP [US] ET AL) 17 July 2008 (2008-07-17) * abstract; figure 6 * * paragraphs [0014], [0022] - [0031], [0036], [0037] *	1-13	INV. H05B45/00 H05B45/30
X A	US 2009/174338 A1 (MURAMATSU YASUNORI [JP]) 9 July 2009 (2009-07-09) * abstract; figures 1,2,3 *	1,3,5, 7-9,13 2,4,6, 10-12	
			TECHNICAL FIELDS SEARCHED (IPC)
			H05B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	28 April 2023	Mesic, Maté

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28-04-2023

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