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(71) Applicant: **Samsung Electronics Co., Ltd.**
Suwon-si, Gyeonggi-do 16677 (KR)

(72) Inventors:
• **CHOE, Dukhyun**
16678 Suwon-si (KR)

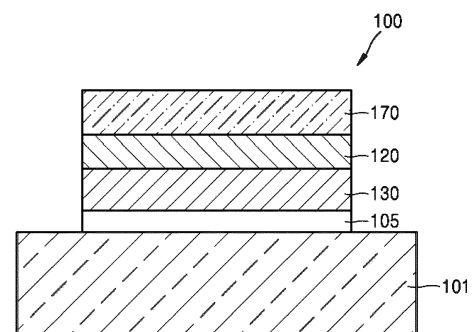
- **HEO, Jinseong**
16678 Suwon-si (KR)
- **LEE, Hyunjae**
16678 Suwon-si (KR)
- **NAM, Seunggeol**
16678 Suwon-si (KR)
- **PARK, Yoonsang**
16678 Suwon-si (KR)
- **YOO, Sijung**
16678 Suwon-si (KR)

(74) Representative: **Elkington and Fife LLP**
Prospect House
8 Pembroke Road
Sevenoaks, Kent TN13 1XR (GB)

(54) **MEMORY DEVICE IMPLEMENTING MULTI-BIT AND MEMORY APPARATUS INCLUDING THE SAME**

(57) Provided are a memory device (100) implementing multi-bit functionality and a memory apparatus including the memory device. The memory device includes a semiconductor substrate (101), a gate electrode (170) on the semiconductor substrate, and a plurality of ferroelectric layers (120, 130) laminated between the semiconductor substrate and the gate electrode in a first direction perpendicular to a surface of the semiconductor substrate and including at least one first ferroelectric layer (120) and at least one second ferroelectric layer (130). The first ferroelectric layer has a doping concentration gradient in which a doping concentration increases in the first direction, and the second ferroelectric layer has a doping concentration gradient in which a doping concentration decreases in the first direction. The memory device is configured to implement multi-bit functionality according to an operating voltage.

FIG. 1



Description

FIELD OF THE INVENTION

[0001] Various example embodiments relate to a memory device implementing multi-bit and/or a memory apparatus including the memory device.

BACKGROUND OF THE INVENTION

[0002] Ferroelectrics refer to a material having ferroelectricity to maintain spontaneous polarization by aligning internal electric dipole moments, while no electric field is applied from the outside. Recently, researches for implementing multi-bit memory cells by applying ferroelectrics to memory devices have been conducted.

SUMMARY OF THE INVENTION

[0003] Provided are a memory device implementing multi-bit and/or a memory apparatus including the memory device.

[0004] Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, and/or may be learned by practice of the various example embodiments.

[0005] According to some example embodiments, a memory device includes a semiconductor substrate, a gate electrode on the semiconductor substrate, and a plurality of ferroelectric layers including at least one first ferroelectric layer and at least one second ferroelectric layer, the plurality of ferroelectric layers laminated between the semiconductor substrate and the gate electrode in a first direction perpendicular to a surface of the semiconductor substrate. The first ferroelectric layer has a doping concentration gradient in which a doping concentration increases in the first direction, and the second ferroelectric layer has a doping concentration gradient in which a doping concentration decreases in the first direction. The memory device is configured to implement multi-bit functionality according to an operating voltage.

[0006] Embodiments may therefore propose imprinted ferroelectric lamination for multi-bit memory applications. This may facilitate introduction of ferroelectric thin films into DRAM, NAND flash memory, and neuromorphic devices to be utilized as memory devices and processors.

[0007] Proposed embodiments may therefore enable multi-bit memory technology, which was previously difficult to implement using ferroelectric or ferroelectric lamination alone, by utilizing imprint.

[0008] By way of example, embodiments may provide a structure including, from below, a semiconductor substrate, an interfacial layer, a layer in which ferroelectrics imprinted in different directions are deposited in multiple layers, and a gate electrode layer. In such a structure, the semiconductor substrate may include Si, Ge, SiGe, and the like, which are group IV semiconductors, and have dopants of which concentration is 10^{15} - 10^{20} .

[0009] By way of another example, embodiments may provide a structure including, from below, a semiconductor substrate, an interfacial layer, a layer with multiple layers of semi-ferroelectrics imprinted in different directions, and a gate electrode layer.

[0010] Yet another example embodiment may provide a structure including, from below, a semiconductor substrate, an interfacial layer, a layer cross-deposited with multiple layers of paraelectrics/ferroelectrics/semi-ferroelectrics imprinted in different directions, and a gate electrode layer. The paraelectrics may include fixed charges to cause an imprint in the ferroelectrics/semi-ferroelectrics layer.

[0011] Alternatively or additionally according to various example embodiments, provided is an operating method of a memory device, the memory device including a semiconductor substrate, a gate electrode on the semiconductor substrate, and a plurality of ferroelectric layers including at least one first ferroelectric layer and at least one second ferroelectric layer, the plurality of ferroelectric layers laminated between the semiconductor substrate and the gate electrode in a first direction perpendicular to a surface of the semiconductor substrate. The first ferroelectric layer has a doping concentration gradient in which a doping concentration increases in the first direction, and the second ferroelectric layer has a doping concentration gradient in which a doping concentration decreases in the first direction. The operating method comprises obtaining multiple-levels in different polarization states from each other by adjusting an operating voltage based on a hysteresis curve associated with the plurality of ferroelectric layers.

[0012] Alternatively or additionally according to various example embodiments, a memory apparatus includes a plurality of gate electrodes laminated in a direction perpendicular to a surface of a substrate, a plurality of ferroelectric layers on the plurality of gate electrodes and including at least one first ferroelectric layer and at least one second ferroelectric layer, and a channel layer on the plurality of ferroelectric layers, wherein the first ferroelectric layer has a doping concentration gradient in which a doping concentration increases in the first direction, and the second ferroelectric layer has a doping concentration gradient in which a doping concentration decreases in the first direction, and wherein the memory apparatus is configured to implement multi-bit functionality according to an operating voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other aspects, features, and advantages of certain embodiments of the disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a memory device according to some example embodiments;

FIG. 2A is a diagram of a capacitor including a fer-

roelectric layer imprinted in a (-) voltage direction;
 FIG. 2B is a diagram illustrating polarization (P) -
 voltage (V) characteristics of the ferroelectric layer
 of the capacitor illustrated in FIG. 2A;
 FIG. 3A is a diagram of a capacitor including a fer-
 roelectric layer imprinted in a (+) voltage direction;
 FIG. 3B is a diagram illustrating polarization (P) -
 voltage (V) characteristics of the ferroelectric layer
 of the capacitor illustrated in FIG. 3A;
 FIG. 4A is a diagram of a capacitor including a lam-
 ination structure of a first ferroelectric layer imprinted
 in a (-) voltage direction and a second ferroelectric
 layer imprinted in a (+) voltage direction;
 FIG. 4B is a diagram illustrating polarization (P) -
 voltage (V) characteristics of the lamination structure
 of the first and second ferroelectric layers of the ca-
 pacitor illustrated in FIG. 4A;
 FIG. 5A is a diagram illustrating an example of a
 cross-section of a first ferroelectric layer applicable
 to the memory device illustrated in FIG. 1;
 FIG. 5B is a diagram illustrating another example of
 a cross-section of a first ferroelectric layer applicable
 to the memory device illustrated in FIG. 1;
 FIG. 6A is a diagram illustrating an example of a
 cross-section of a second ferroelectric layer applica-
 ble to the memory device illustrated in FIG. 1;
 FIG. 6B is a diagram illustrating another example of
 a cross-section of a second ferroelectric layer appli-
 cable to the memory device illustrated in FIG. 1;
 FIG. 7 is a diagram illustrating another example of a
 cross-section of a first ferroelectric layer applicable
 to the memory device illustrated in FIG. 1;
 FIG. 8 is a diagram illustrating another example of a
 cross-section of a second ferroelectric layer applica-
 ble to the memory device illustrated in FIG. 1;
 FIG. 9 is a diagram illustrating one of the polarization
 (P) - voltage (V) characteristics illustrated in FIG. 4B;
 FIG. 10 is a diagram illustrating an example of the
 number of levels of the lamination structure of the
 first and second ferroelectric layers illustrated in FIG.
 4A which may be implemented according to an im-
 print voltage;
 FIG. 11 is a cross-sectional view of a memory device
 according to various example embodiments;
 FIG. 12 is a cross-sectional view of a memory device
 according to various example embodiments;
 FIG. 13 is a cross-sectional view of a memory device
 according to various example embodiments;
 FIG. 14A is a diagram of a capacitor including a lam-
 ination structure of a first ferroelectric layer, a second
 ferroelectric layer, and a third ferroelectric layer il-
 lustrated in FIG. 13;
 FIG. 14B is a diagram illustrating polarization (P) -
 voltage (V) characteristics of the lamination structure
 of the first, second, and third ferroelectric layers il-
 lustrated in FIG. 14A;
 FIG. 15 is a diagram illustrating an example of the
 number of levels of the lamination structure of the

first, second, and third ferroelectric layers illustrated
 in FIG. 14A which may be implemented according to
 an imprint voltage;
 FIG. 16 is a cross-sectional view of a memory device
 according to various example embodiments;
 FIG. 17 is a cross-sectional view of a memory device
 according to various example embodiments;
 FIG. 18 is a cross-sectional view of a memory device
 according to various example embodiments;
 FIG. 19 is a perspective view schematically illustrat-
 ing a memory apparatus according to some example
 embodiments;
 FIG. 20 is a diagram illustrating a cross-section of a
 cell string of the memory apparatus illustrated in FIG.
 19;
 FIG. 21 is a schematic circuit diagram of a memory
 apparatus according to some example embodi-
 ments;
 FIG. 22 is a schematic circuit diagram of an artificial
 intelligence device according to some example em-
 bodiments;
 FIG. 23 is a schematic block diagram of a display
 driver integrated circuit (DDI) and a display appara-
 tus including the DDI according to some example
 embodiments;
 FIG. 24 is a block diagram of an electronic apparatus
 according to some example embodiments;
 FIG. 25 is a block diagram of an electronic apparatus
 according to various example embodiments; and
 FIGS. 26 and 27 are conceptual diagrams schemat-
 ically illustrating a device architecture applicable to
 an electronic apparatus according to some example
 embodiments.

DETAILED DESCRIPTION

[0014] Reference will now be made in detail to various
 embodiments, examples of which are illustrated in the
 accompanying drawings, wherein like reference numer-
 als refer to like elements throughout. In this regard, the
 present embodiments may have different forms and
 should not be construed as being limited to the descrip-
 tions set forth herein. Accordingly, various embodiments
 are merely described below, by referring to the figures,
 to explain aspects. As used herein, the term "and/or" in-
 cludes any and all combinations of one or more of the
 associated listed items. Expressions such as "at least
 one of," when preceding a list of elements, modify the
 entire list of elements and do not modify the individual
 elements of the list.

[0015] Hereinafter, some example embodiments will
 be described in detail with reference to the accompanying
 drawings. In the drawings, like reference numerals in the
 drawings denote like elements, and sizes of components
 in the drawings may be exaggerated for clarity and con-
 venience of explanation. Meanwhile, various embodi-
 ments described below are provided only as an example,
 and thus can be embodied in various forms.

[0016] It will be understood that when a component is referred to as being "on" or "over" another component, the component can be directly on, under, on the left of, or on the right of the other component, or can be on, under, on the left of, or on the right of the other component in a non-contact manner. An expression used in the singular encompasses the expression of the plural, unless it has a clearly different meaning in the context. When a portion "includes" an element, another element may be further included, rather than excluding the existence of the other element, unless otherwise described.

[0017] The use of the terms "a" and "an" and "the" and similar referents in the context of describing embodiments (especially in the context of the following claims) are to be construed to cover both the singular and the plural. The operations of all methods described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context, and embodiments are not limited to the described order of the operations.

[0018] Moreover, the terms "part," "module," etc. refer to a unit processing at least one function or operation, and may be implemented by a hardware, a software, or a combination thereof.

[0019] The connecting lines, or connectors shown in the various figures presented are intended to represent exemplary functional relationships and/or physical or logical couplings between the various elements, and thus it should be noted that many alternative or additional functional relationships, physical connections or logical connections may be present in a practical device.

[0020] The use of any and all examples, or exemplary language provided herein, is intended merely to better illuminate technical ideas and does not pose a limitation on the scope of embodiments unless otherwise claimed.

[0021] FIG. 1 is a cross-sectional view of a memory device 100 according to some example embodiments. The memory device 100 illustrated in FIG. 1 may be a ferroelectric field effect transistor (FEFET).

[0022] Referring to FIG. 1, the memory device 100 may include a semiconductor substrate 101, a gate electrode 170, a first ferroelectric layer 120 and a second ferroelectric layer 130 laminated between the semiconductor substrate 101 and the gate electrode 170. A channel region may be formed on the semiconductor substrate 101 in correspondence with the gate electrode 170, and a source region and a drain region may be formed on either sides of the channel region, respectively.

[0023] The semiconductor substrate 101 may include at least one Group IV semiconductor material doped with a dopant having a certain polarity. The Group IV semiconductor material may include, for example, one or more of Si, Ge, or SiGe. However, example embodiments are not limited thereto.

[0024] A dopant doped with a Group IV semiconductor material may become a p-type dopant or an n-type dopant. A p-type dopant may include, for example, one or more of B, Al, Ga, In, etc., and an n-type dopant may

include, for example, one or more of P, As, etc. More specifically, the semiconductor substrate 101 may be a p-Si substrate including Si doped with a p-type dopant or an n-Si substrate including Si doped with an n-type dopant. However, this is only an example. A concentration of a dopant doped to the semiconductor substrate 101 may be, for example, about 10^{15} cm^{-3} to 10^{20} cm^{-3} (dopants per cubic centimeter). However, example embodiments are not limited thereto. In some example embodiments, the semiconductor substrate 101 may be doped with both n-type dopants and p-type dopants but at different concentrations from each other; for example, a dopant concentration of p-type dopants may be much greater than (e.g., several orders of magnitude greater than), or may be much less than (e.g., several orders of magnitude less than) a dopant concentration of n-type dopants.

[0025] An insulating layer 105 may be further provided on a surface of the semiconductor substrate 101. The insulating layer 105 may include an oxide and/or an oxynitride of a Group IV semiconductor material. For example, the insulating layer 105 may include one or more of SiO_2 , GeO_2 , SiGeO_4 , SiON, GeON, SiGeON, etc. However, the foregoing is provided only as an example.

[0026] The gate electrode 170 may be provided on the semiconductor substrate 101. The gate electrode 170 may include a metal and/or a metallic nitride. The metal may include, for example, one or more of aluminum (Al), tungsten (W), molybdenum (Mo), titanium (Ti), or tantalum (Ta), and the metallic nitride may include, for example, titanium nitride (TiN) and/or tantalum nitride (Ta₂N₃).

[0027] The gate electrode 170 may include one or more of a metal carbide, polysilicon such as undoped or doped polysilicon, or a two-dimensional (2D) conductive material. The metal carbide may be or may include a metal carbide doped with aluminum or silicon. More specifically, the metal carbide may include one or more of TiAlC, TaAlC, TiSiC, or TaSiC. The gate electrode 170 may have a structure in which a plurality of materials are laminated. For example, the gate electrode 170 may have a lamination structure of metal nitride layer/metal layer or a lamination structure of metal nitride layer/metal carbide layer/metal layer, such as TiN/TiAlC/W.

[0028] The first and second ferroelectric layers 120 and 130 may be laminated between, e.g. may be directly between, the semiconductor substrate 101 and the gate electrode 170 in a direction perpendicular to the semiconductor substrate 101. The first and second ferroelectric layers 120 and 130 may each include a ferroelectric material including a certain dopant. The first and second ferroelectric layers 120 and 130 may include the same material; however, example embodiments are not limited thereto, and the first and second ferroelectric layers 120 and 130 may include different materials from each other.

[0029] Ferroelectric materials refer to a material having ferroelectricity to maintain spontaneous polarization by aligning internal electric dipole moments. Ferroelectric materials have remnant polarization by a dipole even

when no electric field from outside is applied thereto. In ferroelectric materials, a polarization direction may be switched in units of domains by an external electric field dopant unit.

[0030] The first and second ferroelectric layers 120 and 130 may each independently or concurrently include, for example, one or more of a nitride-based material, perovskite, or a fluorite-based material. The nitride-based material may include, for example AlScN, and perovskite may include, for example, PZT, BaTiOs, PbTiOs, etc. However, example embodiments are not limited thereto. The fluorite-based material may include, for example, an oxide of at least one selected from Hf, Si, Al, Zr, Y, La, Gd, and Sr. More specifically, the fluorite-based material may include at least one of a hafnium oxide (HfO), a zirconium oxide (ZrO), and a hafnium-zirconium oxide (HfZrO).

[0031] The first and second ferroelectric layers 120 and 130 may each include a certain dopant. For example, the first and second ferroelectric layers 120 and 130 may each include a hafnium oxide injected with or incorporating a certain dopant. The dopant may include, for example, at least one of Zr, La, Al, Si, and Y. However, example embodiments are not limited thereto. For example, the content of Zr dopant included in the hafnium oxide may be about 20at% or more (for example, about 30at% or more, for example, about 40at% or more) and about 80at% or less (for example, about 70at% or less, for example about 60at% or less). For example, the first and second ferroelectric layers 120 and 130 may each include an aluminum nitride injected with a certain dopant. The dopant may include, for example, at least one of B and Sc; however, example embodiments are not limited thereto. The first ferroelectric layer 120 and the second ferroelectric layer 130 may include the same and/or different dopants from each other.

[0032] The first and second ferroelectric layers 120 and 130 may each include an imprinted ferroelectric material. The "imprint of ferroelectric material" refers to a phenomenon in which hysteresis characteristics of a ferroelectric material move along a voltage axis in a polarization (P) - voltage (V) characteristics curve of the ferroelectric material. The imprint of ferroelectric material includes a negative (-) imprint which involves hysteresis characteristics of a ferroelectric material moving in the negative (-) voltage direction and a positive (+) imprint which involves hysteresis characteristics of a ferroelectric material moving in the positive (+) voltage direction. Such an imprint of ferroelectric material may be caused by asymmetry of ferroelectricity of the ferroelectric material. The asymmetry of ferroelectricity may occur when a doping concentration gradient is generated due to change of dopant concentration according to a position in a ferroelectric material, and/or from formation of different material layers at upper and lower interfaces of the ferroelectric material. The greater the asymmetry of ferroelectricity in a ferroelectric material is, the greater the imprint of the ferroelectric material may be.

[0033] The first and second ferroelectric layers 120 and 130 may include ferroelectric materials imprinted in opposite directions to each other. More specifically, the first ferroelectric layer 120 may include a ferroelectric layer imprinted in a negative (-) voltage direction, and the second ferroelectric layer 130 may include a ferroelectric layer imprinted in a positive (+) voltage direction. As described below, as the lamination structure of the first and second ferroelectric layers 120 and 130 imprinted in opposite directions to each other is provided between the semiconductor substrate 101 and the gate electrode 170, multi-bit having a multi-level of three or more levels may be implemented.

[0034] FIG. 2A illustrates a capacitor including a ferroelectric layer 120' imprinted in the (-) voltage direction, and FIG. 2B illustrates polarization (P) - voltage (V) characteristics of the ferroelectric layer 120' of the capacitor illustrated in FIG. 2A.

[0035] Referring to FIG. 2A, the ferroelectric layer 120' imprinted in the (-) voltage direction may be provided between two metal electrodes 11 and 12. The ferroelectric layer 120' imprinted in the (-) voltage direction may have a doping concentration gradient in which concentration of a dopant varies (e.g., various linearly or continuously, such as monotonically) in a thickness direction of the ferroelectric layer 120'. For example, the ferroelectric layer 120' imprinted in the (-) voltage direction may have a doping concentration gradient in which concentration of a dopant increases from a lower portion of the ferroelectric layer 120' to an upper portion. The concentration gradient may be concave and/or convex, and in some example embodiments may be monotonic; example embodiments are not limited thereto; in some cases, the concentration gradient may be discontinuous. The ferroelectric layer 120' imprinted in the (-) voltage direction may include a ferroelectric material layer and interface layers including different materials at upper and lower interfaces of the ferroelectric material layer.

[0036] Referring to FIG. 2B, "h0" represents a hysteresis curve of an unimprinted ferroelectric layer, "h1," "h2," and "h3" respectively represent hysteresis curves of the ferroelectric layer 120' imprinted in the (-) voltage direction. The greater the imprint degree of the ferroelectric layer 120' in the (-) voltage direction is, the more the hysteresis curve of the ferroelectric layer 120' may move towards "h3".

[0037] FIG. 3A illustrates a capacitor including a ferroelectric layer 130' imprinted in the (+) voltage direction, and FIG. 3B illustrates polarization (P) - voltage (V) characteristics of the ferroelectric layer 130' of the capacitor illustrated in FIG. 3A.

[0038] Referring to FIG. 3A, the ferroelectric layer 130' imprinted in the (+) voltage direction may be provided between two metal electrodes 11 and 12. The ferroelectric layer 130' imprinted in the (+) voltage direction may have a doping concentration gradient in which concentration of a dopant varies in a thickness direction of the ferroelectric layer 130'. The ferroelectric layer 130' im-

printed in the (+) voltage direction may have a doping concentration gradient that is opposite to that of the ferroelectric layer 120' imprinted in the (-) voltage direction. For example, the ferroelectric layer 130' imprinted in the (+) voltage direction may have a doping concentration gradient in which concentration of a dopant decreases, e.g. decreases monotonically and/or continuously, from a lower portion of the ferroelectric layer 130' to an upper portion. The ferroelectric layer 130' imprinted in the (+) voltage direction may include a ferroelectric material layer and interface layers including different materials at upper and lower interfaces of the ferroelectric material layer.

[0039] Referring to FIG. 3B, "h0" represents a hysteresis curve of an unimprinted ferroelectric layer, "h1," "h2," and "h3" respectively represent hysteresis curves of the ferroelectric layer 130' imprinted in the (+) voltage direction. The greater the imprint degree of the ferroelectric layer 130' in the (+) voltage direction is, the more the hysteresis curve of the ferroelectric layer 130' may move towards "h3".

[0040] FIG. 4A is a diagram of a capacitor including a lamination structure of the first ferroelectric layer 120 imprinted in the (-) voltage direction and the second ferroelectric layer 130 imprinted in the (+) voltage direction. The first and second ferroelectric layers 120 and 130 illustrated in FIG. 4A may be the same as the first and second ferroelectric layers 120 and 130 illustrated in FIG. 1.

[0041] Referring to FIG. 4A, the first ferroelectric layer 120 and the second ferroelectric layer 130 may be laminated between the two metal electrodes 11 and 12 in a direction perpendicular to the metal electrodes 11 and 12. The first and second ferroelectric layers 120 and 130 may be imprinted in opposite directions to each other. More specifically, the first ferroelectric layer 120 may be imprinted in the (-) voltage direction, and the second ferroelectric layer 130 may be imprinted in the (+) voltage direction. A thickness of the first ferroelectric layer 120 may be the same as, greater than, or less than that of the second ferroelectric layer 130.

[0042] The first and second ferroelectric layers 120 and 130 may each have a doping concentration gradient in which concentration of a dopant varies in a thickness direction. More specifically, the first ferroelectric layer 120 imprinted in the (-) voltage direction may have a concentration gradient in which doping concentration of a dopant increases from a lower portion of the first ferroelectric layer 120 towards an upper portion of the first ferroelectric layer 120, and the second ferroelectric layer 130 imprinted in the (+) voltage direction may have a concentration gradient in which doping concentration of a dopant decreases from a lower portion of the second ferroelectric layer 130 towards an upper portion of the second ferroelectric layer 130.

[0043] FIG. 5A illustrates a first ferroelectric layer 120a imprinted in the (-) voltage direction. In FIG. 5A, "MO" represents a metal oxide, and "HfO" represents a metal dopant included in a hafnium oxide (HfO). Referring to

FIG. 5A, the thickness of the hafnium oxide (HfO) layer may increase towards the lower portion of the first ferroelectric layer 120a, and the thickness of the metal oxide (MO) layer including the metal dopant may increase towards the upper portion of the first ferroelectric layer 120a. Accordingly, the first ferroelectric layer 120a imprinted in the (-) voltage direction may have a concentration gradient in which concentration of a dopant increases from the lower portion of the first ferroelectric layer 120a towards the upper portion of the first ferroelectric layer 120a.

[0044] FIG. 5B illustrates a first ferroelectric layer 120b imprinted in the (-) voltage direction. The first ferroelectric layer 120b imprinted in the (-) voltage direction illustrated in FIG. 5B may have a concentration gradient continuously increasing (e.g., monotonically increasing) from the lower portion of the first ferroelectric layer 120b towards the upper portion of the first ferroelectric layer 120b. The first ferroelectric layer 120b illustrated in FIG. 5B may be formed by annealing the first ferroelectric layer 120a illustrated in FIG. 5A.

[0045] FIG. 6A illustrates a second ferroelectric layer 130a imprinted in the (+) voltage direction. Referring to FIG. 6A, the thickness of the hafnium oxide (HfO) layer may increase towards the upper portion of the second ferroelectric layer 130a, and the thickness of the metal oxide (MO) layer including the metal dopant may increase towards the lower portion of the second ferroelectric layer 130a. Accordingly, the second ferroelectric layer 130a imprinted in the (+) voltage direction may have a concentration gradient in which concentration of a dopant decreases from the lower portion of the second ferroelectric layer 130a towards the upper portion of the second ferroelectric layer 130a.

[0046] FIG. 6B illustrates a second ferroelectric layer 130b imprinted in the (+) voltage direction. The second ferroelectric layer 130b imprinted in the (+) voltage direction illustrated in FIG. 6B may have a concentration gradient continuously decreasing from the lower portion of the second ferroelectric layer 130b towards the upper portion of the second ferroelectric layer 130b. The second ferroelectric layer 130b illustrated in FIG. 6B may be formed by annealing the second ferroelectric layer 130a illustrated in FIG. 6A.

[0047] The foregoing embodiments describe the case in which, in the first ferroelectric layer (120a and 120b) imprinted in the (-) voltage direction, the doping concentration of a dopant increases from the lower portion towards the upper portion of the first ferroelectric layer (120a and 120b), and in the second ferroelectric layer (130a and 130b) imprinted in the (+) voltage direction, the doping concentration of a dopant decreases, e.g. decreases continuously or monotonically, from the lower portion towards the upper portion of the second ferroelectric layer (130a and 130b). However, example embodiments are not limited thereto, and according to a charge state, in the first ferroelectric layer imprinted in the (-) voltage direction, the doping concentration of a dopant decreases-

es from the lower portion to the upper portion of the first ferroelectric layer, and in the second ferroelectric layer imprinted in the (+) voltage direction, the doping concentration of a dopant increases from the lower portion to the upper portion of the second ferroelectric layer.

[0048] FIG. 7 illustrates a first ferroelectric layer 220 imprinted in the (-) voltage direction, and FIG. 8 illustrates a second ferroelectric layer 230 imprinted in the (+) voltage direction.

[0049] Referring to FIG. 7, the first ferroelectric layer 220 may include a first ferroelectric material layer 223 and first and second interface layers 221 and 222 respectively provided on upper and lower surfaces of the first ferroelectric material layer 223. The first ferroelectric material layer 223 may include, for example, one or more of a nitride-based material, perovskite, a fluorite-based material, etc., and may further include a certain dopant. The first interface layer 221 provided on the upper surface of the first ferroelectric material layer 223 and the second interface layer 222 provided on the lower surface of the first ferroelectric material layer 223 may include different materials from each other. The first and second interface layers 221 and 222 may each include, for example, at least one of SiO_2 , Al_2O_3 , La_2O_3 , and Y_2O_3 . For example, one of the first and second interface layers 221 and 222 may include Al_2O_3 and may not include SiO_2 and the other one may include SiO_2 , and may not include Al_2O_3 . However, the foregoing is provided only as an example.

[0050] By forming the first and second interface layers 221 and 222 including different materials from each other on the upper and lower surfaces of the first ferroelectric material layer 223, asymmetry of ferroelectricity may occur, and accordingly, the first ferroelectric layer 220 imprinted in the (-) voltage direction may be formed.

[0051] Referring to FIG. 8, the second ferroelectric layer 230 may include a second ferroelectric material layer 233 and third and fourth interface layers 231 and 232 respectively provided on upper and lower surfaces of the second ferroelectric material layer 233. The second ferroelectric material layer 233 may include a material identical to or different from the first ferroelectric material layer 223. The third interface layer 231 provided on the upper surface of the second ferroelectric material layer 233 and the fourth interface layer 232 provided on the lower surface of the second ferroelectric material layer 233 may include different materials from each other. The third and fourth interface layers 231 and 232 may each include, for example, at least one of SiO_2 , Al_2O_3 , La_2O_3 , and Y_2O_3 .

[0052] The fourth interface layer 232 formed on the lower surface the second ferroelectric material layer 233 and the first interface layer 221 formed on the upper surface of the first ferroelectric material layer 223 may include the same material. The third interface layer 231 formed on the upper surface of the second ferroelectric material layer 233 and the second interface layer 222 formed on the lower surface of the first ferroelectric material layer 223 may include the same material.

[0053] By forming the third and fourth interface layers 231 and 232 including different materials from each other on the upper and lower surfaces of the second ferroelectric material layer 233, asymmetry of ferroelectricity may occur, and accordingly, the second ferroelectric layer 230 imprinted in the (+) voltage direction may be formed.

[0054] Similar to the first and second ferroelectric layers 120 and 130 in FIG. 1, as the first and second ferroelectric material layers 223 and 233 have a doping concentration gradient in which concentration of a dopant varies in the thickness direction, asymmetry of ferroelectricity may further increase. For example, the first ferroelectric material layer 223 may have a concentration gradient in which doping concentration of a dopant increases from the lower portion towards the upper portion of the first ferroelectric material layer 223, and the second ferroelectric material layer 233 may have a concentration gradient in which doping concentration of a dopant decreases from the lower portion to the upper portion of the second ferroelectric material layer 233.

[0055] FIG. 4B illustrates polarization (P) - voltage (V) characteristics of a lamination structure of the first and second ferroelectric layers 120 and 130 of the capacitor illustrated in FIG. 4A.

[0056] FIG. 4B shows hysteresis curves (H1, H2, and H3) of lamination structure of the first ferroelectric layer 120 imprinted in the (-) voltage direction and the second ferroelectric layer 130 imprinted in the (+) voltage direction. Each hysteresis curve may have combined characteristics of hysteresis characteristics of the first ferroelectric layer 120 imprinted in the (-) voltage direction and hysteresis characteristics of the second ferroelectric layer 130 imprinted in the (+) voltage direction. In the lamination structure of the first and second ferroelectric layers 120 and 130, the more the imprint degree of the first and second ferroelectric layers 120 and 130 increases, the more the hysteresis curve of the lamination structure of the first and second ferroelectric layers 120 and 130 moves towards "H3".

[0057] FIG. 9 is a diagram illustrating one of the polarization (P) - voltage (V) characteristics illustrated in FIG. 4B.

[0058] Referring to FIG. 9, when an applied voltage is 0 V, multi-bit functionality wherein a single cell has three levels of different polarization states, e.g., multi-bit functionality wherein a single memory cell has A, B, and C levels may be implemented. FIG. 9 illustrates a polarization state in the first and second ferroelectric layers 120 and 130 at each level (A, B, and C). For example, at the A level, both of the first and second ferroelectric layers 120 and 130 may have an upward polarization direction. At the B level, the first ferroelectric layer 120 may have an upward polarization direction, and the second ferroelectric layer 130 may have a downward polarization direction. At the C level, both of the first and second ferroelectric layers 120 and 130 may have a downward polarization direction.

[0059] As such, as the lamination structure of the first

ferroelectric layer 120 imprinted in the (-) voltage direction and the second ferroelectric layer 130 imprinted in the (+) voltage direction is provided between the semiconductor substrate 101 and the gate electrode 170, multi-bit functionality having three levels in different polarization states may be implemented.

[0060] FIG. 10 is a diagram illustrating an example of the number of levels of the lamination structure of the first and second ferroelectric layers 120 and 130 illustrated in FIG. 4A which may be implemented according to an imprint voltage. In FIG. 10, the "imprint voltage" refers to a voltage level moving along a voltage axis of a hysteresis curve. Here, the material used for the first and second ferroelectric layers 120 and 130 is HfZrO (Hf:Zr=1:1).

[0061] Referring to FIG. 10, when the imprint voltage is less than 1.8 V, 2-level characteristics may be shown, and when the imprint voltage is about 1.8 V to about 3 V, 3-level characteristics may be implemented. When the imprint voltage is greater than 3 V, 1-level characteristics may be shown, which leads to loss of non-volatile characteristics.

[0062] As such, as the lamination structure of the first ferroelectric layer 120 imprinted in the (-) voltage direction and the second ferroelectric layer 130 imprinted in the (+) voltage direction is provided between the semiconductor substrate 101 and the gate electrode 170, multi-bit having a multi-level of three levels may be implemented.

[0063] FIG. 11 is a cross-sectional view of a memory device 300 according to various example embodiments. Hereinafter, differences from the above-described embodiments will be provided mainly.

[0064] Referring to FIG. 11, the memory device 300 may include the semiconductor substrate 101, the gate electrode 170, the first and second ferroelectric layers 120 and 130 laminated between the semiconductor substrate 101 and the gate electrode 170, and a paraelectric layer 361 provided between the first and second ferroelectric layers 120 and 130.

[0065] The first and second ferroelectric layers 120 and 130 may be laminated between the semiconductor substrate 101 and the gate electrode 170 in a direction perpendicular to the semiconductor substrate 101. The first and second ferroelectric layers 120 and 130 may include ferroelectric materials imprinted in opposite directions to each other. For example, the first ferroelectric layer 120 may include a ferroelectric layer imprinted in the (-) voltage direction, and the second ferroelectric layer 130 may include a ferroelectric layer imprinted in the (+) voltage direction. As the first and second ferroelectric layers 120 and 130 are already described above, any redundant description will be omitted.

[0066] The paraelectric layer 361 may be provided between the first and second ferroelectric layers 120 and 130. The paraelectric layer 361 may be provided to adjust ferroelectric characteristics of the first and second ferroelectric layers 120 and 130. The paraelectric layer 361

may include at least one of SiO₂, Al₂O₃, La₂O₃, and Y₂O₃. However, this is just an example, and the paraelectric layer 361 may include various other dielectric materials. A paraelectric layer 362 may be provided between the gate electrode 170 and the first ferroelectric layer 120.

[0067] FIG. 12 is a cross-sectional view of a memory device 400 according to various example embodiments. Hereinafter, differences from the above-described embodiments will be provided mainly.

[0068] Referring to FIG. 12, the memory device 400 may include the semiconductor substrate 101, the gate electrode 170, a first anti-ferroelectric layer 420 and a second anti-ferroelectric layer 430 laminated between the semiconductor substrate 101 and the gate electrode 170. The insulating layer 105 may be further provided on a surface of the semiconductor substrate 101. The gate electrode 170 may be provided on the semiconductor substrate 101.

[0069] The first and second anti-ferroelectric layers 420 and 430 may be laminated between the semiconductor substrate 101 and the gate electrode 170 in the direction perpendicular to the semiconductor substrate 101. The first and second anti-ferroelectric layers 420 and 430 may each include an anti-ferroelectric material including a certain dopant.

[0070] Anti-ferroelectric materials may include an array of electric dipoles, but the remnant polarization may be 0 or close to 0. As the directions of adjacent dipoles become opposite to each other when there is no electric field, which leads to offset of polarization, the overall spontaneous polarization and remnant polarization may be 0 or close to 0. However, when an external electric field is applied, polarization characteristics and switching characteristics may be shown.

[0071] The first and second anti-ferroelectric layers 420 and 430 may each include, for example, a nitride-based material, perovskite, or a fluorite-based material. The anti-ferroelectric material may have a different crystal structure from that of a ferroelectric material. For example, a crystal structure of a tetragonal system may have anti-ferroelectricity, and a crystal structure of an orthorhombic system may have ferroelectricity.

[0072] For example, the first and second anti-ferroelectric layers 420 and 430 may each include a zirconium oxide injected with a certain dopant. The dopant may include, for example, at least one of Al, Ga, Co, Ni, Mg, In, La, Y, Nd, Sm, Er, Sr, Ba, Gd, Ge, N, and Si. However, this is only an example.

[0073] The first and second anti-ferroelectric layers 420 and 430 may each include an imprinted anti-ferroelectric material. The "imprint of anti-ferroelectric material" refers to a phenomenon in which hysteresis characteristics of an anti-ferroelectric material move along a voltage axis in a polarization (P) - voltage (V) characteristics curve of the anti-ferroelectric material. The imprint of anti-ferroelectric material includes a (-) imprint which involves hysteresis characteristics of an anti-ferroelectric material moving in the (-) voltage direction and a (+) imprint which

involves hysteresis characteristics of an anti-ferroelectric material moving in the (+) voltage direction. Such imprint of anti-ferroelectric material may be caused by asymmetry of anti-ferroelectricity of an anti-ferroelectric material. The asymmetry of anti-ferroelectricity may occur when a doping concentration gradient is generated due to change of dopant concentration according to a position in an anti-ferroelectric material and/or to a formation of different material layers at upper and lower interfaces of the anti-ferroelectric material. The greater the asymmetry of anti-ferroelectricity in an anti-ferroelectric material is, the greater the imprint of the ferroelectric material may be.

[0074] The first and second anti-ferroelectric layers 420 and 430 may include anti-ferroelectric materials imprinted in opposite directions to each other. More specifically, the first anti-ferroelectric layer 420 may include an anti-ferroelectric layer imprinted in the (-) voltage direction, and the second anti-ferroelectric layer 430 may include an anti-ferroelectric layer imprinted in the (+) voltage direction. As such, as the lamination structure of the first and second anti-ferroelectric layers 420 and 430 imprinted in opposite directions to each other is provided between the semiconductor substrate 101 and the gate electrode 170, multi-bit may be implemented.

[0075] Although it is not shown in the drawings, a paraelectric layer for adjusting paraelectric characteristics may be further provided between the first and second anti-ferroelectric layers 420 and 430, and a paraelectric layer may also be provided between the gate electrode 170 and the first anti-ferroelectric layer 420.

[0076] FIG. 13 is a cross-sectional view of a memory device 500 according to various example embodiments. Hereinafter, differences from the above-described embodiments will be provided mainly.

[0077] Referring to FIG. 13, the memory device 500 may include the semiconductor substrate 101, the gate electrode 170, a first anti-ferroelectric layer 520, a second anti-ferroelectric layer 530, and a third anti-ferroelectric layer 540 laminated between the semiconductor substrate 101 and the gate electrode 170. The first to third ferroelectric layers 520, 530, and 540 may be laminated between the semiconductor substrate 101 and the gate electrode 170 in the direction perpendicular to the semiconductor substrate 101.

[0078] The first and second ferroelectric layers 520 and 530 respectively provided on upper and lower surfaces of the third ferroelectric layer 540 may include ferroelectric materials imprinted in opposite directions to each other. For example, the first ferroelectric layer 520 may include a ferroelectric layer imprinted in the (-) voltage direction, and the second ferroelectric layer 530 may include a ferroelectric layer imprinted in the (+) voltage direction. The third ferroelectric layer 540 may include an unimprinted ferroelectric material. Although FIG. 13 illustrates the case in which the first to third ferroelectric layers 520, 530, and 540 are sequentially laminated on a lower surface of the gate electrode 170, this is just an example,

and the lamination order of the first to third ferroelectric layers 520, 530, and 540 may vary.

[0079] As such, as the memory device 500 includes the first and second ferroelectric layers 520 and 530 imprinted in opposite directions to each other and the lamination structure of three ferroelectric layers (520, 530, and 540) including the unimprinted third ferroelectric layer 540, multi-bit having multi-level characteristics of maximum 4 levels may be implemented. Accordingly, more information (e.g., more logic levels) may be stored in the memory device 500.

[0080] FIG. 14A is a diagram of a capacitor including a lamination structure of the first ferroelectric layer 520, the second ferroelectric layer 530, and the third ferroelectric layer 540 illustrated in FIG. 13.

[0081] FIG. 14A illustrates a capacitor including a lamination structure of the first ferroelectric layer 520 imprinted in the (-) voltage direction, the second ferroelectric layer 530 imprinted in the (+) voltage direction, and the unimprinted third ferroelectric layer 540 between the two metal electrodes 11 and 12.

[0082] FIG. 14B is a diagram illustrating polarization (P)-voltage (V) characteristics of the lamination structure of the first, second, and third ferroelectric layers 520, 530, and 540 illustrated in FIG. 14A. In FIG. 14B, "L1" represents a hysteresis curve which may be obtained when a voltage, e.g., a maximum applied voltage is about 2 V, and "L2" represents a hysteresis curve which may be obtained when a voltage, e.g., a maximum applied voltage is about 1 V.

[0083] Referring to FIG. 14B, in the capacitor illustrated in FIG. 14A, when the applied voltage is 0V, four levels (i.e., A, B, C, and D levels) having different polarization states may be implemented. More specifically, when the applied voltage is about 2 V to 0 V, A and D levels may be implemented by the "L1" hysteresis curve, and when the applied voltage is about 1 V to 0 V, B and C levels may be implemented by the "L2" hysteresis curve. FIG. 14B illustrates a polarization state in the first to third ferroelectric layers 520, 530, and 540 at each level (A, B, C, and D). As such, in the lamination structure including three ferroelectric layers (520, 530, and 540), by adjusting a maximum applied voltage, four levels having different polarization states may be implemented.

[0084] FIG. 15 is a diagram illustrating an example of the number of levels of the lamination structure of the first to third ferroelectric layers 520, 530, and 540 illustrated in FIG. 14A which may be implemented according to an imprint voltage. Here, the material used for the first, second, and third ferroelectric layers 520, 530, and 540 is HfZrO (Hf:Zr=1:1).

[0085] Referring to FIG. 15, when the imprint voltage is less than 2.8 V, 2-level characteristics may be shown, and when the imprint voltage is about 2.8 V to about 3.5 V, 4-level characteristics may be implemented. When the imprint voltage is greater than 3.5 V, 2-level characteristics may be shown. Accordingly, in the memory device 500 including the lamination structure including the first

to third ferroelectric layers 520, 530, and 540, by adjusting the imprint voltage, 4-level characteristics may be implemented.

[0086] According to the an exemplary embodiment, the imprint voltage may be about 1.8V or more (for example, about 2.0V or more, for example about 2.5V or more, for example 2.7V or more) and about 3.5V or less (for example, about 3.3V or less).

[0087] The foregoing example embodiments describe the case in which the memory device 500 includes the lamination structure of the first to third ferroelectric layers 520, 530, and 540; however, the memory device 500 may include a lamination structure of first to third anti-ferroelectric layers. The first and second anti-ferroelectric layers may include anti-ferroelectric materials imprinted in opposite directions to each other, and the third anti-ferroelectric layer may include an unimprinted anti-ferroelectric material.

[0088] FIG. 16 is a cross-sectional view of a memory device 600 according to various example embodiments.

[0089] Referring to FIG. 16, the memory device 600 may include the semiconductor substrate 101, the gate electrode 170, the first to third ferroelectric layers 520, 530, and 540 laminated between the semiconductor substrate 101 and the gate electrode 170, and paraelectric layers 561 and 562 provided between the first to third ferroelectric layers 520, 530, and 540.

[0090] The first to third ferroelectric layers 520, 530, and 540 are the same as the first to third ferroelectric layers 520, 530, and 540 illustrated in FIG. 13. The first and second ferroelectric layers 520 and 530 may include ferroelectric materials imprinted in opposite directions to each other, and the third ferroelectric layer 540 may include an unimprinted ferroelectric material.

[0091] The paraelectric layers 561 and 562 may be provided between the first and second ferroelectric layers 520 and 530 and between the second and third ferroelectric layers 530 and 540 to adjust ferroelectric characteristics. The paraelectric layers 561 and 562 may independently or concurrently include at least one of SiO_2 , Al_2O_3 , La_2O_3 , and Y_2O_3 . A paraelectric layer 563 may be provided between the gate electrode 170 and the first ferroelectric layer 520. Thicknesses of each of the paraelectric layers 561, 562, and 563 may be the same; alternatively a thickness of any one of the paraelectric layers 561, 562, and 563 may be different from another of the paraelectric layers 561, 562, and 563. Although example embodiments describe the cases in which the paraelectric layers 561 and 562 are provided between every adjacent ferroelectric layers (520, 530, and 540), the paraelectric layer may be provided at one of areas between the adjacent ferroelectric layers (520, 530, and 540).

[0092] FIG. 17 is a cross-sectional view of a memory device 700 according to various example embodiments. FIG. 17 only illustrates a lamination structure provided between the semiconductor substrate 101 and the gate electrode 170 for convenience sake.

[0093] Referring to FIG. 17, the memory device 700 may include a plurality of ferroelectric layers laminated between the semiconductor substrate 101 and the gate electrode 170. The plurality of ferroelectric layers may include a plurality of first ferroelectric layers (720-1, 720-2,..., 720-n), a plurality of second ferroelectric layers (730-1, 730-2,..., 730-n), and a third ferroelectric layer 740.

[0094] The first ferroelectric layers (720-1, 720-2,..., 720-n) and the second ferroelectric layers (730-1, 730-2,..., 730-n) may include ferroelectric materials imprinted in opposite directions to each other. For example, the first ferroelectric layers (720-1, 720-2,..., 720-n) may be imprinted in the (-) voltage direction, and include ferroelectric materials having different imprint degrees from each other. The second ferroelectric layers (730-1, 730-2,..., 730-n) may be imprinted in the (+) voltage direction, and include ferroelectric materials having different imprint degrees from each other. The third ferroelectric layer 740 may include an unimprinted ferroelectric material.

[0095] FIG. 17 illustrates an example of a lamination structure including $2n+1$ ferroelectric layers including n first ferroelectric layers (720-1, 720-2,..., 720-n), n second ferroelectric layers (730-1, 730-2,..., 730-n), and one third ferroelectric layer 740. The memory device 700 including the lamination structure illustrated in FIG. 17 may implement a maximum of $2n+2$ levels. When the memory device 700 further includes an additional material layer in addition to the aforementioned ferroelectric layers, the memory device 700 may implement $2n+2$ levels or more.

[0096] The lamination order of ferroelectric layers illustrated in FIG. 17 is just an example and may vary. The foregoing example embodiments illustrate the case in which the memory device 700 includes a plurality of ferroelectric layers; however, the memory device 700 may include a plurality of anti-ferroelectric layers.

[0097] FIG. 18 is a cross-sectional view of a memory device 770 according to various example embodiments. FIG. 18 only illustrates a lamination structure provided between the semiconductor substrate 101 and the gate electrode 170 for convenience sake.

[0098] Referring to FIG. 18, the memory device 770 may include a plurality of ferroelectric layers laminated between the semiconductor substrate 101 and the gate electrode 170 and a plurality of paraelectric layers 761. The plurality of ferroelectric layers may include a plurality of first ferroelectric layers (720-1, 720-2,..., 720-n), a plurality of second ferroelectric layers (730-1, 730-2,..., 730-n), and a third ferroelectric layer 740, which are already described in the aforementioned embodiments.

[0099] The plurality of paraelectric layers 761 may be provided between the plurality of ferroelectric layers to adjust ferroelectric characteristics. The paraelectric layers 761 may independently or concurrently include at least one of SiO_2 , Al_2O_3 , La_2O_3 , and Y_2O_3 ; however, example embodiments are not limited thereto. FIG. 18 illustrates the case in which the paraelectric layers 761

are provided between every adjacent ferroelectric layers. However, example embodiments are not limited thereto, and the paraelectric layers 761 may be provided between some of areas between adjacent ferroelectric layers.

[0100] The aforementioned memory devices (i.e., FEFET) may be employed in various electronic apparatuses. For example, the memory devices may be used as a memory cell, a plurality of memory cells may be arranged in a 2D manner, arranged in vertical or horizontal direction, or arranged in one direction to form a memory string cell, and a plurality of memory string cells may be arranged in a 2D manner, etc. to form a memory cell array. The aforementioned memory devices may be a part of an electronic circuit constituting an electronic apparatus, along with other circuit elements.

[0101] FIG. 19 is a perspective view schematically illustrating a memory apparatus 3700 according to some example embodiments. The memory apparatus 3700 illustrated in FIG. 19 may be a vertical non-volatile memory apparatus (for example, VNAND apparatus). FIG. 20 is a diagram illustrating a cross-section of a cell string CS of the memory apparatus 3700 illustrated in FIG. 19.

[0102] Referring to FIGS. 19 and 20, the memory apparatus 3700 may include a plurality of cell strings CS arranged on a substrate 3701. Each cell string CS may extend in a direction perpendicular to the substrate 3701 (z-axis direction). The plurality of cell strings CS may be arranged in various forms on the substrate 3701.

[0103] Each cell string CS may include a plurality of memory cells MC laminated in the direction perpendicular to the substrate 3701 (z-axis direction). Each memory cell MC may have the same configuration as the memory devices (100, 300, 400, 500, 600, and 700) according to the aforementioned embodiments.

[0104] The substrate 3701 may include various materials. For example, the substrate 3701 may include a single-crystal silicon substrate, a compound semiconductor substrate, or silicon-on-insulator (SOI) substrate; however, example embodiments are not limited thereto. The substrate 3701 may further include, for example, an impurity area due to doping, an electronic device such as a transistor, etc., a periphery circuit which selects and controls memory cells storing data, etc.

[0105] A plurality of gate electrodes 3710 may be laminated apart from each other in a direction perpendicular to the substrate 3701. Each gate electrode 3710 may extend in a direction parallel with the substrate 3701. The gate electrode 3710 is to control corresponding channel layer 3720, and a word line may be electrically connected to the gate electrode 3710. A voltage turning on/off the corresponding channel layer 3720 may be selectively applied to the gate electrode 3710.

[0106] The gate electrode 3710 may include a conductive material such as a metal, a metal nitride, a metal oxide, polysilicon such as doped polysilicon, etc. However, this is just an example, and the gate electrode 3710 may include various other conductive materials. A plurality of interlayer-insulating layers 3715 may be laminat-

ed between the gate electrodes 3710 in the direction perpendicular to the substrate 3701. The interlayer-insulating layers 3715 may function as spacer layers for insulation between the gate electrodes 3710. The interlayer-insulating layers 3715 may each include, for example, a silicon oxide, a silicon nitride, etc.; however, example embodiments are not limited thereto.

[0107] A plurality of ferroelectric layers 3730 and 3740 and the channel layer 3720 may be sequentially provided on the inner surface of the gate electrode 3710. The plurality of ferroelectric layers 3730 and 3740 and the channel layer 3720 may each extend perpendicular to the substrate 3701 and may be shared by the plurality of memory cells MC. A source and a drain may be provided under and on the channel layer 3720, and the source and the drain may be connected to a common source line and a bit line.

[0108] A through hole penetrating the gate electrodes 3710 and the interlayer-insulating layers 3715 may be formed in the direction perpendicular to the substrate 3701, and the through hole may be formed to have, for example, a circular cross-section. The plurality of ferroelectric layers 3730 and 3740 and the channel layer 3720 may be sequentially provided on the inner wall of the through hole in the direction parallel with the substrate 3701. The plurality of ferroelectric layers 3730 and 3740 and the channel layer 3720 may each have a cylindrical shape extending in the direction perpendicular to the substrate 3701.

[0109] The channel layer 3720 may include a semiconductor material. For example, the channel layer 3720 may include a Group IV semiconductor such as Si, Ge, SiGe, etc., or include a Groups III-V semiconductor compound. The channel layer 3720 may include, for example, an oxide semiconductor, a nitride semiconductor, an oxynitride semiconductor, a 2D semiconductor material, a quantum dot, or an organic semiconductor. The oxide semiconductor may include, for example, InGaZnO, etc., the 2D semiconductor material may include, for example, TMD or graphene, and the quantum dot may include a colloidal quantum dot, a nanocrystal structure, etc. However, this is just an example, and example embodiments are not limited thereto.

[0110] The channel layer 3720 may further include a dopant. The dopant may include a p-type dopant or an n-type dopant. The p-type dopant may include, for example, a Group III element, such as B, Al, Ga, In, etc., and the n-type dopant may include, for example, a Group V element, such as P, As, Sb, etc. A filling insulating layer 3760 be provided on an inner surface of the channel layer 3720 to fill the through hole. The filling insulating layer 3760 may include, for example, a silicon oxide, air, etc.; however, example embodiments are not limited thereto.

[0111] The plurality of ferroelectric layers 3730 and 3740 may be provided between the gate electrode 3710 and the channel layer 3720. The plurality of ferroelectric layers 3730 and 3740 may include a first ferroelectric layer 3730 and a second ferroelectric layer 3740 lami-

nated in the direction parallel with the substrate 3701. The first and second ferroelectric layers 3730 and 3740 may be the first and second ferroelectric layers 120 and 130 illustrated in FIG. 1. Accordingly, any redundant description thereon is omitted.

[0112] The first and second ferroelectric layers 3730 and 3740 may each include, a nitride-based material, perovskite, a fluorite-based material etc. The first and second ferroelectric layers 3730 and 3740 may each include a certain dopant. For example, the first and second ferroelectric layers 3730 and 3740 may each include a hafnium oxide injected with a dopant including at least one of Zr, La, Al, Si, and Y. For example, the first and second ferroelectric layers 3730 and 3740 may each include an aluminum nitride injected with a dopant including at least one of B and Sc.

[0113] The first and second ferroelectric layers 3730 and 3740 may each include an imprinted ferroelectric material. The first and second ferroelectric layers 3730 and 3740 may include ferroelectric materials imprinted in opposite directions to each other. For example, the first ferroelectric layer 3730 may include a ferroelectric layer imprinted in the (-) voltage direction, and the second ferroelectric layer 3740 may include a ferroelectric layer imprinted in the (+) voltage direction. As such, as the lamination structure of the first and second ferroelectric layers 3730 and 3740 imprinted in opposite directions to each other is provided between the channel layer 3720 and the gate electrode 3710, each memory cell MC may implement multi-bit functionality having a multi-level of three or more levels. Accordingly there may be improvements in the integration of and/or density of a memory device according to example embodiments.

[0114] Similar to FIGS. 7 and 8, the first ferroelectric layer 3730 may include a first ferroelectric material layer and first and second interface layers respectively provided on upper and lower surfaces of the first ferroelectric material layer, and the second ferroelectric layer 3740 may include a second ferroelectric material layer and third and fourth interface layers respectively provided on upper and lower surfaces of the second ferroelectric material layer. The lamination structure provided between the channel layer 3720 and the gate electrode 3710 may include a plurality of first ferroelectric layers and a plurality of second ferroelectric layers, and the lamination structure may include a paraelectric layer or an unimprinted third ferroelectric layer. FIG. 21 is a schematic circuit diagram of a memory apparatus 800 according to some example embodiments.

[0115] Referring to FIG. 21, the memory apparatus 800 may include an array of a plurality of memory devices 820 arranged in a 2D manner. Each memory device 820 may be a memory cell in the memory apparatus 800. The memory device 820 (FEFET) may be one of the memory devices according to the aforementioned embodiments. In addition, the memory apparatus 800 may include a plurality of bit lines (BLO and BL1), a plurality of select lines (SLO and SL1), and a plurality of word lines (WLO

and WL1). The select lines (SLO and SL1) may be electrically connected to a first source/drain region of the memory device 820, the bit lines (BLO and BL1) may be electrically connected to a second source/drain region of the memory device 820, and the word lines (WLO and WL1) may be electrically connected to the gate electrode of the memory device 820. The memory apparatus 800 may further include an amplifier 810 for amplifying a signal output from the bit lines (BLO and BL1).

[0116] Although FIG. 21 shows a 2D plan view for convenience sake, the memory apparatus 800 may have a lamination structure of 2 or more levels. For example, the plurality of bit lines (BLO and BL1) extending in the vertical direction and the plurality of select lines (SLO and SL1) may be arranged in a 2D manner, and the plurality of word lines (WLO and WL1) extending in the horizontal direction may respectively be arranged at a plurality of layers. However, example embodiments are not limited thereto, and the memory cells may be arranged in a 3D manner in various ways.

[0117] The aforementioned memory devices (FEFET) may be applied to an artificial intelligence device 900 illustrated in FIG. 22. Each memory cell constituting the artificial intelligence device 900 may include one FET and one FEFET. The FEFET may be one of the memory devices according to the aforementioned embodiments. When a synaptic weight is applied to a transistor, a potential may be delivered to a ferroelectric material, which may change a state of memory. At this time, when a potential greater than a threshold voltage is applied to the ferroelectric material, a neuron-synapse operation in which a potential of a pre-synaptic neuron is delivered to a post-synaptic neuron may occur.

[0118] FIG. 23 is a schematic block diagram of a display apparatus 1520 including a display driver integrated circuit (DDI) 1500 according to some example embodiments.

[0119] Referring to FIG. 23, the DDI 1500 may include a controller 1520, a power supply circuit 1504, a driver block 1506, and a memory block 1508. The controller 1520 may receive and decode a command applied from a main processing unit (MPU) 1522, and control each block of the DDI 1500 to implement an operation according to the command. The power supply circuit 1504 may generate a driving voltage in response to the control by the controller 1520. The driver block 1506 may drive a display panel 1524 by using the driving voltage generated by the power supply circuit 1504 in response to the control by the controller 1520. The display panel 1524 may be or may include, for example, one or more of a liquid crystal display panel, an organic light-emitting device (OLED) display panel, or a plasma display panel. The memory block 1508 may temporarily store a command input to the controller 1520, control signals output from the controller 1520, or necessary data, and may include a memory such as one or more of RAM, ROM, etc. For example, the memory block 1508 may include the memory devices according to the aforementioned embodiments.

[0120] FIG. 24 is a block diagram of an electronic apparatus 1600 according to some example embodiments.

[0121] Referring to FIG. 24, the electronic apparatus 1600 may include a memory 1610 and a memory controller 1620. The memory controller 1620 may control the memory 1610 to read data from the memory 1610 and/or write data to the memory 1610 in response to a request from a host 1630. The memory 1610 may include the memory devices according to the aforementioned embodiments.

[0122] FIG. 25 is a block diagram of an electronic apparatus 1700 according to some example embodiments.

[0123] Referring to FIG. 25, the electronic apparatus 1700 may constitute a wireless communication apparatus or an apparatus capable of transmitting and/or receiving information in a wireless environment. The electronic apparatus 1700 may include a controller 1710, an input/output (I/O) device 1720, a memory 1730, and a wireless interface 1740, which are connected to each other through a bus 1750.

[0124] The controller 1710 may include at least one of a microprocessor, a digital signal processor, and other similar processing apparatuses. The I/O device 1720 may include at least one of a keypad, a keyboard, and a display. The memory 1730 may be used to store a command executed by the controller 1710. For example, the memory 1730 may be used to store user data. The electronic apparatus 1700 may use the wireless interface 1740 to transmit/receive data through a wireless communication network. The wireless interface 1740 may include an antenna and/or a wireless transceiver. In some embodiments, the electronic apparatus 1700 may be used in a communication interface protocol of a third generation communication system, for example, one or more of code division multiple access (CDMA), global system for mobile communications (GSM), North American digital cellular (NADC), and extended-time division multiple access (E-TDMA), and/or a third generation communication system such as wide band code division multiple access (WCDMA). The memory 1730 of the electronic apparatus 1700 may include the memory devices according to the aforementioned embodiments.

[0125] FIGS. 26 and 27 are conceptual diagrams schematically illustrating a device architecture applicable to an electronic apparatus according to some example embodiments.

[0126] Referring to FIG. 26, an electronic device architecture 1000 may include a memory unit 1010 and a control unit 1030, and may further include an arithmetic logic unit (ALU) 1020. The memory unit 1010, the ALU 1020, and the control unit 1030 may be electrically connected. For example, the electronic device architecture 1000 may be implemented as a single chip including the memory unit 1010, the ALU 1020, and the control unit 1030. Specifically, the memory unit 1010, the ALU 1020, and the control unit 1030 may be interconnected by a metal line on an on-chip and communicate directly with each other. The memory unit 1010, the ALU 1020, and the control

unit 1030 may be integrated on one substrate in a monolithic manner and constitute a single chip. Input/output devices 2000 may be connected to the electronic device architecture (chip) 1000. The memory unit 1010 may include both of a main memory and a cache memory. Such electronic device architecture (chip) 1000 may be an on-chip memory processing unit. The memory unit 1010, the ALU 1020, and/or the control unit 1030 may each independently include the semiconductor device according to the embodiments described above.

[0127] Referring to FIG. 27, a cache memory 2510, an ALU 2520, and a control unit 2530 may constitute a central processing unit (CPU) 2500, and the cache memory 2510 may include static random access memory (SRAM). Separate from the CPU 1500, a main memory 2600 and an auxiliary storage 2700 may be provided, and an I/O device 240 may also be provided. The main memory 2600 may include, for example, the semiconductor device according to the embodiments described above.

[0128] In some cases, the electronic device architecture may be implemented in a form in which computing unit elements and memory unit elements are adjacent to each other on a single chip without separating sub-units.

[0129] According to various example embodiments, the memory device may implement multi-bit having multi-level characteristics of three or more levels by including a lamination structure in which a plurality of ferroelectric layers (or anti-ferroelectric layers) imprinted in opposite directions from each other are laminated in a direction perpendicular to a semiconductor substrate.

[0130] Any of the elements and/or functional blocks disclosed above may include or be implemented in processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the processing circuitry more specifically may include, but is not limited to, a central processing unit (CPU), an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), a System-on-Chip (SoC), a programmable logic unit, a microprocessor, application-specific integrated circuit (ASIC), etc. The processing circuitry may include electrical components such as at least one of transistors, resistors, capacitors, etc. The processing circuitry may include electrical components such as logic gates including at least one of AND gates, OR gates, NAND gates, NOT gates, etc.

[0131] It should be understood that embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each example embodiment should typically be considered as available for other similar features or aspects in other embodiments. While one or more embodiments have been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from

the scope as defined by the following claims.

Claims

1. A memory device comprising:

a semiconductor substrate;
a gate electrode on the semiconductor substrate; and
a plurality of ferroelectric layers including at least one first ferroelectric layer and at least one second ferroelectric layer, the plurality of ferroelectric layers laminated between the semiconductor substrate and the gate electrode in a first direction perpendicular to a surface of the semiconductor substrate, wherein:

the first ferroelectric layer has a doping concentration gradient in which a doping concentration increases in the first direction, and the second ferroelectric layer has a doping concentration gradient in which a doping concentration decreases in the first direction; and
the memory device is configured to implement multi-bit functionality according to an operating voltage.

2. The memory device of claim 1, wherein the first ferroelectric layer and the second ferroelectric layer are imprinted in a positive (+) voltage direction and a negative (-) voltage direction, respectively.

3. The memory device of claim 1 or 2, wherein the plurality of ferroelectric layers include n ferroelectric layers associated with multi-bit functionality having a multi-level of at least (n+1) levels.

4. The memory device of any preceding claim, further comprising: a paraelectric layer between the plurality of ferroelectric layers.

5. The memory device of claim 4, wherein the paraelectric layer includes at least one of SiO₂, Al₂O₃, La₂O₃, and Y₂O₃.

6. The memory device of any preceding claim, further comprising:

a first interface layer and a second interface layer respectively on upper and lower surfaces of the first ferroelectric layer and including different paraelectric materials from each other; and
a third interface layer and a fourth interface layer respectively on upper and lower surfaces of the second ferroelectric layer and including different paraelectric materials from each other.

7. The memory device of claim 6, wherein the first interface layer and the fourth interface layer include a same material, and the second interface layer and the third interface layer include a same material.

8. The memory device of any preceding claim, wherein the first ferroelectric layer and the second ferroelectric layer each include a hafnium oxide incorporating a dopant.

9. The memory device of claim 8, wherein the dopant includes at least one of Zr, La, Al, Si, and Y.

10. The memory device of any preceding claim, wherein the first ferroelectric layer and the second ferroelectric layer each include an aluminum nitride incorporating a dopant.

11. The memory device of claim 10, wherein the dopant includes at least one of B and Sc.

12. The memory device of any preceding claim, wherein the plurality of ferroelectric layers further include an unimprinted third ferroelectric layer between the first ferroelectric layer and the second ferroelectric layer.

13. An operating method of a memory device according to any preceding claim, the operating method comprising obtaining multiple-levels in different polarization states from each other by adjusting an operating voltage based on a hysteresis curve associated with the plurality of ferroelectric layers.

14. The operating method of claim 13, wherein the adjusting of the operating voltage is performed by varying a maximum applied voltage.

15. The operating method of claim 13 or 14, wherein the plurality of ferroelectric layers include n ferroelectric layers associated with multi-bit functionality having a multi-level of at least (n+1) levels.

FIG. 1

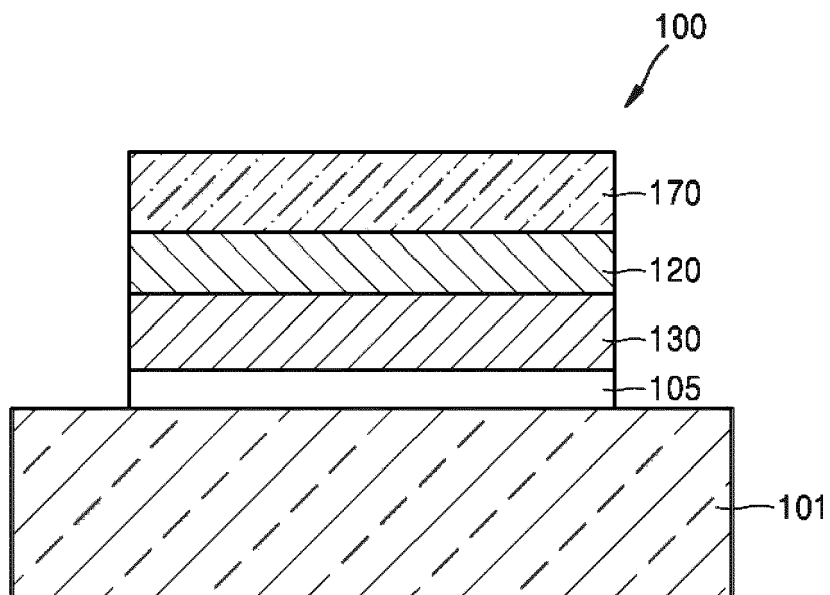


FIG. 2A

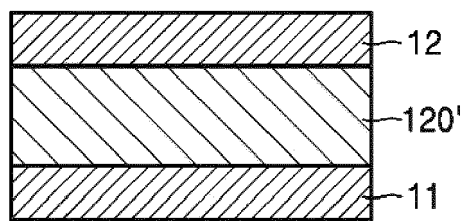


FIG. 2B

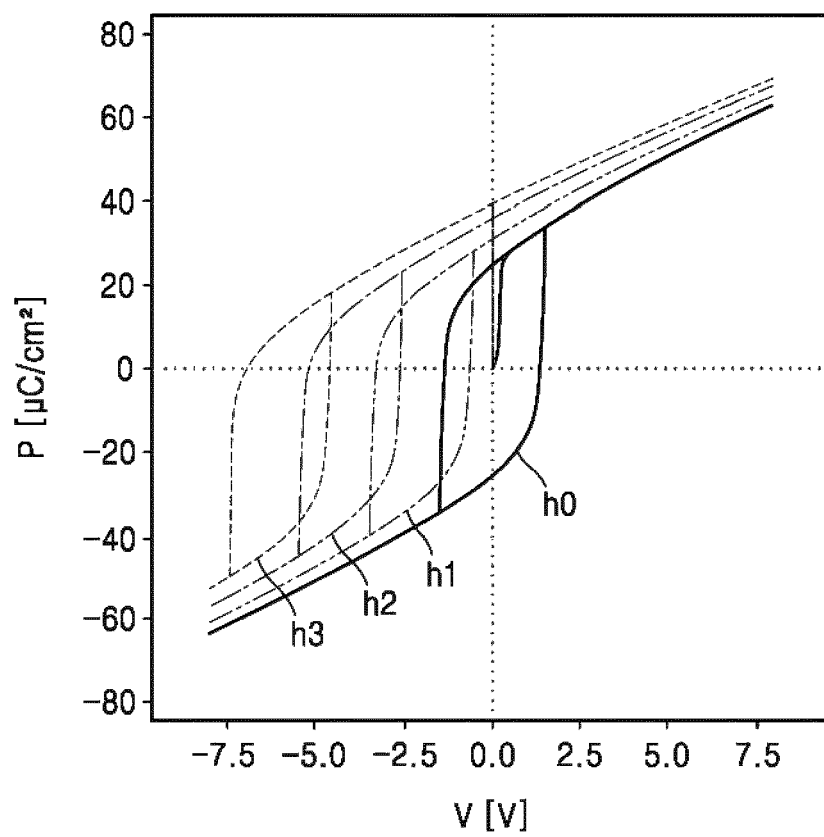


FIG. 3A

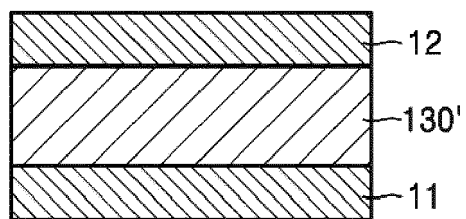


FIG. 3B

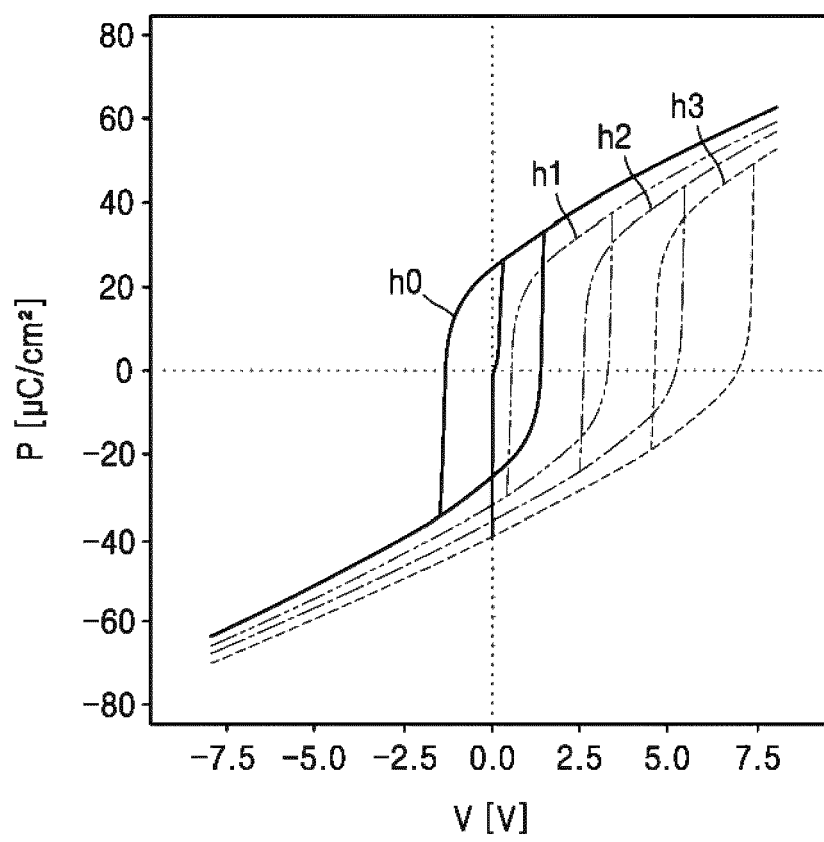


FIG. 4A

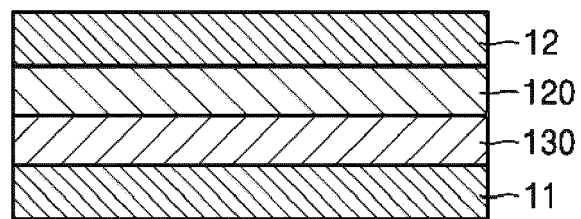


FIG. 4B

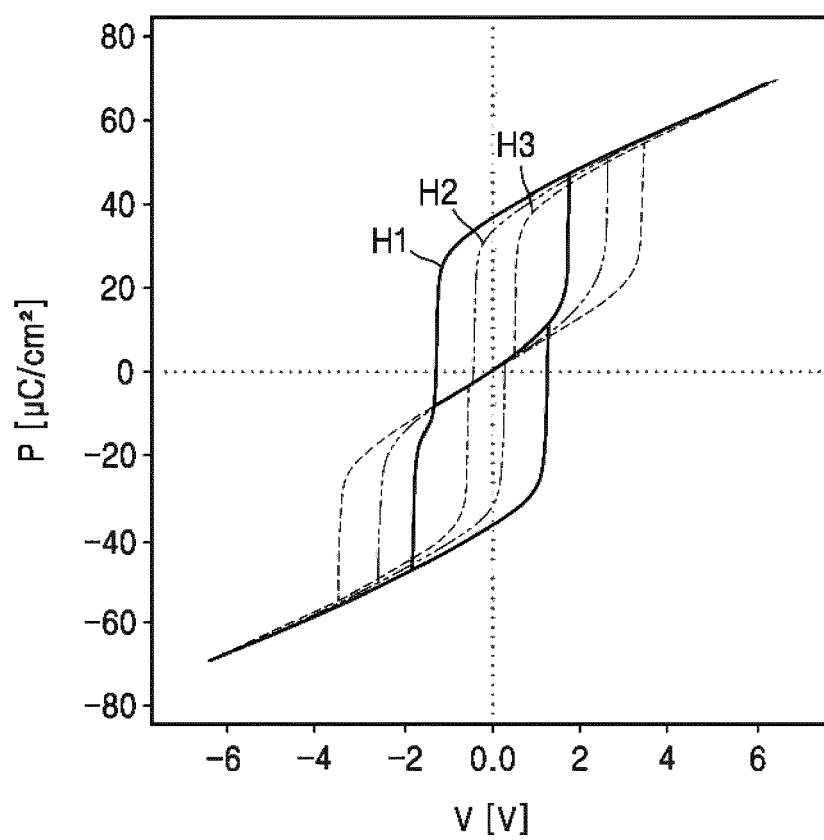


FIG.5A

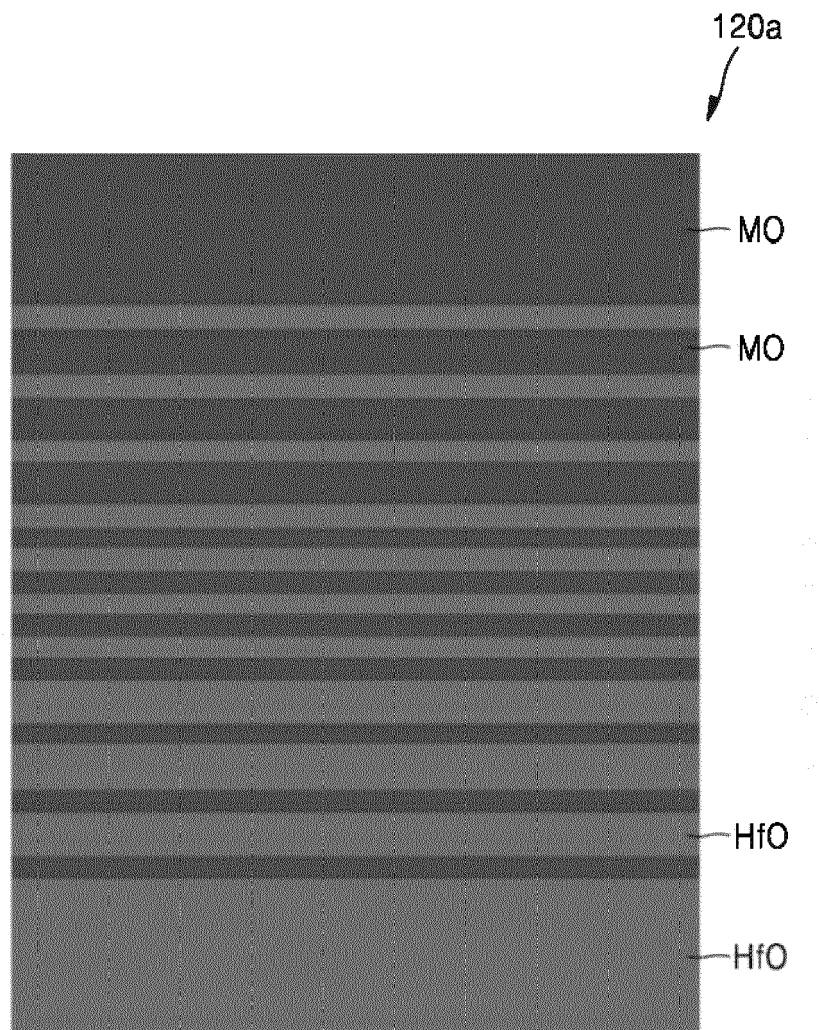


FIG. 5B

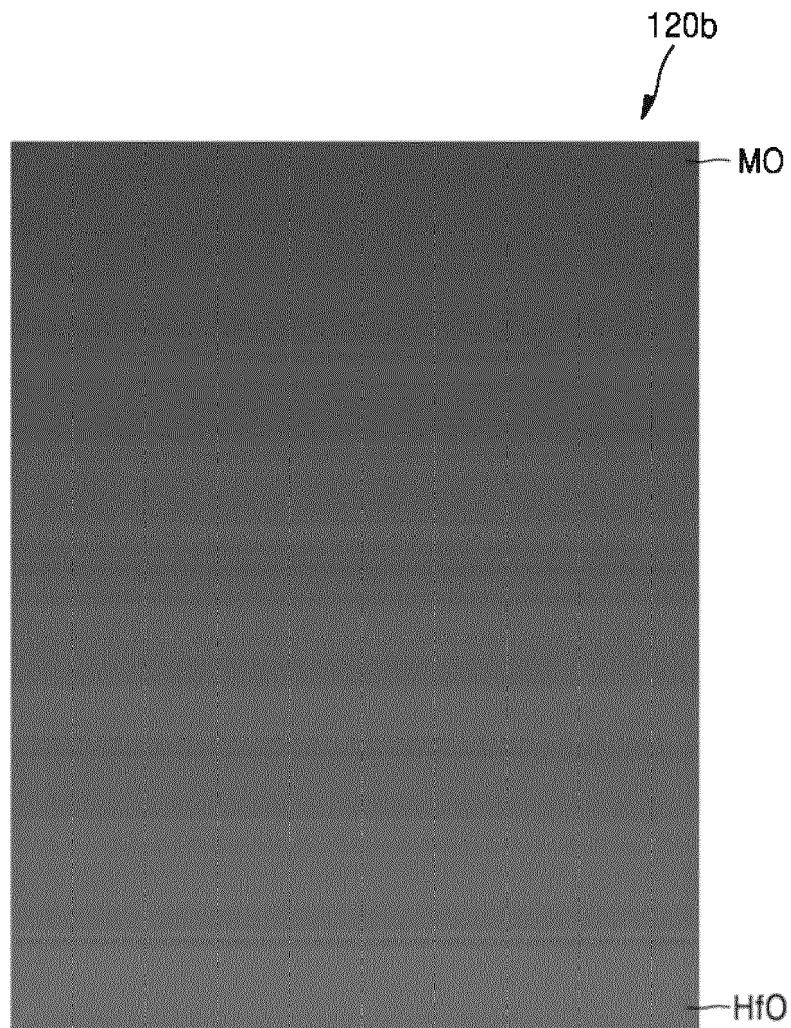


FIG. 6A

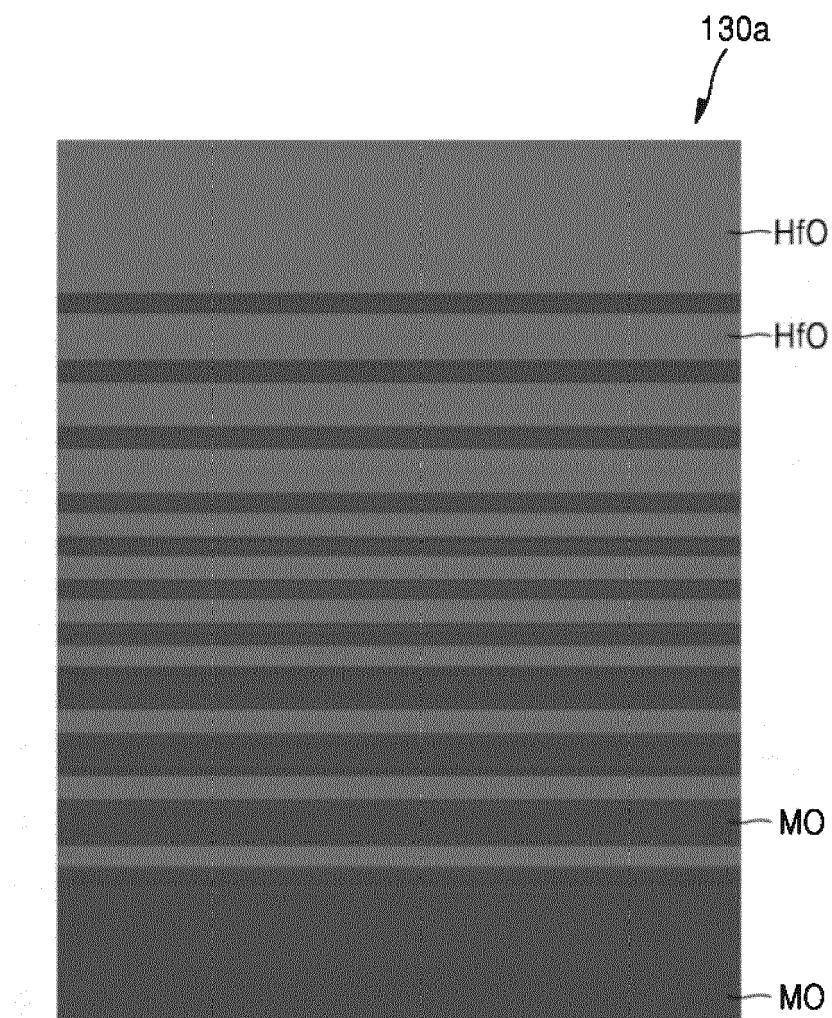


FIG. 6B

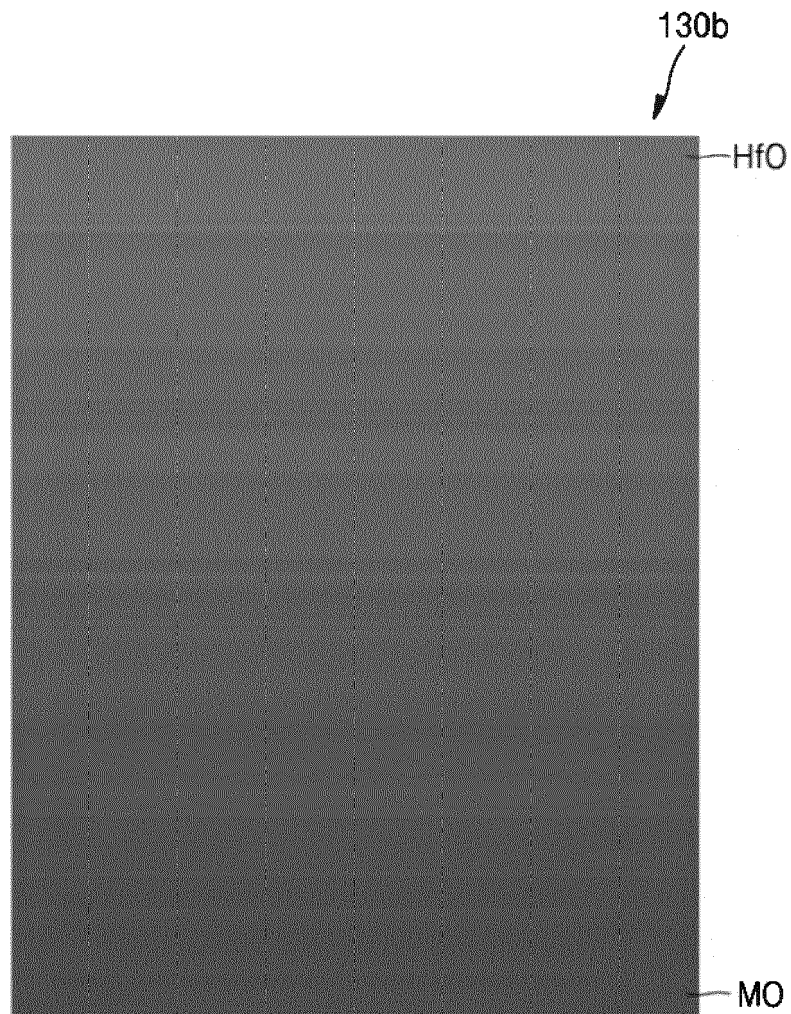


FIG. 7

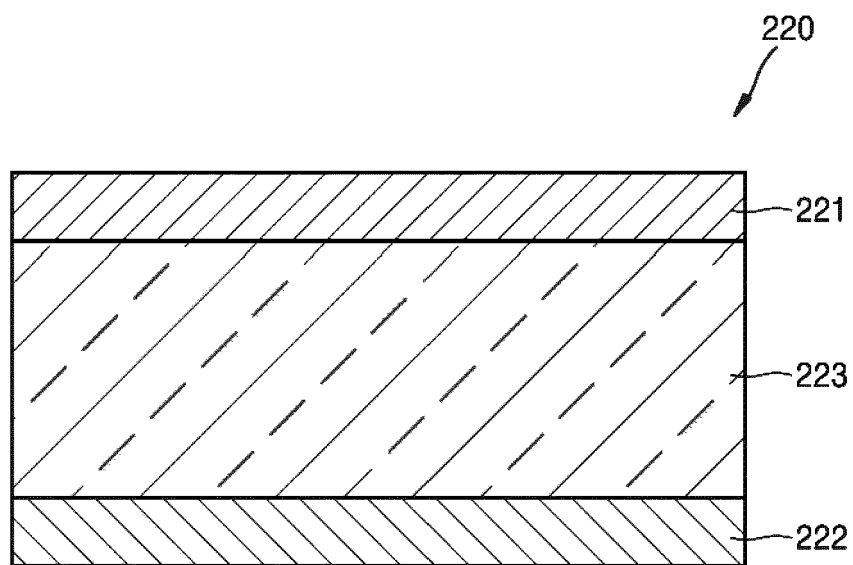


FIG. 8

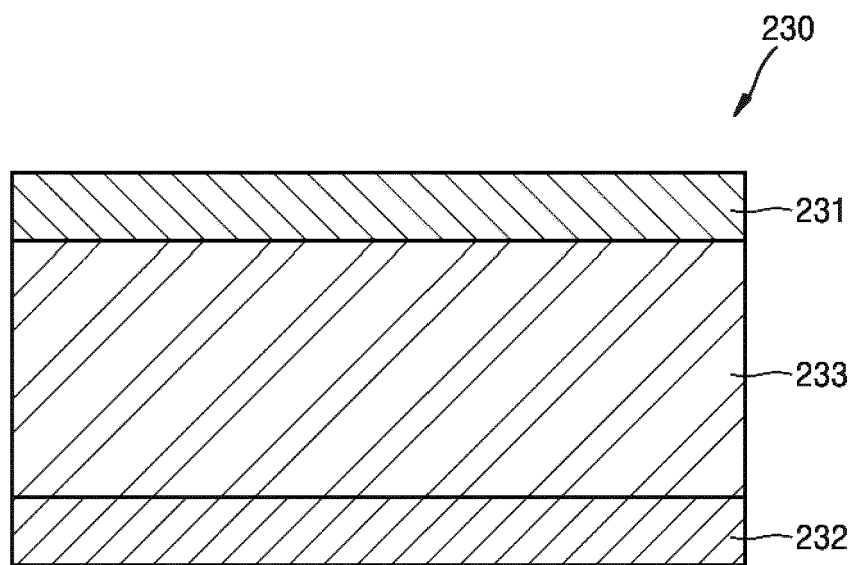


FIG. 9

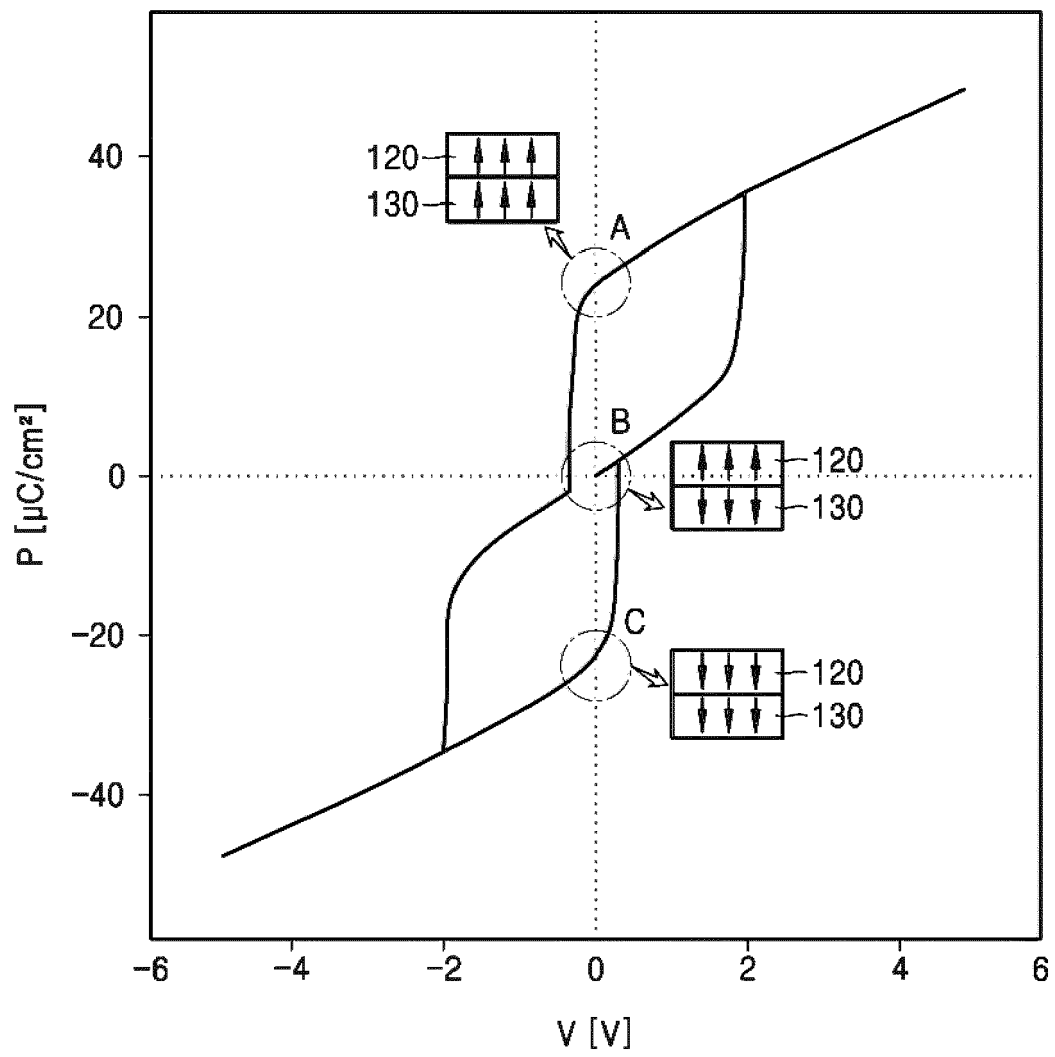


FIG. 10

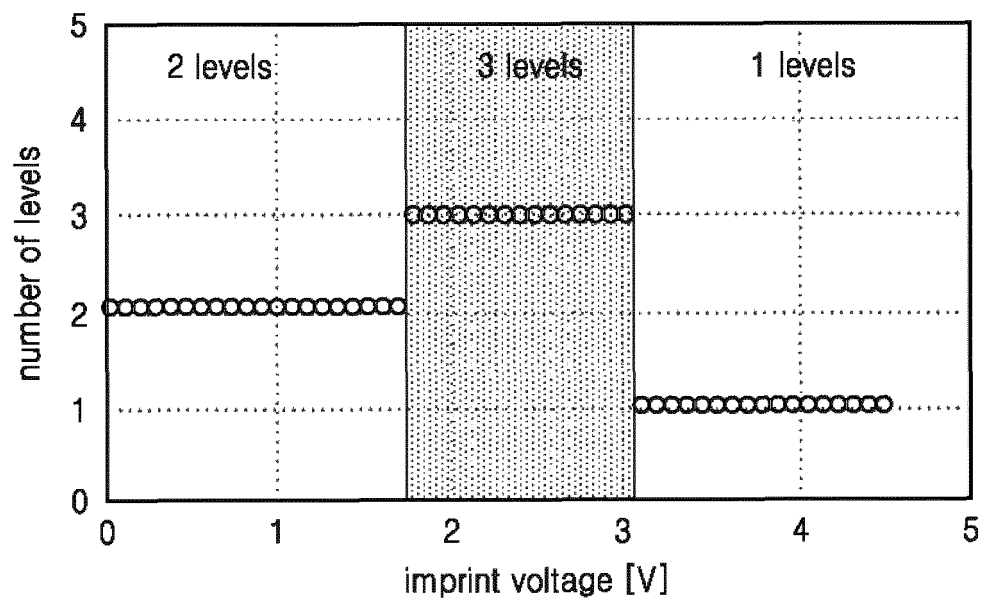


FIG. 11

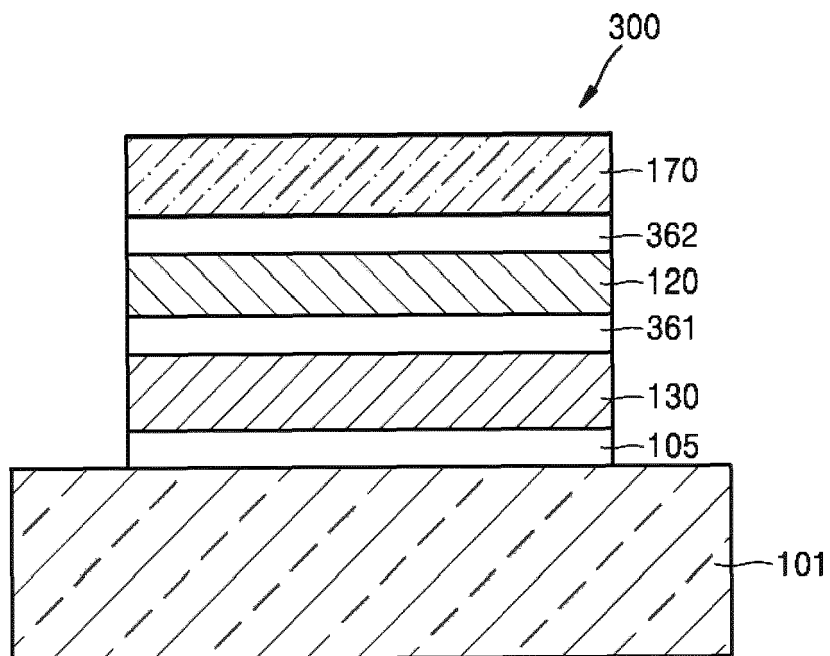


FIG. 12

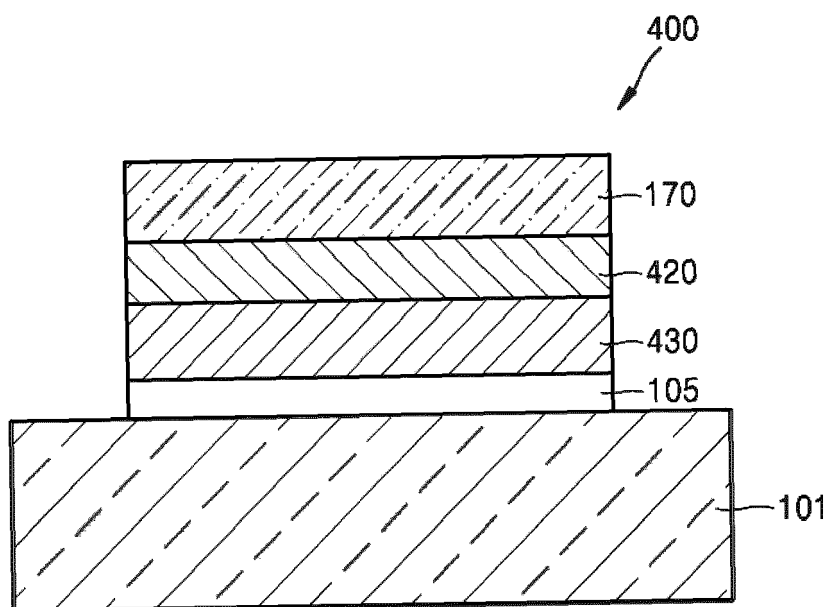


FIG. 13

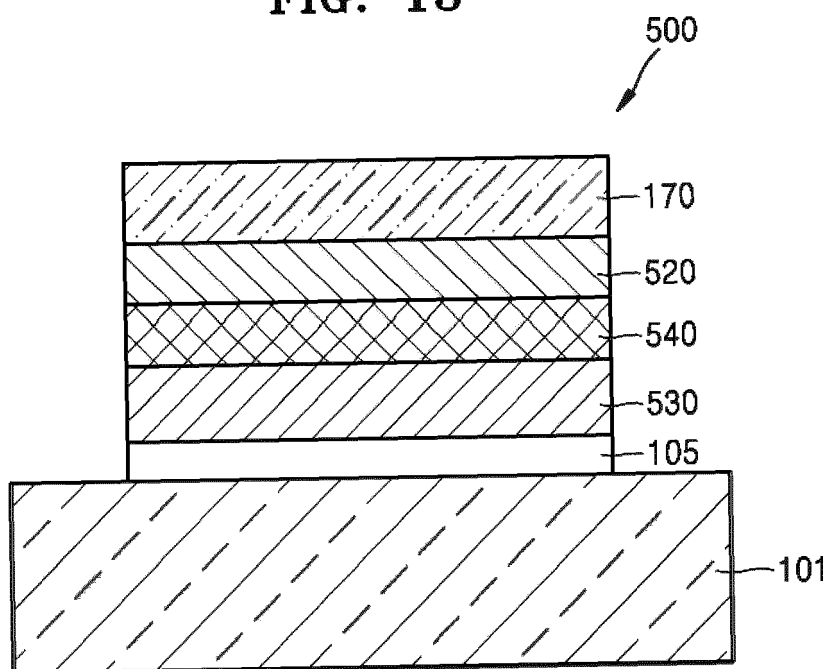


FIG. 14A

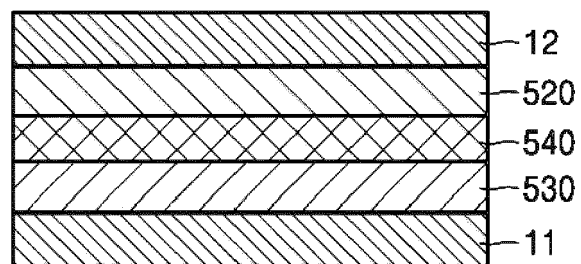


FIG. 14B

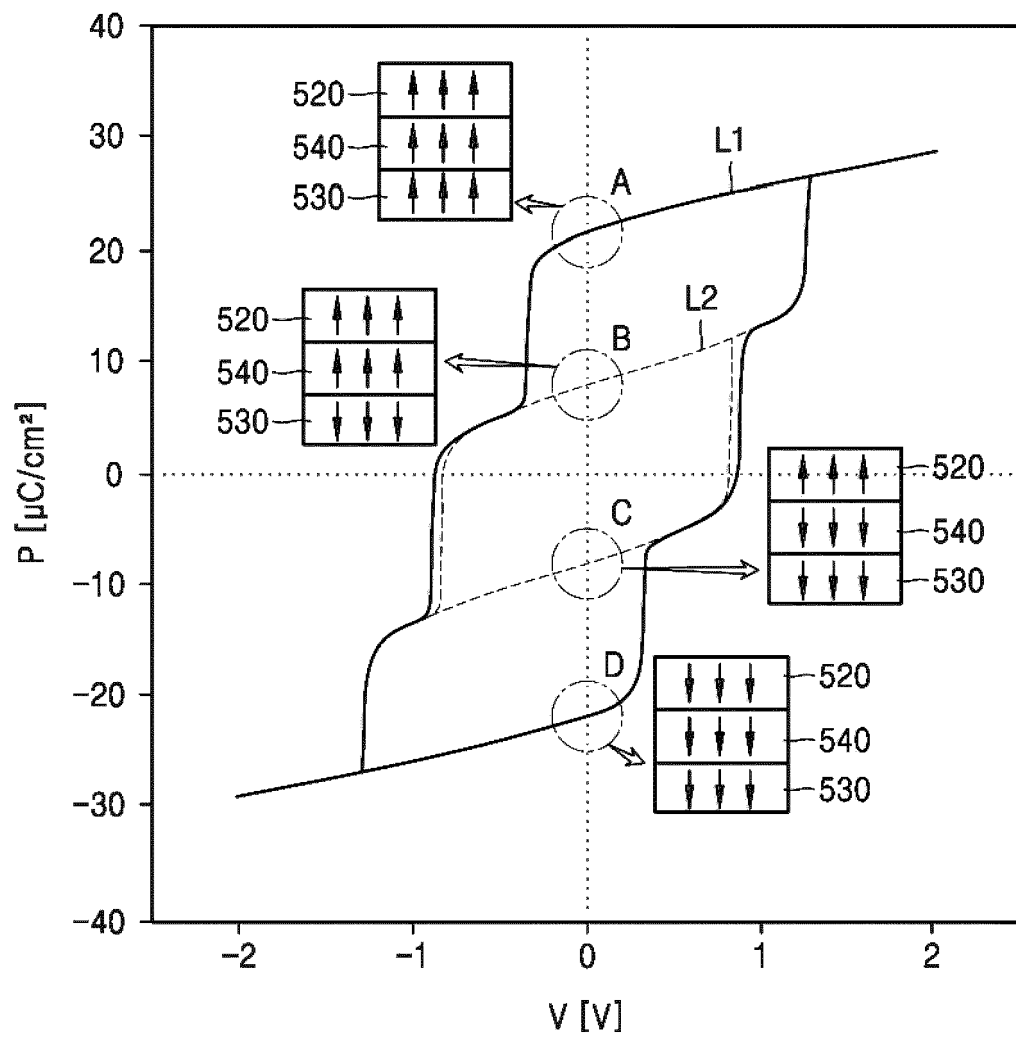


FIG. 15

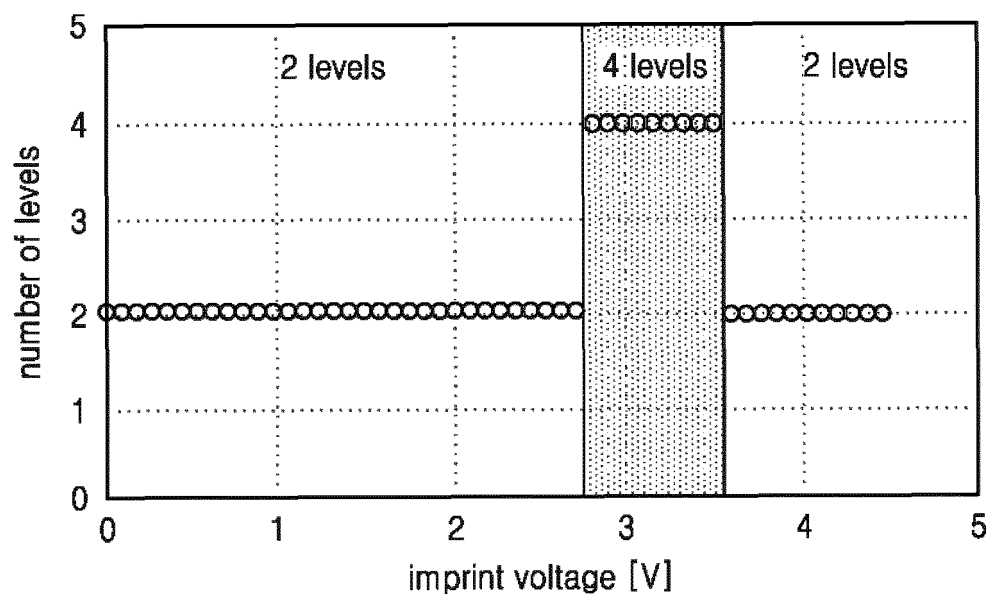


FIG. 16

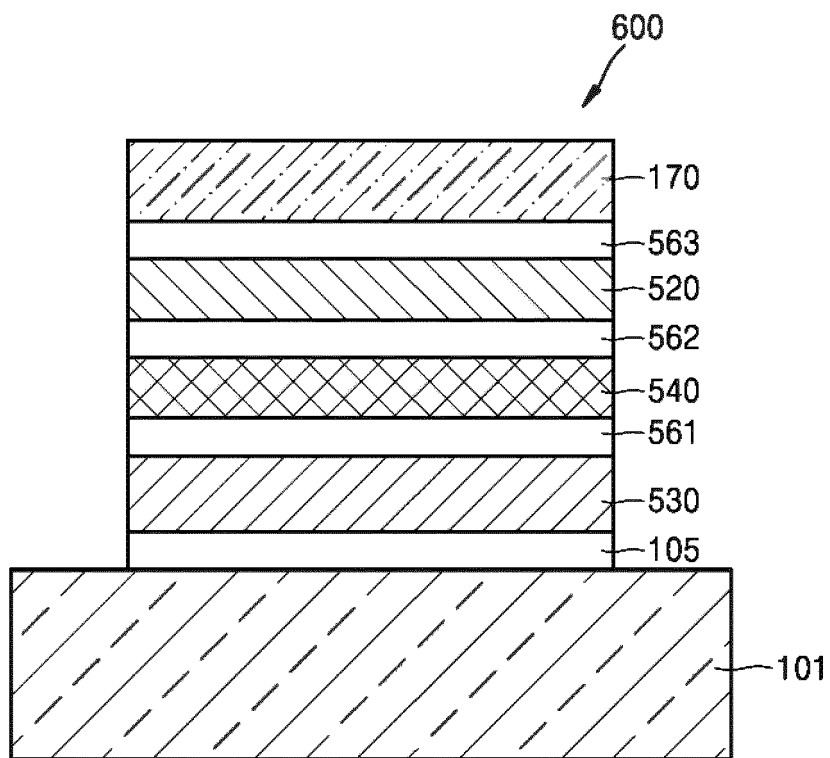


FIG. 17

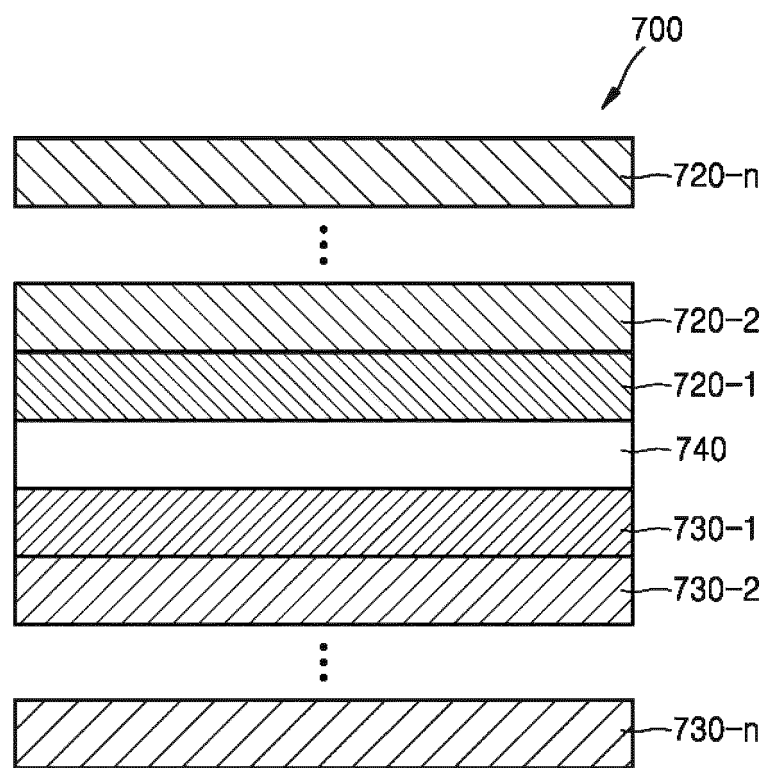


FIG. 18

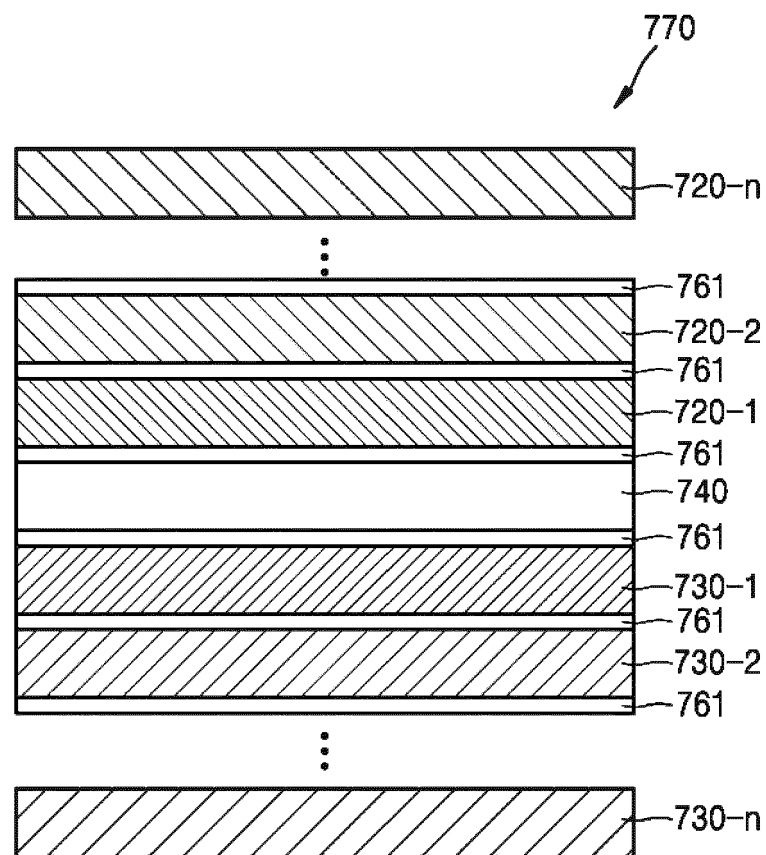


FIG. 19

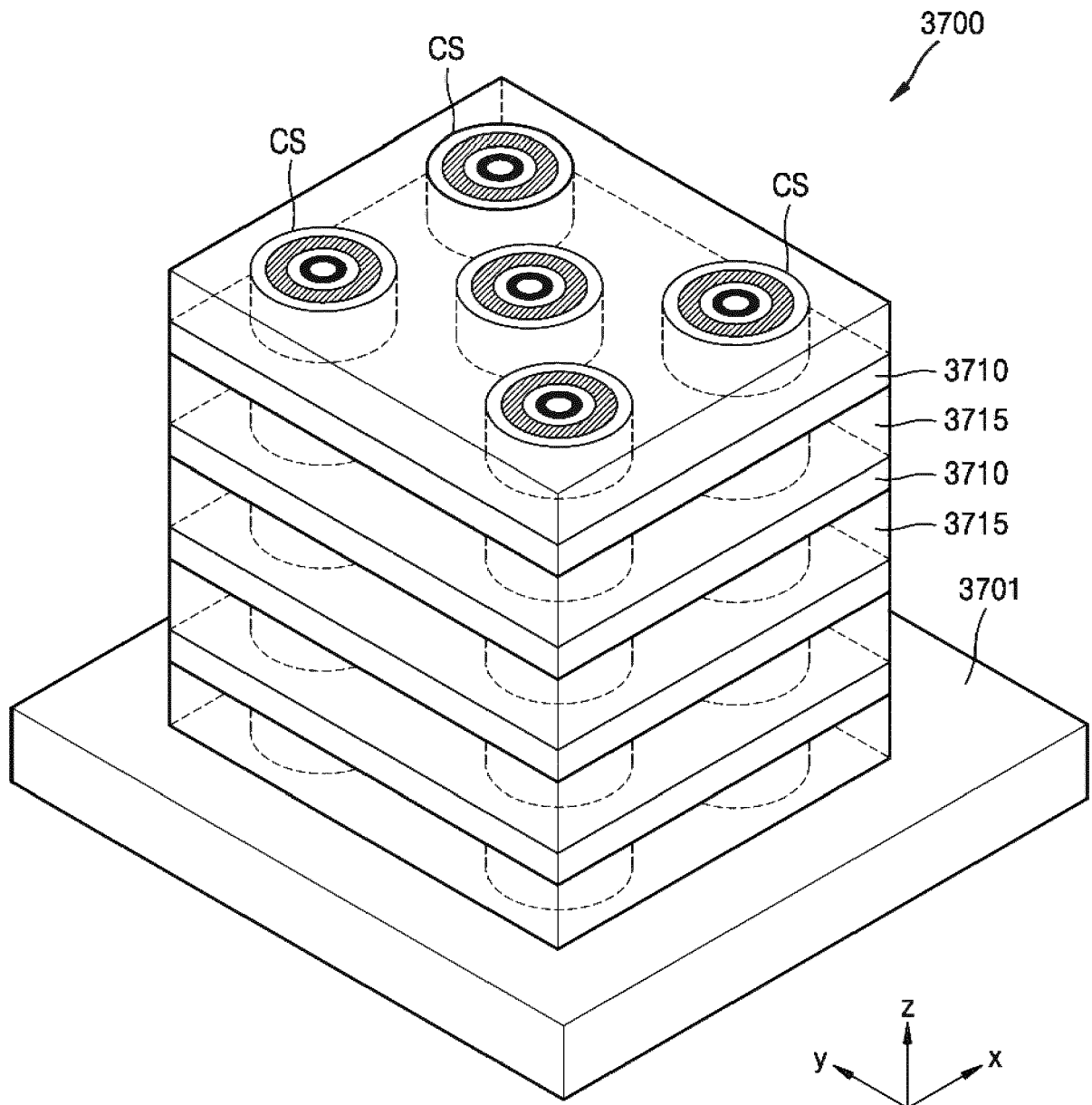


FIG. 20

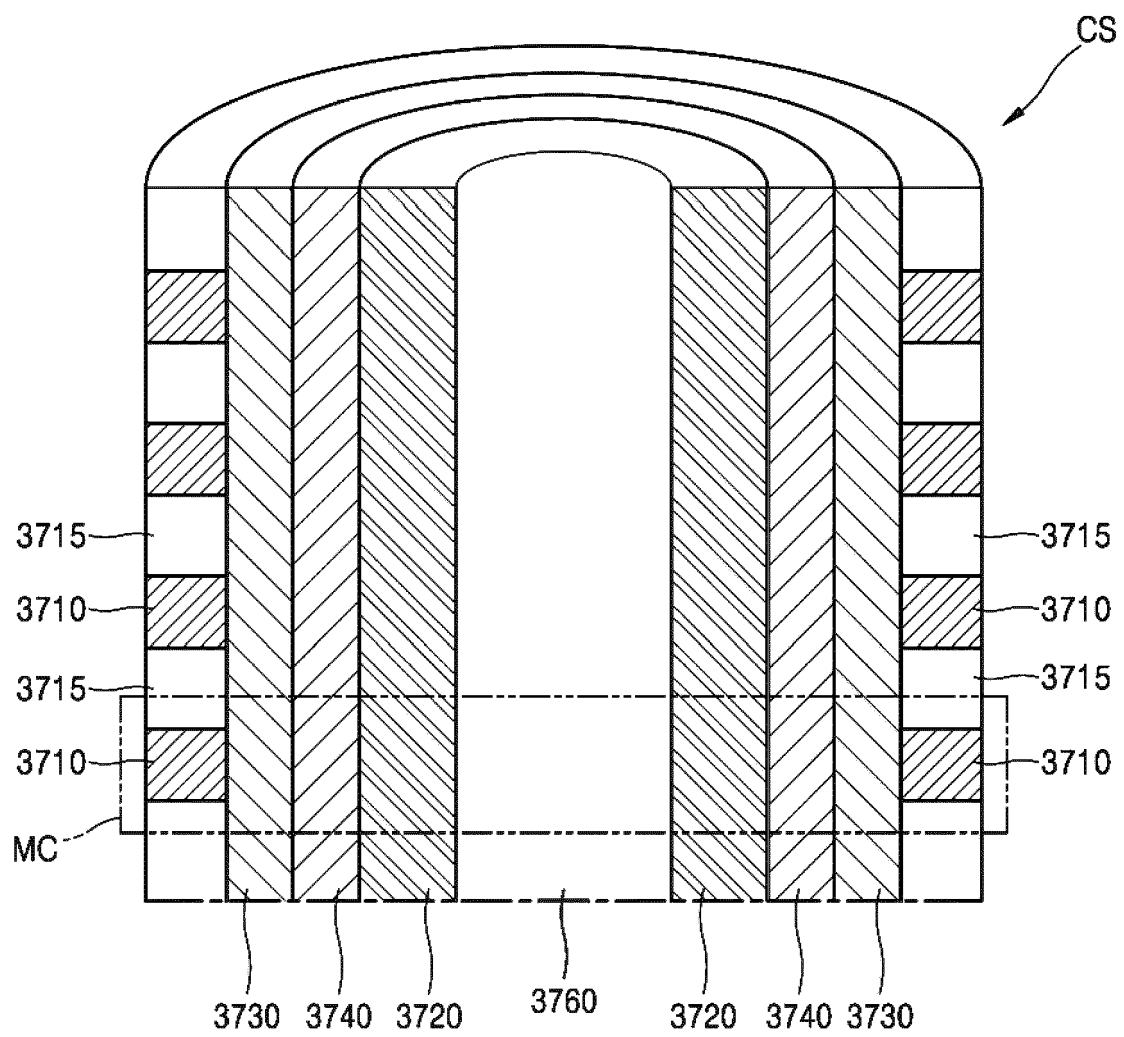


FIG. 21

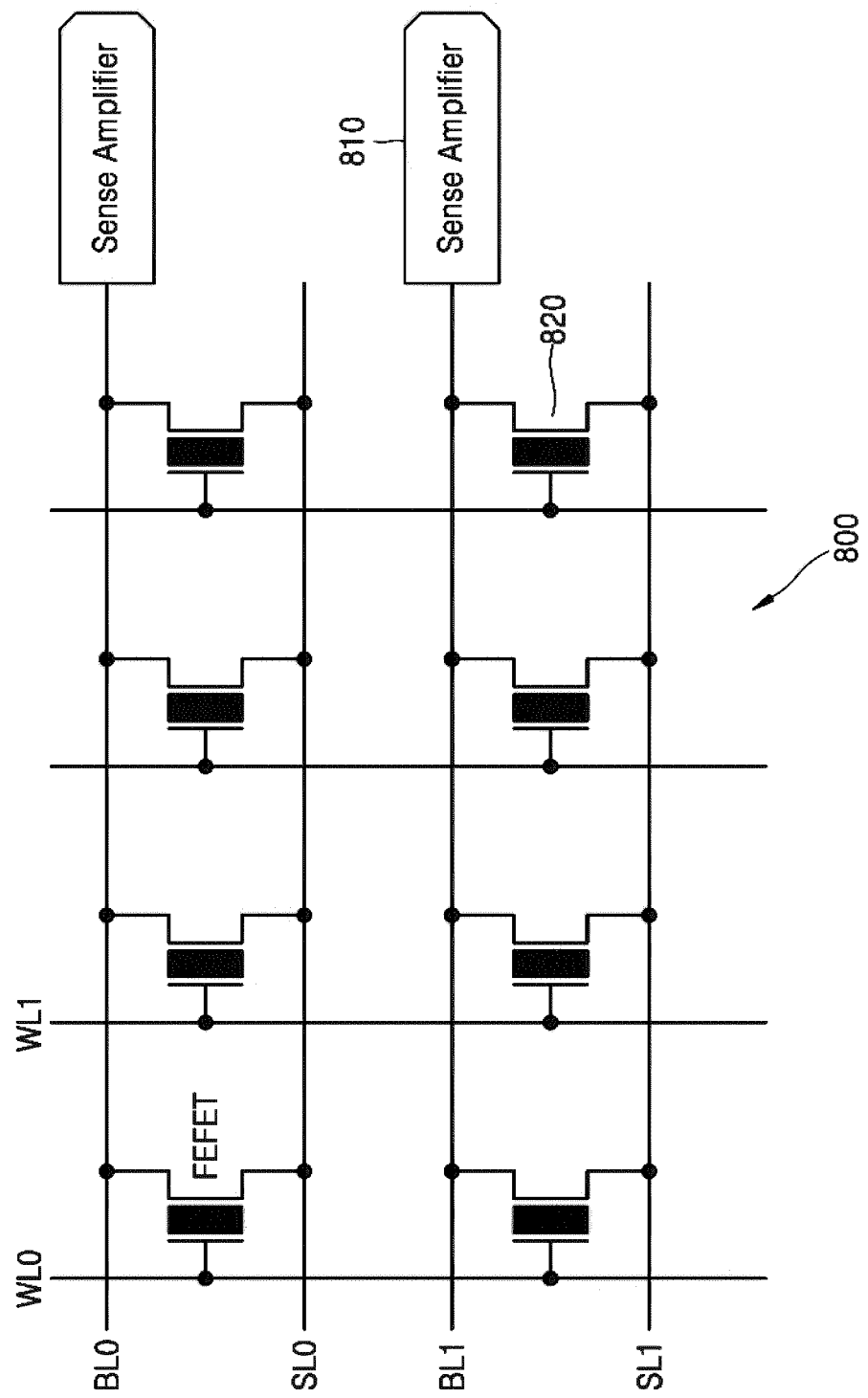


FIG. 22

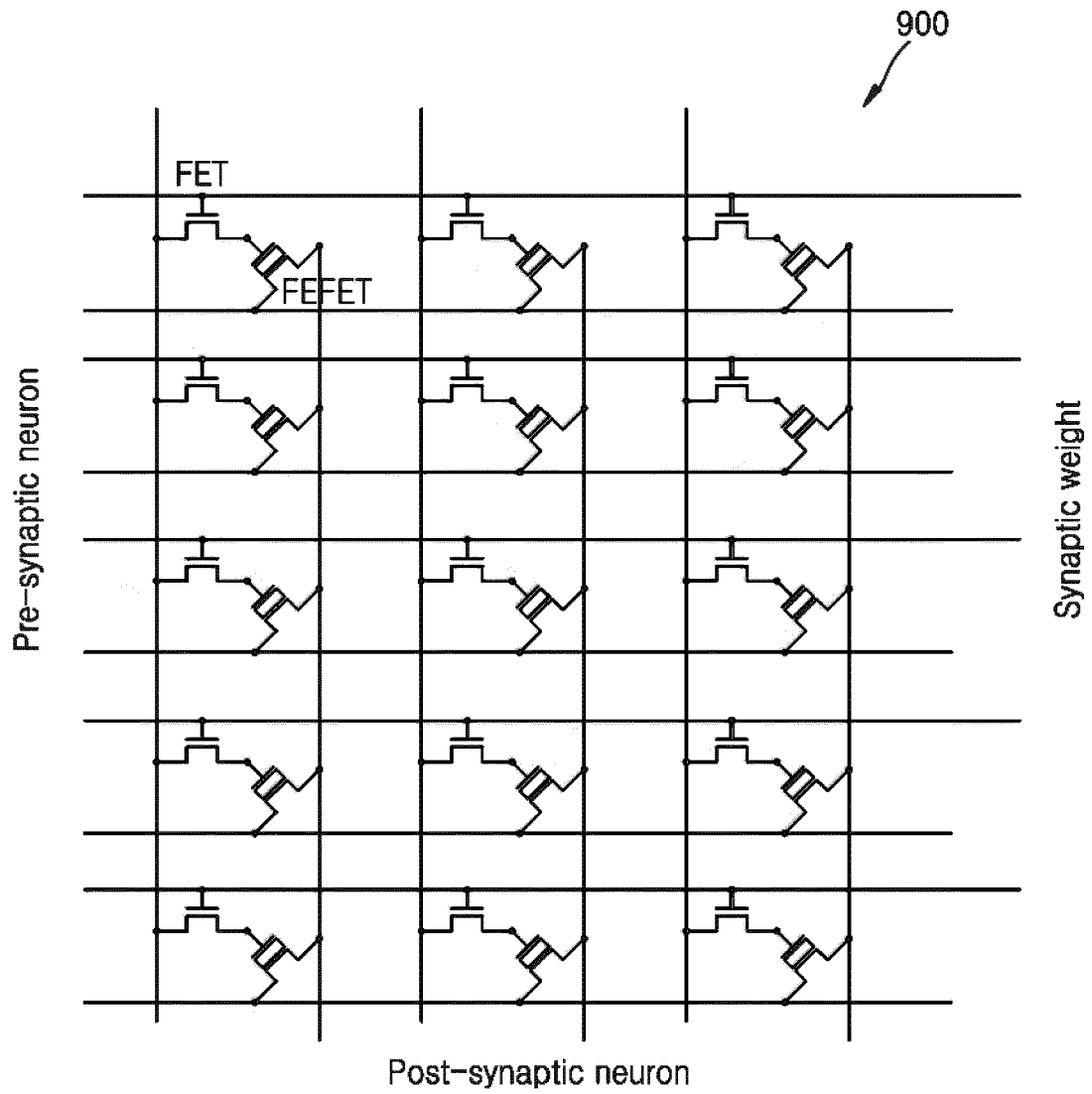


FIG. 23

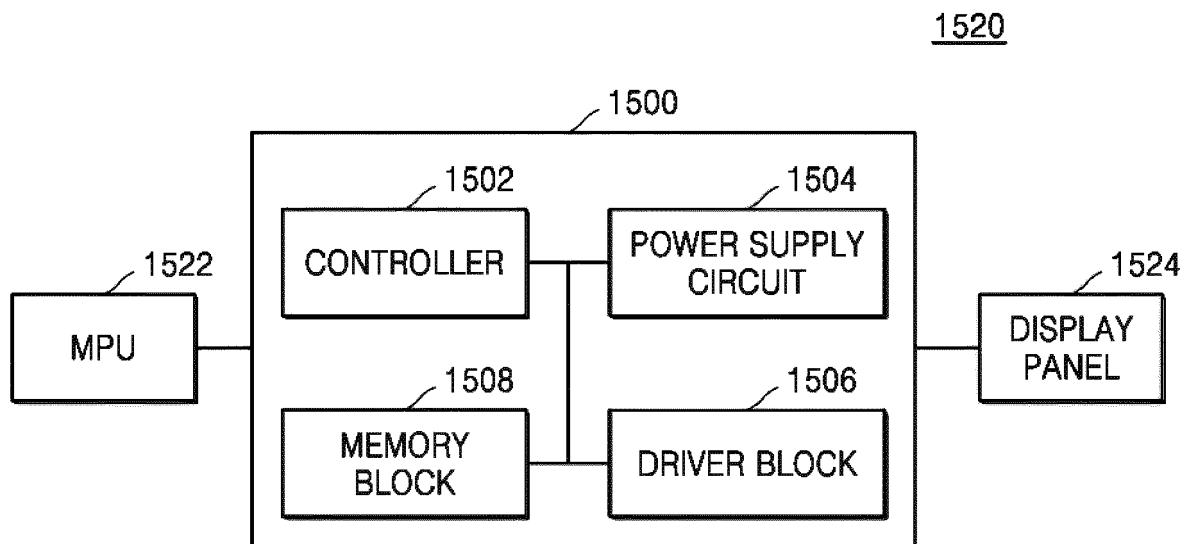


FIG. 24

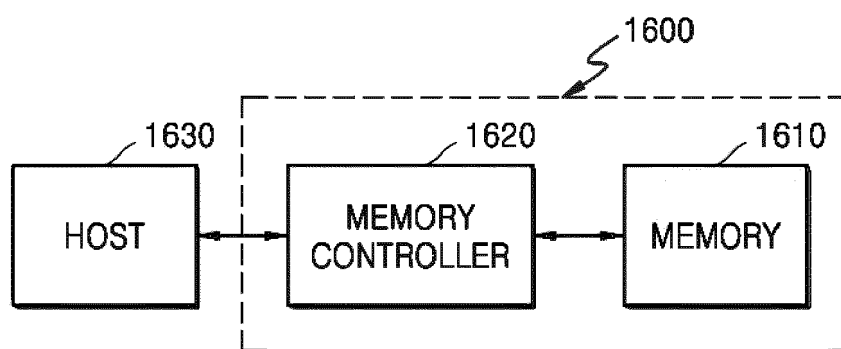


FIG. 25

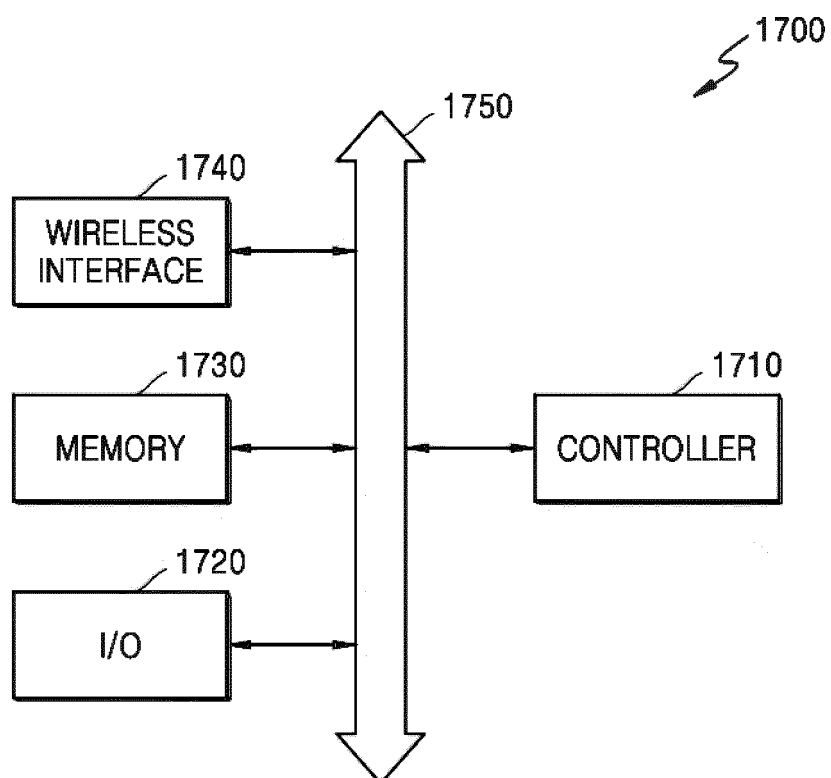


FIG. 26

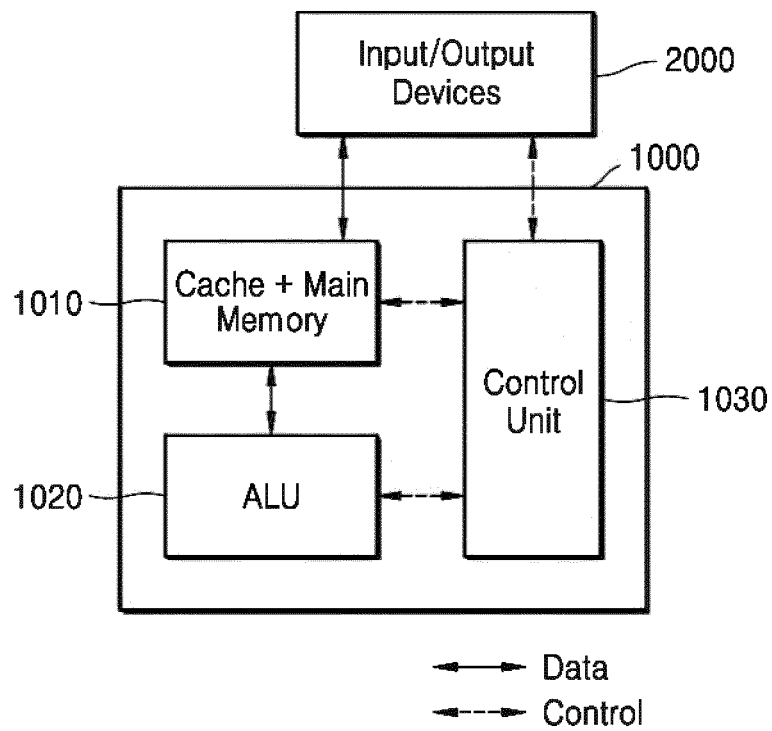
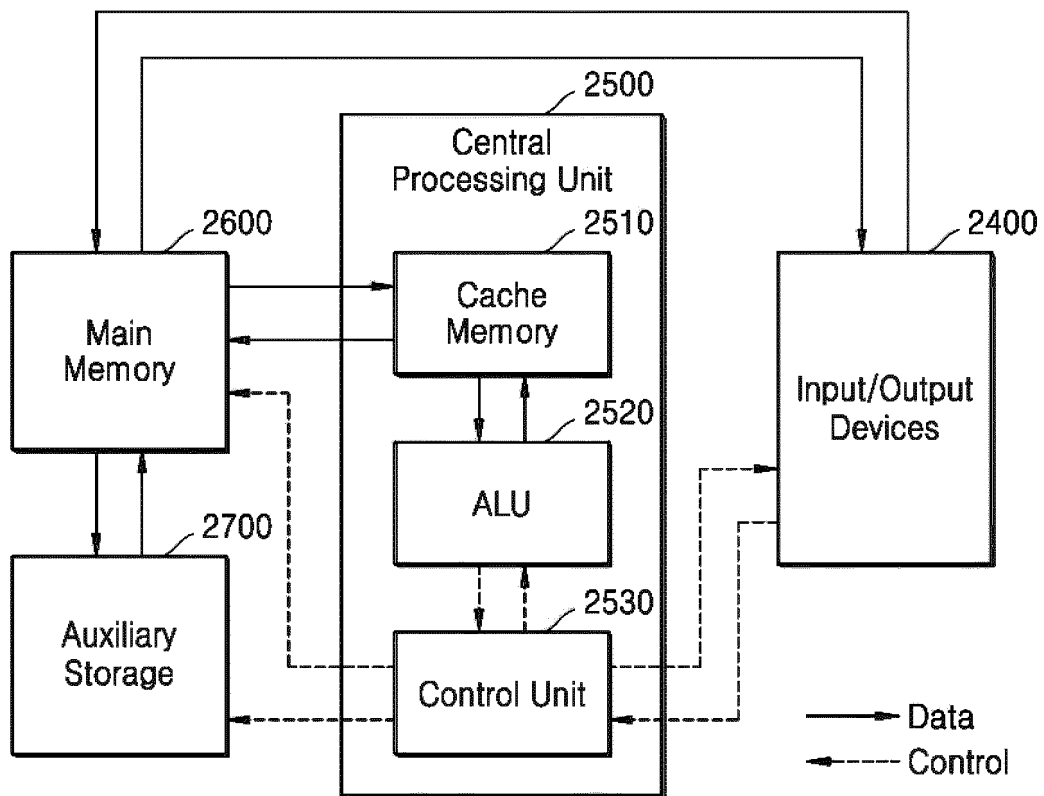


FIG. 27





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A	* paragraph [0017]; figures 1, 7, 8 * * paragraph [0046] - paragraph [0054]; figures 10-12 *	4-7, 12-15	H01L29/51 H01L29/66 H01L29/78 H10B51/20 H10B51/30
A	US 2014/070289 A1 (TANAKA MASAYUKI [JP] ET AL) 13 March 2014 (2014-03-13) * paragraph [0063] - paragraph [0065]; figures 1A, 1B, 7A-7D *	1-15	
A	US 2021/328063 A1 (LEE JUN HEE [KR] ET AL) 21 October 2021 (2021-10-21) * paragraph [0092] - paragraph [0098]; figures 11, 12 *	1-15	
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			TECHNICAL FIELDS SEARCHED (IPC)
			H01L H10B
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 5 June 2024	Examiner Nesso, Stefano
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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