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(54) LIGHT-EMITTING ELEMENT FOR DISPLAY

(57) A light-emitting element for a display according to one embodiment comprises: a first LED lamination; a second LED lamination; a third LED lamination; a first transparent electrode interposed between the first LED lamination and the second LED lamination and being in ohmic contact with the lower surface of the first LED lamination; a second transparent electrode interposed between the first LED lamination and the second LED lamination and being in ohmic contact with the upper surface of the second LED lamination; a third transparent electrode interposed between the second LED lamination and the third LED lamination and being in ohmic contact with the upper surface of the third LED lamination; an n electrode pad disposed on a first conductive semiconductor layer of the third LED lamination; a lower p electrode pad disposed on the third transparent electrode; and bump pads arranged on the first LED lamination, wherein the upper surface of the n electrode pad is located at the same height as that of the upper surface of the lower p electrode pad.

EP 4 407 697 A2

Description

[Technical field]

[0001] Exemplary embodiments relate to a light emitting device for a display and a display apparatus, and, more particularly, to a light emitting device having a stack structure of a plurality of LEDs for a display, and a display apparatus including the same.

[Related art]

[0002] As an inorganic light source, light emitting diodes have been used in various technical fields, such as displays, vehicular lamps, general lighting, and the like. With various advantages of the light emitting diodes, such as longer lifespan, lower power consumption, and faster response, than existing light sources, light emitting diodes have been replacing the existing light sources.

[0003] Light emitting diodes have been generally used as backlight light sources in display apparatuses. However, LED displays that directly realize images using the light emitting diodes have been recently developed.

[0004] In general, a display apparatus displays various colors through mixture of blue, green, and red light. In order to realize various images, the display apparatus includes a plurality of pixels, each including sub-pixels corresponding to one of blue, green, and red light. As such, a color of a certain pixel is typically determined based on the colors of the sub-pixels, so that images can be realized through the combination of such pixels.

[0005] Since LEDs can emit various colors depending upon materials thereof, individual LED chips emitting blue, green and red light may be arranged on a two-dimensional plane to provide a display apparatus. However, when one LED chip is provided to each sub-pixel, the number of LED chips may be increased, which may require excessive time for a mounting process during manufacture.

[0006] Moreover, since the sub-pixels are arranged on the two-dimensional plane in the display apparatus, a relatively large area is occupied by one pixel that includes the sub-pixels for blue, green, and red light. Thus, an area of each subpixel must be reduced in order to arrange the subpixels in a restricted area. However, reduction in the area of the LED chip may cause difficulties in mounting the LED chip and reduction in a luminous area.

[Disclosure]

[Technical Problem]

[0007] Exemplary embodiments provide a light emitting device for a display that is capable of increasing an area of each sub-pixel in a restricted pixel area and a display apparatus including the same.

[0008] Exemplary embodiments also provide a light emitting device for a display that is capable of reducing a time associated with a mounting process and a display apparatus including the same.

[0009] Exemplary embodiments further provide a light emitting device for a display that is capable of increasing the production yield and a display apparatus including the same.

[Technical Solution]

[0010] An exemplary embodiment of the present disclosure provides a light emitting device for a display including: a first LED stack; a second LED stack disposed under the first LED stack; a third LED stack disposed under the second LED stack; a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack; a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack; a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack; an n electrode pad disposed on a first conductivity type semiconductor layer of the third LED stack; a lower p electrode pad disposed on the third transparent electrode; and bump pads disposed on the first LED stack, wherein each of the first to third LED stacks includes a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer, the bump pads include first to third bump pads and common bump pads, wherein the common bump pad is commonly electrically connected to the first to third LED stacks, the first to third bump pads are electrically connected to the first to third LED stacks, respectively, and an upper surface of the n electrode pad is located at the same elevation as that of the lower p electrode pad.

[0011] An exemplary embodiment of the present disclosure provides a light emitting device for a display including: a first LED stack; a second LED stack disposed under the first LED stack; a third LED stack disposed under the second LED stack; a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack; a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack; a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack; bump pads disposed on the first LED stack, wherein each of the first to third LED stacks includes a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer, and at least one of the first to third transparent electrodes is recessed from an edge of the second conductivity type semiconductor layer of the first to third LED stacks.

[0012] Embodiments of the present disclosure provide a display apparatus including: a circuit board; and a plurality of light emitting devices arranged on the circuit board, wherein each of the light emitting devices is the light emitting device set forth above, and the electrode pads are electrically connected to the circuit board.

[Description of Drawings]

[0013]

FIG. 1 shows schematic perspective views illustrating display apparatuses according to exemplary embodiments.

FIG. 2 is a schematic plan view illustrating a display panel according to an exemplary embodiment.

FIG. 3A is a schematic plan view illustrating a light emitting device according to an exemplary embodiment.

FIG. 3B, FIG. 3C, and 3D are schematic cross-sectional views taken along the lines A-A', B-B', and C-C' of FIG. 3A, respectively.

FIG. 4A, FIG. 4B, and FIG. 4C are schematic cross-sectional views illustrating first, second, and third LED stacks grown on a growth substrate, respectively, according to an exemplary embodiment.

FIGS. 5A, 5B, 5C, 5D, 6A, 6B, 6C, 6D, 7A, 7B, 7C, 7D, 8A, 8B, 8C, 8D, 9A, 9B, 9C, 9D, 10A, 10B, 10C, 10D, 11A, 11B, 11C, 11D, 12A, 12B, 12C, 12D, 13A, 13B, 13C and 13D are schematic plan views and cross-sectional views illustrating a method of manufacturing a light emitting device for a display according to an exemplary embodiment.

FIG. 14 is a schematic cross-sectional view illustrating a light emitting device mounted on a circuit board according to an exemplary embodiment.

FIG. 15A, FIG. 15B, and FIG. 15C are schematic cross-sectional views illustrating a method of transferring a light emitting device to a circuit board according to an exemplary embodiment.

[Best Mode]

[0014] Hereinafter, embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. The following embodiments are provided by way of example so as to fully convey the spirit of the present disclosure to those skilled in the art to which the present disclosure pertains. Accordingly, the present disclosure is not limited to the embodiments disclosed herein and can also be implemented in different forms. In the drawings, widths, lengths, thicknesses, and the like of elements can be exaggerated for clarity and descriptive purposes. When an element or layer is referred to as being "disposed above" or "disposed on" another element or layer, it can be directly "disposed above" or "disposed on" the other element or layer or intervening elements or layers can be present. Throughout the specification, like reference numerals denote like elements having the same or similar functions.

[0015] A light emitting device for a display according to one embodiment of the present disclosure includes: a first LED stack; a second LED stack disposed under the first LED stack; a third LED stack disposed under the second LED stack; a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack; a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack; a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack; an n electrode pad disposed on a first conductivity type semiconductor layer of the third LED stack; a lower p electrode pad disposed on the third transparent electrode; and bump pads disposed on the first LED stack, wherein each of the first to third LED stacks includes a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer, the bump pads include first to third bump pads and common bump pads, wherein the common bump pad is commonly electrically connected to the first to third LED stacks, the first to third bump pads are electrically connected to the first to third LED stacks, respectively, and an upper surface of the n electrode pad is located at the same elevation as that of the lower p electrode pad.

[0016] In the present specification, it is described for convenience of description that the second LED stack is disposed under the first LED stack, and the third LED stack is disposed under the second LED stack, but the light emitting device may be flip-bonded. Therefore, it should be noted that upper and lower positions of these first to third LED stacks may be reversed.

[0017] With the structure where the first to third LED stacks are stacked one above another, the light emitting device may increase a luminous area of each subpixel without increasing a pixel area.

[0018] Furthermore, the upper surface of the n electrode pad is set to be located at the same elevation as that of the lower p electrode pad, and thus damage to any one of these pads may be prevented.

[0019] In one embodiment, the first LED stack may emit light having a longer wavelength than that of the second LED stack, and the second LED stack may emit light having a longer wavelength than that of the third LED stack. For example, the first, second and third LED stacks may emit red light, green light and blue light, respectively. In another embodiment, the first LED stack may emit light having a longer wavelength than that of the third LED stack, and the second LED stack may emit light having a shorter wavelength than that of the third LED stack. For example, the first, second and third LED stacks may emit red light, blue light and green light, respectively.

[0020] Meanwhile, the first to third LED stacks may be independently driven, light generated from the first LED stack may be emitted outside through the second LED stack and the third LED stack, and light generated from the second LED stack may be emitted outside through the third LED stack.

[0021] In one embodiment, any one of the first to third transparent electrodes may be formed of a material different from the remaining transparent electrodes. For example, the first transparent electrode may be formed of indium-tin-oxide (ITO), and the second and third transparent electrodes may be formed of ZnO.

[0022] Meanwhile, each of the first to third transparent electrodes may contact the second conductivity type semiconductor layer, and the second and third transparent electrodes may be recessed to have a smaller area than that of the second conductivity type semiconductor layer of the second LED stack and that of the second conductivity type semiconductor layer of the third LED stack, respectively.

[0023] The second and third transparent electrodes are recessed, and thus they may be prevented from being damaged by etching gas during the manufacturing process.

[0024] Further, the common bump pad may be commonly electrically connected to first conductivity type semiconductor layers of the first to third LED stacks, wherein the first to third bump pads may be electrically connected to second conductivity type semiconductor layers of first to third LED stacks, respectively. However, the present disclosure is not limited thereto, the common bump pad may be commonly electrically connected to the second conductivity type semiconductor layers of the first to third LED stacks, and the first to third bump pads may be electrically connected to the first conductivity type semiconductor layers of the third LED stacks, respectively.

[0025] Meanwhile, the light emitting device may further include an insulation layer covering side surfaces of the first to third LED stacks, wherein the side surfaces of the first to third LED stacks and a side surface of the first transparent electrode may be in contact with the insulation layer, and side surfaces of the second and third transparent electrodes may be spaced apart from the insulation layer.

[0026] Side surfaces of the light emitting device may be inclined at a range of 75 degrees to 90 degrees with respect to the upper surface of the third LED stack. The inclination angle of the side surfaces of the light emitting device is set to 75 degrees or more, and thus a luminous area of the first LED stack may be secured.

[0027] In addition, the light emitting device may further include a first bonding layer interposed between the second LED stack and the third LED stack; and a second bonding layer interposed between the first LED stack and the second LED stack.

[0028] In addition, the light emitting device may further include lower through holes passing through the second LED stack and the first bonding layer to expose the n electrode pad and the lower p electrode pad, respectively; a lower common connector connected to the n electrode pad; and a lower p connector connected to the lower p electrode pad, wherein the lower common connector may be electrically connected to the first conductivity type semiconductor layer of the LED stack, and connected to the n electrode pad exposed through the lower through hole, and the lower p connector may be electrically connected to the lower p electrode pad exposed through the lower through hole.

[0029] Moreover, the light emitting device may further include an upper p electrode pad which is disposed on the second transparent electrode and electrically connected to the second conductivity type semiconductor layer of the second LED stack.

[0030] Furthermore, the light emitting device may further include a through hole passing through the first LED stack to expose the first transparent electrode; through holes passing through the first LED stack, the first transparent electrode and the second bonding layer to expose the upper p electrode pad, the lower p connector, and the lower common connector, respectively; and first to third upper connectors and an upper common connector disposed on the first LED stack, and electrically connected to the first transparent electrode, the upper p electrode pad, the lower p connector, and the lower common connector through through holes passing through the first LED stack, wherein the bump pads may be disposed on the first to third upper connectors and the upper common connector, respectively.

[0031] In one embodiment, the bump pads may be located on flat portions of the first to third upper connectors and the upper common connector, respectively.

[0032] In addition, the light emitting device may further include an upper insulation layer covering the first to third upper connectors and the upper common connector, wherein the upper insulation layer may have openings exposing the first to third upper connectors and the upper common connector, and each of the bump pads may be disposed in the openings.

[0033] Furthermore, the light emitting device may further include an intermediate insulation layer disposed between the first LED stack and the upper connectors, wherein the intermediate insulation layer may cover a side surface of the light emitting device and a sidewall of the through hole passing through the first LED stack, and may include openings exposing the first transparent electrode, the upper p electrode pad, the lower p connector, and the lower common connector.

[0034] In this disclosure, the first to third LED stacks may be stacks separated from a growth substrate. The light emitting device does not have the growth substrate.

[0035] A light emitting device for a display according to another embodiment of the present disclosure may include: a first LED stack; a second LED stack disposed under the first LED stack; a third LED stack disposed under the second LED stack; a first transparent electrode

interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack; a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack; a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack; bump pads disposed on the first LED stack, wherein each of the first to third LED stacks may include a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer, and at least one of the first to third transparent electrodes may be recessed from an edge of the second conductivity type semiconductor layer of the first to third LED stacks.

[0036] Furthermore, the light emitting device may further include an n electrode pad disposed on the first conductivity type semiconductor layer of the third LED stack; a lower p electrode pad disposed on the third transparent electrode, wherein an upper surface of the n electrode pad may be located at the same elevation as that of the lower p electrode pad.

[0037] A display apparatus in accordance with one embodiment of the present disclosure includes: a circuit board; and a plurality of light emitting devices arranged on the circuit board, wherein each of the light emitting devices is the light emitting device set forth above and the bump pads are electrically connected to the circuit board.

[0038] Hereinafter, exemplary embodiments of the inventive concepts will be described in detail with reference to the accompanying drawings.

[0039] FIG. 1 shows schematic perspective views illustrating display apparatuses according to exemplary embodiments.

[0040] The display apparatus according to exemplary embodiments may be used in a VR display apparatus, such as a smart watch 1000a or a VR headset 1000b, or an AR display apparatus, such as augmented reality glasses 1000c. However, the inventive concepts are not limited thereto. The display apparatus may include a display panel for implementing an image.

[0041] FIG. 2 is a schematic plan view illustrating the display panel according to an exemplary embodiment.

[0042] Referring to FIG. 2, the display panel includes a circuit board 101 and light emitting devices 100.

[0043] The circuit board 101 may include a circuit for passive matrix driving or active matrix driving. In an exemplary embodiment, the circuit board 101 may include interconnection lines and resistors. In another exemplary embodiment, the circuit board 101 may include interconnection lines, transistors, and capacitors. The circuit board 101 may also have pads disposed on an upper surface thereof to allow electrical connection to the circuit therein.

[0044] A plurality of light emitting devices 100 are arranged on the circuit board 101. Each of the light emitting devices 100 may form one pixel. The light emitting device 100 includes bump pads 73, and the bump pads 73 are electrically connected to the circuit board 101. For example, the bump pads 73 may be bonded to pads exposed on the circuit board 101.

[0045] An interval between the light emitting devices 100 may be greater than at least a width of the light emitting device 100.

[0046] A configuration of the light emitting device 100 according to an exemplary embodiment will be described with reference to FIG. 3A, FIG. 3B, FIG. 3C, and FIG. 3D. FIG. 3A is a schematic plan view illustrating the light emitting device 100 according to an exemplary embodiment. FIG. 3B, FIG. 3C, and 3D are schematic cross-sectional views taken along the lines A-A', B-B', and C-C' of FIG. 3A, respectively. Hereinafter, although the bump pads 73r, 73b, 73g, and 73c are exemplarily illustrated and described as being disposed at an upper side in FIG. 3A to FIG. 3D, the inventive concepts are not limited thereto. For example, in some exemplary embodiments, the light emitting device 100 may be flip-bonded on the circuit board 101 shown in FIG. 2, and in this case, the bump pads 73r, 73b, 73g, and 73c may be disposed at a lower side.

[0047] Referring to FIG. 3A, FIG. 3B, FIG. 3C and FIG. 3D, the light emitting device 100 may include a first LED stack 23, a second LED stack 33, a third LED stack 43, a first transparent electrode 25, a second transparent electrode 35, a third transparent electrode 45, an n-electrode pad 47a, a lower p-electrode pad 47b, an upper p-electrode pad 53g, a lower p-connector 53b, a lower common connector 53c, an upper common connector 63c, a first upper connector 63r, a second upper connector 63g, a third upper connector 63b, a first bonding layer 49, a second bonding layer 59, a lower insulation layer 51, an intermediate insulation layer 61, an upper insulation layer 71, and bump pads 73a, 73b, 73c, and 73d. The light emitting device 100 may further include through holes 23h1, 23h2, 23h3, and 23h4 passing through the first LED stack 23, and through holes 33h1 and 33h2 passing through the second LED stack 33.

[0048] As shown in FIG. 3B, the first, second, and third LED stacks 23, 33, and 43 according to an exemplary embodiment are stacked in the vertical direction. The first, second, and third LED stacks 23, 33, and 43 may be grown on different growth substrates from each other, and according to the illustrated exemplary embodiment, each of the growth substrates may be removed from the final light emitting device 100. As such, the light emitting device 100 does not include the growth substrates of the first, second, and third LED stacks 23, 33, and 43. However, the inventive concepts are not limited thereto, and in some exemplary embodiments, at least one of the growth substrates may be included in the light emitting device 100.

[0049] Each of the first LED stack 23, the second LED stack 33 and the third LED stack 43 includes a first conductivity type semiconductor layer 23a, 33a, or 43a, a

second conductivity type semiconductor layer 23b, 33b, or 43b, and an active layer interposed therebetween. The active layer may have a multiple quantum well structure, for example.

[0050] The second LED stack 33 is disposed under the first LED stack 23, and the third LED stack 43 is disposed under the second LED stack 33. Light generated in the first to third LED stacks 23, 33, and 43 may be emitted to the outside through the third LED stack 43.

[0051] In an exemplary embodiment, the first LED stack 23 may emit light having a longer wavelength than those emitted from the second and third LED stacks 33 and 43, and the second LED stack 33 may emit light having a longer wavelength than that emitted from the third LED stack 43. For example, the first LED stack 23 may be an inorganic light emitting diode emitting red light, the second LED stack 33 may be an inorganic light emitting diode emitting green light, and the third LED stack 43 may be an inorganic light emitting diode to emitting blue light. For example, the first LED stack 23 may include an AlGaInP-based well layer, the second LED stack 33 may include an AlGaInP or AlGaInN-based well layer, and the third LED stack 43 may include an AlGaInN-based well layer.

[0052] Since the first LED stack 23 emits light having a longer wavelength than those emitted from the second and third LED stacks 33 and 43, light generated from the first LED stack 23 may be emitted to the outside after passing through the second and third LED stacks 33 and 43. In addition, since the second LED stack 33 emits light having a longer wavelength than that of emitted from the third LED stack 43, light generated from the second LED stack 33 may be emitted to the outside after passing through the third LED stack 43.

[0053] In another exemplary embodiment, the first LED stack 23 may emit light having a longer wavelength than those emitted from the second and third LED stacks 33 and 43, and the second LED stack 33 may emit light having a shorter wavelength than that emitted from the third LED stack 43. For example, the first LED stack 23 may be an inorganic light emitting diode emitting red light, the second LED stack 33 may be an inorganic light emitting diode emitting blue light, and the third LED stack 43 may be an inorganic light emitting diode emitting green light. For example, the first LED stack 23 may include an AlGaInP-based well layer, the second LED stack 33 may include an AlGaInN-based well layer, and the third LED stack 43 may include an AlGaInP-based or AlGaInN-based well layer.

[0054] A portion of light generated in the second LED 33 stack may be absorbed in the third LED stack 43, and thus, luminous intensity of light emitted from the second LED stack 33 may be relatively lower than that of light emitted from the first or third LED stacks 23 or 43. Accordingly, a ratio of luminance intensity of light emitted from the first to third LED stacks 23, 33, and 43 may be controlled.

[0055] According to the illustrated exemplary embodiment, the first conductivity type semiconductor layer 23a, 33a or 43a of each of the LED stacks 23, 33, and 43 may be an n-type semiconductor layer, and the second conductivity type semiconductor layer 23b, 33b or 43b thereof may be a p-type semiconductor layer. In addition, according to the illustrated exemplary embodiment, an upper surface of the first LED stack 23 may be an n-type semiconductor layer 23a, an upper surface of the second LED stack 33 may be a p-type semiconductor layer 33b, and an upper surface of the third LED stack 43 may be a p-type semiconductor layer 43b. More particular, the first LED stack 23 has a stacked sequence of semiconductor layers different from those of the second and third LED stacks 33 and 43. The semiconductor layers of the second LED stack 33 are stacked in the same order as the semiconductor layers of the third LED stack 43, and thus, process stability may be enhanced, which will be described in more detail later with reference to a manufacturing method.

[0056] The second LED stack 33 includes a mesa etching region, in which a portion of the second conductivity type semiconductor layer 33b is removed to expose an upper surface of the first conductivity type semiconductor layer 33a. The third LED stack 43 also includes a mesa etching region, in which a portion of the second conductivity type semiconductor layer 43b is removed to expose an upper surface of the first conductivity type semiconductor layer 43a. The first LED stack 23, however, may not include a mesa etching region. The through holes 33h1 and 33h2 may be formed in the mesa etching regions, and thus, sidewalls of the through holes 33h1 and 33h2 may have a stepped structure. In this case, since the first LED stack 23 does not include the mesa etching region, the through holes 23h1, 23h2, 23h3, and 23h4 may have uniformly inclined sidewalls without having stepped sidewalls.

[0057] The third LED stack 43 according to an exemplary embodiment may have a flat lower surface, without being limited thereto. For example, the third LED stack 43 may include irregularities on a surface of the first conductivity type semiconductor layer 43a, and light extraction efficiency may be improved by the irregularities. The irregularities on the surface of the first conductivity type semiconductor layer 43a may be formed by separating a patterned sapphire substrate or by texturing the surface after separating the growth substrate, for example. In some exemplary embodiments, the first conductivity type semiconductor layer 33a of the second LED stack 33 may also have a textured surface.

[0058] The first LED stack 23, the second LED stack 33 and the third LED stack 43 according to the illustrated exemplary embodiment may be stacked to overlap one another, and may also have substantially the same luminous area. However, the luminous area of the first LED stack 23 may be smaller than that of the second LED stack 33, and the luminous area of the second LED stack 33 may be smaller than that of the third LED stack 43, by the through holes 23h1, 23h2, 23h3, and 23h4 and

the through holes 33h1 and 33h2. In addition, a side surface of the light emitting device 100 may be inclined, such that a width of the light emitting device 100 may be gradually increasing from the first LED stack 23 to the third LED stack 43. As such, the luminous area of the third LED stack 43 may be larger than that of the first LED stack 23. An inclination angle of the side surface of the light emitting device 100 with respect to the upper surface of the third LED stack 43 may be about 75 degrees to about 90 degrees. When the inclination angle is less than 75 degrees, the luminous area of the first LED stack 23 may become too small, and thus, it may be difficult to reduce a size of the light emitting device 100.

[0059] The first transparent electrode 25 is disposed between the first LED stack 23 and the second LED stack 33. The first transparent electrode 25 is in ohmic contact with the second conductivity type semiconductor layer 23b of the first LED stack 23, and transmits light generated by the first LED stack 23. The first transparent electrode 25 may be formed using a transparent oxide layer or a metal layer, such as indium tin oxide (ITO). The first transparent electrode 25 may cover an entire surface of the second conductivity type semiconductor layer 23b of the first LED stack 23, and a side surface thereof may be disposed in parallel with a side surface of the first LED stack 23. More particular, the side surface of the first transparent electrode 25 may not be covered with the second bonding layer 59. Furthermore, the through holes 23h2, 23h3, and 23h4 may pass through the first transparent electrode 25, and thus, the first transparent electrode 25 may be exposed by the sidewalls of the through holes 23h2, 23h3, and 23h4. Meanwhile, the through hole 23h1 exposes an upper surface of the first transparent electrode 25. However, the inventive concepts are not limited thereto, and in some exemplary embodiments, the first transparent electrode 25 may be partially removed along an edge of the first LED stack 23, and thus, at least a portion of the side surface of the first transparent electrode 25 may be covered with the second bonding layer 59. In addition, when the first transparent electrode 25 is previously patterned and removed in a region where the through holes 23h2, 23h3, and 23h4 are formed according to other exemplary embodiments, the first transparent electrode 25 may not be exposed by the sidewalls of the through holes 23h2, 23h3, and 23h4.

[0060] A second transparent electrode 35 is in ohmic contact with the second conductivity type semiconductor layer 33b of the second LED stack 33. As shown in the drawings, the second transparent electrode 35 contacts the upper surface of the second LED stack 33 between the first LED stack 23 and the second LED stack 33. The second transparent electrode 35 may be formed of a metal layer or a conductive oxide layer that is transparent to red light. For example, the conductive oxide layer may include SnO_2, InO_2, ITO, ZnO, IZO, or the like. In particular, the second transparent electrode 35 may be formed of ZnO, which may be formed as a single crystal on the second LED stack 33. In this manner, the ZnO may have favorable electrical and optical characteristics as compared with the metal layer or other conductive oxide layers. In particular, ZnO has a strong bonding force to the second LED stack 33, and remains undamaged even when the growth substrate is separated using a laser lift-off process during manufacture.

[0061] The second transparent electrode 35 may be partially removed along an edge of the second LED stack 33, and, accordingly, an outer side surface of the second transparent electrode 35 is not exposed to the outside, but is covered with the lower insulation layer 51. In particular, the side surface of the second transparent electrode 35 is recessed inwardly than that of the second LED stack 33, and a region where the second transparent electrode 35 is recessed is filled with the lower insulation layer 51 and the second bonding layer 59. The second transparent electrode 35 is also recessed near the mesa etching region of the second LED stack 33, and the recessed region is filled with the lower insulation layer 51 and the second bonding layer 59.

[0062] The third transparent electrode 45 is in ohmic contact with the second conductivity type semiconductor layer 43b of the third LED stack 43. The third transparent electrode 45 may be disposed between the second LED stack 33 and the third LED stack 43, and contacts the upper surface of the third LED stack 43. The third transparent electrode 45 may be formed of a metal layer or a conductive oxide layer that is transparent to red light and green light. For example, the conductive oxide layer may include SnO_2, InO_2, ITO, ZnO, IZO, or the like. In particular, the third transparent electrode 45 may be formed of ZnO, which may be formed as a single crystal on the third LED stack 43. In this manner, the ZnO may have favorable electrical and optical characteristics as compared with the metal layer or other conductive oxide layers. In particular, ZnO has a strong bonding force to the third LED stack 43, and remains undamaged even when the growth substrate is separated using the laser lift-off process during manufacture.

[0063] The third transparent electrode 45 may be partially removed along an edge of the third LED stack 43, and, accordingly, an outer side surface of the third transparent electrode 45 is not exposed to the outside, but is covered with the first bonding layer 49. In particular, the side surface of the third transparent electrode 45 is recessed inwardly than that of the third LED stack 43, and a region where the third transparent electrode 45 is recessed is filled with the first bonding layer 49. The third transparent electrode 45 is also recessed near the mesa etching region of the third LED stack 43, and the recessed region is filled with the first bonding layer 49.

[0064] The second transparent electrode 35 and the third transparent electrode 45 are recessed as described above, and thus, the side surfaces of the second transparent electrode 35 and the third transparent electrode 45 may be prevented from being exposed to an etching gas, thereby improving the production yield of the light emitting device 100.

[0065] According to an exemplary embodiment, the second transparent electrode 35 and the third transparent electrode 45 may be formed of the same kind of conductive oxide layer, for example, ZnO, and the first transparent electrode 25 may be formed of a different kind of conductive oxide layer from the second and third transparent electrodes 35 and 45, such as ITO. However, the inventive concepts are not limited thereto, and each of the first to third transparent electrodes 25, 35, and 45 may be of the same kind, or at least one may be of a different kind.

[0066] The first to third transparent electrodes 25, 35, and 45 may be formed using a technique, such as thermal deposition, sputtering, sol-gel, hydrothermal synthesis, or the like. In particular, a transparent electrode formed through a chemically thin-film forming method, such as hydrothermal synthesis method, may generate a porous thin-film. In this case, voids in the porous thin-film may improve the light extraction efficiency of the LED stack, and may further relieve stress.

[0067] The voids may be controlled to be distributed at locations to enhance the optical properties of the LED stack. According to an exemplary embodiment, the voids may be distributed generally close to a side of the second conductivity type semiconductor layer 22b, 33b, and 43b at one half point of the transparent electrode. The transparent electrode formed through the hydrothermal synthesis method may have voids and also have crystallinity, and, in particular, may be formed of a single crystal.

[0068] According to another exemplary embodiment, the voids may be distributed relatively uniformly over a wide area. The transparent electrode including the voids has an improved light extraction efficiency compared to a transparent electrode without the voids. The transparent electrode may be, for example, a ZnO layer or a doped ZnO layer. The doped ZnO layer may include at least one of, for example, silver (Ag), indium (In), tin (Sn), zinc (Zn), cadmium (Cd), gallium (Ga), aluminum (Al), magnesium (Mg), titanium (Ti), molybdenum (Mo), nickel (Ni), copper (Cu), gold (Au), platinum (Pt), rhodium (Rh), iridium (Ir), ruthenium (Ru), and palladium (Pd), as a dopant.

[0069] In an exemplary embodiment, the ZnO layer may also include a ZnO seed layer and a ZnO bulk layer. The ZnO seed layer has a relatively continuous surface. In addition, the ZnO seed layer and the ZnO bulk layer form a single crystal structure. In an exemplary embodiment, the ZnO seed layer and the ZnO bulk layer do not exhibit any interface between the ZnO seed layer and the ZnO bulk layer. In an exemplary embodiment, the ZnO seed layer has a thickness of several hundred angstroms. The ZnO seed layer may have, for example, a thickness of 200 angstroms or less. The ZnO bulk layer may have a thickness of 1 μm or less. In an exemplary embodiment, the ZnO bulk layer has a thickness of 8000 angstroms or less.

[0070] The n-electrode pad 47a is in ohmic contact with the first conductivity type semiconductor layer 43a of the third LED stack 43. The n-electrode pad 47a may be disposed on the first conductivity type semiconductor layer 43a exposed through the second conductivity type semiconductor layer 43b, that is, in the mesa etching region. The n-electrode pad 47a may be formed of, for example, Cr/Au/Ti. An upper surface of the n-electrode pad 47a may be placed higher than that of the second conductivity type semiconductor layer 43b, and further, higher than that of the third transparent electrode 45. For example, a thickness of the n-electrode pad 47a may be about 2 μm or more. The n-electrode pad 47a may have a shape of a truncated cone, but is not limited thereto. The n-electrode pad 47a may have various shapes, such as a square pyramid, a cylindrical shape, or a cylindrical shape.

[0071] The lower p-electrode pad 47b may include substantially the same material as the n-electrode pad 47a. An upper surface of the lower p-electrode pad 47b is located at the substantially same elevation as the n-electrode pad 47a, and, accordingly, a thickness of the lower p-electrode pad 47b may be less than that of the n-electrode pad 47a. More particularly, the thickness of the lower p-electrode pad 47b may be approximately equal to a thickness of a portion of the n-electrode pad 47a protruding above the second transparent electrode 45. For example, the thickness of the lower p-electrode pad 47b may be about 1.2 μm or less. The upper surface of the lower p-electrode pad 47b is located at substantially the same elevation as that of the n-electrode pad 47a, and thus, the lower p-electrode pad 47b and the n-electrode pad 47a may be simultaneously exposed when the through holes 33h1 and 33h2 are formed. When the elevations of the n-electrode pad 47a and the lower p-electrode pad 47b are different, any one of the electrode pads may be damaged in the etching process. As such, the elevations of the n-electrode pad 47a and the lower p-electrode pad 47b are set to be approximately equal, and thus, it is possible to prevent any one of the electrode pads from being damaged during the etching process or the like.

[0072] The first bonding layer 49 couples the second LED stack 33 to the third LED stack 43. The first bonding layer 49 may be disposed between the first conductivity type semiconductor layer 33a and the third transparent electrode 45. The first bonding layer 49 may partially contact the second conductivity type semiconductor layer 43b, and may partially contact the first conductivity type semiconductor layer 43a exposed by the mesa etching region. In addition, the first bonding layer 49 may cover the n-electrode pad 47a and the lower p-electrode pad 47.

[0073] The first bonding layer 49 may be formed of a transparent organic material layer, or may be formed of a transparent inorganic material layer. For example, the organic material layer may include SU8, poly methylmethacrylate (PMMA), polyimide, parylene, benzocyclobutene (BCB), or the like, and the inorganic material layer may include Al_2O_3, SiO_2, SiNx, or the like. In addition, the first bonding layer 49 may be formed of spin-on-

glass (SOG).

[0074] The through hole 33h1 and the through hole 33h2 pass through the second LED stack 33 and the first bonding layer 49 to expose the n-electrode pad 47a and the lower p-electrode pad 47b, respectively. As described above, the through holes 33h1 and 33h2 may be formed in the mesa etching region, and thus, the through holes 33h1 and 33h2 may have stepped sidewalls.

[0075] The lower insulation layer 51 is formed on the second LED stack 33, and covers the second transparent electrode 35. The lower insulation layer 51 also covers the sidewalls of the through holes 33h1 and 33h2. The lower insulation layer 51 may have openings 51a exposing the n-electrode pad 47a, the lower p-electrode pad 47b, the first conductivity type semiconductor layer 33a, and the second transparent electrode 35. The lower insulation layer 51 may be formed of a silicon oxide film or a silicon nitride film, and may be formed to have a thickness of, for example, about 800 nm.

[0076] The lower common connector 53c may be disposed on the lower insulation layer 51, and connected to the first conductivity type semiconductor layer 33a and the n-electrode pad 47a exposed through the openings 51a of the lower insulation layer 51. In particular, the lower common connector 53c is connected to the first conductivity type semiconductor layer 33a in the mesa etching region of the second LED stack 33, and is connected to the n-electrode pad 47a through the through hole 33h1.

[0077] The lower p-connector 53b may be disposed on the lower insulation layer 51, and connected to the lower p-electrode pad 47b exposed through the opening 51a of the lower insulation layer 51. At least a portion of the lower p-connector 53b is disposed on the lower insulation layer 51.

[0078] The upper p-electrode pad 53g may be disposed on the second transparent electrode 35 in the opening 51a of the lower insulation layer 51. As shown in FIG. 3A and FIG. 3C, the upper p-electrode pad 53g may be disposed in the opening 51a with a narrower width than that of the opening 51a. However, the inventive concepts are not limited thereto, and in some exemplary embodiments, the width of the upper p-electrode pad 53g may be greater than that of the opening 51a, and a portion of the upper p-electrode pad 53g may be disposed on the lower insulation layer 51.

[0079] The lower common connector 53c, the lower p-connector 53b, and the upper p-electrode pad 53g may be formed together in the same process and may include substantially the same material. For example, the lower common connector 53c, the lower p-connector 53b, and the upper p-electrode pad 53g may include Ni/Au/Ti, and may be formed to have a thickness of about 2 μm.

[0080] The second bonding layer 59 couples the first LED stack 23 to the second LED stack 33. As shown, the second bonding layer 59 may be disposed between the first transparent electrode 25 and the lower insulation layer 51. The second bonding layer 59 may also cover the lower common connector 53c, the lower p-connector 53b, and the upper p-electrode pad 53g. The second bonding layer 59 may also partially contact the second transparent electrode 35 exposed through the opening 51a of the lower insulation layer 51. The second bonding layer 59 may include substantially the same material that may form the first bonding layer 49 described above, and thus, repeated descriptions thereof will be omitted to avoid redundancy.

[0081] The through holes 23h1, 23h2, 23h3, and 23h4 pass through the first LED stack 23. The through hole 23h1 is formed to provide a passage for allowing electrical connection to the first transparent electrode 25. In the illustrated exemplary embodiment, the through hole 23h1 exposes the upper surface of the first transparent electrode 25, and does not pass through the first transparent electrode 25. However, the inventive concepts are not limited thereto, and in some exemplary embodiments, the through hole 23h1 may pass through the first transparent electrode 25, as long as the through hole 23h1 provides the passage for electrical connection to the first transparent electrode 25.

[0082] The through holes 23h2, 23h3, and 23h4 may pass through the first LED stack 23, and may also pass through the second bonding layer 59. The through hole 23h2 exposes the upper p-electrode pad 53g, the through hole 23h3 exposes the lower p-connector 53b, and the through hole 23h4 exposes the lower common connector 53c.

[0083] The through holes 23h1, 23h2, 23h3, and 23h4 may be formed by etching the first conductivity type semiconductor layer 23a and the second conductivity type semiconductor layer 23b in the same process, and thus, the sidewalls of the through holes 23h1, 23h2, 23h3, and 23h4 may have inclined surfaces without having a stepped structure.

[0084] The intermediate insulation layer 61 covers the first LED stack 23, and covers the sidewalls of the through holes 23h1, 23h2, 23h3, and 23h4. The intermediate insulation layer 61 may also cover side surfaces of the first to third LED stacks 23, 33, and 43. The intermediate insulation layer 61 may be patterned to have openings 61a exposing a bottom portion of each of the through holes 23h1, 23h2, 23h3, and 23h4. The first transparent electrode 25, the upper p-electrode pad 53g, the lower p-connector 53b, and the lower common connector 53c may be exposed in the through holes 23h1, 23h2, 23h3, and 23h4 by the openings 61a. Further, the intermediate insulation layer 61 may have an opening 61b exposing the upper surface of the first LED stack 23, that is, the first conductivity type semiconductor layer 23a. The intermediate insulation layer 61 may be formed of an aluminum oxide film, a silicon oxide film, or a silicon nitride film, and may be formed to have a thickness of, for example, about 800 nm.

[0085] The first upper connector 63r, the second upper connector 63g, the third upper connector 63b, and the upper common connector 63c are disposed on the intermediate insulation layer 61. Each of the upper connectors

63r, 63g, 63b, and 63c is connected to the first transparent electrode 25, the upper p-electrode pad 53g, and the lower p-connector 53b exposed through the openings 61a of the intermediate insulation layer 61, respectively. Furthermore, the upper common connector 63c may be connected to the first conductivity type semiconductor layer 23a exposed to the opening 61b.

[0086] The first upper connector 63r, the second upper connector 63g, the third upper connector 63b, and the upper common connector 63c may be formed of substantially the same material, for example, AuGe/Ni/Au/Ti, in the same process. In this case, AuGe may be in ohmic contact with the first conductivity type semiconductor layer 23a. AuGe may be formed to have a thickness of about 100nm, and Ni/Au/Ti may be formed to have a thickness of about 2um. In some exemplary embodiments, AuTe may replace AuGe.

[0087] The upper insulation layer 71 covers the intermediate insulation layer 61, and covers the first upper connector 63r, the second upper connector 63g, the third upper connector 63b, and the upper common connector 63c. The upper insulation layer 71 may also cover the intermediate insulation layer 61 on the side surfaces of the first to third LED stacks 23, 33, and 43. The upper insulation layer 71 may have openings 71a exposing the first upper connector 63r, the second upper connector 63g, the third upper connector 63b, and the upper common connector 63c. The openings 71a of the upper insulation layer 71 may be generally disposed on flat surfaces of the first upper connector 63r, the second upper connector 63g, the third upper connector 63b, and the upper common connector 63c. The upper insulation layer 71 may be formed of a silicon oxide film or a silicon nitride film, and may be formed thinner than the intermediate insulation layer 61, for example, about 400 nm thick.

[0088] Each of the bump pads 73r, 73g, 73b, and 73c may be disposed on the first upper connector 63r, the second upper connector 63g, and the third upper connector 63b, and the common connector 63c in the openings 71a of the upper insulation layer 71 and electrically connected thereto.

[0089] The first bump pad 73r may be electrically connected to the second conductivity type semiconductor layer 23b of the first LED stack 23 through the first upper connector 63r and the first transparent electrode 25.

[0090] The second bump pad 73g may be electrically connected to the second conductivity type semiconductor layer 33b of the second LED stack 33 through the second upper connector 63g, the upper p-electrode pad 53g, and the second transparent electrode 35.

[0091] The third bump pad 73b may be electrically connected to the second conductivity type semiconductor layer 43b of the third LED stack 43 through the third upper connector 63b, the lower p-connector 53b, the lower p-electrode pad 47b, and the third transparent electrode 45.

[0092] The common bump pad 73c may be electrically connected to the first conductivity type semiconductor layer 23a of the first LED stack 23 through the upper common connector 63c, electrically connected to the first conductivity type semiconductor layer 33a of the second LED stack 33 through the lower common connector 53c, and electrically connected to the first conductivity type semiconductor layer 43a of the third LED stack 43 through the n-electrode pad 47a.

[0093] As such, each of the first to third bump pads 73r, 73g, and 73b may be electrically connected to the second conductivity type semiconductor layers 23b, 33b, and 43b of the first to third LED stacks 23, 33, and 43, and the common bump pad 73c may be commonly electrically connected to the first conductivity type semiconductor layers 23a, 33a, and 43a of the first to third LED stacks 23, 33, and 43.

[0094] The bump pads 73r, 73g, 73b, and 73c may be disposed in the openings 71a of the upper insulation layer 71, and upper surfaces of the bump pads 73r, 73g, 73b, and 73c may be substantially flat. The bump pads 73r, 73g, 73b, and 73c may be disposed on the flat surfaces of the first to third upper connectors 63r, 63g, and 63b, and the upper common connector 63c. The bump pads 73r, 73g, 73b, and 73c may be formed of Au/In. For example, Au may be formed to have a thickness of about 3 μm, and In may be formed to have a thickness of about 1 μm. According to an exemplary embodiment, the light emitting device 100 may be bonded to the pads on the circuit board 101 using In. However, the inventive concepts are not limited thereto, and in some exemplary embodiments, the light emitting device 100 may be bonded to the pads using Pb or AuSn of the bump pads.

[0095] In the illustrated exemplary embodiment, the upper surfaces of the bump pads 73r, 73g, 73b, and 73c are described and illustrated as being flat, but the inventive concepts are not limited thereto. For example, in some exemplary embodiments, the bump pads 73r, 73g, 73b, and 73c may have irregular upper surfaces, and some of the bump pads may be disposed on the upper insulation layer 71.

[0096] According to the illustrated exemplary embodiment, the first LED stack 23 is electrically connected to the bump pads 73r and 73c, the second LED stack 33 is electrically connected to the bump pads 73g and 73c, and the third LED stack 43 is electrically connected to the bump pads 73b and 73c. Accordingly, cathodes of the first LED stack 23, the second LED stack 33, and the third LED stack 43 are electrically connected to the common bump pad 73c, and anodes thereof are electrically connected to the first to third bump pads 73a, 73b, and 73c, respectively. Accordingly, the first to third LED stacks 23, 33, and 43 may be driven independently.

[0097] A structure of the light emitting device 100 will be further described through a method of manufacturing the light emitting device 100 described below. FIG. 4A, FIG. 4B, and FIG. 4C are schematic cross-sectional views illustrating the first to third LED stacks grown on growth substrates, respectively, according to an exemplary embodiment.

[0098] First, referring to FIG. 4A, a first LED stack 23

including a first conductivity type semiconductor layer 23a and a second conductivity type semiconductor layer 23b is grown on a first substrate 21. An active layer may be interposed between the first conductivity type semiconductor layer 23a and the second conductivity type semiconductor layer 23b.

[0099] The first substrate 21 may be a substrate capable of growing the first LED stack 23 thereon, such as a GaAs substrate. The first conductivity type semiconductor layer 23a and the second conductivity type semiconductor layer 23b may be formed of an AlGaInAs-based or AlGaInP-based semiconductor layer, and the active layer may include, for example, an AlGaInP-based well layer. A composition ratio of AlGaInP may be determined so that the first LED stack 23 emits red light, for example.

[0100] A first transparent electrode 25 may be formed on the second conductivity type semiconductor layer 23b. As described above, the first transparent electrode 25 may be formed of a metal layer or a conductive oxide layer that transmits light generated by the first LED stack 23, for example, red light. The first transparent electrode 25 may be formed of, for example, indium-tin oxide (ITO).

[0101] Referring to FIG. 4B, a second LED stack 33 including a first conductivity type semiconductor layer 33a and a second conductivity type semiconductor layer 33b is grown on a second substrate 31. An active layer may be interposed between the first conductivity type semiconductor layer 33a and the second conductivity type semiconductor layer 33b.

[0102] The second substrate 31 may be a substrate capable of growing the second LED stack 33 thereon, such as a sapphire substrate, a GaN substrate, or a GaAs substrate. The first conductivity type semiconductor layer 33a and the second conductivity type semiconductor layer 33b may be formed of an AlGaInAs-based or AlGaInP-based semiconductor layer, an AlGaInN-based semiconductor layer, and the active layer may include, for example, an AlGaInP-based well layer or AlGaInN-based well layer. A composition ratio of AlGaInP or AlGaInN may be determined so that the second LED stack 33 emits green light, for example.

[0103] A second transparent electrode 35 may be formed on the second conductivity type semiconductor layer 33b. As described above, the second transparent electrode 35 may be formed of a metal layer or a conductive oxide layer that transmits light generated by the first LED stack 23, for example, red light. In particular, the second transparent electrode 35 may be formed of ZnO.

[0104] Referring to FIG. 4C, a third LED stack 43 including a first conductivity type semiconductor layer 43a and a second conductivity type semiconductor layer 43b is grown on a third substrate 41. An active layer may be interposed between the first conductivity type semiconductor layer 43a and the second conductivity type semiconductor layer 43b.

[0105] The third substrate 41 may be a substrate capable of growing the third LED stack 43 thereon, such as a sapphire substrate, a SiC substrate, or a GaN substrate. In an exemplary embodiment, the third substrate 41 may be a flat sapphire substrate, but may also be a patterned sapphire substrate. The first conductivity type semiconductor layer 43a and the second conductivity type semiconductor layer 43b may be formed of an AlGaInN-based semiconductor layer, and the active layer may include, for example, an AlGaInN-based well layer. A composition ratio of AlGaInN may be determined so that the third LED stack 43 emits blue light, for example.

[0106] A third transparent electrode 45 may be formed on the second conductivity type semiconductor layer 43b. As described above, the third transparent electrode 45 may be formed of a metal layer or a conductive oxide layer that transmits light generated in the first and second LED stacks 23 and 33, for example, red light and green light. In particular, the third transparent electrode 45 may be formed of ZnO.

[0107] The first to third LED stacks 23, 33, and 43 are grown on the different growth substrates 21, 31, and 41, respectively, and, accordingly, the order of the manufacturing process is not particularly limited.

[0108] Hereinafter, a method of manufacturing the light emitting device 100 using first to third LED stacks 23, 33, and 43 grown on growth substrates 21, 31, and 41 will be described. Hereinafter, although a region of a single light emitting device 100 will be mainly illustrated and described, a plurality of light emitting devices 100 may be manufactured in a batch in the same manufacturing process using the LED stacks 23, 33, and 43 grown on the growth substrates 21, 31, and 41.

[0109] FIGS. 5A, 5B, 5C, 5D, 6A, 6B, 6C, 6D, 7A, 7B, 7C, 7D, 8A, 8B, 8C, 8D, 9A, 9B, 9C, 9D, 10A, 10B, 10C, 10D, 11A, 11B, 11C, 11D, 12A, 12B, 12C, 12D, 13A, 13B, 13C, and 13D are schematic plan views and cross-sectional views illustrating the method of manufacturing the light emitting device 100 for a display according to an exemplary embodiment of the present disclosure. Hereinafter, the cross-sectional views are shown to correspond to those shown in FIGS. 3B, 3C, and 3D, respectively.

[0110] First, referring to FIG. 5A, FIG. 5B, FIG. 5C, and FIG. 5D, the third transparent electrode 45 and the second conductivity type semiconductor layer 43b of the third LED stack 43 are patterned to expose the first conductivity type semiconductor layer 43a using photo and etching techniques. This process corresponds to, for example, a mesa etching process. A photoresist pattern may be used as an etching mask. For example, after the etching mask is formed, the third transparent electrode 45 may be etched first by a wet etching technique, and then the second conductivity type semiconductor layer 43b may be etched by a dry etching technique using the same etching mask. In this manner, the third transparent electrode 45 may be recessed from a mesa etching region. FIG. 5A exemplarily shows an edge of the mesa and does not show an edge of the third transparent electrode 45 to simplify illustrating. However, since the third trans-

parent electrode 45 is wet etched using the same etching mask, the edge of the third transparent electrode 45 may also be recessed from the edge of the mesa toward an inner side of the mesa. Since the same etching mask is used, the number of photo processes may not be increased, thereby reducing the process costs. However, the inventive concepts are not limited thereto, and the etching mask for etching the mesa etching process may be different from the etching mask for etching the third transparent electrode 45.

[0111] Subsequently, an n-electrode pad 47a and a lower p-electrode pad 47b are formed on the first conductivity type semiconductor layer 43a and the third transparent electrode 45, respectively. The n-electrode pad 47a and the lower p-electrode pad 47b may be formed to have different thicknesses. In particular, an upper surface of the n-electrode pad 47a and that of the lower p-electrode pad 47b may be located at substantially the same elevation.

[0112] Referring to FIG. 6A, FIG. 6B, FIG. 6C, and FIG. 6D, the second LED stack 33 shown in FIG. 4B is bonded onto the third LED stack 43 described with reference to FIG. 5A, FIG. 5B, FIG. 5C, and FIG. 5D. The second LED stack 33 is bonded to a temporary substrate using a temporary bonding/ debonding (TBDB) technique, and the second substrate 31 is removed from the second LED stack 33. The second substrate 31 may be removed using, for example, a laser lift off technique. After the second substrate 31 is removed, a roughened surface may be formed on a surface of the first conductivity type semiconductor layer 33a. Thereafter, the first conductivity type semiconductor layer 33a of the second LED stack 33 bonded to the temporary substrate may be disposed to face the third LED stack 43 and bonded to the third LED stack 43. The second LED stack 33 and the third LED stack 43 are bonded to each other by a first bonding layer 49. After bonding the second LED stack 33 to the third LED stack 43, the temporary substrate may be removed using the laser lift off technique. Accordingly, the second LED stack 33 may be disposed on the third LED stack 43, in which the second transparent electrode 35 may form an upper surface.

[0113] In general, when the second transparent electrode 35 is formed of ITO, ITO may be peeled from the second LED stack 33 when the second substrate 31 is removed using the laser lift off technique. As such, when the second substrate 31 is to be removed using the laser lift-off technique, the second transparent electrode 35 may include ZnO, which has a favorable bonding force.

[0114] Subsequently, the second transparent electrode 35 and the second conductivity type semiconductor layer 33b are patterned to expose the first conductivity type semiconductor layer 33a. The second transparent electrode 35 and the second conductivity type semiconductor layer 33b may be patterned by using photo and etching techniques. This process may be performed using the wet etching and the dry etching techniques in substantially the same manner as the mesa etching process, during which the third transparent electrode 45 and the second conductivity type semiconductor layer 43b are etched as described above.

[0115] For example, after the etching mask is formed, the second transparent electrode 35 may be etched first by the wet etching technique, and then the second conductivity type semiconductor layer 33b may be etched by the dry etching technique using the same etching mask. Accordingly, the second transparent electrode 35 may be recessed from the mesa etching region. FIG. 6A exemplarily shows an edge of the mesa, and does not show an edge of the second transparent electrode 35 to simplify illustration. However, since the second transparent electrode 35 is wet etched using the same etching mask, the edge of the second transparent electrode 35 may also be recessed from the edge of the mesa toward an inner side of the mesa. In this manner, since the same etching mask is used, the number of photo processes may not be increased, thereby reducing the process costs. However, the inventive concepts are not limited thereto, and in some exemplary embodiments, the etching mask for etching the mesa etching process and the etching mask for etching the second transparent electrode 35 may be different from each other.

[0116] As shown in FIG. 6A, a mesa etching region of the second LED stack 33 may be partially overlapped with that of the third LED stack 43. For example, a portion of the mesa etching region of the second LED stack 33 may be formed over the n-electrode pad 47a. In addition, another portion of the mesa etching region thereof may be disposed over the lower p-electrode pad 47b. In addition, a portion of the mesa etching region of the second LED stack 33 may be disposed on the mesa region of the third LED stack 43.

[0117] Referring to FIG. 7A, FIG. 7B, FIG. 7C, and FIG. 7D, through holes 33h1 and 33h2 passing through the second LED stack 33 are formed. The through holes 33h1 and 33h2 pass through the first bonding layer 49 to expose the n-electrode pad 47a and the lower p-electrode pad 47b. The through holes 33h1 and 33h2 may be formed in the mesa etching region, and thus, a stepped structure may be formed on sidewalls of the through holes 33h1 and 33h2.

[0118] Since the upper surfaces of the lower p-electrode pad 47b and the n-electrode pad 47a are located at substantially the same elevation, any one of the pads may be prevented from being exposed and damaged during the formation of the through holes 33h1 and 33h2.

[0119] Referring to FIG. 8A, FIG. 8B, FIG. 8C, and FIG. 8D, a lower insulation layer 51 is formed on the second LED stack 33. The lower insulation layer 51 covers the second transparent electrode 35, and covers the second conductivity type semiconductor layer 33b. In addition, the lower insulation layer 51 covers the sidewalls of the through holes 33h1 and 33h2. The lower insulation layer 51 may have openings 51a exposing the second transparent electrode 35, the first conductivity type semiconductor layer 33a, the n-electrode pad 47a and the lower

p-electrode pad 47b.

[0120] Subsequently, a lower common connector 53c, a lower p-connector 53b, and an upper p-electrode pad 53g are formed on the lower insulation layer 51. The lower common connector 53c, the lower p-connector 53b, and the upper p-electrode pad 53g may be formed together with the same material.

[0121] An upper p-electrode pad 53g may be disposed on the second transparent electrode 35 exposed in the opening 51a. The lower p-connector 53b is connected to the lower p-electrode pad 47b exposed through the opening 51a, and is also partially disposed on the lower insulation layer 51. The lower common connector 53c is connected to the first conductivity type semiconductor layer 33a and the n-electrode pad 47a exposed through the openings 51a, and a portion of the lower common connector 53c is disposed on the lower insulation layer 51.

[0122] Referring to FIG. 9A, FIG. 9B, FIG. 9C and FIG. 9D, the first LED stack 23 of FIG. 4A is bonded to the second LED stack 33. The first LED stack 23 and the second LED stack 33 may be bonded using a second bonding layer 59, so that the first transparent electrode 25 faces the second LED stack 33. Accordingly, the second bonding layer 59 is in contact with the first transparent electrode 25, and also is in contact with the lower insulation layer 51, the lower p-connector 53b, the upper p-electrode pad 53g, and the lower common connector 53c, and, further, in contact with the second transparent electrode 35 exposed in a periphery of the lower p-connector 53b. The first substrate 21 is removed from the first LED stack 23. The first substrate 21 may be removed using, for example, an etching technique.

[0123] Referring to FIG. 10A, FIG. 10B, FIG. 10C, and FIG. 10D, through holes 23h1, 23h2, 23h3, and 23h4 passing through the first LED stack 23 are formed. The through hole 23h1 exposes the first transparent electrode 25, and the through holes 23h2, 23h3, and 23h4 pass through the second bonding layer 59 to expose the upper p-electrode pad 53g, the lower p-connector 53b, and the lower common connector 53c, respectively. Since the through holes 23h1 and the through holes 23h2, 23h3, and 23h4 have different depths, they may be formed by different processes. Meanwhile, the through holes 23h2, 23h3, and 23h4 may be formed together in the same process because the depths thereof are substantially the same.

[0124] The through holes 23h1, 23h2, 23h3, and 23h4 may be formed to pass through the first LED stack 23, and thus, sidewalls of the through holes may be formed without steps, unlike those of the through holes 33h1 and 33h2.

[0125] Referring to FIG. 11A, FIG. 11B, FIG. 11C, and FIG. 11D, an isolation trench is formed to define a region of the light emitting device 100 by an isolation process. The isolation trench may expose the third substrate 41 along peripheries of the first to third LED stacks 23, 33, and 43. Between regions of the light emitting device, the isolation trench may be formed by sequentially removing the first LED stack 23, the first transparent electrode 25, the second bonding layer 59, the lower insulation layer 51, the second LED stack 33, the first bonding layer 49, and the third LED stack 43. The second transparent electrode 35 and the third transparent electrode 45 are not exposed during the isolation process, and thus, the second transparent electrode 35 and the third transparent electrode 45 may not be damaged by etching gas. When the second and third transparent electrodes 35 and 45 are formed of ZnO, ZnO may be easily damaged by etching gas. However, according to the illustrated exemplary embodiment, the second transparent electrode 35 and the third transparent electrode 45 may be prevented from being exposed to an etching gas by forming the second and third transparent electrodes 35 and 45 to be recessed inwardly.

[0126] In the illustrated exemplary embodiment, the first to third LED stacks 23, 33, and 43 are described as being sequentially patterned through the isolation process, but the inventive concepts are not limited thereto. For example, in some exemplary embodiments, the third LED stack 43 may be removed in advance in a region where the isolation trench will be formed before bonding the second LED stack 33, or the second LED stack 33 may be removed in advance in the region in which the isolation trench will be formed before bonding the first LED stack 23. In this case, the region where the third LED stack 43 is removed may be filled with the first bonding layer 49, and the region where the second LED stack 33 is removed may be filled with the second bonding layer 59. Accordingly, the second and third LED stacks 33 and 43 may not be exposed in the isolation process.

[0127] Referring to FIG. 12A, FIG. 12B, FIG. 12C, and FIG. 12D, an intermediate insulation layer 61 is formed on the first LED stack 23. The intermediate insulation layer 61 may cover side surfaces of the first to third LED stacks 23, 33, and 43, side surfaces of the first and second bonding layers 49 and 59, a side surface of the transparent electrode 25, and a side surface of the lower insulation layer 51 exposed through the isolation trench.

[0128] The intermediate insulation layer 61 may also cover sidewalls of the through holes 23h1, 23h2, 23h3, and 23h4. However, the intermediate insulation layer 61 is patterned to have openings 61a exposing bottoms of the through holes 23h1, 23h2, 23h3, and 23h4, and an opening 61b exposing the first conductivity type semiconductor layer 23a of the first LED stack 23. The openings 61a expose the first transparent electrode 25, the upper p-electrode pad 53g, the lower p-connector 53b, and the lower common connector 53c in the through holes 23h1, 23h2, 23h3, and 23h4.

[0129] First to third upper connectors 63r, 63g, and 63b, and an upper common connector 63c are formed on the intermediate insulation layer 61. The first upper connector 63r is connected to the first transparent electrode 25, the second upper connector 63g is connected to the upper p-electrode pad 53g, and the third upper connector 63b is connected to the lower p-connector 53b.

The upper common connector 63c may be connected to the lower common connector 53c.

[0130] Referring to FIG. 13A, FIG. 13B, FIG. 13C, and FIG. 13D, an upper insulation layer 71 is formed to cover the intermediate insulation layer 61 and the connectors 63r, 63g, 63b, and 63c. The upper insulation layer 71 may also cover the intermediate insulation layer 61 on the side surfaces of the first to third LED stacks 23, 33, and 43. However, the upper insulation layer 71 may be patterned to have openings 71a exposing the first to third upper connectors 63r, 63g, and 63b, and the upper common connector 63c.

[0131] Subsequently, bump pads 73r, 73g, 73b, and 73c are formed in the openings 71a, respectively. The first bump pad 73r is disposed on the first upper connector 63r, the second bump pad 73g is disposed on the second upper connector 63g, and the third bump pad 73b is disposed on the third upper connector 63b. The common bump pad 73c is disposed on the upper common connector 63c.

[0132] Then, the light emitting device 100 is bonded onto a circuit board 101 (see FIG. 14), and the third substrate 41 may be separated to from the light emitting device 100. A schematic cross-sectional view of the light emitting device 100 bonded to the circuit board 101 is exemplarily shown in FIG. 14.

[0133] Although FIG. 14 exemplarily illustrates a single light emitting device 100 disposed on the circuit board 101, however, a plurality of light emitting devices 100 may be mounted on the circuit board 101. Each of the light emitting devices 100 may form one pixel capable of emitting any one of blue light, green light, and red light, and a plurality of pixels are arranged on the circuit board 101 to provide a display panel.

[0134] The plurality of light emitting devices 100 may be formed on the substrate 41, and the light emitting devices 100 may be transferred onto the circuit board 101 in a group, not individually. FIG. 15A, FIG. 15B, and FIG. 15C are schematic cross-sectional views illustrating a method of transferring the light emitting device to the circuit board according to an exemplary embodiment. Hereinafter, a method of transferring the light emitting devices 100 formed on the substrate 41 to the circuit board 101 in a group will be described.

[0135] Referring to FIG. 15A, as described above, when the process of FIG. 13A, FIG. 13B, of FIG. 13C, and FIG. 13D are completed, the plurality of light emitting devices 100 are isolated from each other, and are arranged on the substrate 41 by the isolation trench.

[0136] Meanwhile, the circuit board 101 having pads on an upper surface thereof is provided. The pads are arranged on the circuit board 101 to correspond to locations where the pixels for a display are to be arranged. In general, an interval between the light emitting devices 100 arranged on the substrate 41 may be more dense than that of the pixels on the circuit board 101.

[0137] Referring to FIG. 15B, bump pads of the light emitting devices 100 are selectively bonded to the pads on the circuit board 101. The bump pads and the pads may be bonded using In bonding, for example. In this case, the light emitting devices 100 located between pixel regions may be spaced apart from the circuit board 101, since these light emitting devices 100 do not have pads of the circuit board 101 to be boned to.

[0138] Subsequently, a mask 201 is disposed on the substrate 41 and is irradiated with a laser. A light transmitting region of the mask 201 is disposed to correspond to the light emitting devices 100 bonded to the circuit board 101, and thus, the light emitting devices 100 bonded to the pads of the circuit board 101 are selectively irradiated with the laser. Thereafter, the light emitting devices 100 are transferred to the circuit board 101 by separating the light emitting devices 100 irradiated with the laser from the substrate 41. Accordingly, the display panel in which the light emitting devices 100 are arranged on the circuit board 101 is provided. The display panel may be mounted on various display apparatuses as described with reference to FIG. 1.

[0139] Although some embodiments have been described herein, it should be understood that these embodiments are provided for illustration only and are not to be construed in any way as limiting the present disclosure. It should be understood that features or components of one embodiment can also be applied to other embodiments without departing from the spirit and scope of the present disclosure.

[0140] The invention provides, in particular, the following:

1. A light emitting device for a display, comprising:

a first LED stack;
a second LED stack disposed under the first LED stack;
a third LED stack disposed under the second LED stack;
a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack;
a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack;
a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack;
an n electrode pad disposed on a first conductivity type semiconductor layer of the third LED stack;
a lower p electrode pad disposed on the third transparent electrode; and
bump pads disposed on the first LED stack,
wherein each of the first to third LED stacks includes a first conductivity type semiconductor

layer, an active layer and a second conductivity type semiconductor layer,
wherein the bump pads include first to third bump pads and common bump pads,
wherein the common bump pad is commonly electrically connected to the first to third LED stacks,
wherein the first to third bump pads are electrically connected to the first to third LED stacks, respectively, and
wherein an upper surface of the n electrode pad is located at the same elevation as that of the lower p electrode pad.

2. The light emitting device for a display of item 1, wherein the first, second and third LED stacks emit red light, green light and blue light, respectively.
3. The light emitting device for a display of item 1,

wherein the first to third LED stacks are independently driven,
wherein light generated from the first LED stack is emitted outside passing through the second LED stack and the third LED stack, and
light generated from the second LED stack is emitted outside passing through the third LED stack.

4. The light emitting device for a display of item 1, wherein any one of the first to third transparent electrodes is formed of a material different from the remaining transparent electrodes.
5. The light emitting device for a display of item 4, wherein the first transparent electrode is formed of ITO, and the second and third transparent electrodes are formed of ZnO.
6. The light emitting device for a display of item 5,

wherein each of the first to third transparent electrodes contacts the second conductivity type semiconductor layer, and
wherein the second and third transparent electrodes are recessed to have a smaller area than that of the second conductivity type semiconductor layer of the second LED stack and that of the second conductivity type semiconductor layer of the third LED stack, respectively.

7. The light emitting device for a display of item 6,

wherein the common bump pad is commonly electrically connected to first conductivity type semiconductor layers of the first to third LED stacks,
wherein the first to third bump pads are electrically connected to second conductivity type semiconductor layers of first to third LED stacks, respectively.

8. The light emitting device for a display of item 6, further comprising:
an insulation layer covering side surfaces of the first to third LED stacks,
wherein the side surfaces of the first to third LED stacks and a side surface of the first transparent electrode are in contact with the insulation layer, and side surfaces of the second and third transparent electrodes are spaced apart from the insulation layer.
9. The light emitting device for a display of item 1, wherein side surfaces of the light emitting device are inclined at a range of 75 degrees to 90 degrees with respect to the upper surface of the third LED stack.
10. The light emitting device for a display of item 1, further comprising:

a first bonding layer interposed between the second LED stack and the third LED stack; and
a second bonding layer interposed between the first LED stack and the second LED stack.

11. The light emitting device for a display of item 10, further comprising:

lower through holes passing through the second LED stack and the first bonding layer to expose the n electrode pad and the lower p electrode pad, respectively;
a lower common connector connected to the n electrode pad; and
a lower p connector connected to the lower p electrode pad,
wherein the lower common connector is electrically connected to the first conductivity type semiconductor layer of the LED stack, and connected to the n electrode pad exposed through the lower through hole, and
wherein the lower p connector is electrically connected to the lower p electrode pad exposed through the lower through hole.

12. The light emitting device for a display of item 11, further comprising:
an upper p electrode pad disposed on the second transparent electrode and electrically connected to the second conductivity type semiconductor layer of the second LED stack.
13. The light emitting device for a display of item 12, further comprising:

a through hole passing through the first LED stack to expose the first transparent electrode;
through holes passing through the first LED stack, the first transparent electrode and the second bonding layer to expose the upper p electrode pad, the lower p connector, and the lower common connector, respectively; and
first to third upper connectors and an upper com-

mon connector disposed on the first LED stack, and electrically connected to the first transparent electrode, the upper p electrode pad, the lower p connector, and the lower common connector through through holes passing through the first LED stack,
wherein the bump pads are disposed on the first to third upper connectors and the upper common connector, respectively.

14. The light emitting device for a display of item 13, wherein the bump pads are located on flat portions of the first to third upper connectors and the upper common connector, respectively.

15. The light emitting device for a display of item 14, further comprising:

an upper insulation layer covering the first to third upper connectors and the upper common connector,
wherein the upper insulation layer has openings exposing the first to third upper connectors and the upper common connector, and
wherein each of the bump pads is disposed in the openings.

16. The light emitting device for a display of item 15, further comprising:

an intermediate insulation layer disposed between the first LED stack and the upper connectors,
wherein the intermediate insulation layer covers a side surface of the light emitting device and a sidewall of the through hole passing through the first LED stack, and includes openings exposing the first transparent electrode, the upper p electrode pad, the lower p connector, and the lower common connector.

17. The light emitting device for a display of item 1, wherein the first to third LED stacks are isolated from a growth substrate.

18. A light emitting device for a display, comprising:

a first LED stack;
a second LED stack disposed under the first LED stack;
a third LED stack disposed under the second LED stack;
a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack;
a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack;
a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack;
bump pads disposed on the first LED stack,
wherein each of the first to third LED stacks includes a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer, and
wherein at least one of the first to third transparent electrodes is recessed from an edge of the second conductivity type semiconductor layer of the first to third LED stacks.

19. The light emitting device for a display of item 18, further comprising:

an n electrode pad disposed on the first conductivity type semiconductor layer of the third LED stack;
a lower p electrode pad disposed on the third transparent electrode,
wherein an upper surface of the n electrode pad is located at the same elevation as that of the lower p electrode pad.

20. A display apparatus comprising:

a circuit board; and
a plurality of light emitting devices arranged on the circuit board, each of the light emitting devices comprising:

a first LED stack;
a second LED stack disposed under the first LED stack;
a third LED stack disposed under the second LED stack;
a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack;
a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack;
a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack;
an n electrode pad disposed on a first conductivity type semiconductor layer of the third LED stack;
a lower p electrode pad disposed on the third transparent electrode; and
bump pads disposed on the first LED stack; and
wherein each of the first to third LED stacks

includes a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer,
wherein the bump pads include first to third bump pads and common bump pads,
wherein the common bump pad is commonly electrically connected to the first to third LED stacks,
wherein the first to third bump pads are electrically connected to the first to third LED stacks, respectively,
wherein an upper surface of the n electrode pad is located at the same elevation as that of the lower p electrode pad, and
wherein the bump pads are bonded to the circuit board.

21. A display apparatus comprising:

a circuit board; and
a plurality of light emitting devices arranged on the circuit board, each of the light emitting devices comprising:

a first LED stack;
a second LED stack disposed under the first LED stack;
a third LED stack disposed under the second LED stack;
a first transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with a lower surface of the first LED stack;
a second transparent electrode interposed between the first LED stack and the second LED stack, and being in ohmic contact with an upper surface of the second LED stack;
a third transparent electrode interposed between the second LED stack and the third LED stack, and being in ohmic contact with an upper surface of the third LED stack;
bump pads disposed on the first LED stack; and
wherein each of the first to third LED stacks includes a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer,
wherein at least one of the first to third transparent electrodes is recessed from an edge of the second conductivity type semiconductor layer of the first to third LED stacks, and
wherein the bump pads are bonded to the circuit board.

Claims

1. A light emitting device comprising:

a first LED stack including a first conductivity type semiconductor layer, and active layer and a second conductivity type semiconductor layer;
a second LED stack disposed under the first LED stack and including a first conductivity type semiconductor layer, and active layer and a second conductivity type semiconductor layer;
a third LED stack disposed under the second LED stack and including a first conductivity type semiconductor layer, and active layer and a second conductivity type semiconductor layer;
a first transparent electrode disposed on the second conductivity type semiconductor layer of the first LED stack, and being in ohmic contact with the second conductivity type semiconductor layer of the first LED stack;
a second transparent electrode disposed on the second conductivity type semiconductor layer of the second LED stack, and being in ohmic contact with the second conductivity type semiconductor layer of the second LED stack;
a third transparent electrode disposed on the second conductivity type semiconductor layer of the third LED stack, and being in ohmic contact with the second conductivity type semiconductor layer of the third LED stack;
bump pads disposed on the first LED stack; and
a lower insulation layer disposed between the first LED stack and the second LED stack,
wherein a side surface of the second transparent electrode is recessed inwardly than that of the second LED stack, and
wherein the lower insulation covers an outer side surface of the second transparent electrode.

2. The light emitting device of claim 1, wherein a side surface of the third transparent electrode is recessed inwardly from that of the third LED stack.

3. The light emitting device of claim 1, further comprising a first bonding layer disposed between the second LED stack and the third LED stack.

4. The light emitting device of claim 3, wherein the first bonding layer covers an outer side of the third transparent electrode.

5. The light emitting device of claim 1, wherein the first to third LED stacks are independently driven, wherein light generated from the first LED stack is emitted outside passing through the second LED stack and the third LED stack, and light generated from the second LED stack is emitted outside passing through the third LED stack.

6. The light emitting device of claim 1, wherein the bump pads comprisie a common bump pad which is electrically connected to first conductivity type semiconductor layers of the first to third LED stacks.

7. The light emitting device of claim 6, the bump pads further comprising a first to third bump pads are electrically connected to second conductivity type semiconductor layers of first to third LED stacks, respectively.

8. The light emitting device of claim1, further comprising:

an insulation layer covering side surfaces of the first to third LED stacks,
wherein the side surface of the first to third LED stacks and a side surface of the first transparent electrode are on contact with the insulation layer, and
side surfaces of the second and third transparent electrodes are space apart from the insulation layer.

9. The light emitting device of claim 1, wherein side surfaces of the light emitting device are inclined at a range of 75 degrees to 90 degrees with respect to the upper surface of the third LED stack.

10. The light emitting device of claim 1, wherein the first, second, and third LED stacks are isolated from a growth substrate.

11. The light emitting device of claim 1, wherein any one of the first to third transparent electrodes is formed of a material different from the remaining transparent electrode.

12. The light emitting device of claim1, wherein the second LED stack includes a mesa etching region, in which a portion of the second conductivity type semiconductor layer is removed to expose an upper surface of the first conductivity type semiconductor layer.

13. The light emitting device of claim 12, wherein the third LED stack includes a mesa etching region, in which a portion of the second conductivity type semiconductor layer is removed to expose an upper surface of the first conductivity type semiconductor layer.

14. The light emitting device of claim 13, wherein a mesa etching region of the second LED stack is partially overlapped with that of the third LED stack.

15. The light emitting device of claim 14, wherein a portion of the mesa etching region of the second LED stack is disposed on the mesa region of the third LED stack.

FIG. 1

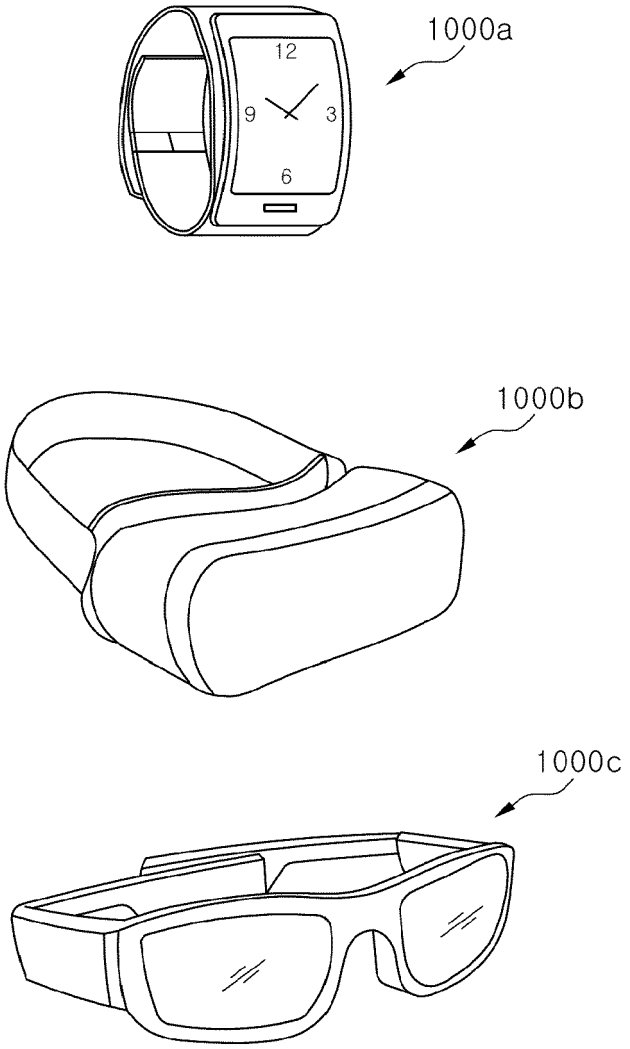

FIG. 2

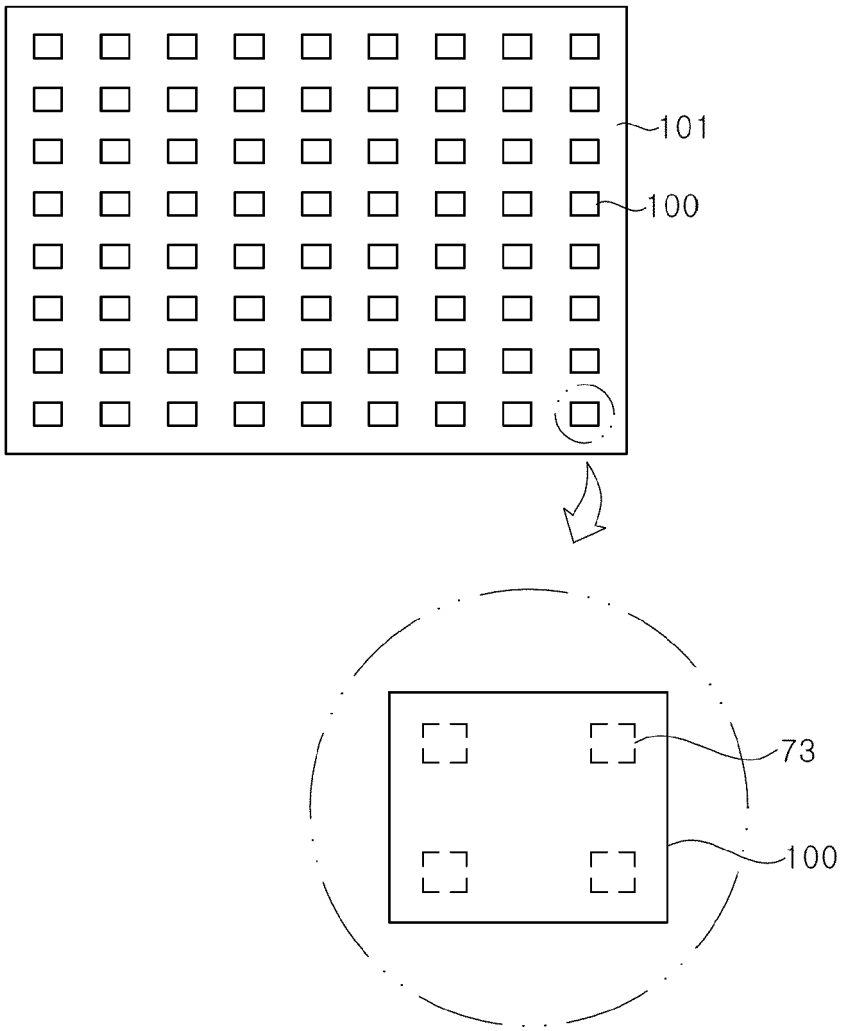

FIG. 3A

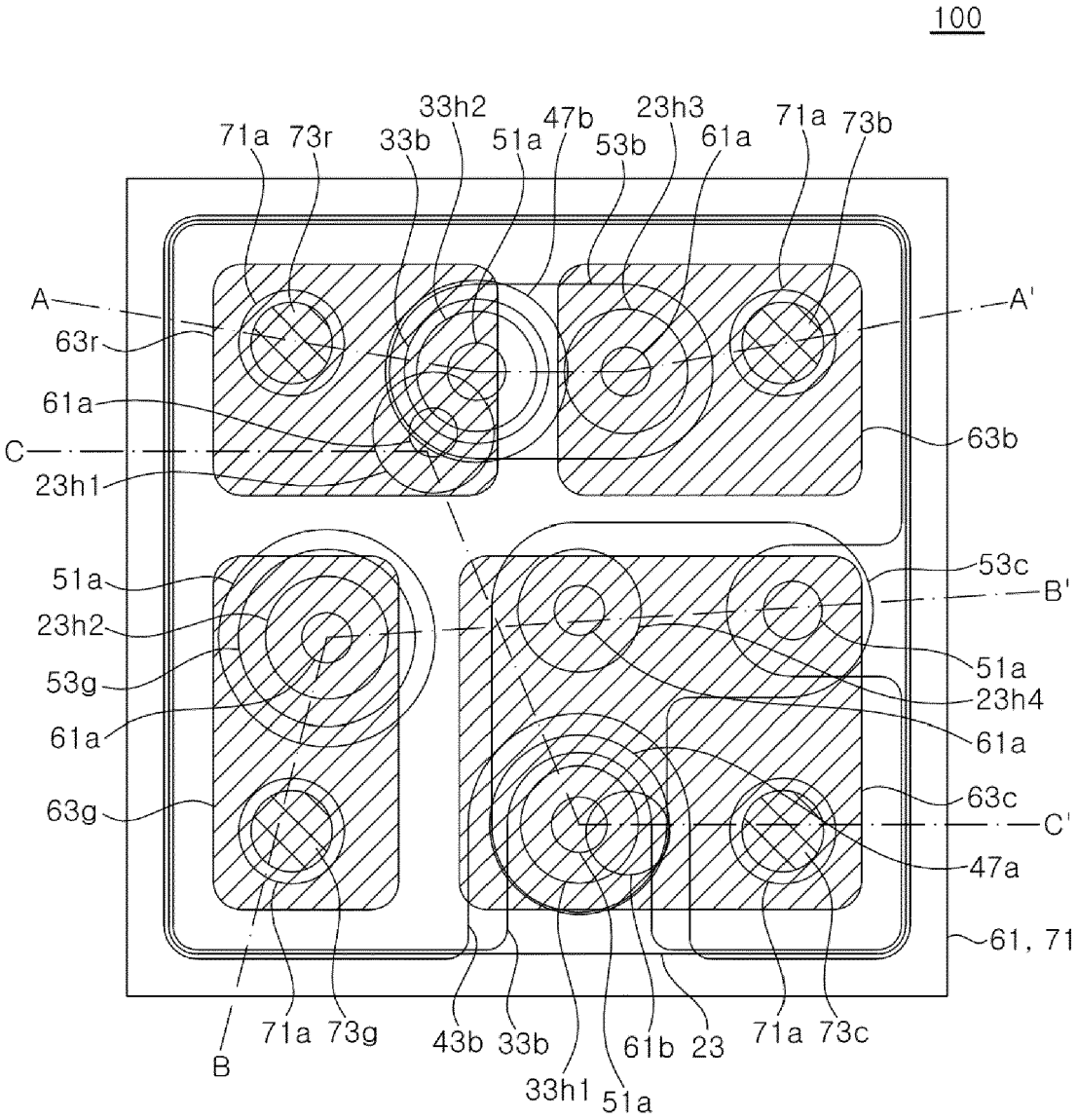
100
71a
73r
33h2
33b
51a
47b
53b
23h3
61a
71a
73b
A
A'
63r
61a
C
23h1
63b
51a
23h2
53g
61a
63g
53c
B'
51a
23h4
61a
63c
C'
47a
61, 71
B
71a
73g
43b
33b
33h1
51a
61b
23
71a
73c

FIG. 3B

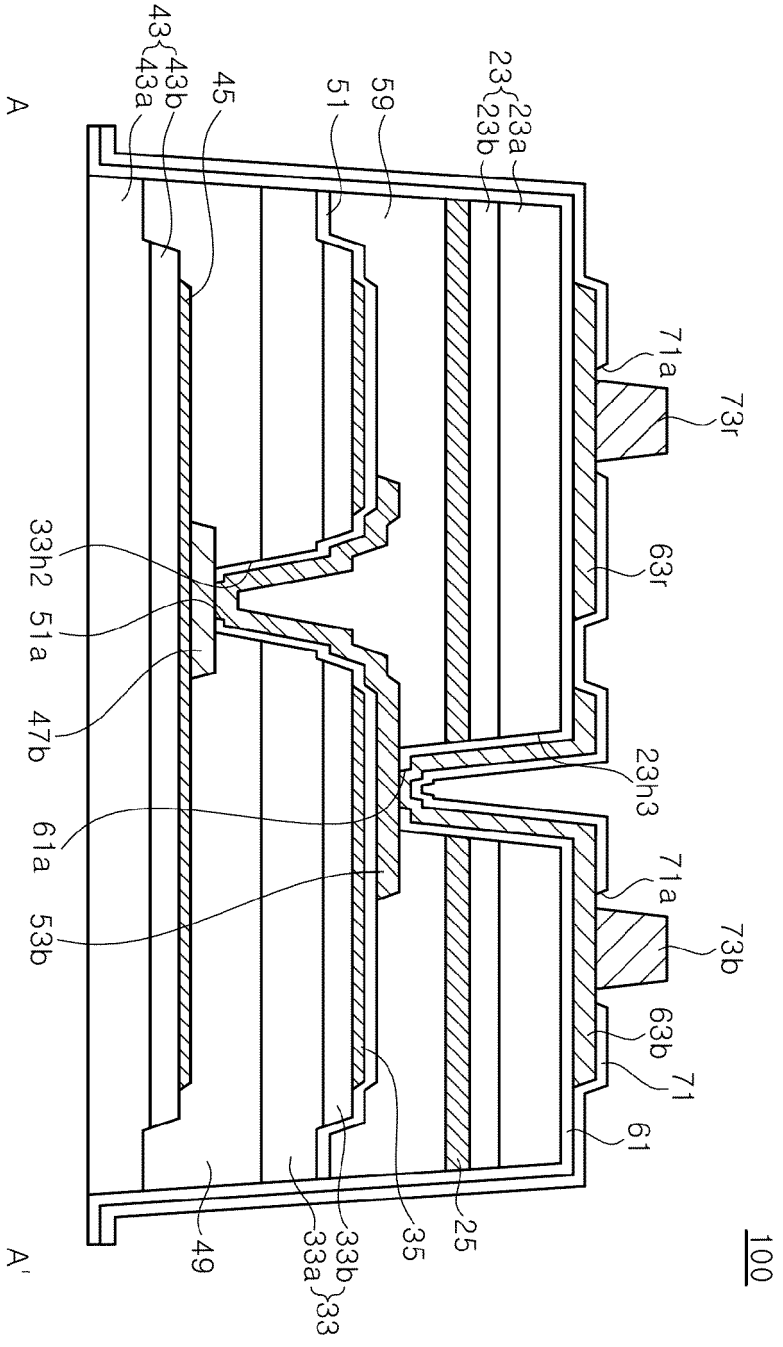
A
A'
43
43b
43a
45
51
59
23
23a
23b
71a
73r
63r
33h2
51a
47b
23h3
61a
53b
71a
73b
63b
71
61
49
33b
33a
33
35
25
100

FIG. 3C

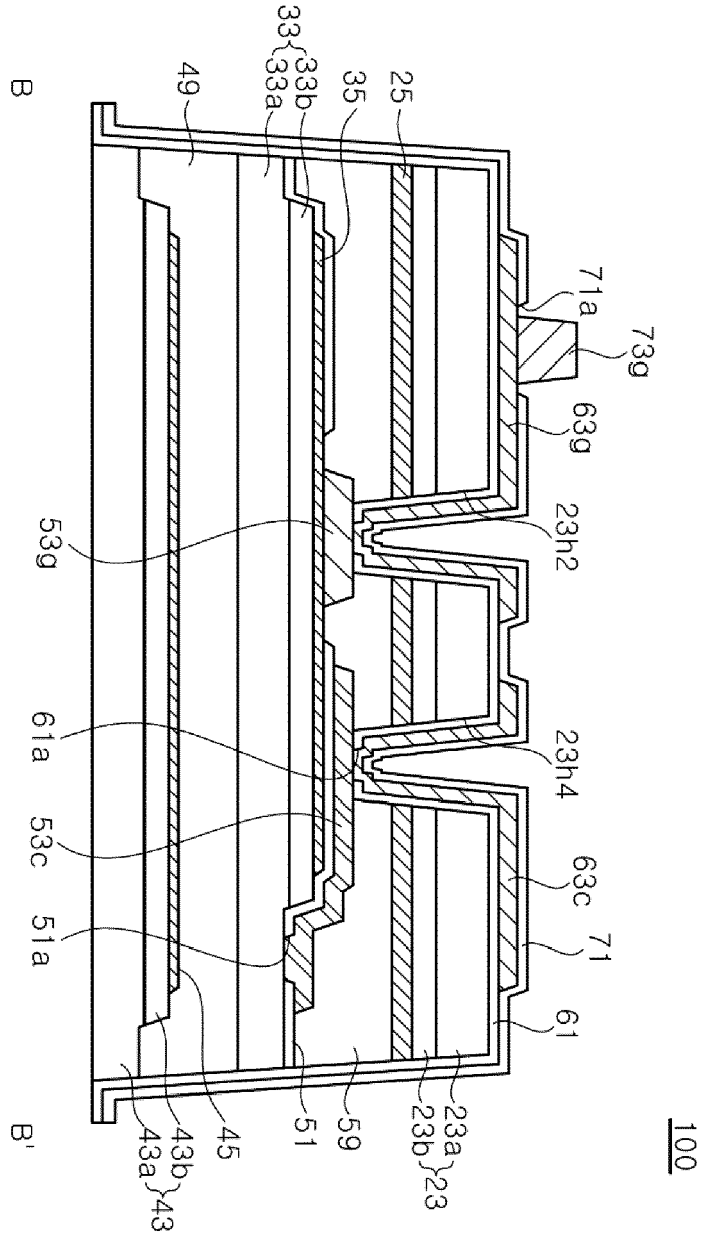
B
B'
33
33b
33a
49
35
25
71a
73g
63g
23h2
53g
61a
23h4
53c
63c
71
51a
61
45
51
59
23a
23b
23
43b
43a
43
100

FIG. 3D

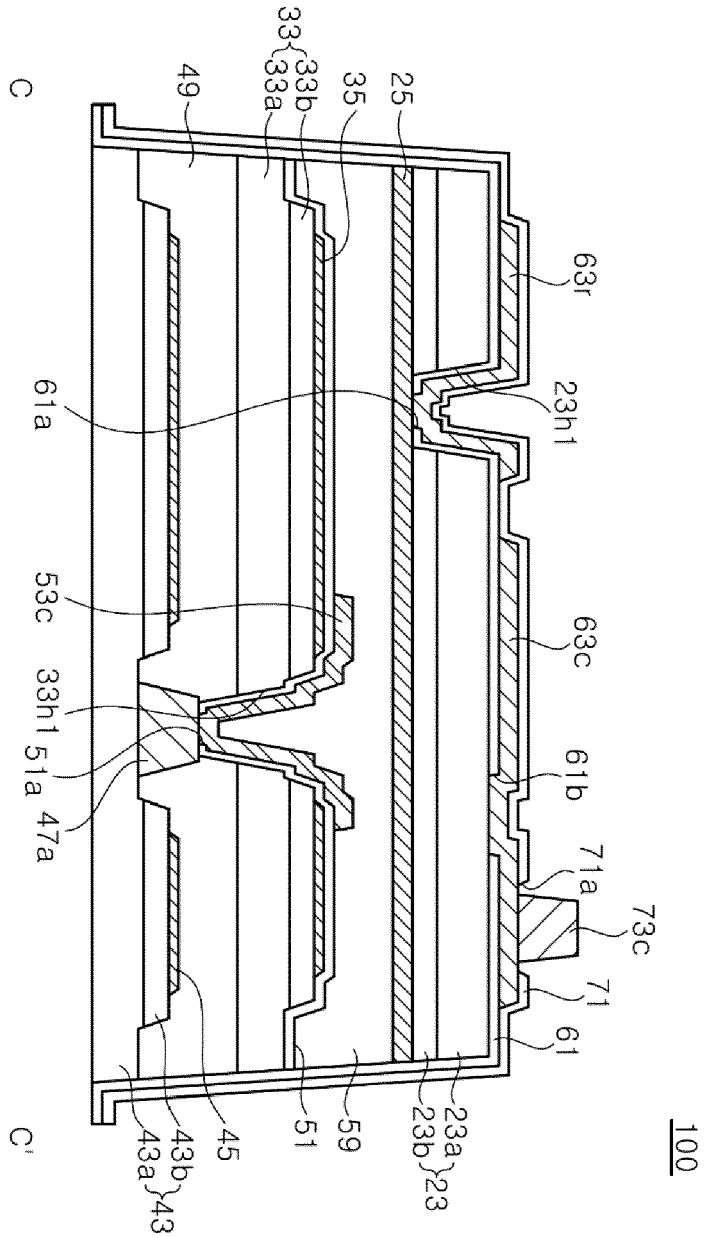
C
C'
49
33
33a
33b
35
25
63r
23h1
61a
53c
63c
33h1
51a
47a
61b
71a
73c
71
61
45
51
59
23a
23b
23
43b
43a
43
100

FIG. 4A

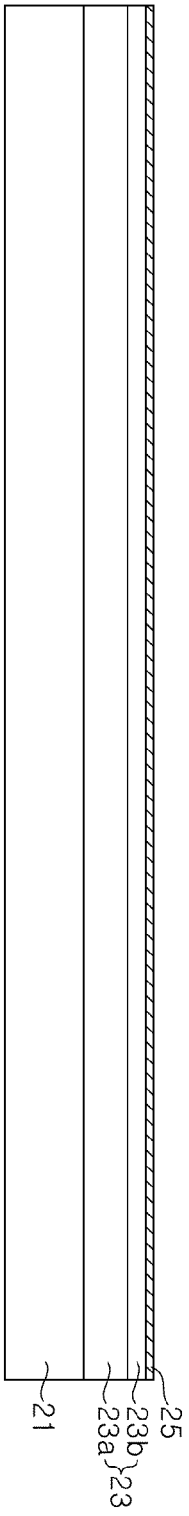

FIG. 4B

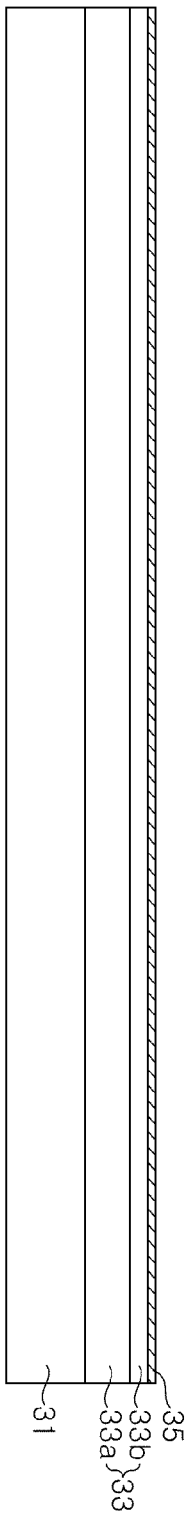

FIG. 4C

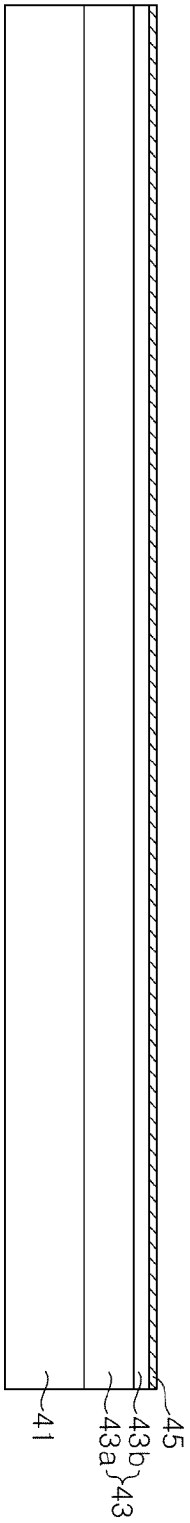

FIG. 5A

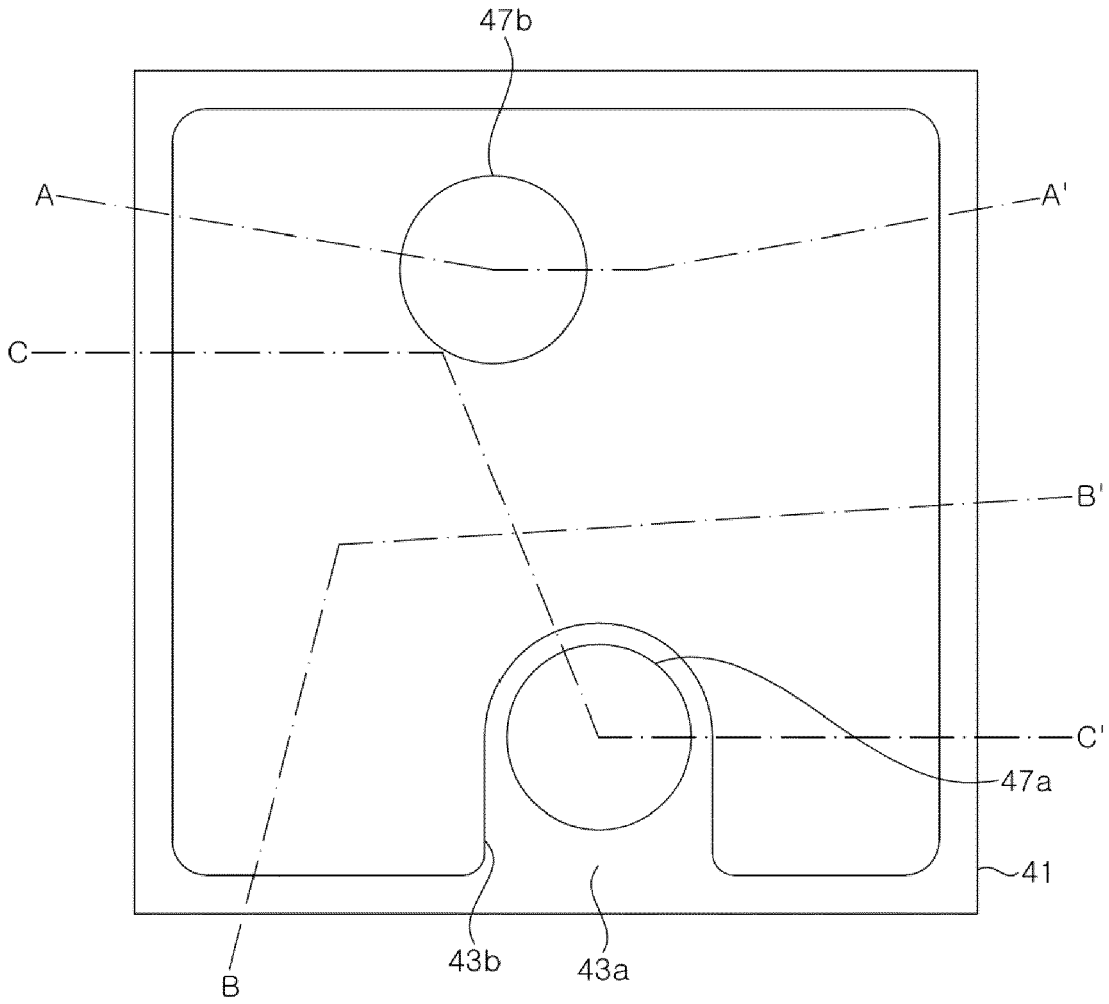

FIG. 5B

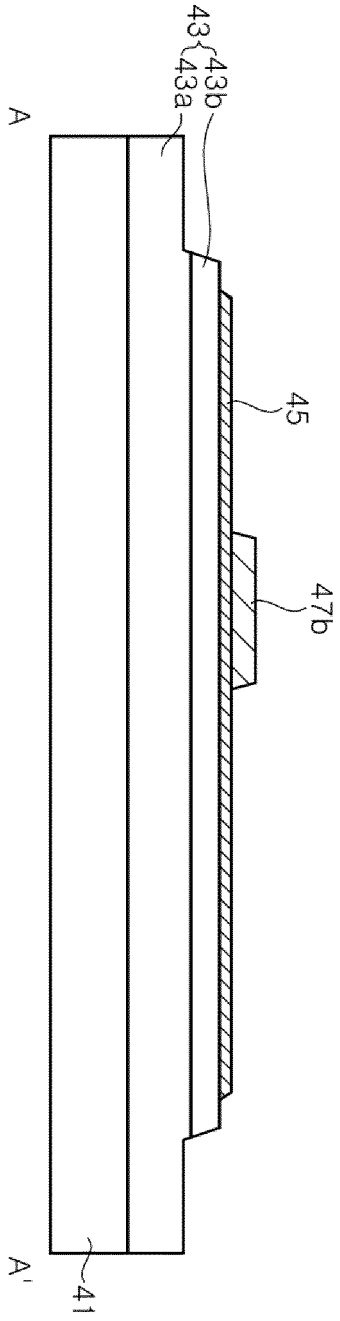

FIG. 5C

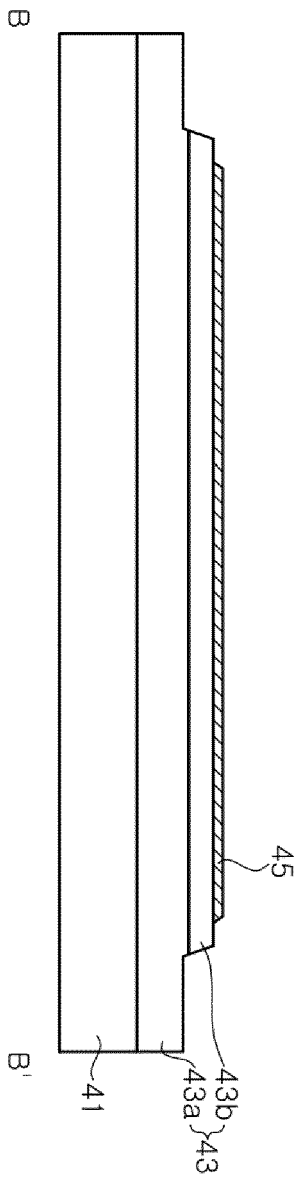

FIG. 5D

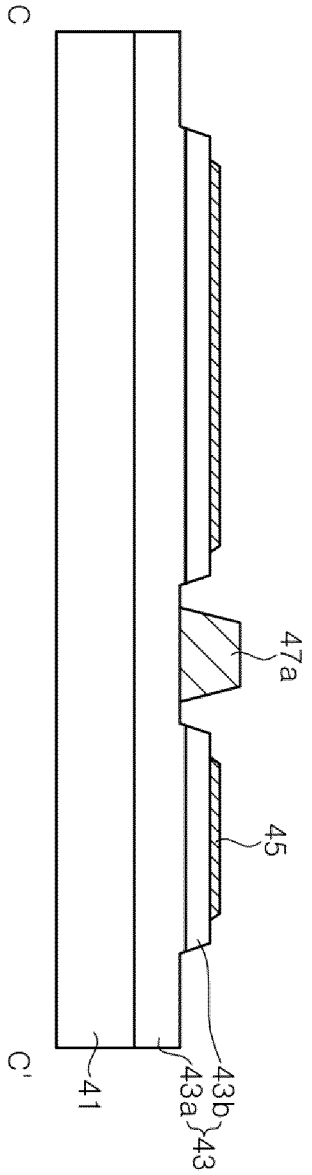

FIG. 6A

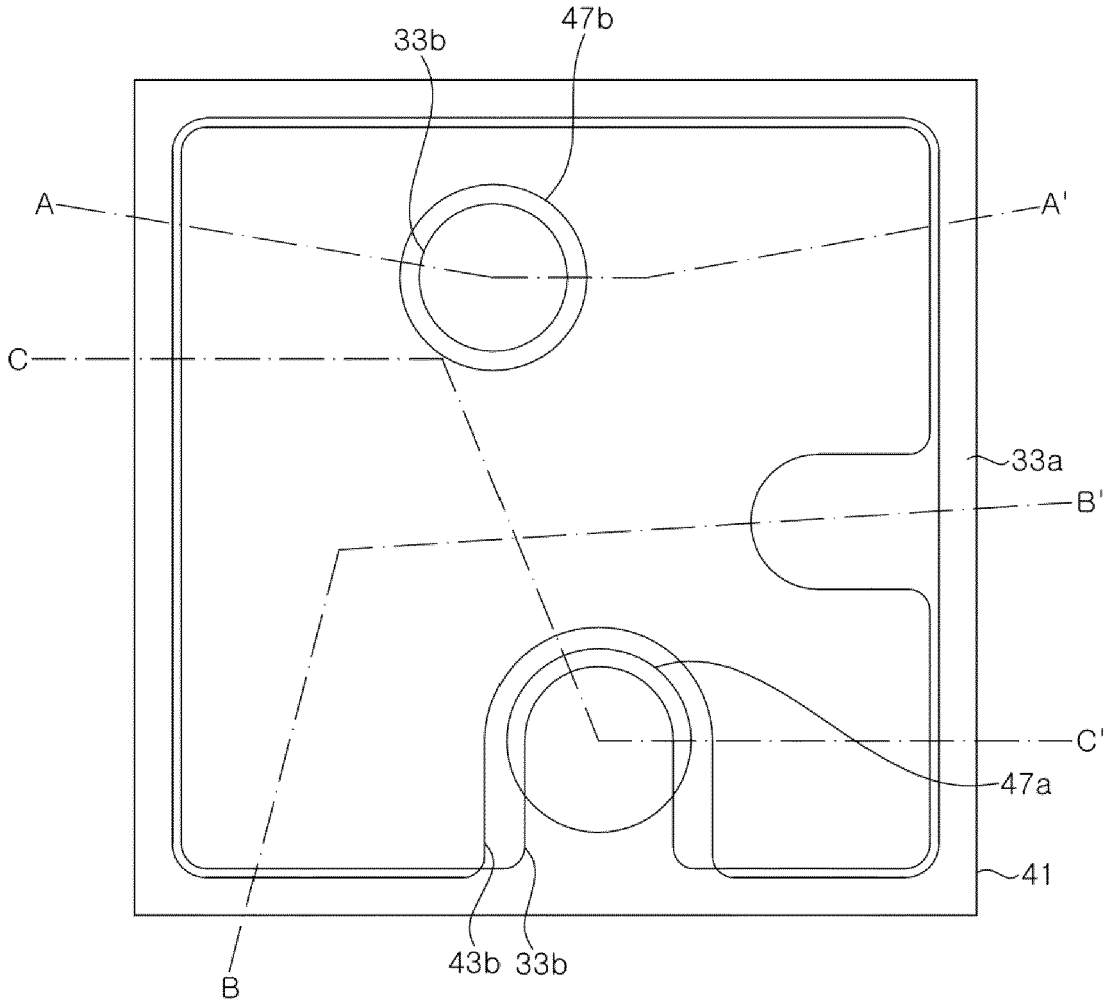

FIG. 6B

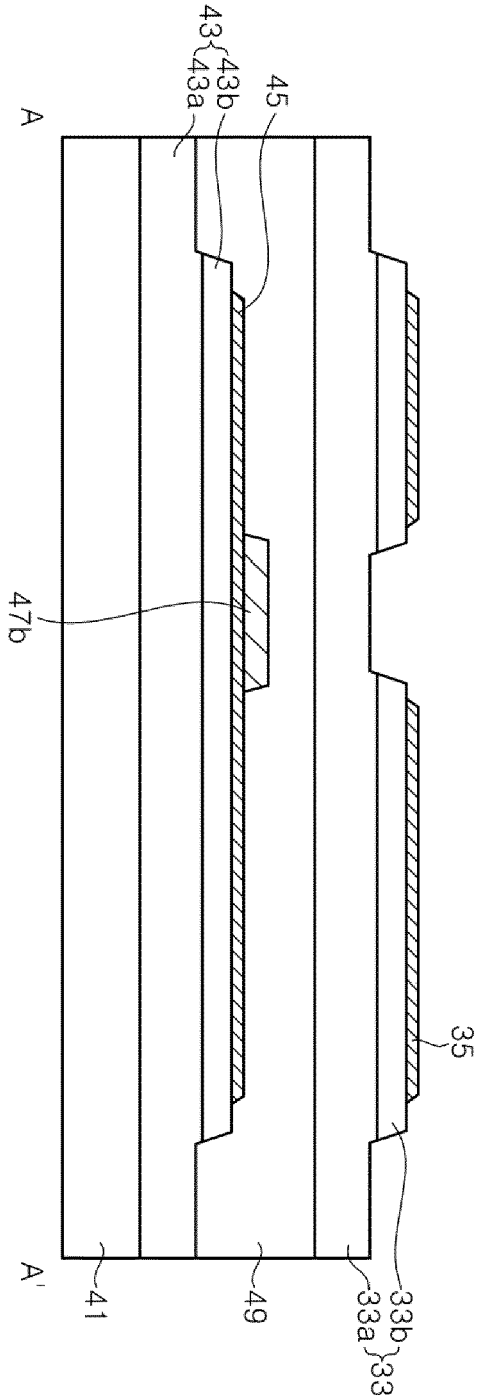

FIG. 6C

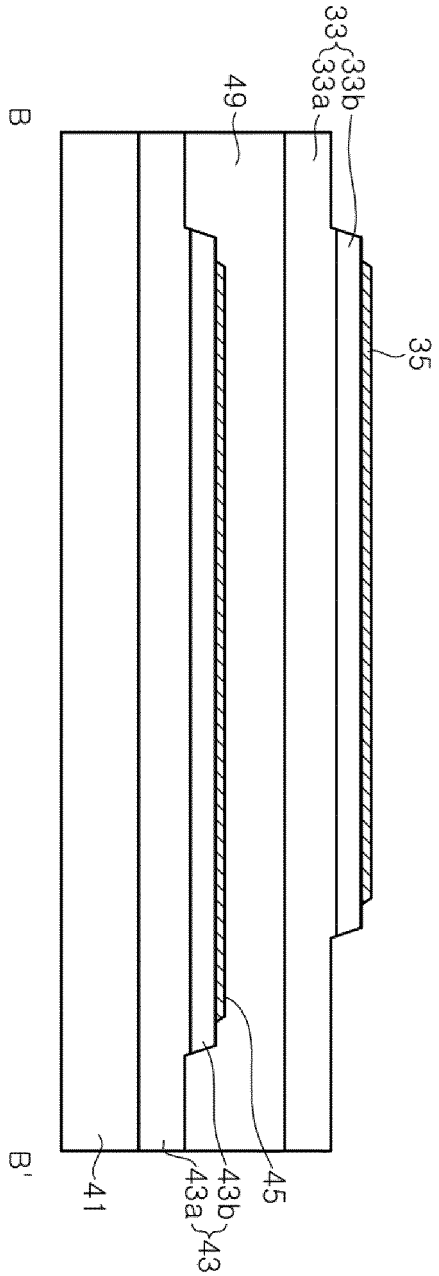

FIG. 6D

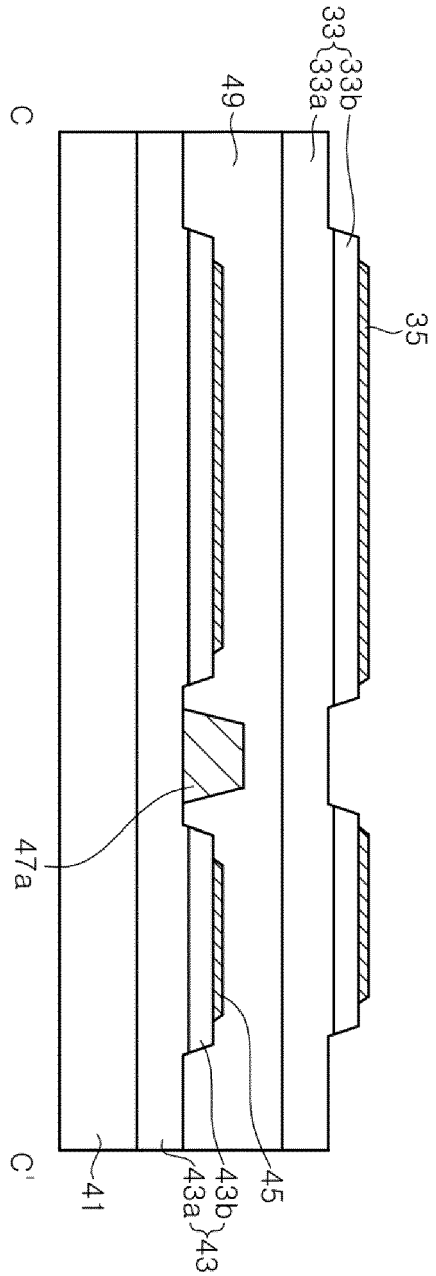

FIG. 7A

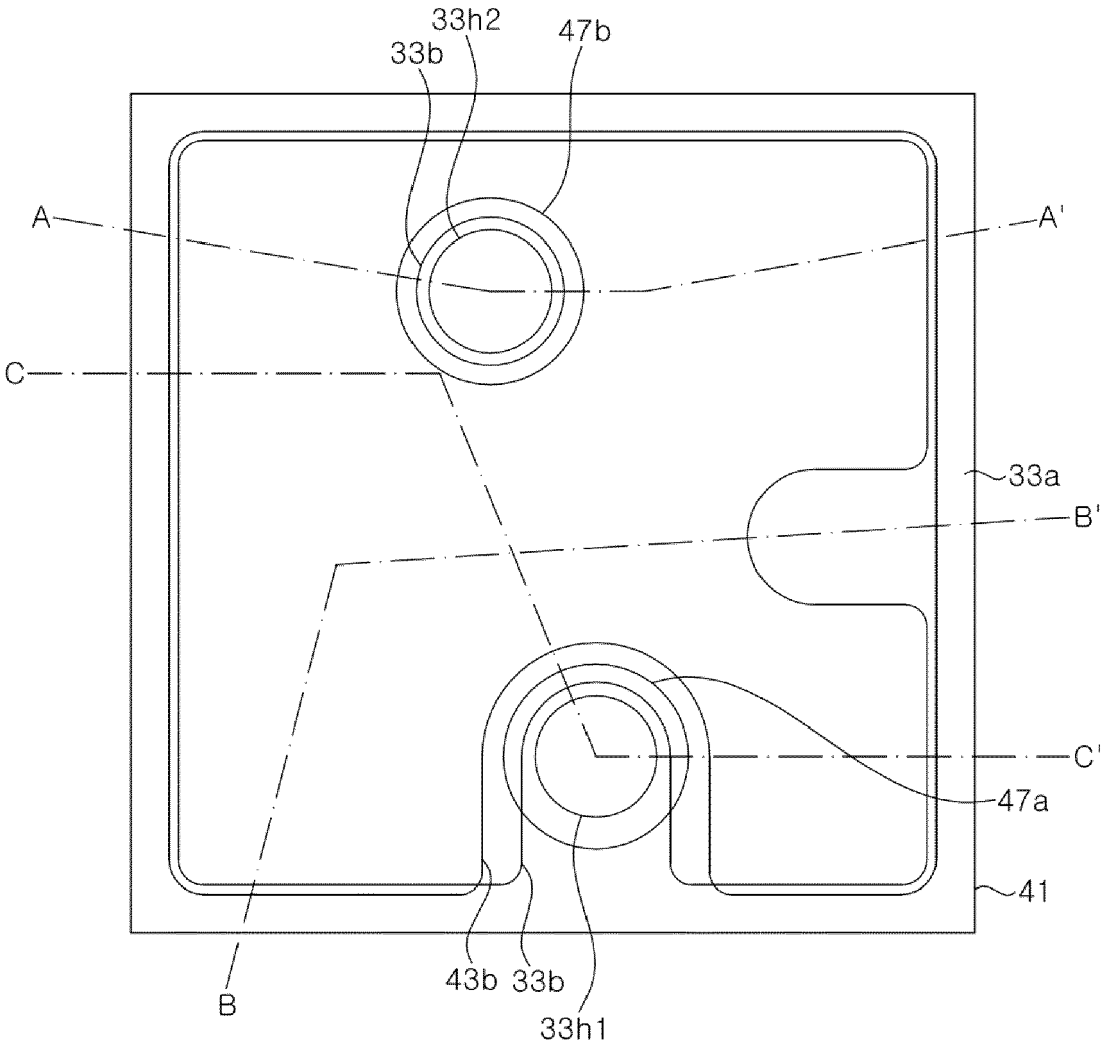

FIG. 7B

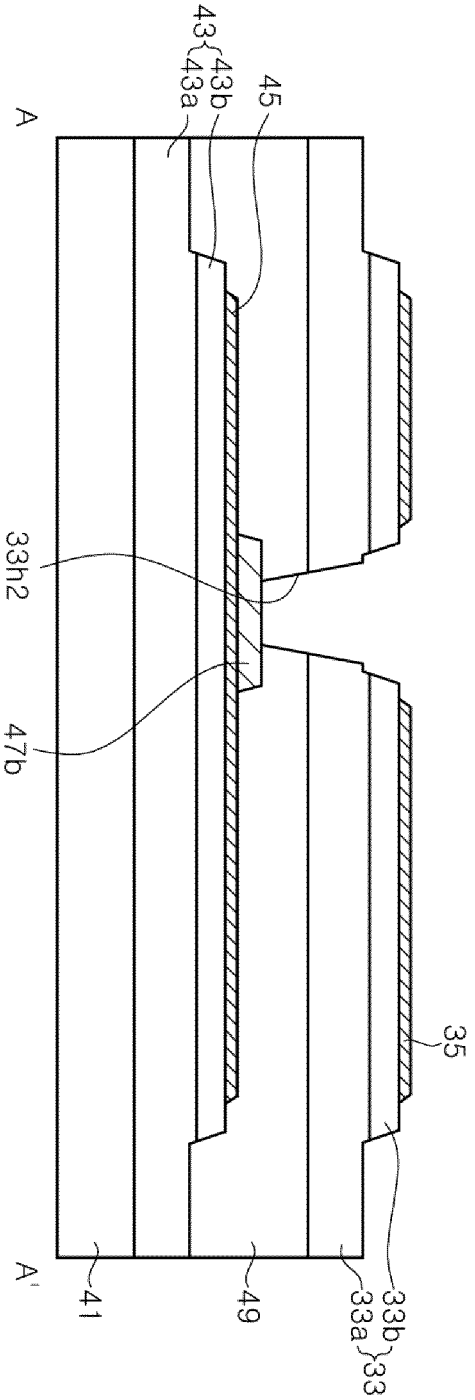

FIG. 7C

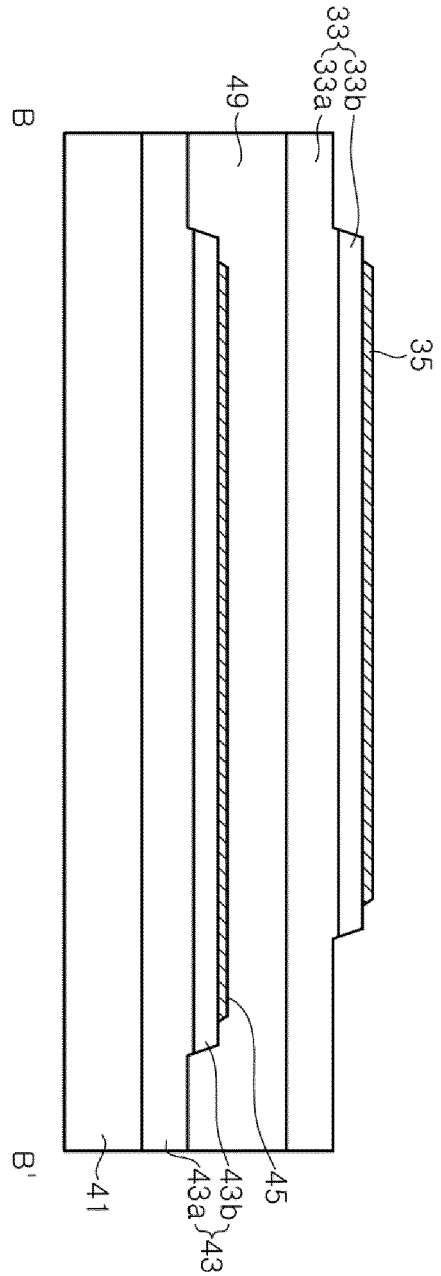

FIG. 7D

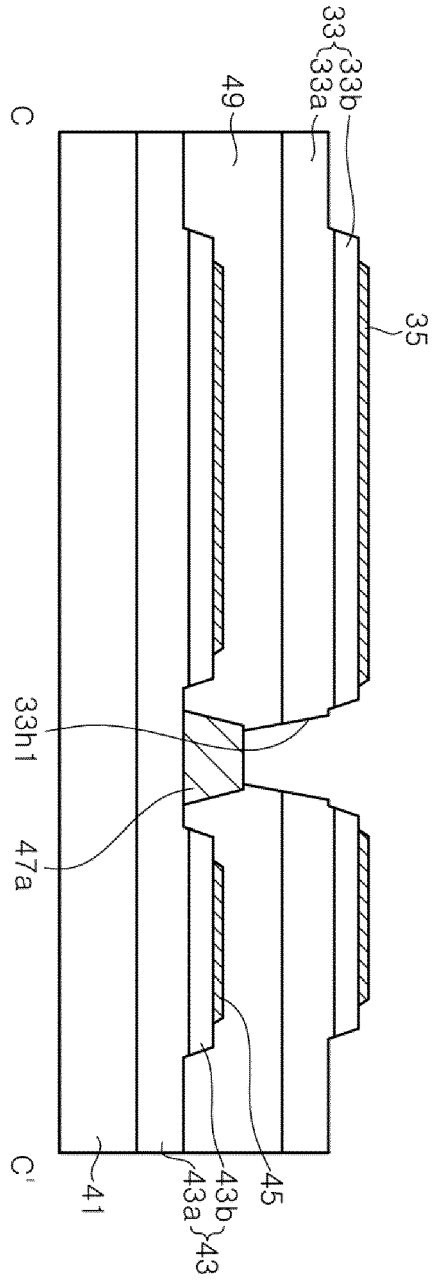

FIG. 8A

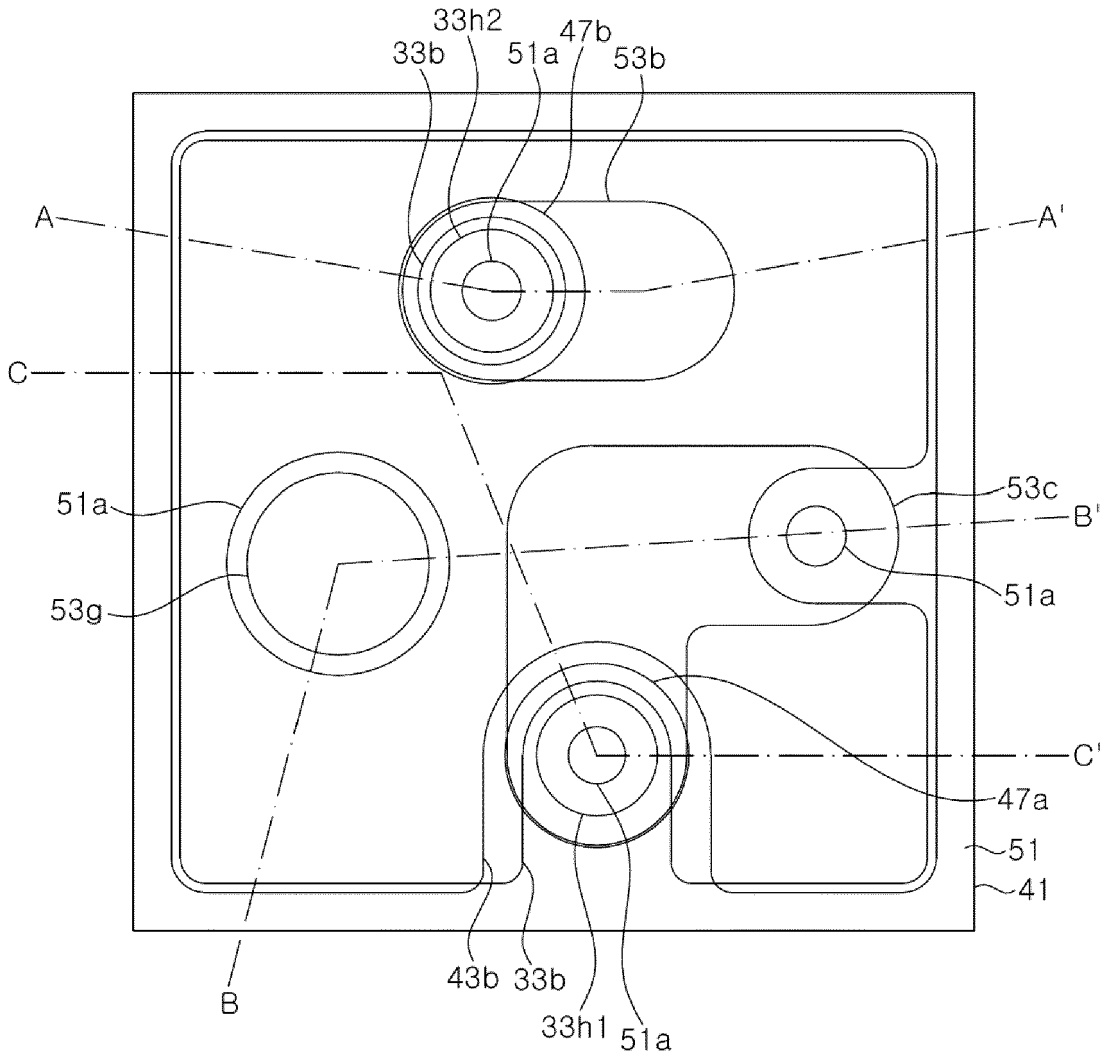
33h2
33b
51a
47b
53b
A
A'
C
51a
53c
B'
53g
51a
C'
47a
51
41
43b
33b
B
33h1
51a

FIG. 8B

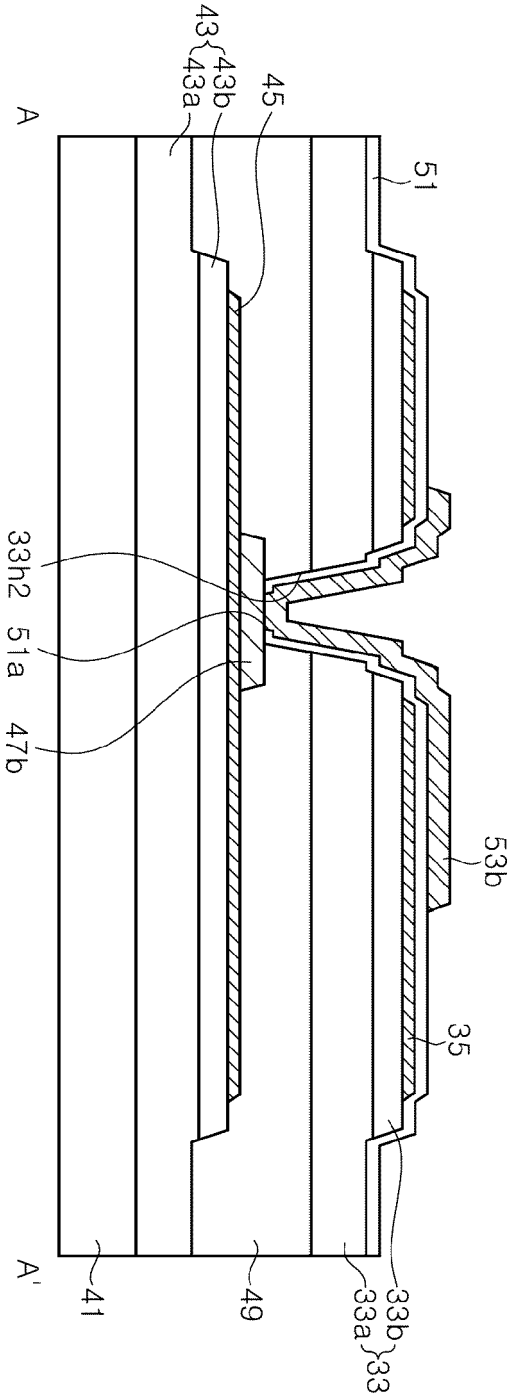

FIG. 8C

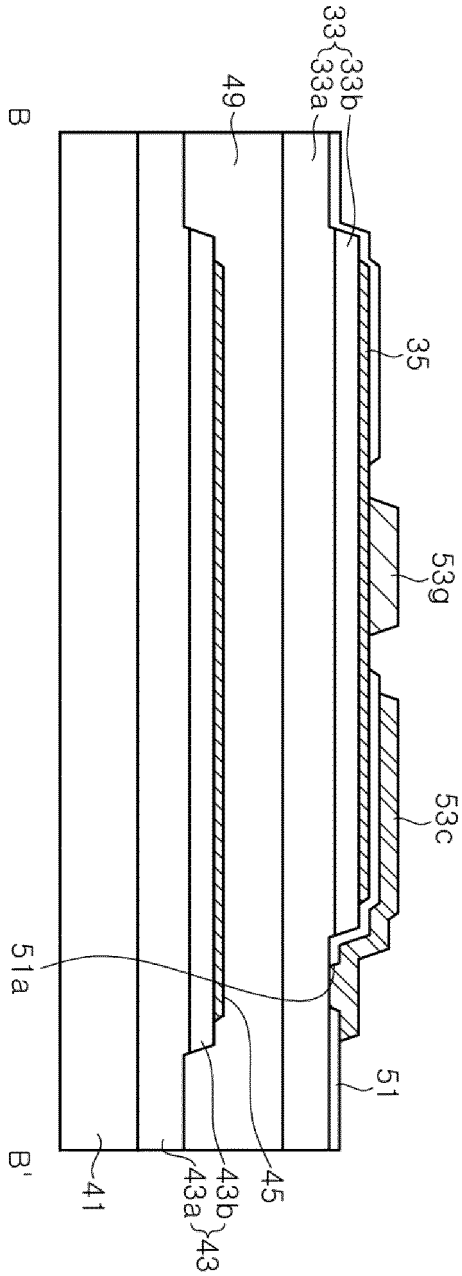

FIG. 8D

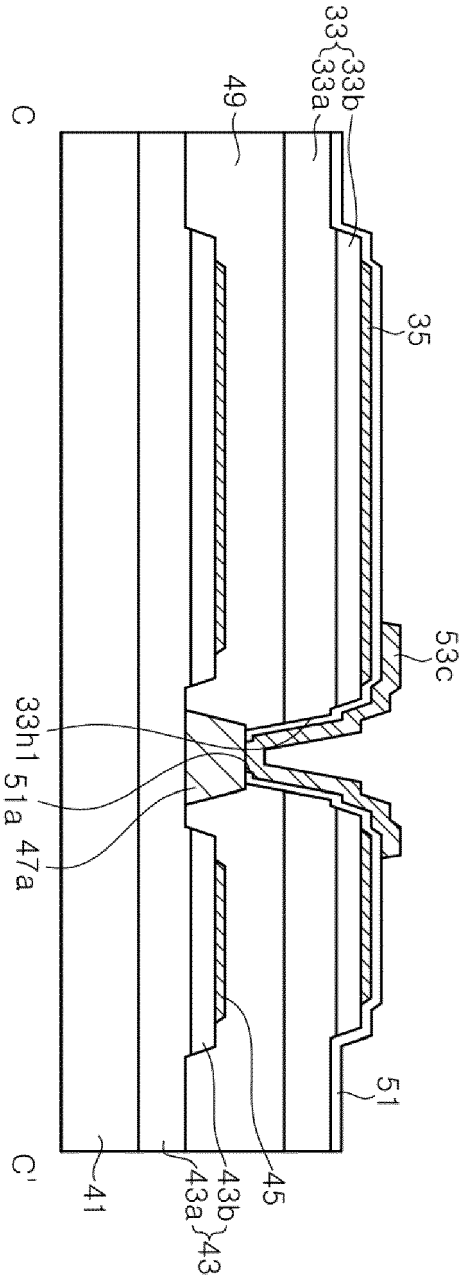

FIG. 9A

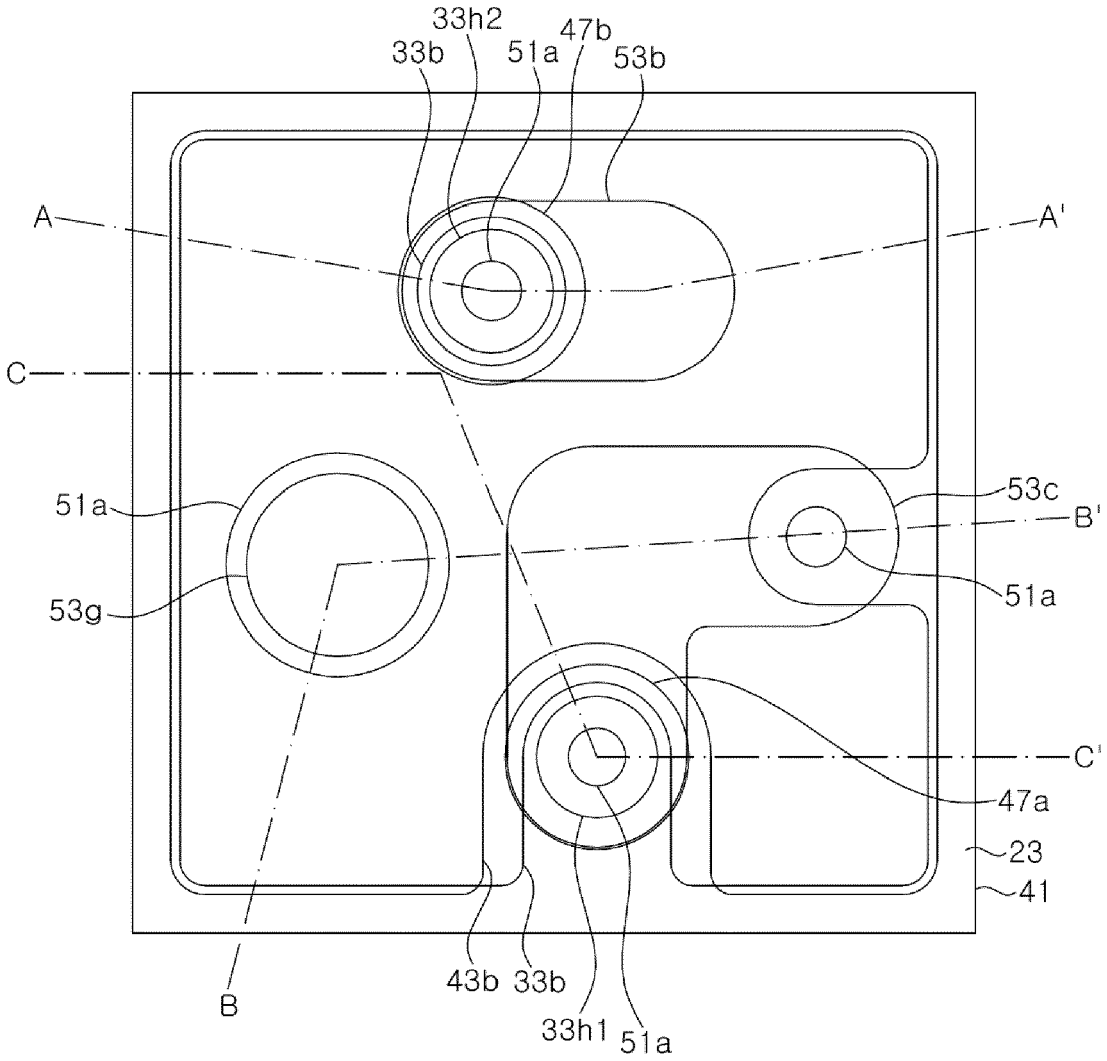
33h2
33b
51a
47b
53b
A
A'
C
51a
53c
B'
53g
51a
C'
47a
23
41
43b
33b
B
33h1
51a

FIG. 9B

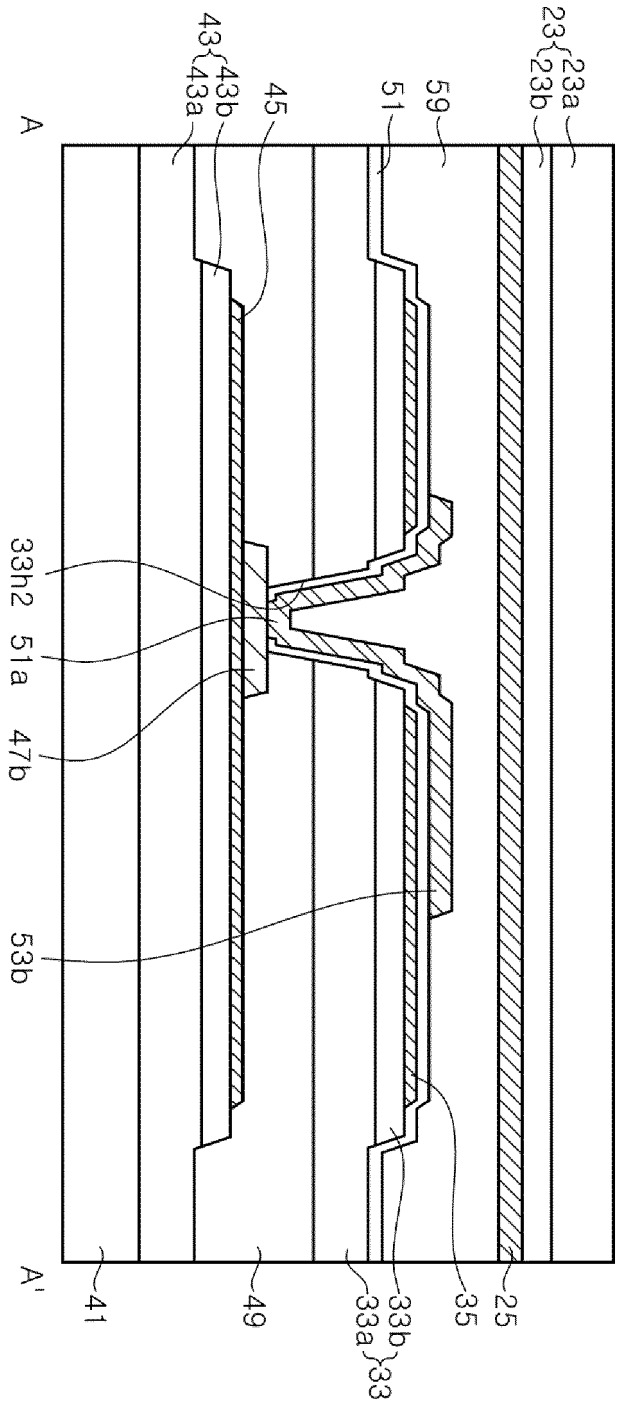
A
A'
43
43a
43b
45
51
59
23
23a
23b
33h2
51a
47b
53b
41
49
33a
33b
33
35
25

FIG. 9C

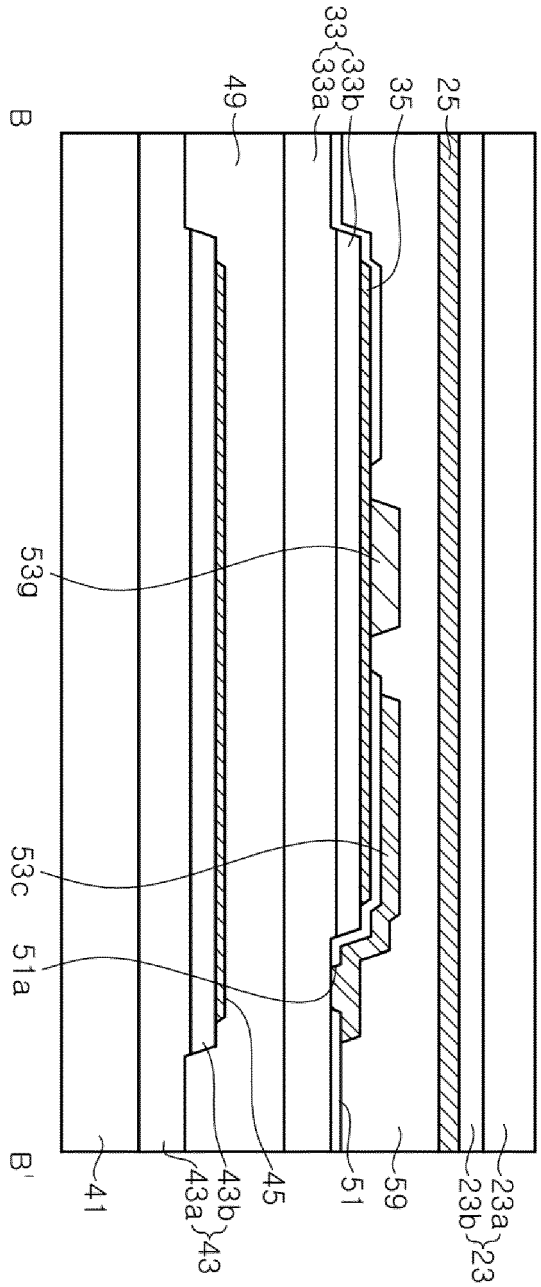

FIG. 9D

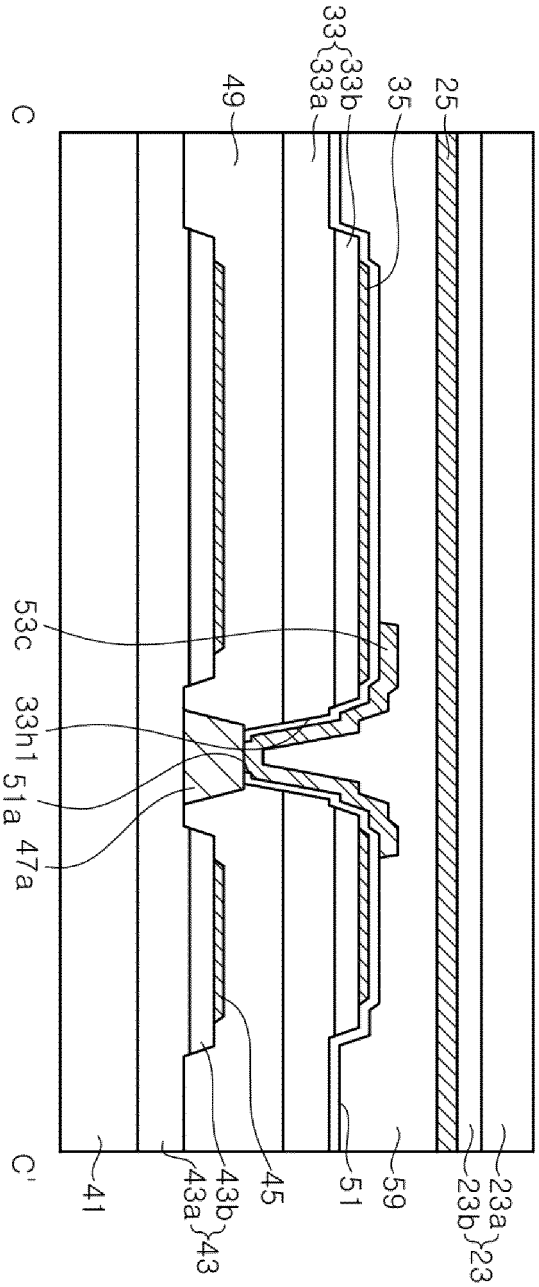
C
C'
49
33
33b
33a
35
25
53c
33h1
51a
47a
41
43a
43b
43
45
51
59
23a
23b
23

FIG. 10A

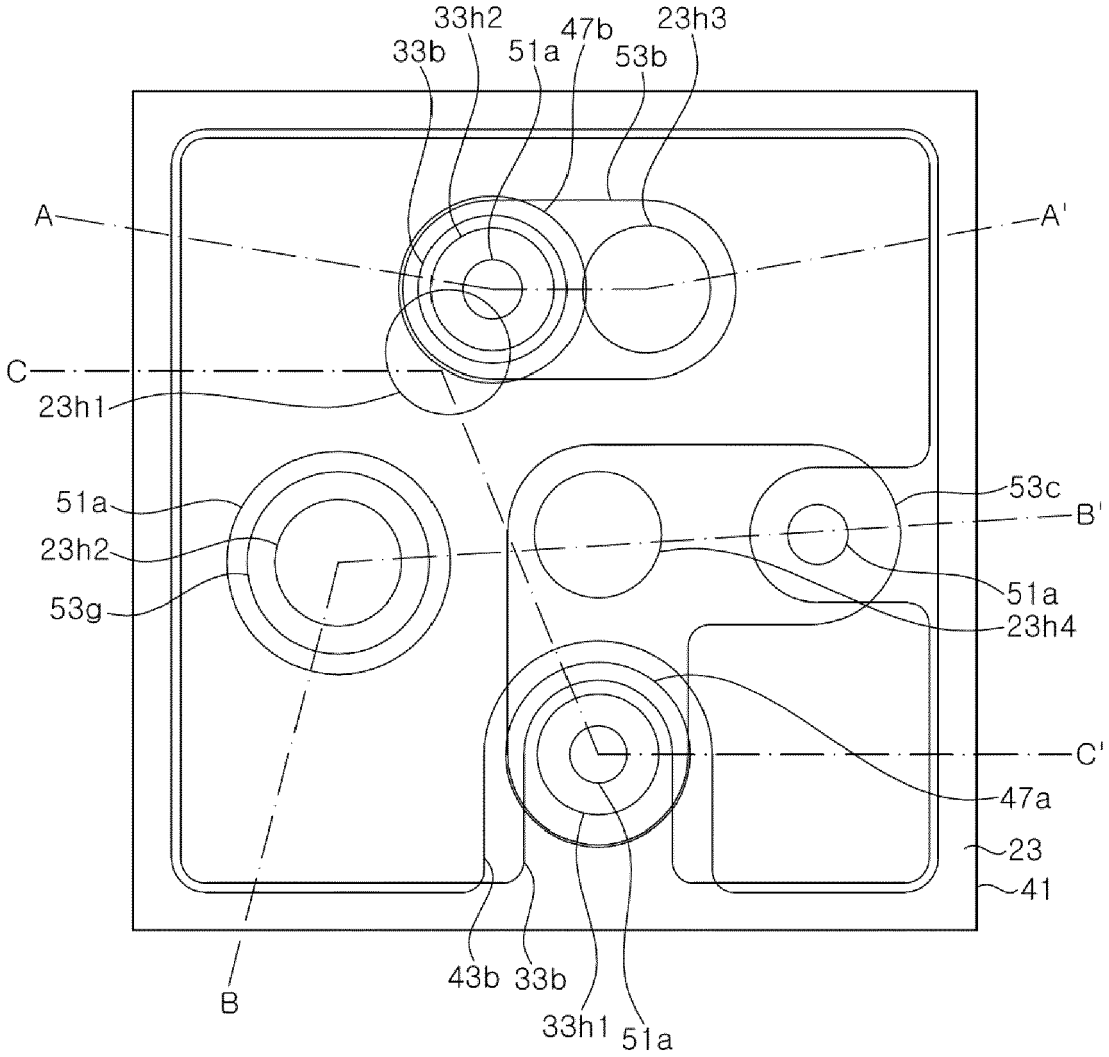
33h2
33b
51a
47b
53b
23h3
A
A'
C
23h1
51a
23h2
53g
53c
B'
51a
23h4
C'
47a
23
41
B
43b
33b
33h1
51a

FIG. 10B

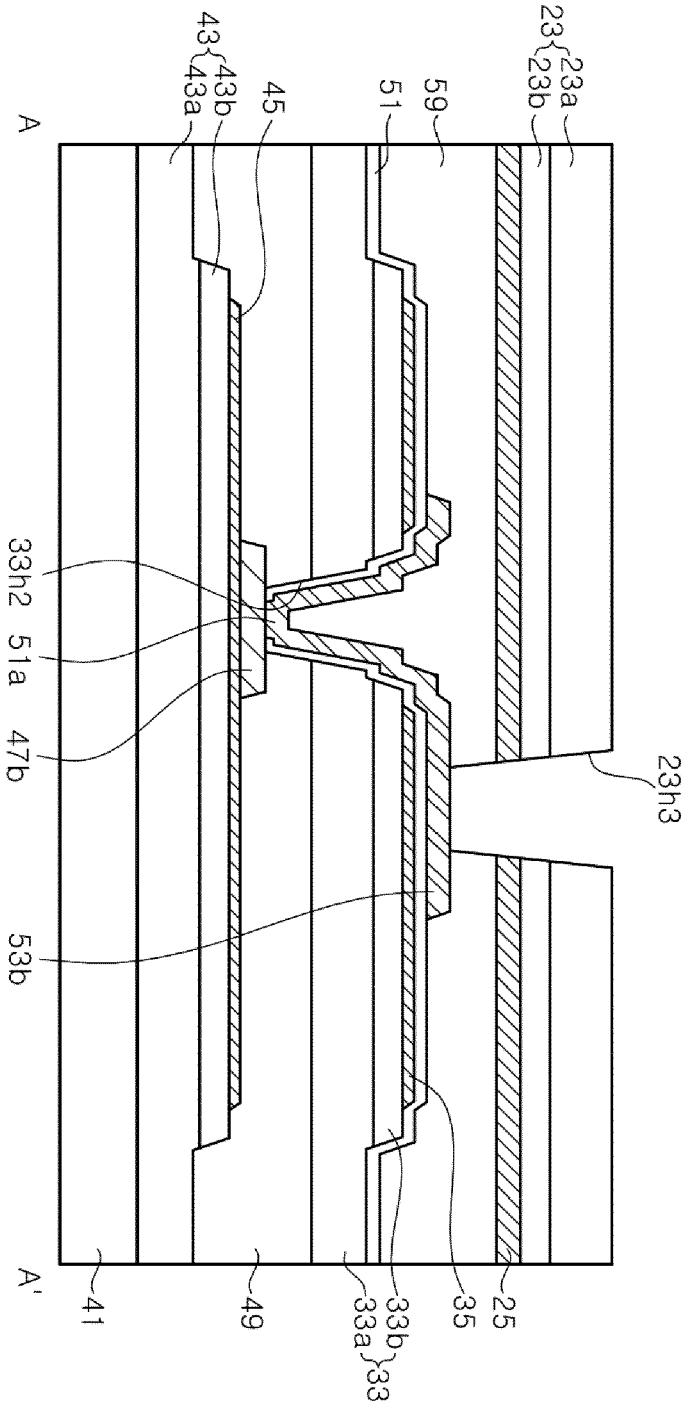
A
A'
43
43a
43b
45
51
59
23
23a
23b
33h2
51a
47b
53b
23h3
41
49
33a
33b
33
35
25

FIG. 10C

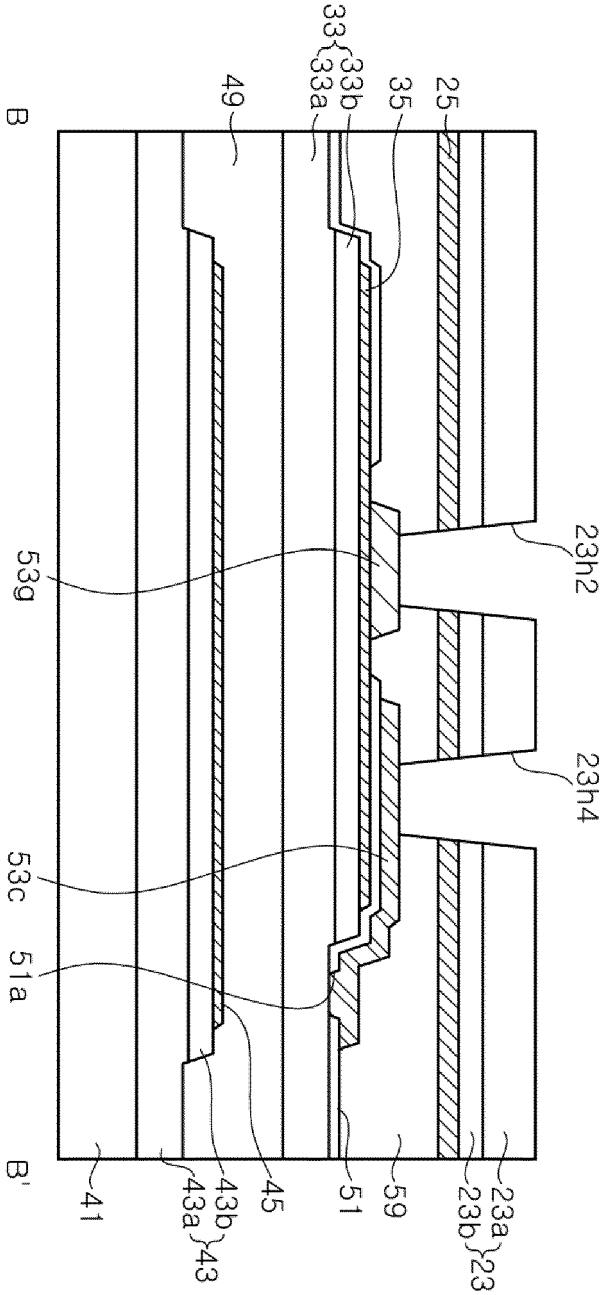
B
49
33
33b
33a
35
25
23h2
53g
23h4
53c
51a
B'
41
43b
43a
43
45
51
59
23a
23b
23

FIG. 10D

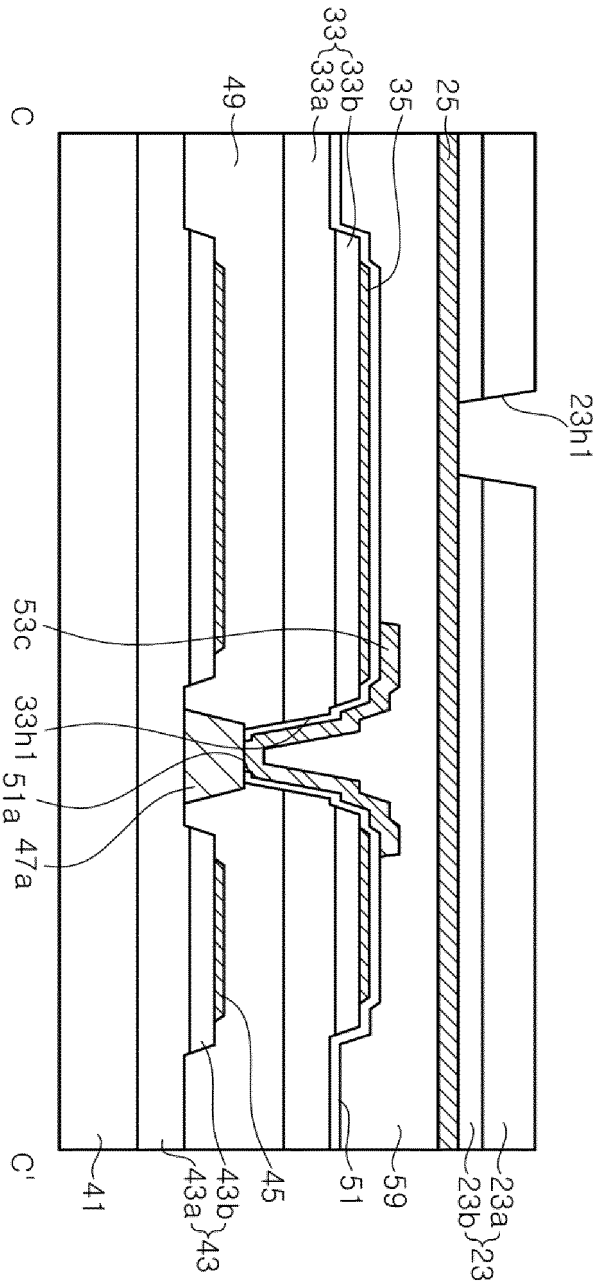
C
C'
49
33
33b
33a
35
25
23h1
53c
33h1
51a
47a
41
43a
43b
43
45
51
59
23a
23b
23

FIG. 11A

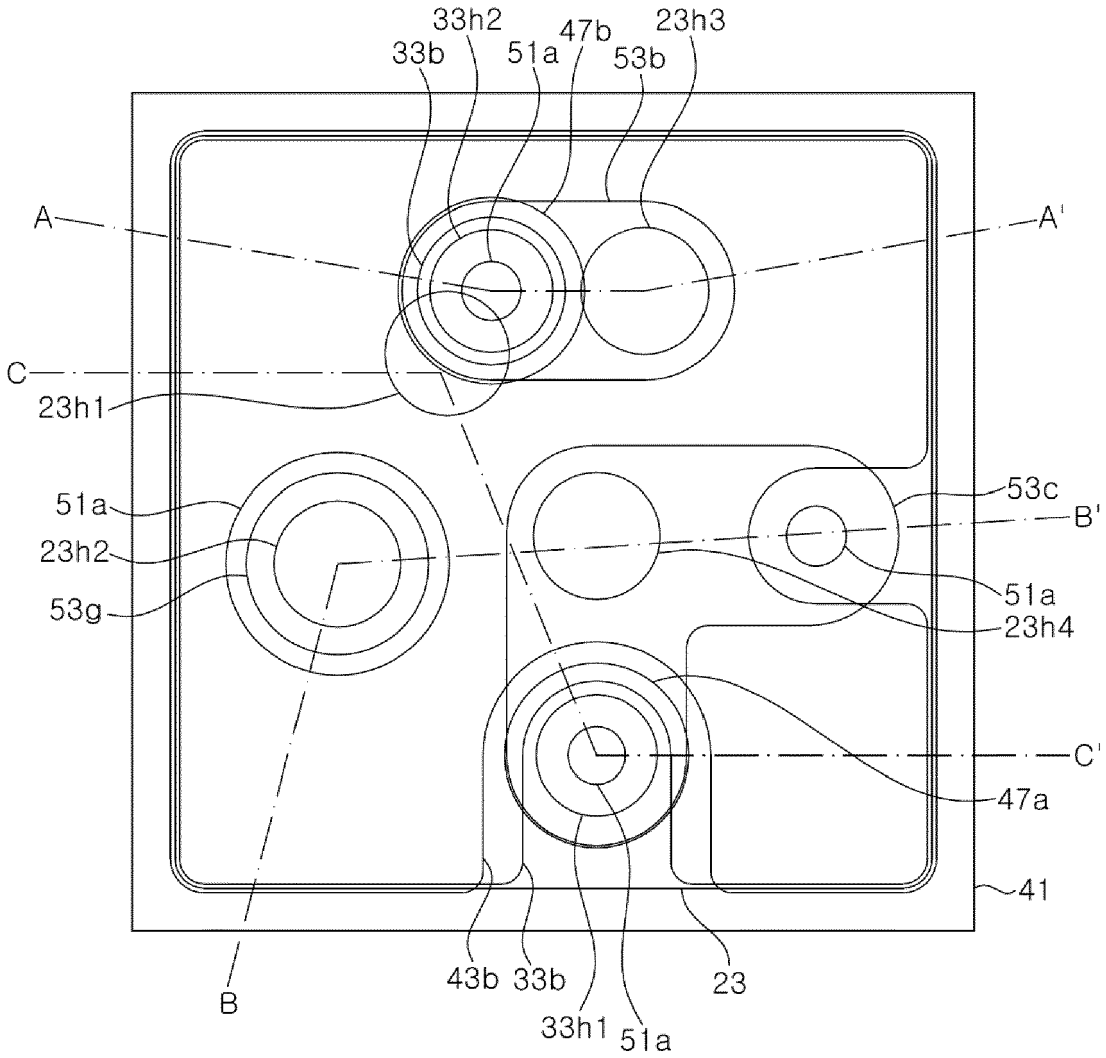
33h2
33b
51a
47b
53b
23h3
A
A'
C
23h1
51a
23h2
53g
53c
B'
51a
23h4
C'
47a
41
B
43b
33b
33h1
51a
23

FIG. 11B

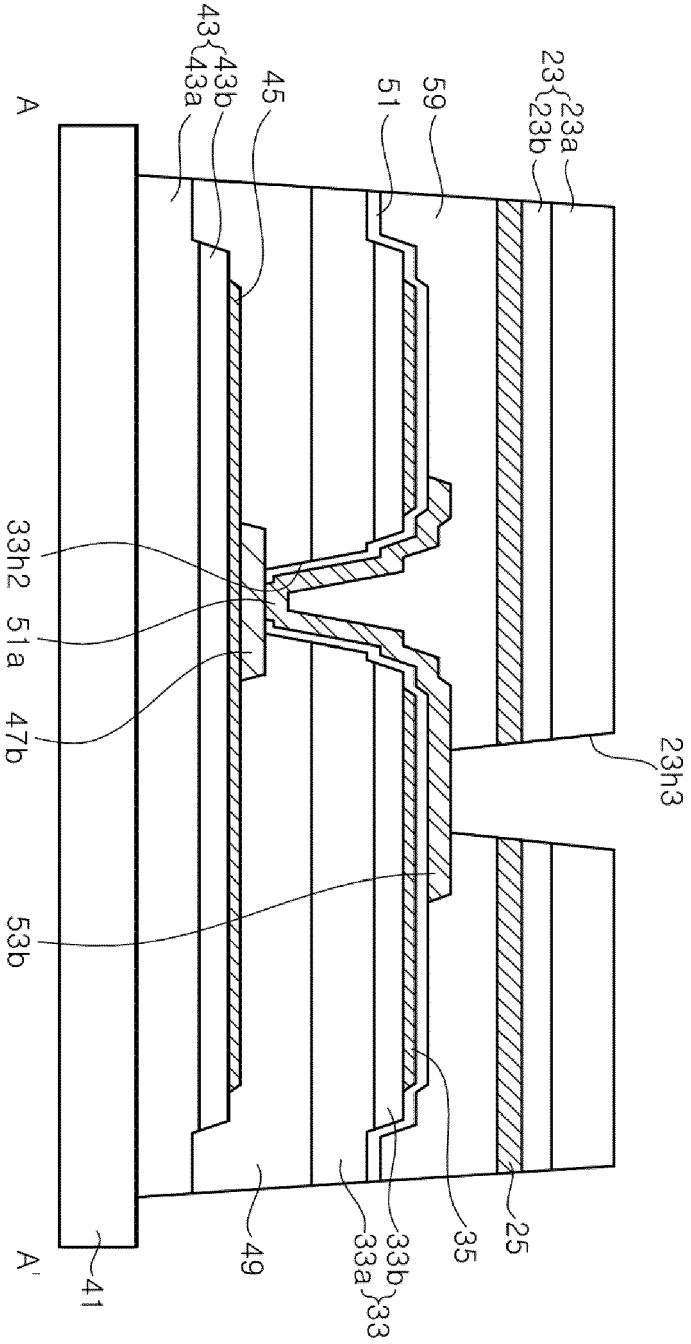
A
A'
43
43a
43b
45
51
59
23
23a
23b
33h2
51a
47b
53b
23h3
41
49
33a
33b
33
35
25

FIG. 11C

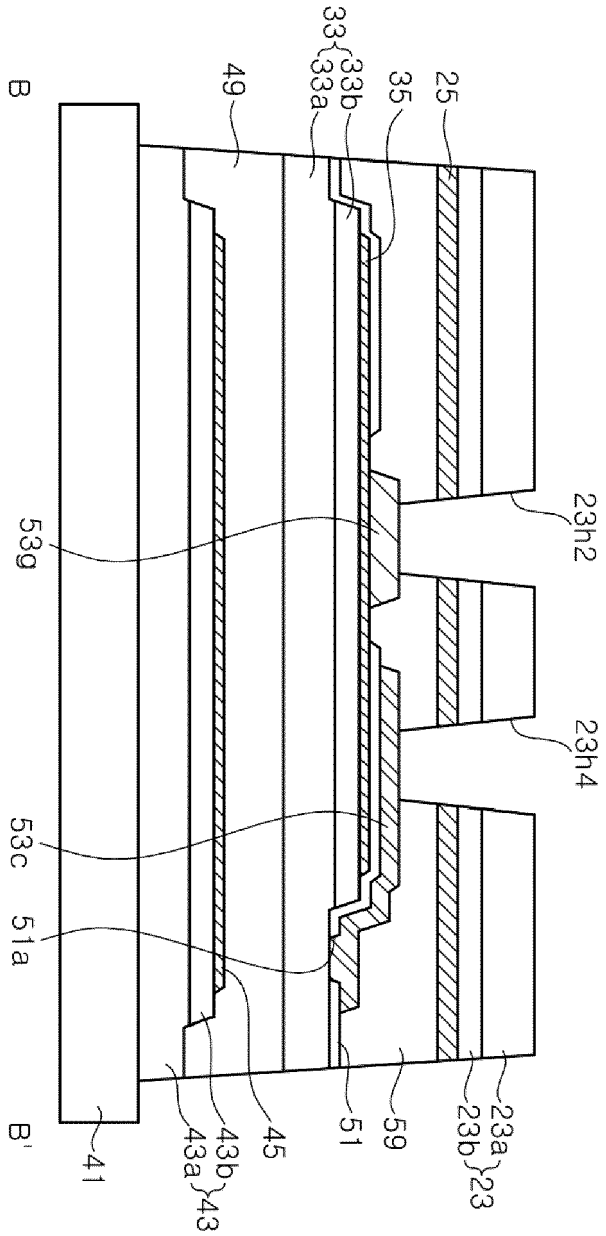
B
49
33
33b
33a
35
25
23h2
53g
23h4
53c
51a
B'
41
43a
43b
43
45
51
59
23b
23a
23

FIG. 11D

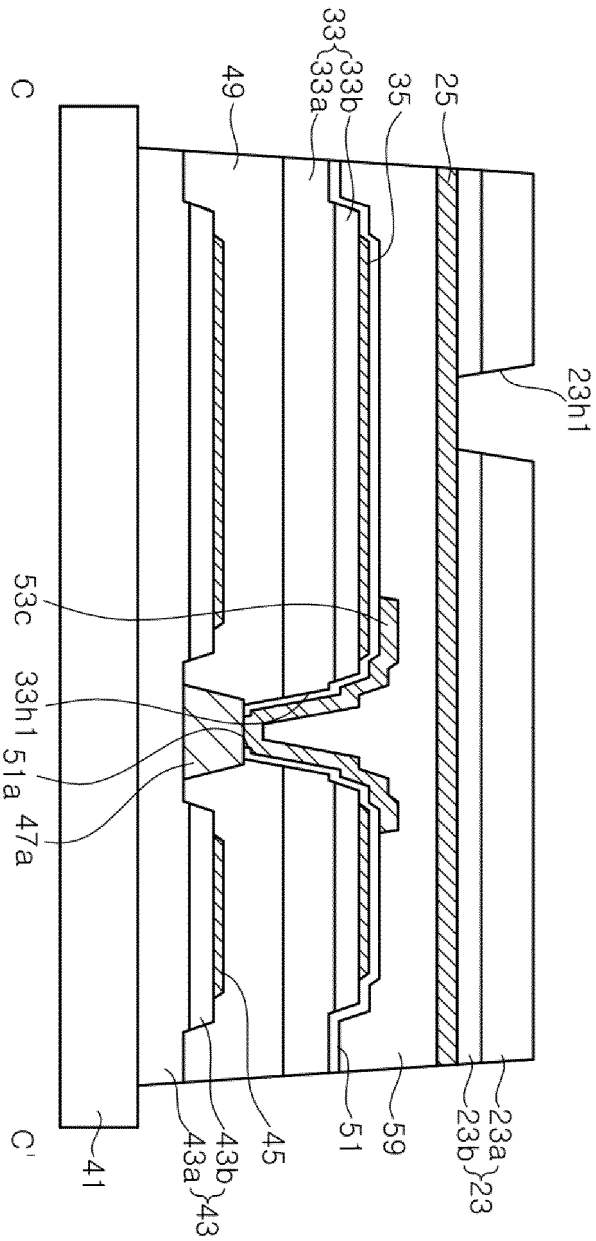
C
49
33
33b
33a
35
25
23h1
53c
33h1
51a
47a
C'
41
43a
43b
43
45
51
59
23a
23b
23

FIG. 12A

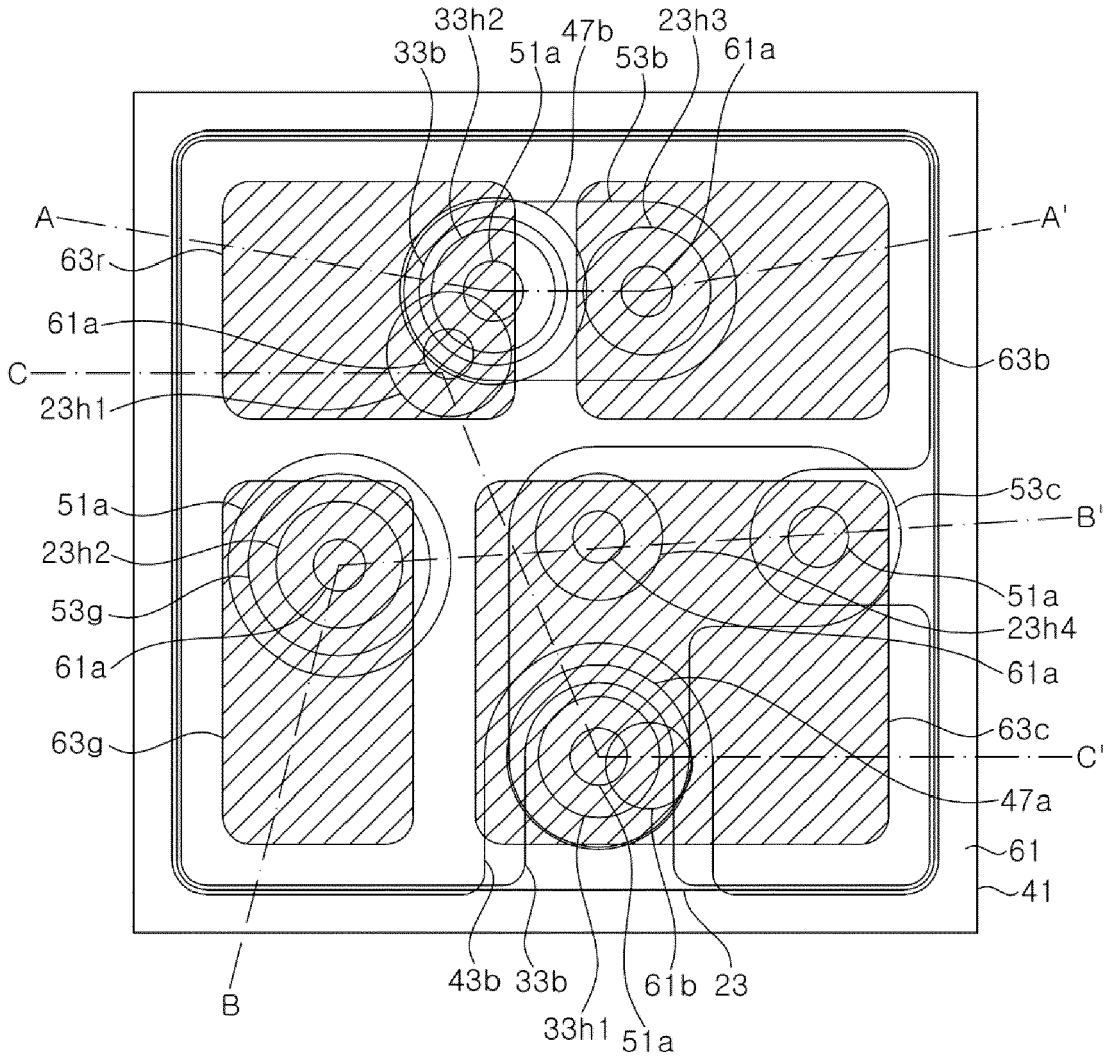
33h2
33b
51a
47b
53b
23h3
61a
A
A'
63r
61a
C
23h1
63b
51a
53c
B'
23h2
53g
61a
63g
51a
23h4
61a
63c
C'
47a
61
41
B
43b
33b
33h1
51a
61b
23

FIG. 12B

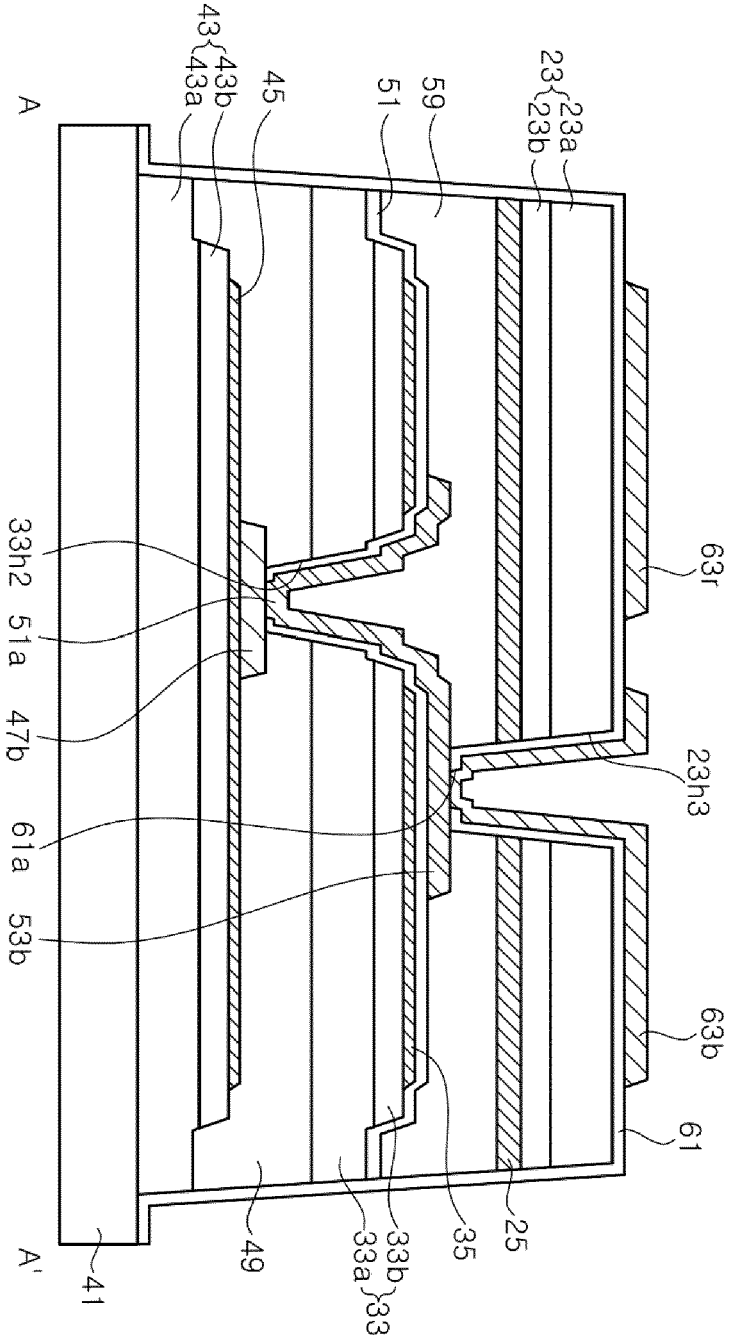
A
A'
43
43a
43b
45
51
59
23
23a
23b
33h2
51a
47b
61a
53b
63r
23h3
63b
61
41
49
33a
33b
33
35
25

FIG. 12C

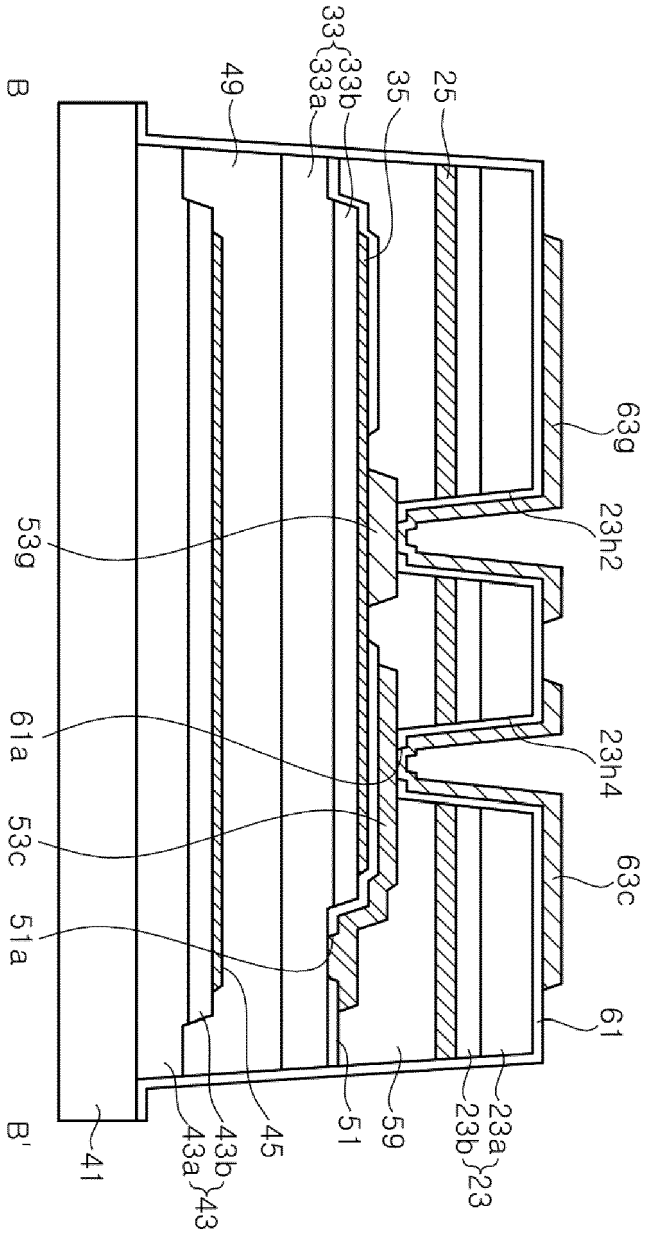
B
49
33
33b
33a
35
25
63g
23h2
53g
61a
23h4
53c
63c
51a
61
B'
41
45
51
59
23a
23b
23
43b
43a
43

FIG. 12D

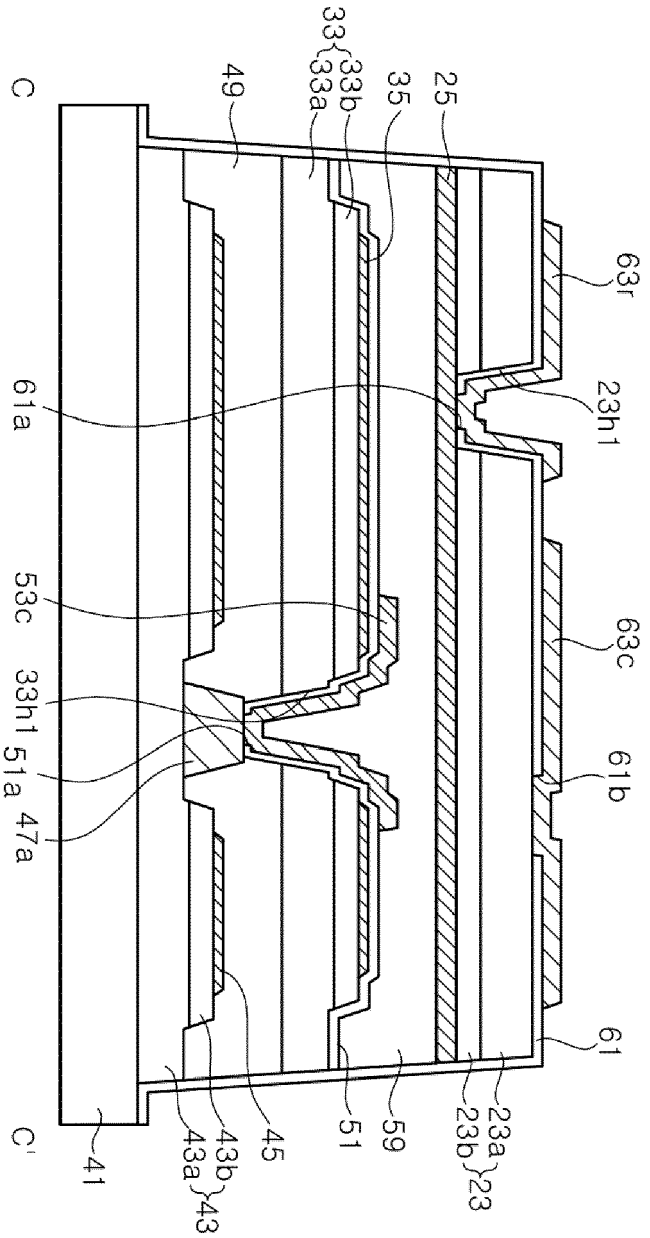
C
C'
49
33
33b
33a
35
25
63r
23h1
61a
53c
63c
33h1
61b
51a
47a
61
41
43a
43b
43
45
51
59
23a
23b
23

FIG. 13A

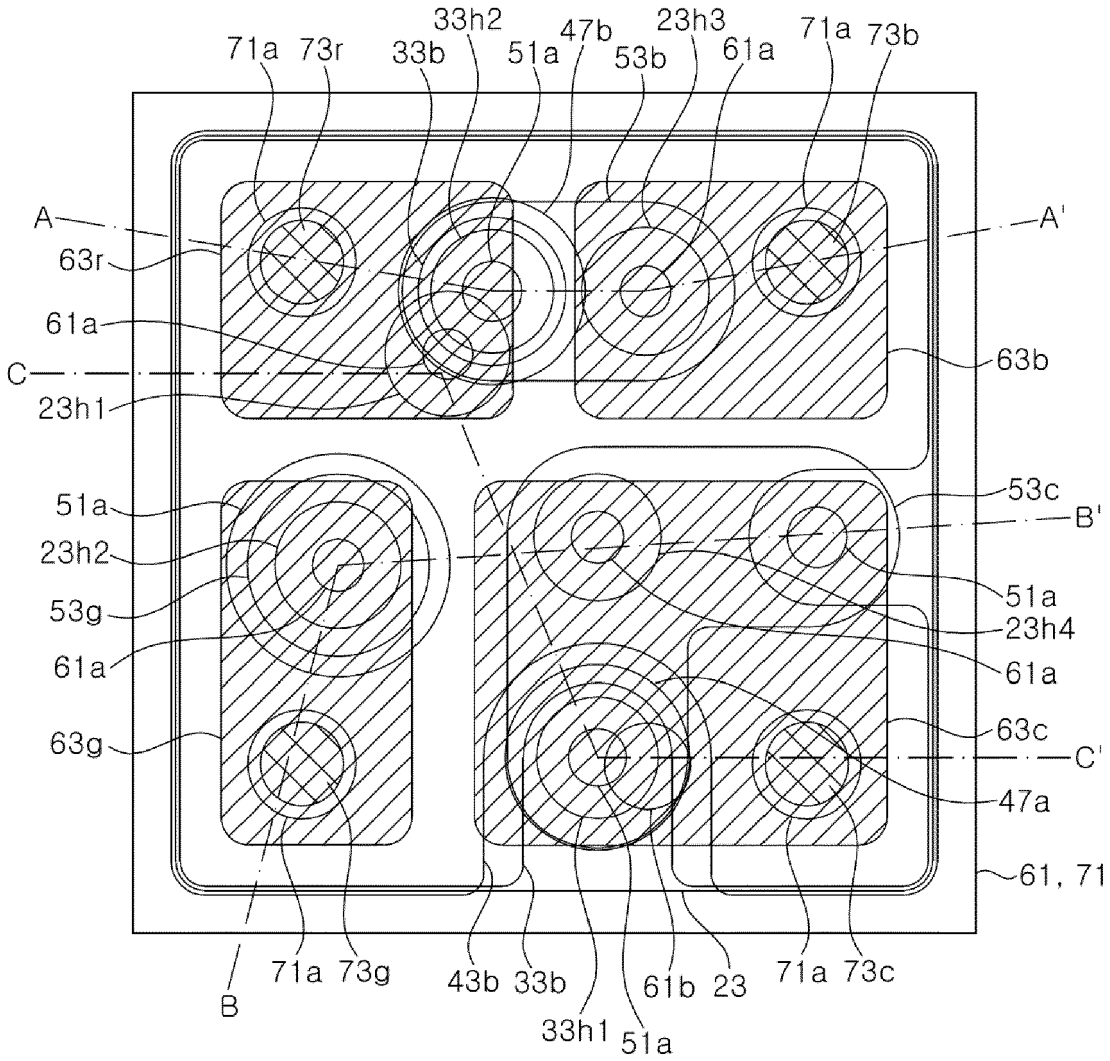
71a
73r
33b
33h2
51a
47b
53b
23h3
61a
71a
73b
A
A'
63r
61a
C
23h1
63b
51a
23h2
53g
61a
63g
53c
B'
51a
23h4
61a
63c
C'
47a
61, 71
B
71a
73g
43b
33b
33h1
51a
61b
23
71a
73c

FIG. 13B

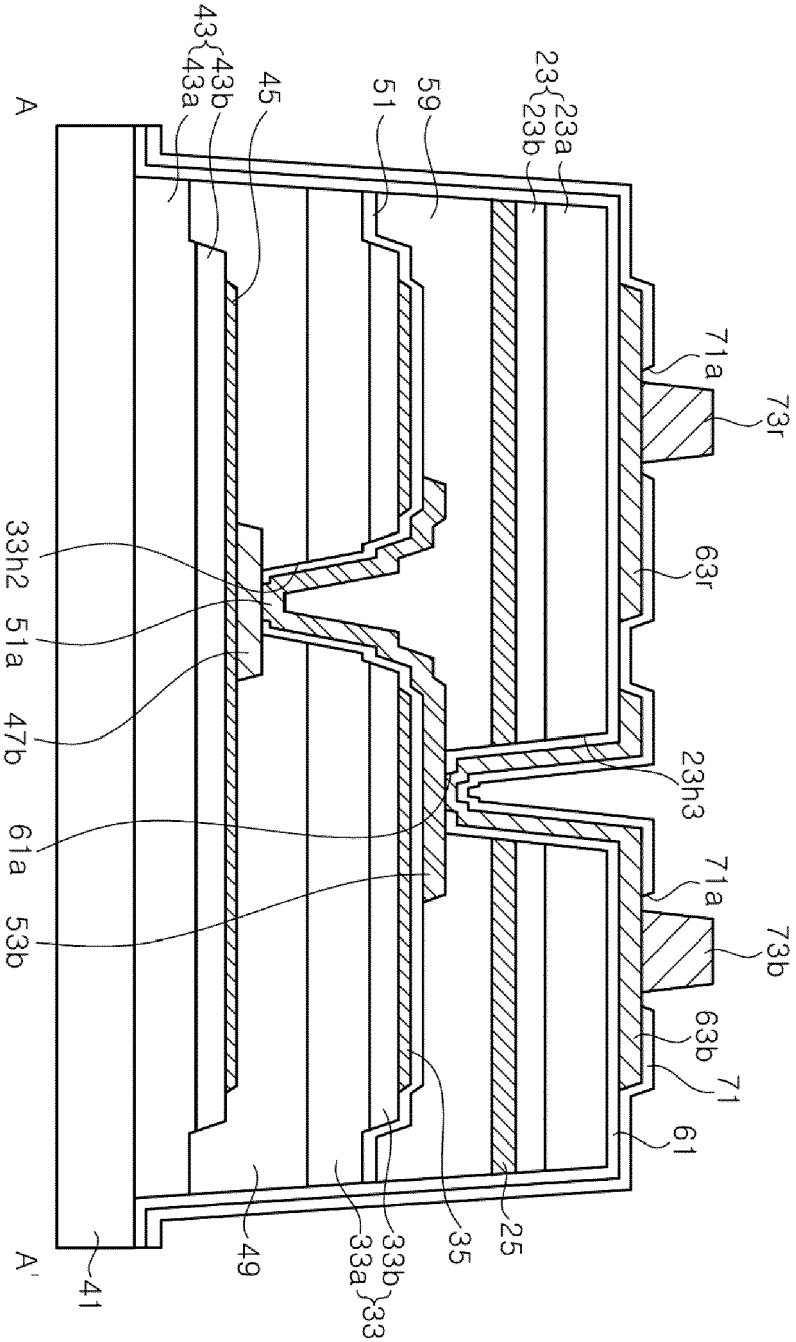
A
A'
43
43a
43b
45
51
59
23
23a
23b
71a
73r
63r
33h2
51a
47b
61a
53b
23h3
71a
73b
63b
71
61
49
35
25
33b
33a
33
41

FIG. 13C

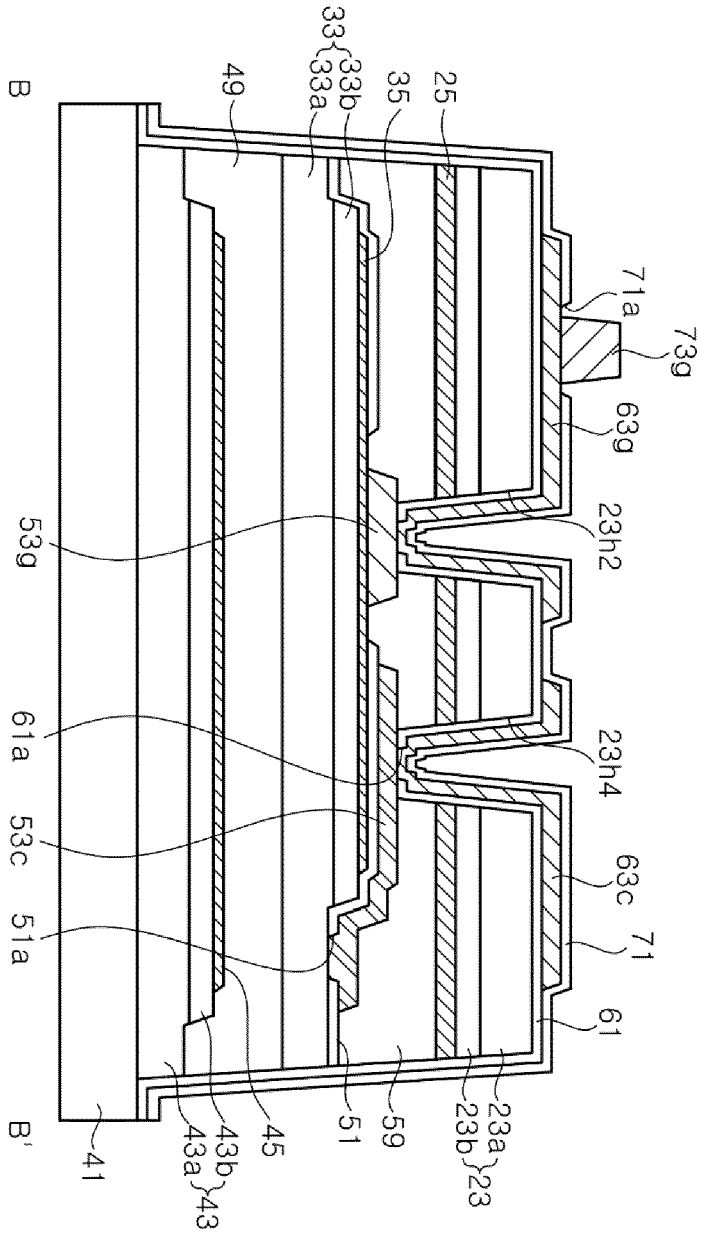
B
B'
33
33b
33a
49
35
25
71a
73g
63g
23h2
53g
61a
23h4
53c
63c
71
51a
61
41
43a
43b
43
45
51
59
23a
23b
23

FIG. 13D

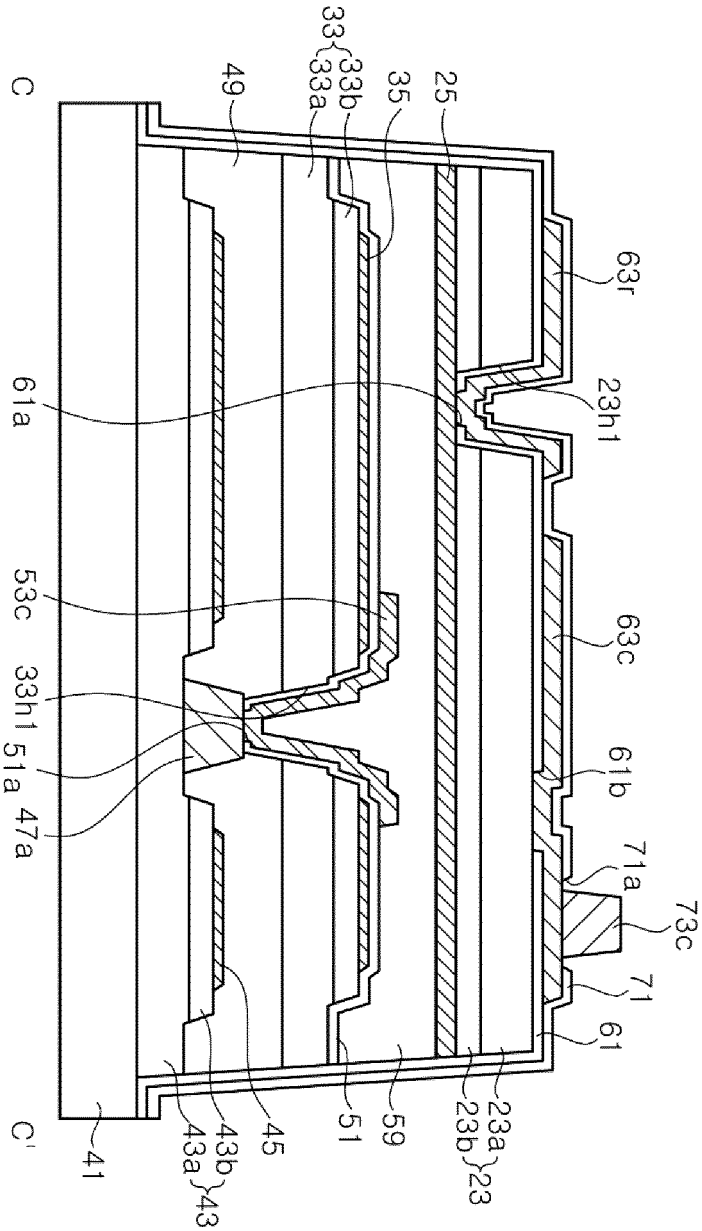
C
C'
33
33b
33a
49
35
25
63r
23h1
61a
53c
63c
33h1
51a
47a
61b
71a
73c
71
61
23a
23b
23
59
51
45
43b
43a
43
41

FIG. 14

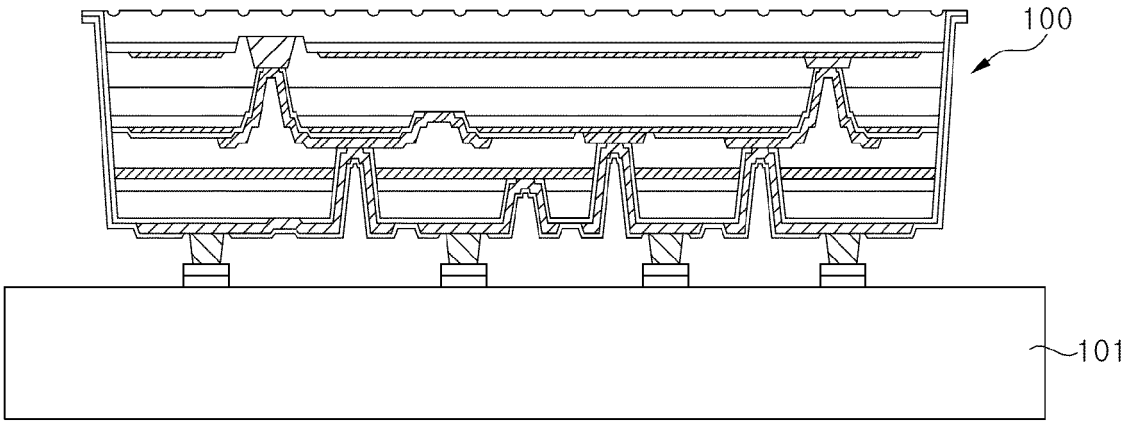

FIG. 15A

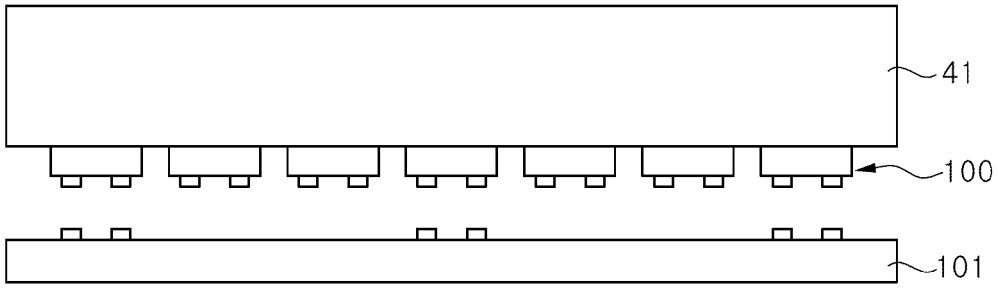

FIG. 15B

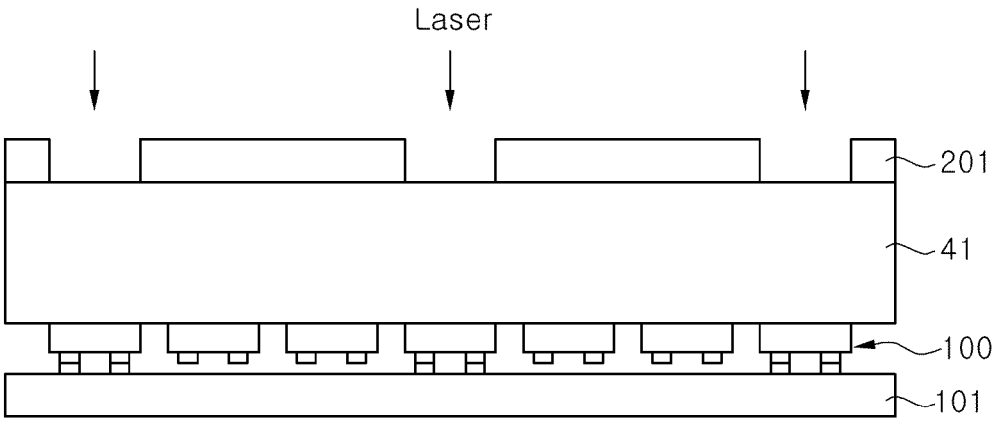

FIG. 15C