(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 513 292 A2**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
26.02.2025 Bulletin 2025/09

(21) Application number: **24189704.0**

(22) Date of filing: **19.07.2024**

(51) International Patent Classification (IPC):
G05F 3/24 *(2006.01)* ***G05F 3/26*** *(2006.01)*

(52) Cooperative Patent Classification (CPC):
G05F 3/262; G05F 3/245

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA
Designated Validation States:
GE KH MA MD TN

(30) Priority: **22.08.2023 US 202318453882**

(71) Applicant: **Analog Devices, Inc.**
Wilmington, MA 01887 (US)

(72) Inventors:
- **WRENNER, Kevin**
  Wilmington, 01887 (US)
- **YUN, Ruida**
  Wilmington, 01887 (US)
- **RICHARDSON, Kenneth**
  Wilmington, 01887 (US)

(74) Representative: **Horler, Philip John**
Withers & Rogers LLP
2 London Bridge
London SE1 9RA (GB)

(54) BIAS CURRENT WITH HYBRID TEMPERATURE PROFILE

(57) Aspects of the present disclosure include a scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising a bias mirror circuit configured to provide a zero temperature coefficient (ZTC) current, a PTAT control circuit configured to generate, based on the ZTC current, a PTAT current with a slope having a non-zero value, alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current, and provide the altered PTAT current, a hybrid circuit configured to receive the ZTC current and the altered PTAT current, and output a larger current of the ZTC current and the altered PTAT current as a hybrid current.

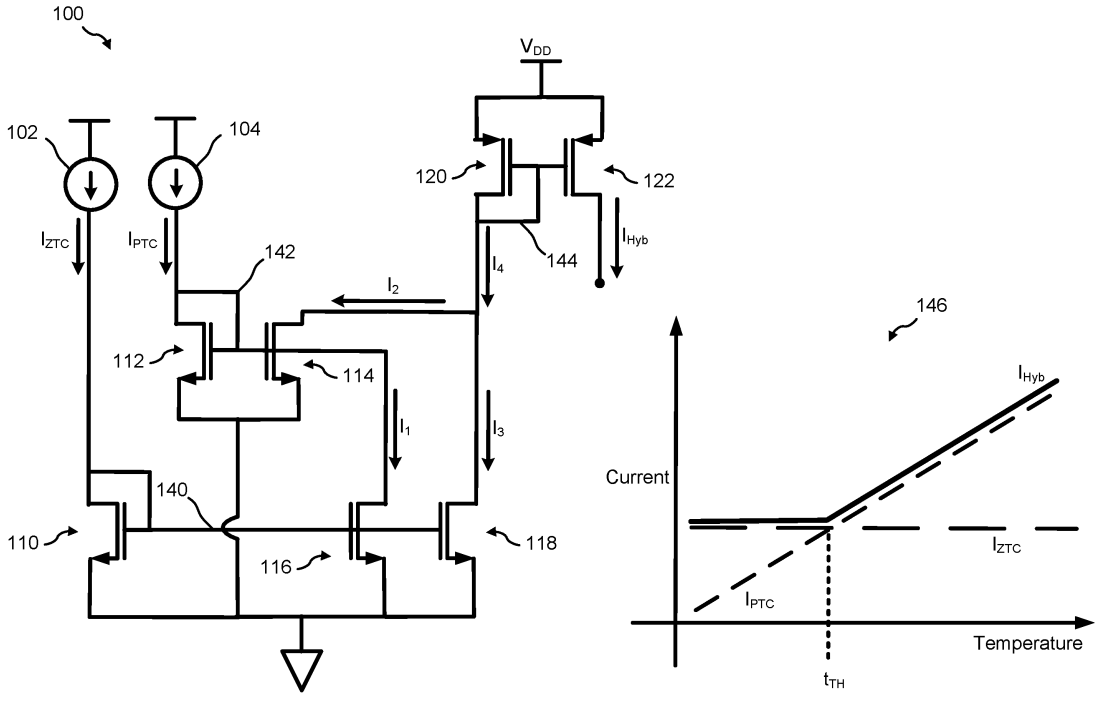

FIG. 1

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Description

BACKGROUND

[0001] Integrated circuits (ICs) are commonly designed with a zero temperature coefficient (ZTC) bias scheme or a positive temperature coefficient (PTC) bias scheme (also known as proportional to absolute temperature (PTAT) bias). A ZTC bias circuit is a circuit that provides a bias current that is substantially invariant to temperature changes. A PTC bias circuit is a circuit that provides a bias current that changes proportionally with temperature. However, a ZTC bias circuit may be unable to provide sufficient current and/or gain above a certain temperature. Similarly, a PTC bias circuit, while able to provide sufficient current and/or gain above a certain temperature, may be unable to provide sufficient current and/or gain below a certain temperature.

[0002] Thus, improvements in such bias circuits are desired.

SUMMARY

[0003] The following presents a simplified summary of one or more aspects in order to provide a basic understanding of such aspects. This summary is not an extensive overview of all contemplated aspects, and is intended to neither identify key or critical elements of all aspects nor delineate the scope of any or all aspects. Its sole purpose is to present some concepts of one or more aspects in a simplified form as a prelude to the more detailed description that is presented later.

[0004] Aspects of the present disclosure include a scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising a bias mirror circuit configured to provide a zero temperature coefficient (ZTC) current, a PTAT control circuit configured to generate, based on the ZTC current, a PTAT current with a slope having a non-zero value, alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current, and provide the altered PTAT current, a hybrid circuit configured to receive the ZTC current and the altered PTAT current, and output a larger current of the ZTC current and the altered PTAT current as a hybrid current.

[0005] Aspects of the present disclosure include a scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising a bias mirror circuit having a zero temperature coefficient (ZTC) current source configured to induce a ZTC current, a PTAT control circuit having two or more first source transistors, a first BJT connected to one of the two or more first source transistors, a first variable resistor connected to the first BJT, a first transistor connected to the first variable resistor, wherein the first BJT, the first variable resistor, and the first transistor are connected in series, a second transistor, a second variable resistor connected to a drain terminal of the second transistor and a first base of the first BJT, a third variable resistor connected to the second variable resistor, wherein the second transistor, the second variable resistor, and the third variable resistor are connected in series, a bandgap circuit having a second BJT and a third BJT, wherein a second base of the second BJT and a third base of the third BJT are connected to the second variable resistor and the third variable resistor, a fourth variable resistor connected to the second BJT of the bandgap circuit, and a third transistor connected to the fourth variable resistor, and a hybrid circuit.

[0006] Aspects of the present disclosure include a method of providing a hybrid current by a scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising: providing a zero temperature coefficient (ZTC) current, generating, based on the ZTC current, a PTAT current having a slope having a non-zero value, altering the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current, and outputting a larger current of the ZTC current and the altered PTAT current as a hybrid current.

[0007] To the accomplishment of the foregoing and related ends, the one or more aspects comprise the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative features of the one or more aspects. These features are indicative, however, of but a few of the various ways in which the principles of various aspects may be employed, and this description is intended to include all such aspects and their equivalents.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The disclosed aspects will hereinafter be described in conjunction with the appended drawings, provided to illustrate and not to limit the disclosed aspects, wherein like designations denote like elements, and in which:

FIG. 1 is a circuit diagram of an example of a hybrid circuit, including an inset graph of current versus temperature performance of the hybrid circuit, according to aspects of the present disclosure.

FIG. 2 is a circuit diagram of another example of the hybrid circuit of Fig. 1 according to aspects of the present disclosure.

FIG. 3 is a circuit diagram of a further example of the hybrid circuit of Fig. 1 according to aspects of the present disclosure.

FIG. 4 includes example graphs of example characteristics of the hybrid circuit, including current versus temperature performance, and corresponding temperature coefficient versus temperature performance, according to aspects of the present disclosure.

FIG. 5 is a circuit diagram of an example of another hybrid circuit, including an inset graph of current

versus temperature performance of the hybrid circuit, according to aspects of the present disclosure.

FIG. 6 includes graphs of examples of current versus temperature profiles of a scalable PTAT hybrid circuit according to aspects of the present disclosure.

FIG. 7 is a circuit diagram of an example of a scalable PTAT hybrid circuit according to aspects of the present disclosure.

FIG. 8 is a flowchart of an example of a method for providing a hybrid current via a scalable PTAT hybrid circuit according to aspects of the present disclosure.

FIG. 9 illustrates examples of current supplies according to aspects of the present disclosure.

FIG. 10 is an example of a circuit configured as a variable resistor according to aspects of the present disclosure.

FIG. 11 illustrates additional examples of variable resistors according to aspects of the present disclosure.

FIG. 12 is an example of a PTAT generator according to aspects of the present disclosure.

FIG. 13 is an example of a PTAT generator with one or more variable resistors according to aspects of the present disclosure.

DETAILED DESCRIPTION

[0009] The detailed description set forth below in connection with the appended drawings is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well known structures and components are shown in block diagram form in order to avoid obscuring such concepts.

[0010] According to one aspect of the present disclosure, an integrated circuit (IC) bias scheme may operate with a positive temperature coefficient (PTC) at temperatures above a threshold temperature, and with zero temperature coefficient (ZTC) at temperatures below the threshold temperature. This hybrid approach may compensate for gain loss at higher temperatures without sacrificing signal levels at lower temperatures.

[0011] In one aspect of the present disclosure, a scalable proportional to absolute temperature (PTAT) hybrid circuit may output a hybrid current having a ZTC current at temperatures below a threshold temperature and a PTC current at temperature above the threshold temperature. The PTAT hybrid circuit may be configured to control the current magnitude of the hybrid current, and/or the slope of the PTC current.

[0012] Referring to FIG. 1, a hybrid circuit 100 configured to provide a PTC current at temperatures above a threshold temperature, and a ZTC current at temperatures below the threshold temperature. The hybrid circuit 100 may include a ZTC current source 102 configured to provide a ZTC current I_{ZTC} into the hybrid circuit 100. The hybrid circuit 100 may include a PTC current source 104 configured to provide a PTC current I_{PTC} into the hybrid circuit 100. The hybrid circuit 100 may include a first current sink 110 configured to sink the ZTC current I_{ZTC}. The hybrid circuit 100 may include a second current sink 112 configured to sink the PTC current I_{PTC}. The first current sink 110 may be disposed in series, parallel, or other configurations with respect to the ZTC current source 102. The second current sink 112 may be disposed in series, parallel, or other configurations with respect to the PTC current source 104.

[0013] In some aspects of the present disclosure, the hybrid circuit 100 may include a first transistor 114 configured to provide a second current I_2, which may be the maximum of zero current and the difference between the PTC current I_{PTC} and the ZTC current I_{ZTC}. The hybrid circuit 100 may include a second transistor 116 configured to sink a first current I_1, which may be the minimum of the ZTC current I_{ZTC} and the PTC current I_{PTC}. The hybrid circuit 100 may include a third transistor 118 configured to sink a third current I_3, which may be the ZTC current I_{ZTC}.

[0014] In certain aspects of the present disclosure, the hybrid circuit 100 may include a first current source 120 configured to accept a fourth current I_4, which may be a summation current of the second current I_2 and the third current I_3. The hybrid circuit 100 may include a current mirror 122 configured to mirror the fourth current I_4 and provide a hybrid current I_{Hyb}. The first current source 120 and the current mirror 122 may be connected to a voltage supply V_{DD}.

[0015] During normal operation, in certain aspects of the present disclosure, the ZTC current source 102 may provide the ZTC current I_{ZTC} toward the first current sink 110. The ZTC current I_{ZTC} may cause a first gate voltage on a first gate terminal 140. The first gate voltage may turn the first current sink 110, the second transistor 116, and/or the third transistor 118 from an off state to an on state. The first gate voltage may cause the third transistor 118 to mirror the same amount of current (i.e., the third current I_3) as I_{ZTC}. Specifically, the first gate voltage may turn on the third transistor 118, which may provide the third current I_3. Since the source terminal of the third transistor 118 is connected to the ground terminal, a third gate voltage may be developed on the drain terminal of the third transistor, which is shorted to a third gate terminal 144. Since the first current source 120 is consistently biased in the saturation regime (i.e., gate and drain terminals connected), the third gate voltage may cause the first current source 120 to provide the fourth current.

[0016] In some aspects, the PTC current source 104 may provide the PTC current I_{PTC} toward the second current sink 112. The PTC current I_{PTC} may cause a second gate voltage on a second gate terminal 142.

The second gate voltage may be insufficient to turn on the second current sink 112 or the first transistor 114, or be sufficient to turn the second current sink 112 and the first transistor 114 from an off state to an on state, depending on the ZTC current I_{ZTC} as explained below.

[0017] In some aspects of the present disclosure, as shown in graph 146, for temperatures below a threshold temperature T_{TH}, the ZTC current I_{ZTC} may be larger than the PTC current I_{PTC}. As explained above, the ZTC current I_{ZTC} may induce the first gate voltage at the first gate terminal 140. Since the ZTC current I_{ZTC} is larger than the PTC current I_{PTC}, the first gate voltage may turn on the second transistor 116. Consequently, the PTC current I_{PTC} provided by the PTC current source 104 may not turn on the first transistor 114 because an entire amount of the PTC current I_{PTC} is sunk through the second transistor 116. As such, the second current I_2 is zero because the first transistor 114 is off. Therefore, the third current I_3 and the fourth current I_4 may both equal to the ZTC current I_{ZTC}, and the current mirror 122 will provide the hybrid current I_{Hyb} having the same current level as the ZTC current I_{ZTC}. In other words, for temperatures below the threshold temperature T_{TH}, the hybrid current I_{Hyb} is equal to the ZTC current I_{ZTC}.

[0018] In other aspects of the present disclosure, for temperature above the threshold temperature T_{TH}, the PTC current I_{PTC} may be larger than the ZTC current I_{ZTC}. As explained above, the ZTC current I_{ZTC} may induce the first gate voltage at the first gate terminal 140. Since the PTC current I_{PTC} is larger than the ZTC current I_{ZTC}, the first gate voltage may turn on the second transistor 116. However, the second transistor 116 is able to sink only the ZTC current I_{ZTC} (which is smaller than the PTC current I_{PTC}). Consequently, a differential current (i.e., I_{PTC} - I_{ZTC}) may be sunk through the second current sink 112. The differential current may cause the second gate voltage to be developed on the second gate terminal 142. The second gate voltage may turn on the first transistor 114 such that the second current I_2 mirrors the differential current (i.e., I_{PTC} - I_{ZTC}). Since the third current I_3 may be equal to the ZTC current I_{ZTC}, the fourth current I_4 may become a sum of the second current I_2 and the third current I_3, which is the PTC current I_{PTC} (i.e., $I_2 + I_3 = (I_{PTC} - I_{ZTC}) + I_{ZTC} = I_{PTC}$). As a result, the current mirror 122 will provide the hybrid current I_{Hyb} having the same current level as the PTC current I_{PTC}. In other words, for temperatures above the threshold temperature T_{TH}, the hybrid current I_{Hyb} is equal to the PTC current I_{PTC}.

[0019] In some aspects, the hybrid current I_{Hyb} provided by the hybrid circuit 100 may exhibit characteristics shown in the graph 146. Specifically, at temperatures below the threshold temperature T_{TH}, the hybrid current I_{Hyb} may be constant with temperature. And, at temperatures above the threshold temperature T_{TH}, the hybrid current I_{Hyb} may increase with temperature. The hybrid current I_{Hyb} may be the maximum current of the PTC current I_{PTC} and the ZTC current I_{ZTC}.

[0020] In some aspects of the present disclosure, one or more of the first current sink 110, the second current sink 112, the first transistor 114, the second transistor 116, and/or the third transistor 118 may be nMOS (e.g., n-type metal oxide semiconductor field effect transistor (MOSFET)) or other n-type transistors. One or more of the first current source 120 and/or the current mirror 122 may be pMOS or other p-type transistors. The one or more of the first current sink 110, the second current sink 112, the first transistor 114, the second transistor 116, and/or the third transistor 118 may be the same or different (e.g., same or different widths, lengths, dopings, geometries, etc.). The one or more of the first current source 120 and/or the current mirror 122 may be p-type transistors may be the same or different (e.g., same or different widths, lengths, dopings, geometries, etc.).

[0021] In certain aspects, the slopes, curvatures, and/or shapes of the current vs. temperature behavior of the hybrid current I_{Hyb} may vary according to some aspects of the present disclosure.

[0022] Referring to FIG. 2, an example of the hybrid circuit 100, including one implementation of input current circuitry, is configured to provide a PTC current at temperatures above a threshold temperature and a ZTC current at temperature below the threshold temperature. The hybrid circuit 100 may include a ZTC current source 202, which is an example of the ZTC current source 102 that provides constant current as temperatures change. The hybrid circuit 100 may include a PTC current source 204, which is an example of the PTC current source 104 that provides current that increases with temperature.

[0023] In an aspect, it may be desirable to manage signal levels in On Off Keying (OOK) transmission across an isolation barrier. For example, it may be desirable to compensate for transmission transformer loss at temperatures above the threshold temperature T_{TH} and/or reduce reception signal loss at temperature below the threshold temperature T_{TH}. Specifically, a ZTC current source operating alone may provide a constant current below and above the threshold temperature T_{TH}. However, as temperatures rise, the transformer loss may increase with the operating temperature. Since the current provided by the ZTC current source remains constant with temperature, the ZTC current source may be unable to compensate for the transmission transformer loss at temperatures above the threshold temperature T_{TH}. Similarly, a PTC current source operating alone may provide a current that changes with temperature. As temperatures drop, the current provided by the PTC current source may decrease accordingly. This may cause reception signal loss at temperature below the threshold temperature T_{TH}. Aspects of the present disclosure include the hybrid circuit 100 configured to provide a constant current at temperatures below the threshold temperature T_{TH} and a variable temperature at temperatures above the threshold temperature T_{TH}.

[0024] Referring to FIG. 3, an example of the hybrid circuit 300 configured to provide a source current with

variable slopes at temperatures below and above the threshold temperature T_{TH}. The hybrid circuit 300 may be configured to provide variable bias currents, such as but not limited to bias currents with different temperature coefficients (TCs) (i.e., rate of current change as a function of temperature change). For example, the hybrid circuit 300 may include a first TC current source 304-1 configured to provide a first TC current I_{TC}-1, a second TC current source 304-2 configured to provide a second TC current I_{TC-2}... and an *n*th TC current source 304-n configured to provide an nth TC current I_{TC-n}. Here, n may be a positive integer greater than 1. In some aspects, the hybrid circuit 300 may have two or more TC current sources with different TCs.

[0025] In some aspects of the present disclosure, the hybrid circuit 300 may include a multiplexer/combining circuit 350 configured to select one or more of the currents provided by the first TC current source 304-1, the second TC current source 304-2... and/or the *n*th TC current source 304-n. The currents that are selected may be determined by indications provided to the multiplexer/combining circuit 350. For instance, the selected input currents may have different slopes above and/or below the threshold temperature T_{TH}. The hybrid circuit 300 may include a output 360 configured to output a hybrid current I_{Hyb} including a selected PTC current I_{S-PTC} and a selected ZTC current I_{S-ZTC}. The selected PTC current I_{S-PTC} may include one or some combination of the first TC current I_{TC-1}, the second TC current I_{TC-2}... the *n*th TC current I_{TC-n}. The selected ZTC current I_{S-ZTC} may include one or some combination of the first TC current I_{TC-1}, the second TC current I_{TC-2}... the *n*th TC current I_{TC-n}. In some optional implementations, the multiplexer/combining circuit 350 may be configured to apply one or more gain factors to the one or more of the first TC current I_{TC-1}, the second TC current I_{TC-2}... the nth TC current I_{TC-n} prior to outputting the I_{Hyb} via the output 360. For example, the multiplexer/combining circuit 350 may amplify the magnitude of the currents prior to outputting the I_{Hyb} via the output 360.

[0026] In an aspect, the hybrid circuit 300 may additionally include a decision circuit 352 configured to provide one or more indication signals to the multiplexer/combining circuit 350 for indicating the selection of the one or some combination of the currents provided by the first TC current source 304-1, the second TC current source 304-2... and/or the nth TC current source 304-n. The decision circuit 352 may optionally include one or more analog-to-digital converter (ADC). For example, the decision circuit 352 may receive analog input and output digital control signals. The decision circuit 352 may include logic, functions, or algorithms used to control how the multiplexer/combining circuit 350 generates the I_{Hyb} from one or some combination of the first TC current source 304-1, the second TC current source 304-2... and/or the nth TC current source 304-n. For example, the decision circuit 352 may utilize an input 355 from a temperature sensor 354, e.g., for temperature-dependent generation of the output 360 and/or one or more optional inputs 353, to generate the indication signals. The one or more optional inputs 353 may include, but are not limited to, desired slopes of the current above and/or below the threshold temperature T_{TH}. Based on the desired slopes, the decision circuit 352 may control the multiplexer/combining circuit 350 to select one or more of the currents provided by the first TC current source 304-1, the second TC current source 304-2... and/or the nth TC current source 304-n.

[0027] Referring to FIG. 4, example graphs 400 include example characteristics of the hybrid circuit 100 shown in Figs. 1 and 2, the hybrid circuit 300 shown in Fig. 3, and/or a p-type hybrid circuit 500 shown in Fig. 5 (below), including current versus temperature characteristic graphs 402 and corresponding temperature coefficient versus temperature characteristic graphs 404, which may be utilized in any of the aspects of the hybrid circuits described herein. In some instances, the temperature coefficients versus temperature characteristics may be derived based on the slope values of the current versus temperature characteristics (i.e., indicating the instantaneous change in the current versus temperature characteristics).

[0028] In some cases, a first current graph 410, which may be the same as or similar to graph 146, may illustrate a hybrid circuit output current based on a ZTC current having a zero slope over a first temperature range, and a PTC current having a positive slope over a second temperature range. A second current graph 412 may illustrate a hybrid circuit output current based on a ZTC current having a zero slope over some temperatures, and two PTC currents having different slopes over other temperatures. A third current graph 414 may illustrate a hybrid circuit output current based on a ZTC current having a first positive slope over some temperatures, and a PTC current having a second positive slope larger than the first positive slope over other temperatures. A fourth current graph 416 may illustrate a hybrid circuit output current based on a ZTC current having a first variably positive slope over some temperatures, and a PTC current having a second variably positive slope over other temperatures. The fourth current graph 416 may illustrate an example of a hybrid circuit having gradual (non-abrupt) transition between a ZTC current having a first zero or positive slope and a PTC current having a second positive slope larger than the slope of the ZTC current.

[0029] In some aspects of the present disclosure, a first TC graph 420 may illustrate the TC curve corresponding to the hybrid circuit output current in the first current graph 410. The first TC graph 420 shows that the slope of the ZTC current is zero and the slope of the PTC current is a positive number. A second TC graph 422 may illustrate the TC curve corresponding to the hybrid circuit output current in the second current graph 412. The second TC graph 422 shows that the slope of the ZTC current is zero and the slope of the PTC current increases with tempera-

tures in a first temperature range and remains a positive number in a second temperature range. A third TC graph 424 illustrates the TC curve corresponding to the hybrid circuit output current in the third current graph 414. The third TC graph 424 shows that the slope of the ZTC current is a first positive number and the slope of the PTC current is a second positive number larger than the first positive number. A fourth TC graph 426 illustrates the TC curve corresponding to the hybrid circuit output current in the fourth current graph 416. The fourth TC graph 426 shows that the slope of the ZTC current increases with temperature, and the slope of the PTC current increases with temperatures in a first temperature range and remains a positive number in a second temperature range.

[0030] Other current and/or TC profiles may also be implemented according to aspects of the present disclosure.

[0031] Referring to FIG. 5, an example of a p-type hybrid circuit 500 is configured to provide a PTC current at temperatures above a threshold temperature and a ZTC current at temperature below the threshold temperature. The p-type hybrid circuit 500 may include a PTC current source 502 configured to sink the PTC current I_{PTC} from the p-type hybrid circuit 500. The p-type hybrid circuit 500 may include a ZTC current source 504 configured to sink the ZTC current I_{ZTC} from the p-type hybrid circuit 500. The p-type hybrid circuit 500 may include a first P current source 550 configured to source the ZTC current I_{ZTC} toward the ZTC current source 504. The p-type hybrid circuit 500 may include a first P transistor 552 configured to provide a first P current I_{P-1}, which may be the minimum of the PTC current I_{PTC} and the ZTC current I_{ZTC}. The p-type hybrid circuit 500 may include a first P current mirror 554 configured to provide a third P current I_{P-3} that mirrors the ZTC current I_{ZTC} sourced by the first P current source 550. The third P current I_{P-3} may have the same magnitude as the ZTC current I_{ZTC}. The first p current source 550 may be disposed in series, parallel, or other configurations with respect to the ZTC current source 504.

[0032] In certain aspects of the present disclosure, the p-type hybrid circuit 500 may include a second P transistor 556 configured to provide a variable current ranging from zero to a differential current between the PTC current I_{PTC} and the ZTC current I_{ZTC} as described in further details below. The p-type hybrid circuit 500 may include a second P current mirror 558 configured to provide a second P current I_{P-2} that mirrors the variable current provided by the second P transistor 556.

[0033] During normal operation, in certain aspects, the first P current source 550 may provide the ZTC current I_{ZTC} in response to the ZTC current source 504. Because the drain terminal and the gate terminal of the first P current source 550 are connected, the first P current source 550 may operate in the saturation regime and a fourth gate voltage at a fourth gate terminal 560 may be developed on the drain terminal and the gate terminal of the first P current source 550. Consequently, the fourth gate voltage may be applied to the fourth gate terminal 560, including the gate terminals of the first P transistor 552 and/or the first P current mirror 554. As a result, the first P current mirror 554 may source the third P current I_{P-3}.

[0034] In some aspects of the present disclosure, as shown in a graph 590, for temperatures above a P threshold temperature T_{P-TH}, the PTC current I_{PTC} may be larger than the ZTC current I_{ZTC}. The PTC current I_{PTC} may induce a fifth gate voltage at the fifth gate terminal 562. Since the PTC current I_{PTC} is larger than the ZTC current I_{ZTC}, the fifth gate voltage may turn on the second P transistor 556 because the first P current I_{P-1} (having a current magnitude equaling to the ZTC current I_{ZTC}) is insufficient to supply the PTC current I_{PTC} alone. The fifth gate voltage may turn on the second P transistor 556 such that the second P transistor 556 supplies the differential current between the PTC current I_{PTC} and the ZTC current I_{ZTC}. Consequently, the second P current mirror 558 may mirror the second P transistor 556 and supply the second P current I_{P-2} (having the same magnitude as the differential current $I_{PTC} - I_{ZTC}$). Therefore, the second P current I_{P-2} may equal to the differential current of $I_{PTC} - I_{ZTC}$ and the third P current I_{P-3} may equal to the ZTC current I_{ZTC}. As a result, the hybrid current I_{Hyb} may equal to the sum of the second P current I_{P-2} and the third P current I_{P-3}, which is the PTC current I_{PTC}. In other words, for temperatures above the P threshold temperature T_{P-TH}, the hybrid current I_{Hyb} is equal to the PTC current I_{PTC}.

[0035] In other aspects of the present disclosure, for temperature below the P threshold temperature T_{P-TH}, the ZTC current I_{ZTC} may be larger than the PTC current I_{PTC}. As such, the first P transistor 552 may supply the ZTC current I_{ZTC} as the first P current I_{P-1}. Consequently, the fifth gate voltage may remain "high" to keep the second P transistor 556 off. The second P current mirror 558 may similarly remain in the off state and supply no current as the second P current I_{P-2}. As a result, the hybrid current I_{Hyb} may equal to the sum of the second P current I_{P-2} and the third P current I_{P-3}, which is the ZTC current I_{ZTC}. In other words, for temperatures below the P threshold temperature T_{P-TH}, the hybrid current I_{Hyb} is equal to the ZTC current I_{ZTC}.

[0036] In some aspects, the hybrid current I_{Hyb} provided by the hybrid circuit 100 may exhibit characteristics shown in the graph 590. At temperatures below the P threshold temperature T_{P-TH}, the hybrid current I_{Hyb} may be constant with temperature. At P threshold temperature T_{P-TH}, the hybrid current I_{Hyb} may increase with temperature. The hybrid current I_{Hyb} may be the maximum current of the PTC current I_{PTC} and the ZTC current I_{ZTC}.

[0037] FIG. 6 includes example graphs 601 and 605 of current versus temperature behaviors of a scalable PTAT hybrid circuit according to aspects of the present disclosure. Referring to graph 601, in certain aspects, a scal-

able PTAT hybrid circuit (described below in FIG. 7) may output a hybrid current exhibiting a first current versus temperature behavior 600 without PTAT scaling. In some aspects, the scalable PTAT hybrid circuit may perform a negative PTAT scaling such that the hybrid current is shifted to exhibit a second current versus temperature behavior 602. The second current versus temperature behavior 602 may be the first current versus temperature behavior 600 being shifted negatively by ΔI_1. In other words, at a temperature t_1, the current level of the first current versus temperature behavior 600 (without PTAT scaling) is ΔI_1 higher than the current level of the second current versus temperature behavior 602 (due to the negative PTAT scaling).

[0038] Still referring to graph 601, in certain aspects, the scalable PTAT hybrid circuit may perform a positive PTAT scaling such that the hybrid current is shifted to exhibit a third current versus temperature behavior 604. The third current versus temperature behavior 604 may be the first current versus temperature behavior 600 being shifted positively by ΔI_2. In other words, at a temperature t_1, the current level of the first current versus temperature behavior 600 (without PTAT scaling) is ΔI_2 lower than the current level of the third current versus temperature behavior 604 (due to the positive PTAT scaling).

[0039] Referring to graph 605, in some aspects of the present disclosure, the first current versus temperature behavior 600 of the PTAT hybrid circuit may have a slope of m_1 in the positive temperature coefficient regime (without slope control). In an aspect of the present disclosure, the PTAT hybrid circuit may increase the slope of the output hybrid circuit to exhibit a fourth current verses temperature behavior 606 having a slope of m_4 in the positive temperature coefficient regime. In another aspect, the PTAT hybrid circuit may decrease the slope of the output hybrid circuit to exhibit a fifth current verses temperature behavior 608 having a slope of m_5 in the positive temperature coefficient regime.

[0040] In some aspects of the present disclosure, the PTAT hybrid circuit may perform both the PTAT scaling and the slope control.

[0041] FIG. 7 shows an example of a scalable PTAT hybrid circuit 700 configured to scale the current magnitude of a hybrid current, and/or adjust the slope of the hybrid current in the temperature dependent regime. In certain implementations, a scalable PTAT hybrid circuit 700 may include a bias mirror circuit 702 configured to provide currents to the remaining portions of the scalable PTAT hybrid circuit 700. The bias mirror circuit 702 may include a ZTC current source 704 configured to provide a ZTC current (I_{ZTC}). The scalable PTAT hybrid circuit 700 may include a PTAT control circuit 720 configured to scale a magnitude of a hybrid current (I_{HYB}) and/or a slope of the PTAT current (I_{PTAT}). In some implementations, the PTAT control circuit 720 may be configured to provide the I_{PTAT}. The scalable PTAT hybrid circuit 700 may include a hybrid circuit 770 configured to combine the I_{ZTC} and the I_{PTAT} to provide the I_{HYB}.

[0042] In some aspects, the PTAT control circuit 720 may include a first resistor R_1. The PTAT control circuit 720 may include a first transistor T_1. The PTAT control circuit 720 may include a second transistor T_2. The PTAT control circuit 720 may include a second transistor R_2. The R_1, T_1, T_2, and R_2 may be configured to determine the magnitude and/or slope of the I_{PTAT}. The PTAT control circuit 720 may include a slope control circuit 730 configured to control the slope of the current versus temperature behaviors of the hybrid current as described in FIG. 6 and below.

[0043] In some aspects, the PTAT control circuit 720 may include a bandgap circuit 740 including a second bipolar junction transistor (BJT) Q2, and a third BJT Q3. The bandgap circuit 740 may optionally include a base current cancellation circuit BCC configured to prevent the base currents of the Q2 and/or Q3 from interfering with the slope of the I_{PTAT}. The bandgap circuit 740 may be configured to generate at least a portion of the I_{PTAT}.

[0044] The slope control circuit 730 may include a third resistor R_3 and a fourth resistor R_4. The resistances of the R_3 and R_4 may determine the voltages at V_3 and/or V_4, which controls the amount of current flow through Q1 and/or Q2. The R_3 and R_4 may be variable resistors.

[0045] In optional aspects, the scalable PTAT hybrid circuit 700 may include an optional bias-gain circuit 750 configured to keep collector voltages V_{C1}, V_{C2} of the Q2 and Q3 constant.

[0046] In some aspects, the PTAT control circuit 720 may include first source transistors 722 configured to provide first source current ($I_{SOURCE-1}$). The PTAT control circuit 720 may include second source transistors 732 configured to provide a second source current ($I_{SOURCE-2}$). The PTAT control circuit 720 may include third source transistors 734 configured to provide a third source current ($I_{SOURCE-3}$).

[0047] During operation, the bias mirror circuit 702 may be configured to induce the $I_{SOURCE-1}$ into the PTAT control circuit 720 via first source transistors 722 of the PTAT control circuit 720. A first voltage V_1 may appear across the first resistor R_1. The first resistor R_1 may be a variable resistor ranging from 0 S2 to 10 kiloohms (kQ), for example 1.8 kS2, 2 kS2, 2.2 kS2.

[0048] In one example, the first source current $I_{SOURCE-1}$ may be approximately 50 microamps (μA), the first voltage drop V_{R1} may be 100 millivolts (mV), and the first resistor R_1 may be 1.8 kS2.

[0049] In some aspects, the first source current $I_{SOURCE-1}$ may flow through the first transistor T_1. A second voltage V_2 induced by the first source current $I_{SOURCE-1}$ may be applied to the gate of the first transistor T_1. As a result, the first transistor T_1 may be a triode device exhibiting linear current behavior. The second voltage V_2 may be applied to the gate of the second transistor T_2. As a result, the second transistor T_2 may be a triode device exhibit linear current behavior. Other devices may also be used to apply the second voltage V_2. The first transistor

T_1 and the second transistor T_2 may be matched (e.g., same size). The ratio of the sizes of the T_1 and the T_2 may determine the slope and/or scaling of the I_{HYB}.

[0050] In some aspects, the bandgap circuit 740 may operate as described below. The $I_{SOURCE-1}$, and therefore, the second voltage V_2, may induce the $I_{SOURCE-2}$ through second source transistors 732, the second BJT Q2, and the second transistor T_2. Similarly, the $I_{SOURCE-1}$ and the second voltage V_2 may induce the $I_{SOURCE-3}$ flowing through third source transistors 734 and the third BJT Q3. A second base-emitter voltage V_{BE-2} may be developed across the second BJT Q2 due to the $I_{SOURCE-2}$. A third base-emitter voltage V_{BE-3} may be developed across the third BJT Q3 due to the $I_{SOURCE-3}$. A difference in voltage ΔV between the V_{BE-2} and the V_{BE-3} may be generated due to one or more of a difference in the dimensions (e.g., emitter area) of the second BJT Q2 and the third BJT Q3, and/or a difference between the $I_{SOURCE-2}$ and the $I_{SOURCE-3}$. Individually, the V_{BE-2} and the V_{BE-3} are inversely proportional to temperature (i.e., as temperature increases, the corresponding voltage decreases) due to the P-N junction diode formed between the base and the emitter. Specifically, as temperature increases, the number of carriers injected increases, requiring less voltage to drive the same current. The difference in the base-emitter voltages ($|V_{BE-2} - V_{BE-3}|$, aka ΔV) is proportional to temperature (i.e., as temperature increases, the difference in voltage increases). Therefore, as temperature increases, the ΔV increases.

[0051] In some aspects, the third voltage V_3 may be an improper fraction multiple (e.g., $\sim(R_3 + R_4)/R_4$) of ΔV. As the ΔV increases (e.g., due to temperature), the third voltage V_3 decreases.

[0052] In certain aspects, the $I_{SOURCE-3}$ may be mirrored by the hybrid circuit 770 to generate the I_{PTAT} as described above. The ratio of the $I_{SOURCE-2}$ and the $I_{SOURCE-3}$ may be determined by one or more of the sizes of the Q2 and Q3, and/or the sizes of the second source transistors 732 and the third source transistors 734.

[0053] In certain aspects, the bias-gain circuit 750 may lock the collector voltages (Vci and V_{C2}) to match for the operation of the bandgap circuit 740. Alternatively or additionally, the bias-gain circuit 750 may provide the base currents to one or more of the Q2 and/or Q3. In some aspects, the bias-gain circuit 750 may prevent the introduction of undesirable temperature coefficients during the biasing of the bandgap circuit 740.

[0054] According to an aspect of the present disclosure, as the I_{ZTC} changes in current magnitude, the I_{PTAT} will change accordingly. Referring to FIGs. 6 and 7, the I_{ZTC} in the hybrid circuit 700 for the first current versus temperature behavior 600 may change in current magnitude (i.e., shift up or increase in current magnitude, or shift down or decreases in current magnitude). During a change in I_{ZTC} in the bias mirror circuit 702, the $I_{SOURCE-1}$ may change accordingly (i.e., a decrease in I_{ZTC} leads to a decrease in $I_{SOURCE-1}$, and vice versa). As the $I_{SOURCE-1}$ changes, the R_1 and/or R_2 may change correspondingly. As a result, the $I_{SOURCE-2}$ may change, which leads to a change in the I_{PTAT}.

[0055] For example, if the I_{ZTC} decreases in the bias mirror circuit 702, the $I_{SOURCE-1}$ may decrease accordingly. The decrease in the $I_{SOURCE-1}$ may lead to an increase in the R_1 / T_1 pair resistance because voltage drop across the R_1 may remain approximately constant due to a first BJT Q1 (i.e., V_1 remains unchanged). As a result, the R_2 may increase correspondingly, causing an decrease to the $I_{SOURCE-2}$. Consequently, I_{PTAT} may decrease.

[0056] In another aspect of the present disclosure, the slope of the hybrid current in the positive temperature coefficient regime may be controlled by selecting the temperature coefficient of the first voltage V_1, which causes the resistance of the R_1 to scale with temperature. The first voltage V_1 may be determined by the values of the third resistor R_3 and/or the fourth resistor R_4 of the slope control circuit 730.

[0057] In some implementations, the R_1, R_2, R_3, and R_4 may be polysilicon variable resistors.

[0058] In an aspect of the present disclosure, V_1 may provide a reference voltage. In the current example, V_1 is generated on-chip via Q1. However, in some implementations, V_1 may be provided off-chip. V_1 may be a digital input. Other schemes to generate reference voltage and/or reference current may also be used according to aspects of the present disclosure. $I_{SOURCE-1}$ and/or V_1 may include a temperature coefficient. The triode FETs (i.e., the first transistor T1 and the second transistor T2) may be the tuning elements that change the pair resistance of R1 / T1 and/or the pair resistance of R2 / T2. The temperature dependency of $I_{SOURCE-1}$ and/or V_1 may be transferred to $I_{SOURCE-2}$ and/or $I_{SOURCE-3}$ via V_2.

[0059] In optional aspects of the present disclosure, the temperature dependency of I_{PTAT} may originate from the temperature dependencies of R_1 and/or R_2. In one aspect, the size difference between Q2 and Q3 may cause a difference in V_{BE-2} and V_{BE-3}. The difference in the voltages may appear across R2, which generates the temperature dependency of I_{PTAT}.

[0060] In some aspects of the present disclosure, the slope control circuit 730 may control V_4. The ratios of R_3 and R_4 may determine the voltage value of V_4, which may change the voltage value of V_2. V_3 may track V_{BE-2} and/or V_{BE-3}.

[0061] An example of analysis of the first voltage V_1 may be as follow:

$$V_{R2} = \Delta V = V_T \text{ x } \ln (n \text{ x } m)$$

[0062] Here, V_{R2} is the voltage drop across the R_2, $V_T = kT/q$, T is the temperature, q is the electronic charge, n is the ratio of the sizes of the Q2 to the Q3, and m is the ratio of the sizes of the two or more second source transistors to the two or more third source transistors. Further,

$$V_{BE\text{-}1} \approx V_{BE\text{-}2} = V_4 - V_{BE\text{-}2}$$

$$V_{BE\text{-}1} = V_3 - V_1$$

$$V_4 = V_{R2} + V_{T2} + V_{BE\text{-}2}, \text{ wherein } V_4 = V_{BE\text{-}3}$$

$$V_3 = V_4 \left(\frac{R_3 + R_4}{R_4}\right)$$

$$V_1 = V_3 - V_{BE\text{-}1} = V_{BG.}$$

[0063] Here, V_4 may be the voltage between the R_3 and R_4, and $V_{BE\text{-}1}$ may be the emitter-base voltage for Q1. $V_{BE\text{-}1}$ is substantially constant except as adjusted by R_3 to trim the slope of the hybrid current I_{Hyb} (example shown in the graph 605 of FIG. 6). By simplifying the equation above:

$$V_1 = \frac{R_3}{R_4} \text{ x } V_{BG},$$

where V_{BG} is the bandgap voltage of Q2.

[0064] Turning to FIG. 8, a method 800 of providing a hybrid current may be performed by the scalable PTAT hybrid circuit 700.

[0065] At block 805, the method 800 may provide a zero temperature coefficient (ZTC) current. For example, the bias mirror circuit 702 may provide a zero temperature coefficient (ZTC) current.

[0066] At block 810, the method 800 may generate, based on the ZTC current, a PTAT current with a slope having a non-zero value. For example, the PTAT control circuit 720 and/or the bandgap circuit 740 may generate, based on the ZTC current, a PTAT current with a slope having a non-zero value.

[0067] At block 815, the method 800 may provide a reference voltage to alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current. For example, the PTAT control circuit 720, the Q1, the R1, T1, and/or the slope control circuit 730 may provide V_1 (generated from dividing $I_{SOURCE\text{-}1}$ by R_1 to control the resistance(s) of R_2 and/or T2 to alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current.

[0068] At block 820, the method 800 may output a larger current of the ZTC current and the altered PTAT current as a hybrid current. For example, the hybrid circuit 770 may output a larger current of the ZTC current and the altered PTAT current as a hybrid current.

[0069] FIG. 9 illustrates examples of current supplies according with aspects of the present disclosure. The current supply 900 includes a resistor with a resistance of R, and a transistor have a dimension of W/L. When the gate voltage is applied, a current that is proportional to [1/R x W/L] flows through the transistor. The current supply 910 includes a variable resistor with a resistance of R/N, and a transistor have a dimension of W/L. When the gate voltage is applied, a current that is proportional to [N/R x W/L] flows through the transistor. Here N may be changed during the operation of the bias circuits described above to change the current supplied.

[0070] FIG. 10 illustrates another example of a circuit 1000 configured as a variable resistor according to aspects of the present disclosure. Here, an input voltage of V_{REF} is applied to an op-amp, which supplies the gate voltage of the transistor. A drain current of I_{REF} flows through the transistor, where the drain current I_{REF} is a function of the input voltage V_{REF}. In a first regime of operation, I_{REF} may be linearly proportional to V_{REF} (i.e, linear regime). In a second regime of operation, V_{REF} may exceed the saturation voltage of the transistor, and I_{REF} may be constant as V_{REF} increases. As such, the circuit 1000 has an output behavior that emulates a variable resistor, where the effective variable resistance $R = \frac{V_{REF}}{I_{REF}}$. Here, the effective variable resistance varies with V_{REF} while I_{REF} remains substantially constant.

[0071] FIG. 11 illustrates additional examples of variable resistors according to aspects of the present disclosure. A variable resistor circuit 1100 may operate in the triode operation. Here, the field effect transistor may operate under the condition where $|V_{GS} - V_T| \gg V_{DS}$. During the triode operation, $\frac{V_{DS}}{I_D} \approx R_{DS}$ or, equivalently, $V_{DS} \approx I_D R_{DS}$. As shown in the graph 1102, R_{DS} operates as a variable resistor in the resistive range. Here, the resistance of the transistor between the drain and the source is a variable resistor that is a function of the applied gate to source voltage.

[0072] Similarly, in some aspects of the present disclosure, a variable resistor circuit 1110 may include a built-in fixed resistor in series with the transistor. In some instances, having a built-in fixed resistor may extend the resistive range of the variable resistor circuit 1110 as shown in the graph 1112. In certain aspects, by adding the fixed resistor in series, the linearity may be improved over temperature and/or process. Either type of variable resistor circuits shown in FIG. 11 may be implemented in the bias temperature circuit according to aspects of the present disclosure.

[0073] FIG. 12 illustrates an example of a PTAT generator 1200 according to aspects of the present disclosure. Referencing FIGs. 7 and 12, the PTAT generator 1200 may be an implementation of the slope control circuit 730 and the bandgap circuit 740. Here, V_4 may equal to the base-emitter voltage (V_{BE}) of the third BJT

Q3. V_3 may equal to $V_{BE}\left(\frac{R_4}{R_3+R_4}\right)$.

[0074] FIG. 13 illustrates an example of a PTAT generator 1300 with one or more variable resistors according to aspects of the present disclosure. Referencing FIGs. 7 and 13, the PTAT generator 1300 may be an implementation of the slope control circuit 730 and the bandgap circuit 740. Here, the reference voltage may be derived as follows. V_3 may be calculated as $1 + KV_{BE\text{-}3}$. The voltage V_5 may be calculated as $(1 + K)(V_{BE\text{-}3} - V_{BE\text{-}2})$, which may be simplified to $(1 + K)\Delta V_{BE}$. The expression may be further simplified to $V_1 = KV_{BE} + \Delta V_{BE}$, which is the bandgap type reference voltage according to aspects of the present disclosure.

[0075] Aspects of the present disclosure include a scalable proportional-to-absolute-temperature (PTAT) hybrid circuit, including a bias mirror circuit configured to provide a zero temperature coefficient (ZTC) current, a PTAT control circuit configured to generate, based on the ZTC current, a PTAT current with a slope having a non-zero value, to alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current, and to output a larger current of the ZTC current and the altered PTAT current as a hybrid current.

[0076] Aspects of the present disclosure include the PTAT hybrid circuit above, wherein the bias mirror circuit comprises a ZTC current source.

[0077] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the PTAT control circuit comprises two or more first source transistors configured to provide a first source current through a first bipolar junction transistor (BJT), a first variable resistor, and a first transistor.

[0078] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the PTAT control circuit further comprises the first BJT, the first variable resistor, and the first transistor, wherein the first BJT, the first variable resistor, and the first transistor are connected in series.

[0079] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the PTAT control circuit further comprises a slope control circuit configured to change the slope of the PTAT current.

[0080] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the slope control circuit comprises a second transistor, a second variable resistor, and a third variable resistor, wherein the second transistor, the second variable resistor, and the third variable resistor are connected in series.

[0081] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein a drain of the second transistor is connected to a base of the first BJT.

[0082] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the PTAT control circuit comprises a bandgap circuit configured to generate the PTAT current.

[0083] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the bandgap circuit comprises a first bipolar junction transistor (BJT) and a second BJT, wherein a first gate of the first BJT is connected to a second gate of the second BJT.

[0084] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the bandgap circuit comprises a base current cancellation circuit.

[0085] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the PTAT control circuit further comprises a bias gain circuit.

[0086] Aspects of the present disclosure include a scalable proportional-to-absolute-temperature (PTAT) hybrid circuit, comprising a bias mirror circuit having a zero temperature coefficient (ZTC) current source configured to induce a ZTC current, a PTAT control circuit having two or more first source transistors, a first BJT connected to one of the two or more first source transistors, a first variable resistor connected to the first BJT, a first transistor connected to the first variable resistor, wherein the first BJT, the first variable resistor, and the first transistor are connected in series, a second transistor, a second variable resistor connected to a drain terminal of the second transistor and a first base of the first BJT, a third variable resistor connected to the second variable resistor, wherein the second transistor, the second variable resistor, and the third variable resistor are connected in series, a bandgap circuit having a second BJT and a third BJT, wherein a second base of the second BJT and a third base of the third BJT are connected to the second variable resistor and the third variable resistor, a fourth variable resistor connected to the second BJT of the bandgap circuit, and a third transistor connected to the fourth variable resistor, and a hybrid circuit.

[0087] Aspects of the present disclosure include the PTAT hybrid circuit above, further including two or more second source transistors, wherein a drain of one of the two or more source transistors is connected to a second collector of the second BJT.

[0088] Aspects of the present disclosure include any of the PTAT hybrid circuits above, further including two or more third source transistors, wherein a drain of one of the two or more source transistors is connected to a third collector of the third BJT.

[0089] Aspects of the present disclosure include any of the PTAT hybrid circuits above, further comprising a base current cancellation circuit connected to the second base of the second BJT and the third base of the third BJT.

[0090] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein the first transistor and the third transistor are matched in size.

[0091] Aspects of the present disclosure include any of the PTAT hybrid circuits above, wherein a first width of the second BJT is twice a second width of the third BJT.

[0092] Aspects of the present disclosure include any of the PTAT hybrid circuits above, further comprising a bias gain circuit.

[0093] Aspects of the present disclosure include any of

the PTAT hybrid circuits above, wherein the first variable resistor, the second variable resistor, the third variable resistor, and the fourth variable resistor are polysilicon variable resistors.

[0094] Aspects of the present disclosure include a method of providing a hybrid current by a scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising: providing a zero temperature coefficient (ZTC) current, generating, based on the ZTC current, a PTAT current with a slope having a non-zero value, altering the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current, and outputting a larger current of the ZTC current and the altered PTAT current as a hybrid current.

[0095] Aspects of the present disclosure include a hybrid circuit, including a first current sink configured to sink a zero temperature coefficient (ZTC) current provided by a ZTC current source, a second current sink configured to sink a positive temperature coefficient (PTC) current provided by a PTC current source, a first transistor configured to provide a first current having a first current magnitude of zero in response to the ZTC current being larger than the PTC current or a second current magnitude of a difference between the PTC current and the ZTC current in response to the PTC current being larger than the ZTC current, a second transistor configured to provide a second current having a third current magnitude of the ZTC current in response to the PTC current being larger than the PTC current or a fourth current magnitude of the PTC current in response to the ZTC current being larger than the ZTC current, a third transistor configured to provide a third current mirroring the ZTC current, a fourth transistor configured to provide a sum current of the first current and the third current, and a current mirror configured provide a hybrid current mirroring the sum current.

[0096] Aspects of the present disclosure include the aspect above, further including the ZTC current source and the PTC current source.

[0097] Aspects of the present disclosure include any of the aspects above, wherein the ZTC current source comprises a plurality of current sources configured to each provide a corresponding source current having a different temperature coefficient of a plurality of temperature coefficients.

[0098] Aspects of the present disclosure include any of the aspects above, wherein the PTC current source comprises a plurality of current sources configured to each provide a corresponding source current having a different temperature coefficient of a plurality of temperature coefficients.

[0099] Aspects of the present disclosure include any of the aspects above, further including a plurality of current sources configured to each provide a corresponding source current having a different temperature coefficient of a plurality of temperature coefficients.

[0100] Aspects of the present disclosure include any of the aspects above, further including a multiplexer configured to receive one or more source currents of the plurality of current sources, combine the one or more source currents as a combined current, and output the combined current as the PTC current or the ZTC current.

[0101] Aspects of the present disclosure include any of the aspects above, further including a temperature sensor configured to measure a temperature associated with the hybrid circuit, and output an indication indicating the temperature measured by the temperature sensor.

[0102] Aspects of the present disclosure include any of the aspects above, further including a decision circuit configured to select the one or more source currents based at least partially on the indication.

[0103] Aspects of the present disclosure include a hybrid circuit including a first current sink connected to a zero temperature coefficient (ZTC) current source, corresponding gate terminals of a second transistor and a third transistor, and a ground terminal, a second current sink connected to a positive temperature coefficient (PTC) current source, a corresponding gate terminal of a first transistor, and the ground terminal, the first transistor connected to a corresponding drain terminal of the second transistor, a corresponding drain terminal of the third transistor, a corresponding drain terminal of a fourth transistor, and the ground terminal, the second transistor connected to the ZTC current source, the PTC current source, a corresponding gate terminal of the first current sink, a corresponding gate terminal of the second current sink, the corresponding gate terminal of the first transistor, the corresponding gate terminal of the third transistor, and the ground terminal, the third transistor connected to the ZTC current source, the corresponding gate terminal of the first current sink, the corresponding gate terminal of the second transistor, a corresponding drain terminal of the first transistor the corresponding drain terminal of the fourth transistor, and the ground terminal, the fourth transistor connected to a voltage supply, a corresponding gate terminal of a current mirror, the corresponding drain terminal of the first transistor, and the corresponding drain terminal of the third transistor, the current mirror connected to the voltage supply.

[0104] Aspects of the present disclosure include the aspect above, wherein the first transistor is configured to provide a first current having a first current magnitude of zero in response to the ZTC current being larger than the PTC current, or a second current magnitude of a difference between the PTC current and the ZTC current in response to the PTC current being larger than the ZTC current.

[0105] Aspects of the present disclosure include any of the aspects above, wherein the second transistor is configured to provide a second current having a third current magnitude of the ZTC current in response to the PTC current being larger than the PTC current, or a fourth current magnitude of the PTC current in response to the ZTC current being larger than the ZTC current.

[0106] Aspects of the present disclosure include any of

the aspects above, wherein the fourth transistor is configured to provide a sum current of the first current and the third current.

[0107] Aspects of the present disclosure include any of the aspects above, wherein the current mirror is configured provide a hybrid current mirroring the sum current.

[0108] Aspects of the present disclosure include any of the aspects above, wherein the third transistor mirror is configured to provide a current mirroring the ZTC current.

[0109] Aspects of the present disclosure include any of the aspects above, further including a plurality of current sources connected to a multiplexer, the multiplexer connected one or more of a decision circuit or a temperature sensor, the decision circuit, and the temperature sensor.

[0110] Aspects of the present disclosure include any of the aspects above, wherein the plurality of current sources are configured to each provide a corresponding source current having a different temperature coefficient of a plurality of temperature coefficients.

[0111] Aspects of the present disclosure include any of the aspects above, wherein the multiplexer is configured to receive one or more source currents of the plurality of current sources, combine the one or more source currents as a combined current, and output the combined current as the PTC current or the ZTC current.

[0112] Aspects of the present disclosure include any of the aspects above, wherein the temperature sensor is configured to measure a temperature associated with the hybrid circuit, and output an indication indicating the temperature measured by the temperature sensor.

[0113] Aspects of the present disclosure include any of the aspects above, wherein the decision circuit is configured to select the one or more source currents based at least partially on the indication.

[0114] Aspects of the present disclosure include a method of providing a hybrid current including sinking, by a first current sink, a zero temperature coefficient (ZTC) current provided by a ZTC current source, sinking, by a second current sink, a positive temperature coefficient (PTC) current provided by a PTC current source, providing, by a first transistor, a first current having a first current magnitude of zero in response to the ZTC current being larger than the PTC current or a second current magnitude of a difference between the PTC current and the ZTC current in response to the PTC current being larger than the ZTC current, providing, by a second transistor, a second current having a third current magnitude of the ZTC current in response to the PTC current being larger than the PTC current or a fourth current magnitude of the PTC current in response to the ZTC current being larger than the ZTC current, providing, by a third transistor, a third current mirroring the ZTC current, providing, by a fourth transistor, a sum current of the first current and the third current, and providing, by a current mirror, a hybrid current mirroring the sum current.

[0115] The above detailed description set forth above in connection with the appended drawings describes examples and does not represent the only examples that may be implemented or that are within the scope of the claims. The term "example," when used in this description, means "serving as an example, instance, or illustration," and not "preferred" or "advantageous over other examples." The detailed description includes specific details for the purpose of providing an understanding of the described techniques. These techniques, however, may be practiced without these specific details. For example, changes may be made in the function and arrangement of elements discussed without departing from the scope of the disclosure. Also, various examples may omit, substitute, or add various procedures or components as appropriate. For instance, the methods described may be performed in an order different from that described, and various steps may be added, omitted, or combined. Also, features described with respect to some examples may be combined in other examples. In some instances, well-known structures and apparatuses are shown in block diagram form in order to avoid obscuring the concepts of the described examples.

[0116] Information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, computer-executable code or instructions stored on a computer-readable medium, or any combination thereof.

[0117] Several aspects of telecommunication systems will now be presented with reference to various apparatus and methods. These apparatus and methods will be described in the following detailed description and illustrated in the accompanying drawings by various blocks, components, circuits, processes, algorithms, etc. (collectively referred to as "elements"). These elements may be implemented using electronic hardware, computer software, or any combination thereof. Whether such elements are implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0118] By way of example, an element, or any portion of an element, or any combination of elements may be implemented as a "processing system" that includes one or more processors. Examples of processors include microprocessors, microcontrollers, graphics processing units (GPUs), central processing units (CPUs), application processors, digital signal processors (DSPs), reduced instruction set computing (RISC) processors, systems on a chip (SoC), baseband processors, field programmable gate arrays (FPGAs), programmable logic devices (PLDs), state machines, gated logic, discrete hardware circuits, and other suitable hardware configured to perform the various functionality described throughout this disclosure. One or more processors in the processing system may execute software. Software

shall be construed broadly to mean instructions, instruction sets, code, code segments, program code, programs, subprograms, software components, applications, software applications, software packages, routines, subroutines, objects, executables, threads of execution, procedures, functions, etc., whether referred to as software, firmware, middleware, microcode, hardware description language, or otherwise.

[0119] Accordingly, in one or more example embodiments, the functions described may be implemented in hardware, software, or any combination thereof. If implemented in software, the functions may be stored on or encoded as one or more instructions or code on a computer-readable medium. Computer-readable media includes computer storage media. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may comprise a random-access memory (RAM), a read-only memory (ROM), an electrically erasable programmable ROM (EEPROM), optical disk storage, magnetic disk storage, other magnetic storage devices, combinations of the aforementioned types of computer-readable media, or any other medium that may be used to store computer executable code in the form of instructions or data structures that may be accessed by a computer.

[0120] The various illustrative blocks and components described in connection with the disclosure herein may be implemented or performed with a specially-programmed device, such as but not limited to a processor, a digital signal processor (DSP), an ASIC, a FPGA or other programmable logic device, a discrete gate or transistor logic, a discrete hardware component, or any combination thereof designed to perform the functions described herein. A specially-programmed processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A specially-programmed processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0121] The functions described herein may be implemented in hardware, software executed by a processor, firmware, or any combination thereof. If implemented in software executed by a processor, the functions may be stored on or transmitted over as one or more instructions or code on a non-transitory computer-readable medium. Other examples and implementations are within the scope and spirit of the disclosure and appended claims. For example, due to the nature of software, functions described above may be implemented using software executed by a specially programmed processor, hardware, firmware, hardwiring, or combinations of any of these. Features implementing functions may also be physically located at various positions, including being distributed such that portions of functions are implemented at different physical locations. Also, as used herein, including in the claims, "or" as used in a list of items prefaced by "at least one of" indicates a disjunctive list such that, for example, a list of "at least one of A, B, or C" means A or B or C or AB or AC or BC or ABC (i.e., A and B and C).

[0122] Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage medium may be any available medium that may be accessed by a general purpose or special purpose computer. By way of example, and not limitation, computer-readable media may comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to carry or store desired program code means in the form of instructions or data structures and that may be accessed by a general-purpose or special-purpose computer, or a general-purpose or special-purpose processor. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, include compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above are also included within the scope of computer-readable media.

[0123] The previous description of the disclosure is provided to enable a person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the common principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Furthermore, although elements of the described aspects may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated. Additionally, all or a portion of any aspect may be utilized with all or a portion of any other aspect, unless stated otherwise. Thus, the disclosure is not to be limited to the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

Claims

1. A scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising:

a bias circuit configured to provide an input current;
a PTAT control circuit configured to:

generate, based on the input current, a PTAT current with a slope having a non-zero value,
provide a reference voltage to alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current, and
provide the altered PTAT current;

a hybrid circuit configured to:

receive a zero temperature coefficient (ZTC) current and the altered PTAT current; and
output a larger current of the ZTC current and the altered PTAT current as a hybrid current.

2. The scalable PTAT hybrid circuit of claim 1, wherein the PTAT control circuit is further configured to provide the reference voltage by controlling a resistance of one or more variable resistors.

3. The scalable PTAT hybrid circuit of claim 2, wherein the PTAT control circuit comprises two or more first source transistors configured to provide a first source current through a first bipolar junction transistor (BJT), a first variable resistor, and a first transistor.

4. The scalable PTAT hybrid circuit of claim 3, wherein the PTAT control circuit is further configured to control the resistance by:

controlling an amount of the first source current; and
mirroring a second source current through the one or more variable resistors.

5. The scalable PTAT hybrid circuit of claim 4, wherein the one or more variable resistors include a second variable resistor and a second transistor.

6. The scalable PTAT hybrid circuit of claim 5, wherein the first variable resistor and the second variable resistor maintain a substantially fixed ratio.

7. The scalable PTAT hybrid circuit of any of claims 3 to 6, wherein:

the PTAT control circuit further comprises a slope control circuit configured to change the slope of the PTAT current; and
the slope control circuit comprises:

a second transistor;
a second variable resistor; and
a third variable resistor, wherein the second transistor, the second variable resistor, and the third variable resistor are connected in series.

8. The scalable PTAT hybrid circuit of any preceding claim, wherein the PTAT control circuit is further configured to provide the reference voltage by supplying an external reference voltage.

9. The scalable PTAT hybrid circuit of any preceding claim, wherein the bias circuit comprises a ZTC current source configured to provide the ZTC current.

10. The scalable PTAT hybrid circuit of any preceding claim, wherein:

the PTAT control circuit comprises a bandgap circuit configured to generate the PTAT current;
the bandgap circuit comprises a first bipolar junction transistor (BJT) and a second BJT; and
a first gate of the first BJT is connected to a second gate of the second BJT.

11. The scalable PTAT hybrid circuit of claim 10, wherein the bandgap circuit comprises a base current cancellation circuit.

12. A scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising:

a bias mirror circuit having a zero temperature coefficient (ZTC) current source configured to induce a ZTC current;
a PTAT control circuit having:

two or more first source transistors;
a first BJT connected to one of the two or more first source transistors;
a first variable resistor connected to the first BJT;
a first transistor connected to the first variable resistor, wherein the first BJT, the first variable resistor, and the first transistor are connected in series;
a second transistor;
a second variable resistor connected to a drain terminal of the second transistor and a first base of the first BJT;
a third variable resistor connected to the second variable resistor, wherein the second transistor, the second variable resistor, and the third variable resistor are connected

in series;
a bandgap circuit having a second BJT and a third BJT, wherein a second base of the second BJT and a third base of the third BJT are connected to the second variable resistor and the third variable resistor;
a fourth variable resistor connected to the second BJT of the bandgap circuit; and
a third transistor connected to the fourth variable resistor; and

a hybrid circuit.

13. The PTAT hybrid circuit of claim 12, further comprising:

two or more second source transistors, wherein a drain of one of the two or more source transistors is connected to a second collector of the second BJT,
and optionally further comprising two or more third source transistors, wherein a drain of one of the two or more source transistors is connected to a third collector of the third BJT.

14. The PTAT hybrid circuit of claim 12 or claim 13, wherein at least one of the following applies:

(a) the PTAT hybrid circuit further comprises a base current cancellation circuit connected to the second base of the second BJT and the third base of the third BJT;
(b) the first transistor and the third transistor are matched in size;
(c) a first width of the second BJT is twice a second width of the third BJT;
(d) the PTAT hybrid circuit further comprises a bias gain circuit;
(e) the first variable resistor, the second variable resistor, the third variable resistor, and the fourth variable resistor are polysilicon variable resistors.

15. A method of providing a hybrid current by a scalable proportional to absolute temperature (PTAT) hybrid circuit, comprising:

providing a zero temperature coefficient (ZTC) current;
generating, based on the ZTC current, a PTAT current with a slope having a non-zero value;
providing a reference voltage to alter the PTAT current by at least scaling the PTAT current or changing the slope of the PTAT current to generate an altered PTAT current; and
outputting a larger current of the ZTC current and the altered PTAT current as a hybrid current.

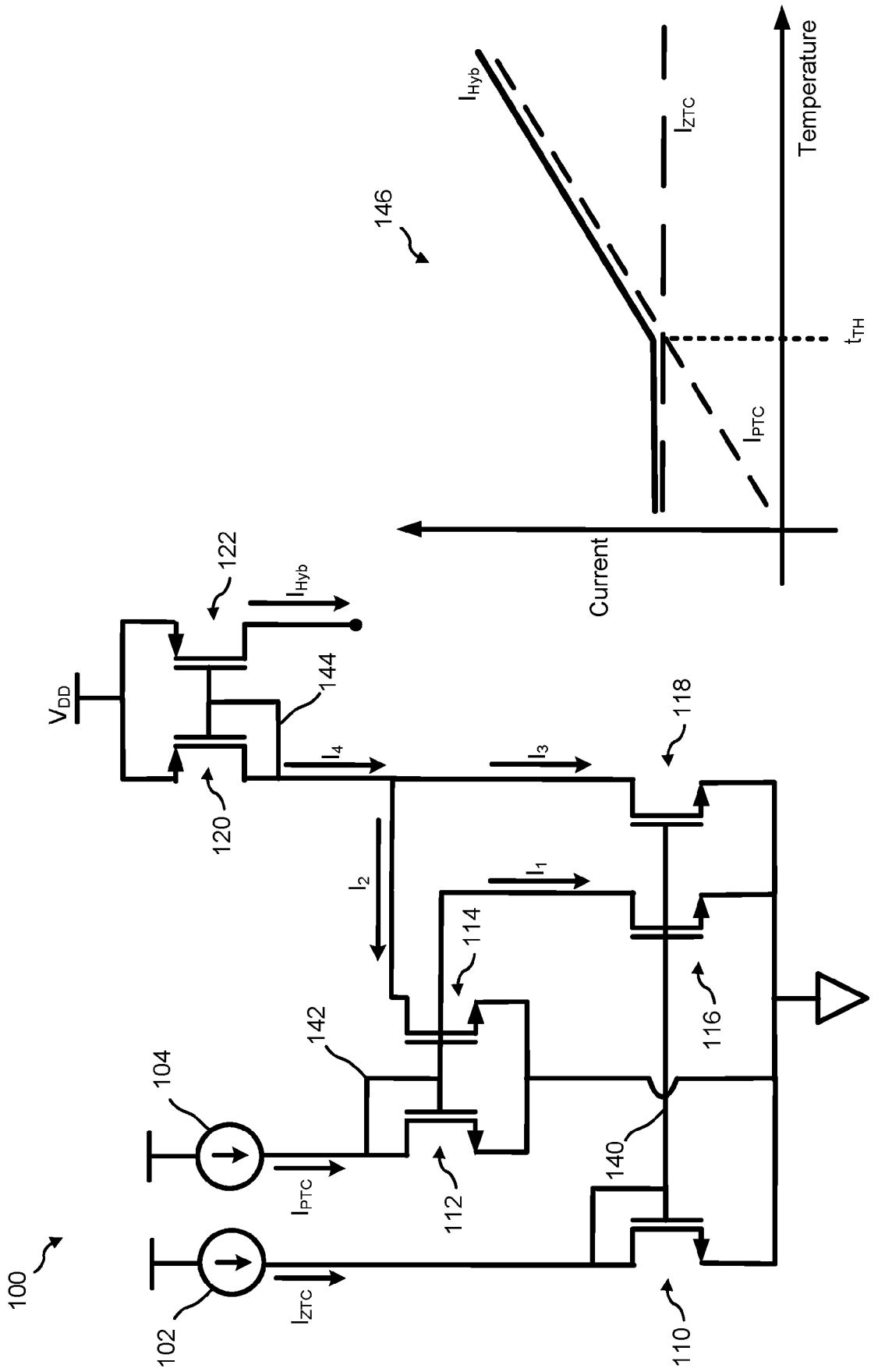
100
102
104
110
112
114
116
118
120
122
140
142
144
146
V_{DD}
I_{PTC}
I_{ZTC}
I_{Hyb}
I_1
I_2
I_3
I_4
Current
Temperature
t_{TH}

FIG. 1

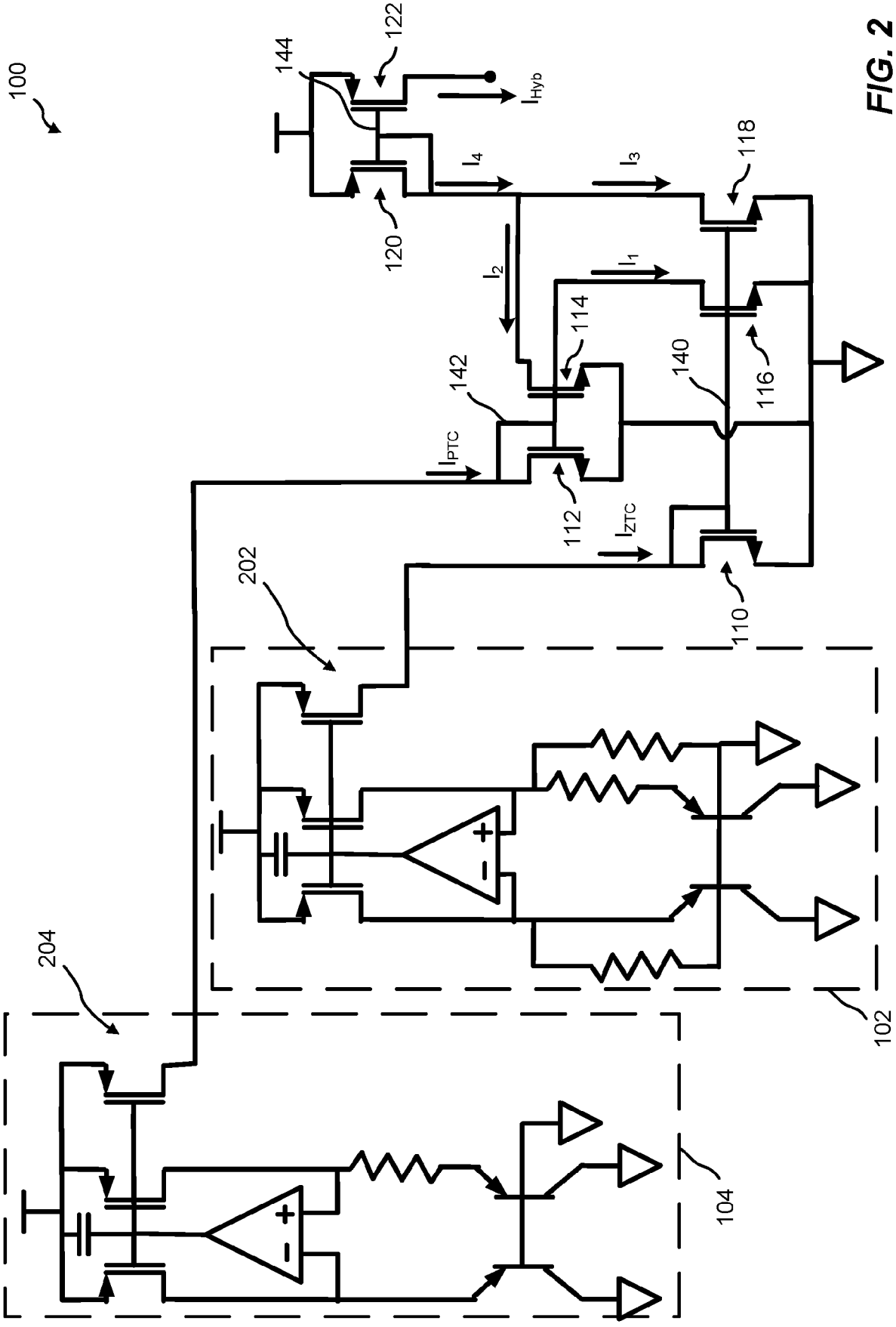
100
144
122
I_{Hyb}
I_4
I_3
118
120
I_2
I_1
114
142
140
116
I_{PTC}
112
I_{ZTC}
110
202
204
102
104

FIG. 2

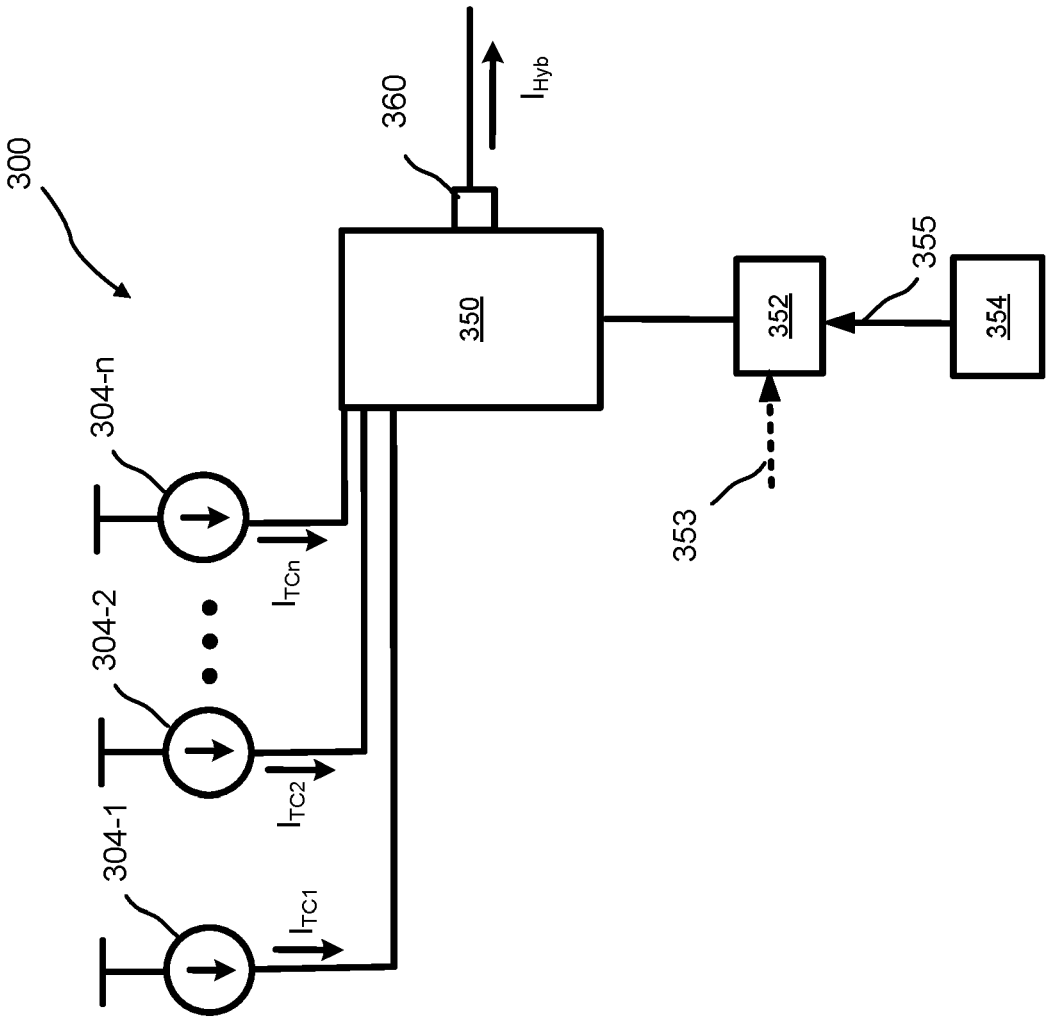

FIG. 3

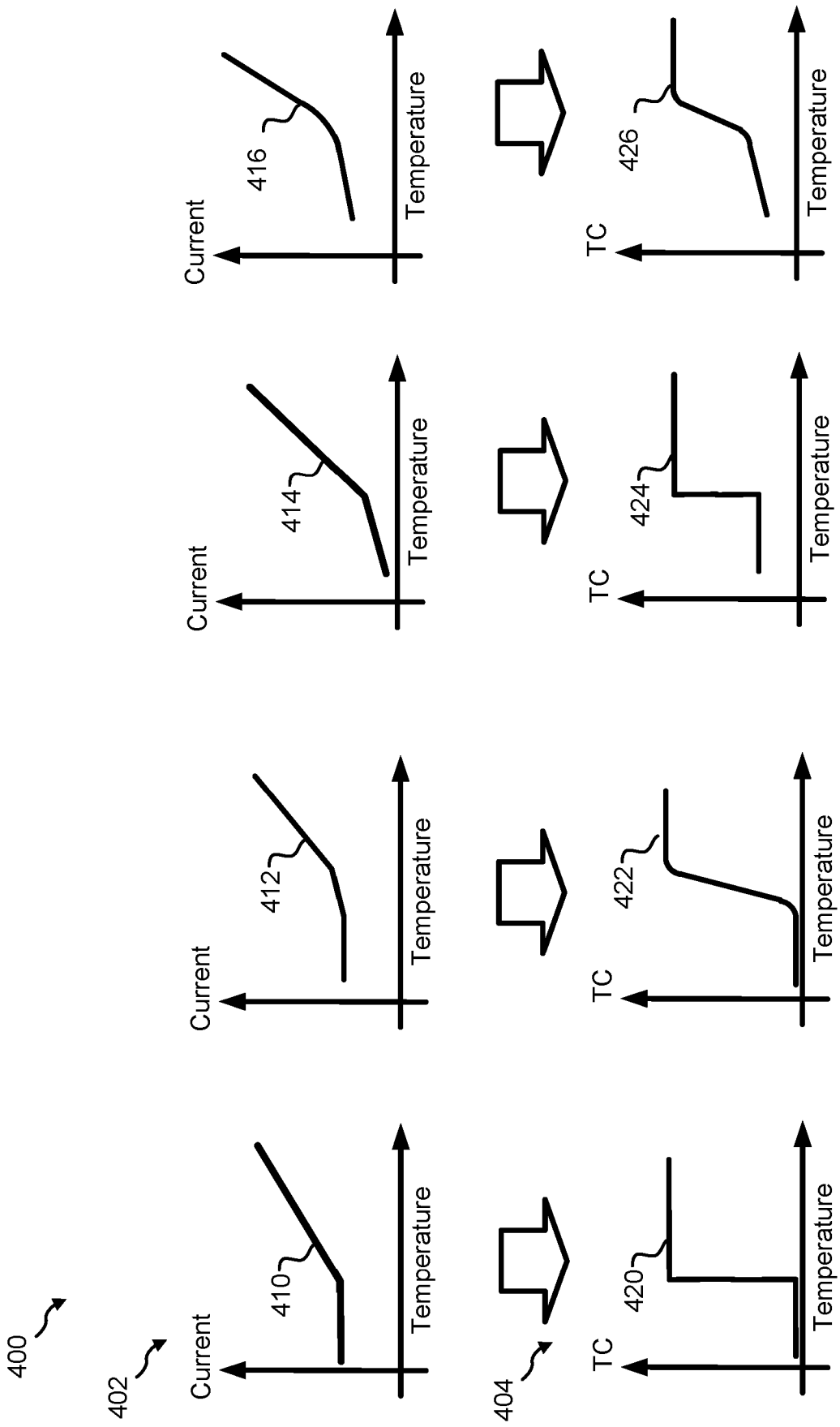
400
402
404
Current
Temperature
410
412
414
416
TC
420
422
424
426

FIG. 4

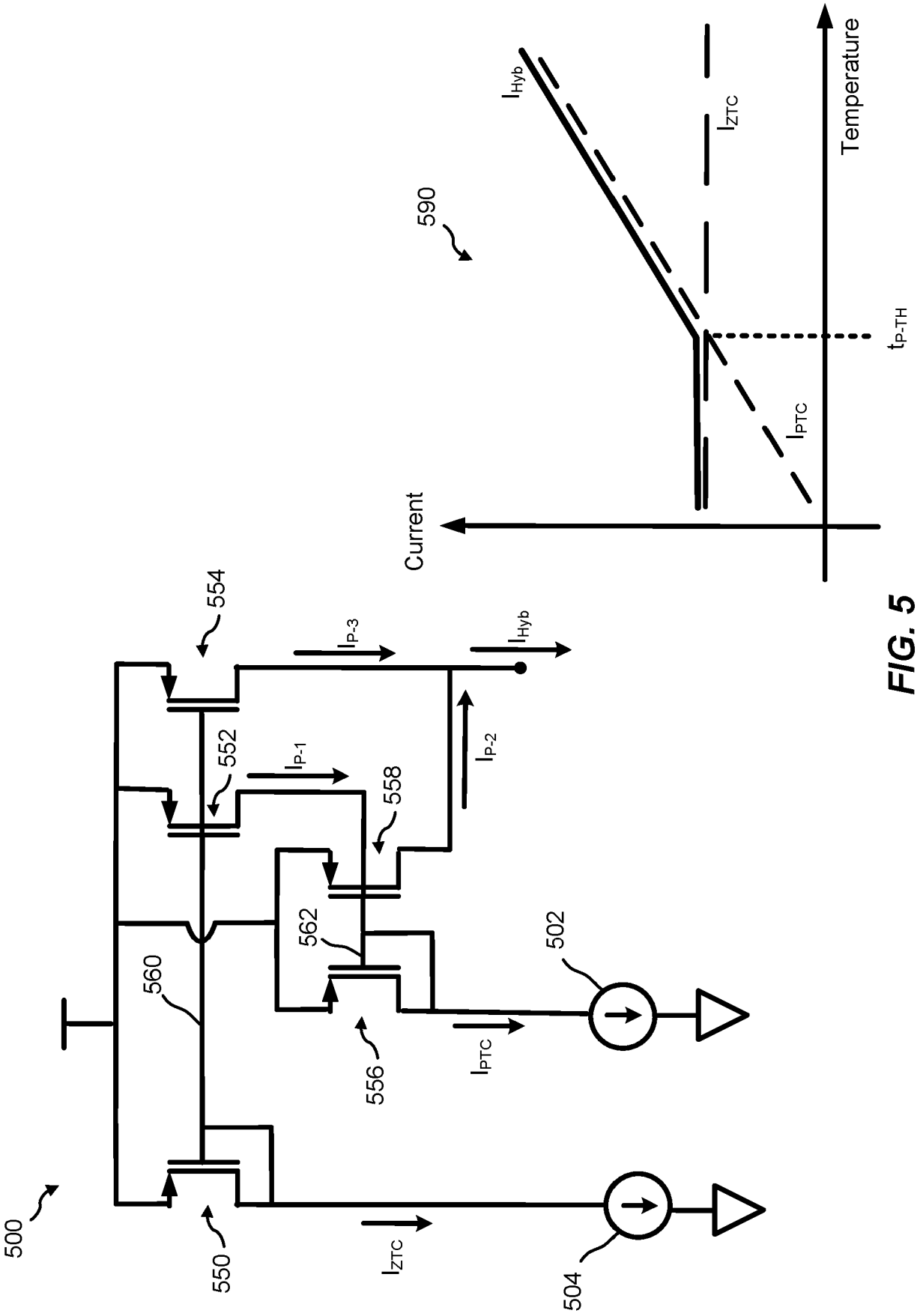
500
550
552
554
556
558
560
562
502
504
590
I_{P-1}
I_{P-2}
I_{P-3}
I_{Hyb}
I_{ZTC}
I_{PTC}
Current
Temperature
t_{P-TH}

FIG. 5

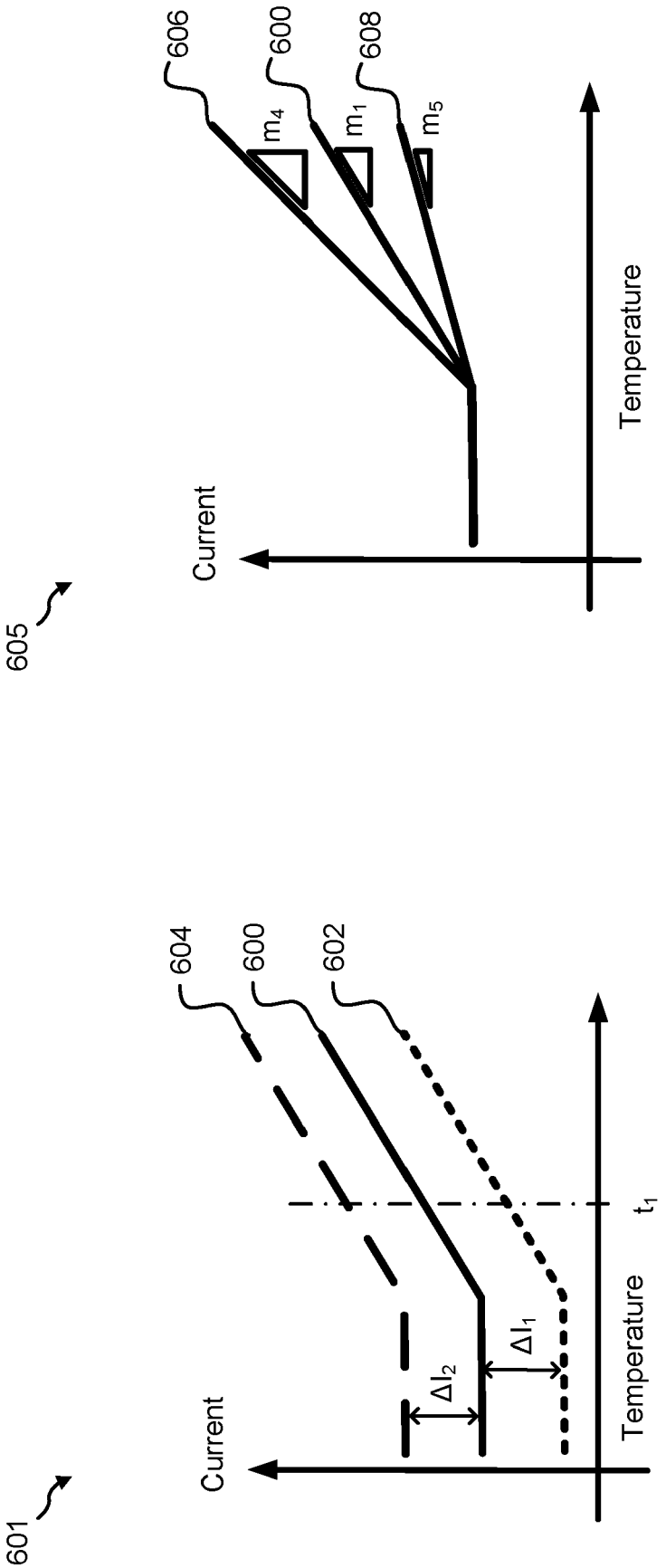
606
600
608
m_4
m_1
m_5
Current
Temperature
605
604
600
602
t_1
ΔI_2
ΔI_1
Current
Temperature
601

FIG. 6

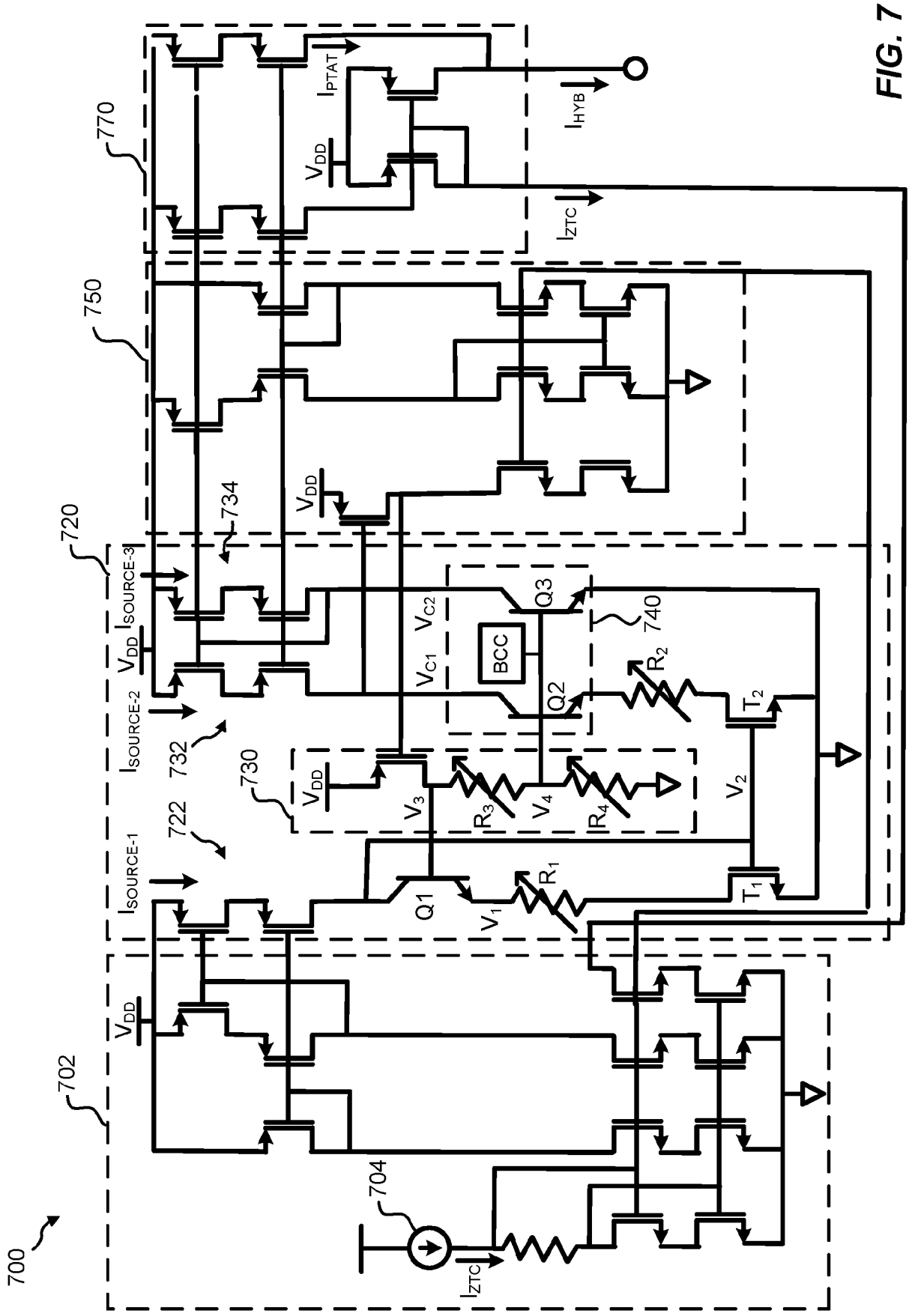
700
702
704
720
722
730
732
734
740
750
770
$I_{SOURCE-1}$
$I_{SOURCE-2}$
$I_{SOURCE-3}$
I_{PTAT}
I_{HYB}
I_{ZTC}
V_{DD}
V_{C1}
V_{C2}
V_1
V_2
V_3
V_4
R_1
R_2
R_3
R_4
T_1
T_2
Q1
Q2
Q3
BCC

FIG. 7

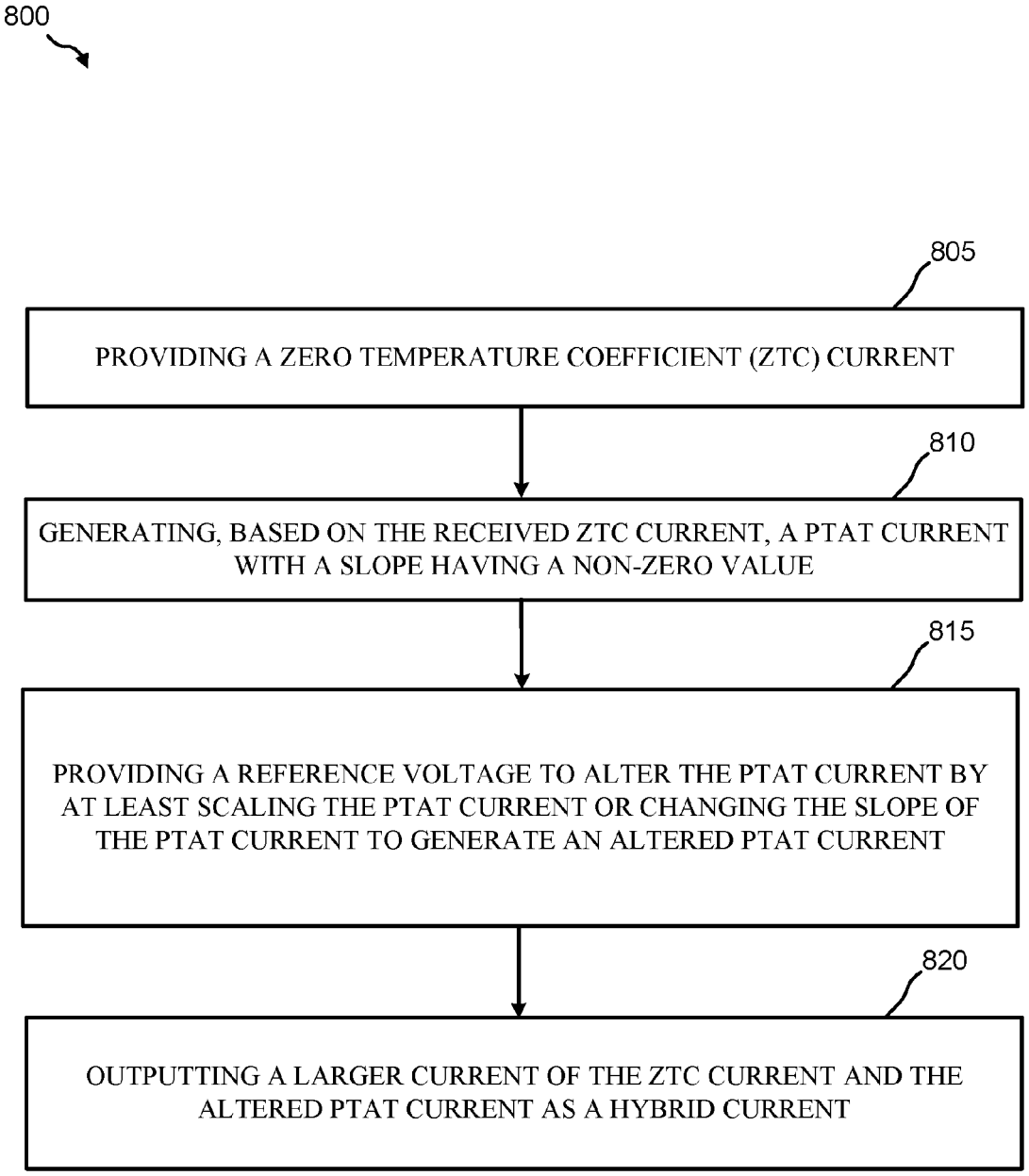
800
805
PROVIDING A ZERO TEMPERATURE COEFFICIENT (ZTC) CURRENT
810
GENERATING, BASED ON THE RECEIVED ZTC CURRENT, A PTAT CURRENT WITH A SLOPE HAVING A NON-ZERO VALUE
815
PROVIDING A REFERENCE VOLTAGE TO ALTER THE PTAT CURRENT BY AT LEAST SCALING THE PTAT CURRENT OR CHANGING THE SLOPE OF THE PTAT CURRENT TO GENERATE AN ALTERED PTAT CURRENT
820
OUTPUTTING A LARGER CURRENT OF THE ZTC CURRENT AND THE ALTERED PTAT CURRENT AS A HYBRID CURRENT

FIG. 8

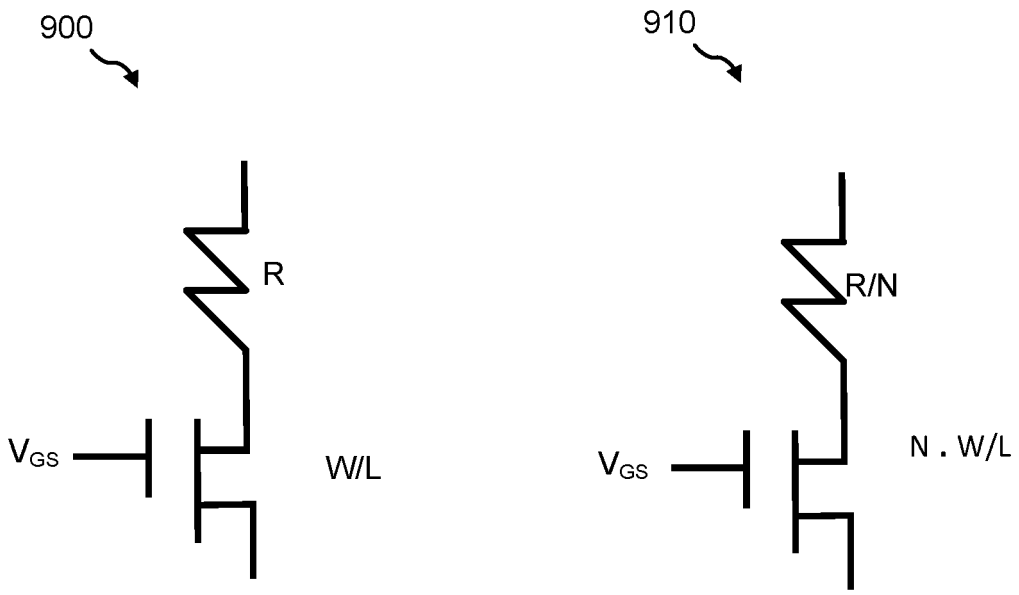

FIG. 9

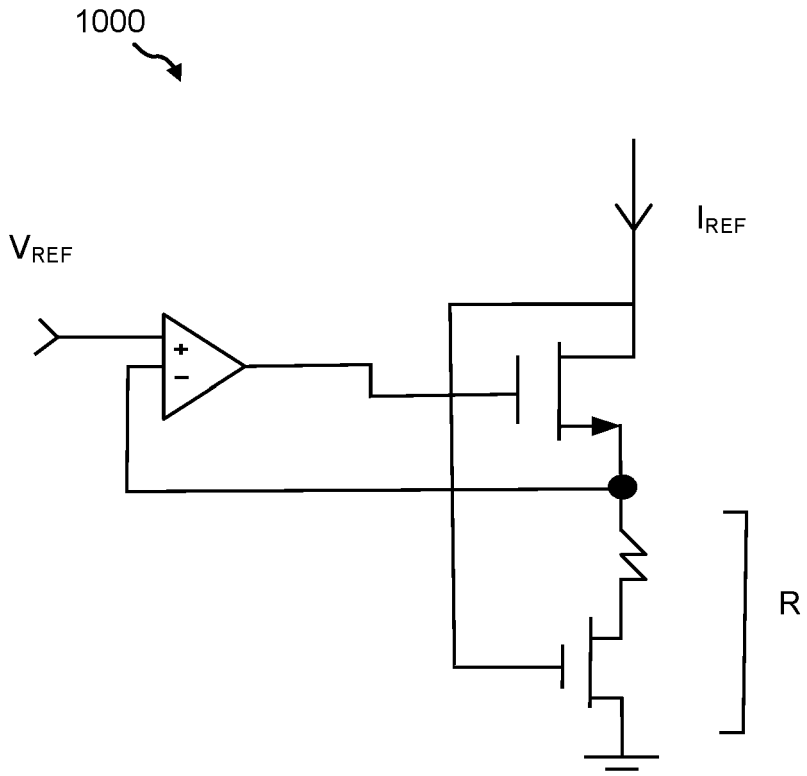

FIG. 10

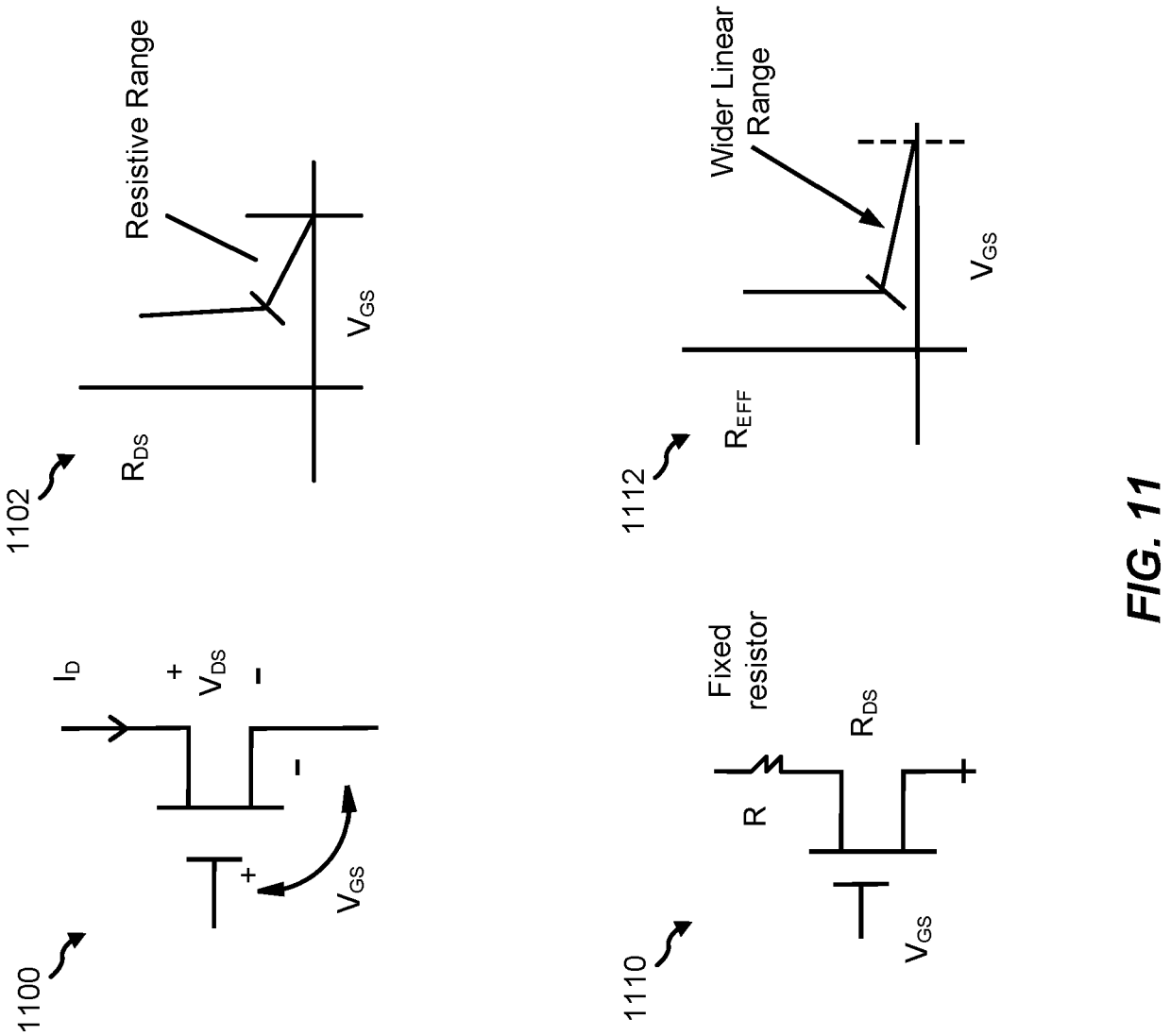
1100
I_D
+
V_{DS}
-
-
+
V_{GS}
1102
Resistive Range
R_{DS}
V_{GS}
1110
Fixed resistor
R
R_{DS}
V_{GS}
1112
Wider Linear Range
R_{EFF}
V_{GS}

FIG. 11

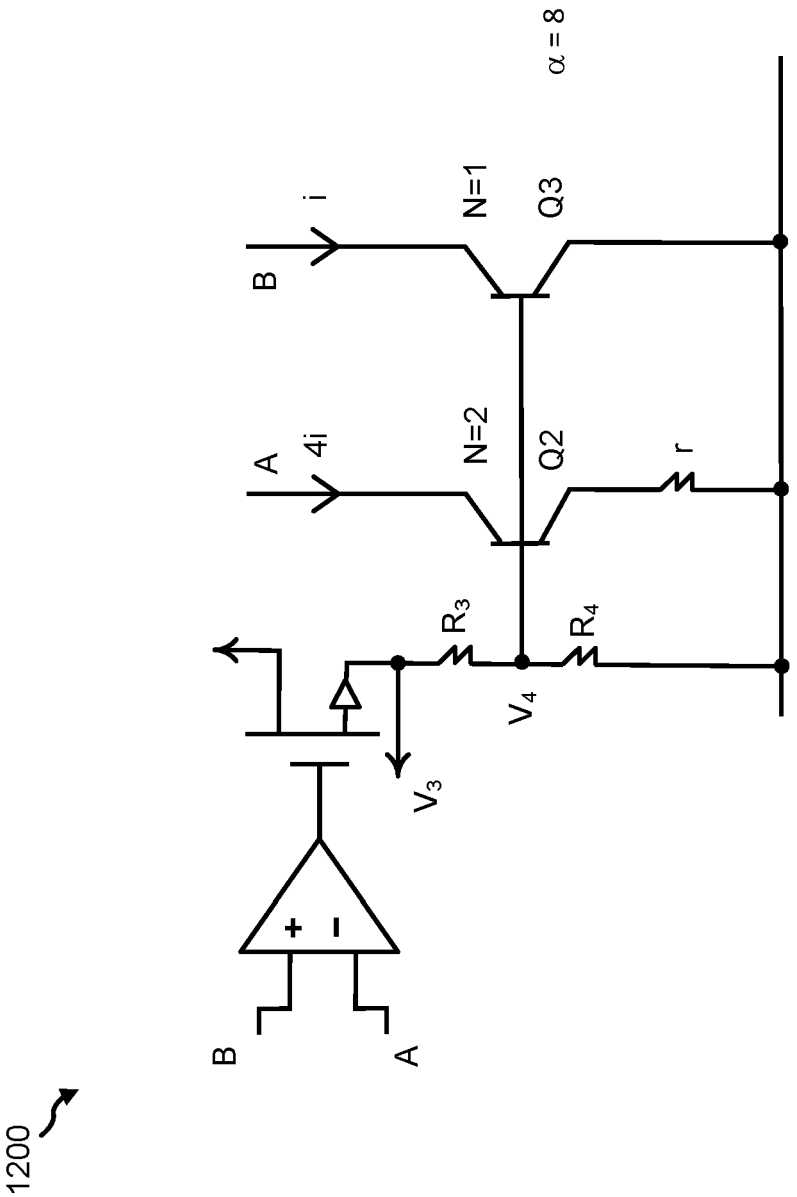

FIG. 12

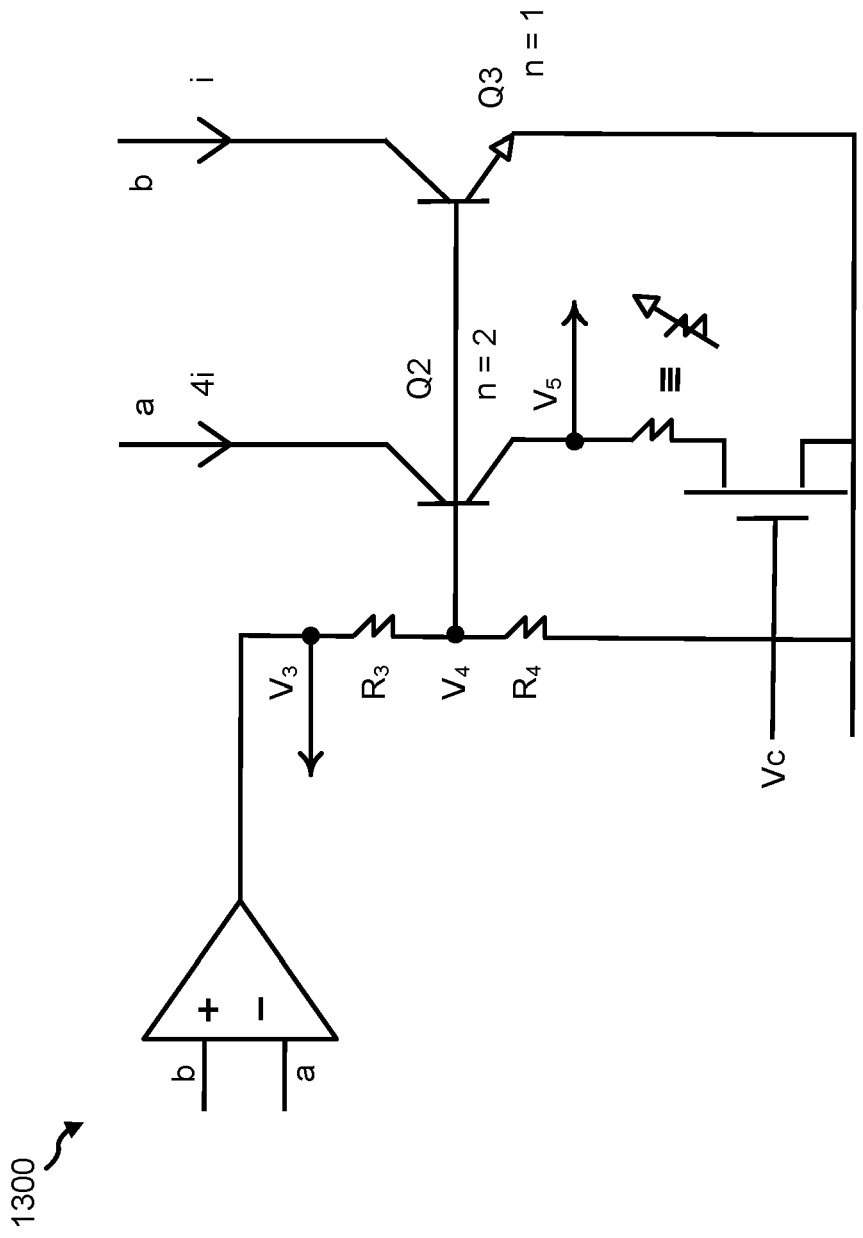

FIG. 13